Course: UESTC3020
Names (in Pinyin)**:**
GUID:
Date: 12 January 2024

These 5 lines should not be removed. You should add the name and GUID of all members of the group.

UESTC Coursework Report

This file is the template to adhere to for the VHDL coursework report that must be submitted before **Sunday 12th January 2024, 23.00**. Submission on Moodle only. If the report is submitted late, standard University of Glasgow penalty regulations will be applied.

The report should have a maximum of **five** (**5**) pages, without counting appendices containing VHDL codes. The six pages should be organised as follow:

- **The first three pages (pages #1 to 3) should only contain text for Part II and Part III** (no figure allowed)**.**
- **The last two pages (pages #4 and #5) should only contain figures for Part II and Part III (no text allowed on these two pages)**.

The report presentation must be professional, but you do not have to add a Table of Contents (due to space restrictions) or an abstract.

The report should present the work you have done to complete the design, the simulations to prove your design is working as expected (the simulation set-up is critical, and you should justify why you choose specific input values) and justify your decisions (both design and simulations).

The most important point is the justification of your decisions. Your expected added value is to make informed decisions after considering all relevant aspects of the design. Justifying or analysing results is not the same as describing the results.

The presentation of the report should respect **exactly** the presentation of this template. The font is *calibri*, size 11pt, line spacing is 1.15 and the margins are: left = 1.75cm, right = 1.75cm, top = 1.5cm and bottom = 2cm. The length of the report should not exceed six pages (**this is a strict limit**). If the report has a 7th page (before the start of the Appendix) or does not follow this template, a penalty will be applied. No abstract or table of contents needed.

The report is marked out of 15. The breakdown of the mark is as follow:

- Part II, combinational in VHDL: **out of 3**;
- Part III, sequential and overall system: **out of 9**;
- Report presentation: **out of 3**; (if the template is not adhered to and/or the report is longer than 5 pages and/or does not respect the breakdown listed above, the mark for report presentation will be reduced to 0)

For each sub-part of Part II and Part III, the grades will be given based on:

- Quality of VHDL coding and/or design.
- Correction of simulations.
- Quality of explanation and justification (you must justify your decisions).

The last point being the most important criterion.

For the submission, only one student per group has to submit (Moodle should be configured by groups so any submission from one student will also appear for the second student in the group). You are expected to upload three files:

- The report combining Part I, Part II and Part III. The format of the file must be 'pdf'.
- The Xillinx project including all the relevant VHDL codes. **The format must be compressed 'zip'**.

Two different links will be available on Moodle. Be careful to submit the correct file to the correct link. The links for the last two files will only accept 'pdf' and 'zip' respectively, so be careful to prepare the documents under the right format.

As a reminder:

The template must be adhered to the point. If not, penalty would be applied.

You can remove the instruction on this page. Apart from the 5/6 lines at the start, you can remove the rest about the formatting (font type and size, margin, etc) should be as mentioned in the text. A template without the instructions is also available on Moodle.

As for all your work, collusion and plagiarism are not allowed. The work submitted must be your group work and your group work only. If any suspicious of collusion/plagiarism is detected, your submission will be reported to UofG Senate following UofG regulations.

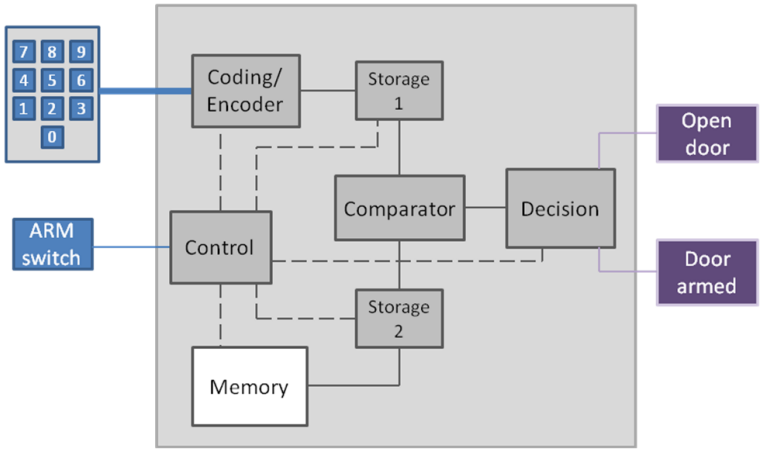

Figure 1: Example of figure

Appendix A: VHDL Codes

This section is to provide the VHDL codes you have written. No text to be added (but you should have comments in your code).

The appendix is not part of the 6-page count. But if any text other than VHDL code is added in appendix, it will not be counted toward the final grade for this report.