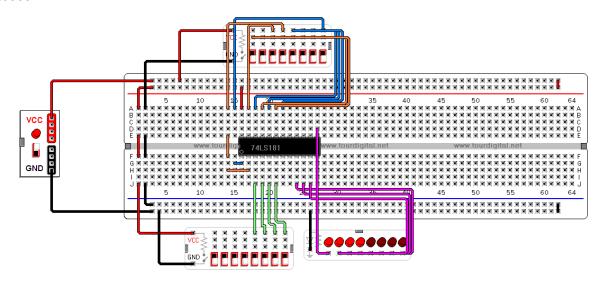
Marcos Ani Cury Vinagre Silva - 684903 / Terceiro Período Relatório 2 de Arquitetura de Computador 2

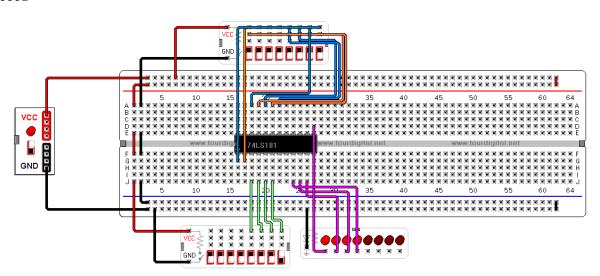
1) Tabela ULA

А	В	C	D	E	F	G	H		J	K	L	M	N	0	P	Q
S=	0000.	0001.	0010.	0011.	0100.	0101.	0110.	0111.	1000.	1001.	1010.	1011.	1100.	1101.	1110.	1111.
A=0000	1111.	1111.	0000.	0000.	1111.	1111.	0000.	0000.	1111.	1111.	0000.	0000.	1111.	1111.	0000.	0000.
B=0000																
A=0001	1110.	1110.	0000.	0000.	1110.	1110.	0000.	0000.	1111.	1111.	0001.	0001.	1111.	1111.	0001.	0001.
B=0001																
A=0100	1011.	1011.	0000.	0000.	1011.	1011.	0000.	0000.	1111.	1111.	0100.	0100.	1111.	1111.	0100.	0100.
B=0100																
A=1000	0111.	0111.	0000.	0000.	0111.	0111.	0000.	0000.	1111.	1111.	1000.	1000.	1111.	1111.	1000.	1000.
B=1000																

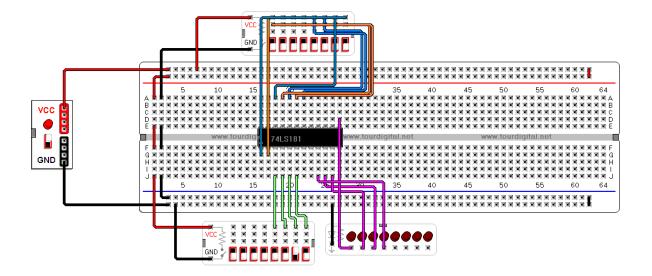
2)0000



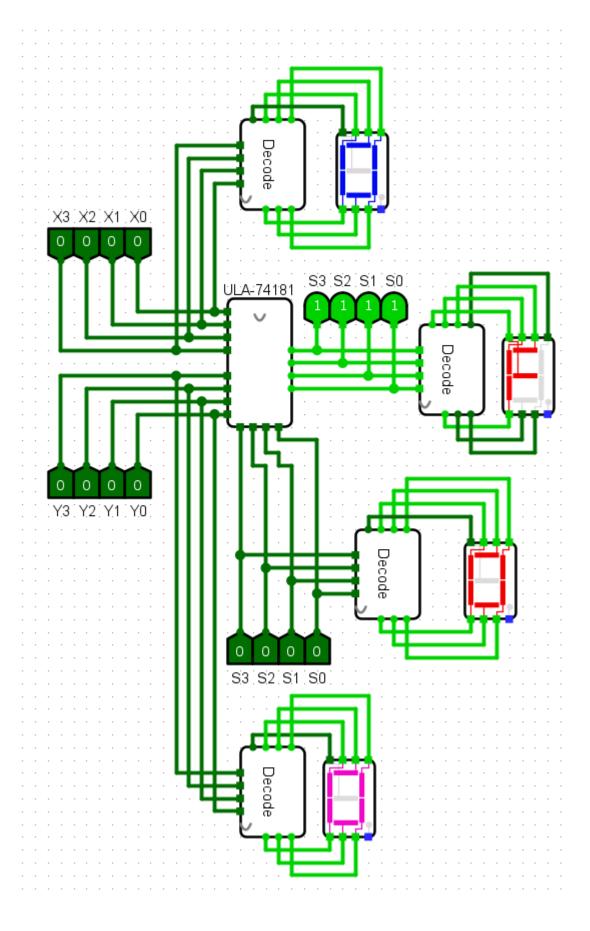
0001

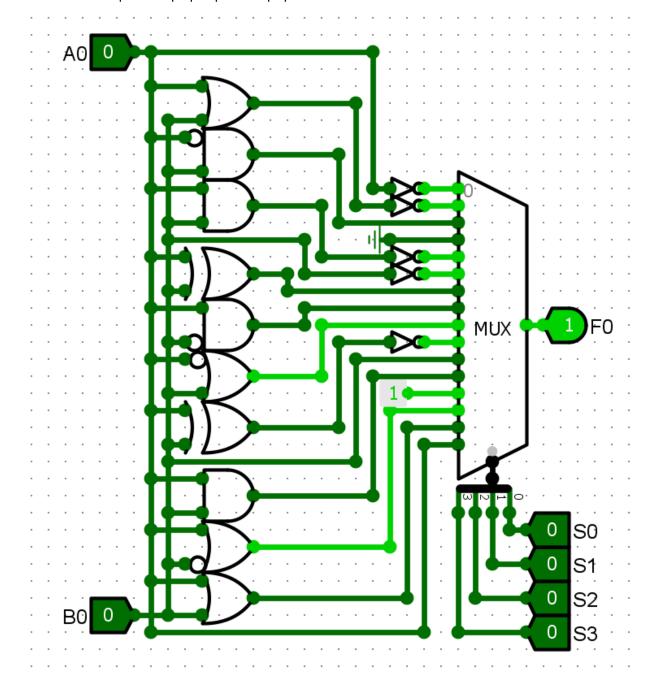


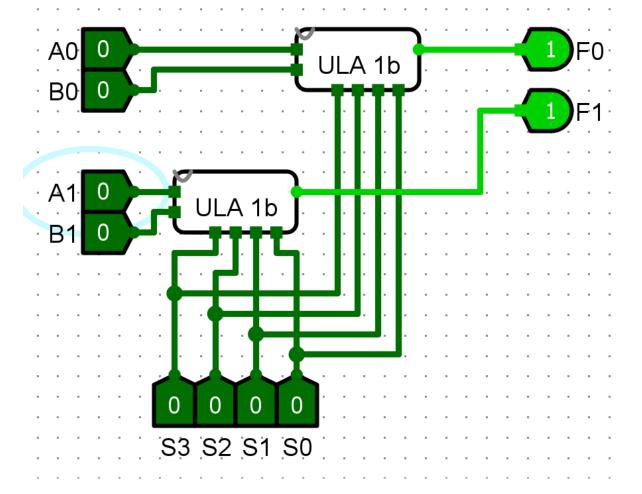
0010

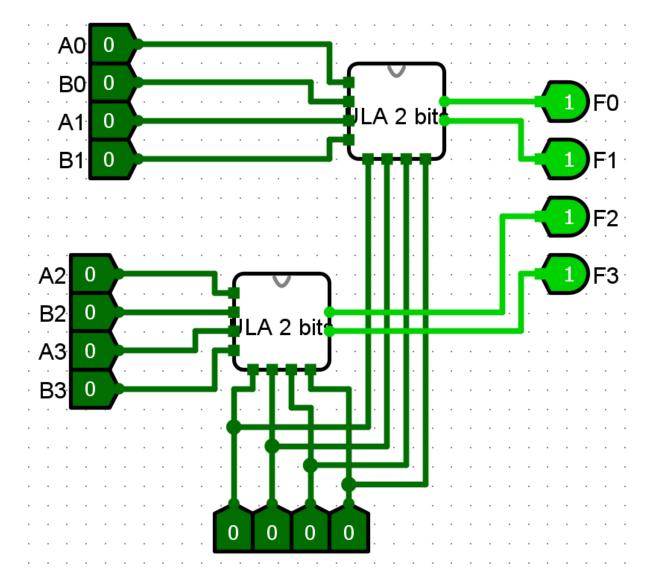


3)Parte principal

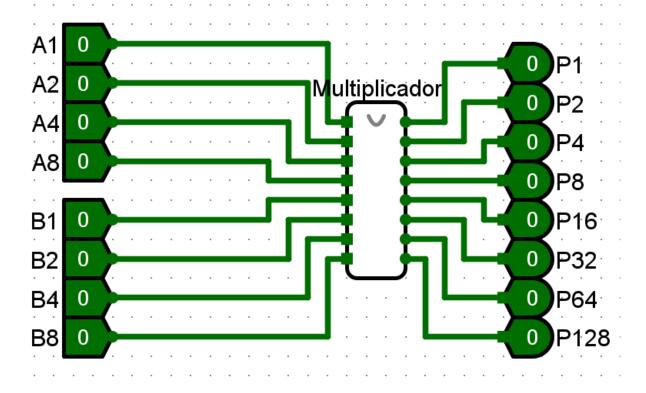








4)Parte principal do multiplicador



5)Parte interna do circuito

