

Relatório – Laboratório de ac2

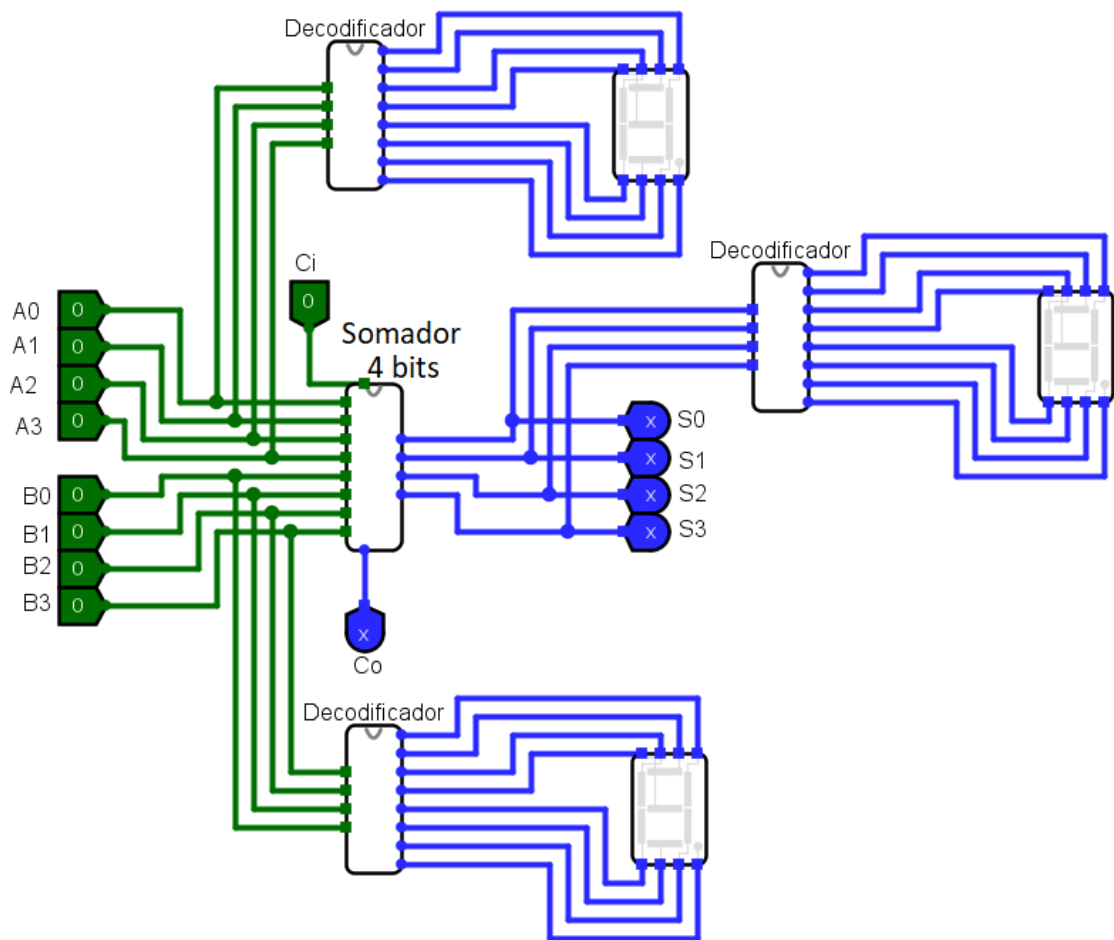
Aula número: 2

Objetivo: Identificar os circuitos integrados/portas lógicas. Utilização do simulador de protoboard para elaboração de circuitos e comprovação através de simulação lógica.

Neste relatório iremos implementar uma calculadora que some números em hexadecimal. Poderemos ver as parcelas e o valor da soma.

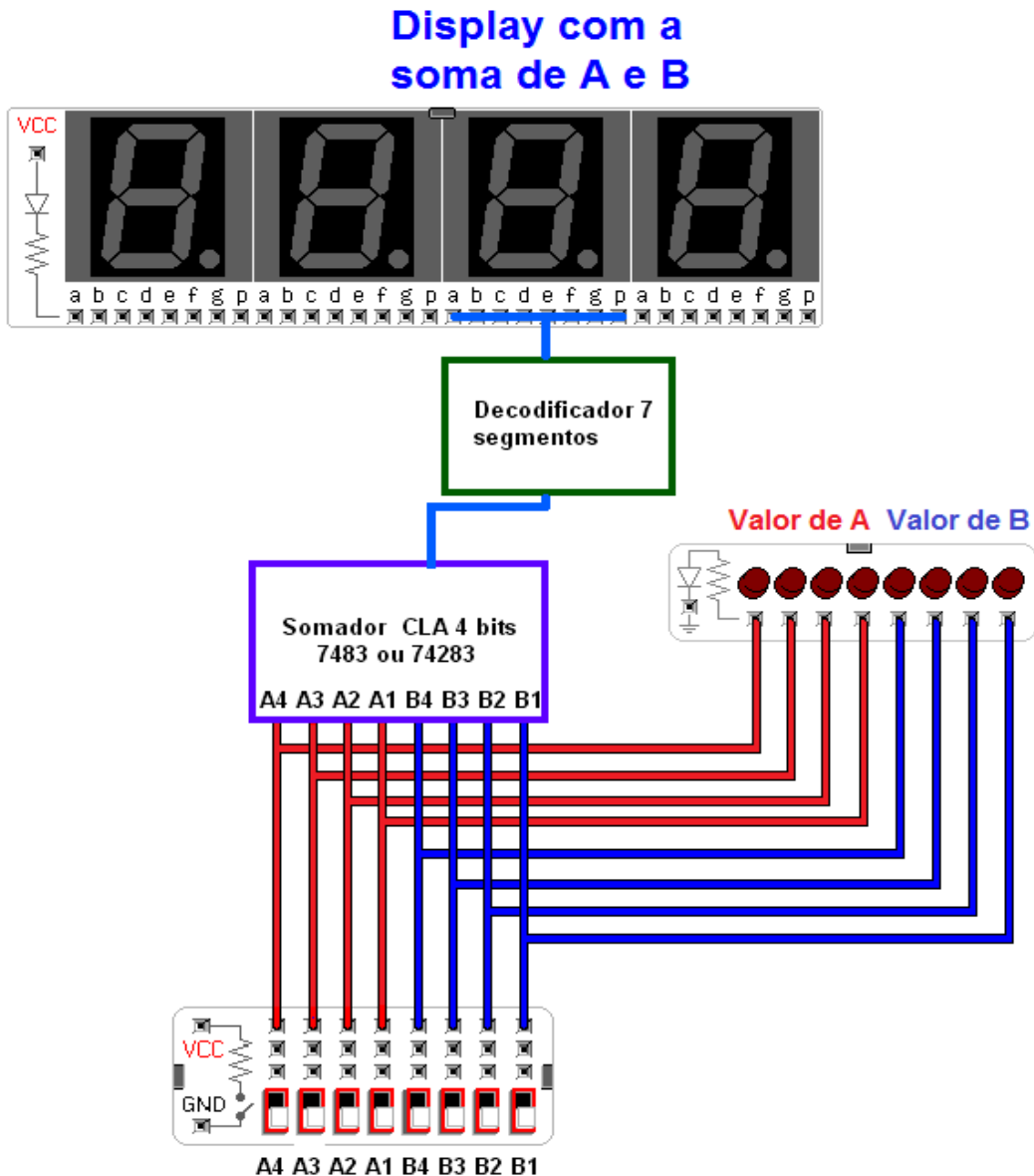
Experiência:

1. Uma das formas de se tornar as somas mais velozes é através do CLA.
2. Inicialmente iremos construir um circuito que some dois números através do somador completo de 4 bits construído na aula anterior e em um passo seguinte, substituir este somador por um somador CLA de 4 bits e avaliar a soma em um display de 7 segmentos. Em um primeiro momento você deverá construir todo o circuito no Logisim usando subcircuitos conforme o circuito abaixo:



Você deverá construir no logisim o decodificador de 4 bits para 7 segmentos do display.

3. Após testar o funcionamento, você deverá elaborar um circuito com o CLA. Procure utilizar um dos circuitos CLA cujos datasheets estão ao final deste relatório. Após construir o subcircuito no Logisim, você deverá substituir o somador de 4 bits original por este que você acabou de construir e verificar o funcionamento.
4. Agora monte o mesmo circuito no Simulador 97 conforme ilustrado abaixo. Use o circuito integrado do CLA. Simule a entrada através de chaves, serão 4 chaves para o dado A e quatro chaves para o dado B, procure seguir a figura a seguir para a sua montagem. Use o Display apenas para o resultado da soma, não é necessário um para cada dado da entrada conforme a montagem no logisim, use leds no caso das entradas.



5. Para a montagem no simulador de protoboard você deverá utilizar o chip 7483 ou 74283. Use os datasheets anexados a esse relatório para descobrir como os chips funcionam (olhe a tabela verdade para descobrir a função de cada pino).

Cuidado os 2 somadores executam a mesma função. A única diferença entre eles (7483 e 74283) é a distribuição dos pinos.

Escolha apenas um deles para a sua montagem, aquele que melhor se adapte à sua configuração de entradas e saídas.

6. O que apresentar para esse relatório:
 - O gif/jpg dos circuito projetados no logisim. (a calculadora completa e o circuito do CLA).
 - O gif/jpg do Jbreadboard ou simulador_97 com alguns testes realizados.

Obs:

- 1) Existe um decodificador chips 7447 ou 74247, teste ambos para verificar se poderão ser utilizados nesse circuito. Observe os pinos a serem conectados, se funcionam com níveis altos ou baixos na saída e que principalmente esse decodificador se presta apenas à decodificação BCD display de 7 segmentos (**não é hexadecimal para display de 7 segmentos**).
- 2) Para sua montagem, use inicialmente LEDS para testar se as ligações do somador estão corretas e o resultado da soma está OK, só então conecte o decodificador e o display.

Anexos:

Datasheet de diversos somadores (7483 e 74283) e dos decodificadores (7447 e 74247)..

HD74HC83

4-Bit Binary Full Adder (with Fast Carry)

HITACHI

Description

This improved full adder performs the addition of two 4-bit binary numbers. The sum () output are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit.

This adder features full internal look ahead across all four bit generating the carry term in ten nanoseconds typically.

This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

Features

- High Speed Operation: $t_{pd} (A_i \text{ or } B_i \text{ to } Z_i) = 16 \text{ ns typ } (C_L = 50 \text{ pF})$
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: $1 \mu\text{A max}$
- Low Quiescent Supply Current: $I_{CC} (\text{static}) = 4 \mu\text{A max } (T_a = 25^\circ\text{C})$

HD74HC83

Function Table

Inputs				Outputs					
				When $C_0 = L$ /When $C_2 = L$			When $C_0 = H$ /When $C_2 = H$		
A_1/A_3	B_1/B_3	A_2/A_4	B_2/B_4	Σ_1/Σ_3	Σ_2/Σ_4	C_2/C_4	Σ_1/Σ_3	Σ_2/Σ_4	C_2/C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H : High level

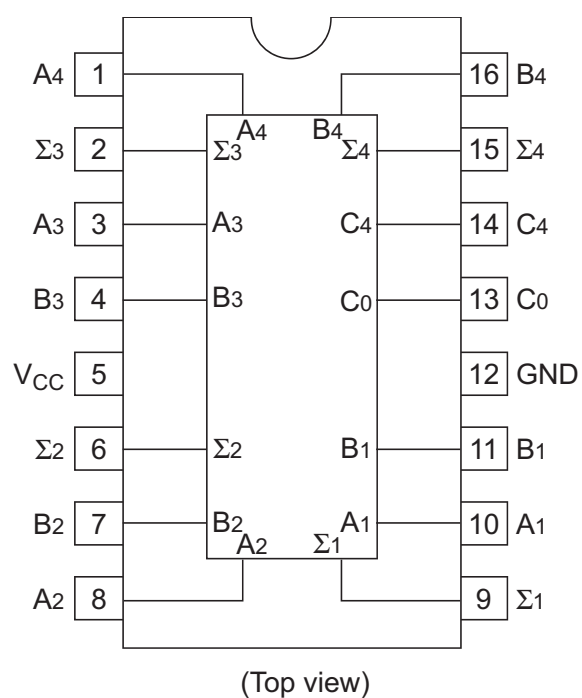
L : Low level

X : Irrelevant

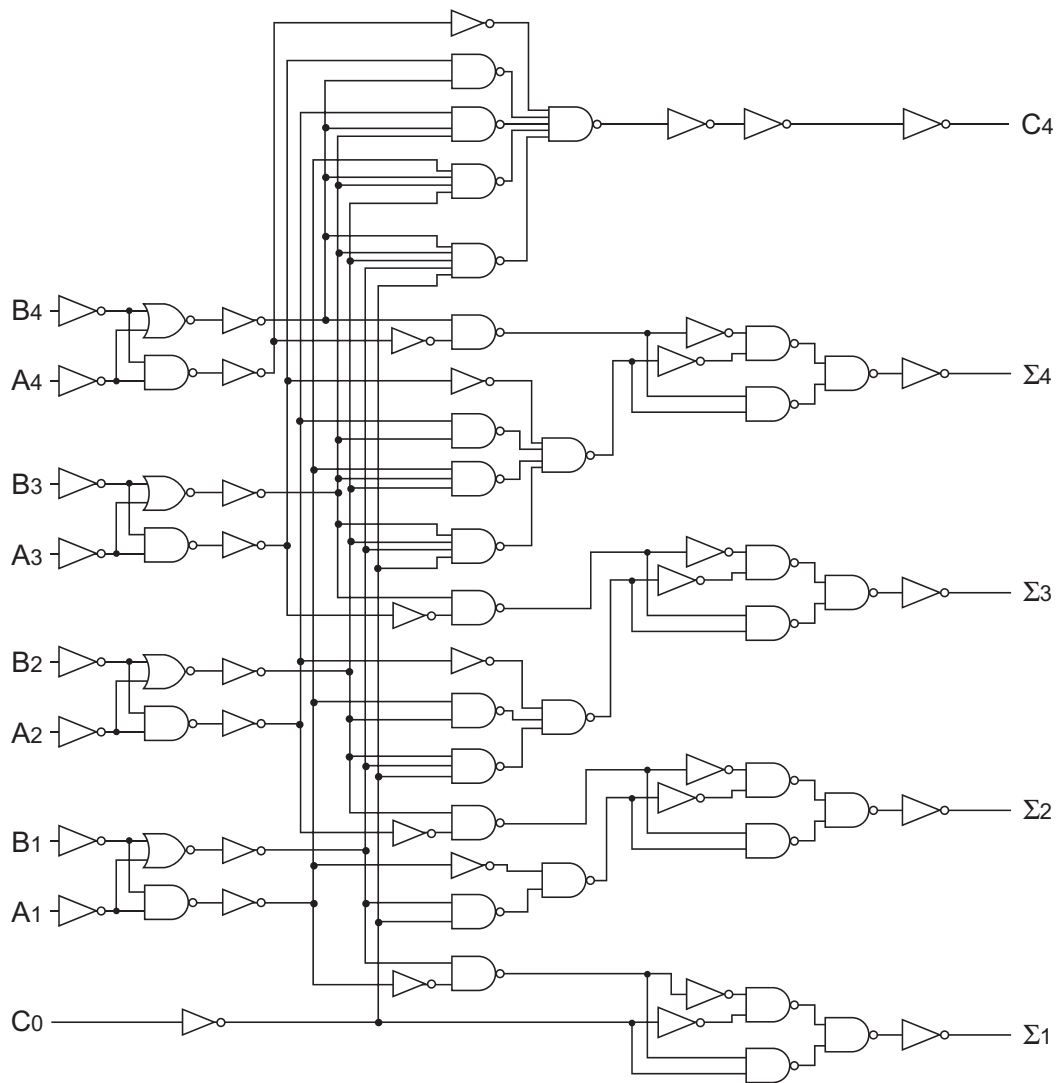
Note: Input conditions at A_1 , B_1 , A_2 , B_2 and C_0 are used to determine outputs Σ_1 and Σ_2 and the value of the internal carry C_2 .

The value at C_2 , A_3 , B_3 , A_4 and B_4 are then used to determine outputs Σ_3 , Σ_4 and C_4

Pin Arrangement



Block Diagram (1//2)

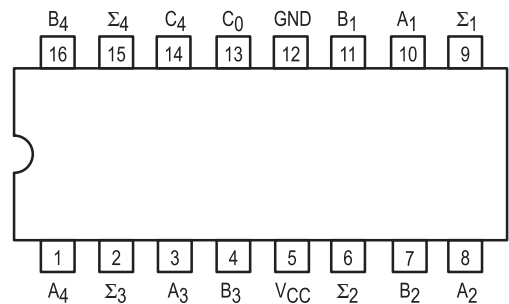


HITACHI

4-BIT BINARY FULL ADDER WITH FAST CARRY

The SN54/74LS83A is a high-speed 4-Bit binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1-A_4 , B_1-B_4) and a Carry Input (C_0). It generates the binary Sum outputs $\Sigma_1-\Sigma_4$ and the Carry Output (C_4) from the most significant bit. The LS83A operates with either active HIGH or active LOW operands (positive or negative logic). The SN54/74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

A_1-A_4	Operand A Inputs
B_1-B_4	Operand B Inputs
C_0	Carry Input
$\Sigma_1-\Sigma_4$	Sum Outputs (Note b)
C_4	Carry Output (Note b)

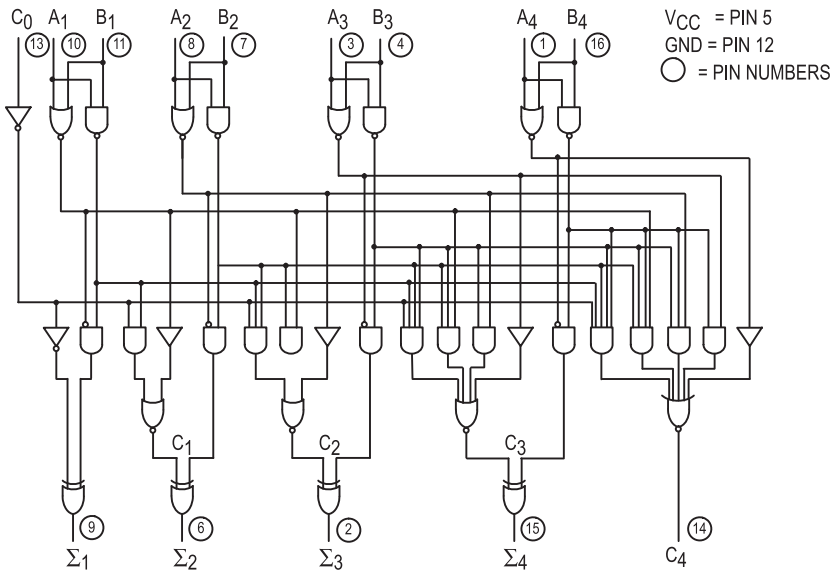
LOADING (Note a)

HIGH	LOW
1.0 U.L.	0.5 U.L.
1.0 U.L.	0.5 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.
10 U.L.	5 (2.5) U.L.

NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

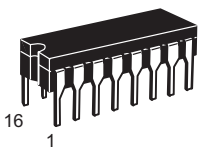


V_{CC} = PIN 5
GND = PIN 12
○ = PIN NUMBERS

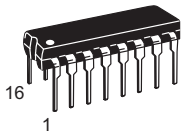
SN54/74LS83A

4-BIT BINARY FULL ADDER WITH FAST CARRY

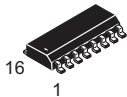
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-08



N SUFFIX
PLASTIC
CASE 648-08

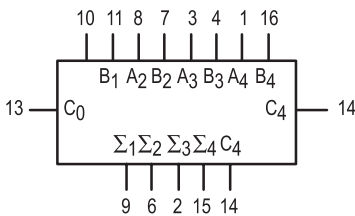


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



SN54/74LS83A

FUNCTIONAL DESCRIPTION

The LS83A adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_4) outputs.

$$C_0 + (A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH Inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C ₀	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ_1	Σ_2	Σ_3	Σ_4	C ₄	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6 = 12)

Interchanging inputs of equal weight does not affect the operation, thus C₀, A₁, B₁, can be arbitrarily assigned to pins 10, 11, 13, etc.

FUNCTIONAL TRUTH TABLE

C (n-1)	A _n	B _n	Σ_n	C _n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C₁ — C₃ are generated internally
C₀ — is an external input
C₄ — is an output generated internally

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

54LS283/DM54LS283/DM74LS283 4-Bit Binary Adders with Fast Carry

General Description

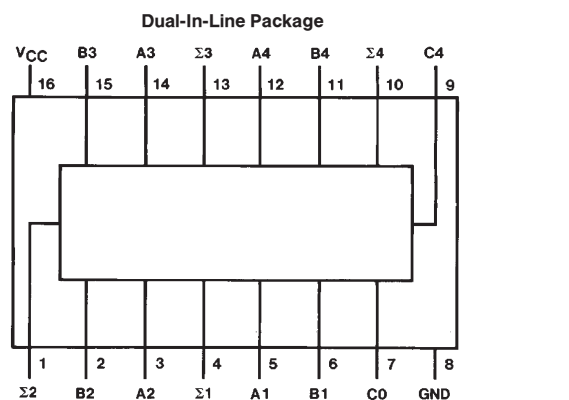
These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
 - Two 8-bit words 25 ns
 - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW
- Alternate Military/Aerospace device (54LS283) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



Order Number 54LS283DMQB, 54LS283FMQB, 54LS283LMQB,
DM54LS283J, DM54LS283W, DM74LS283M or DM74LS283N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\text{ k}\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma 1, \Sigma 2$		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma 1, \Sigma 2$		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma 3$		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma 3$		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma 4$		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma 4$		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to Σ_i		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to Σ_i		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to C4		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to C4		17		26	ns

Function Table

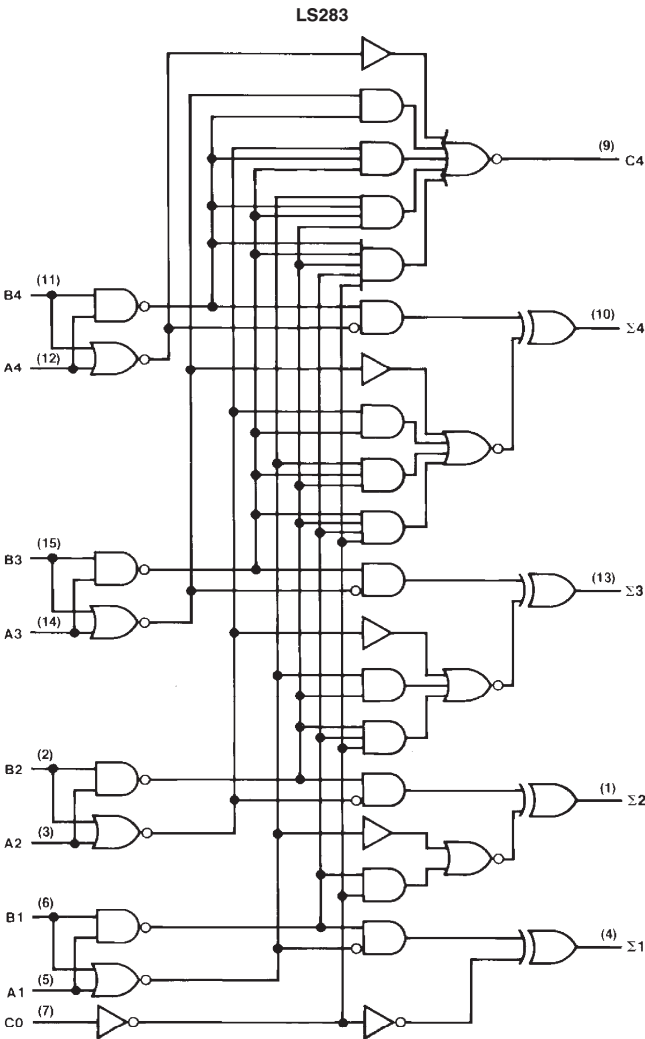
Input				Outputs					
				When C0 = L			When C0 = H		
A1 A3		B1 B3		When C2 = L			When C2 = H		
				$\Sigma 1$	$\Sigma 2$	C2	$\Sigma 1$	$\Sigma 2$	C2
A4	B4	$\Sigma 3$	$\Sigma 4$	C4	$\Sigma 3$	$\Sigma 4$	C4	$\Sigma 3$	$\Sigma 4$
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	L	H
H	L	H	L	H	H	L	L	L	H
L	H	H	L	L	L	H	H	L	H
H	H	H	L	L	H	L	H	H	L
L	L	L	H	L	H	L	L	L	H
H	L	L	H	H	H	L	L	L	H
L	H	L	H	L	L	H	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	L	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

TL/F/6421-3

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs $\Sigma 1$ and $\Sigma 2$ and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs $\Sigma 3$, $\Sigma 4$, and C4.

Logic Diagram



TL/F/6421-2

SN74LS283

4-Bit Binary Full Adder with Fast Carry

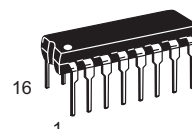
The SN74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1 – A_4 , B_1 – B_4) and a Carry Input (C_0). It generates the binary Sum outputs (Σ_1 – Σ_4) and the Carry Output (C_4) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

GUARANTEED OPERATING RANGES

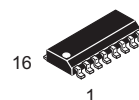
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA



LOW POWER SCHOTTKY



PLASTIC
N SUFFIX
CASE 648



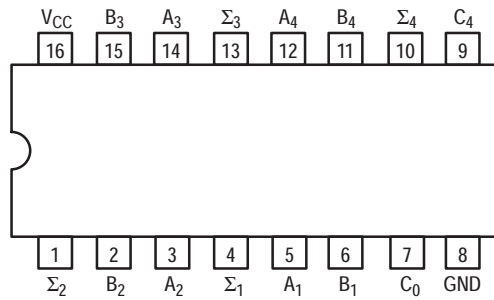
SOIC
D SUFFIX
CASE 751B

ORDERING INFORMATION

Device	Package	Shipping
SN74LS283N	16 Pin DIP	2000 Units/Box
SN74LS283D	16 Pin	2500/Tape & Reel

SN74LS283

CONNECTION DIAGRAM DIP (TOP VIEW)



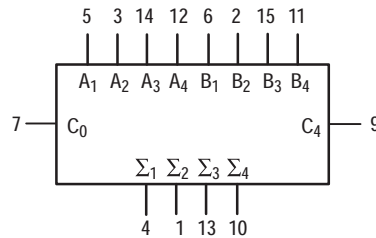
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs	10 U.L.	5 U.L.
C_4	Carry Output	10 U.L.	5 U.L.

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

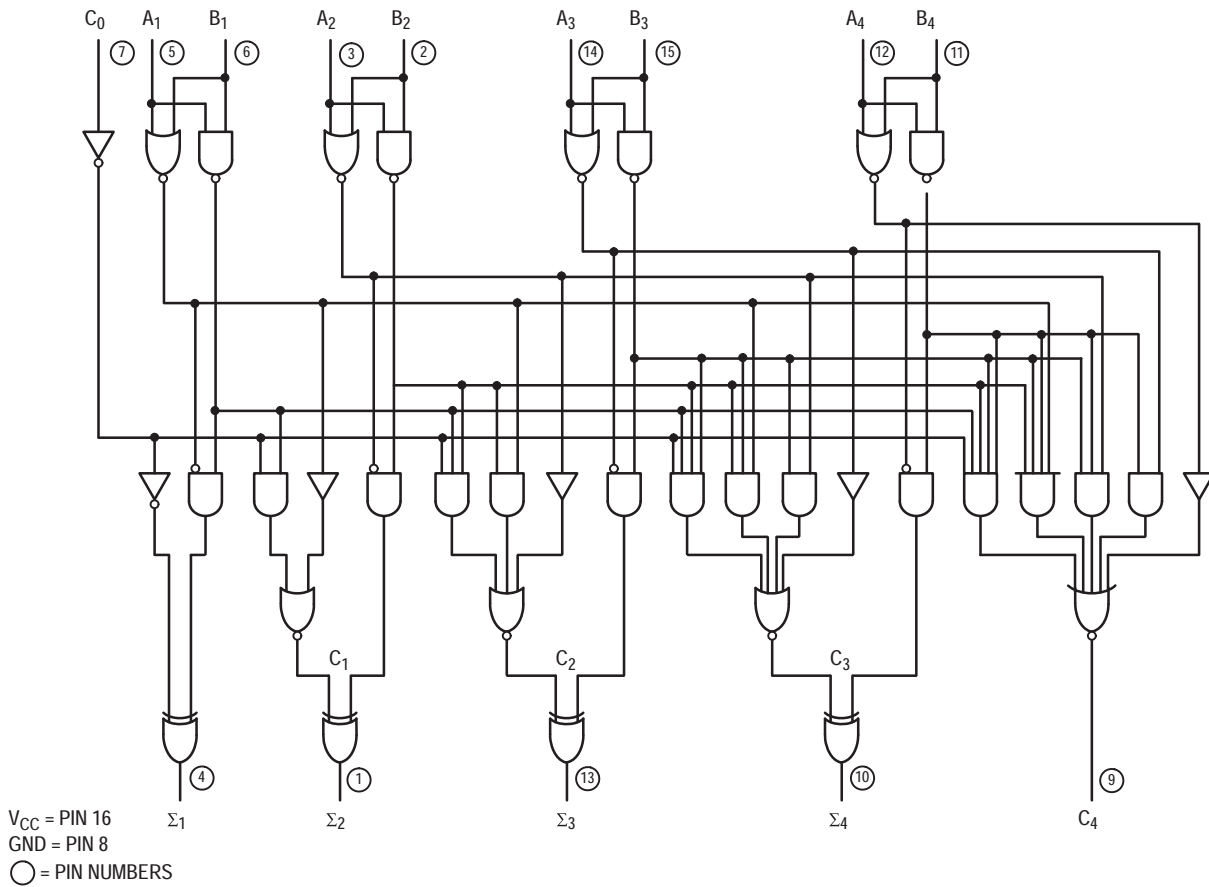
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN74LS283

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS283 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_4) outputs.

$$C_0 + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C ₀	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ ₁	Σ ₂	Σ ₃	Σ ₄	C ₄
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

(10+9=19)

(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C₀, A₁, B₁, can be arbitrarily assigned to pins 7, 5 or 3.

SN74LS283

FUNCTIONAL TRUTH TABLE

C (n-1)	A _n	B _n	Σ _n	C _n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C₁–C₃ are generated internally
C₀ is an external input
C₄ is an output generated internally

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage			–0.65	–1.5	V	V _{CC} = MIN, I _{IN} = –18 mA
V _{OH}	Output HIGH Voltage		2.7	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
V _{OL}	Output LOW Voltage			0.25	0.4	V	I _{OL} = 4.0 mA
				0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current	C ₀			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		Any A or B			40	μA	
		C ₀			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
		Any A or B			0.2	mA	
I _{IL}	Input LOW Current	C ₀			–0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
		Any A or B			–0.8	mA	
I _{OS}	Short Circuit Current (Note 1)		–20		–100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Total, Output HIGH				34	mA	V _{CC} = MAX
	Total, Output LOW				39		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

BCD TO 7-SEGMENT DECODER/DRIVER

The SN54/74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

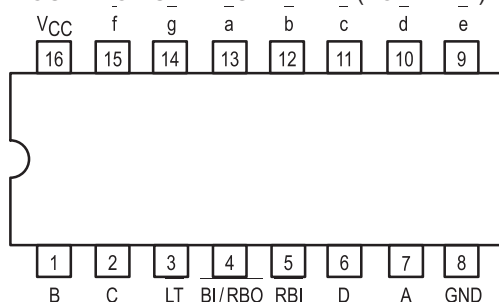
The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN54/74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

These outputs will withstand 15 V with a maximum reverse current of 250 μ A. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN54/74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

- Lamp Intensity Modulation Capability (BI/RBO)
- Open Collector Outputs
- Lamp Test Provision
- Leading/Trailing Zero Suppression
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

A, B, C, D	BCD Inputs
RBI	Ripple-Blanking Input
LT	Lamp-Test Input
BI/RBO	Blanking Input or Ripple-Blanking Output
a, to g	Outputs

LOADING (Note a)

	HIGH	LOW
A, B, C, D	0.5 U.L.	0.25 U.L.
RBI	0.5 U.L.	0.25 U.L.
LT	0.5 U.L.	0.25 U.L.
BI/RBO	0.5 U.L.	0.75 U.L.
a, to g	1.2 U.L.	2.0 U.L.
	Open-Collector	15 (7.5) U.L.

NOTES:

a) 1 Unit Load (U.L.) = 40 μ A HIGH, 1.6 mA LOW.

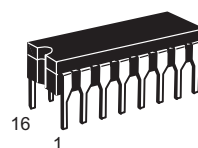
b) Output current measured at $V_{OUT} = 0.5$ V

The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges.

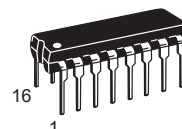
SN54/74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

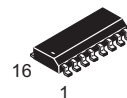
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

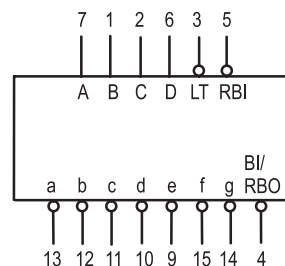


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

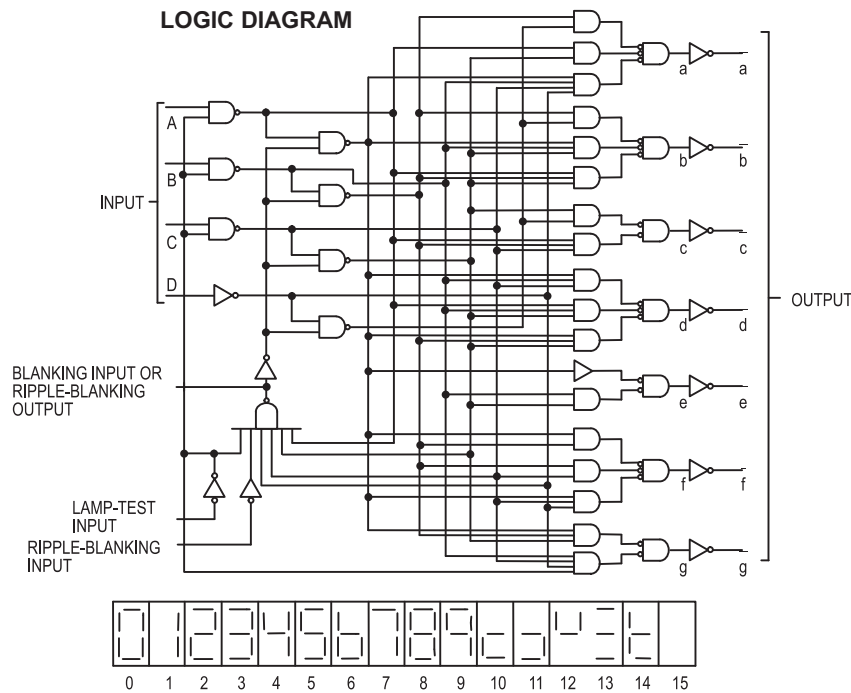
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS47



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS							OUTPUTS							NOTE
	LT	RBI	D	C	B	A	BI/RBO	\bar{a}	\bar{b}	\bar{c}	\bar{d}	\bar{e}	\bar{f}	\bar{g}	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	L	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	L	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial





NOTES:

- (A) BI/RBO is wire-AND logic serving as blanking Input (BI) and/or ripple-blanking output (RBO). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.
- (B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.
- (C) When ripple-blanking input (RBI) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).
- (D) When the blanking input/ripple-blanking output (BI/RBO) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

The SN54/74LS247 thru SN54/74LS249 are BCD-to-Seven-Segment Decoder/Drivers.

The LS247 and LS248 are functionally and electrically identical to the LS47 and LS48 with the same pinout configuration. The LS249 is a 16-pin version of the 14-pin LS49 and includes full functional capability for lamp test and ripple blanking which was not available in the LS49.

The composition of all characters, except the 6 and 9 are identical between the LS247, 248, 249 and the LS47, 48 and 49. The LS47 thru 49 compose the  and  without tails, the LS247 thru 249 compose the  and  with the tails. The LS247 has active-low outputs for direct drive of indicators. The LS248 and 249 have active-high outputs for driving lamp buffers.

All types feature a lamp test input and have full ripple-blanking input/output controls. On all types an automatic leading and/or trailing-edge zero-blanking control (RBI and RBO) is incorporated and an overriding blanking input (BI) is contained which may be used to control the lamp intensity by pulsing or to inhibit the output's lamp test may be performed at any time when the BI/RBO node is at high level. Segment identification and resultant displays are shown below. Display pattern for BCD input counts above 9 are unique symbols to authenticate input conditions.

LS247

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

LS248

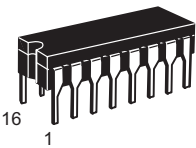
- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

LS249

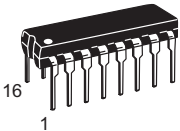
- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

SN54/74LS247
SN54/74LS248
SN54/74LS249

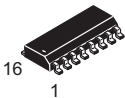
**BCD-TO-SEVEN-SEGMENT
DECODERS/DRIVERS**
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



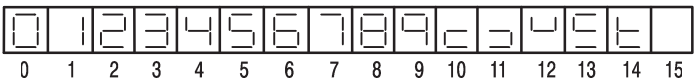
N SUFFIX
PLASTIC
CASE 648-08



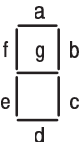
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

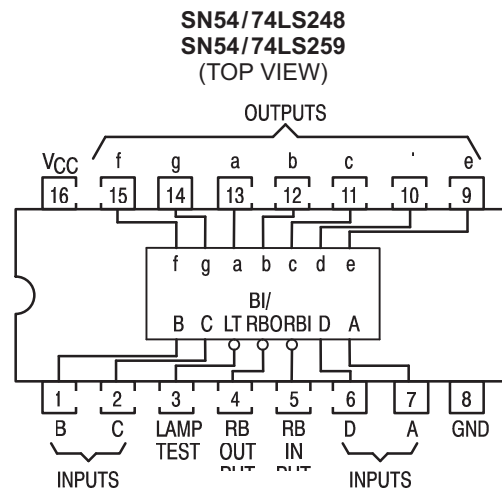
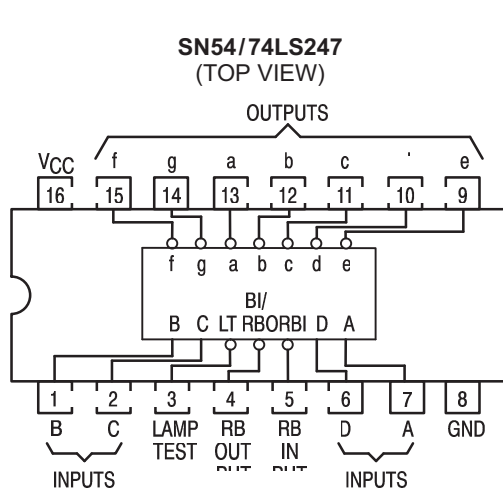


NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS



**SEGMENT
IDENTIFICATION**

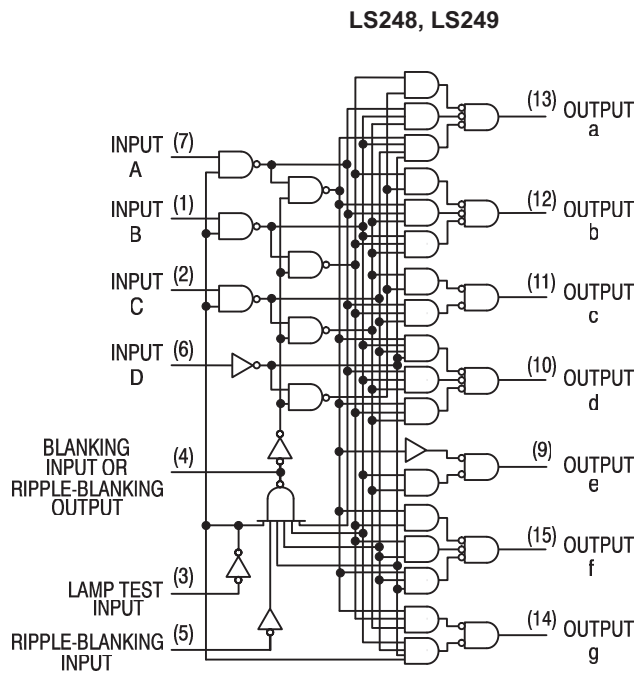
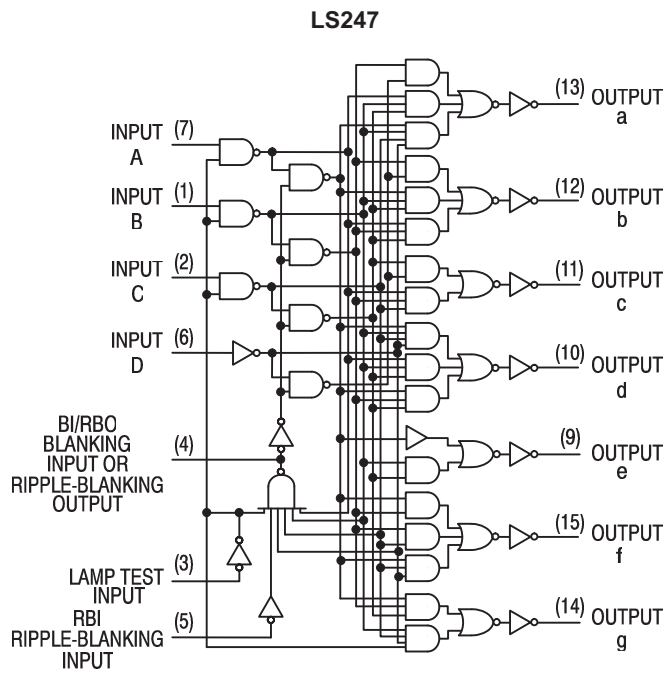
SN54/74LS247 • SN54/74LS248 • SN54/74LS249



ALL CIRCUIT TYPES FEATURE LAMP INTENSITY MODULATION CAPABILITY

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE	
SN54LS247	low	open-collector	12 mA	15 V	35 mW
SN54LS248	high	2.0 kΩ pull-up	2.0 mA	5.5 V	125 mW
SN54LS249	high	open-collector	4.0 mA	5.5 V	40 mW
SN74LS247	low	open-collector	24 mA	15 V	35 mW
SN74LS248	high	2.0 kΩ pull-up	6.0 mA	5.5 V	125 mW
SN74LS249	high	open-collector	8.0 mA	5.5 V	40 mW

LOGIC DIAGRAM



SN54/74LS247 • SN54/74LS248 • SN54/74LS249

LS247
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO [†]	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

LS248, LS249
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO [†]	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	H	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	H	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = HIGH Level, L = LOW Level, X = Irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.

3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

[†] BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).