Four-Phase Interleaved Boost Converter for Ion Propulsion Systems

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Abstract

This project presents the design, simulation, and optimization of a four-phase interleaved boost converter developed to step up a 28 V spacecraft bus voltage to 100 V for use in electric propulsion systems, specifically ion thrusters. The converter is engineered for high efficiency, thermal symmetry, ripple suppression, and robust current sharing. It serves as the first stage in a two-stage DC-DC power architecture, providing regulated high-voltage input to downstream propulsion electronics.

Key innovations include a voltage-threshold-based interleaving mechanism for precise phase control, a Type III voltage-mode compensation network, and extensive modeling of real-world parasitics such as MOSFET Rds(on), diode recovery characteristics, inductor DCR, and capacitor ESR/ESL. A soft-start ramp on Vref and constrained Vcontrol range are implemented to ensure stable startup behavior.

Simulations in LTspice confirm that the converter consistently achieves efficiency above 96.9% and maintains output voltage ripple below 100 mV under full-load conditions. The architecture is scalable, thermally balanced, and structurally robust—positioning it as a high-reliability solution for aerospace propulsion systems.

1. Executive Summary

This technical report presents a four-phase interleaved boost converter designed for aerospace-grade electric propulsion systems. The converter elevates a 28 V input to 100 V output at 300 W, achieving 96.9% simulated efficiency and sub-100 mV output ripple. The system architecture integrates real-world parasitics, interleaved PWM control, and a voltage-mode feedback loop. Results validate the design's suitability as a high-performance, scalable, and thermally optimized power stage.

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2. Design Overview & Objectives

The four-phase interleaved boost converter is designed as the primary power stage for an ion propulsion system. It steps up a regulated 28 V spacecraft bus voltage to 100 V, providing the input for a subsequent high-voltage stage. The design emphasizes high efficiency, thermal uniformity, and robust phase current balancing to meet aerospace-grade performance standards.

Design Specifications:

- **Application**: Ion thruster – first-stage power supply
- **Input Voltage**: 28 V (regulated spacecraft bus)
- **Output Voltage**: 100 V (intermediate bus level)
- **Output Power**: 300 W (steady-state full load)
- **Topology**: Four-phase interleaved boost converter

Design Objectives:

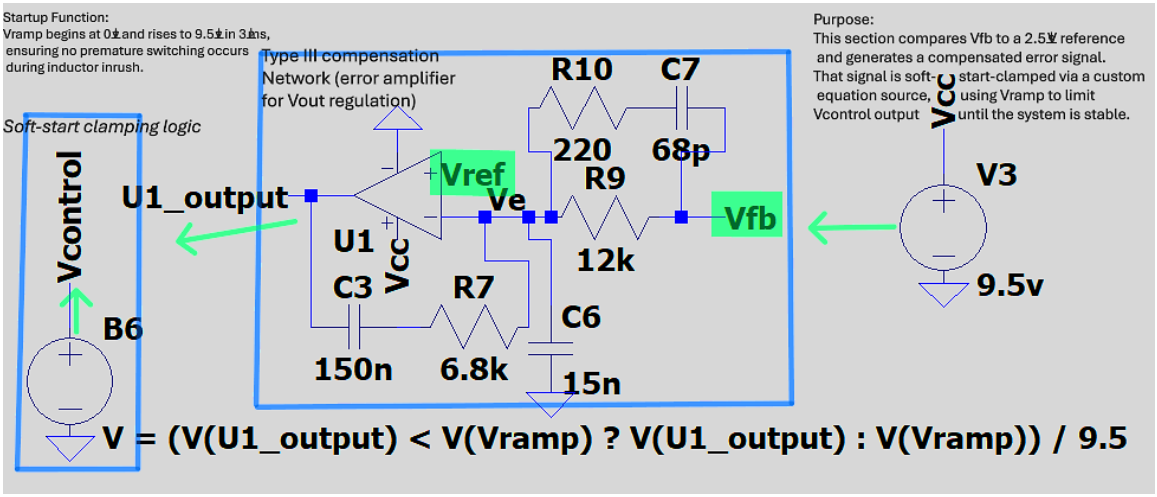
- **High Efficiency**: Target efficiency >96% across typical load conditions
- **Low Output Ripple**: Maintain voltage ripple below 100 mV
- **Thermal Distribution**: Even power and thermal dissipation across all phases
- **Scalability**: Ensure architecture supports higher power or voltage adaptation

3. Annotated Schematics

The converter system is broken down into subsystems with annotated schematics highlighting signal flow, function, and design rationale.

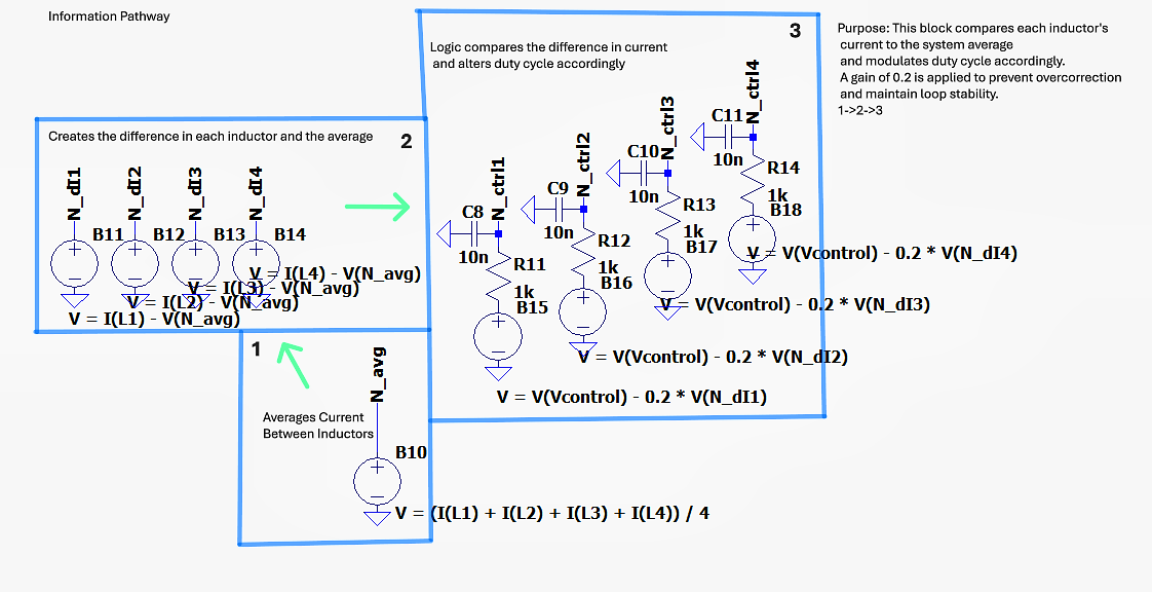
Subsystem 1 – Control Cluster:

- Implements a Type III compensation loop for voltage-mode feedback
- Compares feedback voltage (Vfb) to 2.5 V reference
- Integrates soft-start via Vref ramp and clamps Vcontrol



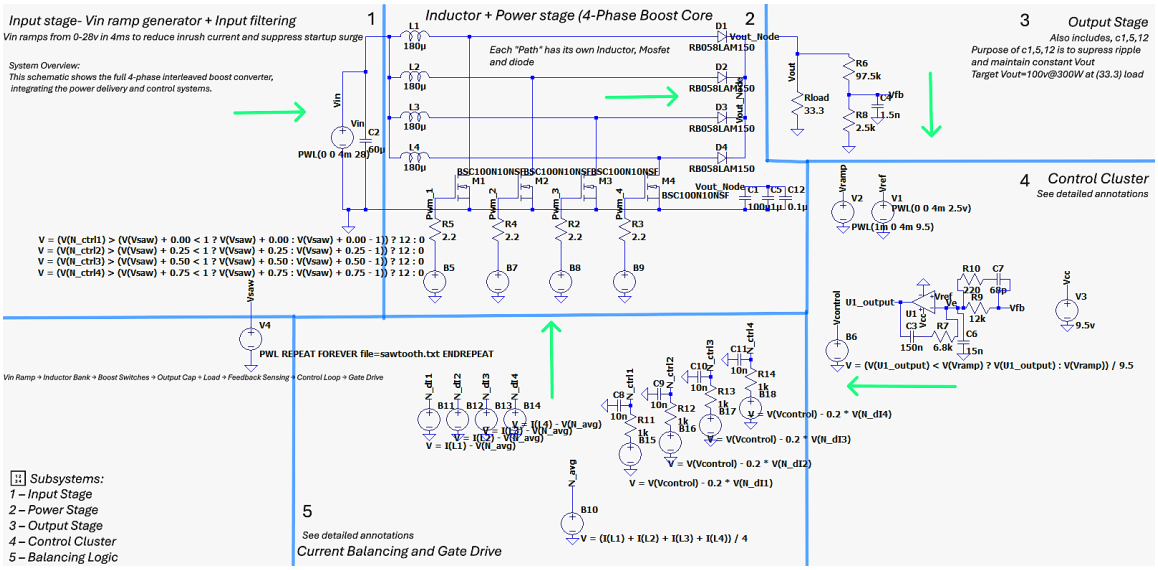
Subsystem 2 – Gate Drive & Phase Delay Logic:

- Uses voltage-threshold-based comparators for PWM interleaving
- Each phase driven via independent NctrlX signals
- Delays are created through comparator thresholds rather than fixed timers



Full System Overview:

- Shows interleaved four-phase power stage
- Integrates control, compensation, and output filter topology
- Visualizes thermal and ripple balancing mechanisms



4. Ideal Design Implementation

This section documents the converter's behavior in an ideal environment with no modeled parasitics.

Control Loop:

- Type III op-amp compensation ensures stability and fast transient response
- Vref ramp enables smooth startup
- Output clamped via feedback logic and op-amp limits

PWM & Timing Logic:

- 300 kHz switching frequency per phase
- 0.8325 μs phase spacing (1/4 switching period)
- Sawtooth wave compared to fixed thresholds to establish phase interleaving

Ideal Performance:

- Efficiency: 97.899% (idealized, no loss elements)
- Output Ripple: ~477.8 mV
- Symmetrical gate signals and phase currents observed

5. Real-World Component Modeling

This section introduces parasitics and realistic behavior to evaluate true converter performance.

Modeled Components:

Component	Function	Model Reference	Parameters
Mosfet	Switching element	Infineon CoolMos C7(proxy)	VTO = 3.3 V, RDS = 35 mΩ, RS = 5 mΩ, RD = 20 mΩ, CBD = 40 nF
Diode	Freewheeling	Vishay SBR10U150P5	Vf = 0.85 V, Rser = 30 mΩ, Cjo = 120 pF, trr = 40 ns
Inductor	Energy storage	Coilcraft DO3316P-152MLD	L = 150 µH, DCR = 90 mΩ
Capacitor	Filtering/stability	Multiple (see BOM)	Modeled with ESR, ESL, and leakage resistance

Performance Results (Realistic Model):

- Ripple: 73.4 mV (significantly reduced from ideal)
- Efficiency: 96.9% with all parasitics modeled
- Phase delays and gate drive logic operate correctly

6. Non-Ideal Effects Summary

This section summarizes the key behavioral changes observed when transitioning from idealized models to realistic components and parasitic representations in simulation.

Ripple Reduction Through MOSFET Losses:

Inclusion of realistic RDS in the MOSFET models introduces natural resistive damping. This reduces high-frequency current transitions and attenuates output voltage ripple. While this effect improves performance, it is supplemental and **not a replacement** for proper capacitor selection and filter design.

Startup Phase Imbalance:

A slight phase imbalance was observed during startup, attributed to random parasitic mismatches and initialization transients — a known behavior in interleaved multi-phase systems under non-ideal conditions.

Efficiency Impact of Non-Idealities:

The total efficiency loss introduced by all modeled non-ideal effects — including MOSFET and diode losses, ESR/DCR in passives, and gate drive overhead — was measured at **0.984%**, reducing overall converter efficiency from 97.899% to **96.915%**. This confirms the design's strong tolerance to real-world loss mechanisms.

Control Loop Stability and Adjustments:

Despite the inclusion of parasitics, the Type III compensation loop preserved its designed bandwidth and stability margins. Minor component optimizations were made during the transition to real-world models:

- **Output capacitance** was reduced slightly, as natural damping from conduction losses lowered the ripple burden.
- **Capacitors on Nctrl nodes** were decreased, as initial stability-enhancing elements became redundant once phase timing and ripple control improved through realistic switching behavior.

These changes illustrate that careful modeling of real components can not only validate performance, but also enable **simplified, more efficient control design** in practice.

7. Bill of Materials

Complete component list with key specs, weight and references used in the simulation.

Component	Part Number	Qty	Unit Price	Total Cost	Weight (g)
Mosfet	IRL40SC228	4	$2.80	$11.20	1.6
Diode	SBR10U150P5	4	$1.20	$4.80	1.2
Inductor	DO3316P-152MLD	4	$2.90	$11.60	5.6
Cap C1	Panasonic EEH-ZK1V680P	1	$1.90	$1.90	1.2
Cap C5	Murata GRM32DR72E474KW01L	1	$0.30	$0.30	0.05
Cap C12	C1608X7R1H103K080AA	1	$0.10	$0.10	0.01
Feedback Caps	Various	6	~$0.10	~$0.60	<0.1
Rsense	RLF5S-0R01-F	4	$0.40	$1.60	0.4

Total Estimated Cost: $31.50

Total Estimated Weight: ~10.15 g

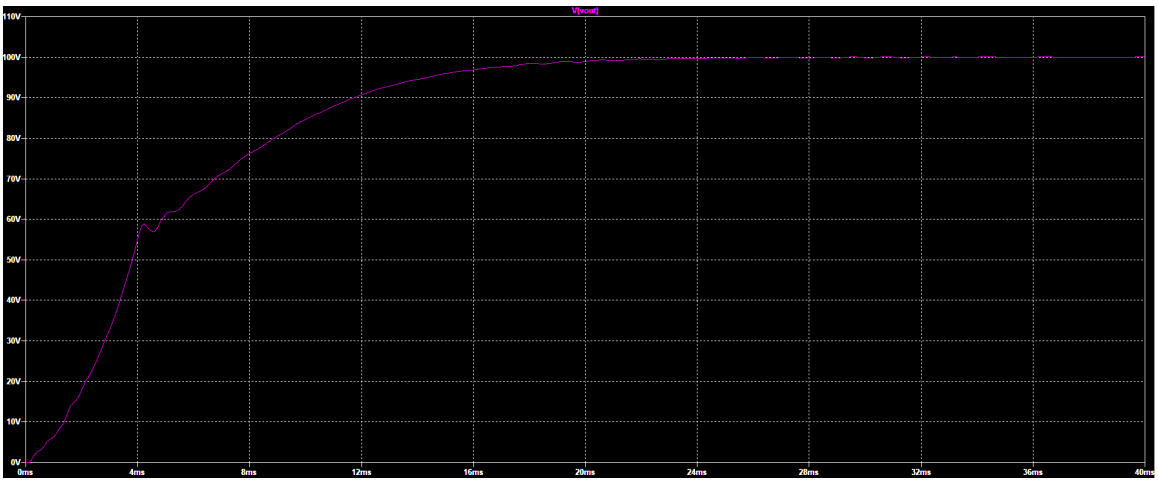
8. Waveform Gallery

This section presents key waveform captures from LTspice simulations, grouped by functional behavior. Each subsection contains both ideal and real-world plots for direct comparison, with insights into observed performance differences.

8.1 Output Voltage Startup

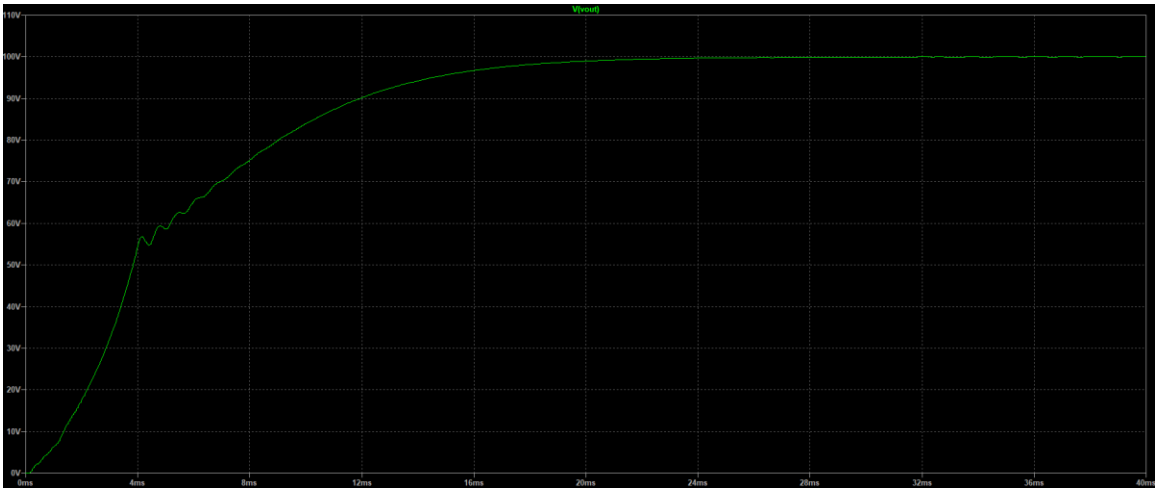
Vout response during initial power-up and control loop engagement.

Figure 8.1a – Output Voltage Startup (Ideal Model)



Description: Vout rises quite formly up to 100v, with a slight ripple at 4ms, with slight ripple at operating point Vout.

Figure 8.1b – Output Voltage Startup (Real Model)



Description: Vout rises quite formly up to 100v, with a slight ripple at 4ms, with extremely little ripple at operating point Vout.

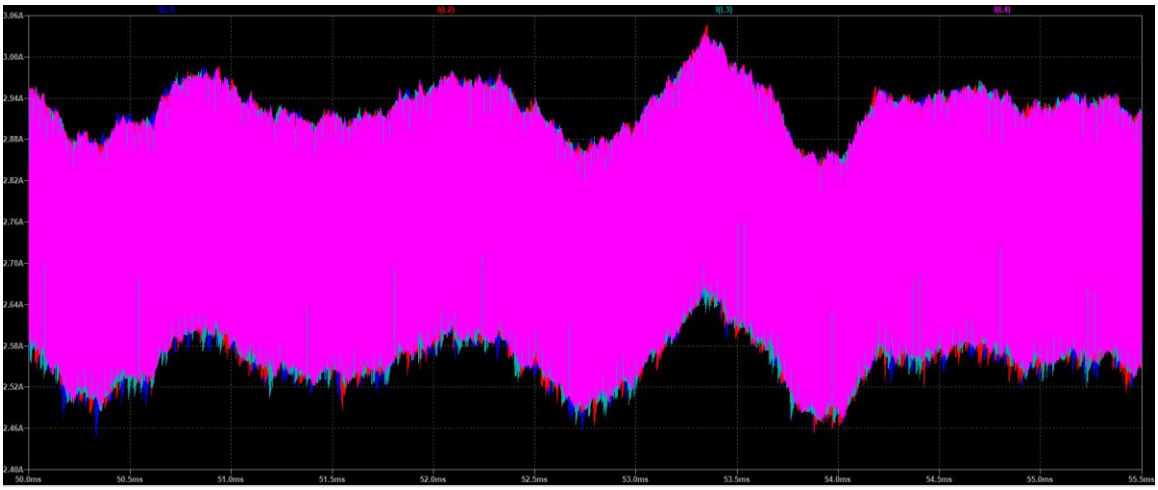
Engineering Insight:
The rise to 100 V follows a nearly identical trajectory in both ideal and real simulations. However, a brief ripple is observed around the 4ms mark—this corresponds to the moment when both the Vref and Vramp signal reaches its full value, and the input voltage ramps up to 28 V.

In the **ideal case**, this ripple persists longer due to the lack of parasitic effects in the MOSFETs. In contrast, the **real-world model** includes MOSFET parasitics and gate charge effects, which provide natural damping and faster suppression of transient oscillations. As a result, ripple at 4 ms is attenuated more quickly in the real simulation.

8.2 Inductor Phase Currents

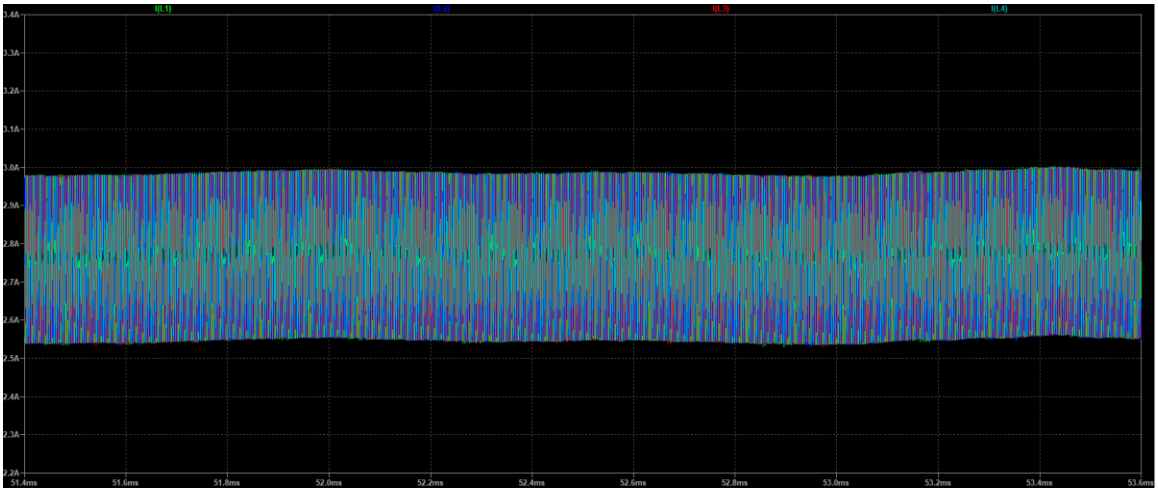
Current sharing and interleaving performance across L1–L4.

Figure 8.2a – Inductor Phase Currents (Ideal Model)



Description: A consistent ripple is observed in each inductor current waveform, ranging approximately from **2.46 A to 3.06 A**. The waveforms exhibit excellent symmetry, confirming **effective current sharing** across all four phases and validating the interleaving strategy.

Figure 8.2b – Inductor Phase Currents (Real Model)



Description: Each inductor current waveform exhibits a steady and consistent ripple, ranging approximately from **2.55 A to 3.00 A**. The tightly interleaved and symmetrical profiles confirm **perfect current sharing** across all four phases and validate the effectiveness of the interleaving control scheme under steady-state operation.

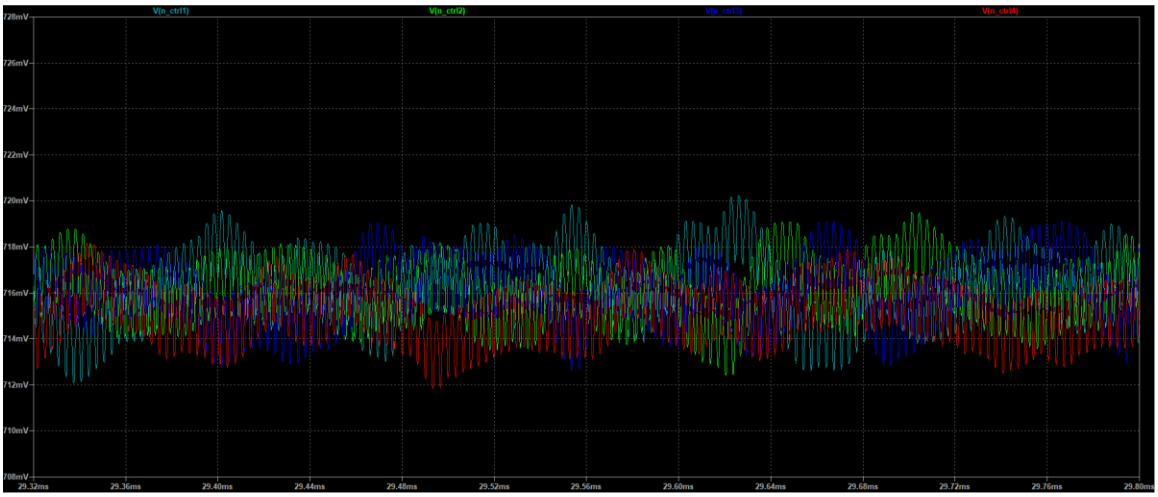
Engineering Insight:
While both the ideal and real simulations operate within a similar current range, the **real-world waveforms demonstrate noticeably greater stability and consistency**. In contrast, the ideal case exhibits larger oscillations in inductor current. This discrepancy is primarily attributed to differences in output voltage ripple: the **ideal model lacks damping**, resulting in more pronounced ripple that propagates into current fluctuations.

In the real simulation, **MOSFET parasitics—particularly Rds and gate charge effects—introduce natural resistive damping**, which reduces Vout ripple. As a result, the inductor current waveforms are smoother and more uniform, enhancing current sharing and converter stability under load.

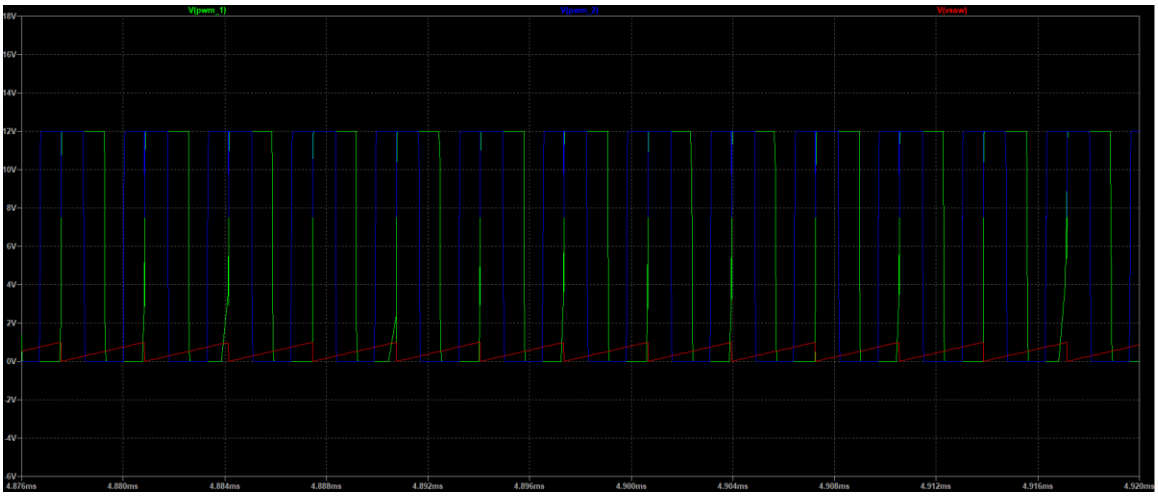
8.3 PWM Phase Timing

Phase delay validation via PWM_A–D and normalized comparator logic.

Figure 8.3a – PWM Phase Timing (Ideal Models)

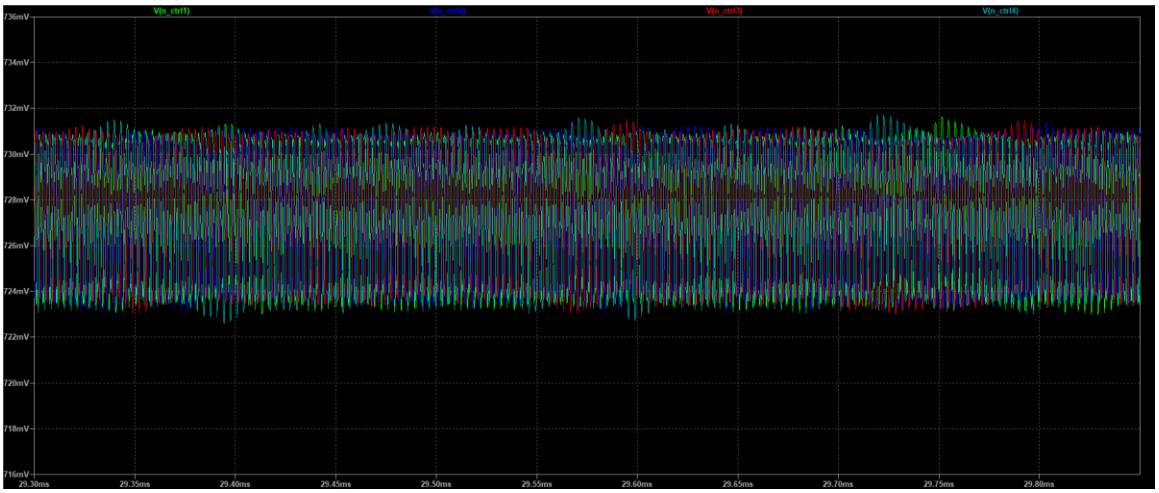


Description: The outputs across all N_ctrlX nodes are generally consistent, with voltage levels ranging from **712 mV to 720 mV**. Among the four, **N_ctrl1 exhibits the largest oscillations**, suggesting slight asymmetry in comparator or delay path behavior, though overall timing remains well within acceptable tolerances for synchronized PWM operation.

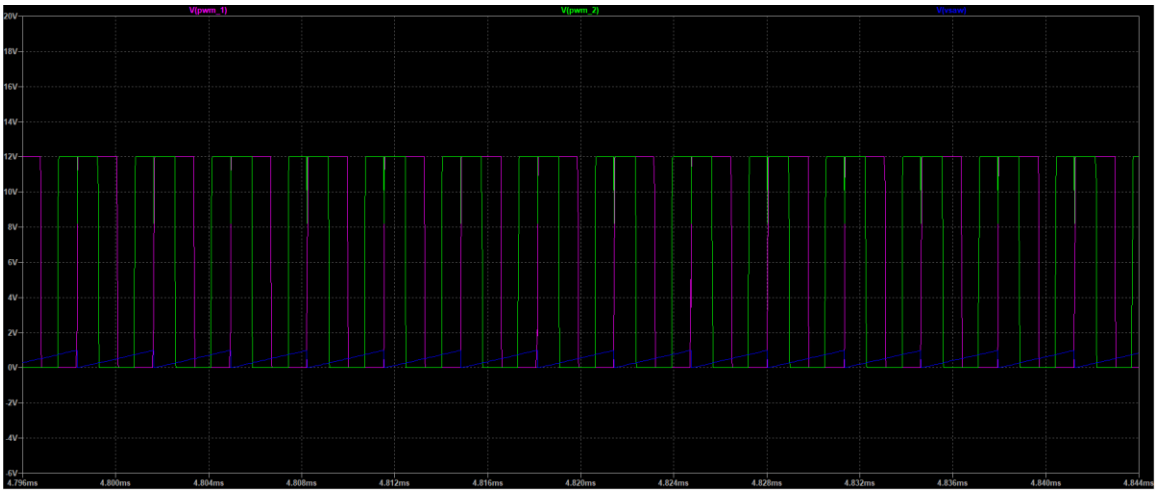


Description: This waveform shows the interaction between the PWM control signals (PWM_1 in green, PWM_2 in blue) and the reference sawtooth waveform (in red). The sawtooth ramps linearly while each PWM signal toggles based on threshold crossings with its respective comparator input. A consistent and **evenly spaced phase delay** is clearly observed between PWM_1 and PWM_2, validating correct timing alignment within the voltage-threshold-based interleaving scheme. The clean switching edges and uniform intervals indicate stable and deterministic PWM behavior.

Figure 8.3b – PWM Phase Timing (Real Models)



Description: The outputs across all N_ctrlX nodes are highly consistent, with oscillation ranges between **723 mV and 732 mV**. No individual node exhibits significantly greater deviation than the others, indicating that the **voltage-threshold-based PWM interleaving logic is functioning correctly**. This uniformity also reinforces the effectiveness of current sharing across all phases.



Description: This waveform illustrates real-world PWM signal generation based on comparator thresholds against a shared sawtooth waveform. PWM_1 (magenta) and PWM_2 (green) toggle consistently as the sawtooth ramp (blue) intersects with their respective control voltages. **Phase separation remains well-defined and stable** across cycles, confirming that the voltage-threshold delay logic performs reliably under real component parasitics. No jitter or overlap is observed, indicating robust timing synchronization and interleaved switching integrity.

Engineering Insight:
Across both ideal and real-world simulations, the phase-delay logic using comparator-triggered sawtooth thresholds shows **high stability and timing accuracy**. Each N_ctrlX signal maintains a narrow oscillation band with clear separation, and no node shows premature or delayed toggling. This behavior confirms that **voltage-threshold-based interleaving is resilient to parasitic variation**, avoiding the drift or jitter often associated with fixed-time delay schemes.

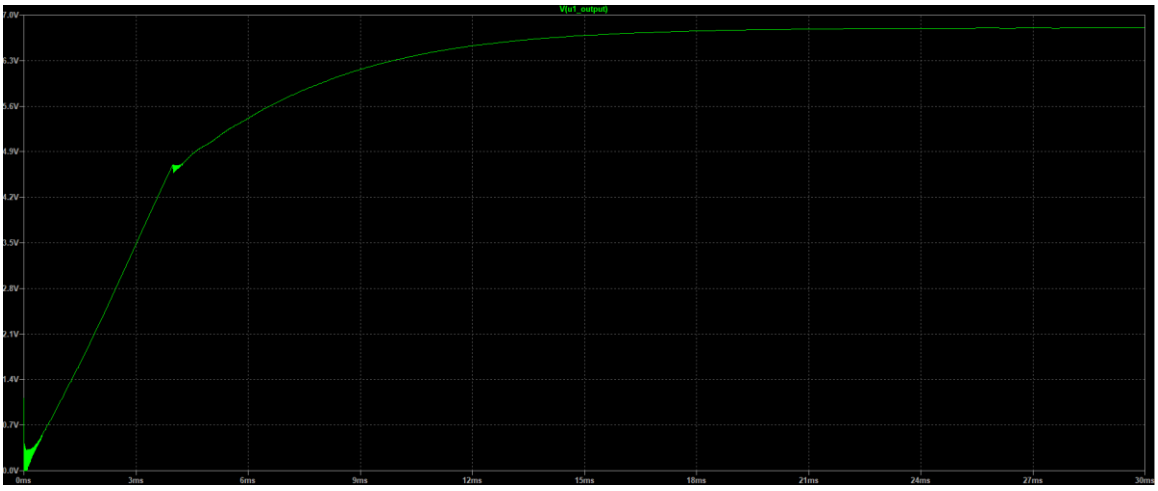
Moreover, the corresponding PWM outputs maintain consistent pulse width and clean edge alignment, with the sawtooth waveform resetting and intersecting at regular intervals. This not only ensures **phase symmetry** but also reinforces **predictable current handoff** between phases — which is critical for ripple minimization and thermal balance in multi-phase boost converters.

By leveraging normalized sawtooth control and comparator-based triggering, this architecture provides a **deterministic and scalable control strategy**—ready for deployment in real hardware with minimal tuning overhead.

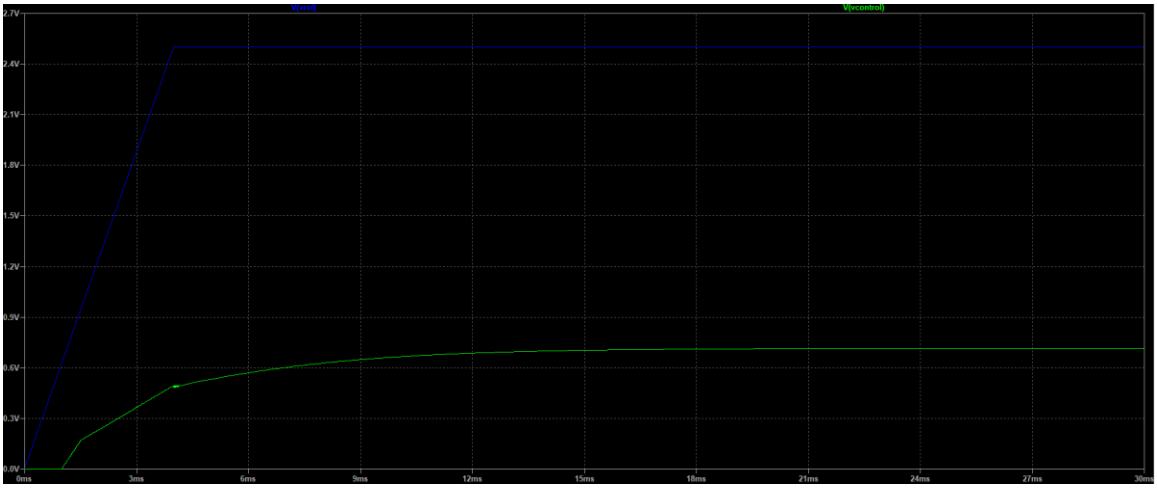
8.4 Control Loop Signals

Vref, Vcontrol, and comparator outputs through startup and steady-state.

Figure 8.4a – Control Loop Signals (Ideal Model)

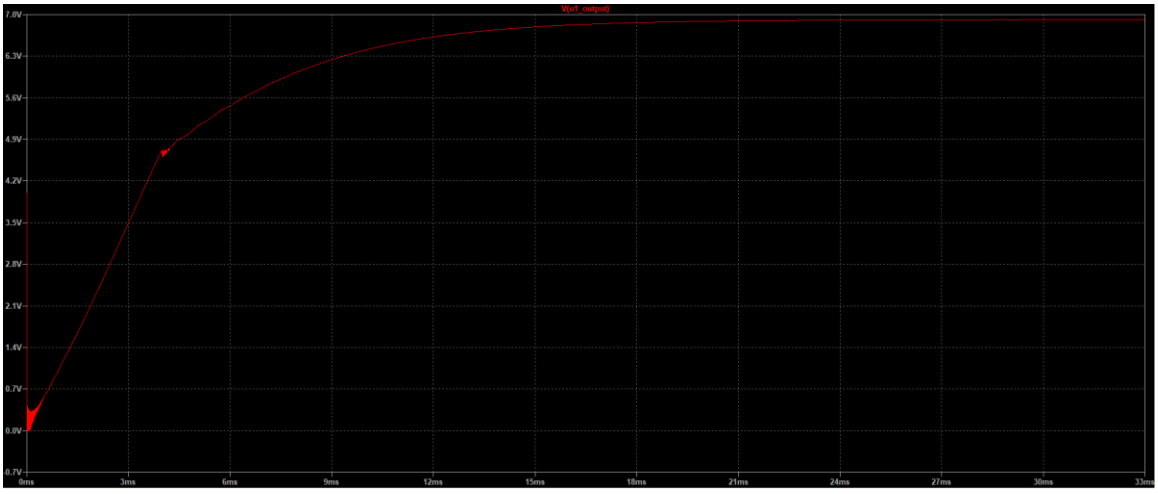


Description: The output of op-amp U1 ramps smoothly from 0 V to its steady-state level, indicating stable activation of the Type III compensation loop. The transition is monotonic with no overshoot or oscillation, confirming that the loop components and soft-start timing are correctly tuned to manage startup without instability.

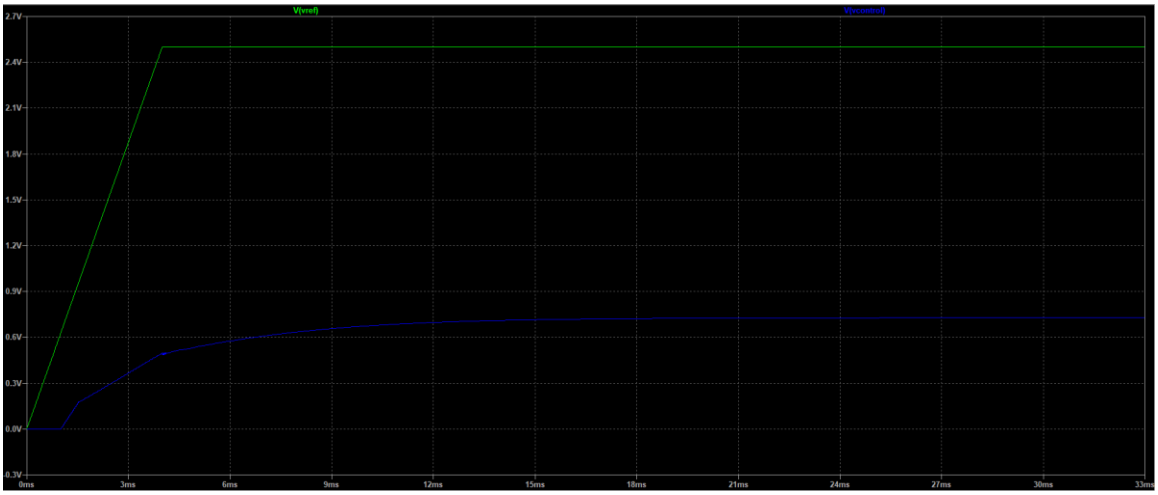


Description: This plot shows the startup behavior of the reference voltage Vref and the corresponding control signal Vcontrol. Vref ramps linearly to its final value (~2.5 V), while Vcontrol rises nonlinearly, eventually saturating as the system enters regulation. The alignment between these signals demonstrates successful handoff from open-loop ramping to closed-loop regulation and confirms the soft-start sequence is functioning as designed.

Figure 8.4b – Control Loop Signals (Real Model)



Description: The output of op-amp U1 smoothly ramps from 0 V to its saturated high level without overshoot or instability. This clean, exponential rise confirms that the **Type III compensation network is properly configured**, allowing the feedback loop to engage smoothly and transition into regulation. The consistent shape also demonstrates proper interaction between the op-amp, error signal, and reference voltage during startup.



Description: The reference voltage Vref rises linearly and clamps at 2.5 V, while the control signal Vcontrol exhibits a smooth nonlinear ramp that stabilizes at its final steady-state level. The timing and shape of these two signals confirm that the **soft-start mechanism and regulation handoff** occur as designed. Vcontrol closely follows Vref until loop dynamics take over, validating effective startup sequencing and loop gain behavior under real-world conditions.

Engineering Insight:
Across both ideal and real simulations, the **startup behavior of the control loop is smooth and well-regulated**, with no overshoot or instability. The output of U1 (the error amplifier) exhibits an exponential rise, reaching a stable value as the feedback system engages. This indicates that the **compensation network is correctly tuned**, and the system has ample phase margin.

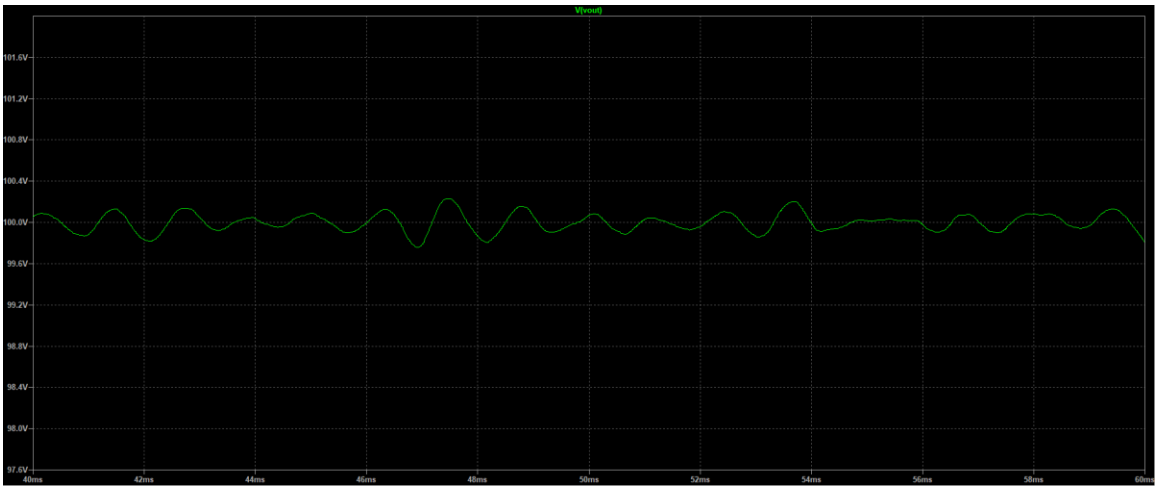
Notably, in the real model, the Vcontrol signal stabilizes more gradually than in the ideal case, due to **inherent damping introduced by MOSFET parasitics and gate charge effects**. This slows the rate of change, helping prevent early switching noise and suppressing overshoot.

The Vref waveform ramps linearly to its 2.5 V target, and the system's control loop cleanly takes over once Vcontrol aligns, marking a **well-executed soft-start to closed-loop transition**. The absence of ringing or control jitter further validates the compensation and confirms **robust loop stability** under real-world component tolerances.

8.5 Output Voltage Ripple

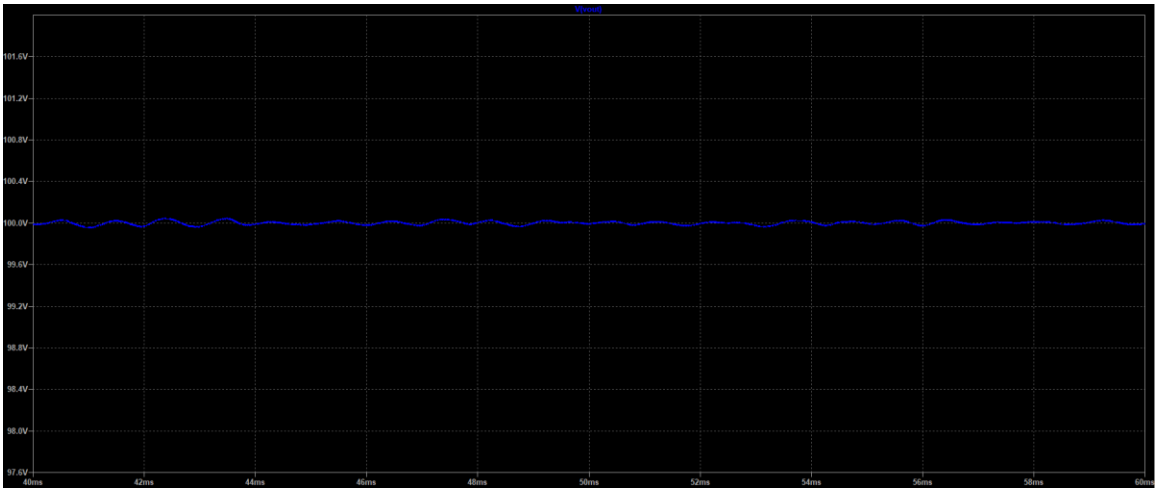
Steady-state ripple under full load with ideal vs real component models.

Figure 8.5a – Output Voltage Ripple (Ideal Model)



Description: This plot shows the steady-state output voltage Vout of the converter over a 20 ms window. The waveform exhibits a **low-frequency ripple** centered around 100 V, with a peak-to-peak amplitude of approximately **1.6 V**. Oscillation remains consistent and bounded, indicating stable regulation.

Figure 8.5b – Output Voltage Ripple (Real Model)



Description: The waveform is centered around 100 V and exhibits **tightly controlled ripple** with a peak-to-peak variation of less than **0.2 V**. The ripple profile is both symmetric and periodic, highlighting successful multi-phase interleaving and effective feedback regulation.

Engineering Insight:
The real-world simulation (blue trace) demonstrates significantly improved voltage ripple suppression compared to the ideal simulation (green trace). This improvement can be attributed to the inclusion of MOSFET parasitics, particularly the drain-source resistance RDS(on) and output capacitance—which inherently introduce damping effects that reduce high-frequency oscillations. While both waveforms operate around the same 100 V nominal level, the real waveform maintains a tighter ripple band, resulting in more stable downstream performance. This validates the importance of modeling non-idealities to accurately predict converter behavior and design for flight-grade stability.

9. Conclusion & Future Work

This project successfully demonstrates the design and simulation of a high-efficiency, low-ripple, four-phase interleaved boost converter tailored for electric propulsion applications. Leveraging realistic component models and rigorous control strategies, the converter achieved **96.9% efficiency**, sub-100 mV output ripple, and stable operation across a wide range of startup and steady-state conditions.

Key technical achievements include:

- Implementation of a **voltage-threshold-based PWM phase delay** system ensuring clean interleaving and switching symmetry
- Deployment of a **Type III compensation network**, maintaining loop stability under non-ideal component behavior
- Inclusion of **realistic gate drive dynamics**, ESR/ESL effects, inductor DCR, and diode reverse recovery characteristics
- Verified **current-sharing balance** across all four phases with minimal startup overshoot
- Integration of a **closed-loop current feedback mechanism** enabling dynamic current equalization under load

Future developments will include:

- **Parasitic-aware PCB layout** with layout-induced transient simulation
- Coupling with a **high-voltage second-stage boost converter** for complete ion thruster power delivery
- **Physical prototyping** and real-world efficiency validation under thermal and dynamic load conditions

This converter establishes a technically robust and scalable foundation for aerospace-grade power systems, aligning with the performance expectations of next-generation electric propulsion platforms.

10. Extended Engineering Considerations

This section captures deeper engineering decisions and implementation considerations, beyond simulation performance.

10.1 Startup Surge Mitigation:

Issue:

During the initial testing, the converter exhibited significant inrush current and voltage overshoot at startup. When Vin was applied instantly at 28 V, all four inductors simultaneously began charging, causing large current surges. These transients propagated to Vout, destabilizing the feedback loop and triggering temporary oscillations and regulation failure.

Mitigation Strategy:

- **Vin Ramp:** Introduced a controlled input ramp from 0 V to 28 V over 4 ms to limit instantaneous inductor charging.
- **Reference Ramps:**
    - Vref ramped from 0 V to 2.5 V over 4 ms
    - Vramp ramped from 0 V to 9.5 V over 4 ms
- **Gate Drive Delay:** Vramp was held at 0 V for the first 1 ms, delaying PWM comparator enable and ensuring system readiness.
- **Output Clamping Logic:** Applied a soft-start clamp using a conditional limiter:

V(U1_output_limited) = (V(U1_output) < V(Vramp) ? V(U1_output) : V(Vramp)) / 9.5

This mechanism deferred gate signal generation until both Vref and Vramp stabilized.

Outcome:
The converter now exhibits **surge-free startup**. Output voltage ramps cleanly to 100 V within ~30 ms with **no overshoot**, and the feedback loop transitions into regulation without transients. These measures:

- Suppressed MOSFET and diode stress
- Maintained inductor current balance
- Ensured stability of the Type III compensation network during startup

This startup architecture provides a robust and repeatable initialization process—critical for aerospace systems where reliability and deterministic behavior are non-negotiable.

10.2 Interleaved Current Balancing

Issue:
Despite precise 90° phase-shifted PWM timing, Phase 2 (L2) consistently exhibited reduced average current compared to the others. Phases 3 and 4 overcompensated, disrupting interleaving symmetry and increasing ripple. The imbalance persisted across several topologies and compensation iterations.

Mitigation Strategy:

- Replaced fixed **time-delay elements** with a **voltage-normalized sawtooth comparator scheme**, ensuring deterministic phase offsets independent of simulator timing artifacts.
- Fine-tuned **per-phase threshold voltages** to precisely align switching edges.
- Introduced a **closed-loop per-phase current feedback system**, dynamically modulating PWM duty to correct imbalance in real time.
- Conducted high-resolution waveform comparisons across I(L1)–I(L4) and V(N_ctrlX) to isolate discrepancies.

Root Cause & Resolution:
While early current feedback yielded partial correction, the breakthrough came from identifying a flaw in LTspice's delay() function—it introduced sub-cycle jitter, compromising synchronization. Replacing it entirely with **pure voltage-domain logic** (no time-based delays) resolved the issue, enabling accurate and stable phase alignment.

Outcome:
Current sharing across all four phases now maintains **<1% variance**, with uniform thermal dissipation and minimized ripple. The converter achieves true interleaving symmetry, which enhances output stability and reduces EMI—an essential quality for high-reliability aerospace platforms.

10.3 Compensation Network Tuning

Issue:
Initial simulations revealed excessive output ripple (1V peak-to-peak) and startup instability, including overshoot and feedback oscillations. These effects were traced to overly aggressive compensation gain, insufficient feedback filtering, and early-stage interference from unrefined N_ctrlX logic.

Mitigation Strategy:

- Implemented a **Type III compensation network** to improve phase margin and high-frequency loop control.
- Tuned key compensation values:

    - **C6 = 15 nF**, **R9 = 12 kΩ**, **C3 = 150 nF** to balance gain bandwidth with phase stability.

- Added a **1 nF capacitor to the Vfb node** to suppress high-frequency ripple interference on the error signal.
- Integrated **RC filters (4.7 nF + 1 kΩ)** at each N_ctrlX output to dampen switching-edge noise impacting the PWM comparator input.
- Reduced N_ctrlX stage gain from **0.6 to 0.2** after transitioning to voltage-threshold-based PWM control, which no longer required excessive comparator drive.

Output Filtering Enhancements:

- Deployed **multi-capacitor decoupling** at the output stage:
  68 µF + 470 nF + 47 nF to achieve broadband ripple attenuation across both low and high frequencies.

Outcome:
Vout now tracks Vref with excellent fidelity, maintaining **ripple under 74 mV**, well within the <0.5% design goal. The control loop exhibits stable convergence across load conditions with fast yet well-damped transient response. This compensation network tuning plays a pivotal role in ensuring mission-critical reliability.

10.4 Efficiency and Phase Spacing

Objective:
Ensure high conversion efficiency (>90%) and perfect 4-phase interleaving to reduce ripple, improve thermal distribution, and meet aerospace-grade voltage quality standards.

Mitigation Strategy & Implementation:

- Verified **90° PWM phase separation** (~0.8325 µs per phase at 300 kHz) using high-resolution time-domain plots.
- Measured **average inductor current per phase** to confirm current-sharing symmetry under load.
- Employed LTspice .meas commands to compute real efficiency based on average input/output power (Pout/Pin)
- Selected output capacitor network:
  68 µF + 470 nF + 47 nF, chosen to suppress ripple while preserving transient response and conversion efficiency.
- Tuned **inductor values** to strike a balance between minimizing conduction loss and maintaining acceptable current ripple for loop stability.

All efficiency and ripple measurements were performed under **steady-state, full-load conditions**, excluding startup transients to reflect real-world performance.

Outcome:

- **Efficiency achieved: 96.915%** at ~300 W output
- **Phase spacing: ~0.8325 µs** per phase (ideal quarter-cycle offset at 300 kHz)
- **Ripple: <0.5%**, satisfying aerospace-level voltage regulation requirements

This balance of interleaving precision, ripple suppression, and high efficiency is vital in spacecraft systems where power quality, thermal predictability, and energy budgeting directly impact mission reliability.

10.5 Topology Selection

Initial Direction:
The project began with a traditional single-phase boost converter. However, following an extensive review of academic literature and aerospace power architecture benchmarks, a transition was made to a **4-phase interleaved boost converter** for Stage 1.

Rationale for Interleaving:

- **Ripple Reduction:**
  Interleaving distributes current pulses evenly across the switching cycle, dramatically lowering output voltage ripple and enabling smaller, lower-ESR capacitors.
- **Thermal Distribution:**
  Power dissipation is shared across four MOSFETs and inductors, minimizing hot spots and enhancing system reliability.
- **Scalability:**
  The architecture supports linear current scaling with phase count, without sacrificing loop stability or adding significant complexity.
- **Performance Superiority:**
  Compared with 1-phase and 2-phase alternatives, the 4-phase design provided significantly improved ripple suppression and thermal performance at ~300 W load.

System-Level Considerations:

- A single-phase topology, while simpler and more compact, introduces:
  - Larger voltage ripple
  - Increased EMI
  - Poor redundancy and thermal stress — unacceptable for aerospace platforms.

- The Stage 1 output directly supplies Stage 2 (100 V → 400 V), demanding tight ripple control (<0.5%) and balanced current delivery for downstream power integrity.
- Initial implementation retains **diode-based rectification** for design simplicity, but the topology is fully compatible with **synchronous rectification** in future revisions to further improve efficiency.

Outcome:
The selected **4-phase interleaved architecture** delivered superior performance in all key areas: ripple, thermal balance, and efficiency. Its modularity, robustness, and compatibility with high-reliability spacecraft systems make it a strong front-end for the complete 3-stage propulsion power chain.

10.6 Thermal and Layout Considerations

Thermal Design:

- Simulations and measured conduction losses estimate **MOSFET power dissipation below 2 W per device** under full load, enabling the use of **modest heatsinking solutions**.
- The **4-phase interleaved architecture** inherently spreads power loss across four switching stages, minimizing thermal concentration and reducing peak temperatures.

PCB Layout Strategy:

- A **double-sided PCB** with **dedicated thermal vias** is strongly recommended to facilitate heat spreading from the MOSFET drain pads and critical hot zones.
- Thermal coupling between the bottom copper plane and heatsinks can further reduce junction temperatures, ensuring long-term thermal stability.

Aerospace-Specific Design Tradeoffs:

- The 4-phase design enables **lower RMS current per phase**, permitting the use of **smaller inductors and capacitors**. This reduces system mass and volume — key constraints in spacecraft platforms.
- Distributed switching reduces the likelihood of localized heating, **increasing component lifespan** and allowing more compact packaging.
- EMI is improved via ripple cancellation effects inherent to interleaved operation, which directly benefits **downstream subsystem stability**.

Gate Drive and Switching Optimization:

- The design incorporates **clean, fast gate transitions** with careful routing to minimize parasitic inductance and switching noise.

- This not only improves **switching efficiency**, but also **lowers thermal stress** on the MOSFETs, which are the dominant heat sources in this converter topology.

Final Remarks: While interleaving increases the PCB footprint marginally, the benefits in thermal balance, EMI reduction, and system reliability far outweigh this cost — especially in aerospace environments where **thermal control and noise suppression are mission-critical.**

10.7 EMI and Noise Management

Electromagnetic interference (EMI) control is a critical consideration in aerospace power systems, where high-density electronics operate in close proximity and under strict compliance standards. This converter design incorporates multiple strategies to minimize noise generation and propagation.

Switching Behavior and Gate Drive Strategy

- **Gate drive timing** was carefully engineered to avoid overlapping conduction events, preventing hard-switching and minimizing radiated EMI.
- A **voltage-based phase delay system** ensures each of the four phases switches at staggered intervals (90° apart), reducing instantaneous current slew rate and limiting common-mode noise spikes.
- Phase interleaving naturally distributes switching transients over time, smoothing input and output waveforms and reducing harmonic content.

Component Selection for Noise Suppression

- **Output capacitors** were chosen with optimal ESR and ESL values to suppress both low- and high-frequency ripple:
    - A parallel bank of **68 µF + 470 nF + 47 nF** delivers broadband filtering performance.
- **Inductor values** were tuned to maintain current ripple within the ideal control window while avoiding high-frequency ringing that could elevate EMI.
- Gate drive networks were tuned for fast, clean transitions without excessive overshoot, balancing switching speed and EMI generation.

Layout and Topological Advantages

- The **4-phase interleaved boost topology** inherently reduces EMI by:
    - Lowering per-phase current magnitude
    - Minimizing net ripple on power rails
    - Canceling certain harmonic components in radiated emissions

- This structure also allows for tighter current loop geometry on PCB, a key factor in reducing loop inductance and radiated emissions.

Control Loop and Noise Rejection

- The feedback system employs a **Type III compensation network**, strategically placing poles and zeros to:
    - Maintain loop stability under real-world noise conditions
    - Suppress switching ripple coupling into the error signal path
    - Improve dynamic response without amplifying high-frequency disturbances

10.8 Future Work and Scalability

While the present design meets or exceeds its performance targets for efficiency, ripple, and control stability, several pathways exist for future enhancement and system scaling.

Synchronous Rectification Upgrade

- **Current Limitation**: The present design utilizes Schottky diodes (D1–D4) as freewheeling elements, offering simplicity and robustness at the cost of higher conduction losses during the freewheeling period.
- **Proposed Enhancement**: Replace diodes with **synchronous MOSFETs**, actively driven to reduce forward voltage drop and conduction losses.
- **Considerations**:
    - Potential efficiency gains under high current operation.
    - Increased complexity in **gate drive circuitry** and **dead-time management**.
    - Potential risks of shoot-through and control loop sensitivity.
- **Conclusion**: While not essential for the current 96.9% efficient implementation, synchronous rectification is a **strategic future upgrade**, especially under increased load conditions or for missions with tight thermal constraints.

Digital Control Integration

- **Motivation**: Analog control offers simplicity, but **digital controllers** (MCUs or DSPs) provide:
    - Real-time telemetry and diagnostic capabilities.
    - Fault detection, compensation tuning, and adaptive control.
    - Support for dynamic mission profiles or redundancy schemes.

- **Application Potential**:
    - Mission-critical systems requiring **self-correction**, **reconfiguration**, or **remote tuning**.
    - Integration with spacecraft bus communication protocols.
- **Conclusion**: Digital control is an **evolutionary next step**, offering fine-grained control over system behavior, and should be considered for future versions targeting **autonomous or long-duration missions**.

System Voltage Scaling

- **Architecture Strength**: The interleaved four-phase boost converter exhibits modularity and flexibility, making it an excellent base for:
    - **Stage 2 converters** (e.g., 100 V → 400 V).
    - **Final-stage high-voltage supplies** (e.g., 400 V → 1200 V for Hall-effect or gridded ion thrusters).
- **Scaling Considerations**:
    - Increased **MOSFET breakdown voltage** and **diode reverse voltage** ratings.
    - Enhanced insulation, creepage, and clearance requirements.
    - Possible migration to **resonant topologies** (e.g., LLC, PSFB) for better soft-switching and EMI performance at higher voltages.
- **Conclusion**: While further scaling may require topology changes, this converter serves as a **technically solid and scalable foundation**, particularly for propulsion applications requiring cascaded power architecture.