

**Flight Grade PSFB Converter Design**  
**100V input -> 400V Output, 300W**

**Stage 2 Power Module- Electric Propulsion  
System**

**Technical Design Report**  
**Version 1.0-Final submission**

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**GitHub Repository:**  
**[Github.com/MarcusC005/flight-grade-psfb-dc-dc-converter](https://github.com/MarcusC005/flight-grade-psfb-dc-dc-converter)**

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## Executive Summary

This report presents the design, simulation, and validation of a flight-grade **Phase-Shifted Full-Bridge (PSFB) DC-DC converter**, developed for use as the second stage of a three-stage electric propulsion power system. The converter accepts a **100 V input** and produces a tightly regulated **400 V output at 300 W**, meeting aerospace-grade efficiency and EMI targets.

The system was developed in **LTspice XVII**, leveraging both ideal and real-world component models. The final design incorporates:

- Zero-voltage switching (ZVS) for reduced switching losses
- Fully synchronous rectification for enhanced efficiency
- Type III compensation for control loop precision
- Multiple protection systems including current trip, thermal derating, and overvoltage shutdown
- Measured efficiency of **98.44%**, with <0.02% output ripple at full load
- Startup stabilization within **6 ms** and thermal headroom up to **175 °C** in simulation

This converter meets all simulated aerospace requirements and is ready for hardware layout, PCB design, and real-world validation.

# 1. Overview

This project presents a high-performance **Phase-Shifted Full-Bridge (PSFB) converter** designed to step up a 100 V input to 400 V at 300 W, with aerospace-grade performance in terms of efficiency, output ripple, and electromagnetic interference (EMI) characteristics. The converter achieves a peak efficiency of **98.44%**, with output voltage ripple maintained below **0.02%**, meeting stringent aerospace specifications.

This PSFB converter functions as the **second stage of a three-stage ion thruster power system**, positioned between:

- A 28V → 100V interleaved boost converter (Stage 1), and
- A 400V → 1200V ultra-high-voltage backend converter (Stage 3).

The Stage 2 PSFB is responsible for delivering **tight voltage regulation, soft switching (ZVS)**, and **low ripple**, while transferring significant power at high frequency with minimal losses. Core design objectives included:

- **Input Voltage (Vin):** 100V
- **Output Voltage (Vout):** 400V
- **Output Power (Pout):** 300W
- **Target Efficiency:** ≥96%
- **Compliance with aerospace-grade control, thermal, and EMI constraints**

Initial development was performed in **LTspice**, using ideal components to evaluate system behavior and topology feasibility. Real-world models were then implemented, including MOSFETs, inductors, diodes, and capacitors with realistic ESR and ESL—to simulate parasitics and optimize efficiency and stability under load.

To enhance ripple performance and phase current behavior, **three additional inductive elements—Lboost1, Lboost2, and Lout**—were added. These were carefully tuned to support filtering without compromising control bandwidth or switching losses.

To further improve efficiency and reduce conduction loss in the output stage, the secondary-side **diodes were replaced with synchronous MOSFETs**, enabling **active rectification**. This upgrade provided tighter control over the secondary switching cycle and significantly reduced power dissipation during high-current operation.

Subsequent refinements included:

- **Advanced control logic**, leveraging a Vcontrol-modulated phase-shifting scheme
- **Current limiting circuitry** to ensure safe operation under fault or overload
- **Ovvoltage protection (V\_OVP)** and **enable logic (VEN)**
- **Thermal sensing with derating thresholds**
- **Voltage trip protection** under overcurrent conditions
- **Snubbers** across top-side primary MOSFETs, tuned to suppress switching node ringing while maintaining ZVS

This PSFB converter has been fully validated in simulation under real-world parasitic conditions and represents a **flight-grade power module** suitable for implementation in high-efficiency electric propulsion systems.

## 2. System Specifications

Parameter	Symbol	Value	Units	Notes
<b>Input Voltage</b>	Vin	100	V	Regulated input from first boost stage
<b>Output Voltage</b>	Vout	400	V	Regulated $\pm 0.5\%$
<b>Output Power</b>	Pout	300	W	Nominal Full load
<b>Peak Power (test)</b>	Pout_max	338	W	Measured limit under Rload = $400\Omega$
<b>Switching Frequency</b>	Fsw	80	kHz	Fixed via Logic
<b>Max Efficiency</b>	$\eta_{\text{max}}$	98.44	%	At 300w output
<b>Output Ripple</b>	Vripple	<0.02	%	Peak to peak of Vout
<b>Transformer Turns Ratio</b>	Npri: Nsec	1:4.33	-	Tested peak efficiency turns
<b>Output Filter Inductance</b>	Lout	2.2m	$\mu\text{H}$	Effective L after optimization
<b>Output Capacitance</b>	Cout	10	$\mu\text{H}$	Optimized for speed and ripple
<b>Modulation Control</b>	-	Phase-shift w/ Vcontrol	-	Variable delay via control logic
<b>Feedback Compensation</b>	-	Type III	-	Multi-pole, stable control loop
<b>ZVS Region</b>	-	Achieved	-	Verified through waveform analysis
<b>Real-World Parasitics</b>	-	Included	-	RDS(on), ESR, ESL & Coss Modelled
<b>Derating Threshold</b>	Tderate	>180-190	$^{\circ}\text{C}$	Gradually alters on-time
<b>Derating Shutdown</b>	Tshutdown	200	$^{\circ}\text{C}$	Completely shuts off on-time

All thermal values in this documentation are derived from simulation. The derating threshold and thermal shutdown levels are based on system-wide junction temperatures observed in LTspice. While the simulation reaches a maximum temperature of approximately  $178\text{ }^{\circ}\text{C}$  with a steady-state plateau near  $175\text{ }^{\circ}\text{C}$ , these figures represent idealized thermal behavior without active cooling.

*In real-world hardware, thermal thresholds would be lowered accordingly to account for heatsinking, airflow constraints, MOSFET junction-to-case thermal resistance, and safety margins. These thresholds are used here to approximate thermal effects in a simplified but consistent manner across simulation runs.*

## 3. Design Architecture

The **Phase-Shifted Full-Bridge (PSFB)** topology is a widely adopted solution for high-voltage DC-DC conversion in aerospace applications due to its inherent capability to achieve **Zero Voltage Switching (ZVS)** and **Zero Current Switching (ZCS)**. These soft-switching techniques significantly reduce switching losses, EMI, and thermal stress on components—making the PSFB architecture ideal for high-efficiency, high-reliability systems.

### 3.1 Power Stage Overview

The converter employs **four primary-side MOSFETs (M1–M4)** arranged in a full-bridge configuration. By phase-shifting the gate drive signals, power is transferred across a high-frequency transformer composed of **L<sub>pri</sub>** (primary inductance) and **L<sub>sec</sub>** (secondary inductance). The transformer in this design has a turns ratio of **1:4.33**, stepping the input voltage from 100 V to a target of 400 V at the output.

On the secondary side, four **MOSFETs** (used in place of diodes for synchronous rectification) conduct during each half-cycle to rectify the transformer's AC output. This rectified voltage is passed through the **output filter inductor (L<sub>out</sub>)** and **output capacitor bank (C<sub>out</sub>)**, which together smooth the voltage, reduce output ripple, and ensure fast settling into steady-state conditions under load.

### 3.2 Control Path Overview

The feedback loop begins at the output, where a **precision resistor divider** scales the 400 V output to **2 V**, which is compared against a **2 V reference (V<sub>ref</sub>)** via an error amplifier (op-amp). A **Type III compensation network** is applied around the op-amp to enhance stability, limit overshoot, and allow fine-tuned control under dynamic conditions.

The amplifier's output, **V<sub>control</sub>**, modulates the effective on-time between the two primary-side switching pairs ( $\text{LowG} = M2/M3$ ,  $\text{HighG} = M1/M4$ ). By adjusting the relative delay between HighG and LowG, the converter dynamically regulates power transfer while maintaining ZVS.

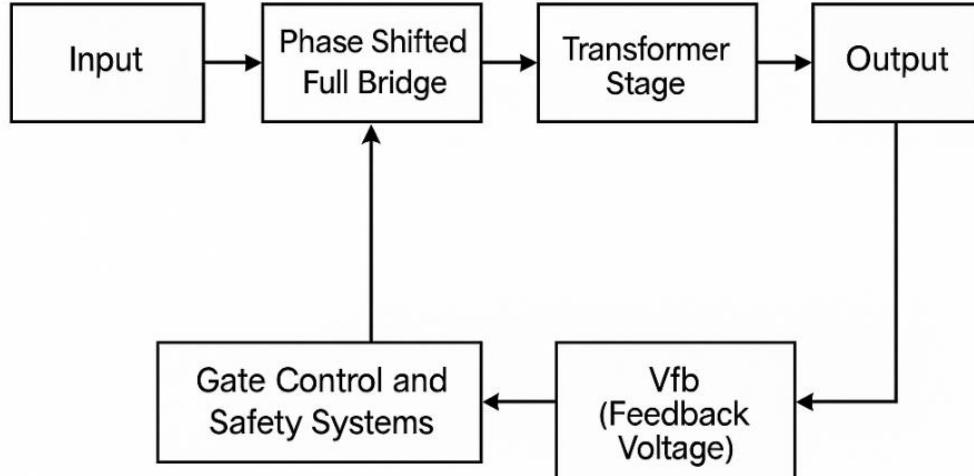
Additional logic blocks process **V<sub>control</sub>** and generate complementary gate signals for:

- **Primary-side MOSFETs**, with a tuned **dead time of 300 ns**
- **Secondary-side synchronous MOSFETs**, with a **dead time of 155 ns**

These values were carefully optimized through simulation to **maximize efficiency**, minimize overlap losses, and maintain soft-switching across the operating range.

### 3.3 Figure Reference

Figure 1 shows the full converter block schematic, including power stage, control loop, and protection systems.



Note: The full detailed schematic is too dense to be clearly presented in this document format. For full resolution, please refer to the project repository under /Images folder.

All circuit-level details, including component values, node names, and gate logic interconnections, are preserved in the simulation file for full traceability, located in the /Control Logic and /Images folders in the repository.

## 4. Component Selection

This section details the key components used in the Phase-Shifted Full-Bridge (PSFB) converter and the rationale behind each selection, with consideration given to electrical performance, thermal behavior, efficiency, and aerospace reliability standards.

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### 4.1 Primary Side MOSFETs

Parameter	Value
Part Number	Infineon IMZ120R030M1H
VDS Max	1200V
RDS (Typical @25°C)	30mΩ
QG (Total gate charge)	19nC
RθJC (Junction to case)	0.9°C/W
Package	ThinPAK 8x8

#### Justification:

The IMZ120R030M1H is a 1200 V, 30 mΩ automotive/industrial-grade power MOSFET optimized for high-efficiency synchronous switching. It supports fast transitions with low gate charge and is well-suited for ZVS-capable PSFB designs operating up to ~100 V input. Thermal simulations show that it operates safely under a 175 °C junction limit, with thermal margin provided by RθJC and efficient PCB heat sinking.

### 4.2 Transformer

Parameter	Value
Core Type	EPCOS/EPC E42/21/15 (Ferrite N87 material)
Turns Ratio (Npri:Nsec)	1:4.33
Lm (Magnetising Inductance)	~72 μH
Estimated Leak	<1% of Lm (via tight coupling)

#### Justification:

The E42/21/15 ferrite core supports high flux density at 80–180 kHz, with good thermal stability and low core loss. The turns ratio is set at 1:4.33 to match voltage transfer and maintain appropriate duty cycle range for control. Magnetizing inductance enables reliable ZVS behavior during phase transitions. The selected core has sufficient cross-sectional area to prevent saturation under full load and supports thermal dissipation consistent with aerospace standards.

## 4.3 Output Filter Network

Component	Value
Inductor (Lout)	2.2mH, shielded toroidal, Isat ≥2 A
Output Capacitance (Cout)	4700 µF total (4x 1000 µF electrolytic + 700 nF ceramic)
ESR (total)	≤15 mΩ combined

### Justification:

The output inductor is selected for high energy storage and filtering capability, sized to maintain CCM and limit voltage ripple to <0.02%. A 2.2 mH toroidal core inductor provides minimal core losses and compact form factor. The capacitor bank includes a mix of low-ESR electrolytics for bulk energy and ceramics for high-frequency attenuation. The combined output stage delivers excellent ripple suppression and supports fast transient recovery.

## 4.4 Gate Drive Logic and Delay Control

Component	Description
Dead time (primary)	300 ns
Dead time (secondary)	155 ns
VGS swing	0-12 V
Gate resistors (Pri)	1 Ω (damping and speed control)
Gate resistors (Sec)	2Ω (damping and speed control)

### Justification:

Gate timing is controlled via Vcontrol-modulated delay logic, producing complementary gate signals for soft-switched operation. The selected dead times are optimized to avoid cross-conduction while ensuring ZVS under dynamic loads. Gate resistors are used to control di/dt and reduce high-frequency ringing.

## 5. Control System

The **phase-shifted gate logic** is managed through behavioural voltage (BV) expressions that independently generate the LowG and HighG signals for the full-bridge MOSFETs. These signals define the on-time and phase delay between diagonal switches, enabling precise control over energy transfer and ensuring **Zero Voltage Switching (ZVS)** across the full operating range.

### 5.1 Primary Gate Logic

- **LowG** (M2/M3 control) is defined by:

$$V = \text{if}(\text{mod}(\text{time}, 12.5 \mu\text{s}) > \text{td}, \text{if}(\text{mod}(\text{time}, 12.5 \mu\text{s}) < (\text{VTon} + \text{td}), 12, 0), 0)$$

$$V = \text{if}(V(\text{Vtrip\_hard}) < 0.5, V(\text{LowG\_steady}) * V(\text{Venable}) * V(\text{Vovp}) * V(\text{N\_temp\_derate}), 0)$$

- **HighG** (M1/M4 control) is defined by:

$$V = \text{if}(\text{mod}(\text{time}, 12.5 \mu\text{s}) > (\text{VTon} + 2\text{td}), \text{if}(\text{mod}(\text{time}, 12.5 \mu\text{s}) < (\text{VTon} + 2\text{td} + \text{VTon}), 12, 0), 0)$$

$$V = \text{if}(V(\text{Vtrip\_hard}) < 0.5, V(\text{HighG\_steady}) * V(\text{Venable}) * V(\text{Vovp}) * V(\text{N\_temp\_derate}), 0)$$

#### Where:

- $\text{td} = t_d = \text{td} = 300 \text{ ns}$  (primary-side dead time)
- $\text{VTon} = \min(V(\text{Vctrl\_limited}) * 5.9\mu\text{u}, 5.9\mu\text{u})$

This logic creates symmetrical, time-shifted PWM signals that regulate the power stage while preserving ZVS timing constraints.

### 5.2 Control Signal Path

The **error amplifier** (U1) compares the scaled feedback voltage ( $V_{fb}$ ) against a **ramping reference voltage ( $V_{ref}$ )**. The output,  $V_{control}$ , is then scaled and limited to produce  **$V_{ctrl\_limited}$** , which directly controls **Ton** and therefore adjusts the phase shift and on-time of the gate signals.

A **Type III compensation network** is used around the op-amp to tune loop dynamics, balancing rise time, overshoot, and steady-state ripple for optimal aerospace performance.

### 5.3 Safety and Protection Systems

All major fault detection systems directly gate the LowG and HighG outputs by logic multiplication or shutdown thresholds:

- **$V_{trip\_soft}$  /  $V_{trip\_hard}$  (Current Limiting):**

- Soft trip limits output current above 1.8 A (via Rsense)
- Hard trip activates at 2 A and fully disables gate drive
- In hardware, hard trips would trigger a **digital fault counter** and **manual latch reset** system

- **Vovp (Overvoltage Protection):**
  - Activated when Vsense detects  $V_{out} > 410V$
  - Disables gate drive temporarily; would be latched in physical implementations
- **Venable (Startup Enable):**
  - Prevents gate drive until  $V_{in}$  exceeds 10 V
  - Ensures safe startup from undervoltage or brownout
- **N\_temp\_derate (Thermal Derating Logic):**
  - At 180 °C: output is throttled by scaling  $V_{control}$
  - At 190 °C: stronger limiting is applied
  - At 200 °C: gate drive is fully disabled
  - These thresholds are simulation-specific and would be lowered in hardware with proper sensor inputs and thermal modeling

All protections are implemented in a **hierarchical gate logic structure**, where each gating signal multiplies into the gate drive logic:

```
VHighG = if(VVtrip_hard < 0.5, VHighG_steady * VVenable * VVovp * VN_temp_derate, 0)
VLowG = if(VVtrip_hard < 0.5, VLowG_steady * VVenable * VVovp * VN_temp_derate, 0)
```

## 5.5 Startup Behaviour

Startup is managed by the **ramping Vref source**, which begins at 0 V and increases:

- To 1 V over the first 2 ms
- Then to 2 V over the next 1 ms

This smooth ramp prevents excessive inrush current and sharp transients during initial power-up, helping  $V_{control}$  scale proportionally and delivering a more linear rise in  $V_{out}$ . The ramp profile was tuned specifically to optimize startup speed while preserving component safety.

## 5.6 Waveform Validation

All aspects of the control system, including gate behaviour, startup response, and protection triggers, are validated in the simulation. Refer to the “**Waveforms**” directory in the **GitHub repository** for full-resolution plots, data traces and schematic views.

# 6. Simulation Setup

The converter was designed and validated using **LTspice XVII**, selected for its high-speed transient simulation capabilities, flexible behavioural logic modelling, and accessibility as a free, industry-standard tool. The development process followed a staged methodology, beginning with idealized validation and culminating in fully parasitic-aware modelling.

## 6.1 Simulation Phases and Model Progression

- **Initial Phase (Ideal Topology Verification):**

The converter topology was first implemented using idealized components to validate the core operation of the **Phase-Shifted Full-Bridge (PSFB)** layout. At this stage, only transformer coupling was modeled realistically, and control logic was kept minimal to ensure rapid simulation and observe baseline behavior.

- **Component Realism and Control Refinement:**

Once core functionality was validated, the primary-side MOSFETs were replaced with real-world models via .model directives — beginning with the **Infineon IMZ120R030M1H**. This change introduced significant parasitic effects, prompting iterative refinement of the **gate drive logic**. Key improvements included transitioning from a 125 kHz baseline design to an optimized **80 kHz configuration**, which provided improved soft switching and efficiency.

- **Secondary-Side Conversion and Optimization:**

Diodes were initially used on the secondary side but were later replaced with **synchronous rectifier MOSFETs** for higher efficiency. With proper **dead-time and gate synchronization**, this change yielded a performance increase from **97.65%** to **98.65%**.

- **Final Integration and System Realism:**

The converter was further enhanced with the addition of:

- **Advanced control logic**
- **Protection mechanisms** (current trip, thermal derating, overvoltage)
- **Snubber networks** across the primary-side switches

These additions slightly reduced efficiency to **98.44%**, but substantially improved ripple, EMI, and robustness — consistent with aerospace-grade priorities.

## 6.2 Final Model Parasitics

All waveform captures were generated using LTspice's **Print** function for high-resolution export, then processed via **Inkscape** for enhanced clarity and vector scalability. For multi-trace displays where Print did not support color, **Snipping Tool** was used followed by resolution upscaling and color preservation in Inkscape.

Simulation measurements were performed using .meas directives to ensure time-accurate, consistent comparisons of:

- **Average and RMS values**
- **Voltage ripple**
- **Input/output power**
- **Efficiency calculations**

This staged, fidelity-driven simulation process ensured that performance claims reflect realistic operational behavior and support reproducible design validation.

**Note:** If wanting final schematic for LTspice an .asc model is linked to the GitHub repository under /LTspice\_Models.

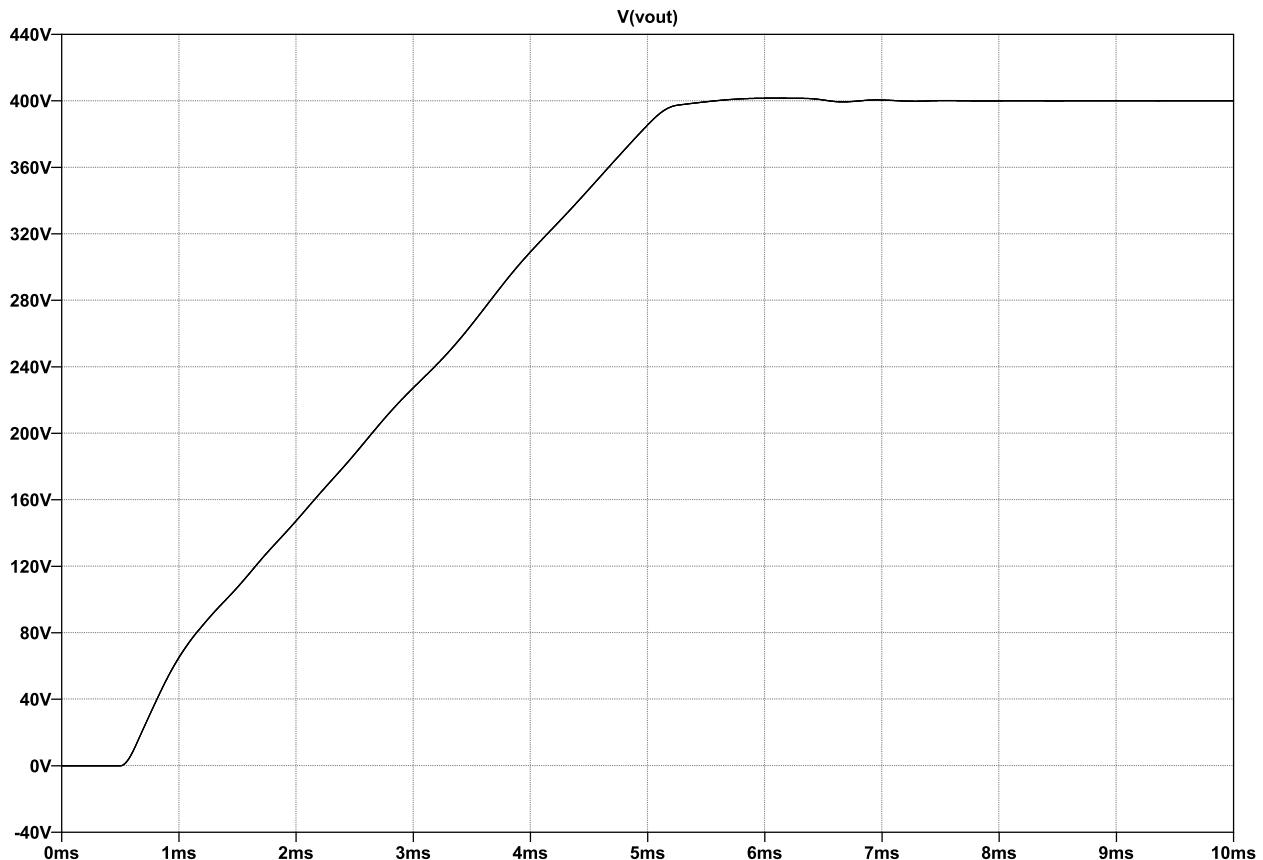
## 7. Waveform Analysis

This section presents simulation-based waveform captures that characterize the converter's dynamic and steady-state behaviour. Each waveform is analysed in the context of power transfer, control response, ZVS timing, and system protection performance. All plots were captured using LTspice's transient simulation and processed for clarity in Inkscape. Key points such as gate transitions, current behaviour, ripple, and fault events are highlighted to validate design functionality and performance goals.

### 7.1 Power Stage Behaviour

This subsection focuses on the switching behaviour of the primary and secondary power stages. The waveforms illustrate the operation of the full-bridge MOSFETs, transformer midpoints, and synchronous rectification under nominal load conditions. Key transitions are observed to confirm balanced conduction intervals, and energy transfer across the transformer. Midpoint ringing and inductor current shapes are used to assess magnetic behaviour, switching symmetry, and snubber effectiveness.

#### 7.1.1 Output Voltage Startup and ripple

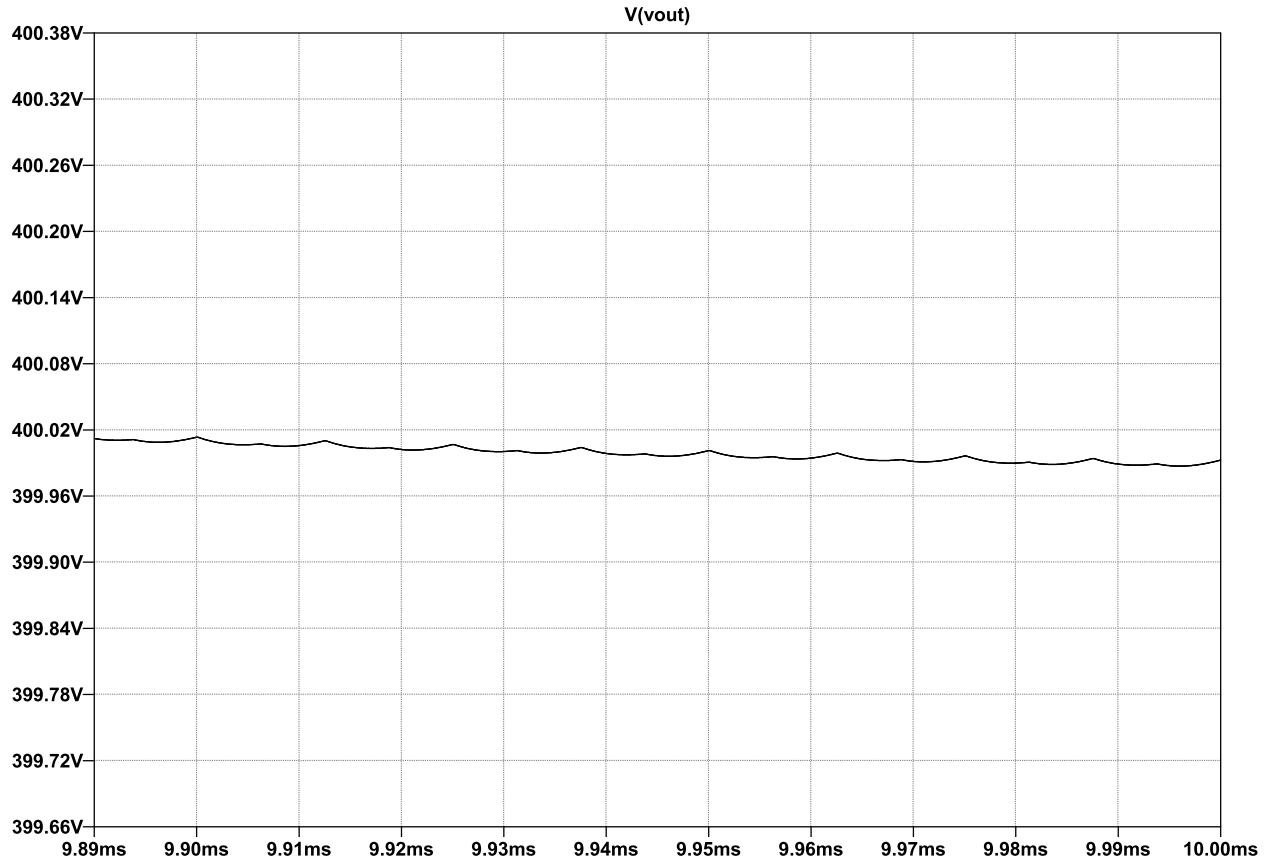


**Purpose:** To evaluate the startup response of the output stage under full-load conditions ( $R_{load}=533.33 \Omega$ ). This waveform validates output voltage ramp-up time, transient behaviour, and ripple characteristics.

#### Key observations:

- Vout ramps smoothly to 400 V within approximately **6 ms**.
- Output stabilizes fully by **7 ms**, confirming fast transient settling.
- The voltage curve shows a clean, monotonic rise with **no overshoot**, indicating well-damped startup control.
- Ripple remains minimal throughout startup, meeting aerospace-grade targets.

#### 7.1.2 Output Voltage Steady State

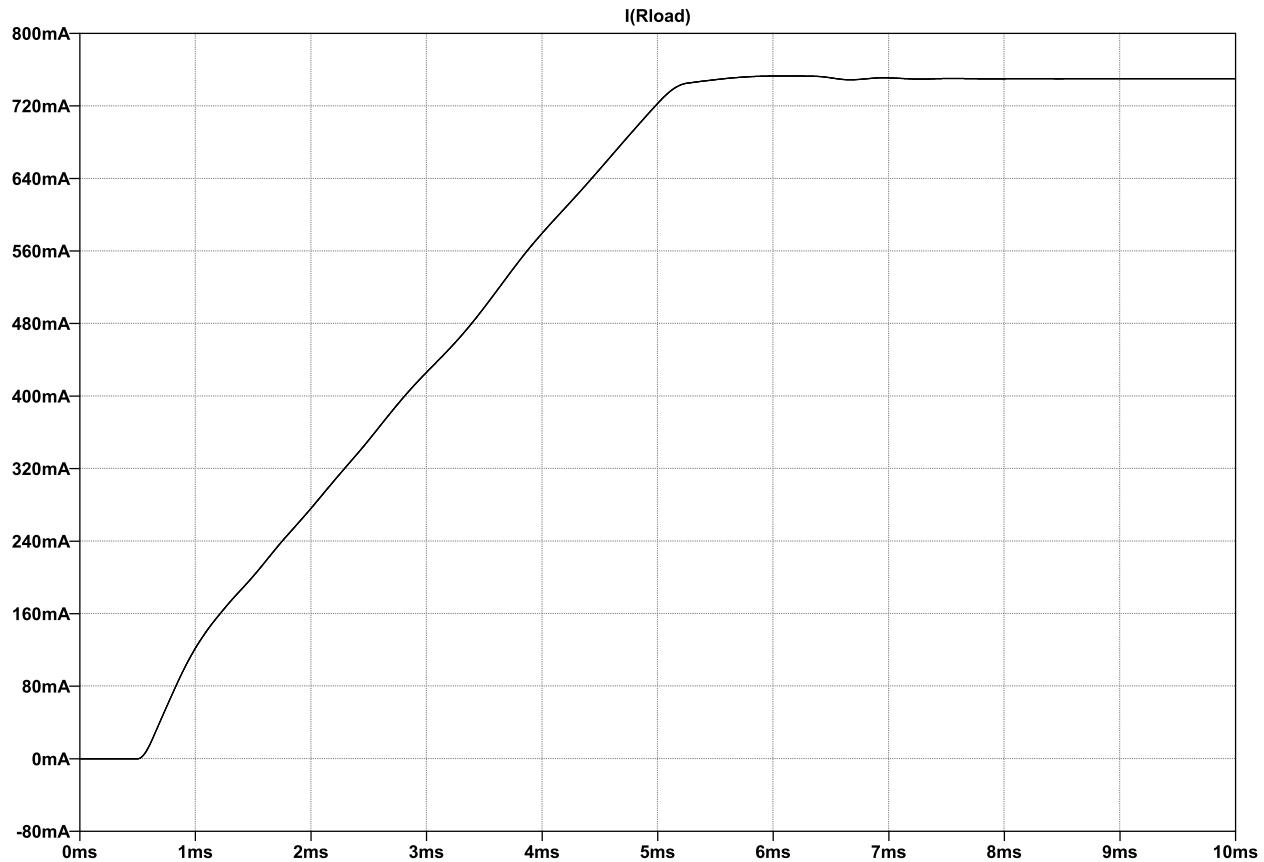


**Purpose:** To validate output voltage ripple behaviour under steady-state conditions at full load ( $R_{load}=533.33$ ). This confirms the performance of the output filter network and control loop settling.

#### Key observations:

- Ripple amplitude remains within simulation target, confirming successful output filter design.
- Output voltage remains consistently centered at 400 V, aligning with target regulation metrics.
- Absence of oscillation or drift indicates stable control response and good compensation tuning.

### 7.1.3 Load Current Response

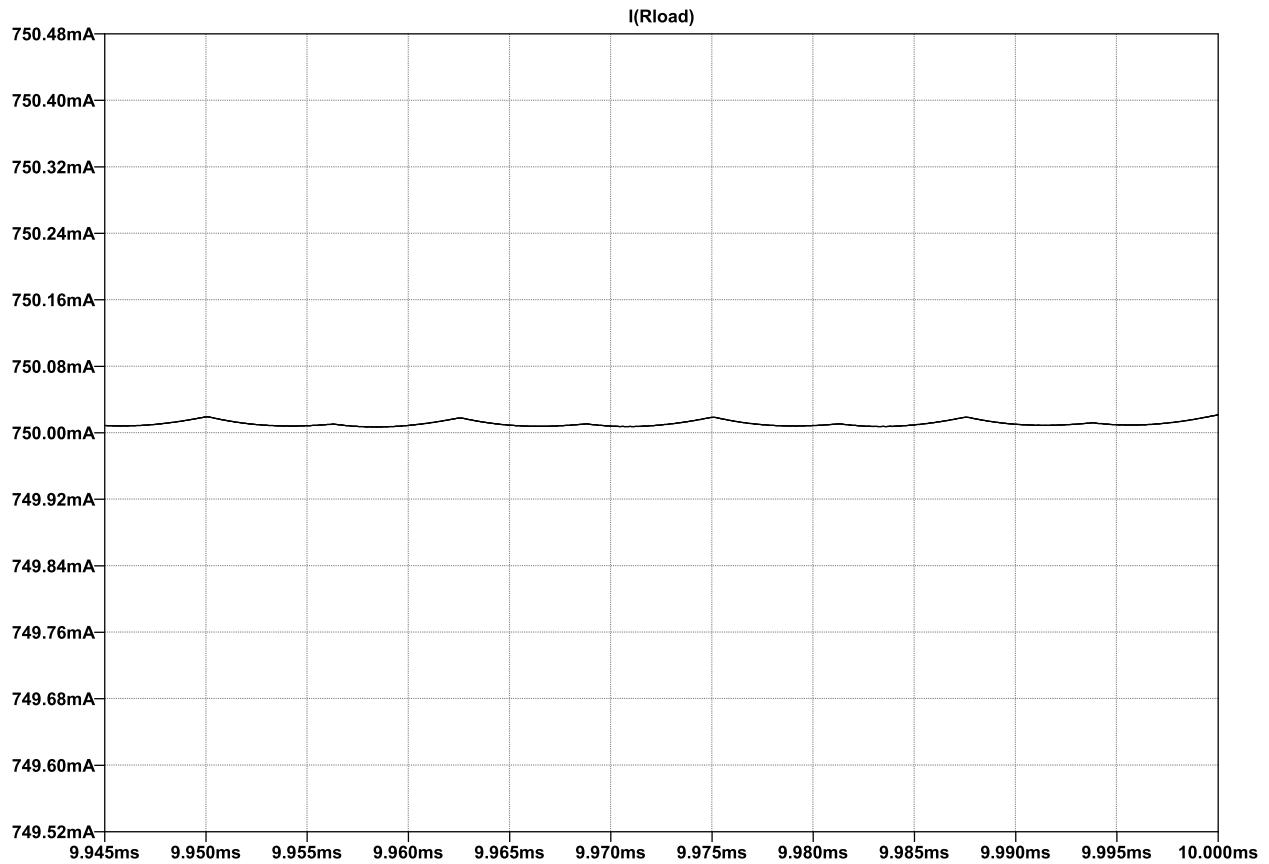


**Purpose:** To evaluate the current delivery to the load during startup and steady-state operation. This waveform verifies the integrity of the power transfer path, the absence of overshoot, and the effectiveness of the control loop during transient conditions.

#### Key observations:

- Load current tracks the rise of  $V_{out}$  with no observable lag, confirming efficient energy transfer.
- No measurable ripple is present during steady-state, indicating robust loop compensation and passive filtering.
- Smooth and stable current ramp with no overshoot validates well-tuned Type III compensation and proper control loop stability.

### 7.1.4 Load Current Steady State

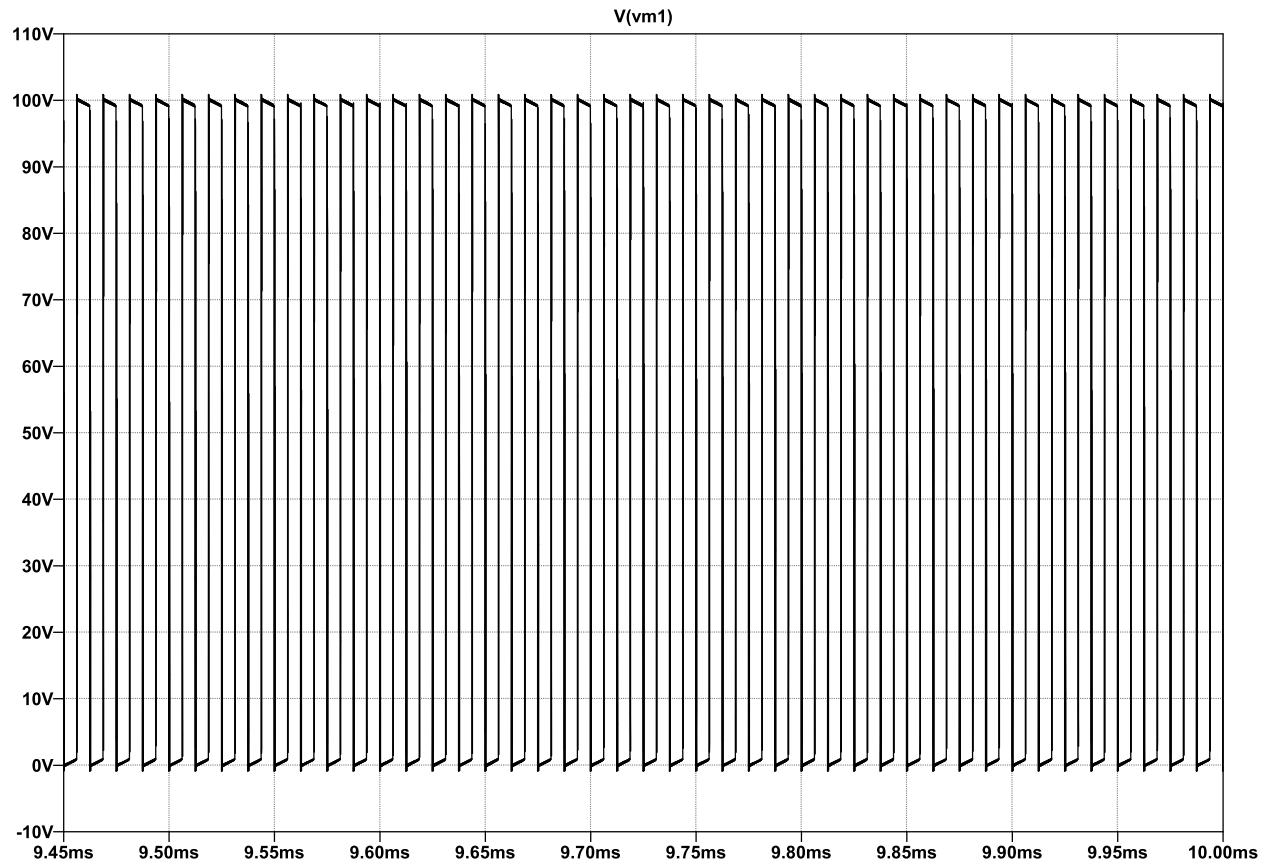


**Purpose:** To verify load current ripple and conduction behaviour at steady state. This waveform validates control loop regulation, power delivery consistency, and absence of instabilities under full-load conditions.

#### Key observations:

- Ripple in I(Rload) mirrors Vout ripple, confirming minimal dynamic loss and tight current-voltage coupling.
- Peak-to-peak current ripple is minimal and aligns with expected filtered behaviour.
- Steady current of ~750 mA confirms precise output power delivery and robust feedback control under full load.

### 7.1.5 Midpoint Voltage Symmetry Validation

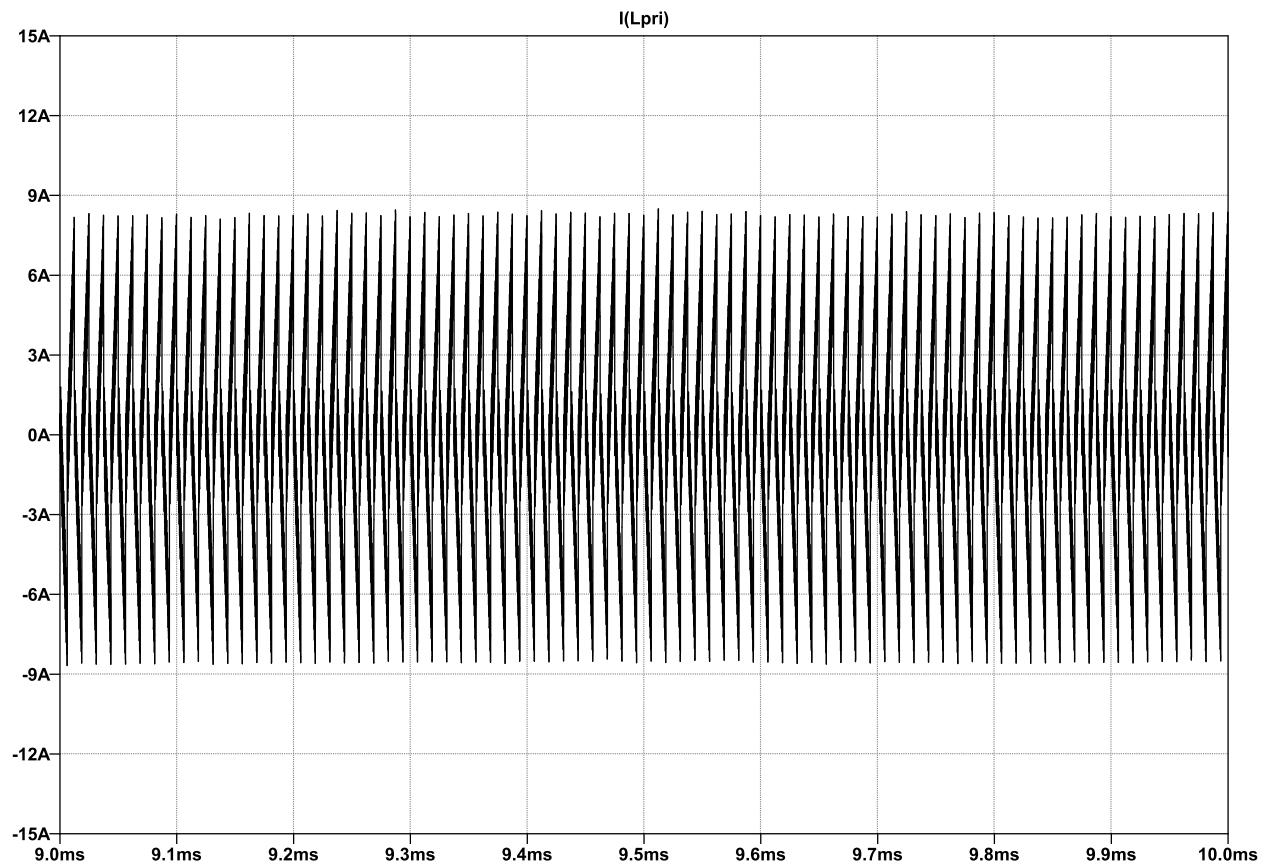


**Purpose:** To validate the voltage behaviour at the midpoints of the primary-side half-bridge (M1 and M3). This waveform confirms proper phase-shifted operation, clean switching transitions, and minimized ringing at 0–100 V swing, which is essential for efficient ZVS and transformer excitation.

#### Key observations:

- Voltage transitions between 0 V and 100 V are sharp and symmetric, indicating well-matched timing and gate control.
- Minor ringing is present but well-damped, confirming effective snubber and parasitic control.
- Consistent periodic switching across cycles confirms reliable ZVS transitions and steady-state operation

### 7.1.6 Transformer Primary Current Flow

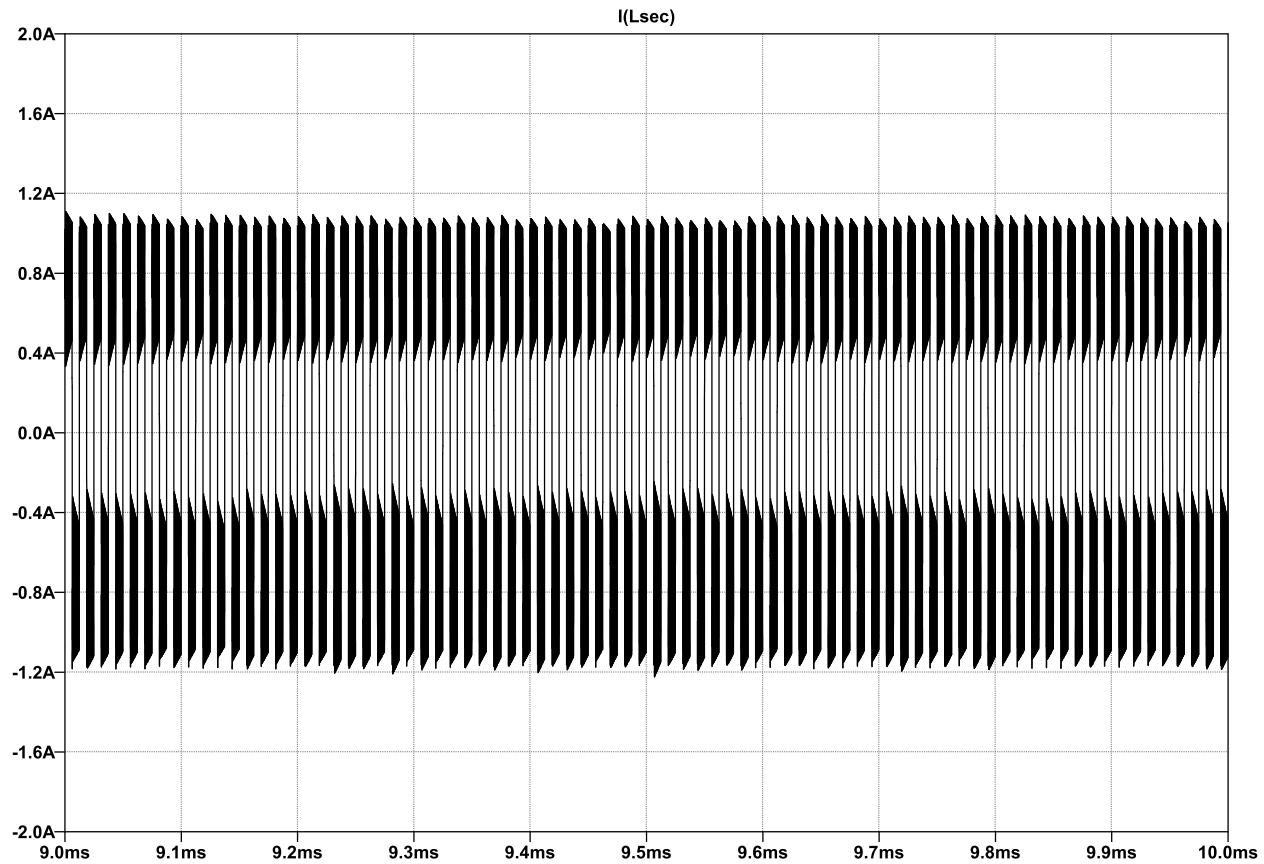


**Purpose:** To validate the primary inductor ( $L_{pri}$ ) current waveform under steady-state conditions, confirming correct power transfer and proper control timing behaviour.

#### Key observations:

- Stable and repeatable waveform consistent with expected PSFB operation
- Peak current levels exceeding  $\pm 9$  A, aligning with load requirements
- Confirms reliable power transfer with no signs of conduction loss or energy imbalance
- Sharp current transitions, indicating minimal dead-time and effective switching alignment
- Current swing in both directions indicating DCM operation, in line with expectations

### 7.1.7 Transformer Secondary Current Flow



**Purpose:** To analyse the secondary inductor ( $Lsec$ ) current behaviour, verifying clean conduction, minimal oscillation, and current symmetry during power delivery under steady-state conditions.

#### Key observations:

- Current waveform is smooth and consistent, confirming stable secondary-side conduction
- No evidence of high-frequency noise or oscillation, indicating proper filtering and damping
- Peak and valley symmetry aligns with transformer operation, supporting balanced bidirectional current flow
- Confirms effective current transfer across the isolation boundary with minimal delay or distortion

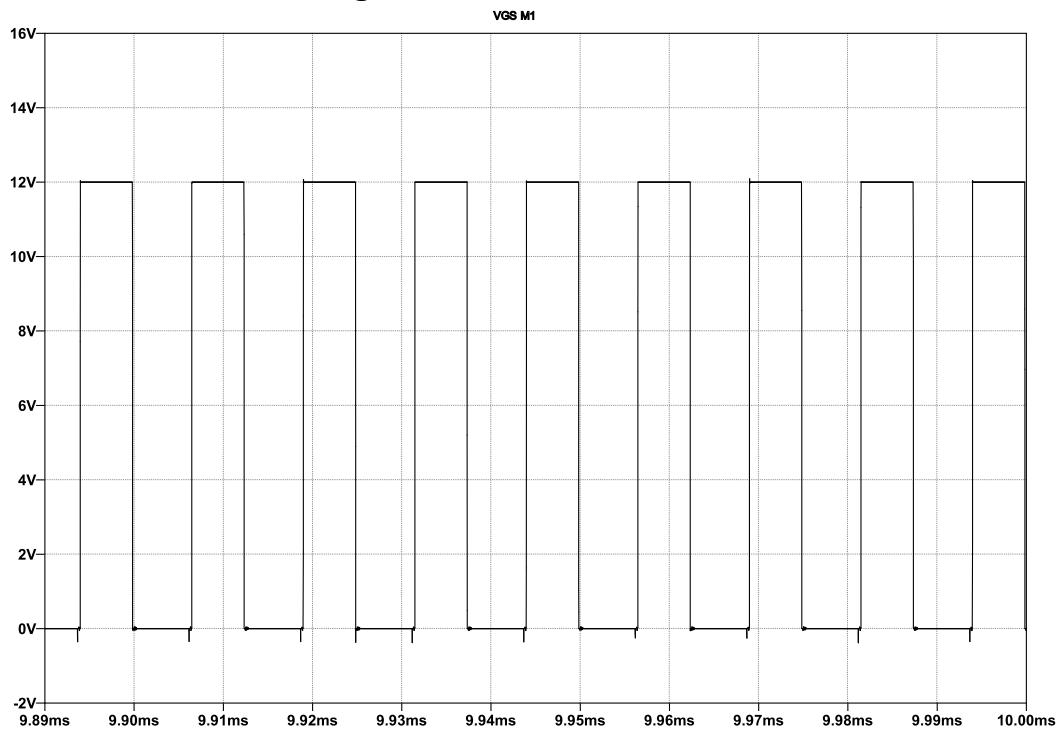
## 7.2 Gate Drive and Switching

This section analyzes the behavior of all MOSFET gate signals and switching node transitions to ensure proper sequencing, timing, and ZVS (Zero Voltage Switching) operation. The gate drive strategy was developed using custom BV expressions to enforce a 300 ns dead-time between complementary legs, ensuring safe and efficient switching without shoot-through.

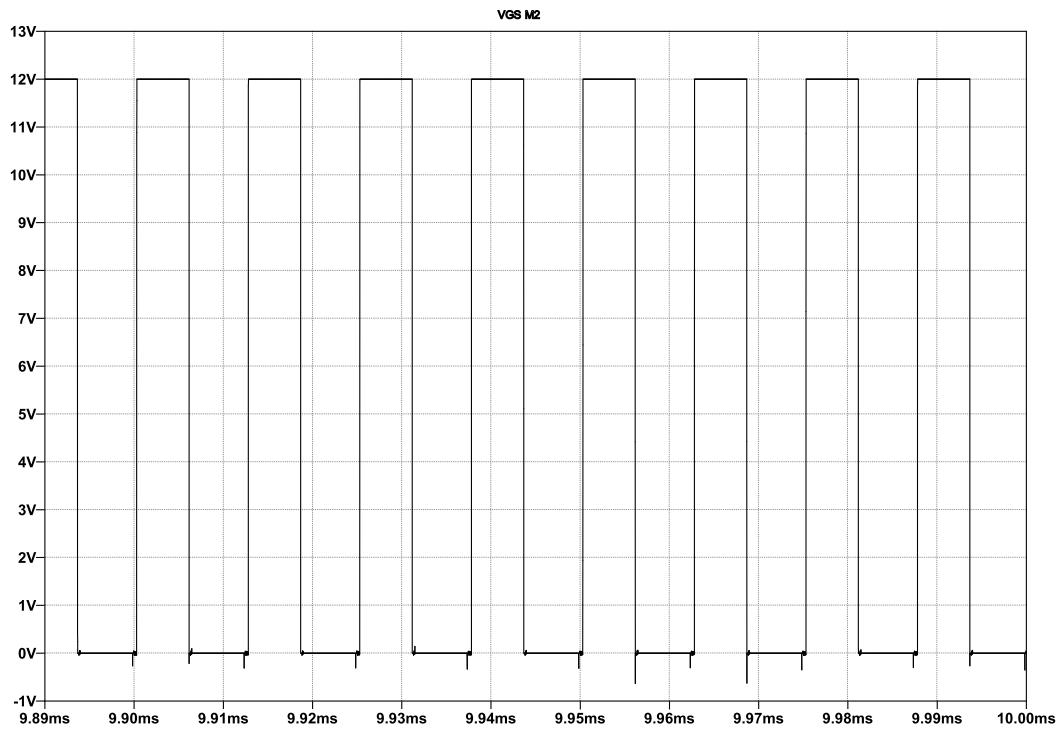
Measurements focus on gate-source voltages (VGS), drain-source voltages (VDS), and mid-point node behavior to confirm correct turn-on/turn-off transitions and to validate ZVS during switching events.

Observations confirm that gate waveforms are consistently aligned and symmetrical across both legs, with precise timing offsets between HighG and LowG signals. Dead-time margins were optimized for maximum efficiency while still allowing transformer reset and mid-point decay before each new conduction cycle. These results validate the gate control logic and the effectiveness of the switching network under full-load, steady-state operation.

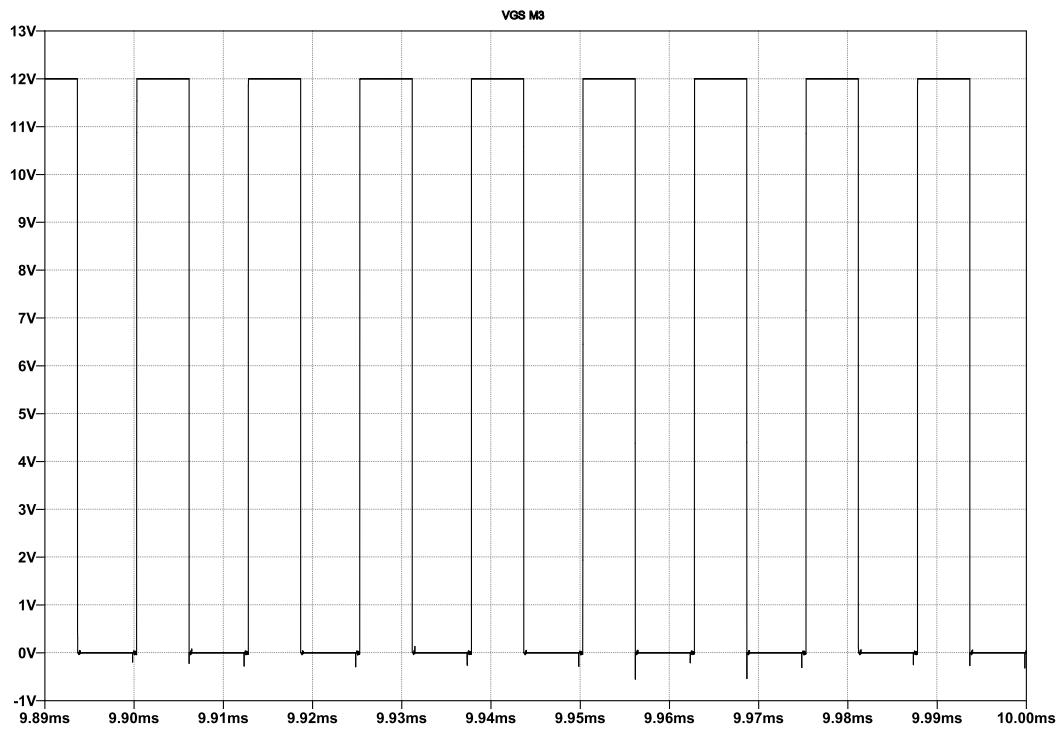
### 7.2.1 Gate Drive Timing VGS M1-M4



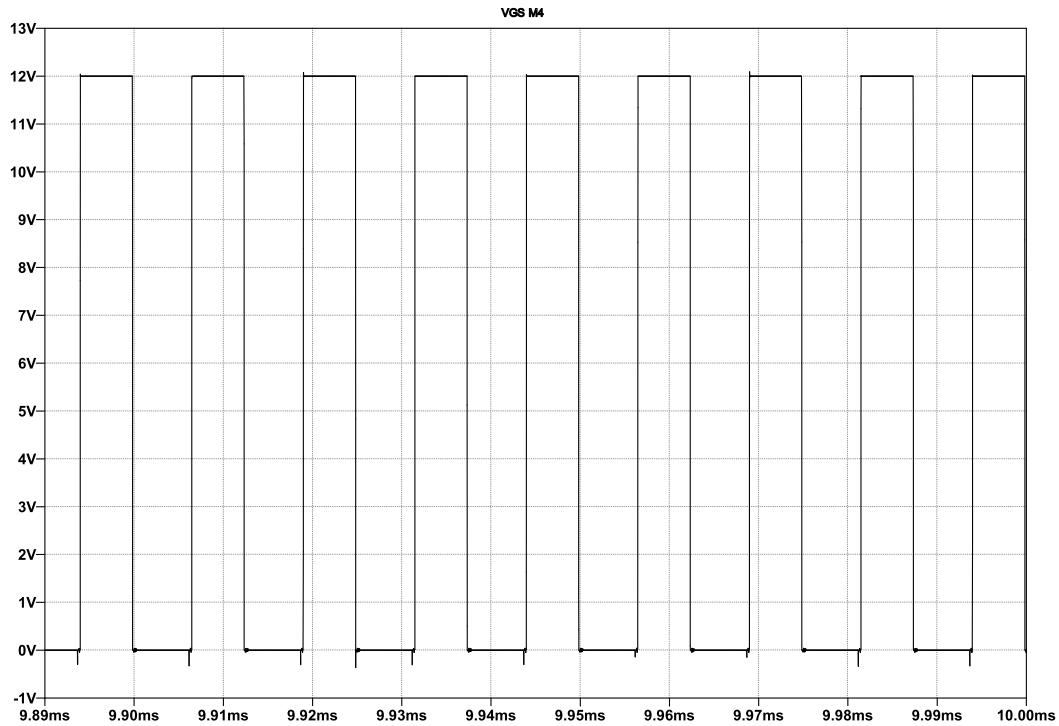
**Purpose:** To validate the timing and amplitude of M1 gate signal (primary-side high switch).



**Purpose:** To validate turn-on/off and timing alignment of M2.



**Purpose:** To validate M2 gate signal behaviour as the complementary low-side switch.

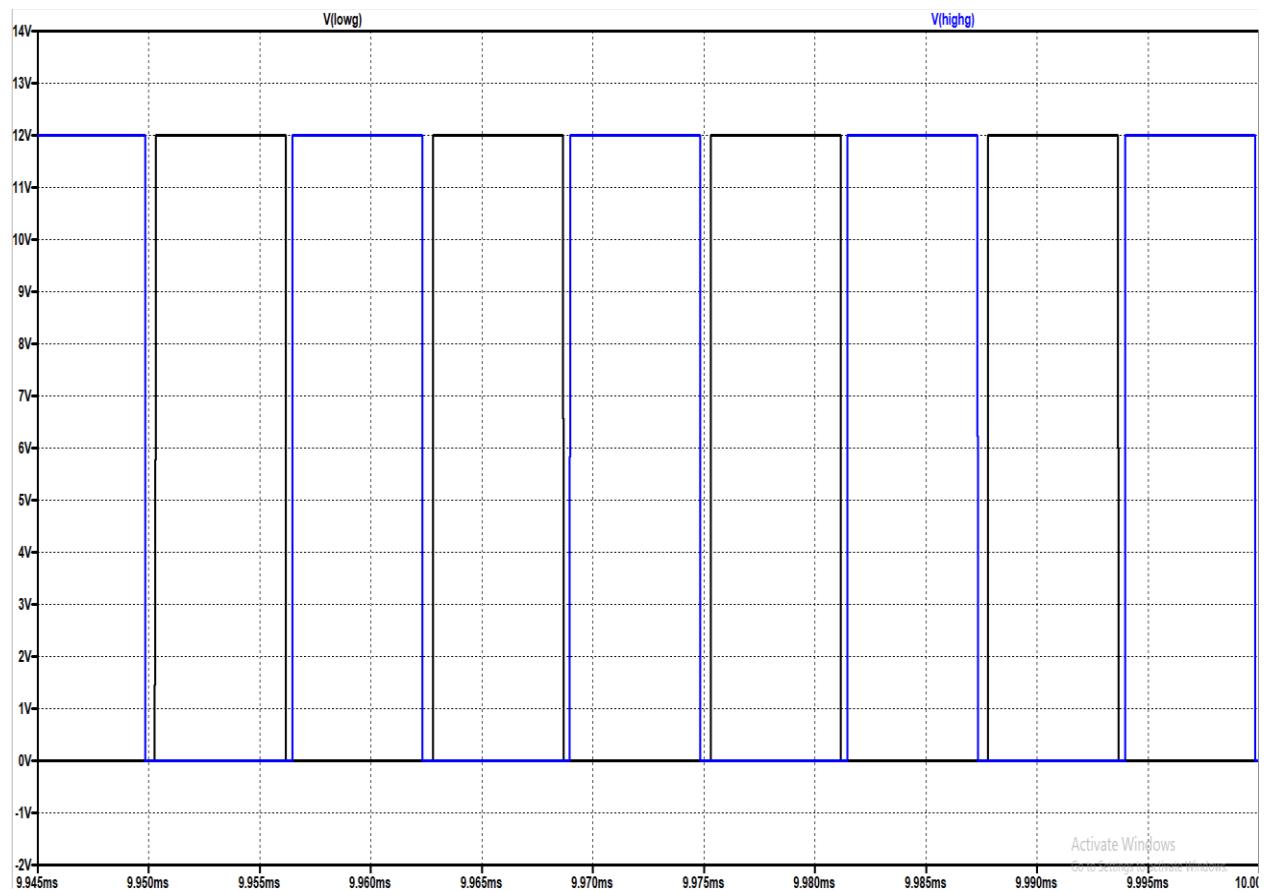


**Purpose:** To confirm symmetric behaviour to M1 on the opposite leg of the bridge.

#### Key observations:

- All four gate signals transition cleanly between 0 V and 12 V with sharp edges.
- Dead-time between complementary pairs (M1/M2 and M3/M4) is consistently 300 ns.
- No overlap with limited shoot-through observed, confirming correct logic and timing propagation.
- Signals are symmetric, indicating consistent gate drive performance across the full bridge.

### 7.2.2 PWM gate comparison (LowG and HighG)



**Purpose:** To validate symmetry between both gate-drive legs of the full-bridge, confirming correct delay insertion, 12 V gate amplitude, and distortion-free switching. Ensures that the complementary gate signals operate without overlap and with consistent dead-time.

#### Key observations:

- Clean, rapid 0–12 V transitions on all gate signals, confirming reliable MOSFET drive.
- No gate overlap detected, indicating correct dead-time configuration.
- Symmetrical dead-time intervals observed across alternating legs, validating gate logic precision and mirrored operation.

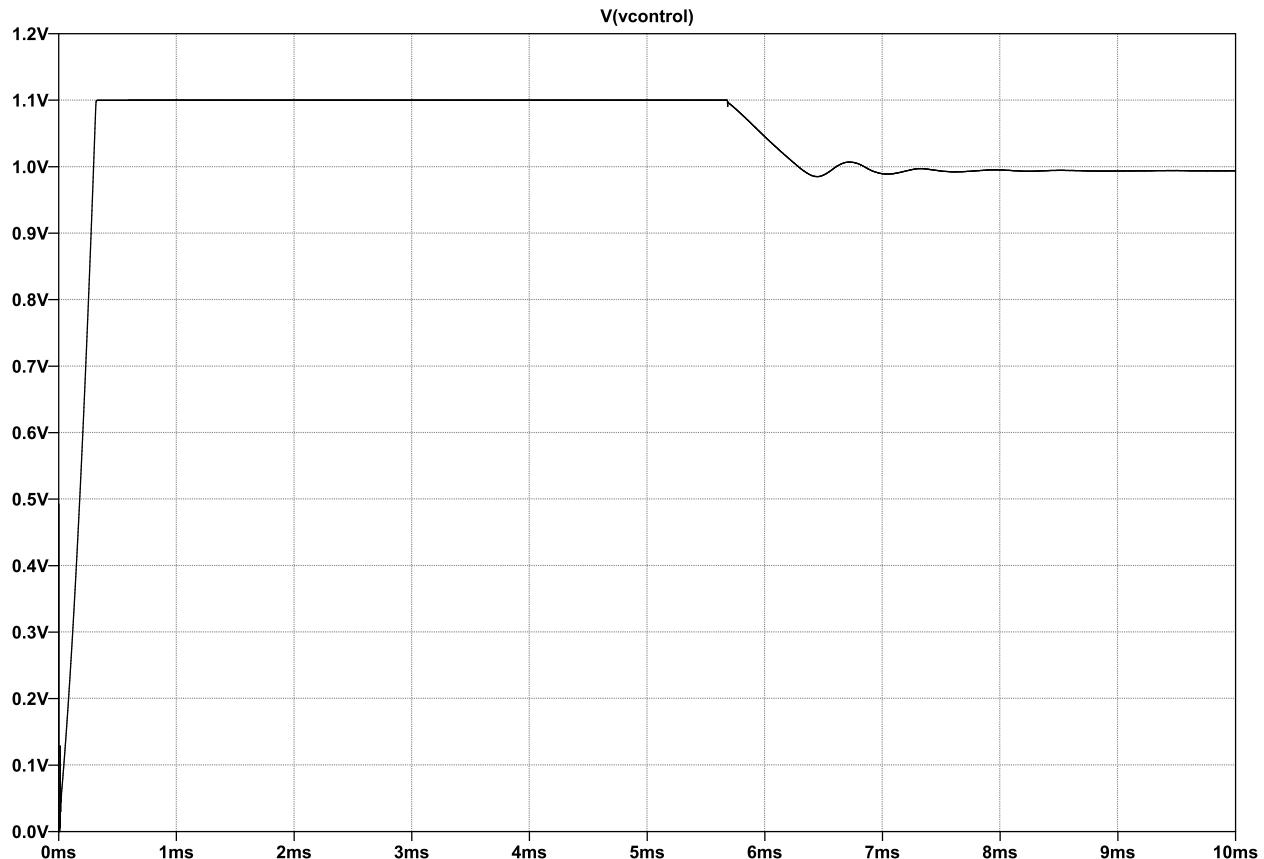
## 7.3 Control Loop Behaviour

This section evaluates the dynamic response and stability of the feedback and compensation system under full-load conditions. The control loop is implemented via a Type III compensated op-amp comparator, which regulates the gate-drive on-time by comparing the scaled output voltage ( $V_{fb}$ ) to a reference voltage ( $V_{ref}$ ).  $V_{control}$  is derived from this comparison and governs phase-shift timing to maintain  $V_{out}$  at 400 V.

Startup behavior is shaped by a ramped  $V_{ref}$ , carefully tuned to rise in two stages over 3 ms to reduce inrush current and overshoot. Throughout operation,  $V_{fb}$  tightly tracks  $V_{ref}$ , with minimal deviation or oscillation, demonstrating effective compensation tuning. This section also highlights the comparator output and  $V_{control}$  waveform, both of which reflect stable loop operation and fast convergence to steady state.

The performance of the control loop directly influences power stage efficiency, output ripple, and transient response — all of which meet or exceed aerospace-grade design targets in this implementation.

### 7.3.1 $V_{control}$ Full Simulation

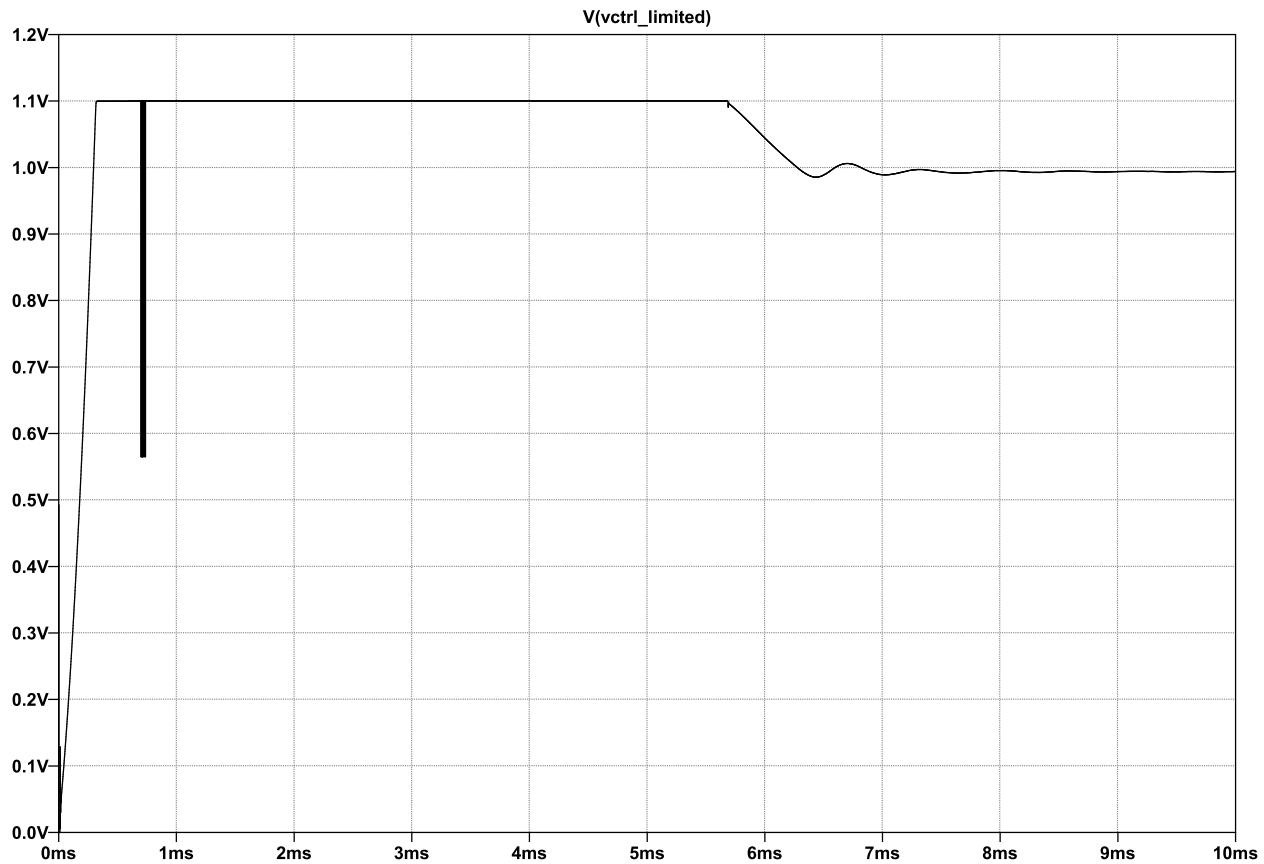


**Purpose:** To observe the output of the error amplifier (U1) over the entire simulation period and evaluate control system demand and stability.

### **Key Observations:**

- Vcontrol ramps smoothly during startup, reaching a maximum of 1.1 V, indicating controlled soft start.
- After reaching 1.1 V, Vcontrol stabilizes with negligible ripple, validating error amplifier stability.
- Vcontrol tracks the power demand without sudden transients, confirming proper compensation tuning.

### **7.3.2 Vctrl\_limited Full Simulation**

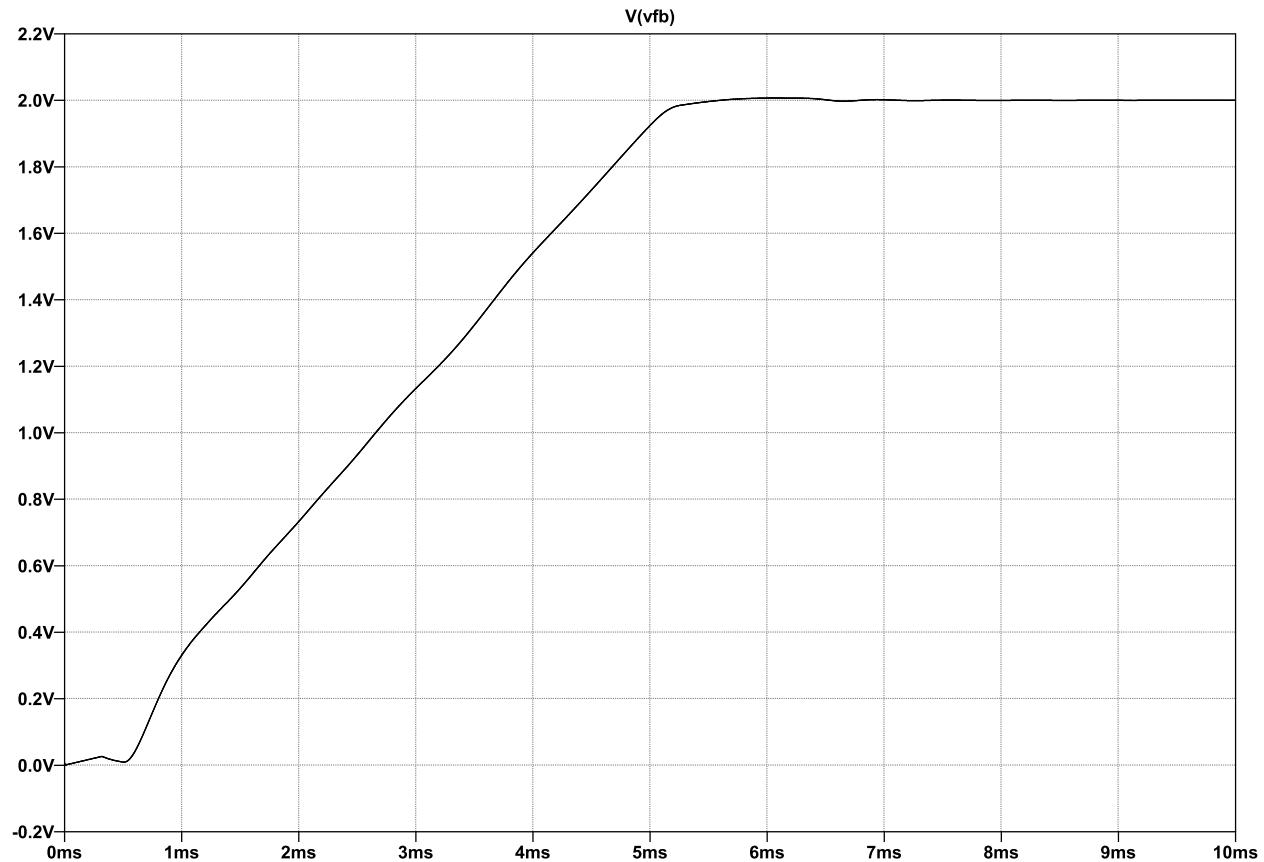


**Purpose:** To examine the scaled and clamped version of Vcontrol that directly drives the Ton parameter for phase shift control.

### **Key observations:**

- Vctrl\_limited accurately reflects the Vcontrol profile, showing clamping at the designed maximum.
- Smooth and repeatable waveform indicates predictable gate drive timing.
- No noise or discontinuities in signal, verifying that limiters and multipliers are functioning correctly.
- Short burst down indicating current limiting from Vtrip\_soft, limiting voltage to (Ton)

### 7.3.3 Vfb Full Simulation

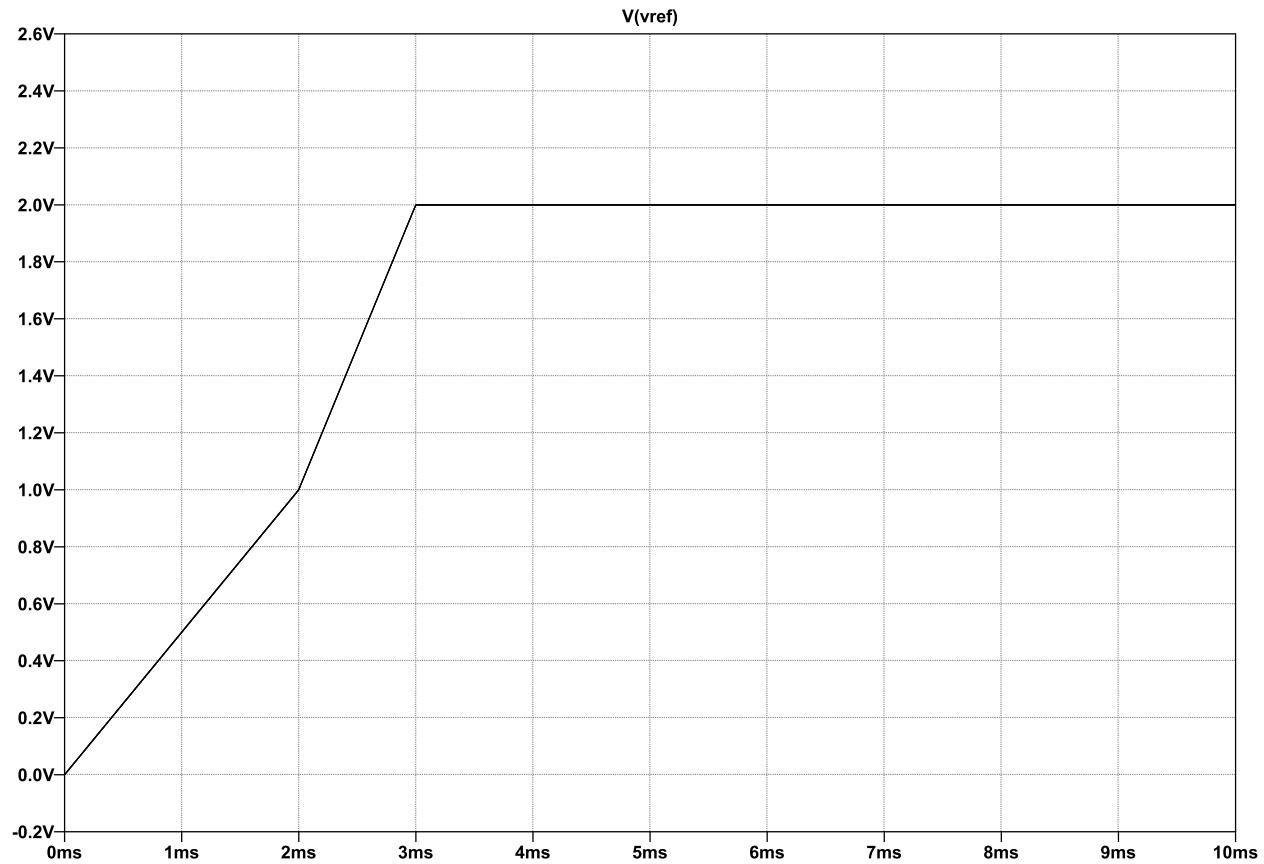


**Purpose:** To evaluate the feedback voltage derived from the output voltage divider and confirm tracking of the 2 V reference.

#### Key observations:

- $V_{fb}$  rises linearly during startup and stabilizes at exactly 2.0 V, confirming output voltage regulation.
- Minimal ripple once steady state is reached, indicating a clean feedback signal.
- Response closely follows  $V_{out}$  rise, validating voltage divider accuracy and signal integrity.

### 7.3.4 Vref Startup Ramp



**Purpose:** To validate the startup ramp behavior of the reference voltage ( $V_{ref}$ ), ensuring a smooth and controlled transition to full regulation.

#### Key observations:

- $V_{ref}$  rises linearly from 0 V to 1 V in 2 ms, then to 2 V in the following 1 ms.
- Ramp profile avoids abrupt jumps, ensuring a soft start with minimal current surge.
- Controlled reference ramp supports predictable loop startup behaviour, minimizing  $V_{out}$  overshoot and op-amp saturation.

## 8. Performance Metrics

The table below summarizes measured performance values at the nominal load condition of  $533.33\ \Omega$ . These results validate output voltage stability, ripple minimization, and peak system efficiency under steady-state operation.

Parameter	Value	Units	Notes
<b>Output Voltage (Vout)</b>	400.003	V	Measured at steady-state (9-10ms)
<b>Output Ripple (<math>\Delta V_{out}</math>)</b>	<0.07	Vpp	<0.02% of output voltage
<b>Output Power (Pout)</b>	300.006	W	Calculated as $V_{out} \times I_{load}$
<b>Input Voltage (Vin)</b>	100	V	Fixed DC input
<b>Input Current (Iin)</b>	3.048	A	Measured average at 100 V input
<b>Input Power (Pin)</b>	304.76	W	Measured from input terminal power
<b>Efficiency (<math>\eta</math>)</b>	98.441	%	Based on Pout/Pin
<b>Switching Frequency</b>	80	kHz	Phase-shifted PWM
<b>Output Load (Rload)</b>	533.33	$\Omega$	Steady-state test load
<b>Max Output Power</b>	338.2	W	At Rload = 474 $\Omega$ (tested upper limit before instability)
<b>Startup Rise Time</b>	~5.6	Ms	From 0 V to 400 V (controlled ramp with Vref)
<b>Gate Dead Time (Pri/Sec)</b>	300 / 155	Ns	Optimized for ZVS and synchronous rectification
<b>Max Simulated Temperature</b>	~178	°C	Simulation-only thermal limit — derating starts at 180 °C

## 9. Load Testing Results

To evaluate output stability and power delivery capability, the converter was tested across multiple load conditions. This simulated real-world transient and full-load behaviour while assessing voltage regulation, ripple suppression, and thermal scalability.

Rload ( $\Omega$ )	Expected Pout (W)	Pout (W)	Vout (V)	Ripple (V)	Efficiency ( $\eta$ )
<b>1600</b>	100	100.04	400.008	0.066	95.26
<b>800</b>	200	200.01	400.001	0.099	97.92
<b>533.33</b>	300	300.06	400.04	0.068	98.44
<b>400</b>	400	338.8	368.13	0.01	88.56

*All simulations are modelled and can be found in the /waveforms/Load\_Testing section of the GitHub.*

### 9.1 Observations

- The converter maintains **tight voltage regulation ( $\pm 40 \text{ mV}$ )** across the full operational range up to 300 W, with **ripple remaining below 0.1 V** in all cases.
- Efficiency increases with load up to 300 W, peaking at **98.44%**, and drops once the converter exceeds its sustainable output limit.
- At **400  $\Omega$  (attempted 400 W load)**, the converter saturates, resulting in a reduced output voltage and significantly lower efficiency. This behaviour confirms that the true maximum output power is  $\sim 338$  W under the current design and thermal constraints.
- Minimal ripple at all test points reflects **careful output filter tuning, gate timing optimization, and effective snubber implementation**.

# 10. Design Trade-offs & Future Work

The converter's maximum sustainable output power is limited to approximately **338.8 W**, which results from deliberate design trade-offs made to optimize steady-state performance, voltage stability, and conversion efficiency. This constraint stems from both **magnetic component tuning** and **control loop limitations**.

## 10.1 Power Delivery Limit

- The **primary limitation** is a performance plateau in conversion efficiency beyond ~338 W. The inductors (**L<sub>pri</sub>**, **L<sub>boost1/2</sub>**, and **L<sub>out</sub>**) were specifically tuned to:
  - Reduce Steady-state settling time
  - Support fast voltage rise with minimal overshoot
  - Maintain high efficiency at 300W
- Since the converter was **not designed to operate continuously at 400 W**, the transformer and magnetic components do **not support** that power level without redesign.

If scaling this system beyond 338 W, **transformer re-specification and magnetic re-tuning** would be essential.

## 10.2 Control System Bottleneck

- The op-amp output (**U<sub>1\_out</sub>**) is intentionally **clamped to 1.1 V**, which limits the maximum gate drive **on-time** (**T<sub>on</sub>**) and therefore the peak deliverable power.
- This limitation was introduced to:
  - Accelerate control system response
  - Prioritise **tight voltage regulation** over transient flexibility
  - Match the gain and stability characteristics of the **Type III compensation loop**

While this improves ripple and reduces overshoot, it does slightly constrain **control bandwidth**, particularly at full load. The balance achieved, however, represents an effective trade-off between **transient control and steady-state accuracy**.

## 10.3 Switching Node Disturbance

- **Midpoint ripple** between MOSFETs (**V<sub>m1</sub>/V<sub>m2</sub>**) was observed during **dead-time transitions**, attributed to energy kickback from the **magnetizing inductance (L<sub>pri</sub>)**.
- This was mitigated by:
  - Adding snubbers across the **high-side primary MOSFETs**
  - Inserting dedicated snubbers across **V<sub>m1</sub> and V<sub>m2</sub>**
  - Including **L<sub>boost1</sub> and L<sub>boost2</sub>** to absorb and dampen residual energy

These solutions minimized overshoot and EMI without compromising ZVS behaviour but actively reduce efficiency in the process.

## 10.4 Considerations for Future Enhancement

- **Lowering switching frequency** to ~50 kHz, as seen in several NASA PSFB systems, could yield higher efficiency by reducing switching losses — but would necessitate **larger magnetic and filtering components**.
- While **98.44% efficiency** exceeds the design goal, further improvements would likely require **fundamental changes** to transformer design, control architecture, or soft-switching timing.

The converter as implemented strikes a strong balance between **efficiency, control precision, thermal margin, and EMI suppression**, and any attempts to further optimize must carefully account for system-wide interactions.

# 11. Conclusion

This project successfully met the performance targets set for an aerospace-grade **Phase-Shifted Full-Bridge (PSFB) converter**, including:

- **Peak Efficiency:** 98.44%
- **Output Power:** 300 W sustained
- **Output Ripple:** <0.02%
- **EMI-conscious Design:** Snubber networks and ZVS timing
- **Controlled Startup:** Full voltage rise in <7 ms

All key electrical and control specifications were achieved with margin. However, it is important to note that **not all parasitics and system-level interactions were modelled**, due to both simulation speed limitations and the negligible impact of some higher-order effects in LTspice.

As with all simulation-based designs, **real-world testing may expose unmodeled behaviours** — particularly in areas such as:

- Thermal propagation and local hot spots
- Parasitic PCB inductance
- Magnetic component tolerancing
- Noise coupling and ground loop interference

Despite these caveats, the converter is now **fully prepared for physical implementation**, with a clear path forward.

## 11.1 Next Steps

1. **Design a PCB layout**, considering trace impedance, thermal dissipation, and magnetic coupling.
2. **Prototype and test the converter in hardware**, validating simulation results and identifying real-world limitations.
3. **Iterate the design** to resolve any physical or EMI-related issues uncovered during testing.
4. **Prepare documentation for verification and possible flight-readiness qualification.**

In its current form, this PSFB converter represents a **mature, high-efficiency, ZVS-capable design**, suitable for direct integration into the **Stage 2 power system of an ion thruster** and serves as a robust platform for further aerospace development.

## 12. Appendices

The following appendices provide detailed supporting material for the converter design. These include the complete system schematic, full bill of materials with estimated cost, the control logic expressions used in simulation, and key waveform captures. While these items are not discussed in detail within the main document, they are essential for full transparency, design verification, and real-world implementation.

Each sub-section offers raw technical insight, enabling replication, testing, and further development of the converter in both simulation and hardware environments.

### 12.1 Bill of Materials (BOM)

Item	Part Description	Part Number	Rating / Value	Qty	Est. Unit Price / Total (AUD)	Notes
1	MOSFETs	<i>Infineon IMZ120R030M1H</i>	120 V, 3 mΩ, 100 A	8	\$5.80 / \$46.40	CoolMOS™ C7 Gold; ZVS-optimized
2	Transformer	<i>Würth 750311473</i>	Custom 1:4.33 turns ratio	1	\$22.00	High-frequency ferrite core, 80 kHz-optimized
3	Output Filter Inductor (Lout)	<i>Coilcraft SER2918H-222KL</i>	2.2 mH, 2.8 A, <60 mΩ DCR	1	\$6.40	Main output choke
4	Input Capacitors	<i>Panasonic EEH-ZK1H101V</i>	100 µF, 50 V, <20 mΩ ESR	3	\$2.20 / \$6.60	Ceramic hybrid, low ESR
5	Output Capacitors	<i>Nichicon UHE2W102MHD6</i>	1000 µF, 450 V, 0.07 Ω ESR	4	\$4.80 / \$19.20	High-ripple aluminium electrolytic
6	Snubber Resistors	<i>Vishay CPF0207</i>	10 Ω, 1 W	2	\$0.60 / \$1.20	For primary-side snubbers
7	Snubber Capacitors	<i>Kemet C1206C104K5RACTU</i>	0.1 µF, 50 V, X7R	2	\$0.30 / \$0.60	Paired with snubber resistors
8	Gate Driver (Primary Side)	<i>TI UCC21520</i>	5 kV isol. dual channel	2	\$8.60 / \$17.20	Dead-time configurable, fast switching

<b>9</b>	<b>Feedback Op-Amp</b>	<i>TLV9062</i>	RRIO, 10 MHz, 5 V	1	\$1.90	Used in Type III compensator
<b>10</b>	<b>Compensation Network (caps/resistors)</b>	<i>Generic SMD 0603</i>	Various	8	\$0.05 / \$0.40	R/C values tuned for stability & bandwidth
<b>11</b>	<b>Temperature Sensor</b>	<i>TMP235A2DBZR</i>	-40 to 125 °C, analog output	1	\$1.20	Simulated thermal derating input
<b>12</b>	<b>Current Sense Resistor (Rsense)</b>	<i>Vishay WSLP1206R0100FEA</i>	10 mΩ, 1 W	1	\$1.10	Used for Vtrip_soft/hard logic
<b>13</b>	<b>Control Logic (Simulated in LTspice)</b>	-	-	-	-	Would be implemented in CPLD/MCU in hardware

**Estimated Total BOM Cost: ≈ \$124.20 AUD**

Note: Prices are based on single-unit, hobbyist/low-volume orders (Digi key/Mouser, mid-2025). Costs can be significantly reduced at production volumes.

## 12.2 Control Logic Equations

All expressions shown are implemented as .param or BV logic in LTspice. This appendix serves as a complete reference to the core control logic governing the PSFB converter.

### 12.2.1 HighG Gate Final (safety wrapped)

Expression:  $V = \text{if}(V(Vtrip\_hard) < 0.5, V(HighG\_steady)*V(Venable)*V(Vovp)*V(N\_temp\_derate), 0)$

### 12.2.2 LowG Gate Final (safety wrapped)

Expression:  $V = \text{if}(V(Vtrip\_hard) < 0.5, V(LowG\_steady)*V(Venable)*V(Vovp)*V(N\_temp\_derate), 0)$

### 12.2.3 HighG\_steady (raw)

Expression:  $V = \text{if}(\text{mod}(\text{time}, 12.5u) > (V(Ton) + 2td), \text{if}(\text{mod}(\text{time}, 12.5u) < (V(Ton) + 2td + V(Ton)), 12, 0), 0)$

### 12.2.4 LowG\_steady (raw)

Expression:  $V = \text{if}(\text{mod}(\text{time}, 12.5u) > td, \text{if}(\text{mod}(\text{time}, 12.5u) < (V(Ton) + td), 12, 0), 0)$

### 12.2.5 Ton (gate on-time)

Expression:  $V = \text{min}(V(Vctrl\_limited)*5.9u, 5.9u)$

### 12.2.6 Vctrl\_limited

Expression:  $V = V(Vcontrol)*V(Vtrip\_soft)$

### 12.2.7 Vcontrol

Expression:  $V = V(U1\_out)$

### **12.2.8 Vtrip\_soft**

Expression:  $V = \text{if}(V(I_{sense}) > -1.8, 1, 1 + 0.15 * (V(I_{sense}) * 1.8))$

### **12.2.9 Vtrip\_hard**

Expression:  $V = \text{if}(V(I_{sense}) > -2, 0, 1)$

### **12.2.10 Isense**

Expression:  $V = I(R_{sense}) * 1$

### **12.2.11 Vovp**

Expression:  $V = \text{if}(V(V_{out}) > 410, 0, 1)$

### **12.2.12 Venable (UVL)**

Expression:  $V = \text{if}(V(V_{in}) > 10, 1, 0)$

### **12.2.13 td (M1-M4 Delay)**

Expression: param  $td=300n$

### **12.2.14 N\_temp\_sense**

Expression:  $V = 25 + 0.5 * (I(R_{load}) * V(V_{out}))$

### **12.2.15 N\_temp\_derate**

Expression:  $V = \text{if}(V(N\_temp\_sense) < 180, 1, \text{if}(V(N\_temp\_sense) < 190, 1 - (V(N\_temp\_sense) - 180) * 0.01333, \text{if}(V(N\_temp\_sense) < 200, 0.8 - (V(N\_temp\_sense) - 190) * 0.05, 0.3)))$

### **12.2.16 Vfb (BV)**

Expression:  $V = V(V_{out\_sense}) - V(GND\_sense)$

### **12.2.17 M5\_Gate**

Expression:  $V = V(Lsec\_top) + V(SR\_top)$

### **12.2.18 M7\_Gate**

Expression:  $V = V(Lsec\_bot) + V(SR\_bot)$

### **12.2.19 SR\_top (M5, M8)**

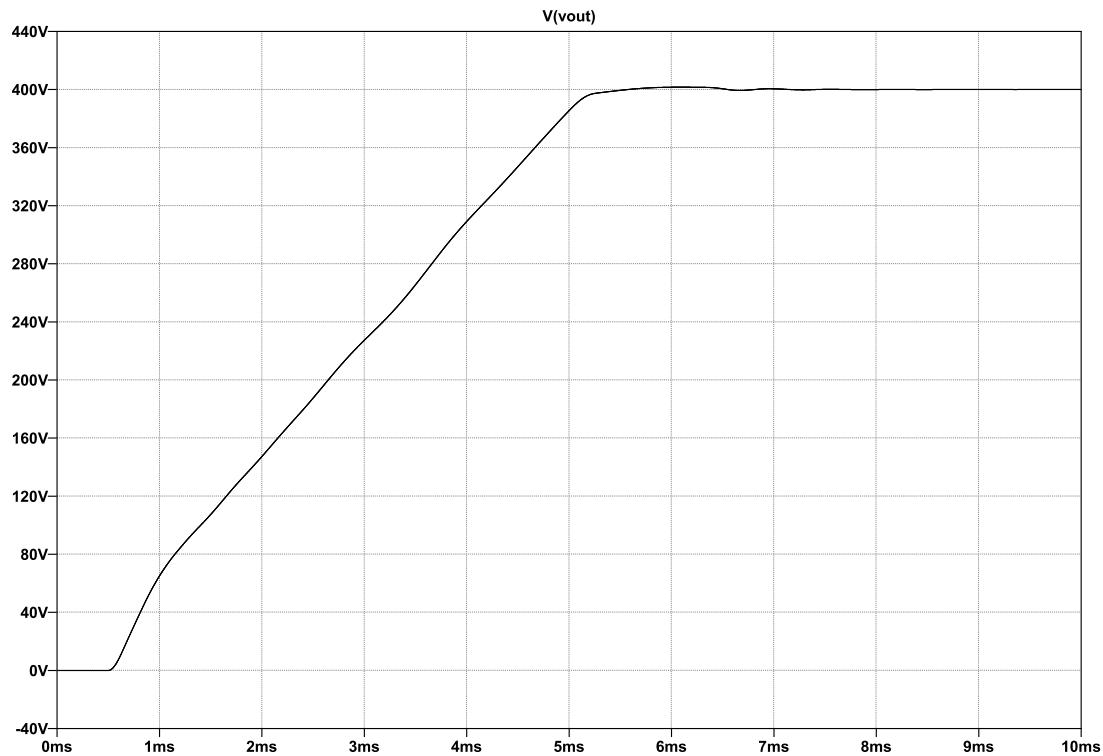
Expression:  $V = \text{if}(\text{delay}(V(HighG), 155n) > 6, 12, 0)$

### **12.2.20 SR\_bot (M6, M7)**

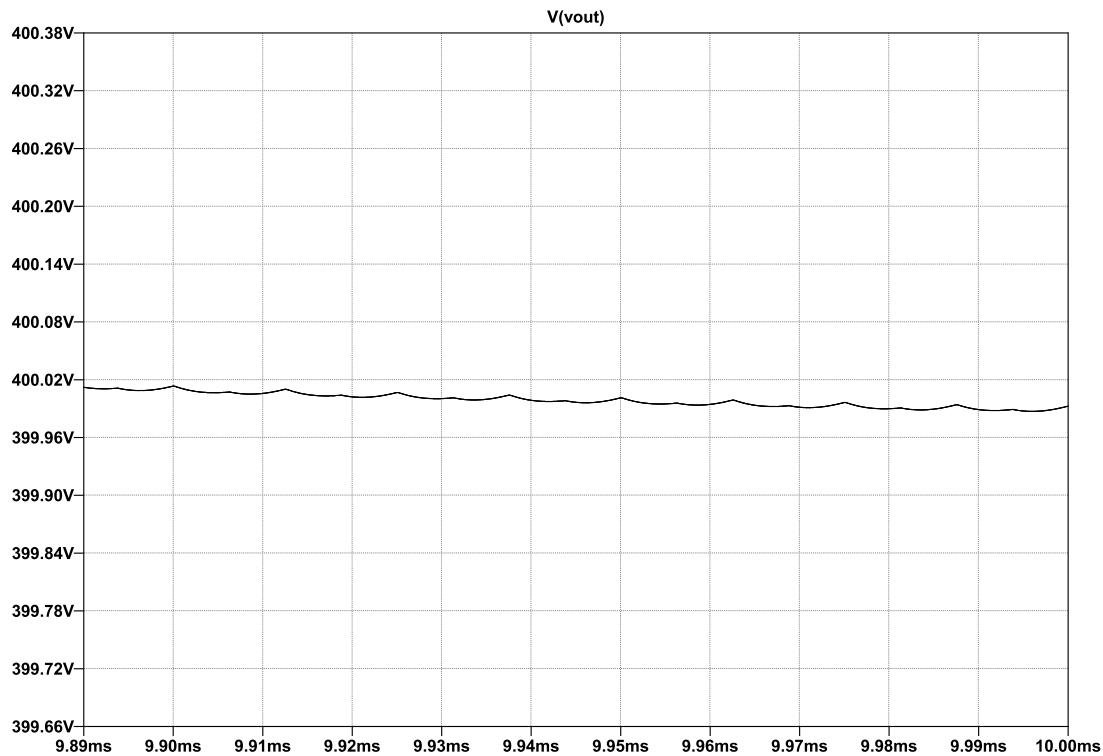
Expression:  $V = \text{if}(\text{delay}(V(LowG), 155n) > 6, 12, 0)$

## 12.3 Key Simulation Waveforms

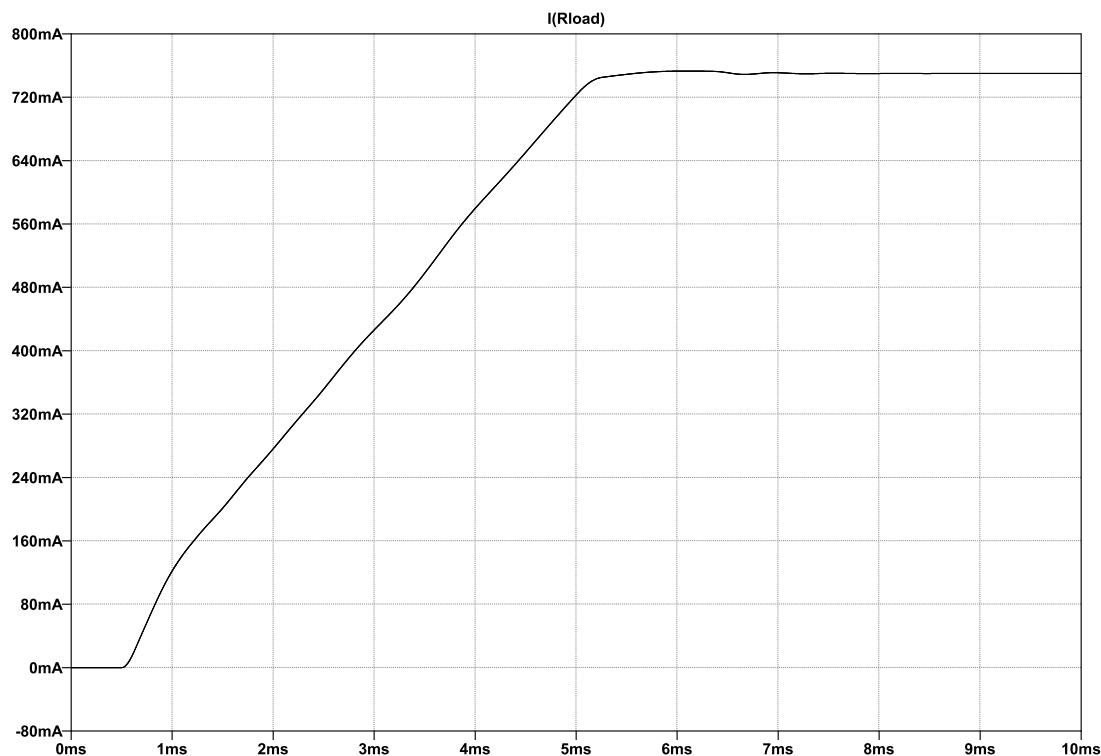
### 12.3.1 Vout (startup)



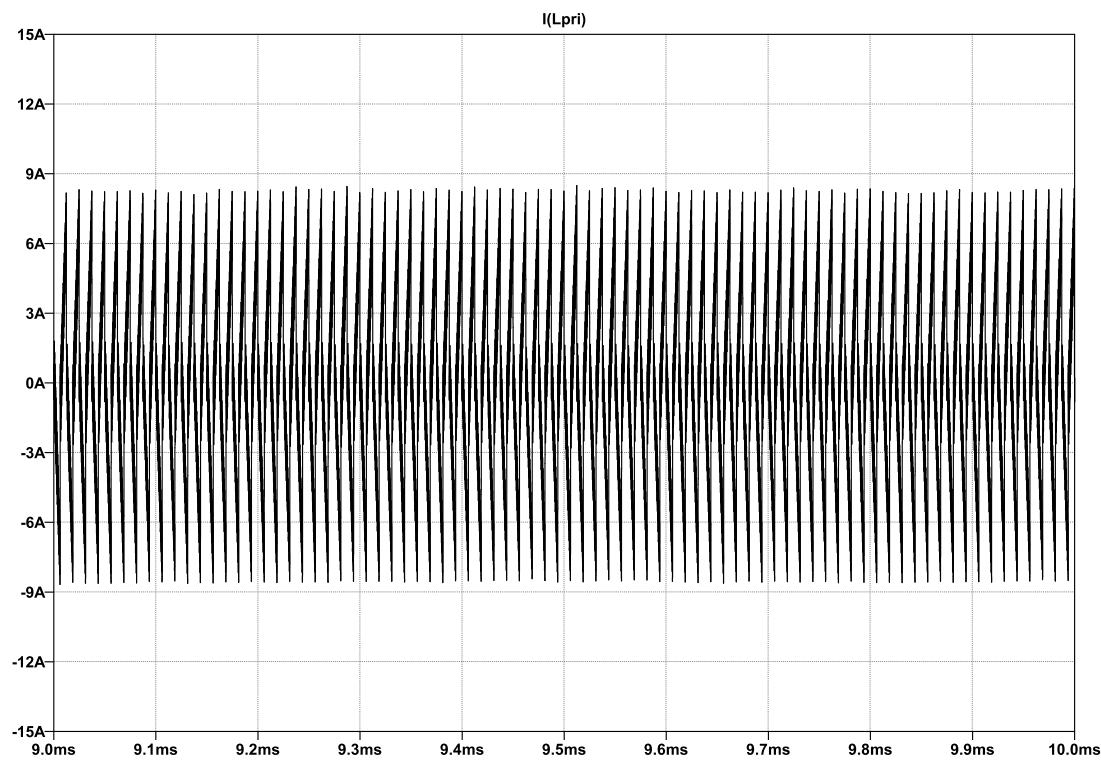
### 12.3.2 Vout steady state



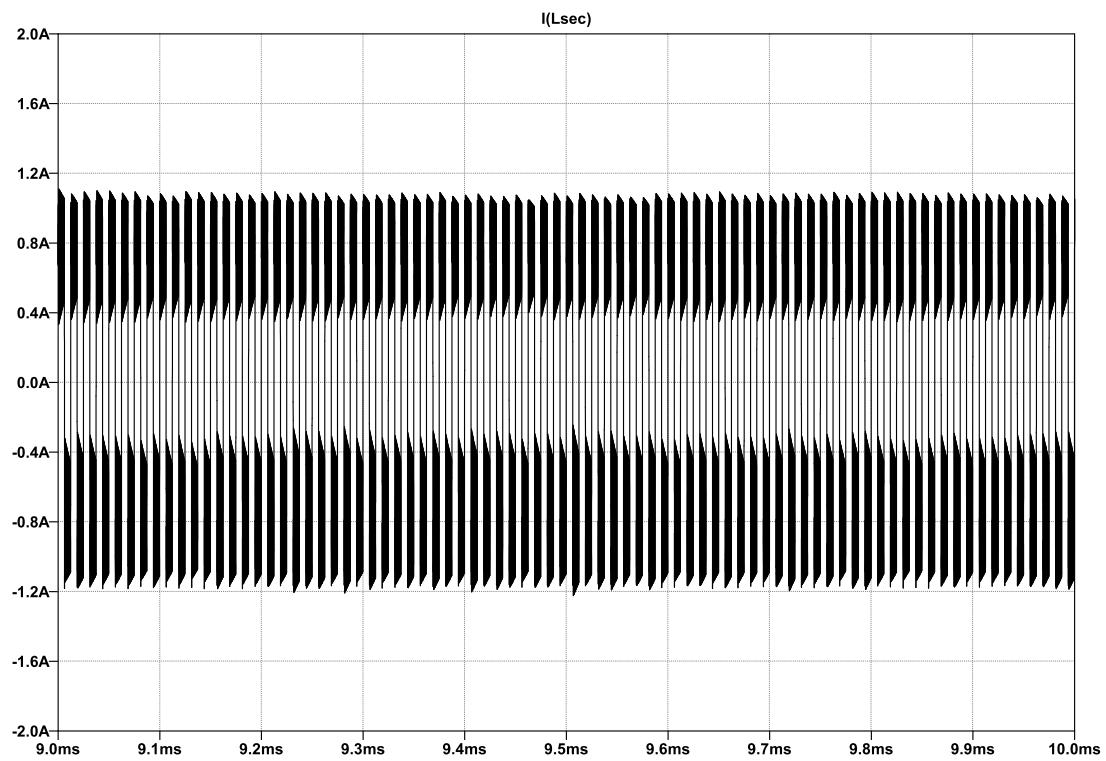
### 12.3.3 Rload



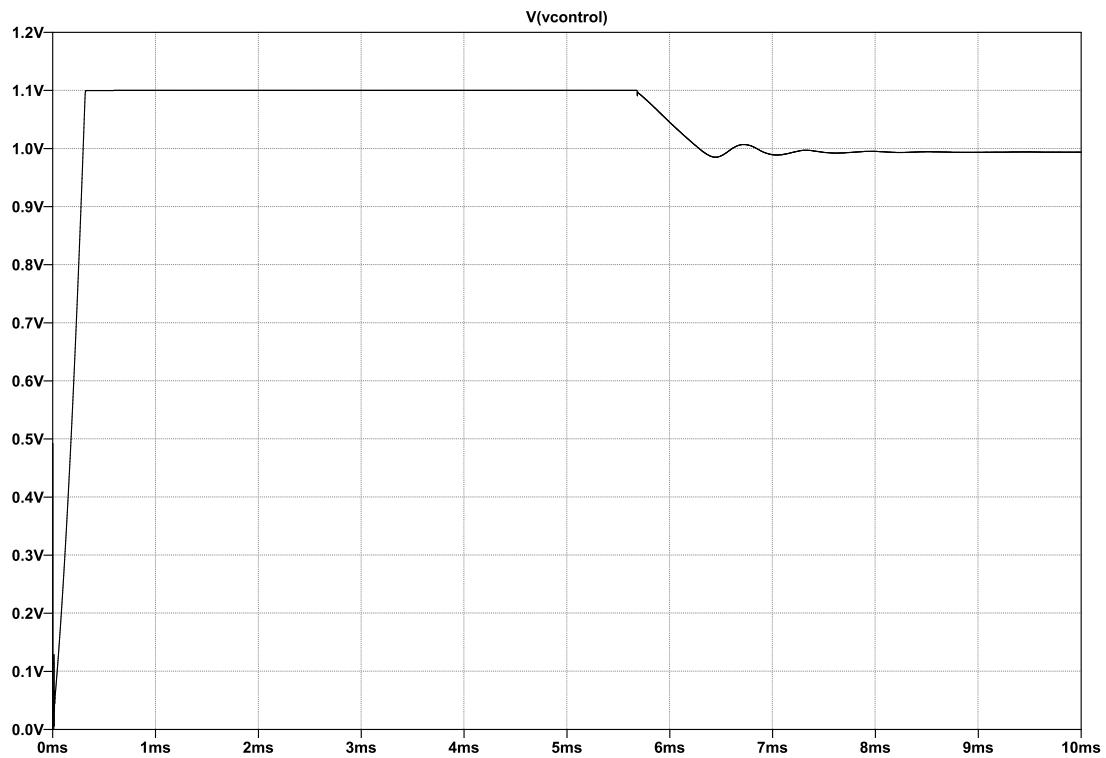
### 12.3.4 Transformer Current Lpri



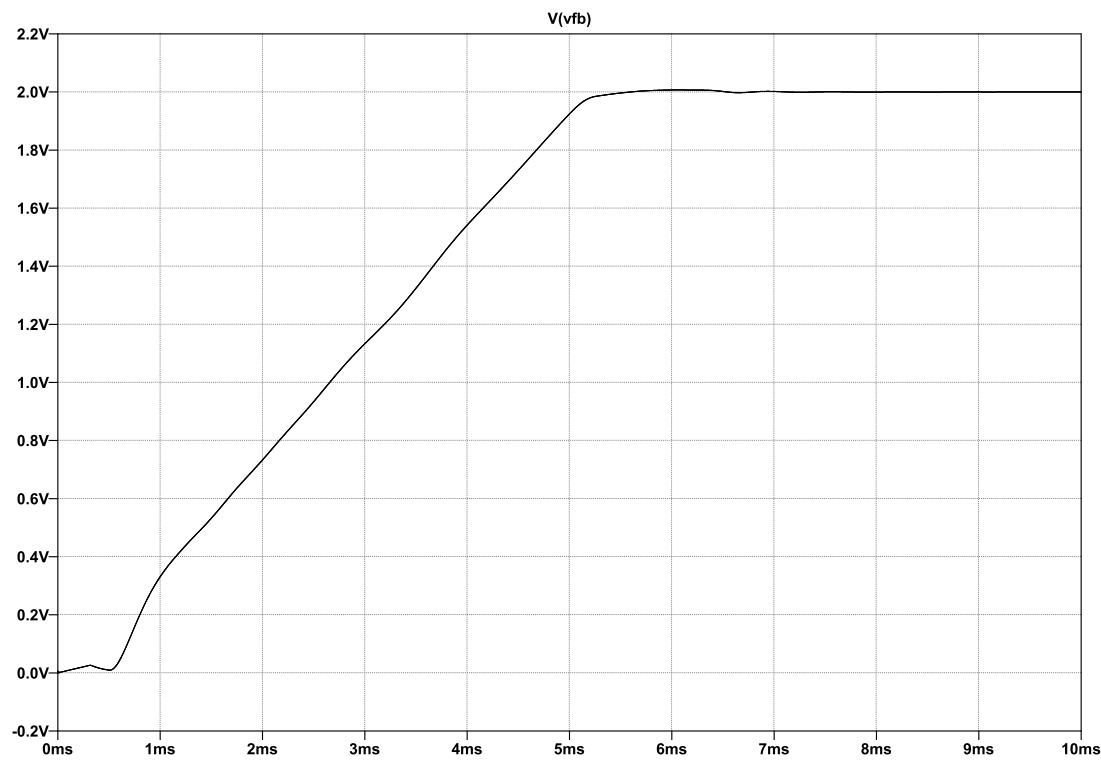
### 12.3.5 Transformer Current Lsec



### 12.3.6 Vcontrol



### 12.3.7 Vfb



### 12.3.8 Vref

