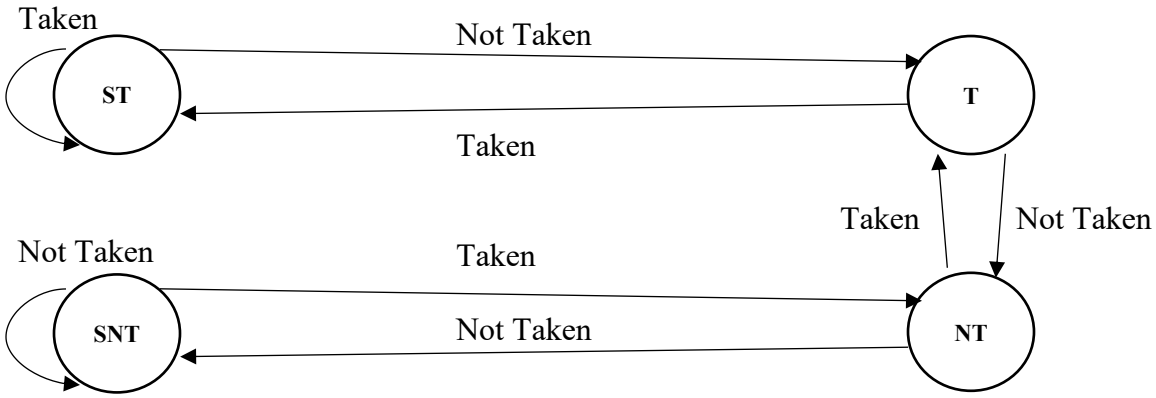
EE 395: Computer HW and Organization
Minnesota State University, Mankato
Project 2

In this project we will design, a simple branch prediction mechanism using 2 bit saturating counters:



State Output:

Current State	Input	Next State	Output
ST	Taken	T	Taken
ST	Not Taken	ST	Taken
T	Taken	ST	Taken
T	Not Taken	NT	Taken
NT	Taken	T	Not Taken
NT	Not Taken	SNT	Not Taken
SNT	Taken	NT	Not Taken
SNT	Not Taken	SNT	Not Taken

Requirements:
1. Initial State is NT and output is Not Taken.
2. At each clock based on what the **Input,** the **Next State** and the **Output** will be displayed.
3. There is a synchronous reset connected with your clock. The reset will take the predictor to initial state.
4. In your testbench you should demonstrate the following things:
1. All possible state transitions. Demonstrate the right output at each state. (7)
2. At each state if you reset then, you should go back to initial state and your output should reflect the change. (3)