DS18B20
Programmable Resolution 1-Wire Digital Thermometer

DESCRIPTION

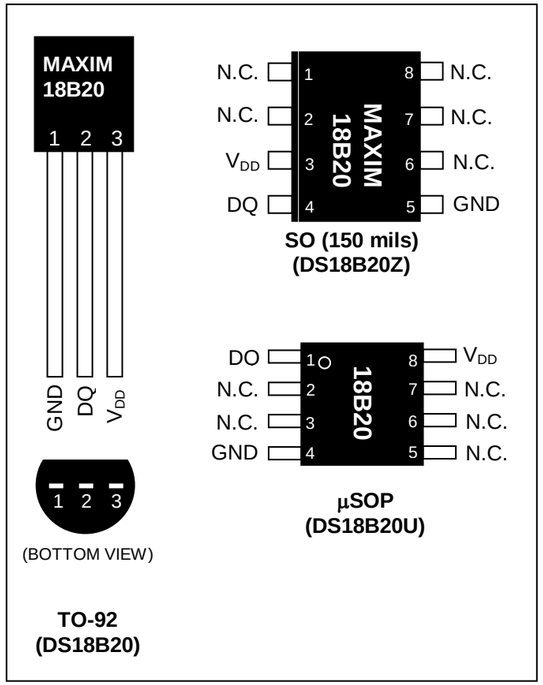
The DS18B20 digital thermometer provides 9-bit to 12-bit Celsius temperature measurements and has an alarm function with nonvolatile user-programmable upper and lower trigger points. The DS18B20 communicates over a 1-Wire bus that by definition requires only one data line (and ground) for communication with a central microprocessor. It has an operating temperature range of -55°C to +125°C and is accurate to ±0.5°C over the range of -10°C to +85°C. In addition, the DS18B20 can derive power directly from the data line ("parasite power"), eliminating the need for an external power supply.

Each DS18B20 has a unique 64-bit serial code, which allows multiple DS18B20s to function on the same 1-Wire bus. Thus, it is simple to use one microprocessor to control many DS18B20s distributed over a large area. Applications that can benefit from this feature include HVAC environmental controls, temperature monitoring systems inside buildings, equipment, or machinery, and process monitoring and control systems.

FEATURES

- Unique 1-Wire® Interface Requires Only One Port Pin for Communication
- Each Device has a Unique 64-Bit Serial Code Stored in an On-Board ROM
- Multidrop Capability Simplifies Distributed Temperature-Sensing Applications
- Requires No External Components
- Can Be Powered from Data Line; Power Supply Range is 3.0V to 5.5V
- Measures Temperatures from -55°C to +125°C (-67°F to +257°F)
- ±0.5°C Accuracy from -10°C to +85°C
- Thermometer Resolution is User Selectable from 9 to 12 Bits
- Converts Temperature to 12-Bit Digital Word in 750ms (Max)
- User-Definable Nonvolatile (NV) Alarm Settings
- Alarm Search Command Identifies and Addresses Devices Whose Temperature is Outside Programmed Limits (Temperature Alarm Condition)
- Available in 8-Pin SO (150 mils), 8-Pin µSOP, and 3-Pin TO-92 Packages
- Software Compatible with the DS1822
- Applications Include Thermostatic Controls, Industrial Systems, Consumer Products, Thermometers, or Any Thermally Sensitive System

PIN CONFIGURATIONS



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可编程分辨率 1线数字温度计

DS18B20数字温度计提供9位至12位摄氏温度测量，并具有非易失性用户可编程上下触发点的报警功能。DS18B20通过1-Wire总线进行通信，根据定义，该总线只需一条数据线(和地)即可与中央微处理器进行通信。它的工作温度范围为-55°c至+125°c，在-10°c至+85°c范围内精确到±0.5°c。此外，DS18B20可以直接从数据线获得电源（"寄生电源"），无需外部电源。

每个DS18B20都有一个独特的64位串行代码，允许多个Ds18b20在同一条1线总线上运行。因此，使用一个微处理器控制分布在大面积上的许多Ds18b20非常简单。可以从这一特性中受益的应用包括暖通空调环境控制、温度监测系统

设备，或机械，以及过程监控和控制系统。

FE

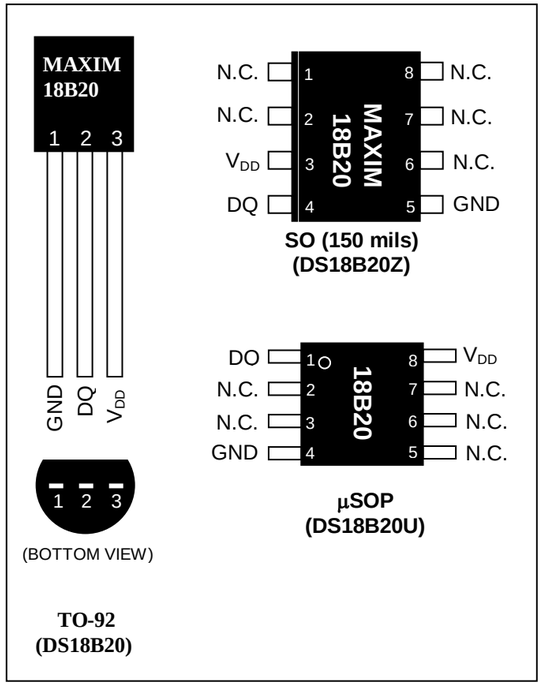
- 独特的1-Wire®接口只需要一个用于通信的端口引脚
- 每个器件都有一个唯一的64位串行代码存储在板载ROM中
- 多点功能简化了分布式

- 无需外部组件
- 可以从数据线供电;电源范围为3.0v至5.5v
- 测量-55°C至+125°C（-67°F至+257°F）的温度
- ±0.5°C精度-10°c至+85°C
- 温度计分辨率是用户可选择的从9到12位
- 在750ms（最大值）内将温度转换为12位数字字

- User-Definable Nonvolatile (NV) Alarm
- 报警搜索命令识别和解决温度超出编程限制（温度）的设备

- 提供8引脚SO(150密耳)、8引脚µsop和3引脚TO-92封装
- 软件兼容DS1822
- 应用范围包括恒温控制、工业系统、消费品温度计，或任何热敏感

引脚配置



1-Wire是MaximIntegratedProducts Inc.的注册商标。

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS18B20	-55°C to +125°C	3 TO-92	18B20
DS18B20+	-55°C to +125°C	3 TO-92	18B20
DS18B20/T&R	-55°C to +125°C	3 TO-92 (2000 Piece)	18B20
DS18B20+T&R	-55°C to +125°C	3 TO-92 (2000 Piece)	18B20
DS18B20-SL/T&R	-55°C to +125°C	3 TO-92 (2000 Piece)*	18B20
DS18B20-SL+T&R	-55°C to +125°C	3 TO-92 (2000 Piece)*	18B20
DS18B20U	-55°C to +125°C	8 µSOP	18B20
DS18B20U+	-55°C to +125°C	8 µSOP	18B20
DS18B20U/T&R	-55°C to +125°C	8 µSOP (3000 Piece)	18B20
DS18B20U+T&R	-55°C to +125°C	8 µSOP (3000 Piece)	18B20
DS18B20Z	-55°C to +125°C	8 SO	DS18B20
DS18B20Z+	-55°C to +125°C	8 SO	DS18B20
DS18B20Z/T&R	-55°C to +125°C	8 SO (2500 Piece)	DS18B20
DS18B20Z+T&R	-55°C to +125°C	8 SO (2500 Piece)	DS18B20

+Denotes a lead-free package. A "+" will appear on the top mark of lead-free packages.
T&R = Tape and reel.
**TO-92 packages in tape and reel can be ordered with straight or formed leads. Choose "SL" for straight leads. Bulk TO-92 orders are straight leads only.*

PIN DESCRIPTION

PIN			NAME	FUNCTION
SO	µSOP	TO-92		
1, 2, 6, 7, 8	2, 3, 5, 6, 7	—	N.C.	No Connection
3	8	3	V_{DD}	Optional V_{DD}. V_{DD} must be grounded for operation in parasite power mode.
4	1	2	DQ	Data Input/Output. Open-drain 1-Wire interface pin. Also provides power to the device when used in parasite power mode (see the *Powering the DS18B20* section.)
5	4	1	GND	Ground

OVERVIEW

Figure 1 shows a block diagram of the DS18B20, and pin descriptions are given in the *Pin Description* table. The 64-bit ROM stores the device's unique serial code. The scratchpad memory contains the 2-byte temperature register that stores the digital output from the temperature sensor. In addition, the scratchpad provides access to the 1-byte upper and lower alarm trigger registers (T_H and T_L) and the 1-byte configuration register. The configuration register allows the user to set the resolution of the temperature-to-digital conversion to 9, 10, 11, or 12 bits. The T_H, T_L, and configuration registers are nonvolatile (EEPROM), so they will retain data when the device is powered down.

The DS18B20 uses Maxim's exclusive 1-Wire bus protocol that implements bus communication using one control signal. The control line requires a weak pullup resistor since all devices are linked to the bus via a 3-state or open-drain port (the DQ pin in the case of the DS18B20). In this bus system, the microprocessor (the master device) identifies and addresses devices on the bus using each device's unique 64-bit code. Because each device has a unique code, the number of devices that can be addressed on one

订购资料

	温度范围	PIN-PACKAGE	最高分数
DS18B20	° °	3 TO-92	
DS18B20+	-55° °		
	°C to +125°C	3 TO-92 (2000 Piece)	18B20
DS18B20+T&R	-55°C to +125°C	3 TO-92 (2000 Piece)	18B20
DS18B20-SL/T&R	-55°C to +125°C	3 TO-92 (2000 Piece)*	18B20
DS18B20-SL+T&R	-55°C to +125°C	3 TO-92 (2000 Piece)*	18B20
DS18B20U	-55°C to +125°C	8 µSOP	18B20
DS18B20U+	-55°C to +125°C	8 µSOP	18B20
DS18B20U/T&R	-55°C to +125°C	8 µSOP (3000 Piece)	18B20
DS18B20U+T&R	-55°C to +125°C	8 µSOP (3000 Piece)	18B20
DS18B20Z	-55°C to +125°C	8 SO	DS18B20
DS18B20Z+	-55°C to +125°C	8 SO	DS18B20
DS18B20Z/T&R	-55°C to +125°C	8 SO (2500 Piece)	DS18B20
DS18B20Z+T&R	-55°C to +125°C	8 SO (2500 Piece)	DS18B20

+表示无铅封装。一个"+"将出现在无铅封装的顶部标记。T&R=卷带。*TO-92磁带和卷筒包装可以用直的或成形的引线订购。选择"SL"直接线索。批量到-92订单只是直接的线索.

引脚描述

PIN			NAME	FUNCTION
SO	µSOP	TO-92		
1, 2, 6, 7, 8	2, 3, 5, 6, 7	—	N.C.	没有联系
3	8	3	V_{DD}	可选VDD.VDD必须接地才能在寄生电源模式下运行。
4	1	2	DQ	数据输入输出。漏极开路1-Wire接口引脚。在寄生电源模式下也为器件供电(参见Ds18b20供电部分)。)
5	4	1	GND	Ground

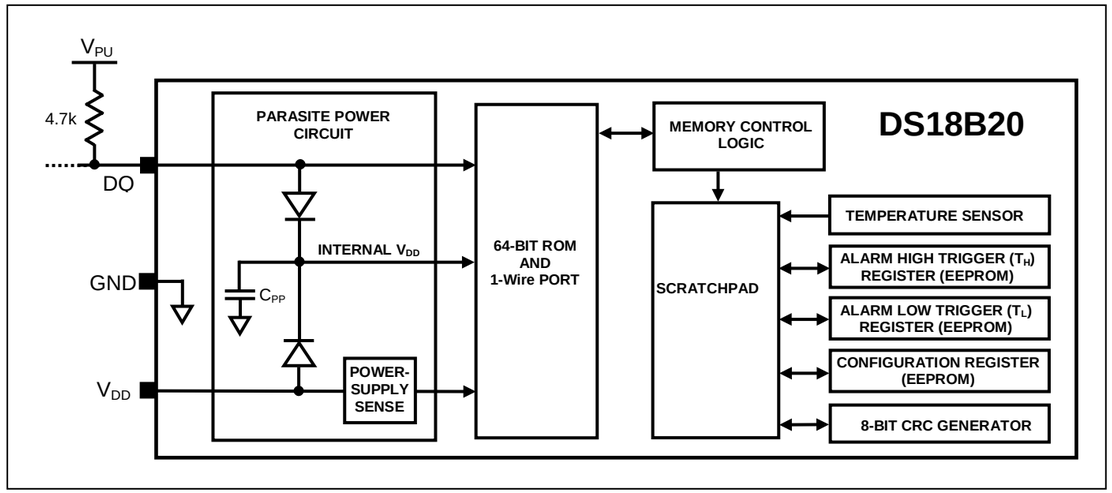
图1显示了DS18B20的框图，引脚描述在引脚描述表中给出。64位ROM存储器件的唯一串行代码。暂存器包含2字节温度寄存器，用于存储温度传感器的数字输出。此外，暂存器还提供对1字节上、下报警触发寄存器(TH和TL)和1字节配置寄存器的访问。配置寄存器允许用户将温度数字转换的分辨率设置为9、10、11或12位。TH、TL和配置寄存器是非易失的(EEPROM)，因此在器件断电时它们将保留数据。

DS18B20采用Maxim独有的1-Wire总线协议，通过一个控制信号实现总线通信。控制线需要一个弱上拉电阻，因为所有器件都通过三态或漏极开路端口(DS18B20的DQ引脚)连接到总线。在该总线系统中，微处理器（主设备）使用每个设备的唯一64位代码识别和寻址总线上的设备。因为每个设备都有一个唯一的代码，所以可以在一个设备上寻址的设备数量

bus is virtually unlimited. The 1-Wire bus protocol, including detailed explanations of the commands and “time slots,” is covered in the *1-Wire Bus System* section.

Another feature of the DS18B20 is the ability to operate without an external power supply. Power is instead supplied through the 1-Wire pullup resistor via the DQ pin when the bus is high. The high bus signal also charges an internal capacitor (C_{PP}), which then supplies power to the device when the bus is low. This method of deriving power from the 1-Wire bus is referred to as “parasite power.” As an alternative, the DS18B20 may also be powered by an external supply on V_{DD}.

Figure 1. DS18B20 Block Diagram



OPERATION—MEASURING TEMPERATURE

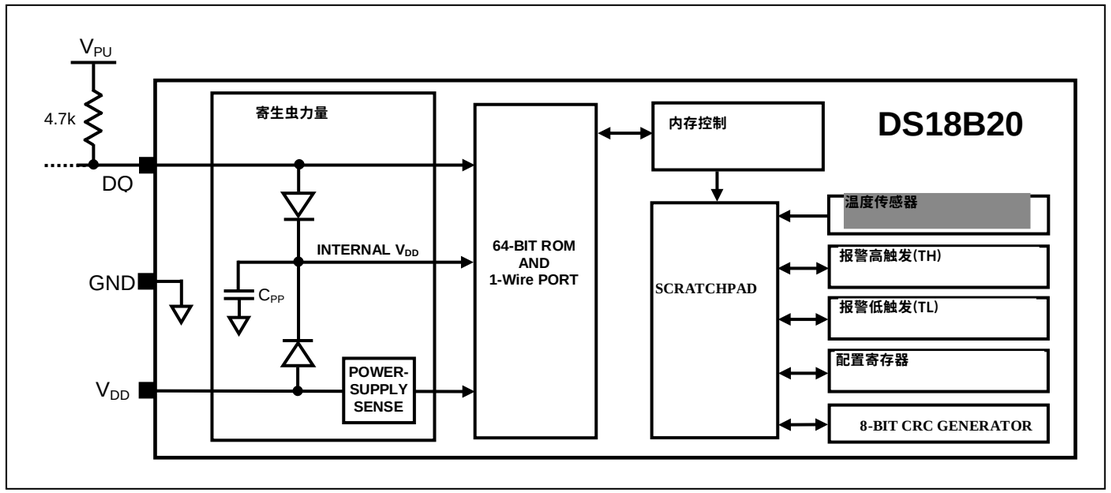
The core functionality of the DS18B20 is its direct-to-digital temperature sensor. The resolution of the temperature sensor is user-configurable to 9, 10, 11, or 12 bits, corresponding to increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively. The default resolution at power-up is 12-bit. The DS18B20 powers up in a low-power idle state. To initiate a temperature measurement and A-to-D conversion, the master must issue a Convert T [44h] command. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the DS18B20 returns to its idle state. If the DS18B20 is powered by an external supply, the master can issue “read time slots” (see the *1-Wire Bus System* section) after the Convert T command and the DS18B20 will respond by transmitting 0 while the temperature conversion is in progress and 1 when the conversion is done. If the DS18B20 is powered with parasite power, this notification technique cannot be used since the bus must be pulled high by a strong pullup during the entire temperature conversion. The bus requirements for parasite power are explained in detail in the *Powering the DS18B20* section.

The DS18B20 output temperature data is calibrated in degrees Celsius; for Fahrenheit applications, a lookup table or conversion routine must be used. The temperature data is stored as a 16-bit sign-extended two’s complement number in the temperature register (see Figure 2). The sign bits (S) indicate if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. If the DS18B20 is configured for 12-bit resolution, all bits in the temperature register will contain valid data. For 11-bit resolution, bit 0 is undefined. For 10-bit resolution, bits 1 and 0 are undefined, and for 9-bit resolution bits 2, 1, and 0 are undefined. Table 1 gives examples of digital output data and the corresponding temperature reading for 12-bit resolution conversions.

公共汽车实际上是无限的.1-Wire总线协议，包括命令和"时隙"的详细解释，在1-Wire总线系统部分介绍。

DS18B20的另一个特点是无需外部电源即可工作。当总线为高电平时，通过DQ引脚通过1-Wire上拉电阻供电。高总线信号还为内部电容(CPP)充电，然后在总线为低电平时为器件供电。这种从1-Wire总线获取电源的方法称为"寄生电源"。"作为替代方案，DS18B20也可以由VDD上的外部电源供电。

图1。DS18B20框图



DS18B20的核心功能是其直接数字温度传感器。温度传感器的分辨率可由用户配置为9、10、11或12位，分别对应0.5°C、0.25°C、0.125°C和0.0625°c的增量。上电时的默认分辨率为12位。DS18B20在低功耗空闲状态下上电。要启动温度测量和A到D转换，主机必须发出ConvertT[44h]命令。转换后，产生的热数据存储在暂存器的2字节温度寄存器中，DS18B20返回空闲状态。如果DS18B20由外部电源供电，主机可以在转换T命令后发出"读取时隙"（见1线总线系统部分），DS18B20将在温度转换进行时发送0，转换完成后发送1。如果DS18B20采用寄生电源供电，则不能使用这种通知技术，因为在整个温度转换过程中，总线必须通过强上拉拉高。寄生电源的总线要求在给DS18B20供电部分有详细说明。

DS18B20输出温度数据以摄氏度校准；对于华氏应用，必须使用查找表或转换例程。温度数据以16位符号扩展2的补码形式存储在温度寄存器中(见图2)。符号位表示温度是正数还是负数：正数S=0，负数S=1。如果DS18B20配置为12位分辨率，温度寄存器中的所有位都将包含有效数据。对于11位分辨率，位0未定义。对于10位分辨率，位1和0未定义，对于9位分辨率，位2、1和0未定义。表1给出了12位分辨率转换的数字输出数据和相应的温度读数示例。

Figure 2. Temperature Register Format

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LS BYTE	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MS BYTE	S	S	S	S	S	2^6	2^5	2^4

S = SIGN

Table 1. Temperature/Data Relationship

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEX)
+125	0000 0111 1101 0000	07D0h
+85*	0000 0101 0101 0000	0550h
+25.0625	0000 0001 1001 0001	0191h
+10.125	0000 0000 1010 0010	00A2h
+0.5	0000 0000 0000 1000	0008h
0	0000 0000 0000 0000	0000h
-0.5	1111 1111 1111 1000	FFF8h
-10.125	1111 1111 0101 1110	FF5Eh
-25.0625	1111 1110 0110 1111	FE6Fh
-55	1111 1100 1001 0000	FC90h

**The power-on reset value of the temperature register is +85°C.*

OPERATION—ALARM SIGNALING

After the DS18B20 performs a temperature conversion, the temperature value is compared to the user-defined two's complement alarm trigger values stored in the 1-byte T_H and T_L registers (see Figure 3). The sign bit (S) indicates if the value is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. The T_H and T_L registers are nonvolatile (EEPROM) so they will retain data when the device is powered down. T_H and T_L can be accessed through bytes 2 and 3 of the scratchpad as explained in the *Memory* section.

Figure 3. T_H and T_L Register Format

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Only bits 11 through 4 of the temperature register are used in the T_H and T_L comparison since T_H and T_L are 8-bit registers. If the measured temperature is lower than or equal to T_L or higher than or equal to T_H, an alarm condition exists and an alarm flag is set inside the DS18B20. This flag is updated after every temperature measurement; therefore, if the alarm condition goes away, the flag will be turned off after the next temperature conversion.

图2。温度寄存器格式

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LS BYTE	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MS BYTE	S	S	S	S	S	2^6	2^5	2^4

S = SIGN

表1。温度数据关系

TEMPERATURE (°C)	数字输出（二进制）	数字输出(十六进制)
+125	0000 0111 1101 0000	07D0h
+85*	0000 0101 0101 0000	0550h
+25.0625	0000 0001 1001 0001	0191h
+10.125	0000 0000 1010 0010	00A2h
+0.5	0000 0000 0000 1000	0008h
0	0000 0000 0000 0000	0000h
-0.5	1111 1111 1111 1000	FFF8h
-10.125	1111 1111 0101 1110	FF5Eh
-25.0625	1111 1110 0110 1111	FE6Fh
-55	1111 1100 1001 0000	FC90h

*温度寄存器的上电复位值为+85°C。

DS18B20执行温度转换后，将温度值与存储在1字节TH和TL寄存器中的用户定义的两个补码报警触发值进行比较(见图3)。符号位表示该值是正数还是负数：正数S=0，负数S=1。TH和TL寄存器是非易失性(EEPROM)，因此在器件断电时它们将保留数据。TH和TL可以通过暂存器的字节2和3访问，如存储器部分所述。

图3。TH和TL寄存器格式

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

由于TH和TL是8位寄存器，因此tH和TL比较仅使用温度寄存器的第11位至第4位。如果测量的温度低于或等于TL或高于或等于TH，则存在报警条件，并在DS18B20内部设置报警标志。该标志在每次温度测量后更新;因此，如果警报条件消失，该标志将在下一次温度转换后关闭。

The master device can check the alarm flag status of all DS18B20s on the bus by issuing an Alarm Search [ECh] command. Any DS18B20s with a set alarm flag will respond to the command, so the master can determine exactly which DS18B20s have experienced an alarm condition. If an alarm condition exists and the T_H or T_L settings have changed, another temperature conversion should be done to validate the alarm condition.

POWERING THE DS18B20

The DS18B20 can be powered by an external supply on the V_{DD} pin, or it can operate in “parasite power” mode, which allows the DS18B20 to function without a local external supply. Parasite power is very useful for applications that require remote temperature sensing or that are very space constrained. Figure 1 shows the DS18B20’s parasite-power control circuitry, which “steals” power from the 1-Wire bus via the DQ pin when the bus is high. The stolen charge powers the DS18B20 while the bus is high, and some of the charge is stored on the parasite power capacitor (C_{PP}) to provide power when the bus is low. When the DS18B20 is used in parasite power mode, the V_{DD} pin must be connected to ground.

In parasite power mode, the 1-Wire bus and C_{PP} can provide sufficient current to the DS18B20 for most operations as long as the specified timing and voltage requirements are met (see the *DC Electrical Characteristics* and *AC Electrical Characteristics*). However, when the DS18B20 is performing temperature conversions or copying data from the scratchpad memory to EEPROM, the operating current can be as high as 1.5mA. This current can cause an unacceptable voltage drop across the weak 1-Wire pullup resistor and is more current than can be supplied by C_{PP}. To assure that the DS18B20 has sufficient supply current, it is necessary to provide a strong pullup on the 1-Wire bus whenever temperature conversions are taking place or data is being copied from the scratchpad to EEPROM. This can be accomplished by using a MOSFET to pull the bus directly to the rail as shown in Figure 4. The 1-Wire bus must be switched to the strong pullup within 10µs (max) after a Convert T [44h] or Copy Scratchpad [48h] command is issued, and the bus must be held high by the pullup for the duration of the conversion (t_{CONV}) or data transfer (t_{WR} = 10ms). No other activity can take place on the 1-Wire bus while the pullup is enabled.

The DS18B20 can also be powered by the conventional method of connecting an external power supply to the V_{DD} pin, as shown in Figure 5. The advantage of this method is that the MOSFET pullup is not required, and the 1-Wire bus is free to carry other traffic during the temperature conversion time.

The use of parasite power is not recommended for temperatures above +100°C since the DS18B20 may not be able to sustain communications due to the higher leakage currents that can exist at these temperatures. For applications in which such temperatures are likely, it is strongly recommended that the DS18B20 be powered by an external power supply.

In some situations the bus master may not know whether the DS18B20s on the bus are parasite powered or powered by external supplies. The master needs this information to determine if the strong bus pullup should be used during temperature conversions. To get this information, the master can issue a Skip ROM [CCh] command followed by a Read Power Supply [B4h] command followed by a “read time slot”. During the read time slot, parasite powered DS18B20s will pull the bus low, and externally powered DS18B20s will let the bus remain high. If the bus is pulled low, the master knows that it must supply the strong pullup on the 1-Wire bus during temperature conversions.

主设备可以通过发出告警搜索[ECh]命令来检查总线上所有Ds18b20的告警标志状态。任何具有设置报警标志的Ds18b20都将响应该命令，因此主机可以准确确定哪些Ds18b20发生了报警情况。如果存在报警条件，并且TH或TL设置已更改，则应进行另一个温度转换以验证报警条件。

为DS18B20供电

DS18B20可以由VDD引脚上的外部电源供电，也可以工作在"寄生电源"模式，这样DS18B20就可以在没有本地外部电源的情况下运行。寄生功率对于需要遥感温度或空间受限的应用非常有用。图1显示了DS18B20的寄生电源控制电路，当总线为高电平时，它通过DQ引脚从1-Wire总线"窃取"电源。被盗电荷在总线为高电平时为DS18B20供电，部分电荷存储在寄生功率电容器(CPP)上，以便在总线为低电平时提供电源。当DS18B20用于寄生电源模式时，VDD引脚必须连接到地。

在寄生电源模式下，只要满足规定的时序和电压要求，1-Wire总线和CPP就能为DS18B20提供足够的电流，用于大多数操作(参见DC电气特性和AC电气特性)。然而，当DS18B20执行温度转换或将数据从暂存器复制到EEPROM时，工作电流可能高达1.5ma。该电流会在弱1-Wire上拉电阻上造成不可接受的压降，并且比CPP提供的电流更大。为了确保DS18B20有足够的电源电流，当温度转换发生或数据从暂存器复制到EEPROM时，必须在1-Wire总线上提供一个强上拉。这可以通过使用MOSFET将总线直接拉到轨上来实现，如图4所示。在发出转换T[44h]或复制暂存器[48h]命令后，1-Wire总线必须在10µs(max)内切换到强上拉，并且在转换(TCONV)或数据传输(tWR=10ms)期间，总线必须由上拉保持高上拉使能时1-Wire总线上不能进行任何其他活动。

DS18B20也可以通过将外部电源连接到VDD引脚的传统方法供电，如图5所示。这种方法的优点是不需要MOSFET上拉，并且在温度转换时间内，1-Wire总线可以自由承载其他流量。

在+100°C以上的温度下，不建议使用寄生电源，因为在这些温度下可能存在较高的漏电流，DS18B20可能无法维持通信。对于可能出现这种温度的应用，强烈建议DS18B20由外部电源供电。

在某些情况下，总线主机可能不知道总线上的Ds18b20是寄生供电还是由外部电源供电。主机需要这些信息来确定在温度转换期间是否应使用强总线上拉。为了获得这些信息，主机可以发出一个跳过ROM[CCh]命令，然后是一个读电源[B4h]命令，然后是一个"读时隙"。在读取时隙期间，寄生供电的DS18B20s将把总线拉低，外部供电的DS18B20s将让总线保持高电平。如果总线被拉低，主机知道它必须在温度转换期间在1-Wire总线上提供强拉。

Figure 4. Supplying the Parasite-Powered DS18B20 During Temperature Conversions

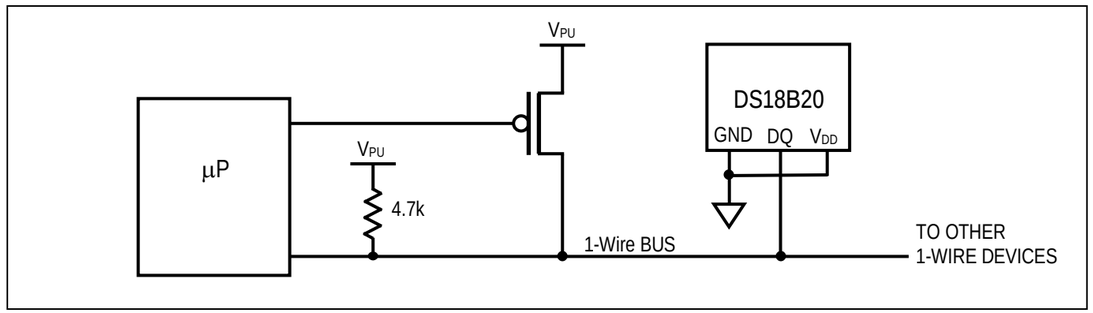
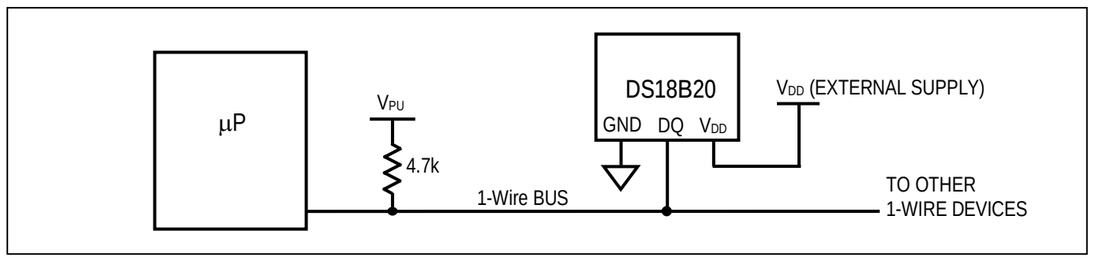


Figure 5. Powering the DS18B20 with an External Supply



64-BIT LASERED ROM CODE

Each DS18B20 contains a unique 64–bit code (see Figure 6) stored in ROM. The least significant 8 bits of the ROM code contain the DS18B20's 1-Wire family code: 28h. The next 48 bits contain a unique serial number. The most significant 8 bits contain a cyclic redundancy check (CRC) byte that is calculated from the first 56 bits of the ROM code. A detailed explanation of the CRC bits is provided in the *CRC Generation* section. The 64-bit ROM code and associated ROM function control logic allow the DS18B20 to operate as a 1-Wire device using the protocol detailed in the *1-Wire Bus System* section.

Figure 6. 64-Bit Lasered ROM Code

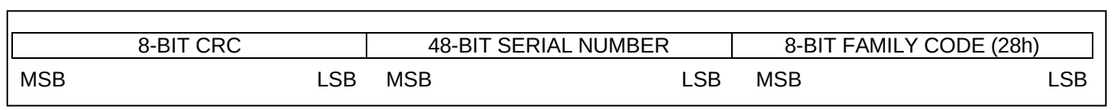


图4。在温度转换期间为寄生虫供电的DS18B20供电

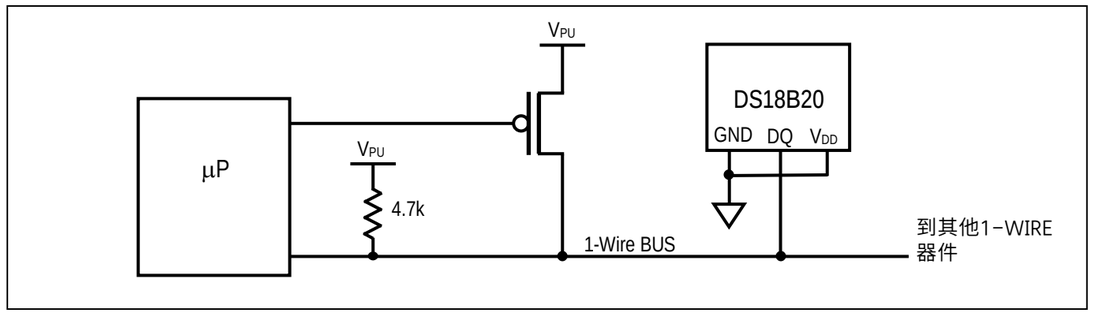
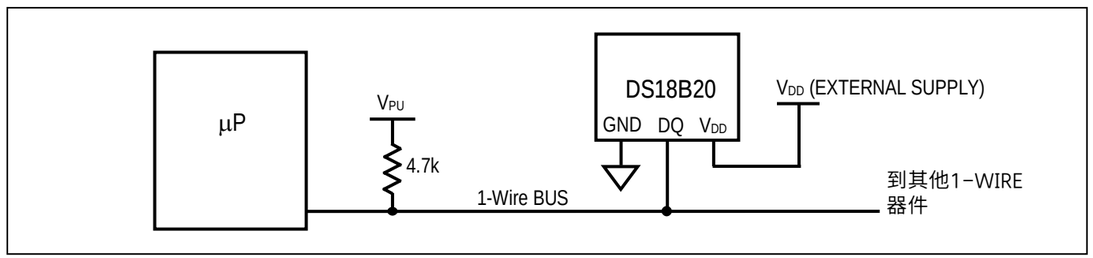
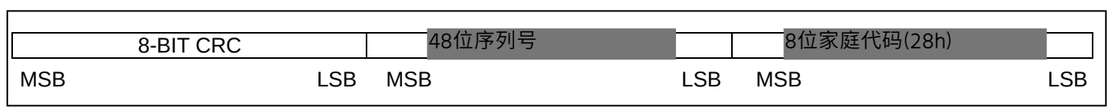


图5。用外部电源为DS18B20供电



64位LASEREDROM代码每个DS18B20包含一个存储在ROM中的唯一64位代码(见图6)。ROM代码的最低有效8位包含DS18B20的1-Wire系列代码：28H。接下来的48位包含一个唯一的序列号。最高有效的8位包含从ROM代码的前56位计算的循环冗余校验(CRC)字节。CRC位的详细解释在CRC生成部分中提供。64位ROM代码和相关的ROM功能控制逻辑允许DS18B20使用1-Wire总线系统部分中详述的协议作为1-Wire器件工作。

图6。64位激光ROM代码



MEMORY

The DS18B20's memory is organized as shown in Figure 7. The memory consists of an SRAM scratchpad with nonvolatile EEPROM storage for the high and low alarm trigger registers (T_H and T_L) and configuration register. Note that if the DS18B20 alarm function is not used, the T_H and T_L registers can serve as general-purpose memory. All memory commands are described in detail in the *DS18B20 Function Commands* section.

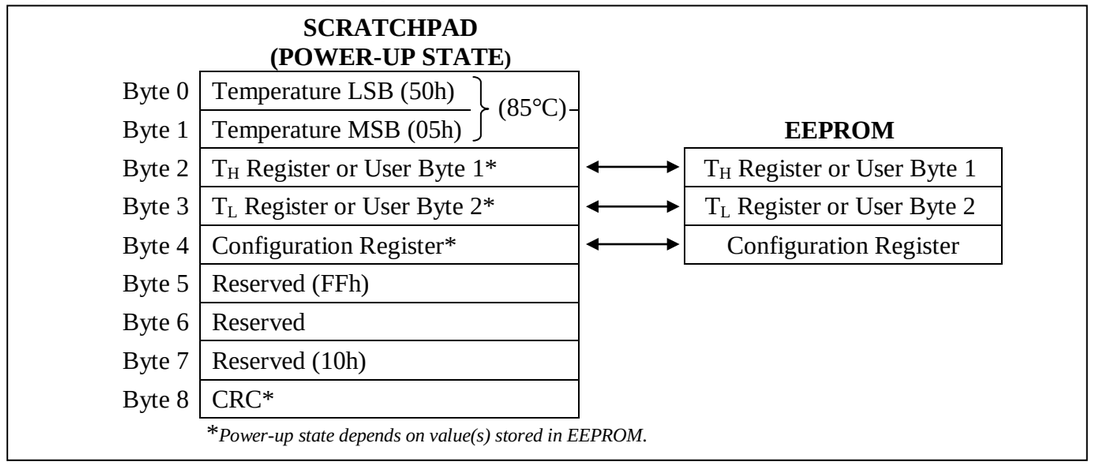
Byte 0 and byte 1 of the scratchpad contain the LSB and the MSB of the temperature register, respectively. These bytes are read-only. Bytes 2 and 3 provide access to T_H and T_L registers. Byte 4 contains the configuration register data, which is explained in detail in the *Configuration Register* section. Bytes 5, 6, and 7 are reserved for internal use by the device and cannot be overwritten.

Byte 8 of the scratchpad is read-only and contains the CRC code for bytes 0 through 7 of the scratchpad. The DS18B20 generates this CRC using the method described in the *CRC Generation* section.

Data is written to bytes 2, 3, and 4 of the scratchpad using the Write Scratchpad [4Eh] command; the data must be transmitted to the DS18B20 starting with the least significant bit of byte 2. To verify data integrity, the scratchpad can be read (using the Read Scratchpad [BEh] command) after the data is written. When reading the scratchpad, data is transferred over the 1-Wire bus starting with the least significant bit of byte 0. To transfer the T_H, T_L and configuration data from the scratchpad to EEPROM, the master must issue the Copy Scratchpad [48h] command.

Data in the EEPROM registers is retained when the device is powered down; at power-up the EEPROM data is reloaded into the corresponding scratchpad locations. Data can also be reloaded from EEPROM to the scratchpad at any time using the Recall E^2 [B8h] command. The master can issue read time slots following the Recall E^2 command and the DS18B20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done.

Figure 7. DS18B20 Memory Map



MEMORY

DS18B20的存储器结构如图7所示。该存储器由一个SRAM暂存器组成，具有用于高、低报警触发寄存器(TH和TL)和配置寄存器的非易失EEPROM存储。注意，如果不使用DS18B20报警功能，TH和TL寄存器可以作为通用存储器。DS18B20功能命令部分详细介绍了所有存储器命令。

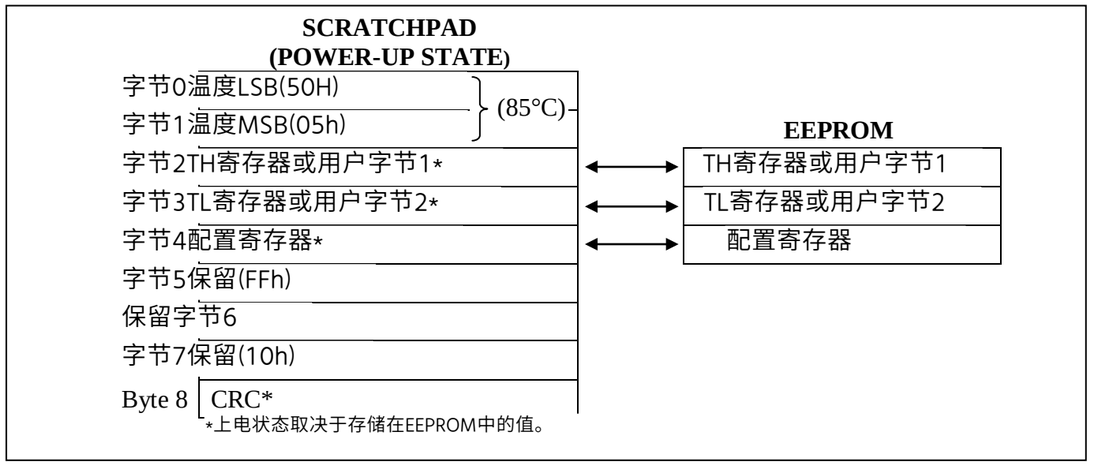
暂存器的字节0和字节1分别包含温度寄存器的LSB和MSB。这些字节是只读的。字节2和3提供对TH和TL寄存器的访问。字节4包含配置寄存器数据，在配置寄存器部分详细解释。字节5、6和7保留供设备内部使用，不能被复盖。

暂存器的字节8是只读的，包含暂存器的字节0到7的CRC码。
DS18B20使用CRC生成部分所述的方法生成该CRC。

使用WriteScratchpad[4eh]命令将数据写入暂存器的字节2、3和4；数据必须从字节2的最低有效位开始传输到DS18B20。为了验证数据的完整性，可以在数据写入后读取暂存器（使用读取暂存器[BEh]命令）。读取暂存器时，数据从字节0的最低有效位开始通过1-Wire总线传输。要将tH、TL和配置数据从暂存器传输到EEPROM，主机必须发出复制暂存器[48h]命令。

当器件断电时，EEPROM寄存器中的数据将被保留；上电时，EEPROM数据将被重新加载到相应的暂存器位置。还可以使用RecallE2[B8h]命令随时将数据从EEPROM重新加载到暂存器。主机可以在调用E2命令后发出读取时隙，DS18B20将在调用进行时发送0，在调用完成时发送1，以指示调用的状态。

图7。DS18B20内存映射



CONFIGURATION REGISTER

Byte 4 of the scratchpad memory contains the configuration register, which is organized as illustrated in Figure 8**.** The user can set the conversion resolution of the DS18B20 using the R0 and R1 bits in this register as shown in Table 2. The power-up default of these bits is R0 = 1 and R1 = 1 (12-bit resolution). Note that there is a direct tradeoff between resolution and conversion time. Bit 7 and bits 0 to 4 in the configuration register are reserved for internal use by the device and cannot be overwritten.

Figure 8. Configuration Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	R1	R0	1	1	1	1	1

Table 2. Thermometer Resolution Configuration

R1	R0	RESOLUTION (BITS)	MAX CONVERSION TIME	
0	0	9	93.75ms	(t_{CONV}/8)
0	1	10	187.5ms	(t_{CONV}/4)
1	0	11	375ms	(t_{CONV}/2)
1	1	12	750ms	(t_{CONV})

CRC GENERATION

CRC bytes are provided as part of the DS18B20's 64-bit ROM code and in the 9th byte of the scratchpad memory. The ROM code CRC is calculated from the first 56 bits of the ROM code and is contained in the most significant byte of the ROM. The scratchpad CRC is calculated from the data stored in the scratchpad, and therefore it changes when the data in the scratchpad changes. The CRCs provide the bus master with a method of data validation when data is read from the DS18B20. To verify that data has been read correctly, the bus master must re-calculate the CRC from the received data and then compare this value to either the ROM code CRC (for ROM reads) or to the scratchpad CRC (for scratchpad reads). If the calculated CRC matches the read CRC, the data has been received error free. The comparison of CRC values and the decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS18B20 that prevents a command sequence from proceeding if the DS18B20 CRC (ROM or scratchpad) does not match the value generated by the bus master.

The equivalent polynomial function of the CRC (ROM or scratchpad) is:

$$CRC = X^8 + X^5 + X^4 + 1$$

The bus master can re-calculate the CRC and compare it to the CRC values from the DS18B20 using the polynomial generator shown in Figure 9. This circuit consists of a shift register and XOR gates, and the shift register bits are initialized to 0. Starting with the least significant bit of the ROM code or the least significant bit of byte 0 in the scratchpad, one bit at a time should shifted into the shift register. After shifting in the 56th bit from the ROM or the most significant bit of byte 7 from the scratchpad, the polynomial generator will contain the re-calculated CRC. Next, the 8-bit ROM code or scratchpad CRC from the DS18B20 must be shifted into the circuit. At this point, if the re-calculated CRC was correct, the shift register will contain all 0s. Additional information about the Maxim 1-Wire cyclic redundancy check

配置寄存器

暂存器存储器的字节4包含配置寄存器，其组织如图8所示。用户可以使用该寄存器中的R0和R1位设置DS18B20的转换分辨率，如表2所示。这些位的上电默认值为R0=1和R1=1（12位分辨率）。请注意，分辨率和转换时间之间存在直接权衡。配置寄存器中的位7和位0至4保留给器件内部使用，不能被复盖。

图8。配置寄存器

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	R1	R0	1	1	1	1	1

表2。温度计分辨率配置

R1	R0	RESOLUTION (BITS)	最大转换	
0	0	9	93.75ms	(t_{CONV}/8)
0	1	10	187.5ms	(t_{CONV}/4)
1	0	11	375ms	(t_{CONV}/2)
1	1	12	750ms	(t_{CONV})

CRC字节作为DS18B2064位ROM代码的一部分，在暂存器存储器的第9个字节中提供。ROM码CRC是从ROM码的前56位计算出来的，包含在ROM的最高有效字节中。暂存器CRC是从存储在暂存器中的数据计算的，因此当暂存器中的数据改变时它改变。当从DS18B20读取数据时，CRCs为总线主机提供了一种数据验证方法。为了验证数据是否被正确读取，总线主机必须从接收到的数据重新计算CRC，然后将该值与ROM代码CRC（用于ROM读取）或暂存器CRC（用于暂存器读取）进行比较。如果计算的CRC与读取的CRC匹配，则数据已无差错地接收。CRC值的比较和继续操作的决定完全由总线主机决定。有没有电路内部的DS18B20，防止命令序列进行，如果

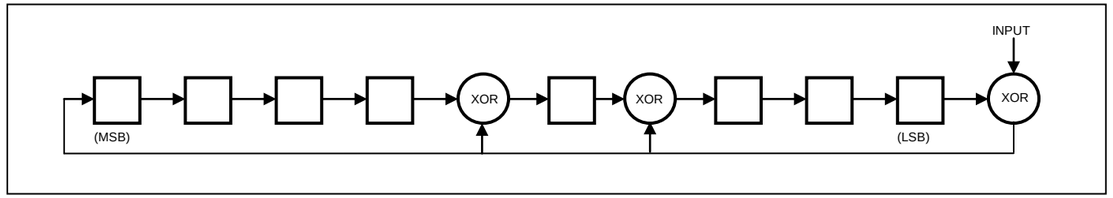
DS18B20CRC(ROM或暂存器)与总线主机生成的值不匹配。
CRC（ROM或暂存器）的等效多项式函数是:

$$CRC = X^8 + X^5 + X^4 + 1$$

总线主机可以重新计算CRC，并使用图9所示的多项式发生器将其与DS18B20的CRC值进行比较。该电路由移位寄存器和异或门组成，移位寄存器位初始化为0。从ROM代码的最低有效位或暂存器中字节0的最低有效位开始，每次一位应移入移位寄存器。在从ROM的第56位或从暂存器的字节7的最高有效位移位后，多项式发生器将包含重新计算的CRC。接下来，必须将来自DS18B20的8位ROM码或暂存器CRC移入电路。此时，如果重新计算的CRC正确，移位寄存器将包含所有0。

is available in *Application Note 27: Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products*.

Figure 9. CRC Generator



1-WIRE BUS SYSTEM

The 1-Wire bus system uses a single bus master to control one or more slave devices. The DS18B20 is always a slave. When there is only one slave on the bus, the system is referred to as a “single-drop” system; the system is “multidrop” if there are multiple slaves on the bus.

All data and commands are transmitted least significant bit first over the 1-Wire bus.

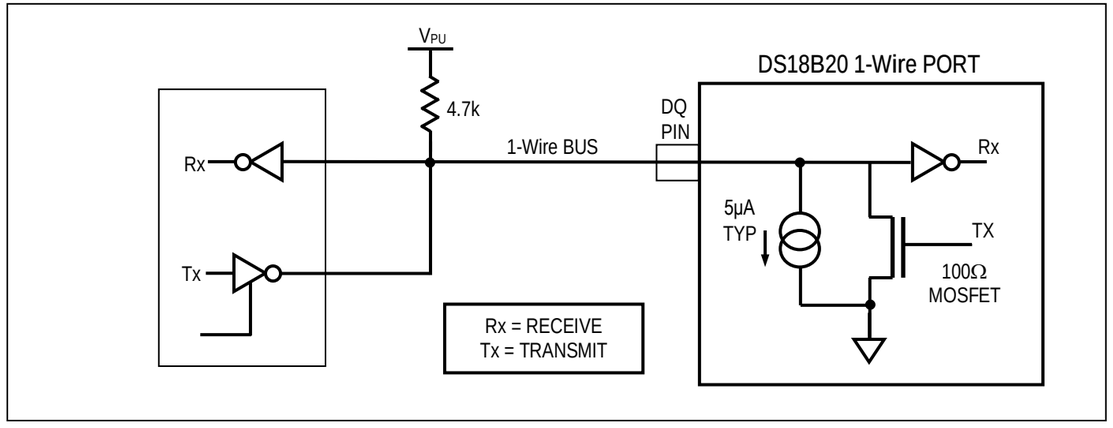
The following discussion of the 1-Wire bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1-Wire bus has by definition only a single data line. Each device (master or slave) interfaces to the data line via an open-drain or 3-state port. This allows each device to “release” the data line when the device is not transmitting data so the bus is available for use by another device. The 1-Wire port of the DS18B20 (the DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 10.

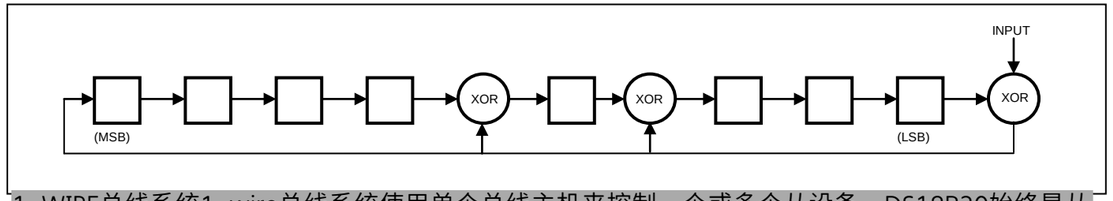
The 1-Wire bus requires an external pullup resistor of approximately 5kΩ; thus, the idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If the bus is held low for more than 480µs, all components on the bus will be reset.

Figure 10. Hardware Configuration



可在应用笔记27:理解和使用MaximiButton产品的循环冗余检查.

图9。CRC发生器



1-WIRE总线系统1-wire总线系统使用单个总线主机来控制一个或多个从设备。DS18B20始终是从机。当总线上只有一个从站时，系统被称为"单滴"系统；如果总线上有多个从站，则系统是"多滴"系统。

所有数据和命令首先通过1-Wire总线传输最低有效位。

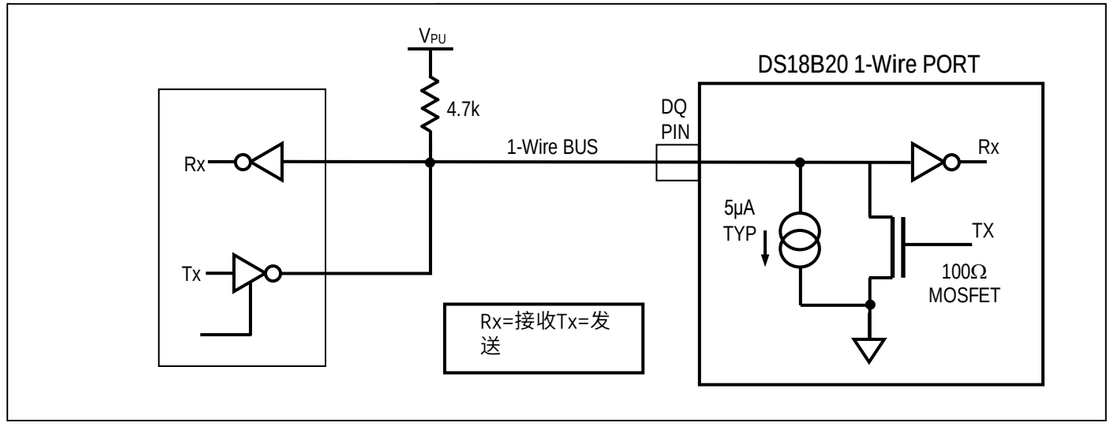
下面对1-Wire总线系统的讨论分为三个主题：硬件配置、事务顺序和1-Wire信令（信号类型和时序）。

硬件配置

根据定义，1-Wire总线只有一条数据线。每个器件（主器件或从器件）通过漏极开路或三态端口与数据线接口。这允许每个设备在设备不传输数据时"释放"数据线，以便总线可供另一个设备使用。DS18B20的1-Wire端口(DQ引脚)漏极开路，内部电路等效于图10所示。

1-Wire总线需要一个大约5kΩ的外部上拉电阻；因此，1-wire总线的空闲状态为高电平。如果由于任何原因需要暂停事务，如果要恢复事务，总线必须保持空闲状态。只要1-Wire总线在恢复期间处于非激活(高)状态，位之间就会出现无限恢复时间。如果总线保持低电平超过480µs，则总线上的所有元件都将复位。

图10。硬件配置



TRANSACTION SEQUENCE

The transaction sequence for accessing the DS18B20 is as follows:

Step 1. Initialization

Step 2. ROM Command (followed by any required data exchange)

Step 3. DS18B20 Function Command (followed by any required data exchange)

It is very important to follow this sequence every time the DS18B20 is accessed, as the DS18B20 will not respond if any steps in the sequence are missing or out of order. Exceptions to this rule are the Search ROM [F0h] and Alarm Search [ECh] commands. After issuing either of these ROM commands, the master must return to Step 1 in the sequence.

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that slave devices (such as the DS18B20) are on the bus and are ready to operate. Timing for the reset and presence pulses is detailed in the *1-Wire Signaling* section.

ROM COMMANDS

After the bus master has detected a presence pulse, it can issue a ROM command. These commands operate on the unique 64-bit ROM codes of each slave device and allow the master to single out a specific device if many are present on the 1-Wire bus. These commands also allow the master to determine how many and what types of devices are present on the bus or if any device has experienced an alarm condition. There are five ROM commands, and each command is 8 bits long. The master device must issue an appropriate ROM command before issuing a DS18B20 function command. A flowchart for operation of the ROM commands is shown in Figure 11.

SEARCH ROM [F0h]

When a system is initially powered up, the master must identify the ROM codes of all slave devices on the bus, which allows the master to determine the number of slaves and their device types. The master learns the ROM codes through a process of elimination that requires the master to perform a Search ROM cycle (i.e., Search ROM command followed by data exchange) as many times as necessary to identify all of the slave devices. If there is only one slave on the bus, the simpler Read ROM command (see below) can be used in place of the Search ROM process. For a detailed explanation of the Search ROM procedure, refer to the *iButton® Book of Standards* at www.maxim-ic.com/ibuttonbook. After every Search ROM cycle, the bus master must return to Step 1 (Initialization) in the transaction sequence.

READ ROM [33h]

This command can only be used when there is one slave on the bus. It allows the bus master to read the slave's 64-bit ROM code without using the Search ROM procedure. If this command is used when there is more than one slave present on the bus, a data collision will occur when all the slaves attempt to respond at the same time.

MATCH ROM [55h]

The match ROM command followed by a 64-bit ROM code sequence allows the bus master to address a specific slave device on a multidrop or single-drop bus. Only the slave that exactly matches the 64-bit ROM code sequence will respond to the function command issued by the master; all other slaves on the bus will wait for a reset pulse.

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交易顺序

访问DS18B20的事务顺序如下:

步骤1。初始化

第二步。ROM命令（后跟任何所需的数据交换）

第三步。DS18B20功能命令（后跟任何所需的数据交换）

每次访问DS18B20时，遵循这个顺序是非常重要的，因为如果序列中的任何步骤丢失或乱序，DS18B20将不会响应。此规则的例外是SearchROM[F0h]和AlarmSearch[ECh]命令。发出这些ROM命令中的任一命令后，主机必须返回序列中的步骤1。

1-Wire总线上的所有事务都以初始化序列开始。初始化序列由总线主机发送的复位脉冲和从机发送的存在脉冲组成。存在脉冲让总线主机知道从设备(如DS18B20)已在总线上并准备工作。复位和存在脉冲的时序在1-Wire信令部分有详细说明。

ROM命令

总线主控器检测到存在脉冲后，可以发出ROM命令。这些命令在每个从器件的唯一64位ROM代码上运行，如果1-Wire总线上存在多个器件，则允许主器件选择一个特定器件。这些命令还允许主站确定总线上有多少和什么类型的设备，或者是否有任何设备经历了报警条件。有五个ROM命令，每个命令是8位长。在发出DS18B20功能命令之前，主器件必须发出适当的ROM命令。ROM命令的操作流程图示于图11。

搜索ROM[F0h]

当系统最初上电时，主机必须识别总线上所有从设备的ROM代码，这允许主机确定从设备的数量及其设备类型。主机通过一个消除过程来学习ROM代码，该过程要求主机根据需要多次执行搜索ROM周期（即搜索ROM命令，然后进行数据交换），以识别所有从设备。如果总线上只有一个从机，则可以使用更简单的读ROM命令（见下文）来代替搜索ROM过程。有关搜索ROM程序的详细说明，请参阅iButton®标准手册，网址为www.maxim-ic.comibuttonbook.在每个搜索ROM周期之后，总线主机必须返回事务序列中的步骤1（初始化）。

读ROM[33h]

此命令只能在总线上有一个从机时使用。它允许总线主机在不使用搜索ROM程序的情况下读取从机的64位ROM代码。如果在总线上有多个从站时使用此命令，则当所有从站试图在同一时间响应时，将发生数据冲突。

匹配ROM[55h]

MatchROM命令后接64位ROM代码序列允许总线主机在多点或单点总线上寻址特定的从器件。只有与64位ROM代码序列完全匹配的从机才会响应主机发出的功能命令；总线上的所有其他从机将等待复位脉冲。

iButton是MaximIntegratedProducts Inc.的注册商标。

SKIP ROM [CCh]

The master can use this command to address all devices on the bus simultaneously without sending out any ROM code information. For example, the master can make all DS18B20s on the bus perform simultaneous temperature conversions by issuing a Skip ROM command followed by a Convert T [44h] command.

Note that the Read Scratchpad [BEh] command can follow the Skip ROM command only if there is a single slave device on the bus. In this case, time is saved by allowing the master to read from the slave without sending the device's 64-bit ROM code. A Skip ROM command followed by a Read Scratchpad command will cause a data collision on the bus if there is more than one slave since multiple devices will attempt to transmit data simultaneously.

ALARM SEARCH [ECh]

The operation of this command is identical to the operation of the Search ROM command except that only slaves with a set alarm flag will respond. This command allows the master device to determine if any DS18B20s experienced an alarm condition during the most recent temperature conversion. After every Alarm Search cycle (i.e., Alarm Search command followed by data exchange), the bus master must return to Step 1 (Initialization) in the transaction sequence. See the *Operation—Alarm Signaling* section for an explanation of alarm flag operation.

DS18B20 FUNCTION COMMANDS

After the bus master has used a ROM command to address the DS18B20 with which it wishes to communicate, the master can issue one of the DS18B20 function commands. These commands allow the master to write to and read from the DS18B20's scratchpad memory, initiate temperature conversions and determine the power supply mode. The DS18B20 function commands, which are described below, are summarized in Table 3 and illustrated by the flowchart in Figure 12.

CONVERT T [44h]

This command initiates a single temperature conversion. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the DS18B20 returns to its low-power idle state. If the device is being used in parasite power mode, within 10µs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for the duration of the conversion (t_{CONV}) as described in the *Powering the DS18B20* section. If the DS18B20 is powered by an external supply, the master can issue read time slots after the Convert T command and the DS18B20 will respond by transmitting a 0 while the temperature conversion is in progress and a 1 when the conversion is done. In parasite power mode this notification technique cannot be used since the bus is pulled high by the strong pullup during the conversion.

WRITE SCRATCHPAD [4Eh]

This command allows the master to write 3 bytes of data to the DS18B20's scratchpad. The first data byte is written into the T_H register (byte 2 of the scratchpad), the second byte is written into the T_L register (byte 3), and the third byte is written into the configuration register (byte 4). Data must be transmitted least significant bit first. All three bytes MUST be written before the master issues a reset, or the data may be corrupted.

READ SCRATCHPAD [BEh]

This command allows the master to read the contents of the scratchpad. The data transfer starts with the least significant bit of byte 0 and continues through the scratchpad until the 9th byte (byte 8 – CRC) is read. The master may issue a reset to terminate reading at any time if only part of the scratchpad data is needed.

跳过ROM[CCh]

主机可以使用此命令同时寻址总线上的所有设备，而无需发送任何ROM代码信息。例如，主机可以通过发出跳过ROM命令和转换T[44h]命令，使总线上的所有Ds18b20同时进行温度转换。请注意，只有当总线上有一个从器件时，读暂存器[BEh]命令才能遵循跳过ROM命令。在这种情况下，通过允许主机从从机读取而不发送器件的64位ROM代码来节省时间。如果有多个从机，则跳过ROM命令后接读暂存器命令将导致总线上的数据冲突，因为多个器件将尝试同时传输数据。

警报搜寻[ECh]

该命令的操作与搜索ROM命令的操作相同，只是只有具有设置报警标志的从站才会响应。该命令允许主器件确定在最近的温度转换过程中是否有Ds18b20出现报警情况。在每个告警搜索周期（即告警搜索命令后接数据交换）之后，总线主控器必须返回事务序列中的步骤1（初始化）。有关警报标志操作的解释 请参阅操作-警报信令部分.

DS18B20功能命令

总线主机使用ROM命令寻址希望与之通信的DS18B20后，主机可以发出DS18B20功能命令之一。这些命令允许主机写入和读取DS18B20的暂存器，启动温度转换并确定电源模式。表3总结了DS18B20的功能命令，并由图12的流程图说明。

CONVERT T [44h]

此命令启动单个温度转换。转换后，产生的热数据存储在暂存器的2字节温度寄存器中，DS18B20返回到低功耗空闲状态。如果器件在寄生电源模式下使用，则在发出此命令后的10µs(max)内，主机必须在转换期间在1-Wire总线上启用强上拉(tCONV)，如DS18B20供电部分所述。如果DS18B20由外部电源供电，主机可以在转换T命令后发出读取时隙，DS18B20将在温度转换进行时发送0，转换完成后发送1。在寄生电源模式下，这种通知技术不能使用，因为总线在转换过程中被强拉高拉高。

WRITE SCRATCHPAD [4Eh]

该命令允许主机向DS18B20的暂存器写入3个字节的数据。第一个数据字节写入TH寄存器（暂存器的字节2），第二个字节写入TL寄存器（字节3），第三个字节写入配置寄存器（字节4）。数据必须首先传输最低有效位。在主机发出复位之前，必须写入所有三个字节，否则数据可能已损坏。

READ SCRATCHPAD [BEh]

此命令允许主机读取暂存器的内容。数据传输从字节0的最低有效位开始，并通过暂存器继续，直到读取第9个字节(字节8-CRC)。如果只需要一部分暂存器数据，主机可以随时发出复位以终止读取。

COPY SCRATCHPAD [48h]

This command copies the contents of the scratchpad T_H, T_L and configuration registers (bytes 2, 3 and 4) to EEPROM. If the device is being used in parasite power mode, within 10µs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for at least 10ms as described in the *Powering the DS18B20* section.

RECALL E^2 [B8h]

This command recalls the alarm trigger values (T_H and T_L) and configuration data from EEPROM and places the data in bytes 2, 3, and 4, respectively, in the scratchpad memory. The master device can issue read time slots following the Recall E^2 command and the DS18B20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done. The recall operation happens automatically at power-up, so valid data is available in the scratchpad as soon as power is applied to the device.

READ POWER SUPPLY [B4h]

The master device issues this command followed by a read time slot to determine if any DS18B20s on the bus are using parasite power. During the read time slot, parasite powered DS18B20s will pull the bus low, and externally powered DS18B20s will let the bus remain high. See the *Powering the DS18B20* section for usage information for this command.

Table 3. DS18B20 Function Command Set

COMMAND	DESCRIPTION	PROTOCOL	1-Wire BUS ACTIVITYAFTER COMMAND IS ISSUED	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	DS18B20 transmits conversion status to master (not applicable for parasite-powered DS18B20s).	1
MEMORY COMMANDS				
Read Scratchpad	Reads the entire scratchpad including the CRC byte.	BEh	DS18B20 transmits up to 9 data bytes to master.	2
Write Scratchpad	Writes data into scratchpad bytes 2, 3, and 4 (T_H, T_L, and configuration registers).	4Eh	Master transmits 3 data bytes to DS18B20.	3
Copy Scratchpad	Copies T_H, T_L, and configuration register data from the scratchpad to EEPROM.	48h	None	1
Recall E^2	Recalls T_H, T_L, and configuration register data from EEPROM to the scratchpad.	B8h	DS18B20 transmits recall status to master.	
Read Power Supply	Signals DS18B20 power supply mode to the master.	B4h	DS18B20 transmits supply status to master.	

Note 1: For parasite-powered DS18B20s, the master must enable a strong pullup on the 1-Wire bus during temperature conversions and copies from the scratchpad to EEPROM. No other bus activity may take place during this time.
Note 2: The master can interrupt the transmission of data at any time by issuing a reset.
Note 3: All three bytes must be written before a reset is issued.

该命令将暂存器TH、TL和配置寄存器(字节2、3和4)的内容复制到EEPROM。如果器件在寄生电源模式下使用，则在发出此命令后的10µs(最大值)内，主机必须在1-Wire总线上使能强上拉至少10 ms，如DS18B20供电部分所述。

2

该命令从EEPROM中调用报警触发值(TH和TL)和配置数据，并将数据分别以字节2、3和4的形式放入暂存器中。主器件可以在RecallE2命令后发出读取时隙，DS18B20将在recall进行时发送0，在recall完成时发送1，以指示recall的状态。召回操作在上电时自动发生，因此在器件上电后，暂存器中可提供有效数据。

读取电源[B4h]

主器件发出此命令后跟读取时隙，以确定总线上是否有Ds18b20使用寄生电源。在读取时隙期间，寄生供电的DS18B20s将把总线拉低，外部供电的DS18B20s将让总线保持高电平。有关此命令的使用信息，请参阅DS18B20供电部分。

表3。DS18B20功能命令集

COMMAND	DESCRIPTION	PROTOCOL	1-Wire BUS 命令发出	NOTES
温度转换命令				
Convert T	启动温度转换。	44h	DS18B20将转换状态传送到主机(不适用于寄生功率DS18B20s)。	1
内存命令				
Read Scratchpad	读取整个暂存器，包括CRC字节。	BEh	DS18B20向主机传输多达9个数据字节。	2
Write Scratchpad	将数据写入暂存器字节2、3和4(TH、TL和配置寄存器)。	4Eh	Master向DS18B20传输3个数据字节。	3
Copy Scratchpad	将tH、TL和配置寄存器数据从暂存器复制到EEPROM。	48h	None	1
Recall E^2	将TH、TL和配置寄存器数据从EEPROM恢复到暂存器。	B8h	DS18B20将召回状态传送给master。	
读取功率	信号DS18B20向主控供电模式。	B4h	DS18B20将电源状态传送给主控器。	

Note 1: 对于寄生供电的Ds18b20，主机必须在温度转换和从暂存器复制到EEPROM期间使能1-Wire总线上的强上拉。在此期间不得进行其他巴士活动。
Note 2: 主机可以随时通过发出复位来中断数据的传输。
Note 3: 在发出复位之前，必须写入所有三个字节。

Figure 11. ROM Commands Flowchart

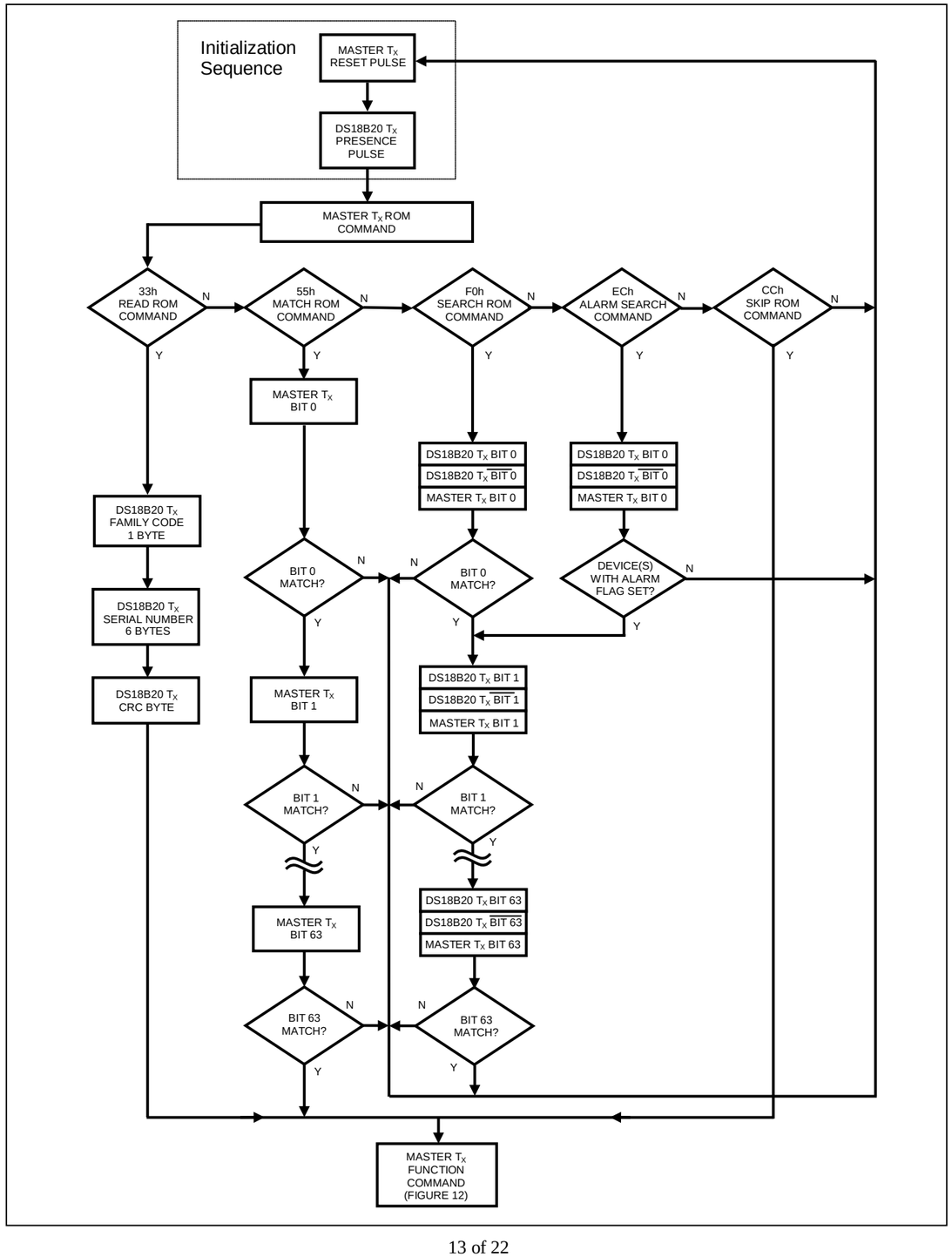


图11。ROM命令流程图

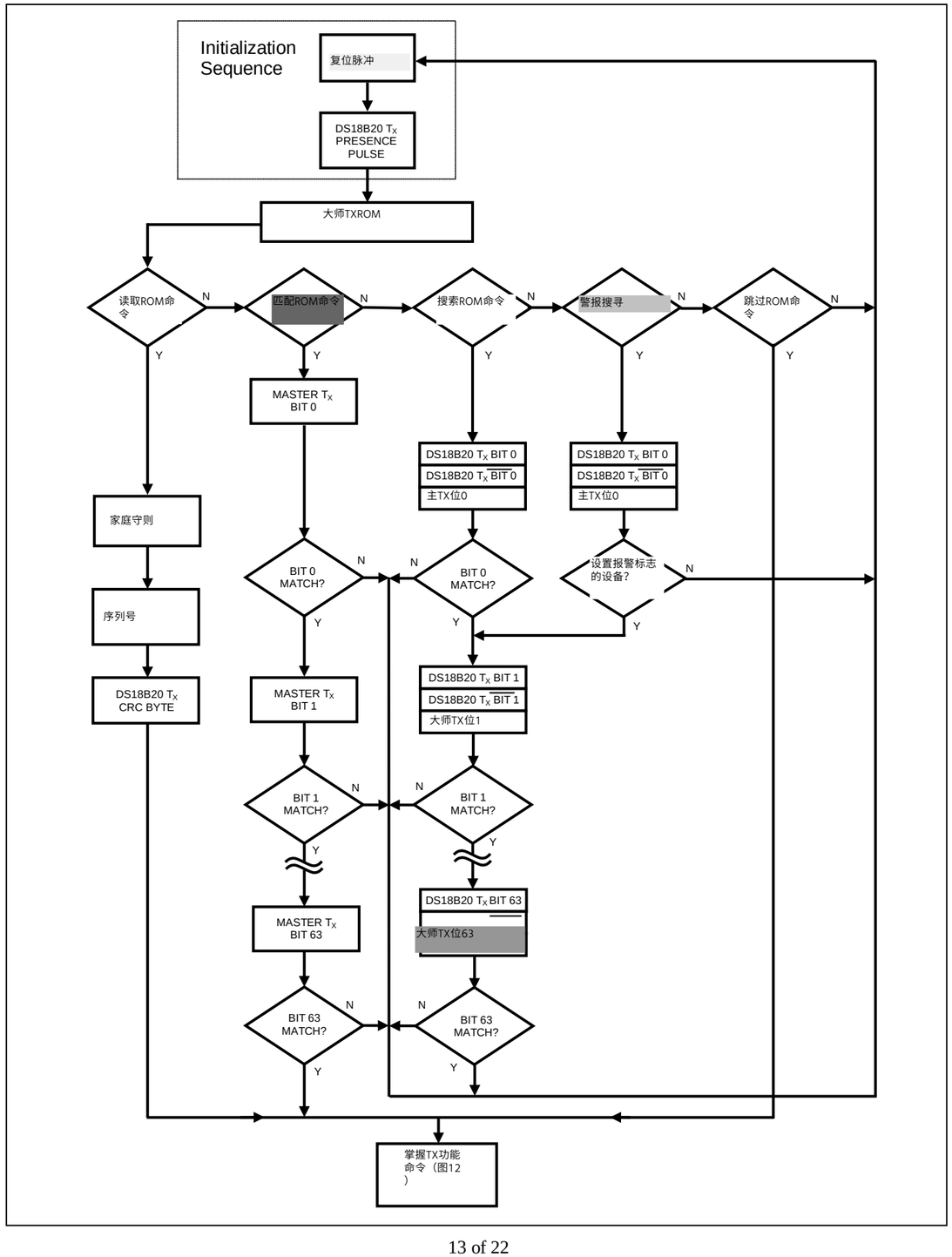


Figure 12. DS18B20 Function Commands Flowchart

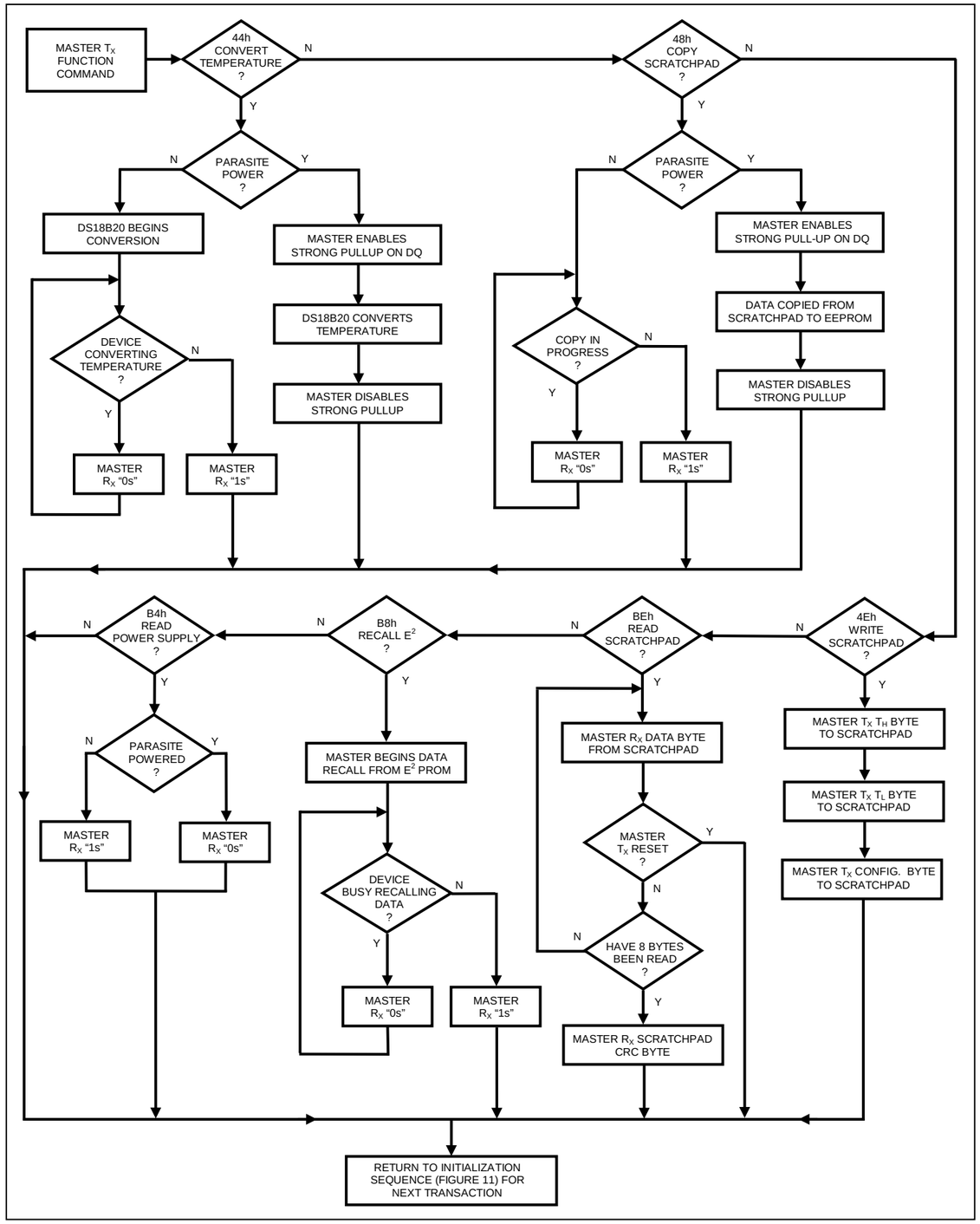
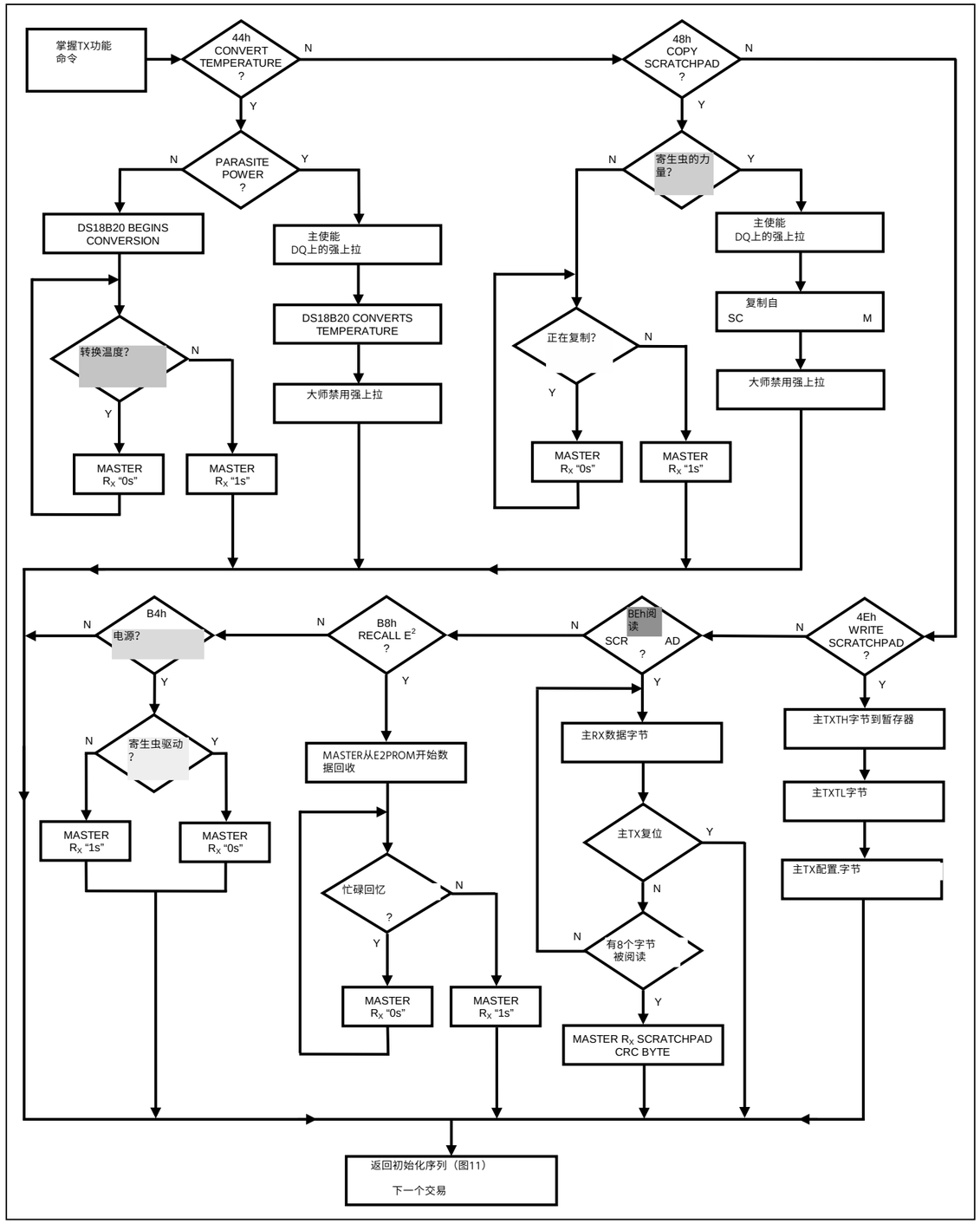


图12.DS18B20功能命令流程图



1-WIRE SIGNALING

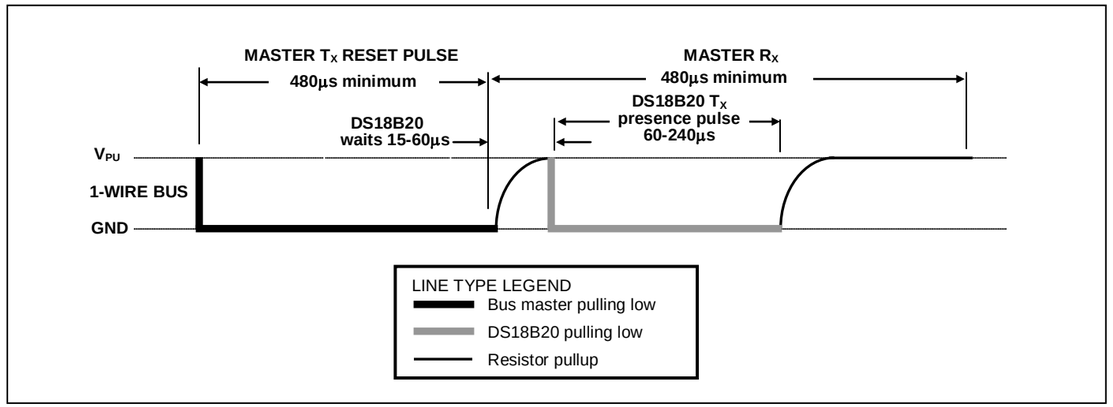
The DS18B20 uses a strict 1-Wire communication protocol to ensure data integrity. Several signal types are defined by this protocol: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. The bus master initiates all these signals, with the exception of the presence pulse.

INITIALIZATION PROCEDURE—RESET AND PRESENCE PULSES

All communication with the DS18B20 begins with an initialization sequence that consists of a reset pulse from the master followed by a presence pulse from the DS18B20. This is illustrated in Figure 13. When the DS18B20 sends the presence pulse in response to the reset, it is indicating to the master that it is on the bus and ready to operate.

During the initialization sequence the bus master transmits (T_X) the reset pulse by pulling the 1-Wire bus low for a minimum of 480µs. The bus master then releases the bus and goes into receive mode (R_X). When the bus is released, the 5kΩ pullup resistor pulls the 1-Wire bus high. When the DS18B20 detects this rising edge, it waits 15µs to 60µs and then transmits a presence pulse by pulling the 1-Wire bus low for 60µs to 240µs.

Figure 13. Initialization Timing



READ/WRITE TIME SLOTS

The bus master writes data to the DS18B20 during write time slots and reads data from the DS18B20 during read time slots. One bit of data is transmitted over the 1-Wire bus per time slot.

WRITE TIME SLOTS

There are two types of write time slots: “Write 1” time slots and “Write 0” time slots. The bus master uses a Write 1 time slot to write a logic 1 to the DS18B20 and a Write 0 time slot to write a logic 0 to the DS18B20. All write time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between individual write slots. Both types of write time slots are initiated by the master pulling the 1-Wire bus low (see Figure 14).

To generate a Write 1 time slot, after pulling the 1-Wire bus low, the bus master must release the 1-Wire bus within 15µs. When the bus is released, the 5kΩ pullup resistor will pull the bus high. To generate a Write 0 time slot, after pulling the 1-Wire bus low, the bus master must continue to hold the bus low for the duration of the time slot (at least 60µs).

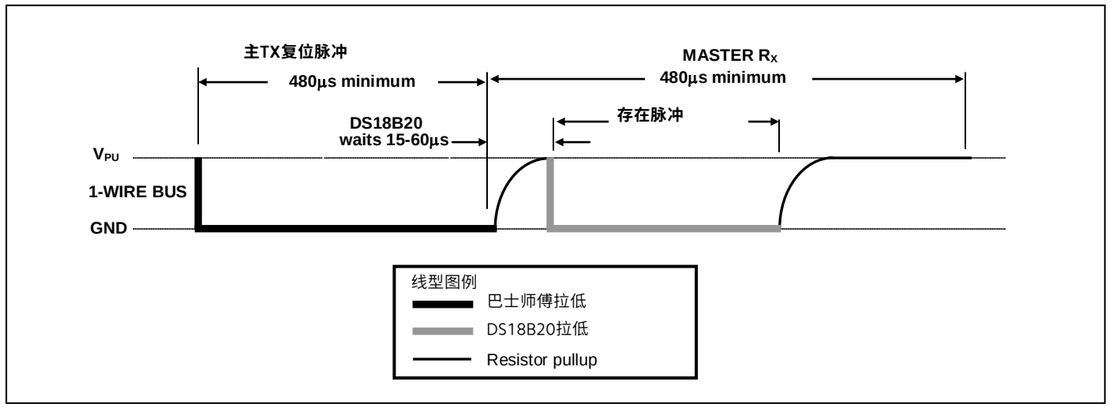
1-WIRE信令DS18B20采用严格的1-Wire通信协议来确保数据完整性。该协议定义了几种信号类型：复位脉冲、存在脉冲、写0、写1、读0和读1。总线主控器启动所有这些信号，但存在脉冲除外。

初始化过程-复位和存在脉冲

与DS18B20的所有通信都始于一个初始化序列，该序列由一个来自主机的复位脉冲和一个来自DS18B20的存在脉冲组成。这在图13中说明。当DS18B20响应复位发送存在脉冲时，它向主机指示它已在总线上并准备工作。

在初始化过程中，总线主机通过将1线总线拉低至少480秒来发送复位脉冲（Tx）。然后总线主机释放总线并进入接收模式（Rx）。当总线被释放时，5kΩ上拉电阻将1-Wire总线拉高。当DS18B20检测到这个上升沿时，它会等待15µs至60µs，然后通过将1-Wire总线拉低60µs至240µs来发送存在脉冲。

图13。初始化定时



读写时隙

总线主机在写时隙向DS18B20写入数据，在读时隙从DS18B20读取数据。每个时隙通过1-Wire总线传输一位数据。

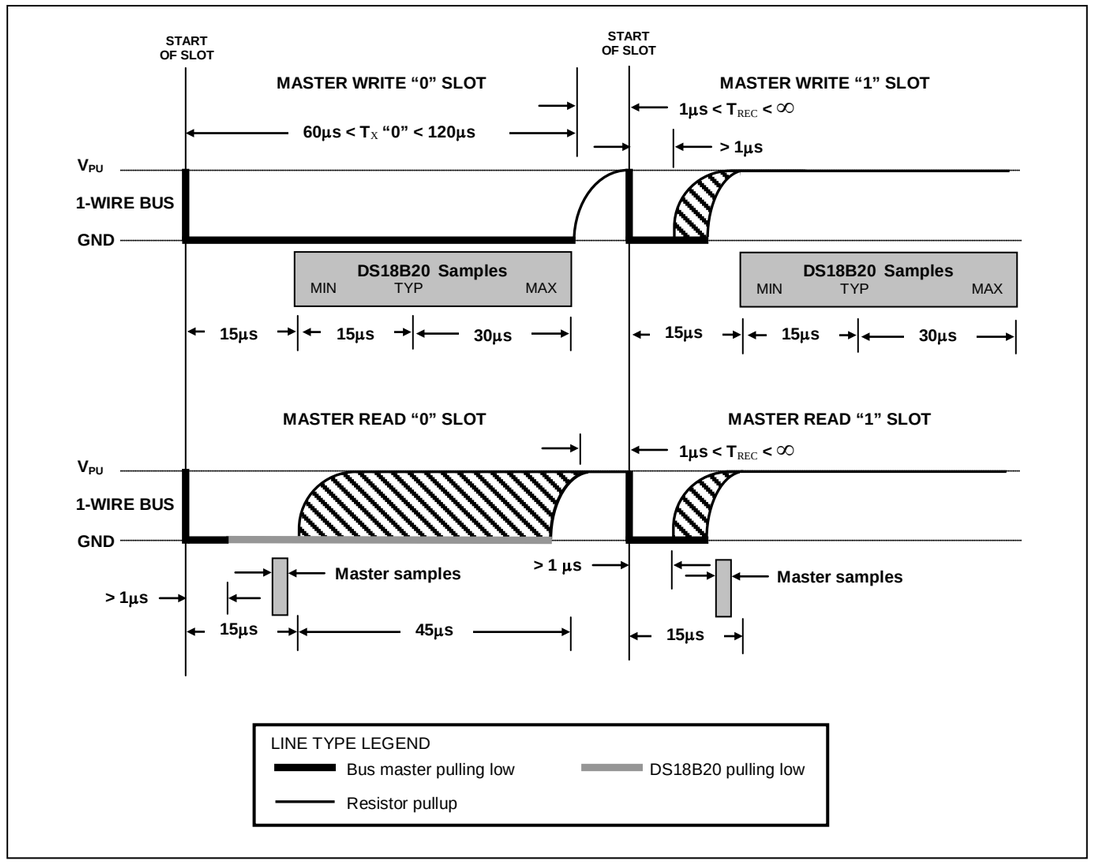
写入时隙

有两种类型的写入时隙："写入1"时隙和"写入0"时隙。总线主机使用写1时隙将逻辑1写入DS18B20，写0时隙将逻辑0写入DS18B20。所有写入时隙的持续时间必须至少为60µs，各个写入时隙之间的恢复时间至少为1µs。两种类型的写入时隙都是由主机将1-Wire总线拉低启动的(见图14)。

为了产生一个写1时隙，在将1线总线拉低后，总线主机必须在15秒内释放1线总线。为了产生写0时隙，在将1-Wire总线拉低后，总线主机必须在该时隙的持续时间内（至少60µs）继续保持总线低电平。

The DS18B20 samples the 1-Wire bus during a window that lasts from 15µs to 60µs after the master initiates the write time slot. If the bus is high during the sampling window, a 1 is written to the DS18B20. If the line is low, a 0 is written to the DS18B20.

Figure 14. Read/Write Time Slot Timing Diagram



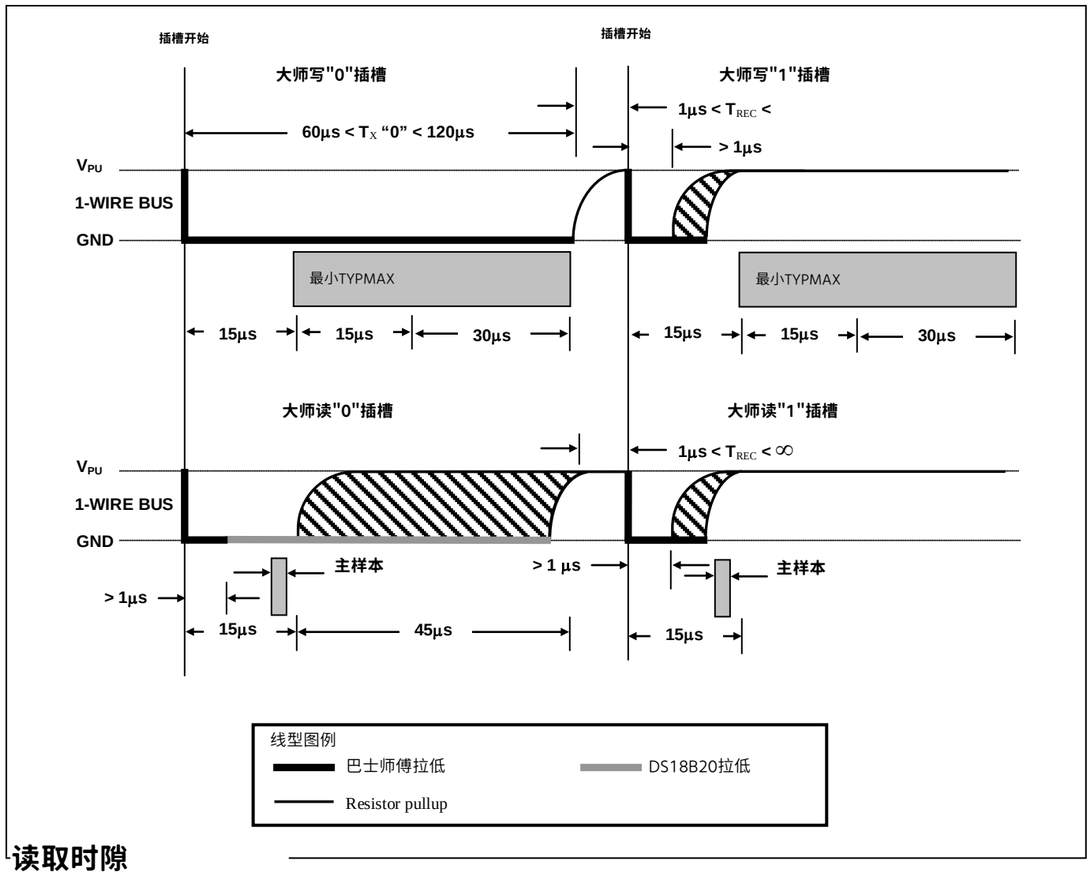
READ TIME SLOTS

The DS18B20 can only transmit data to the master when the master issues read time slots. Therefore, the master must generate read time slots immediately after issuing a Read Scratchpad [BEh] or Read Power Supply [B4h] command, so that the DS18B20 can provide the requested data. In addition, the master can generate read time slots after issuing Convert T [44h] or Recall E^2 [B8h] commands to find out the status of the operation as explained in the *DS18B20 Function Commands* section.

All read time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between slots. A read time slot is initiated by the master device pulling the 1-Wire bus low for a minimum of 1µs and then releasing the bus (see Figure 14). After the master initiates the read time slot, the DS18B20 will begin transmitting a 1 or 0 on bus. The DS18B20 transmits a 1 by leaving the bus high and transmits a 0 by pulling the bus low. When transmitting a 0, the DS18B20 will release the bus by the end of the time slot, and the bus will be pulled back to its high idle state by the pullup resister. Output

在主机启动写入时隙后，DS18B20在15µs至60µs的窗口内对1-Wire总线进行采样。如果在采样窗口期间总线为高电平，则将1写入DS18B20。如果线路为低电平，则将0写入DS18B20。

图14。读写时隙时序图



读取时隙

DS18B20只能在主机发出读取时隙时向主机传输数据。因此，主机必须在发出读暂存器[BEh]或读电源[B4h]命令后立即产生读时隙，以便DS18B20能够提供所请求的数据。此外，主机可以在发出ConvertT[44h]或RecallE2[B8h]命令后生成读取时隙，以了解DS18B20功能命令部分所述的操作状态。

所有读取时隙的持续时间必须至少为60µs，时隙之间的恢复时间至少为1µs。读取时隙由主器件将1-Wire总线拉低至少1µs然后释放总线启动(见图14)。主机启动读时隙后，DS18B20将开始在总线上发送1或0。DS18B20通过将总线保持为高电平传输a1，通过将总线拉低传输a0。发送0时，DS18B20将在时隙结束时释放总线，上拉电阻将总线拉回到高空闲状态。输出

data from the DS18B20 is valid for 15µs after the falling edge that initiated the read time slot. Therefore, the master must release the bus and then sample the bus state within 15µs from the start of the slot.

Figure 15 illustrates that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs for a read time slot. Figure 16 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as short as possible and by locating the master sample time during read time slots towards the end of the 15µs period.

Figure 15. Detailed Master Read 1 Timing

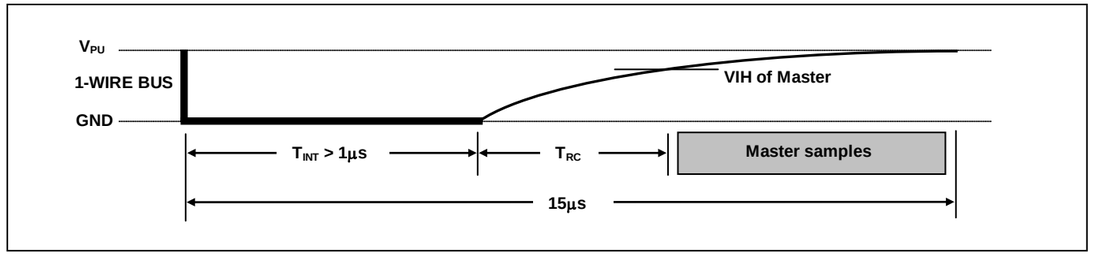
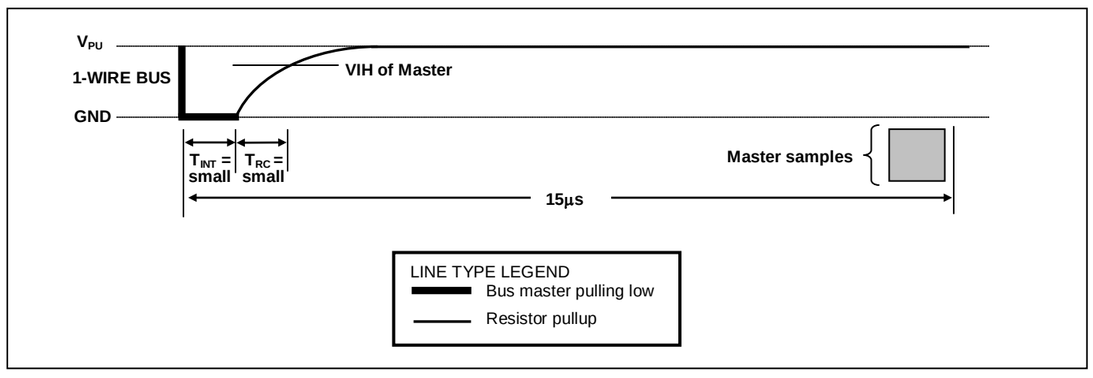


Figure 16. Recommended Master Read 1 Timing



RELATED APPLICATION NOTES

The following application notes can be applied to the DS18B20 and are available on our website at www.maxim-ic.com.

Application Note 27: Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products
Application Note 122: Using Dallas' 1-Wire ICs in 1-Cell Li-Ion Battery Packs with Low-Side N-Channel Safety FETs Master
Application Note 126: 1-Wire Communication Through Software
Application Note 162: Interfacing the DS18x20/DS1822 1-Wire Temperature Sensor in a Microcontroller Environment
Application Note 208: Curve Fitting the Error of a Bandgap-Based Digital Temperature Sensor
Application Note 2420: 1-Wire Communication with a Microchip PICmicro Microcontroller
Application Note 3754: Single-Wire Serial Bus Carries Isolated Power and Data

Sample 1-Wire subroutines that can be used in conjunction with *Application Note 74: Reading and Writing iButtons via Serial Interfaces* can be downloaded from the Maxim website.

DS18B20的数据在启动读取时隙的下降沿后的15µs内有效。因此，主机必须释放总线，然后在从插槽开始的15秒内对总线状态进行采样。

图15说明，对于一个读取时隙，TINIT、TRC和T采样的总和必须小于15µs。图16显示，通过保持TINIT和TRC尽可能短，并将读取时隙中的主采样时间定位在接近15µs周期结束时，系统时序裕度最大化。

图15。详细主读1时序

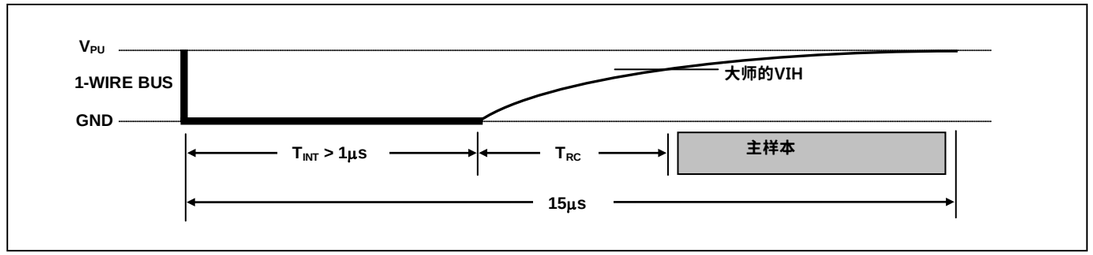
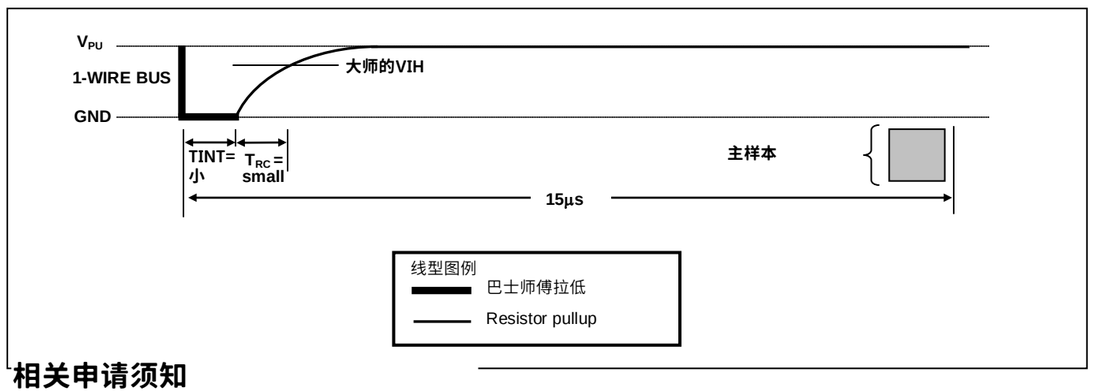


图16。推荐主读1定时



相关申请须知

以下应用说明可应用于DS18B20，可在我们的网站上找到：www.maxim-ic.com...

应用笔记27：理解和使用MaximiButton产品的循环冗余检查应用笔记122：在低边N通道的1节锂离子电池组中使用达拉斯的1线集成电路

安全FETs大师
应用笔记126：通过软件实现1-Wire通信
应用笔记162：在微控制器中连接DS18x20DS18221-Wire温度传感器
Environment
应用笔记208：曲线拟合基于带隙的数字温度传感器的误差
应用笔记2420：与MicrochipPICmicro微控制器的1线通信
应用笔记3754：单线串行总线传输隔离电源和数据
示例1-Wire子例程，可与应用笔记74一起使用：阅读和

通过串行接口编写ibutton可以从Maxim网站下载.

DS18B20 OPERATION EXAMPLE 1

In this example there are multiple DS18B20s on the bus and they are using parasite power. The bus master initiates a temperature conversion in a specific DS18B20 and then reads its scratchpad and recalculates the CRC to verify the data.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18B20s respond with presence pulse.
Tx	55h	Master issues Match ROM command.
Tx	64-bit ROM code	Master sends DS18B20 ROM code.
Tx	44h	Master issues Convert T command.
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for the duration of the conversion (t_{CONV}).
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18B20s respond with presence pulse.
Tx	55h	Master issues Match ROM command.
Tx	64-bit ROM code	Master sends DS18B20 ROM code.
Tx	BEh	Master issues Read Scratchpad command.
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.

DS18B20 OPERATION EXAMPLE 2

In this example there is only one DS18B20 on the bus and it is using parasite power. The master writes to the T_H, T_L, and configuration registers in the DS18B20 scratchpad and then reads the scratchpad and recalculates the CRC to verify the data. The master then copies the scratchpad contents to EEPROM.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18B20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	4Eh	Master issues Write Scratchpad command.
Tx	3 data bytes	Master sends three data bytes to scratchpad (T_H, T_L, and config).
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18B20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	BEh	Master issues Read Scratchpad command.
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18B20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	48h	Master issues Copy Scratchpad command.
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for at least 10ms while copy operation is in progress.

DS18B20操作示例1

在本例中，总线上有多个Ds18b20，它们使用寄生电源。总线主机在特定的DS18B20中启动温度转换，然后读取其暂存器并重新计算CRC以验证数据。

主模式	DATA (LSB FIRST)	MMENTS
	Reset	主发出复位脉冲。
Rx	Presence	DS18B20s响应存在脉冲。
Tx		主发出匹配ROM命令。
Tx	64位ROM代码	Master发送DS18B20ROM代码。
Tx		主发出转换T命令.
Tx	DQ线高企	Master在转换(TCONV)期间对DQ施加强上拉。
Tx	Reset	主发出复位脉冲。
Rx	Presence	DS18B20s响应存在脉冲。
Tx		主发出匹配ROM命令。
Tx	64位ROM代码	Master发送DS18B20ROM代码。
Tx		主发出读取暂存器命令。
Rx	9数据字节	主机读取整个暂存器，包括CRC。然后，主机从暂存器重新计算前八个数据字节的CRC，并将计算的CRC与读取的CRC进行比较（字节9）。如果它们匹配，则主控器继续；如果不匹配，则重复读取操作。

DS18B20操作示例2

在这个例子中，总线上只有一个DS18B20，它使用寄生电源。主机写入Ds18b20暂存器中的TH、TL和配置寄存器，然后读取暂存器并重新计算CRC以验证数据。然后，主机将暂存器内容复制到EEPROM。

主模式	DATA (LSB FIRST)	OMMENTS
	Reset	主发出复位脉冲。
Rx	Presence	DS18B20响应存在脉冲。
Tx	CCh	主发出跳过ROM命令.
Tx		主发出写暂存器命令。
Tx	3数据字节	主机向暂存器发送三个数据字节(TH、TL和config)。
Tx		主发出复位脉冲。
Rx	Presence	DS18B20响应存在脉冲。
Tx	CCh	主发出跳过ROM命令.
Tx	BEh	主发出读取暂存器命令。
Rx	9数据字节	主机读取整个暂存器，包括CRC。然后，主机从暂存器重新计算前八个数据字节的CRC，并将计算的CRC与读取的CRC进行比较（字节9）。如果它们匹配，则主控器继续；如果不匹配，则重复读取操作。
Tx	Reset	主发出复位脉冲。
Rx	Presence	DS18B20响应存在脉冲。
Tx	CCh	主发出跳过ROM命令.
Tx		主机发出复制暂存器命令.
Tx	DQ线高企	当复制操作正在进行时，Master对DQ应用强上拉至少10ms。

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground .....-0.5V to +6.0V
Operating Temperature Range .....-55°C to +125°C
Storage Temperature Range.....-55°C to +125°C
Solder Temperature .....Refer to the IPC/JEDEC J-STD-020 Specification.

These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (-55°C to +125°C; V_{DD}=3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	Local Power	+3.0		+5.5	V	1
Pullup Supply Voltage	V_{PU}	Parasite Power	+3.0		+5.5	V	1,2
		Local Power	+3.0		V_{DD}		
Thermometer Error	t_{ERR}	-10°C to +85°C			±0.5	°C	3
		-55°C to +125°C			±2		
Input Logic-Low	V_{IL}		-0.3		+0.8	V	1,4,5
Input Logic-High	V_{IH}	Local Power	+2.2		The lower of 5.5 or V_{DD} + 0.3	V	1, 6
		Parasite Power	+3.0				
Sink Current	I_L	$V_{I/O}$ = 0.4V	4.0			mA	1
Standby Current	I_{DDS}			750	1000	nA	7,8
Active Current	I_{DD}	V_{DD} = 5V		1	1.5	mA	9
DQ Input Current	I_{DQ}			5		µA	10
Drift				±0.2		°C	11

NOTES:

1) All voltages are referenced to ground.
2) The Pullup Supply Voltage specification assumes that the pullup device is ideal, and therefore the high level of the pullup is equal to V_{PU}. In order to meet the V_{IH} spec of the DS18B20, the actual supply rail for the strong pullup transistor must include margin for the voltage drop across the transistor when it is turned on; thus: $V_{PU\_ACTUAL} = V_{PU\_IDEAL} + V_{TRANSISTOR}$.
3) See typical performance curve in Figure 17.
4) Logic-low voltages are specified at a sink current of 4mA.
5) To guarantee a presence pulse under low voltage parasite power conditions, V_{ILMAX} may have to be reduced to as low as 0.5V.
6) Logic-high voltages are specified at a source current of 1mA.
7) Standby current specified up to +70°C. Standby current typically is 3µA at +125°C.
8) To minimize I_{DDS}, DQ should be within the following ranges: GND ≤ DQ ≤ GND + 0.3V or V_{DD} – 0.3V ≤ DQ ≤ V_{DD}.
9) Active current refers to supply current during active temperature conversions or EEPROM writes.
10) DQ line is high (“high-Z” state).
11) Drift data is based on a 1000-hour stress test at +125°C with V_{DD} = 5.5V.

绝对最大额定值

任何引脚相对于地的电压范围。.....-0.5V至+6.0V
工作温度范围。.....-55°C至+125°C
储存温度范围。.....-55°C至+125°C
焊料温度。.....参考IPCJEDECJ-STD-020规范。
这些仅仅是压力额定值，设备在这些或任何其他条件下的功能操作在本说明书的操作部分指出的那些不是暗示。长时间暴露在绝对最大额定值条件下可能会影响可靠性。

直流电电特性

(-55°C to +125°C; V_D =3.0V to 5.5V)

			MIN	TYP	MAX	单位注意事项	
电源电压	V_{DD}	地方权力	+3.0		+5.5		
Pullup Supply Voltage	V_{PU}	寄生虫力量	+3.0		+5.5	V	1,2
		地方权力	+3.0		V_{DD}		
Thermometer Error	t_{ERR}	C			±0.5	°C	3
		-55°C to +125°C			±2		
Input Logic-Low	V_{IL}		-0.3		+0.8	V	1,4,5
Input Logic-High	V_{IH}	地方权力	+2.2		较低的5.5或VDD+0.3	V	1, 6
		寄生虫力量	+3.0				
吸收电流	I_L	$V_{I/O}$ = 0.4V	4.0			mA	1
待机电流	I_{DDS}			750	1000	nA	7,8
有源电流	I_{DD}	V_{DD} = 5V		1	1.5	mA	9
DQ输入电流	I_{DQ}			5		µA	10
Drift				±0.2		°C	11

注：1）所有电压均以地为参考。2)上拉电源电压规范假设上拉器件是理想的，因此上拉的高电平等于VPU。为了满足DS18B20的VIH规范，强上拉晶体管的实际供电轨必须包括晶体管导通时电压降的裕量；因此：VPU_ACTUAL=VPU_IDEAL+V晶体管。3)参见图17中的典型性能曲线。4)逻辑-低电压在4ma的灌电流下指定。5)为了保证在低电压寄生功率条件下存在脉冲，VIL MAX可能必须降低到0.5v。6)逻辑高电压指定在1ma的源电流下。待机电流在+125°C时通常为3µA。8)为最大限度地减少IDDS，DQ应在以下范围内：GND≤DQ≤GND+0.3V或VDD-0.3V≤DQ≤VDD。9)有源电流是指在有源温度转换或EEPROM写入期间的电源电流。10)DQ线为高电平("高-Z"状态)。11)漂移数据基于+125°c下的1000小时应力测试，VDD=5.5V。

AC ELECTRICAL CHARACTERISTICS—NV MEMORY

(-55°C to +100°C; V_{DD} = 3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NV Write Cycle Time	t_{WR}			2	10	ms
EEPROM Writes	N_{EEWR}	-55°C to +55°C	50k			writes
EEPROM Data Retention	t_{EEDR}	-55°C to +55°C	10			years

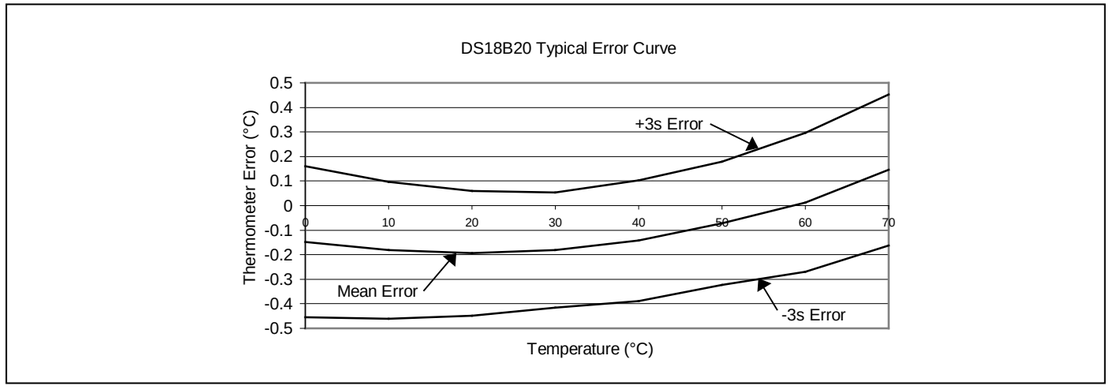
AC ELECTRICAL CHARACTERISTICS (-55°C to +125°C; V_{DD} = 3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}	9-bit resolution			93.75	ms	1
		10-bit resolution			187.5		
		11-bit resolution			375		
		12-bit resolution			750		
Time to Strong Pullup On	t_{SPON}	Start Convert T Command Issued			10	µs	
Time Slot	t_{SLOT}		60		120	µs	1
Recovery Time	t_{REC}		1			µs	1
Write 0 Low Time	t_{LOW0}		60		120	µs	1
Write 1 Low Time	t_{LOW1}		1		15	µs	1
Read Data Valid	t_{RDV}				15	µs	1
Reset Time High	t_{RSTH}		480			µs	1
Reset Time Low	t_{RSTL}		480			µs	1,2
Presence-Detect High	t_{PDHIGH}		15		60	µs	1
Presence-Detect Low	t_{PDLOW}		60		240	µs	1
Capacitance	$C_{IN/OUT}$				25	pF	

NOTES:

1) See the timing diagrams in Figure 18.
2) Under parasite power, if t_{RSTL} > 960µs, a power-on reset may occur.

Figure 17. Typical Performance Curve



交流电电特性-NV存储器

0°C; V_{DD} = 3.0V to 5.5V)

	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NV写周期时间	t_{WR}			2	10	ms
	N_{EEWR}	-55°C to +55°C	50k			writes
EEPROM数据保留						

AC电气特性(-55°c至+125°C;VDD=3.0V至5.5V)

			最小TYP最大单位			
温度转换	t_{CONV}	9-bit resolution			ms	1
		10-bit resolution		187.5		
		11-bit resolution		375		
				750		
是时候强力上拉了	t_{SPON}	开始转换T 发出命令		10	µs	
时间段	t_{SLOT}		60	120	µs	1
恢复时间	t_{REC}		1		µs	1
写0低时间	t_{LOW0}		60	120	µs	1
写1低时间	t_{LOW1}		1	15	µs	1
读取数据有效	t_{RDV}			15	µs	1
复位时间高	t_{RSTH}		480		µs	1
复位时间低	t_{RSTL}		480		µs	1,2
Presence-Detect High	t_{PDHIGH}		15	60	µs	1
Presence-Detect Low	t_{PDLOW}		60	240	µs	1
Capacitance	$C_{IN/OUT}$			25	pF	

注：1）请参阅图18中的时序图。2)在寄生电源下，如果tRSTL>960µs，则可能发生上电复位。

图17。典型性能曲线

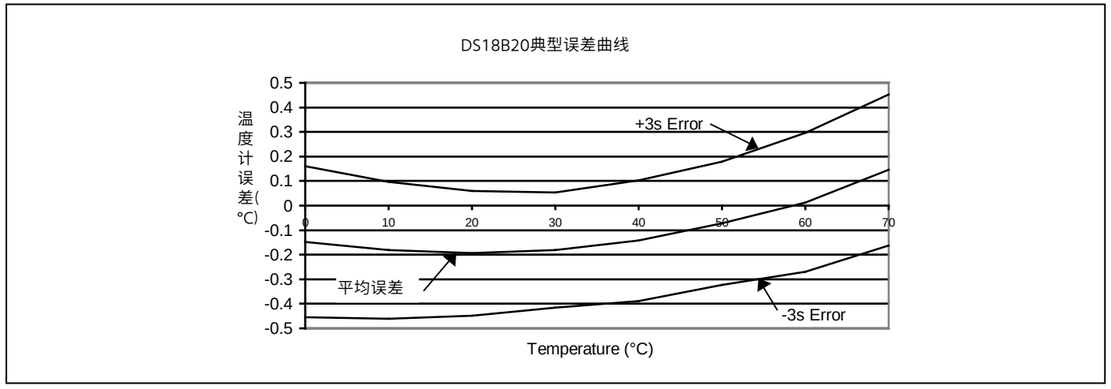


Figure 18. Timing Diagrams

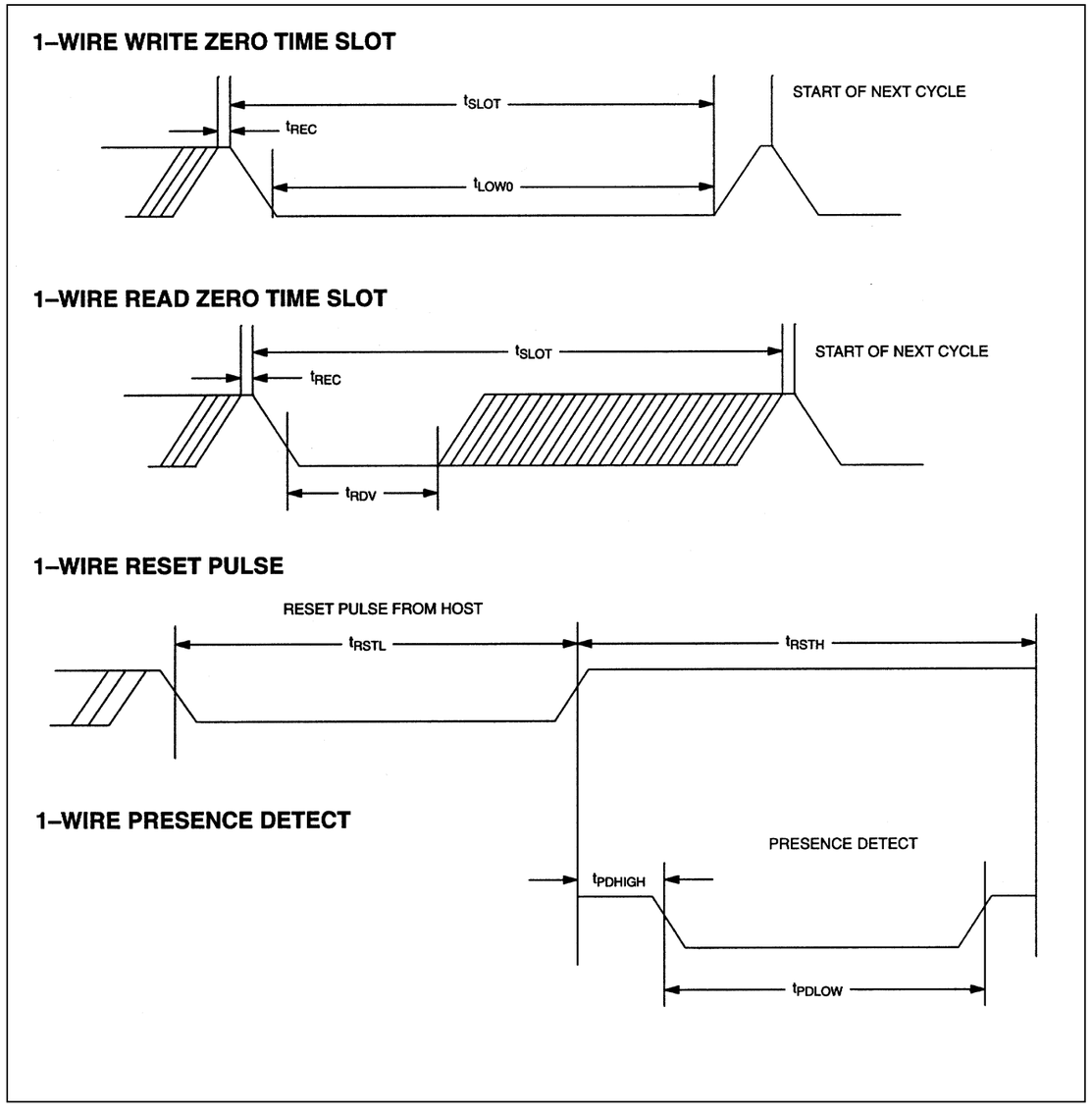
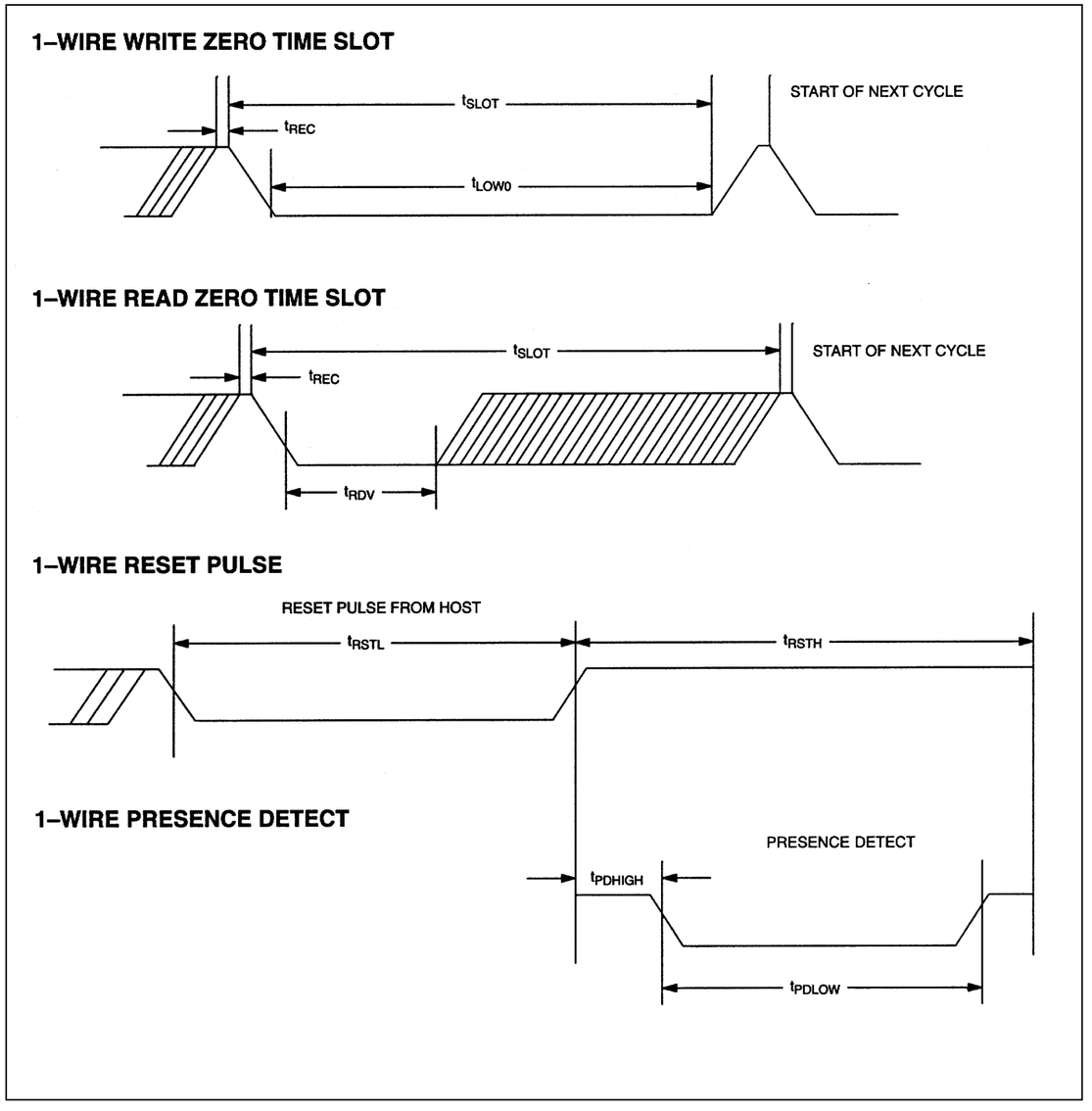


图18。时序图



REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
030107	In the *Absolute Maximum Ratings* section, removed the reflow oven temperature value of +220°C. Reference to JEDEC specification for reflow remains.	19
101207	In the *Operation—Alarm Signaling* section, added “or equal to” in the desciption for a TH alarm condition	5
	In the *Memory* section, removed incorrect text describing memory.	7
	In the *Configuration Register* section, removed incorrect text describing configuration register.	8
042208	In the *Ordering Information* table, added TO-92 straight-lead packages and included a note that the TO-92 package in tape and reel can be ordered with either formed or straight leads.	2

修订历史

DATE	DESCRIPTION	PAGES CHANGED
030107	在绝对最大额定值部分，删除了回流炉温度值+220°C。	19
101207	在操作报警信号部分，在第一个报警条件的描述中添加"或等于"	5
	在"内存"部分中，删除了描述内存的不正确文本。	7
	在配置寄存器部分中，删除了描述配置寄存器的不正确文本。	8
042208	在订购信息表中，添加了TO-92直引线封装，并附有一条说明，卷带中的TO-92封装可以使用成型或直引线进行订购。	2

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600