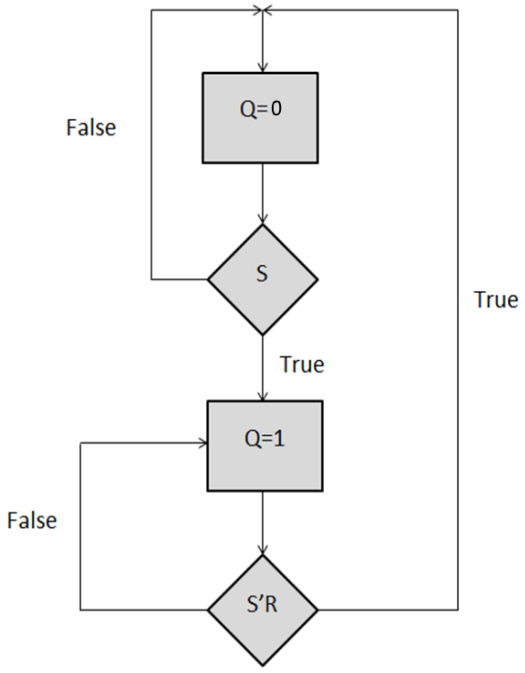
CS1026 – Lab #5 - 16324334

An S-R flip flop, or “latch” is a very simple way of storing volatile memory. This is because when power is taken from the circuit, all memory is lost. An S-R latch takes two inputs, (3 if including the clock), a set input, and a reset input. The set input sets the single bit of memory to 1, the reset changes the bit to 0. S-R latches are nearly always wired to a clock so they only trigger at some times.

Clock	Set	Reset	Q	Q’
0	0	0	Q	Q’
0	0	1	Q	Q’
0	1	0	Q	Q’
0	1	1	Q	Q’
1	0	0	Q	Q’
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0



Note that this S-R latch was designed as a set dominant S-R flip flop, if it wasn’t, the output would be undefined.