CS1026 – Lab #7 - 16324334

To make a divide by 3 clock, a minimum of two J-K flip flops are required. These two serve to count each clock tick in binary until a point at which they are reset again. The following table represents what happens in the circuit:

Flip Flop #1	Flip Flop #2	Z
0	0	1
0	1	1
1	0	0
1	1	X

Note that the two flip flops never reach the final state, as they get reset again at 1,0.

The following table shows the inputs for the J and K parts of the flip flop

Y1/Y2	J1	K1	J2	K2	Z
00	0	0	1	0	1
01	1	0	1	1	1
11	X	X	X	X	X
10	0	1	0	0	0

This table was obtained by using the following rules for J1,J2,K1,K2 and Z

$J1 = Y2$

$K1 = Y1$

$J2 = Y1'$

$K2 = Y2$

$Z = Y1'$

The characteristic table and excitation tables for a JK flip flop shows why these rules were made.

Characteristic table

J	K	Y
0	0	Y
0	1	0
1	0	1
1	1	Y’

Output Excitation Table

Clock	J	K	Change
0	0	0	Y
0	0	1	Y
0	1	0	Y
0	1	1	Y
1	0	0	Y
1	0	1	0
1	1	0	1
1	1	1	Y’

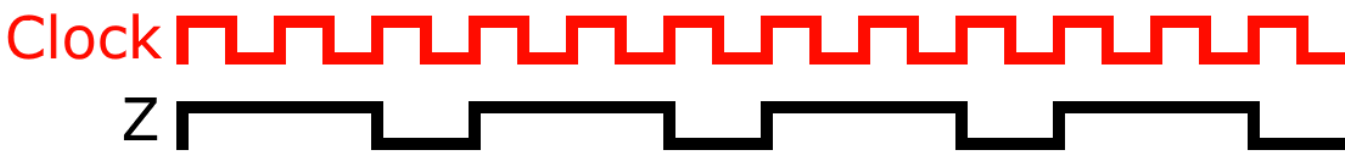
Input Excitation Table

Y	Y’	J	K
0	0	0	-
0	1	1	-
1	0	-	1
1	1	-	0

From these tables it is clear that to change from 00 to 01, only J2 must be activated, then to change from 01 to 10, J1 needs to be on, and J2, K2 toggle the second digit. This could be equally done by just activating K2 but then additional circuitry would have to be implemented.

From 10 to go back to 00, only K1 needs to be toggled.

The result is the following timing diagram:



And the circuit constructed looks like the following, the LED representing the new clock cycle Z: