Release Notes

Traveo II Sample Driver Library

Release Date: May 28, 2021

Thank you for your interest in Cypress Traveo II Sample Driver Library (SDL) version 7.2.0. This document lists the content of release package.

Contents

Cypress provides the Sample Driver Library (SDL) to simplify software development for the Traveo II family of devices. The release provides the following features:

- Drivers for the extensive set of peripherals supported on Traveo II devices
- The ARM Cortex Microcontroller Software Interface Standard (CMSIS) core access header files directly from the CMSIS 5.7.0 release.
- CMSIS complaint device header files, startup code (platform initialization) and device configuration header files
- SDL Application Programming Interface Reference Manual
- Examples to evaluate various peripherals

If you have technical questions, visit www.cypress.com/support for help or contact information.

Releases Details

SDL Release	Description - supported devices
1.0.0	PSVP: TVIIBE1M/a
2.0.0	PSVP: TVIIBE1M/a Silicon: TVIIBE1M/a
2.0.1	PSVP: TVIIBE1M/a Silicon: TVIIBE1M/a, Update and Fixes
3.0.0	PSVP: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a
4.0.0	PSVP: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a
5.0.0	PSVP: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a Silicon: TVIIBH8M/a 176-TEQFP
6.0.0	PSVP: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a Silicon: TVIIBH8M/a 320-BGA, TVIIBE2M/a
6.1.0	PSVP: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a, Silicon: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a 176-TEQFP/320-BGA
6.2.0	PSVP: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, Silicon: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b 176-TEQFP/320-BGA, TVIIC2D6M/a 500-BGA Addition of untested TVIIBH4M/a
6.3.0	PSVP: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8Ma/b, TVIIC2D6M/a, Silicon: TVIIBE1M/b/c, TVIIBE2Ma/b/c, TVIIBH8M/a/b/c 176-TEQFP/320-BGA, TVIIC2D6M/a 500-BGA, TVIIBH4M/a 176-TEQFP/272-BGA Addition of untested TVIIC2D4M/a, TVIIBE1M/d
6.4.0	PSVP: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, TVIIC2D4M/a Silicon: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c 176-TEQFP/320-BGA, TVIIC2D6M/a 327-/500-BGA, TVIIBH4M/a 176-TEQFP/272-BGA Untested: TVIIBH8M/d, TVIIBE4M/a (new device)
6.5.0	PSVP: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, TVIIC2D4M/a Silicon: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a, TVIIBH4M/a/b Untested: TVIIBE512K/d, TVIIBE4M/a (new devices)
6.6.0	PSVP: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, TVIIC2D4M/a Silicon: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a, TVIIBH4M/a/b, TVIIBE512K/a, TVIIBE4M/a, TVIIC2D4M/a
7.0.0	PSVP: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested) Silicon: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a
7.1.0	PSVP: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested) Silicon: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a
7.2.0	PSVP: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) Silicon: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a

Device Support

The SDL includes:

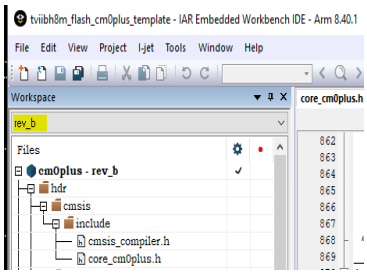
- Device-specific header files that provide a complete definition of all peripheral registers and bits in the device.
- CMSIS-compliant startup code to initialize the system after device reset and transfer the code execution to main().
- Linker files for each supported device and toolchain (IAR/GHS)
- SVD files with a detailed description of peripherals, registers, fields, and bit values.
- GRD files to support register level debugging in GHS
- FreeRTOS support for all devices (Tested only on TVIIBE2M and TVIIC2D4M devices)

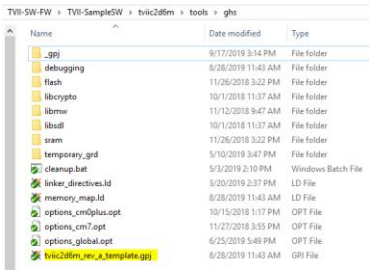
Table 1 Device RTL and MPN Revision Mapping

Device	Device RTL Revision	Datasheet MPN/SDL Revision
TVIIBE1M	A0	A
	B0	B
	B1	C
	B2	D
TVIIBE2M	A0	A
	A1	B
	A2	C
TVIIBH8M	A0	A
	B0	B
	B1	C
	B2	D
TVIIC2D6M	A0	A
	B0	B
TVIIBH4M	A0	A
	A1	B
TVIIC2D4M	A0	A
TVIIBE4M	A0	A
TVIIBE512K	B2	D
TVIIC2D6MDDR	A0	A
TVIICE4M	A0	A

Project configuration,

1. Choose proper build and then perform the compilation in IAR. In case of GHS, device revision is part of the main prject file.





2. **TVIIBE1M: Rev_B, Rev_C, Rev_D**
   a. PSVP 176-LQFP: CY_USE_PSVP=1 and either CYT2B78XAX (176-LQFP package fixed for PSVP and no other package supported)
   b. Silicon 176-LQFP: CY_USE_PSVP=0 and either CYT2B78XAX
   c. Supports both REV *A and REV *C CPU boards through the selection of CPU_BOARD_REVA or CPU_BOARD_REVC respectively
   d. Rev_D has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
3. **TVIIBE2M: Rev_A, Rev_B, Rev_C**
   a. PSVP : CY_USE_PSVP=1 and either CYT2B98XAX (176-LQFP package fixed for PSVP and no other package supported)
   b. Silicon 176-LQFP: CY_USE_PSVP=0 and either CYT2B98XAX
   c. Supports both REV *A and REV *C CPU boards through the selection of CPU_BOARD_REVA or CPU_BOARD_REVC respectively
   d. Rev_C has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
4. **TVIIBH8M: Rev_B, Rev_C, Rev_D**
   a. Defines CY_CORE_CM7_0 or CY_CORE_CM7_1 for either core CM7_0 or CM7_1 selection
   b. PSVP 320-BGA: CY_USE_PSVP=1 and either CYT4BFCCXX (320-BGA package fixed for PSVP and no other package supported)
   c. Silicon 320-BGA: CY_USE_PSVP=0 and either CYT4BFCCXX

      (IAR linker "use_psvp = 0" in its ICF file, GHS relies on global definition CY_USE_PSVP=0)
   d. Silicon 176-TEQFP: CY_USE_PSVP=0 and either CYT4BF8CXX / CYT4A0100S

      (IAR linker "use_psvp = 0" in its ICF file, GHS relies on global definition CY_USE_PSVP=0)
   e. Rev_C onwards has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
   f. Rev_A support is removed
5. **TVIIC2D6M: Rev_A/Rev_B**
   a. PSVP: CY_USE_PSVP=1 and tviic2d6m, CYT4DNDBHS

      (Rev_B only in PSVP, SMIF/ETH/LIN modules have not been tested due to limitations in the bitfile)

b. Silicon 327-BGA: CY_USE_PSVP=0 and tviic2d6m, CYT4DNJBHS

(IAR linker "use_psvp = 0" in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

c. Silicon 500-BGA: CY_USE_PSVP=0 and tviic2d6m, CYT4DNDBHS

(IAR linker "use_psvp = 0" in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

d. Defines CY_CORE_CM7_0 or CY_CORE_CM7_1 for either core CM7_0 or CM7_1 selection

e. Rev_B has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved

f. Rev_B, 500-BGA support removed. Only 327-BGA devices are supported.

6. TVIIBH4M: Rev_A, Rev_B

a. Defines CY_CORE_CM7_0 or CY_CORE_CM7_1 for either core CM7_0 or CM7_1 selection

b. Silicon 272-BGA: CY_USE_PSVP=0 and either CYT4BBBCEX

(IAR linker "use_psvp = 0" in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

c. Silicon 176-TEQFP: CY_USE_PSVP=0 and either CYT4BB8CEX

(IAR linker "use_psvp = 0" in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

d. Rev_A has initial 2KB of SRAM reserved for internal purposes

e. CYT3BB support added

7. TVIIC2D4M: Rev_A

a. PSVP: CY_USE_PSVP=1 and tviic2d4m, CYT3DLBBHS.

b. Silicon 216-TEQFP: CY_USE_PSVP=0 and CYT3DLABAS / CYT3DLABBS / CYT3DLABCS / CYT3DLABDS / CYT3DLABES / CYT3DLABFS / CYT3DLABGS / CYT3DLABHS

(IAR linker "use_psvp = 0" in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

c. Rev_A has initial 2KB of SRAM reserved for internal purposes

8. TVIIBE4M: Rev_A

a. Silicon: 176-LQFP: CY_USE_PSVP=0 and either CYT2BL8XAX / CYT2BL7XAX / CYT2BL5XAX / CYT2BL4XAX / CYT2BL3XAX

b. Rev_A has initial 2KB of SRAM reserved for internal purposes

9. TVIIBE512K: Rev_D

a. Silicon: 100-LQFP: CY_USE_PSVP=0 and either CYT2B65BAS / CYT2B65BAE / CYT2B65CAS / CYT2B65CAE

b. Rev_D has initial 2KB of SRAM reserved for internal purposes

10. TVIIC2D6MDDR: Rev_A

a. PSVP: CY_USE_PSVP=1 and tviic2d6mddr, TVIIC2D6MDDR.

b. Rev_A has initial 2KB of SRAM reserved for internal purposes

11. TVIICE4M: Rev_A

c. PSVP: CY_USE_PSVP=1 and tviice4m, CYT2CL8BAS. (For IAR, from the device selection perspective it is still looking at CYT2BL since the flash patches are not available yet)

d. Rev_A has initial 2KB of SRAM reserved for internal purposes

Note:

- 'X' in the device MPN above signifies different package variants or temperatures supported. Please check the device specific datasheet for more details.
- In all devices, last 6kB of SRAM cannot be used for retention.

Table 2 Device Memory Map

Device	Type	Brief Device Description
TVIIBE1M	PSVP	Dual core CM0+/CM4, Flash 1088-KB, SRAM 128-KB, Work flash 96-KB
	176-LQFP	Dual core CM0+/CM4, Flash 1088-KB, SRAM 128-KB, Work flash 96-KB
TVIIBE2M	PSVP	Dual core CM0+/CM4, Flash 2112-KB, SRAM 256-KB, Work flash 128-KB
	176-LQFP	Dual core CM0+/CM4, Flash 2112-KB, SRAM 256-KB, Work flash 128-KB
TVIIBH8M	PSVP	Triple core CM0+/CM7_0/CM7_1, Flash 2048-KB, SRAM 1024-KB, Work flash 256-KB
	320-BGA 176-TEQFP	Triple core CM0+/CM7_0/CM7_1, Flash 8384-KB, SRAM 1024-KB, Work flash 256-KB
TVIIC2D6M	PSVP	Triple core CM0+/CM7_0/CM7_1, Flash 1024-KB, SRAM 1024-KB, Work flash 128-KB
	327-BGA 500-BGA	Triple core CM0+/CM7_0/CM7_1, Flash 6336-KB, SRAM 640-KB, Work flash 128-KB
TVIIBH4M	176-TEQFP 272-BGA	Triple core CM0+/CM7_0/CM7_1, Flash 4160-KB, SRAM 768-KB, Work flash 256-KB
TVIIC2D4M	216-TEQFP	Dual core CM0+/CM7_0, Flash 4160-KB, SRAM 384-KB, Work flash 128-KB
TVIIBE4M	176-LQFP	Dual core CM0+/CM4, Flash 4160-KB, SRAM 512-KB, Work flash 128-KB
TVIIBE512K	100-LQFP	Dual core CM0+/CM4, Flash 576-KB, SRAM 64-KB, Work flash 64-KB
TVIIC2D6MDDR	PSVP	Triple core CM0+/CM7_0/CM7_1, Flash 1024-KB, SRAM 1024-KB, Work flash 128-KB
TVIICE4M	PSVP	Dual core CM0+/CM4, Flash 1024-KB (Split), SRAM 512-KB, Work flash 128-KB

Supported Toolchains

- Green Hills MULTI: 7.1.4, Compiler: 2017.1.4, Probe Version: 5.6.5
    - *DEVELOPMENT AUTOBUILD 5.6 634260/AB as of patch #12996, or higher*
    - *Flash loaders are not available as part of SDL, will be provided on case by case basis through Cypress Customer Support (also the patches are in GBs, SDL becomes bulky)*
- IAR Embedded Workbench for ARM 8.42.1 (EWARM-CD-8421-xxxxx.exe), IAR I-Jet Debugger
    - *Flash loaders are available at the location*
        - *"\|misc\|tools\|iar\| IAR_EWARM_8421_FlashLoader_Patch_TraveoII"*
    - *Request to go through "\|misc\|tools\|iar\|Readme_Patch.txt" to update the Traveo II patch for IAR.*
- IAR Embedded Workbench for ARM 8.22.1 (EWARM-CD-8221-xxxxx.exe), IAR I-Jet Debugger
    - *Supported only for tviic2d4m and tviic2d6m devices for flash projects*
    - *This EWARM revision is functional safety complaint*
    - *Flash loaders are available at the location*
        - *"\|misc\|tools\|iar\| IAR_EWARM_8222_FlashLoader_Patch_TraveoII"*

Peripheral Drivers

The SDL provides a high-level API to configure, initialize, and use a peripheral driver. The drivers are designed for peripheral IP blocks, therefore work on all Traveo II products that instantiate that IP block.

Following driver (src/driver) modules have been tested and the respective examples are available in the src/examples folder. Some of these drivers/mw are available in the common/src/drivers or common/src/mw which are common across dies, and some are specific to a particular die is available in the die specific drivers/mw say, tviibh8m/src/drivers or tviibh8m/src/mw.

Table 3: Drivers

Driver	Description	API Functionality
ADC	Analog to Digital Converter	Manage ADC operations
Audioss	Sound Subsystem for I^2S, DAC, Mixer, PWM, SG, TDM (TVIIC devices only)	Manages I2S, Audio DAC, Mixer, PCM-PWM, Sound Generator, TDM as part of sound subsystem
AXIDMA	M-DMA on AXI bus	Memory to memory transfer over AXI bus
CAN FD	Controller Area Network Flexible Data-Rate	Manages Classic and FD operations
CPU	CPU driver	Enables core of CPU specific features
CRYPTO	Cryptographic Operations	Perform cryptographic operations on user-designated data. Available as libraries.
CXPI	Clock eXtension Peripheral Interface	Manages communication over CXPI interface
DAC	Audio DAC	Provides global DAC defines and API function definitions
DMA	Direct Access Memory (AHB bus)	Perform memory-to-memory (M-DMA) and peripheral-to-memory (P-DMA) (and vice versa) operations
ETHERNET	Ethernet	Basic ethernet driver supporting automotive and gigabit ethernet PHYs.
EVTGEN	Event Generator	Performs event generation for interrupts and triggers in active power mode
FLASH	Flash Memory	Manage code/work flash memory operations
FLEXRAY	FlexRAY Interface	Manages FlexRAY communication
FPDLINK	FDP-Link or LVDS	Analog LVDS video driver
GPIO	General Purpose I/O Ports	Configure and access device input/output pins
GFX_ENV	Graphics Environment Setup	Sets up the Graphics environment
I^2S	Inter-IC Sound (TVIIBH8M all revisions and TVIIC2D6M rev_a Only)	Manage Inter-IC Sound. I2S is used to send digital audio streaming data to external I2S devices, such as audio codecs or simple DACs. It can also receive digital audio streaming data.
IPC	Inter Process Communication	Manage data transfer between CPUs or processes in a device
LIN	Local Interconnect Network	Provides master and slave data transfer capabilities
LVD	Low Volatge Detection	Provides LVD capabilities
LPDDR	Low-Power DDR SDRAM	Provides basic capabilities to access DDR memories
MCWDT	Multi-counter Watchdog timer	Provides control and status capabilities
MIPICSI2	Video Input	Manage and control analog video inputs
Mixer	Audio Mixer for I2S, PWM etc.	Provides global Mixer defines and API function definitions
MPU	Mempry Protection Unit	Manages the configuration of MPU
PROT	Memory and Peripheral Protection	Manage the MPU, Shared MPU (SMPU), and Peripheral Protection Unit (PPU)
PWM	Audio Pulse Width Modulation	PWM interface drives PWM output lines and their complementary output lines.
SCB	Serial Communication Block	Manage serial communication as EZI2C, I2C, SPI, or UART
SEGLCD	Segment LCD	Manage Segment LCD interfaces
SD_HOST	Secude Digital Host Controller	Manages SD and eMMC devices
SG	Audio Sound Generator	Helps produce PWM tone (frequency) and amplitude (volume) signals
SMART IO	Smart I/O	Configure and access the Smart I/O hardware present between the GPIOs (pins) and HSIOMs (pin muxes) on select device ports. It can be used to perform simple logic operations on peripheral and GPIO signals at the GPIO port

SMIF	Serial Memory Interface	SPI-based communication interface for interfacing external memory devices to TVII. The SMIF supports Octal-SPI, Dual Quad-SPI, Quad-SPI, DSPI, and SPI. This interface also supports Hyper Bus interfaces like HyperRAM and HyperFlash devices.
SROM	Internal SROM driver	APIs to support some basic access to SROM System calls
SYSCLK	System Clock	Provides APIs to control and read status of various clocking capabilities of the device
SYSFLT	System Fault	Controls CPUs fault processing Subsystem
SYSINT	System Interrupt	Manage interrupts and exceptions, in conjunction with the CMSIS core NVIC API
SYSLIB	System Library	Utility functions to handle delays, register read/write, asserts, silicon unique ID, and more
SYSPM	System Power Modes	Controls device power modes
SYSREGHC/ SYSPMIC	REGHC/PMIC Control and Status	Controls High Current Regulator or the PMIC module
SYSRESET	System Reset	Provides APIs for reading reset reason and clearing them
SYSRTC	System Real Time Clock	Provides capabilities to handle RTC, Alarms etc.
SYSTICK	Systick Timer	Manage a 24-bit down-counter timer
SYSWDT	Free running Watchdog timer	Provides control and status capabilities
TDM	Audio Time-division multiplexing	TDM transmitter and a TDM receiver, I2S support also included in latest revisions.
TCPWM	Timer Counter PWM	Manage a 16- or 32-bit periodic Counter, PWM, Quadrature decoder, Shift register
TRIGMUX	Trigger Multiplxer	Manage the multiplexing of trigger outputs to specific trigger inputs across multiple peripherals

Table 4: Device Specific Middleware

Middleware	Description	API Functionality
GFX_ENV	Graphics Environment Setup	Supported only for TVIIC2D6M/TVIIC2D4M (Graphics environment setup support)
MIPI_SENSOR	MIPI CSI2 controller	Support top level MIPI CSI2 APIs for camera access map to capture interface of VIDEOSS IP
POWER	Reghc or PMIC based power control	REGHC or PMIC controller middleware (REGHC/TVIIBH4M/TVIIBH8M, PMIC/TVIIC2D6M/TVIIC2D4M)
SMIF_MEM	SMIF SPI/Hyper Access Control	SPI or HyperBus specific device support

Table 5: Common Middleware

Middleware	Description	API Functionality
Button	Button middle layer	APIs to support buttons
Semihosting	SCB/UART middle layer	Support top level UART APIs for debugging
SW_Timer	Software Timer	Enables multiple software timers
Flash	Code and work flash	User level APIs for ease of use
AIC261	Audio Codec	Provides APIs for audio codec (ADC/DAC) TI aic 261

Release Contents

The SDL is organized into several folders. The following table shows the SDL folder structure.

Table 6: SDL Folder Structure

Path/Folder	Description
common/hdr/cmsis	CMSIS core access headers
common/src/drivers	Drivers common across all the devices
common/src/mw	Middleware common across all the devices
Common/src/rtos	FreeRTOS support for application cores
common/src/startup	Tool specific startup code for all the devices
docs	SDL API Documentation
misc/tools	GHS/IAR specific flash loaders
tviibe512k/tviibe1m/tviibe2m/tviibe4m/tviice4m	
hdr	Device specific header files, BSP for TV II Base Board, GPIO assignments
hdr/ip	Device IP specific headers
hdr/mcureg	IP Specific Register Addresses
src/drivers	Driver source and respective headers specific to the device
src/examples	Code examples in accordance to the device
src/system	Device's system specific code and system header for clock configurations
src/main_cm0plus.c	Sample main source file for CM0+ core
src/cy_interrupt_map_cm0plus.h	User interrupt mapping file used in case "CY_LINK_SYSTEM_IRQ_TABLE_TO_RAM" not defined
src/main_cm4.c	Sample main source file for CM4 core
src/cy_interrupt_map_cm4.h	User interrupt mapping file used in case "CY_LINK_SYSTEM_IRQ_TABLE_TO_RAM" not defined
tools/ghs	GHS MULTI workspaces for SRAM/Flash for CM0+/CM4 cores, linker specific files, CMSIS SVD files, GRD files
tools/iar	IAR workspaces for SRAM/Flash for CM0+/CM4 cores, linker specific files, CMSIS SVD files
tviibh4m/tviibh8m/tviic2d4m/tviic2d6m/tviic2d6mddr	
hdr	Device specific header files, BSP for TV II Base Board, GPIO assignments
hdr/ip	Device IP specific headers
hdr/mcureg	IP Specific Register Addresses
src/drivers	Driver source and respective headers specific to the device
src/mw/	Middleware support
src/examples	Code examples in accordance device specific
src/system	Device system specific code and system header for clock configurations
src/main_cm0plus.c	Sample main source file for CM0+ core
src/cy_interrupt_map_cm0plus.h	User interrupt mapping file used in case "CY_LINK_SYSTEM_IRQ_TABLE_TO_RAM" not defined
src/main_cm7_0.c	Sample main source file for CM7_0 core
src/cy_interrupt_map_cm7_0.h	User interrupt mapping file used in case "CY_LINK_SYSTEM_IRQ_TABLE_TO_RAM" not defined
src/main_cm7_1.c	Sample main source file for CM7_0 core
src/cy_interrupt_map_cm7_1.h	User interrupt mapping file used in case "CY_LINK_SYSTEM_IRQ_TABLE_TO_RAM" not defined
tools/ghs	GHS MULTI workspaces for SRAM/Flash for CM0+/CM7_0/CM7_1 cores, linker specific files, CMSIS SVD files, GRD files
tools/iar	IAR workspaces for SRAM/Flash for CM0+/CM7_0/CM7_1 cores, linker specific files, CMSIS SVD files

Documentation

SDL API Reference Manual are located in the \docs subdirectory of the SDL installation directory.

Note:

1. ***Application address mapping,***
   a. *TVIIBE1M/TVIIBE2M/TVIIBE4M/TVIIBE512K: In the header "system_cyt2b7.h" / "system_cyt2b9.h" / "system_cyt2bl.h" / "system_cyt2b6.h" macro "CY_CORTEX_M4_APPL_ADDR" needs to be updated to CM4 start address as per the linker config file, it is picked by the respective tool chain automatically*
   b. *TVIIBH4M/TVIIBH8M/TVIIC2D4M/TVIIC2D6M: In the header "system_cyt4bf.h" / "system_cyt4bb.h" / "system_tviic2d6m.h" macro "CY_CORTEX_M7_0_APPL_ADDR" and "CY_CORTEX_M7_1_APPL_ADDR" needs to be updated to CM7_0/CM7_1 start address as per the linker config file, it is picked by the respective tool chain automatically*
   c. *TVIIC2D4M: In the header "system_cyt3dl.h" macro "CY_CORTEX_M7_0_APPL_ADDR" needs to be updated to CM7_0 start address as per the linker config file, it is picked by the respective tool chain automatically*
2. ***Clock Configuration***

Table 7: PSVP Clocks Configuration

Sl. No.	Device (PSVP)	Clock	Clock Frequency
2	TVIIBE1M, TVIIBE2M	CM0+/CM4	24 MHz
3	TVIIBH8M, TVIIC2D6M, TVIIC2D4M	CM0+/CM7_x	24 MHz
4	TVIIC2D6M, TVIIC2D4M, TVIIC2D6MDDR	IMO	8 MHz
5	TVIIBE1M, TVIIBE2M	ILO	32.9 KHz
6	TVIIBH8M, TVIIC2D6M, TVIIC2D4M, TVIIC2D6MDDR	ILO	12.8 KHz
7	TVIIC2D6MDDR	CM0+/CM7_x	26.6 MHz
8		LPDDR	80 MHz
9	TVIICE4M	CM0+/CM4	24 MHz
		IMO/ILO	8MHz/12.8kHz

Table 8: Silicon Clocks Configuration

Sl. No.	Device (Silicon)	Clock	Clock Frequency
1	TVIIBH8M/b/c/d 320-BGA, 176-TEQFP TVIIBH4M/a/b 176-TEQFP, 272-BGA	CM0+	80 MHz
		CM7_0, CM7_1	250/350 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 KHz
2	TVIIBE2M/a/b 176-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 KHz
3	TVIIBE1M/b/c/d 176-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 KHz
4	TVIIC2D6M/a/b 327-/500-BGA	CM0+	80 MHz
		CM7_0, CM7_1	320 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 KHz
5	TVIIC2D4M/a 216-TEQFP	CM0+	80 MHz
		CM7_0	240 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 KHz

6	TVIIBE512K/d 100-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 KHz

3. ***CM0+ samples shall not use IRQs 0/1 (CPUIntIdx0_IRQn/ CPUIntIdx1_IRQn), as they are internally used by the SROM System calls. This can be seen as part of the examples for reference. It would cause hard fault, if used.***
4. ***Interrupt usage:***
   All the examples are modified to use the IRQ table in SRAM and thereby relives from maintaining core specific interrupt map headers (example: cy_interrupt_map_cm7_0.h)
   For IRQs part of SRAM
   a. *No need to update core specific interrupt map headers for any IP specific ISRs, instead update respective example as below (default interrupt map headers at src level will be used as is without any modifications)*
   b. *Cy_SysInt_SetSystemIrqVector(irq_cfg.sysIntSrc, ButtonIntHandler); // typical use case example*
   For IRQs part of flash region
   a. *Users will still need to update the core specific interrupt map header against the IP which is being tested and remove the below define from the respective header,*
   #define CY_LINK_SYSTEM_IRQ_TABLE_TO_RAM

Table 9: Device to SMIF revision mapping

Device	Device Revision	SMIF Revision
TVIIBH4M/TVIIBH8M	All	v2
TVIIC2D4M	Rev_A	v3.1
TVIIC2D6M	Rev_A	v3.0
TVIIC2D6M	Rev_B	v4.0
TVIIC2D6MDDR	Rev_A	v4.0
TVIICE4M	Rev_A	v3.1

Change Log from v7.1.0 to v7.2.0

Sl. No.	Change	Files	Action
1	SDL FOSS package report added (Only Arm CMSIS modified files are listed)	docs/	Addition
2	All system sources and headers, startup assembly files. - Arm license details removed. - These can be adapted and will be local to where used.	NA	Modified
3	Device addition tviice4m, flash patch is not yet updated	TVII-SampleSW/tviice4m	Addition
4	initialization of local variable (smif context of "Cy_SMIF_SEMP_EnableHyperBusInterface").	TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.c	Modified
5	Doxygen fixes	TVII-SampleSW/common/src/drivers/flash TVII-SampleSW/common/src/drivers/sysrtc TVII-SampleSW/common/src/drivers/trigmux	Modified
6	Change GHS DEVICE define to CYT4DNJBRS ('R' marketing option)	TVII-SampleSW/tviic2d6m/tools/ghs/tviic2d6m_common.gpj	Modified
7	Removed CY_LED_TOGGLE_DELAY definition and usage	TVII-SampleSW/common/hdr/cy_project.h	Removed
8	. added the Quality of Service Registers to the lpddr4 config structure . change for Mode Register read when controller is running. The command must be send subsequentially to the controller as the controller can not handle the MRR reuqest to both channels when controller is running. . fixed issue which was present when reading DQS Oscillator sometimes catch old value triggering a retrain request. some correction for the release done this morning moved the static fuction to *.c added the inline function with extern inline to the *.c file to avoid compile error with IAR	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/	Modified
9	LPDDR4 update for compilation	TVII-SampleSW/tviic2d6mddr/tools/ghs/_gpj/libsdl_source.gpj	Addition
10	Adding special label __iar_init$$done to vector table definition in startup assembly files.	TVII-SampleSW/common/src/startup/iar/	Modified
11	improve interface of capture mode setting APIs more functional name for enum of ddr capture mode.	TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.c TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.h	Modified
12	update smif example/mw. S28H mode detecting function improved	TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.h	Modified
13	passTr setting: not use API (synchronize with rev_c)	TVII-SampleSW/tviibh8m/src/system/rev_d/system_tviibh8m_cm0plus.c	Modified
14	Enabling IRQ before SystemInit	All main sources of every device Example: TVII-SampleSW/tviibh4m/src/main_cm0plus.c TVII-SampleSW/tviibh4m/src/main_cm7_0.c TVII-SampleSW/tviibh4m/src/main_cm7_1.c	Modified
15	The parameters for "ConfigureRegulator" has been updated to the latest version.	TVII-SampleSW/common/src/drivers/srom/cy_srom.h TVII-SampleSW/tviibh8m/src/mw/power/cy_power.c	Modified
16	MPU driver defect: "execute" config value was not used in Cy_MPU_Setup	TVII-SampleSW/common/src/drivers/mpu/cy_mpu.c	Modified

Change Log from v7.0.0 to v7.1.0

Sl. No.	Change	Files	Action
1	AUTO ETH added	Traveo-II/TVII-SW-FW/TVII-SampleSW/tviic2d6m/hdr/rev_b/bb_bsp_tviic2d6m.h	Modified
2	Added ul for integer in Cy_Tcpwm_Pwm_Init	TVII-SampleSW/common/src/drivers/tcpwm/cy_tcpwm_pwm.c	Modified
3	add a reading product index API	TVII-SampleSW/tviibe1m/src/drivers/cpu/cy_cpu.c TVII-SampleSW/tviibe1m/src/drivers/cpu/cy_cpu.h	Addition
4	add path input selection "CY_SYSCLK_CLKPATH_IN_LPECO" only when it is available.	TVII-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.h TVII-SampleSW/tviibe4m/src/drivers/sysclk/cy_sysclk.h TVII-SampleSW/tviibe512k/src/drivers/sysclk/cy_sysclk.h TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h	Addition
5	LPECO Clock source option added	TVII-SampleSW/common/src/drivers/sysrtc/cy_sysrtc.h	Addition
6	add WCO Enabling option to system files	All device and their revision system headers	Addition
7	Added LPECO definition and API's for CTL, PRESCALAR, STATUS registers in BACKUP domain.	TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h	Addition
8	. deleted function cy_en_lpddr4_retval_t Cy_Lpddr_ChangeFrequencySetPoint . added function to trigger the DQS2DQ retraining cy_en_lpddr4_retval_t Cy_Lpddr_RequestDQS2DQRetrain . added a function to read LPDDR4 Mode Registers cy_en_lpddr4_retval_t Cy_Lpddr_ReadModeRegister . added function to start the DQS Oscillator which is needed to detect retraining necessity cy_en_lpddr4_retval_t Cy_Lpddr_StartDQSOscillator	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Modified
9	SMIF Documentation fixed	TVII-SampleSW/common/src/drivers/smif/common/cy_smif.h TVII-SampleSW/common/src/drivers/smif/common/cy_smif_memslot.h TVII-SampleSW/common/src/drivers/smif/ver2/cy_smif_ver_specific.h TVII-SampleSW/common/src/drivers/smif/ver3_0/cy_smif_ver_specific.h TVII-SampleSW/common/src/drivers/smif/ver3_1/cy_smif_ver_specific.h TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.h	Modified
10	Faults updated	TVII-SampleSW/tviic2d6mddr/src/drivers/sysflt/cy_sysflt_config.h TVII-SampleSW/tviic2d6m/src/drivers/sysflt/cy_sysflt_config.h	Modified
11	FreeRTOS, CMSIS licenses added	TVII-SampleSW/common/hdr/cmsis/LICENSE.txt TVII-SampleSW/common/src/rtos/license.txt	Addition
12	Added temporary capture configuration function to adapt changes for ip version v4 on PSVP	TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.c TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.h	Modified

13	. moved the initialization of the BISTCFG Registers to Cy_Lpddr_SetupBISTRegister . deleted Cy_Lpddr_ChangeFrequencySetPoint which is no longer needed . commented out timeout time in Cy_Lpddr_WaitUserCMDReady() . Cy_Lpddr_RequestDQS2DQRetrain() added a check of the PTSR2 /3 register id retraining ended without error . changed tRFC Refresh cycle all banks to 280ns --> 180 ns as per datasheet . disabled postpone refresg feature DMCFG .u1REF_POST_PULL_EN = CY_LPDDR4_DISABLED . added some documentation . added CIOR_CHO/CH1 registers in the lpddr4_config these regs are used to set the Command/Address Phy IO driver settings . corrected editor TAB settings . changed some timing seetings to defines from cy_lddr4.h u10T_XSR added JESD209_4B_NS_TXSR,JESD209_4B_NCLK_TXSR, u7T_INIT5 u9T_CAENT u9T_FC u9T_VREFTIMELONG	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Modified
14	Updated the structure and function used for the temperature sensor measurements.	TVII-SampleSW/common/src/drivers/adc/cy_adc.c TVII-SampleSW/common/src/drivers/adc/cy_adc.h	Modified
15	CMSIS 5.7.0: 1. Instruction barrier macros updated 2. Arm architecture 8.1M support added 3. Consistency in using data and return types 4. Addition and fixes for some instructions 5. New APIs for NVIC features for priority encoding, decoding 6. Corrections in some APIs (Set and Get Vectors) 7. Corrections in ITM/ETM Data register definitions 8. Addition of registers for FPU 9. ITM Registers updated for CM7 10. Refactored vector table references for all Cortex-M devices	TVII-SampleSW/common/hdr/cmsis/include	Modified
16	move local var definitions to avoid compiler warnings in PSVP case	TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c	Modified
17	Harmonize i2s driver folder names across devices to prevent confusion Only i2s is used for rev_b I2S handling: - i2s is common across c2d4m a0, c2d6m b0 and c2d6mddr a0 - i2s_rev_a is obviously specific to c2d6m a0	/TVII-SampleSW/tviic2d6m/src/drivers/audioss /TVII-SampleSW/tviic2d6m/src/drivers/audioss/i2s /TVII-SampleSW/tviic2d6m/src/drivers/audioss/i2s_rev_a	Modified
18	removed VRAM, added LPDDR4, moved CM7_x_[I|D]TCM and SMIF1 regions	TVII-SampleSW/tviic2d6mddr/tools/iar/linker_directives_tviic2d6mddr.icf	Modified
19	Fixed PSVP clocks for tviic2d6mddr, fixed usage of hardcoded PSVP frequency value in sysclk driver	TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.c TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr.h	Modified
20	Corrects the BSP definition under PSVP: 1. Audio SCB slave select pin, 2. TCPWM counters definition for SMART IO block	TVII-SampleSW/tviibh8m/hdr/rev_d/bb_bsp_tviibh8m.h TVII-SampleSW/tviibh4m/hdr/rev_a/bb_bsp_tviibh4m_reva.h TVII-SampleSW/tviibh4m/hdr/rev_a/bb_bsp_tviibh4m_revb.h TVII-SampleSW/tviibh4m/hdr/rev_b/bb_bsp_tviibh4m_reva.h TVII-SampleSW/tviibh4m/hdr/rev_b/bb_bsp_tviibh4m_revb.h	Modified
21	Updates the BSP macro definition for SMART IO for PSVP. Adds macro definition for TCPWM counter for SMART IO.	TVII-SampleSW/tviic2d6m/hdr/rev_a/bb_bsp_tviic2d6m.h TVII-SampleSW/tviic2d6m/hdr/rev_b/bb_bsp_tviic2d6m.h	Modified

22	Fixed temperature measurement state machine code for one of the corner case.	TVII-SampleSW/common/src/drivers/adc/cy_adc.c	Modified
23	added Cy_Lpddr_SetupCAIOCntrlRegs in the CY_Lpddr_ControllerInit() init sequence to setup the Command /Address IO Controll registers. - addd the Cy_pddr_WarmStartRefreshAdjust() to the Cy_Lpddr_ControllerInit() init sequence to check if the memory is already in a temperature range where TREFI needs adjustment or maybe also AC timing derating is needed - deleted the checking of the INTSTT_CH0/CH1 register in Cy_LPDDR_SendCmd. As the faultstructure/faulthandler is working now this additional test is no longer need as we would recognize possible problems by jumping to the faulthandler - new function Cy_Lpddr_PerformTimingDerating handling temperature related timing deration - new function Cy_Lpddr_RefreshandTimingAdjust which reads the MR4 DRAM register and is adjusting Refreshrate tREFI(TREG5) and also calling the Cy_Lpddr_PerformTimingDerating to adjust´temperature depending timingRegister5	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Modified
24	. HIB Support for 10 pins updated. SIMO Buck related stuffs removed from compilation.	TVII-SampleSW/common/src/drivers/syspm/cy_syspm.c TVII-SampleSW/common/src/drivers/syspm/cy_syspm.h	Modified
25	some macros needed for SEGLCD driver.	TVII-SampleSW/common/src/drivers/syslib/cy_syslib.h	Addition
26	WCO is not available for SK and hence that portion of code is not needed to be executed.	TVII-SampleSW/tviibe1m/src/system/rev_d/system_cyt2b7.h TVII-SampleSW/tviibe2m/src/system/rev_c/system_cyt2b9.h	Modified
27	Updated the QSPI memory device definition to "CY_SMIF_S25FXXXS" for soldered board.	/TVII-SampleSW/tviic2d4m/hdr/rev_a/bb_bsp_tviic2d4m.h	Modified
28	Updates the Button IRQ macro and SW reference as per the CPU board.	TVII-SampleSW/tviic2d6m/hdr/rev_b/bb_bsp_tviic2d6m.h	Modified
29	CM0+ SystemInit now takes care of globally enabling VIDEOSS IP (and power if applicable), so that VRAM is available already during CM7 startup. GfxEnv_EnableTestImage adapted accordingly	TVII-SampleSW/tviic2d4m/src/system/rev_a/system_tviic2d4m_cm0plus.c TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c TVII-SampleSW/tviic2d6m/src/system/rev_a/system_tviic2d6m_cm0plus.c TVII-SampleSW/tviic2d6m/src/system/rev_b/system_tviic2d6m_cm0plus.c	Modified
30	Cy_Tcpwm_ClearInterrupt doesn't have the code to readback the register after writing ptscTCPWM->unINTR.u32Register. Additional fix for SetInterrupt API to look at correct register.	TVII-SampleSW/common/src/drivers/tcpwm/cy_tcpwm.c	Modified
31	Replaced the defined delay with status check: -> Poll until read bit is set from Cy_Rtc_SyncRegisters() -> Wait until busy bit is cleared from Cy_Rtc_WriteEnable()	TVII-SampleSW/common/src/drivers/sysrtc/cy_sysrtc.c	Modified
32	IAR Patch updated	TVII-SampleSW/misc/tools/iar/IAR_EWARM_8421_FlashLoader_Patch_TraveoII.7z	Addition

Change Log from v6.6.0 to v7.0.0

Sl. No.	Change	Files	Action
1	Added SRAM-ECC example.	TVII-SampleSW/tviic2d6m/src/examples/sram TVII-SampleSW/tviic2d6m/src/examples/sram/ecc TVII-SampleSW/tviic2d6m/src/examples/sram/ecc/main_cm0plus.c TVII-SampleSW/tviic2d4m/src/examples/sram TVII-SampleSW/tviic2d4m/src/examples/sram/ecc TVII-SampleSW/tviic2d4m/src/examples/sram/ecc/main_cm0plus.c	Added
2	New driver addition	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Added
3	tvii_debug.py now clears some control bits in DHCSR before triggering reset to prevent a potential debugger issue GHS tvii_debug.py now prints a solution hint for updating ODB file if flashing results in "Could not detect flash device"	TVII-SampleSW/tviibe1m/tools/ghs/debugging/tvii_debug.py TVII-SampleSW/tviibe2m/tools/ghs/debugging/tvii_debug.py TVII-SampleSW/tviibe4m/tools/ghs/debugging/tvii_debug.py TVII-SampleSW/tviibe512k/tools/ghs/debugging/tvii_debug.py TVII-SampleSW/tviibh4m/tools/ghs/debugging/tvii_debug.py TVII-SampleSW/tviibh8m/tools/ghs/debugging/tvii_debug.py TVII-SampleSW/tviic2d4m/tools/ghs/debugging/tvii_debug.py TVII-SampleSW/tviic2d6m/tools/ghs/debugging/tvii_debug.py TVII-SampleSW/tviic2d6mddr/tools/ghs/debugging/tvii_debug.py	Modified
4	Added pin definition for CXPI channel in PSVP. Updated the CAN channel 0 and 1 macro supported by C2D6M-B0-PSVP.	TVII-SampleSW/tviic2d6m/hdr/rev_b/bb_bsp_tviic2d6m.h	Added
5	Device headers for rev_b added	TVII-SampleSW/tviic2d6m/hdr/rev_b	Added
6	This is a driver from c2d4m and tdm v2.0.	TVII-SampleSW/tviic2d6m/src/drivers/audioss/i2s_v2	Added
7	smif rev and i2s for 6m b0 changed	TVII-SampleSW/common/hdr/cy_project.h Workspaces adapted accordingly	Modified
8	change inclusion of some drivers based on MCU revision, update SMIF instance calculation because of different define meaning due to SMIF4.0, comment more code to prevent warnings	TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif.h TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.h TVII-SampleSW/tviic2d6m/tools/ghs/_gpj/libsdl_source.gpj	Modified
9	Adapted delay tap function	TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif.c TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif.h	Modified
10	Updated port assigns for SMARTIO (100-pin) EXT_CLK Port has been updated CAS/CAE devices added.	TVII-SampleSW/tviibe512k/hdr/rev_a/bb_bsp_tviibe512k.h	Modified
11	272-BGA framework added. Added BSP macros for B-H-8M-272 BGA Package	TVII-SampleSW/tviibh8m/hdr/rev_d/bb_bsp_tviibh8m.h	Modified
12	removed reputations of LED and ETH for 272. Updated proper pins for BB_LIN2 and Assigned proper SS Pin for BB_SPI_EEPROM.	TVII-SampleSW/tviibh4m/hdr/rev_b/bb_bsp_tviibh4m_revb.h	Modified
13	Workaround for 1 bit shift instructions.	TVII-SampleSW/common/src/drivers/crypto/src/cy_crypto_core_vu_hw.h	Modified
14	rev_a -> rev_d to match DS revision.	TVII-SampleSW/tviibe512k/hdr/rev_a TVII-SampleSW/tviibe512k/hdr/rev_d Workspaces also adapted	Modified
15	Update ECO configuration according to user guide.	TVII-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.c TVII-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.h	Modified
16	added ISB() instruction where required. removed comments which is no longer required.	TVII-SampleSW/common/src/drivers/prot/cy_prot.c TVII-SampleSW/common/src/drivers/prot/cy_prot.h	Modified

17	support svc handler in C.	TVII-SampleSW/common/src/drivers/syslib/cy_syslib.c TVII-SampleSW/common/src/startup/ghs/startup_cm0plus.arm TVII-SampleSW/common/src/startup/ghs/startup_cm4.arm TVII-SampleSW/common/src/startup/ghs/startup_cm7.arm TVII-SampleSW/common/src/startup/iar/startup_cm0plus.s TVII-SampleSW/common/src/startup/iar/startup_cm4.s TVII-SampleSW/common/src/startup/iar/startup_cm7.s	Added
18	crypto library reference corrections in some and tuning in all. Addition of button/sw_timer mw, which was missing, to stay consistent across projects.	IAR workspaces	Modified
19	Integrated Starter Kit SW into SDL	BE1M and BE2M devices	Added
20	remove pc_save accessing code. added comments for cy_en_prot_pc_t. e.g. PC0 can't be configured	TVII-SampleSW/common/src/drivers/prot/cy_prot.c TVII-SampleSW/common/src/drivers/prot/cy_prot.h	Modified
21	Fix wrong usage of CY_ASSERT in GfxEnv middleware and examples	TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c	Modified
22	Fix wrong usage of CY_ASSERT in all system and driver files	All device system and driver files	Modified
23	add smif version specific driver.	TVII-SampleSW/common/hdr/cy_project.h TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_device_common.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_device_common.h TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.h TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_s25fl.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_s25fl.h TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_s25fs.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_s25fs.h TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.h TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.h	Modified
24	support dlp functionality.	TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.h TVII-SampleSW/common/src/drivers/smif/ver2/cy_smif_ver_specific.c TVII-SampleSW/common/src/drivers/smif/ver2/cy_smif_ver_specific.h TVII-SampleSW/common/src/drivers/smif/ver3_0/cy_smif_ver_specific.c TVII-SampleSW/common/src/drivers/smif/ver3_0/cy_smif_ver_specific.h TVII-SampleSW/common/src/drivers/smif/ver3_1/cy_smif_ver_specific.c TVII-SampleSW/common/src/drivers/smif/ver3_1/cy_smif_ver_specific.h TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.c TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.h	Added
25	update ECO configure function in clock driver.	TVII-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.c TVII-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.h TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.c TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h TVII-SampleSW/tviibe4m/src/drivers/sysclk/cy_sysclk.c TVII-SampleSW/tviibe4m/src/drivers/sysclk/cy_sysclk.h	Modified
26	FreeRTOS sources added from v202011.00 All devices configured to support in dual mode only, only be2m and c2d4m devices tested	TVII-SampleSW/common/src/rtos/	Added
27	New device headers added	tviic2d6mddr rev_a, tviic2d6m rev_b	Added
28	Change Cy_Flashc_InvalidateFlashCacheBuffer and Cy_Flashc_InvalidateFlashBuffer to ensure completion by HW	TVII-SampleSW/common/src/drivers/flash/cy_flash.h	Modified
29	added functions accessing BACKUP CAL_OUT.	TVII-SampleSW/common/src/drivers/sysrtc/cy_sysrtc.c TVII-SampleSW/common/src/drivers/sysrtc/cy_sysrtc.h	Added
30	Update from IAR	TVII-SampleSW/misc/tools/iar/IAR_EWARM_8421_FlashLoader_Patch_TraveoII.7z	Modified

31	fix flash check sum function.	TVII-SampleSW/common/src/drivers/flash/cy_flash.c TVII-SampleSW/common/src/drivers/flash/cy_flash.h TVII-SampleSW/common/src/drivers/srom/cy_srom.c TVII-SampleSW/common/src/drivers/srom/cy_srom.h	Modified
32	Add 6M-DDR PSVP	TVII-SampleSW/misc/tools/ghs/ghs_comp_xxxxxx_defaults_flash/flash_chips_fcr4tcm.odb TVII-SampleSW/misc/tools/ghs/ghs_comp_xxxxxx_defaults_flash/generator/tvii_chip_list.csv	Added
33	Move setting of global component enable bits in VIDEOSS from Cy_GfxEnv_Init to Cy_GfxEnv_EnableTestImage	TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c	Modified
34	uint8_t offset to int8_t uint8_t gain to int8_t	TVII-SampleSW/common/src/drivers/adc/cy_adc.h	Modified
35	added interrupt register readback, when clearing interrupt flag.	TVII-SampleSW/common/src/drivers/sysflt/cy_sysflt.c	Added

Change Log from v6.5.0 to v6.6.0

Sl. No.	Change	Files	Action
1	CM7 startup code: Added dummy read of CPUSS_CM7_X_CTL register to ensure that the changed setting is effective before proceeding	TVII-SampleSW/common/src/startup/ghs/startup_cm7.arm TVII-SampleSW/common/src/startup/iar/startup_cm7.s	Modified
2	Crypto libs (GHS build) added for tviibe512k and tviibe4m	TVII-SampleSW/ghs_build_crypto_libs.bat TVII-SampleSW/tviibe4m/src/drivers/crypto/libs/libcrypto_client_cm4_ghs.a TVII-SampleSW/tviibe4m/src/drivers/crypto/libs/libcrypto_server_cm0plus_ghs.a TVII-SampleSW/tviibe512k/src/drivers/crypto/libs/libcrypto_client_cm4_ghs.a TVII-SampleSW/tviibe512k/src/drivers/crypto/libs/libcrypto_server_cm0plus_ghs.a	Added
3	tviic2d4m: Make cy_gfx_env svn:external (from tviic2d6m)	TVII-SampleSW/tviic2d4m/src/mw TVII-SampleSW/tviic2d4m/src/mw/gfx_env	Modified
4	cy_gfx_env: Make code for global VIDEOSS IP enabling compatible with old and new register names	TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c	Modified
5	differential clock setup (within ext. memories) is now a config option	TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.h	Modified
6	static_inline qualifier was removed to the function Cy_SD_Host_PollTransferComplete and Cy_SD_Host_PollCmdComplete in cy_sd_host.c and also moved these function prototypes to cy_sd_host.h from cy_sd_host.c	TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.c TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.h	Modified
7	SMIF drivers moved from device specific to common based on their respective revisions	TVII-SampleSW/common/src/drivers/smif	Modified
8	. add volatile as required. . from smif ver 3 we have to use TX_DATA_MMIO_FIFO_STATUS for checking fifo status in MMIO mode. . describe connection between driver version and HW ip version. modify tx fifo register to be read. . update so that proper .h file would be included.	TVII-SampleSW/common/src/drivers/smif/ver3_0/cy_smif.h TVII-SampleSW/common/src/drivers/smif/ver3_1/cy_smif.h TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif.h TVII-SampleSW/common/src/drivers/smif/ver2/Readme.txt TVII-SampleSW/common/src/drivers/smif/ver3_0/Readme.txt TVII-SampleSW/common/src/drivers/smif/ver3_0/cy_smif.h TVII-SampleSW/common/src/drivers/smif/ver3_1/Readme.txt TVII-SampleSW/common/src/drivers/smif/ver4/Readme.txt TVII-SampleSW/common/src/drivers/smif/ver2/cy_smif_memslot.c TVII-SampleSW/common/src/drivers/smif/ver2/cy_smif_memslot.h TVII-SampleSW/common/src/drivers/smif/ver3_0/cy_smif_memslot.c TVII-SampleSW/common/src/drivers/smif/ver3_0/cy_smif_memslot.h TVII-SampleSW/common/src/drivers/smif/ver3_1/cy_smif_memslot.c TVII-SampleSW/common/src/drivers/smif/ver3_1/cy_smif_memslot.h	Modified
9	Added code which enable HF1,because HF1 clock can be output from EXT_CLK pin. This is useful when we check the MCU has really gone to DeepSleep mode. examples which use DeepSleep will use EXT_CLK, thus I enabled HF1 by default.	TVII-SampleSW/tviibe1m/src/system/rev_b/system_tviibe1m_cm0plus.c TVII-SampleSW/tviibe1m/src/system/rev_c/system_tviibe1m_cm0plus.c TVII-SampleSW/tviibe1m/src/system/rev_d/system_tviibe1m_cm0plus.c TVII-SampleSW/tviibe512k/src/system/rev_a/system_tviibe512k_cm0plus.c TVII-SampleSW/tviibe2m/src/system/rev_a/system_tviibe2m_cm0plus.c TVII-SampleSW/tviibe2m/src/system/rev_b/system_tviibe2m_cm0plus.c TVII-SampleSW/tviibe2m/src/system/rev_c/system_tviibe2m_cm0plus.c	Modified

10	Delete code which disables FLL in sysInit() which should not be required.	TVII-SampleSW/tviibe1m/src/system/rev_b/system_tviibe1m_cm0plus.c TVII-SampleSW/tviibe1m/src/system/rev_c/system_tviibe1m_cm0plus.c TVII-SampleSW/tviibe1m/src/system/rev_d/system_tviibe1m_cm0plus.c TVII-SampleSW/tviibe2m/src/system/rev_a/system_tviibe2m_cm0plus.c TVII-SampleSW/tviibe2m/src/system/rev_b/system_tviibe2m_cm0plus.c TVII-SampleSW/tviibe2m/src/system/rev_c/system_tviibe2m_cm0plus.c TVII-SampleSW/tviibe4m/src/system/rev_a/system_tviibe4m_cm0plus.c TVII-SampleSW/tviibe512k/src/system/rev_a/system_tviibe512k_cm0plus.c TVII-SampleSW/tviibh4m/src/system/rev_a/system_tviibh4m_cm0plus.c TVII-SampleSW/tviibh4m/src/system/rev_b/system_tviibh4m_cm0plus.c TVII-SampleSW/tviibh8m/src/system/rev_b/system_tviibh8m_cm0plus.c TVII-SampleSW/tviibh8m/src/system/rev_c/system_tviibh8m_cm0plus.c TVII-SampleSW/tviibh8m/src/system/rev_d/system_tviibh8m_cm0plus.c TVII-SampleSW/tviic2d4m/src/system/rev_a/system_tviic2d4m_cm0plus.c TVII-SampleSW/tviic2d6m/src/system/rev_a/system_tviic2d6m_cm0plus.c TVII-SampleSW/tviic2d6m/src/system/rev_b/system_tviic2d6m_cm0plus.c TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm0plus.c	Modified
11	emulator value correction.delete duplicated changelog.	TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h	Modified
12	delete dummy define and unnecessary #include.	TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.h	Modified
13	align with cy_sysflt_config.h of TVII-2D-C-6M.	TVII-SampleSW/tviic2d4m/src/drivers/sysflt/cy_sysflt_config.h	Modified
14	add intr status reading function.	TVII-SampleSW/tviic2d4m/src/drivers/audioss/i2s/cy_i2s.h	Modified
15	add VIDOSS power enabling code.	TVII-SampleSW/tviic2d4m/src/system/rev_a/system_tviic2d4m_cm0plus.c	Added
16	some modification/addition mixer driver.	TVII-SampleSW/tviic2d6m/src/drivers/audioss/mixer/cy_mixer.c TVII-SampleSW/tviic2d6m/src/drivers/audioss/mixer/cy_mixer.h	Modified
17	CS42448 mw added	TVII-SampleSW/tviic2d4m/src/mw/audio	Added
18	New I2S driver added	TVII-SampleSW/tviic2d4m/src/drivers/audioss/i2s	Added

Change Log from v6.4.0 to v6.5.0

Sl. No.	Change	Files	Action
1	removing MISRA references and tables from comments.	/common/src/drivers/lvd/cy_lvd.h /common/src/drivers/smartio/cy_smartio.h /common/src/drivers/syslib/cy_syslib.h /common/src/drivers/syspm/cy_syspm.h /common/src/drivers/syswdt/cy_syswdt.h	Modified
2	cy_stc_gpio_pin_prt_config_t addition.	/common/src/drivers/gpio/cy_gpio.h	Modified
3	tviibe512k update	/common/src/drivers/canfd/cy_canfd.c /common/src/drivers/flash/cy_flash.h /common/src/drivers/sysint/cy_sysint.c	Modified
4	Drive strength 1/8 removed as it is not supported by TVII devices.	/common/src/drivers/gpio/cy_gpio.h	Modified
5	tviibh4m rev_b addition	/tviibh4m/src/interrupts/rev_b /tviibh4m/src/interrupts/rev_b/cy_interrupt_map.c /tviibh4m/src/interrupts/rev_b/cy_interrupt_map_cm0plus.h /tviibh4m/src/interrupts/rev_b/cy_interrupt_map_cm7_0.h /tviibh4m/src/interrupts/rev_b/cy_interrupt_map_cm7_1.h /tviibh4m/src/system/rev_b /tviibh4m/src/system/rev_b/system_cyt4bb.h /tviibh4m/src/system/rev_b/system_tviibh4m_cm0plus.c /tviibh4m/src/system/rev_b/system_tviibh4m_cm7.c	Added
6	removing MISRA references and tables from comments.	/tviibh8m/src/drivers/sd_host/cy_sd_host.h	Modified
7	removing MISRA references and tables from comments.	/tviibh8m/src/drivers/smif/cy_smif.h	Modified
8	removing MISRA references and tables from comments.	/tviibh8m/src/drivers/audioss/cy_i2s.h	Modified
9	DOXY group correction.	/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.h	Modified
10	removing MISRA references and tables from comments.	/tviic2d6m/src/drivers/audioss/pwm/cy_pwm.h	Modified
11	use enums from cy_sysclk.h for the targetDiv in system_*_cm0plus.c to reduce potential errors in future	All device and respective revision system .c files ex: tviibh4m/src/system/rev_a/system_tviibh4m_cm0plus.c	Modified
12	synchronized cy_gfx_env.c/h and examples for tviic2d4m and tviic2d6m	tviic2d4m/src/examples/gfx_env/fast_init/main_cm0plus.c tviic2d4m/src/examples/gfx_env/fast_init/main_cm7_0.c tviic2d4m/src/examples/gfx_env/flexible_init/main_cm0plus.c tviic2d4m/src/examples/gfx_env/flexible_init/main_cm7_0.c tviic2d4m/src/mw/gfx_env/cy_gfx_env.c tviic2d4m/src/mw/gfx_env/cy_gfx_env.h tviic2d6m/src/examples/gfx_env/fast_init/main_cm0plus.c tviic2d6m/src/examples/gfx_env/fast_init/main_cm7_0.c tviic2d6m/src/examples/gfx_env/flexible_init/main_cm0plus.c tviic2d6m/src/examples/gfx_env/flexible_init/main_cm7_0.c tviic2d6m/src/mw/gfx_env/cy_gfx_env.c tviic2d6m/src/mw/gfx_env/cy_gfx_env.h	Modified
13	fixed FDPLINK #1 ifdefs	tviic2d6m/src/drivers/fpdlink/cy_fpdlink.c tviic2d6m/src/drivers/fpdlink/cy_fpdlink.h	Modified
14	Modify drive GPIO drive strength definition.	/common/src/drivers/gpio/cy_gpio.h	Modified

15	Get Flash interface frequency function: Bug fixed.	/tviibh8m/src/drivers/sysclk/cy_sysclk.c	Modified
16	added new configure regulator scratch structure.	/common/src/drivers/srom/cy_srom.h	Modified
17	correct header.	/common/src/mw/button/cy_button.c	Modified
18	correct typo.	/common/src/drivers/srom/cy_srom.c	Modified
19	UL -> ul for AN. I2C examples cleaned for AN.	/common/src/drivers/scb/cy_scb_common.c /common/src/drivers/scb/cy_scb_common.h /common/src/drivers/scb/cy_scb_ezi2c.c /common/src/drivers/scb/cy_scb_ezi2c.h /common/src/drivers/scb/cy_scb_i2c.c /common/src/drivers/scb/cy_scb_i2c.h /common/src/drivers/scb/cy_scb_spi.c /common/src/drivers/scb/cy_scb_spi.h /common/src/drivers/scb/cy_scb_uart.c /common/src/drivers/scb/cy_scb_uart.h	Modified
20	added I2S audio DAC/ADC (AIC261 TI) interface.	/common/src/mw/aic261 /common/src/mw/aic261/cy_aic261.c /common/src/mw/aic261/cy_aic261.h	Added/Modified
21	added function which sets multiple pins.	/common/src/drivers/gpio/cy_gpio.c /common/src/drivers/gpio/cy_gpio.h	Modified
22	move cxpi driver to common folder.	tviibe2m/tviic2d4m/tviic2d6m workspaces aligned accordingly	Added/Modified
23	use temporary CPU register for peripheral register bit modification.	/common/src/drivers/tcpwm/cy_tcpwm.c /common/src/drivers/tcpwm/cy_tcpwm.h /common/src/drivers/tcpwm/cy_tcpwm_counter.c /common/src/drivers/tcpwm/cy_tcpwm_counter.h /common/src/drivers/tcpwm/cy_tcpwm_pwm.c /common/src/drivers/tcpwm/cy_tcpwm_pwm.h /common/src/drivers/tcpwm/cy_tcpwm_quaddec.c /common/src/drivers/tcpwm/cy_tcpwm_quaddec.h /common/src/drivers/tcpwm/cy_tcpwm_sr.c /common/src/drivers/tcpwm/cy_tcpwm_sr.h	Modified
24	minor beautify	/common/src/drivers/adc/cy_adc.c	Modified
25	Arbitrary beautify for application note.	/common/src/drivers/adc/cy_adc.c /common/src/drivers/adc/cy_adc.h	Modified
26	make them use SROM API driver. (Interface did not change.)	/common/src/drivers/flash/cy_flash.c /common/src/drivers/flash/cy_flash.h /common/src/mw/flash/cy_mw_flash.c /common/src/mw/flash/cy_mw_flash.h	Modified
27	Add non-blocking functions and other utilities.	/common/src/drivers/srom/cy_srom.c /common/src/drivers/srom/cy_srom.h	Modified
28	Added APIs which can access IPC_DATA1.	/common/src/drivers/ipc/cy_ipc_drv.c /common/src/drivers/ipc/cy_ipc_drv.h	Modified
29	move flash drivers to common folder.	/common/src/drivers/flash /common/src/drivers/flash/cy_flash.c /common/src/drivers/flash/cy_flash.h	Added/Modified
30	align structure definition.	/common/src/drivers/dma/cy_pdma.h	Modified
31	correct comments.	/common/src/drivers/trigmux/cy_trigmux.c	Modified
32	align with driver of B-H	/tviibe1m/src/drivers/sysclk/cy_sysclk.c /tviibe1m/src/drivers/sysclk/cy_sysclk.h	Modified

33	align with deriver of B-E.	/tviibh8m/src/drivers/sysclk/cy_sysclk.c /tviibh8m/src/drivers/sysclk/cy_sysclk.h	Modified
34	Add below functions. cy_en_sysclk_status_t Cy_SysClk_GetGroupFrequency cy_en_sysclk_status_t Cy_SysClk_GetFlashInterfaceFrequency cy_en_sysclk_status_t Cy_SysClk_GetRamFastFrequency cy_en_sysclk_status_t Cy_SysClk_GetRamSlowFrequency cy_en_sysclk_status_t Cy_SysClk_GetRomFastFrequency cy_en_sysclk_status_t Cy_SysClk_GetRomSlowFrequency	/tviibe1m/src/drivers/sysclk/cy_sysclk.c /tviibe1m/src/drivers/sysclk/cy_sysclk.h	Modified
35	clean.	/common/src/drivers/mpu/cy_mpu.c /common/src/drivers/mpu/cy_mpu.h	Modified
36	refactor	/tviibh8m/src/drivers/sysclk/cy_sysclk.c /tviibh8m/src/drivers/sysclk/cy_sysclk.h	Modified
37	increase value of descriptor can be negative value. hence, changed variable type uint32_t -> int32_t.	/common/src/drivers/dma/cy_mdma.h /common/src/drivers/dma/cy_pdma.h	Modified
38	Cleanup for Application note.	/common/src/drivers/dma/cy_mdma.c /common/src/drivers/dma/cy_mdma.h /common/src/drivers/dma/cy_pdma.c /common/src/drivers/dma/cy_pdma.h	Modified
39	clean up for Application Note.	/common/src/drivers/syswdt/cy_syswdt.c /common/src/drivers/syswdt/cy_syswdt.h	Modified
40	clean up for Application Note.	/common/src/drivers/sysrtc/cy_sysrtc.c /common/src/drivers/sysrtc/cy_sysrtc.h	Modified
41	arbitrary clean for smartio for Application note.	/common/src/drivers/smartio/cy_smartio.c /common/src/drivers/smartio/cy_smartio.h	Modified
42	modified the driver to adapt SMIF V3.0 and SMIF V2.0 IP	/tviibh8m/src/drivers/smif/cy_smif.h	Modified
43	IP enable bit name and the control register name is changed in videoss	/tviic2d4m/src/mw/gfx_env/cy_gfx_env.c	Modified

Technical Support

For assistance, go to http://www.cypress.com/go/support or contact our customer support at +1 (800) 541-4736 Ext. 8 (in the USA), or +1 (408) 943-2600 Ext. 8 (International).

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