SROM

› **Description**:
  – This example executes three SROM API. "silicon id", "read fuse byte", and "read unique id".

› **Target Device**:
  – Traveo-II Body CYT2Bx, CYT4Bx devices
  – Traveo-II Cluster CYT3DLx, CYT4DNx devices

› **CPU Board**:
  – Body Entry CYT2B7/9/L Devices: CYTVII-B-E-1M-176-CPU Rev. C Board
  – Body Entry CYT2B6 Devices: CYTVII-B-E-1M-100-CPU REV 1.0
  – Body High CYT4Bx Devices: CYTVII-B-H-8M-"176/320/272"-CPU BOARD Rev latest
  – Cluster 4M CYT3DLx Devices: CYTVII-C-2D-4M-216-SO (REV_A)
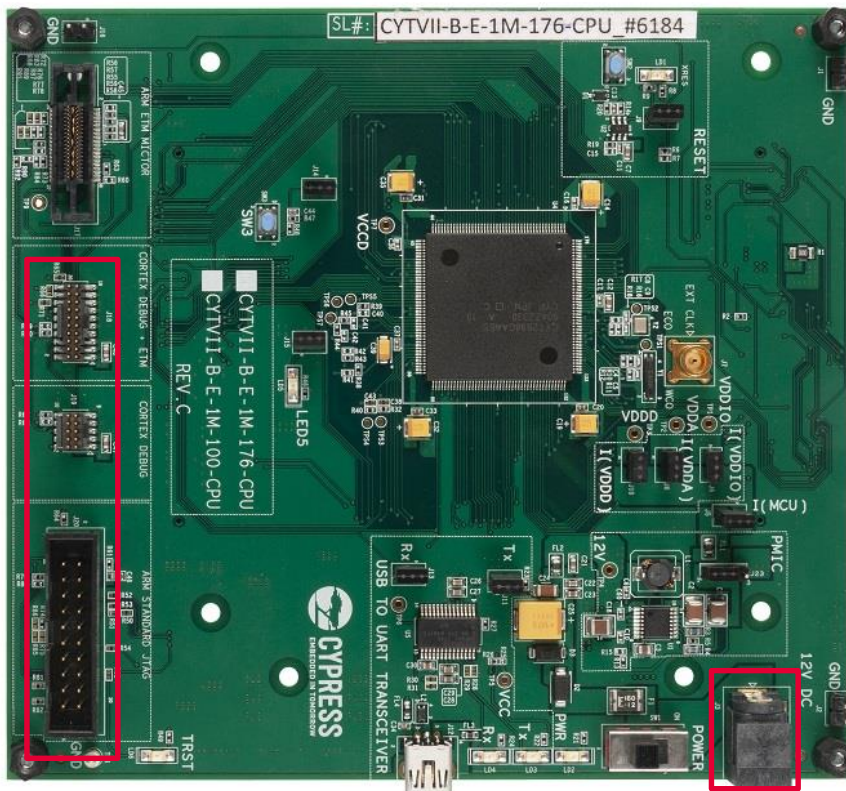 – Cluster 6M CYT4DNx Devices: CYTVII-C-2D-6M-"500/327"-BGA-CPU BOARD Rev latest

› **Dependency:**
  – None

› **Expectation**:
  – Read value will be stored into global variables "SiIdReadValues", "readEfuseByteMap", and "UnIdReadValues". The value depends on CPU revision and its life stage.

SROM

Legend:

- <mark>Red block</mark> for power, debug (Mandatory)

Note:

- Example of TVII-B-E CPU board alone is provided here
- This is true for all the CPU boards targeted for use