

## PROT: SMPU\_PC: cm0plus

### › **Description:**

- This example confirms the functionality of PC (Protection context) using SMPU.
- CM0+ will take a memory access with violation, and CM4 catches the violation details by fault reporting.
- Sets MSx\_CTL (in SMPU) to allow the core to change PC of its MPU to “6”
- Sets PC of MPU associated to CM0+ to “6”
- Sets SMPU STRUCTURE2 so that only masters who have PC value of “6” can access the area (1).
- Sets SMPU STRUCTURE3 so that only masters who have PC value of “5” can access the area (2).
- Accesses the area (1) to confirm CM0+ can access the area.
- Accesses the area (2) to confirm CM0+ can't access the area and causes HardFault.
- CM4 will be noticed of violation details by the fault reporting system.

### › **Target Device:**

- Traveo-II CYT2Bx devices

### › **CPU Board:**

- CYTVII-B-E-1M-176-CPU Rev. C Board

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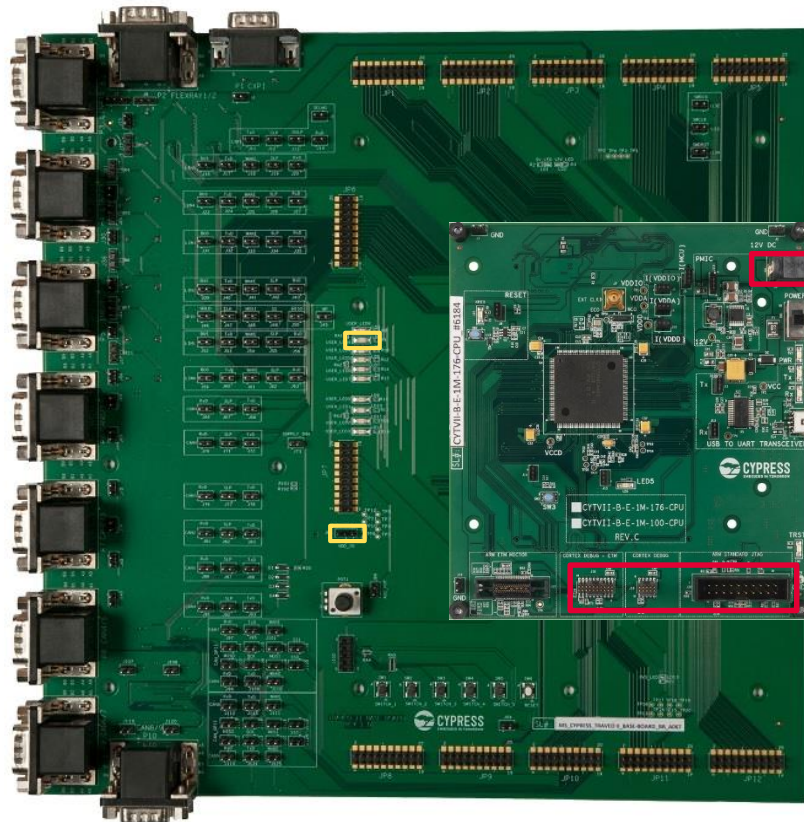
### › **Dependency:**

- Jumper J80 to be short on position 1-2 on Base Board
- CYTVII-B-E-1M-176-CPU board should be connected on CYTVII-B-E-BB board

### › **Expectation:**

- CM0+ core stacks in hardfault handler.
- CM4 blinks an LED in its fault report handler.

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## > Legend:

- Red block for power, debug (Mandatory)
- Yellow block for the example specific connections