Sample Driver Library

Readme

Traveo II Microcontrollers

Date: 05/28/2021

Ver: 7.2.0

Disclaimer

- SDL sample software is provided “as-is”, and **for evaluation purposes only**
- It does not adhere to any industry standard and it is not a production software
- Infineon may, but is not required to, provide technical support for the SDL
- In no event shall Infineon be liable for incidental or consequential damages arising from use of the SDL.

Readme – Tool Chain Support

- **IAR:**
  - IAR Embedded Workbench for ARM 8.42.1, IAR I-Jet Debugger: (Mandatory)
  - Flash loader: /misc/tools/iar/IAR_EWARM_8421_FlashLoader_Patch_TraveoII.7z
  - Installer: http://files.iar.com/ftp/pub/box/EWARM-CD-8421-23878.exe

  - This revision of IAR supports tri-core download and debugging. In multi core mode, after we close the debug session from the master (CM0+) all slaves (CM4/CM7_x) will be automatically closed (This is a new feature in latest IAR revision 8.42.1, not an issue).

  - IAR supports following workspaces:
    - Single core sessions (All devices)
      Ex: tviibe2m_flash_cm4_mc_template.eww, tviibh8m_flash_cm7_0_mc_template.eww etc.
    - Dual core session (All devices)
      Ex: tviic2d6m_flash_cm0plus_cm7_0_template.eww,
      tviibe2m_flash_cm0plus_cm4_template.eww etc.
    - Triple core session (Only TVII-B-H-8M/TVII-C-2D-6M)
      Ex: tviibh8m_flash_cm0plus_cm7_0_cm7_1_template.eww

  - IAR EWARM 8.22.2 support is provided only for cluster devices (TVII-C-2D-4M and TVII-C-2D-6M). Only for the flash projects!
    - Installer: http://files.iar.com/ftp/pub/box/EWARM-CD-8222-15996.exe

Readme – Tool Chain Support

- **Green Hills MULTI**:
  - 7.1.4, Compiler: 2017.1.4, Probe Version: 5.6.5 (DEVELOPMENT AUTOBUILD 5.6 634260/AB as of patch #12996), or higher
  - GHS supports following workspaces:
    - Single core sessions (All devices)
    - Dual core session (All devices)
    - Triple core session (Only TVII-B-H-4M/TVII-B-H-8M/TVII-C-2D-4M/TVII-C-2D-6M)
  - GHS Cortex-M7 ETMv4 trace requirements (please contact GHS for obtaining the necessary SW updates):
    - Probe Package 6.0.2 installed into the used compiler directory
    - Probe:
      - ProbeV4 with at least firmware 6.0.2
      - ProbeV3 or Super Trace Probe with at least firmware v5.7 build 642347

Readme – More Info

- SDL supports multiple revisions based on the devices.
- CY_USE_PSVP must be defined with value '1' or '0' in GHS/IAR project files to compile for PSVP or actual silicon.
- User should select rev_a/rev_b/rev_c based on the device MPN as per the respective device Datasheet.
- For more information on the packages and MPNs/MPN revisions, kindly refer to the Device specific Datasheet.
- FreeRTOS basic support has been added to all the devices, tested on only tviibe2m and tviic2d4m devices/CPU boards.

Readme – Silicon Support

SL. No.	Silicon Die	Device Revision	Package	MPN
1	TVII-B-E-1M	B0/rev_b, B1/rev_c, B2/rev_d	176-LQFP	CYT2B78BAS/CYT2B78BAE/CYT2B78CAS/CYT2B78CAE
2	TVII-B-E-2M	A0/rev_a, A1/rev_b, A2/rev_c	176-LQFP	CYT2B98BAS/CYT2B98BAE/CYT2B98CAS/CYT2B98CAE
3	TVII-B-E-4M	A0/rev_a	176-LQFP	CYT2BL8BAS/CYT2BL8BAE/CYT2BL8CAS/CYT2BL8CAE
4	TVII-B-H-4M	A0/rev_a, A1/rev_b	176-TEQFP 272-BGA	CYT4BB8CEE/CYT4BB8CES CYT4BBBCEE/CYT4BBBCES
5	TVII-B-H-8M	B0/rev_b, B1/rev_c, B2/rev_d	176-TEQFP 320-BGA	CYT4BF8CES/CYT4BF8CEE/CYT4BF8CDS/CYT4BF8CDE/CYTA0100S CYT4BFCCHE/CYT4BFCCHS/CYT4BFCCJE/CYT4BFCCJS
6	TVII-C-2D-6M	A0/rev_a	500-BGA 327-BGA	CYT4DNDBHS CYT4DNJBHS
7	TVII-C-2D-4M	A0/rev_a	216-TEQFP	CYT3DLABAS/CYT3DLABBS/CYT3DLABCS/CYT3DLABDS/CYT3DLABES/ CYT3DLABFS/CYT3DLABGS/CYT3DLABHS
8	TVII-B-E-512K	B2/rev_d	100-LQFP	CYT2B65BAS/CYT2B65BAE/CYT2B65CAS/CYT2B65CAE
9	TVII-C-2D-6M	B0/rev_b	327-BGA	CYT4DNJBxS (Note: No 500-BGA MPNs supported)

Readme – Silicon Support

- **Notes:**
  - For TVII-B-H-4M, TVII-B-H-8M, TVII-C-2D-6M devices,
    - IAR linker “use_psvp = 0” in its ICF file, and global definition CY_USE_PSVP=0
    - GHS relies on global definition CY_USE_PSVP=0.
  - For TVII-B-H-4M/8M devices, with 176-TEQFP REV_E CPU Board
    - User has to define CPU_BOARD_REV4 for using SCB/USB_UART.

Readme – PSVP Support

SL. No.	Silicon Die	Device Revision	Package	MPN
1	TVII-B-E-1M	B0/rev_b	176-LQFP	CYT2B78BAS
2	TVII-B-E-2M	A0/rev_a, A1/rev_b	176-LQFP	CYT2B98BAS
3	TVII-B-H-8M	B0/rev_b	320-BGA	CYT4BFCCHE
4	TVII-C-2D-6M	A0/rev_a, B0/rev_b	500-BGA	CYT4DNDBHS
5	TVII-C-2D-4M	A0/rev_a	328-BGA	CYT3DLBBHS
6	TVII-C-2D-6M-DDR	A0/rev_a	500-BGA	CYT4ENDBHS (Partially tested)
7	TVII-C-E-4M	A0/rev_a	176-LQFP	CYT2CL8BAS (Partially tested)

Readme – PSVP Support

- **Notes**
  - For TVII-B-H-8M, TVII-C-2D-6M, TVII-C-2D-4M, and TVII-C-2D-6M-DDR devices,
    - IAR linker “use_psvp = 1” in its ICF file and global definition CY_USE_PSVP=1.
    - GHS linker relies on global definition CY_USE_PSVP=1.
  - Memory Map: TVII-B-H-8M
    - // Only 2MB of contiguous flash memory is available in PSVP and we use hard-coded assignment
    - // CM0+ :: 0x10000000 to 0x1007ffff (512 KB)
    - // CM7_0 :: 0x10080000 to 0x100fffff (512 KB)
    - // CM7_1 :: 0x10400000 to 0x104fffff (1024 KB)
  - Memory Map: TVII-C-2D-6M/TVII-C-2D-6M-DDR
    - // Only 1MB of non-contiguous flash memory is available in PSVP and we use hard-coded assignment
    - // CM0+ :: 0x10000000 to 0x1003ffff (256 KB)
    - // CM7_0 :: 0x10040000 to 0x1007ffff (256 KB)
    - // CM7_1 :: 0x102f8000 to 0x10377fff (512 KB)
  - Memory Map: TVII-C-2D-4M
    - // Split 512KB +512KB of flash memory is available in PSVP
    - // CM0+ :: 0x10000000 to 0x1007ffff (512 KB)
    - // CM7_0 :: 0x101f8000 to 0x10277fff (512 KB)

Readme – CPU Board Mapping

SL. No.	Silicon Die	Device Revision	CPU Board Revisions
1	TVII-B-E-1M	B0/rev_b, B1/rev_c, B2/rev_d	CYTVII-B-E-1M-176-CPU BOARD REV.A (REV_A) CYTVII-B-E-176-CPU BOARD REV.C (REV_C)
2	TVII-B-E-2M	A0/rev_a, A1/rev_b, A2/rev_c	CYTVII-B-E-1M-176-CPU BOARD REV.A (REV_A) CYTVII-B-E-176-CPU BOARD REV.C (REV_C)
3	TVII-B-E-4M	A0/rev_a	CYTVII-B-E-1M-176-CPU BOARD REV.A (REV_A) CYTVII-B-E-176-CPU BOARD REV.C (REV_C)
4	TVII-B-H-8M	B0/rev_b, B1/rev_c, B2/rev_d	CYTVII-B-H-8M-176-CPU BOARD REV.C/4 CYTVII-B-H-8M-320-CPU BOARD REV.C CYTVII-B-H-8M-272-CPU BOARD REV.B
5	TVII-C-2D-6M	A0/rev_a	CYTVII-C-2D-6M-500-BGA-CPU BOARD REV.B CYTVII-C-2D-6M-327-BGA-CPU BOARD REV.A
6	TVII-B-H-4M	A0/rev_a, A1/rev_b	CYTVII-B-H-8M-176-CPU BOARD REV.C/4 CYTVII-B-H-8M-272-CPU BOARD REV.B
7	TVII-B-E-512K	B2/rev_d	CYTVII-B-E-1M-100-CPU REV 1.0
8	TVII-C-2D-4M	A0/rev_a	CYTVII-C-2D-4M-216-SO (REV_A)
9	TVII-C-2D-6M	B0/rev_b	CYTVII-C-2D-6M-B0-327-BGA-CPU-BOARD-REV-B

Readme – RTOS Support

- **FreeRTOS (FreeRTOSv202011.00)**
  - Supported as example for the application cores CM4 and CM7 in both IAR and GHS in the respective devices
  - IAR: dual core of “CM0+ and CM4” or “CM0+ and CM7_0” to be used for execution
  - GHS: RTOS is included for the application core, no other configuration is needed.
  - For more information refer to readme within the “examples\rtos” of respective device

Readme – General Notes

- **Note TVII-B-H-8M/TVII-C-2D-4M/TVII-C-2D-6M/ TVII-C-2D-6M-DDR:**
  - Not all examples have been tested with CM7 Instruction & Data Caches ON. These examples will disable I- and D-Cache at beginning of main().
  - If issues occur after enabling caches, it is most likely that SCB_CleanInvalidateDCache() and/or SCB_InvalidateICache() calls are missing at the right places.
  - Such issues are expected for examples that involve multiple masters (e.g. DMA, shared SRAM data between multiple CPU cores, ...), or for use cases where data accesses are used to prepare data that will later be accessed instruction-like (e.g. copy code from ROM to RAM before executing it).

Readme – General Notes

- **Note For All Devices:**
  - For all silicons, if the SystemInit is commented out, WDT will be active (default configured in SROM/Flashboot) and may trigger a reset.
  - Reserved SRAM for internal access (NOT AVAILABLE for users, refer to respective Datasheet for more information),
    - Last 2 KB: TVII-B-E-1M rev_a/rev_b/rev_c, TVII-B-E-2M rev_a/rev_b, TVII-B-H-8M rev_a/rev_b, TVII-C-2D-6M rev_a
    - First 2 KB: TVII-B-E-1M rev_d, TVII-B-E-2M rev_c, TVII-B-H-4M rev_a/b, TVII-B-H-8M rev_c/d, TVII-C-2D-6M rev_b, TVII-C-2D-4M rev_a, TVII-B-E-512K/rev_d, TVII-B-E-4M/rev_a, TVII-C-E-4M/rev_a, TVII-C-2D-6M-DDR/rev_a
  - The SRAM area from (SRAM_MAX-6KB) to (SRAM_MAX-2KB) is used by Cypress firmware during boot operation. This area is available to the user, but data retention across resets is not guaranteed in this area, because it might be overwritten by Cypress boot firmware.
  - User needs to change the device PART NUMBER/MPN being used for testing, default ones may be different.
  - rev_a support for tviibh8m device is not available.

Readme – General Notes

- **MPN, PSVP/Silicon, CPU_Board Revision Update**:
  - GHS:
    - File device\tools\ghs\device_common.gpj
    - DEVICE=MPN, USE_PSVP=0 for Silicon and USE_PSVP=1 for PSVP, CPU_BOARD_REV=A or B or C as needed
  - IAR:
    - Open IAR EWARM, select needed revision like rev_a/b etc.
    - Menu Project->Options, C/C++ Compiler->Preprocessor
    - Update SYMBOLS as needed in the "Defined symbols section"

Readme – Specific Terms

- **Terms**
  - Cadence ETH Driver: “*if the customer is using the software to verify/bring-up it is OK to provide them the driver. please get a confirmation that the code should not be published into open-source.*”

Starter Kits Devices Supported

SL. No.	Silicon Die	Device Revision	Package	MPN
1	TVII-B-E-1M	B2/rev_d (starter_kit)	100-LQFP	CYT2B75BAS / CYT2B75BAE / CYT2B75CAS / CYT2B75CAE
2	TVII-B-E-2M	A2/rev_c (starter_kit)	100-LQFP	CYT2B95BAS / CYT2B95BAE / CYT2B95CAS / CYT2B95CAE

Starter Kits Supported

- Traveo II Starter Kit Rev 3.0

Readme – Starter Kits

- **Notes**
  - Demo sample is available in "src/examples/demo" for CM4 core, no other example as part of regular SDL is tested
  - Only IAR supports SK SW.
  - User need to select “starter_kit” from the workspace.
  - Both single and dual cores debugging are supported.
  - IAR with CMSIS-DAP is only supported on SKs.

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