

› **Description:**

- In this example, CM4 core sets fixed PPU for two protection context (PC) so that one PC can access a GPIO register and the other cannot access the GPIO register.
- After that, the CM4 will read the GPIO register with the permitted PC, and with the prohibited PC.
- CM0+ will detect bus error caused by the prohibited access of the CM4.

› **Target Device:**

- Traveo-II CYT2Bx devices

› **CPU Board:**

- CYTVII-B-E-1M-176-CPU Rev. C Board

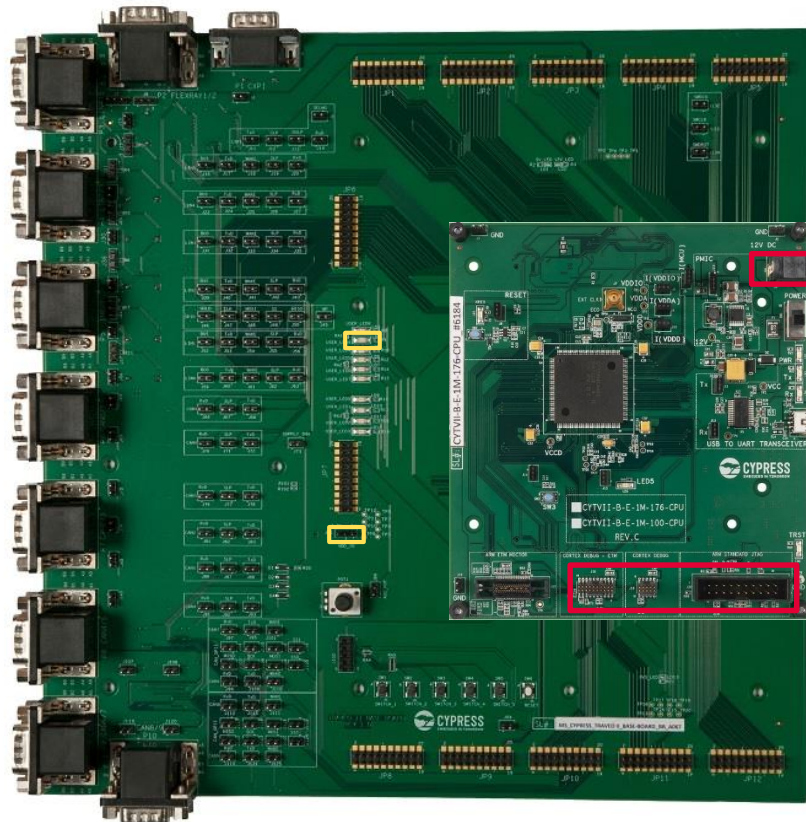
› **Dependency:**

- Jumper J80 to be short on position 1-2 on Base Board
- CYTVII-B-E-1M-176-CPU board should be connected on CYTVII-B-E-BB board.

› **Expectation:**

- CM4 core stacks in hardfault handler.
- CM0+ blinks an LED in its fault report handler.

PROT: PPC_PC: cm4



> Legend:

- Red block for power, debug (Mandatory)
- Yellow block for the example specific connections