

# RISC-V Summit Europe 2025 Summary

Marek Pikuła

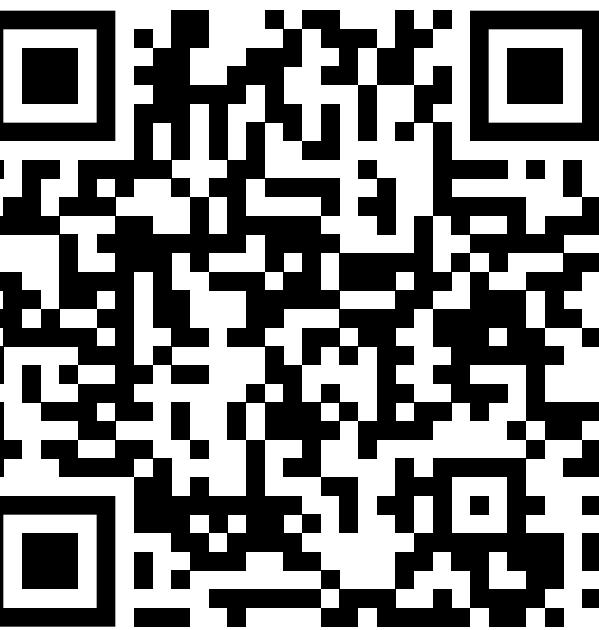
12-15.05.2025, Paris

Conference  
character

<https://riscv-europe.org/summit/2025>

## 3 days in Paris

- 180 attendees on-site
- Hardware/Software: 80/20
- significant China presence

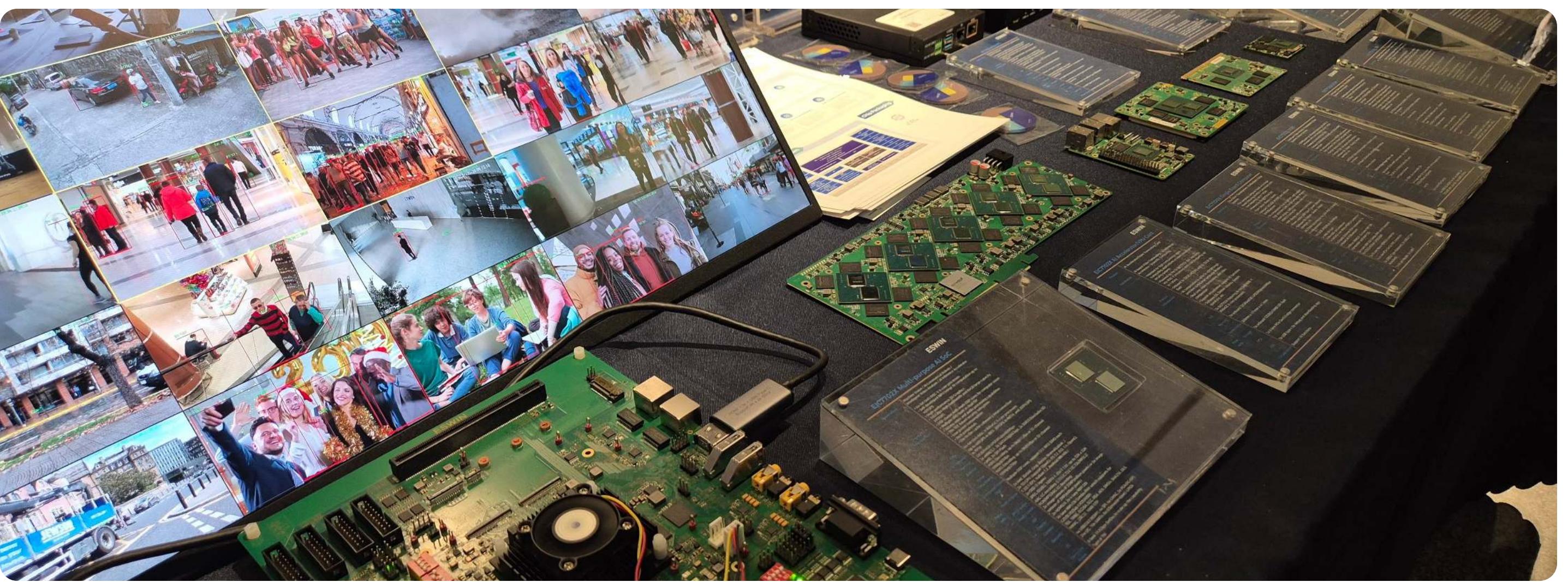
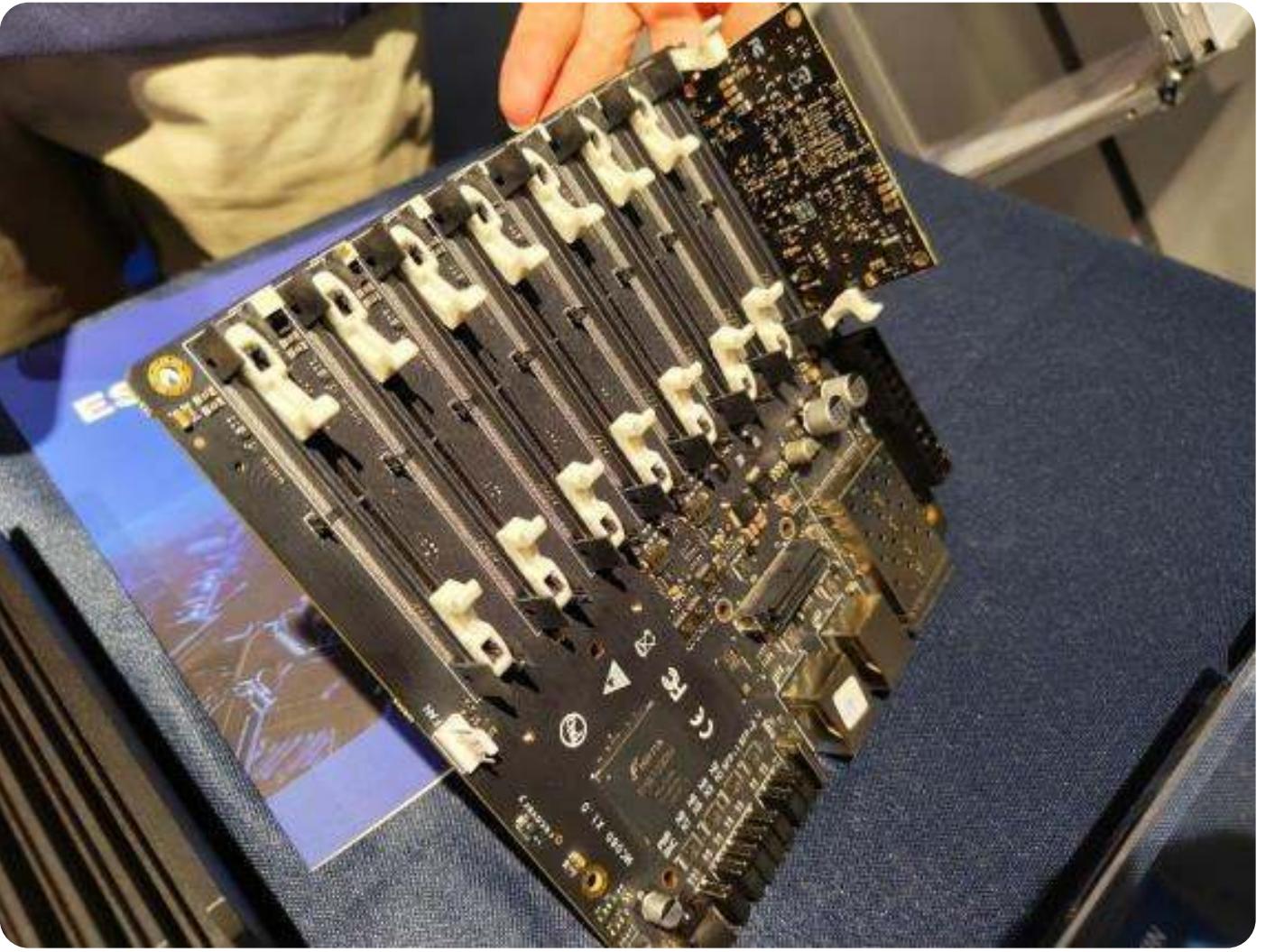


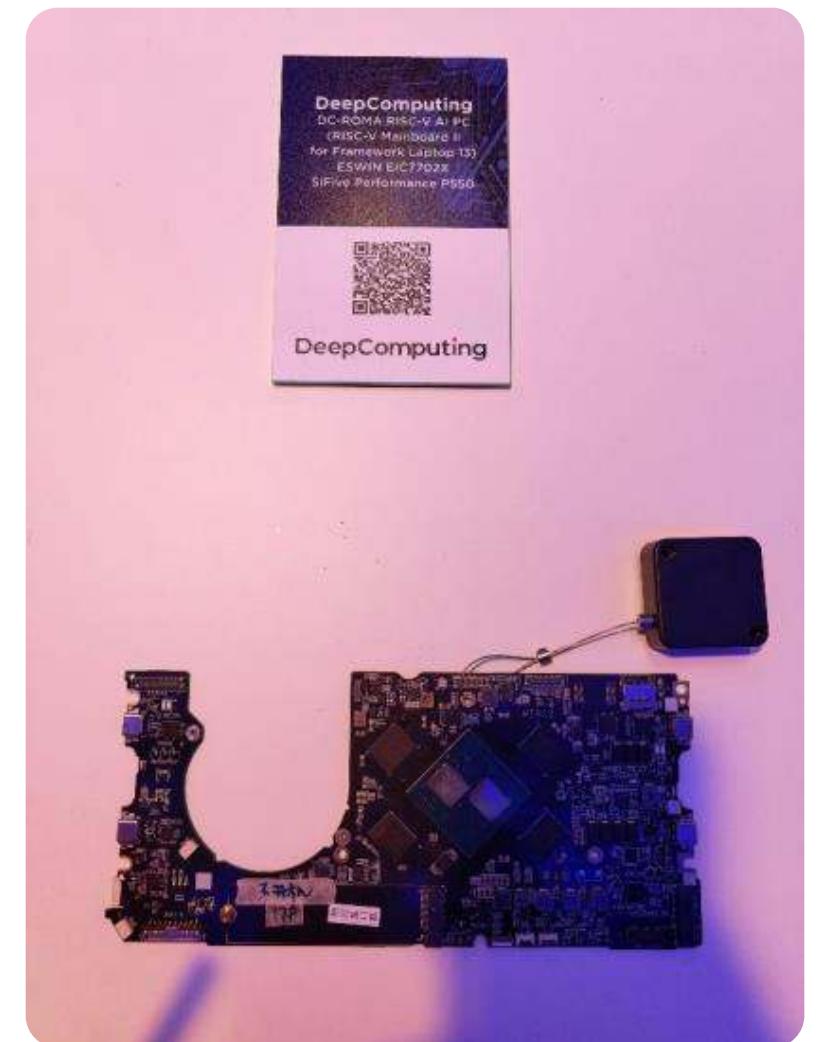
## Domains

- Automotive – migrating to full RISC-V ecosystems.
- Data centers and HPC – first cloud offering, big chips are coming.
- Verification and debugging – a lot of new tools from commercial vendors.
- Security and safety – slow adoption in mission-critical applications.
- Space – ESA completely shifts to RISC-V.



RISC-V  
hardware





# Presentations

# Enabling RISC-V CI in Open-Source Projects: Challenges and Solutions

Author: Marek Pikuła (Samsung R&D Institute Poland)

**Challenge:** Upstream open-source projects lack CI support for RISC-V, hindering validation of architecture-specific code.

**Goal:** Enable RISC-V CI in Freedesktop.org projects (e.g. Pixman, GStreamer Orc) without native hardware.

## Approach:

- Docker-based GitLab runners with QEMU emulation.
- Multi-architecture Docker images with GNU & LLVM toolchains.
- Native execution prioritized; cross-compilation used when needed.

## Impact:

- Found bugs in RISC-V vector (RVV) code early.
- Streamlined testing across SIMD backends and VLENs.
- Enhanced software reliability and contribution workflow.

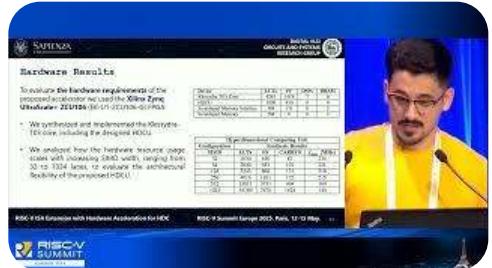
## Outlook:

- Extend to more projects and GitLab instances.
- Explore Cloud-V for hardware-in-CI needs.



# Speech

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## RISC-V ISA Extensions with Hardware Acceleration for Hyperdimensional Computing

Rocco Martino, Sapienza University of Rome et al.

# Description

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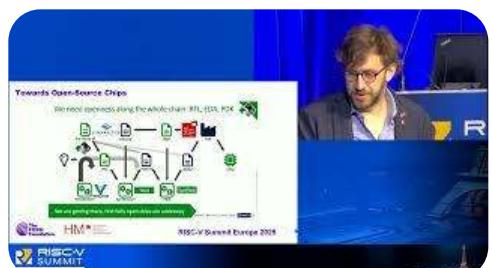
Hyperdimensional computing with custom extensions integrated with GCC. AI on the edge, learning, accelerators. Generic approach, not tightly coupled to dataset.



## RISC-V: Powering the Future of High Performance Computing?

Nick Brown, EPCC

Free-access RISC-V HPC lab. Discussion about hardware readiness and challenges for RISC-V. Showcase of the available accelerators. RISC-V HPC SIG.



## Open Source Chip Design in the European Semiconductor Strategy

Stefan Wallentowitz, FOSSi Foundation

Open source chip design as means for better hardware engineers – they need tools which they can take home and play with. Some European open silicon initiatives.



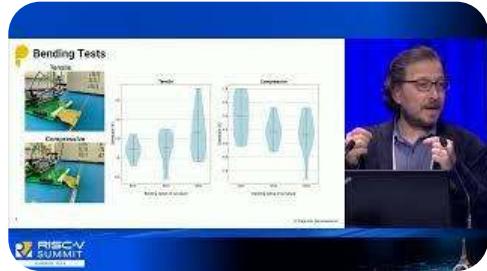
## RISC-V: Reaching New Orbits in Space Computing

Lucana Santos, ESA

ESA: previously SPARC, now tandem SPARC+RISC-V, in the future RISC-V-only. Goal: security, more performance (edge in space), AI/ML for satellite autonomy, advanced DSP, improved fault tolerance. RISC-V is taking over.

# Speech

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## Flex-RV: World's First Non-silicon RISC-V Microprocessor

Emre Ozer, Pragmatic

# Description

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Non-silicon, flexible RISC-V processor based on SERV with small ML accelerator. For now, with external memory. Demo with Hello World.



## The Custom Silicon Imperative: Addressing Manufacturing and Supply Chain Realities

Pablo Valerio, EETimes



## RISC-V State of the Union

Krste Asanović, SiFive

# 15th birthday of RISC-V!

Discussion about profiles: RVA30 – significant step-up in features; until then RVA23 with minor releases with options; early RVM23 profile draft. DSP improvements (Packed SIMD, Matrix Multiplication, AI). Initial work on long instructions.

# Speech



## The Significance of the RVA23 Profile in Advancing RISC-V Ecosystem

Mark Hayter, RIVOS

# Description

Standardization of application cores and a solid base for software vendors. Outlook for the future of profiles (RVM23, RVA30).



## Improvements to RISC-V Vector code generation in LLVM

Alex Bradbury, Igalia

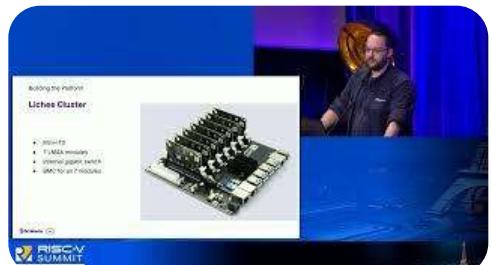
State of RVV autovectorization support in LLVM. Slowly getting to parity with other architectures. Still requires work to use RVV to its full potential.



## The RISE Project: Advancing RISC-V Software

Nathan Egge, Google. Ludovic Henry, Rivos

RISE (RISC-V Software Ecosystem) recent developments. Contribution awards program, (free) training materials.



## Cloud based RISC-V servers: How and why we built them, how you can use them

Fabien Piuzzi, Scaleway

First cloud vendor to offer RISC-V cloud servers. Journey to build the TH1520 cluster hardware. Software adjustments and cloud deployment.

# Thank you!



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