ABSTRACT

The purpose of the assignment is to study the principle of mainframe and the selected mainframe. The mainframe selected for the assignment is IBM zEnterprise EC12 (zEC12). The document explains the overview of a general mainframe including details on the technologies behind, classifications, importance, advantages and disadvantages. It also contains six components about zEC12 such as CPU specification, features and general architecture, Instruction Set and Registers, memory architecture/model, implementation issues, I/O specifications, and Similarities and difference between architecture of zEC12 and the general computer architecture that you study in the class. Not only that, the future of mainframe, limitations of mainframe, and the general conclusion of mainframe will be discussed at the end of the document.

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GANTT CHART

Activities	Duration (week/s)	Periods					
		03/08 – 09/08	10/08 – 16/08	17/08 – 23/08	24/08 – 30/08	31/08 – 06/09	07/09 – 13/09
Preparation	1						
Planning Phase	1						
Work Breakdown	1						
Research	1						
Execution Phase	4						
Evaluation Phase	1						

WORK BREAKDOWN STRUCTURE

TASKS	Albert Tan Choo Sheng (TP035578)	Low Yiyiu (TP035403)	Ng Hui Cheng (TP036501)
Question	Mainframe		
Principle of Mainframe	33%	33%	34%
CPU Specification, Features & General Architecture	100%		
Instruction Set & Registers	100%		
Memory Architecture / Model		100%	
Implementation Issues		100%	
I / O Specifications			100%
Similarities & Differences between Architecture of the Mainframe & the General Computer Architecture that you study in class			100%
Future of Mainframe	33%	34%	33%
Limitation of Mainframe	34%	33%	33%
Conclusion	33%	34%	33%
FAQ	33%	33%	34%
Presentation Slides	34%	33%	33%
Signatures			

I, hereby agree that the above members have undertaken the above tasks and their work is reflective of what I have written above.

Name of Group Leader: **Ng Hui Cheng**

Group Leader's Signature:

OVERVIEW OF MAINFRAME

Mainframe, a term that will not be odd to most of the largest company worldwide since it is playing a central role, performing their daily operations every second. The mainframe is an enormous and expensive computer used primarily by large organizations, fitted of handling hundreds, or even thousands of users concurrently. (Beal, n.d.)

It is a self-contained processing center, powerful enough to perform large-scale transaction processing, manage terabytes of information in the database and handle large bandwidth communication. (Ebbers, et al., 2011)

Typically, the mainframe shares space with many hardware devices such as hardware network routers, external storage devices, channel controllers and automated tape library "robots," and many more. In the past, mainframes need a room just for itself but mainframe need a room just for itself but mainframe these days are not as bulky as before, and it is just part of a data center. (Sasirekha, 2011)

The following section will explain the details on technologies behind mainframe, classifications of the mainframe, the importance of mainframe, and advantages and disadvantages of the mainframe.

Technologies behind Mainframe

Since the 1980s and 1990s, the mainframe has still been surmounting the IT world as a server storage today. It is because mainframe almost never goes down and contains some technologies that have no equivalent in the world of small computers. First of all, it has Tightly Coupled Clustering technology which also known as Parallel Sysplex. The technology features facilitate operating system up to 32 systems as a single system image. Whenever one system fails, the work proceeds automatically on the next live system. At the same time, the performance is thereby improved due to loss of work. Furthermore, it makes the maintenance unit easier as hardware or software of one or more system that need to be maintained can quickly remove. It does not influence the remaining systems as the remaining systems continues with its duty as usual. The removed system also can be plugged in again after the maintenance. With the Parallel Sysplex technology, it helped mainframe in achieving reliability, availability, and serviceability. (Exforsys, 2007)

Virtualization, a virtual version of something such as a server, an operating system, a storage device or network resources (Rouse, 2010). Virtualization enables various operating system instances to run concurrently on a single computer. It means that it enables operating systems to run just like they were installed on physically distinct machines. Modern mainframes provide two level of virtualization namely virtual machines and logical partitions (LPARs). Virtual machines allow a tremendous number of interactive users to communicate or develop and run applications at the same time. Besides, the virtual machine is a self-contained operating environment that behaves as if it is a separate computer (Beal, n.d.). A logical partition (LPAR), is the divisions of a computer's processors, memory, and storage into multiple sets of resources (Rouse, 2013). The reason behind it is so that each set of resources can be operated independently with its operating system and application.

Lastly, the mainframe has Time Sharing Ability technology supported in the system. It is a technology to share a computing resource among multiple users through multi-tasking and multiprogramming (Wikimedia Foundation Incorporation, 2015). Due to mainframe can run multiple operating systems not as a single computer but as some virtual machines, the technology has allowed thousands of users to operate and use the mainframe simultaneously with efficiency. (Exforsys, 2007)

Classification of Mainframe

Mainframes are categorized based on their size, function, purpose, data types and operating system.

SIZE

The size of mainframe computer depends on its age. Meanwhile, the size of the mainframe can be classified as big or medium size. Most mainframes produced are enormous before the year 2000 and reduced in size as time pass. With the miniaturization of computing components, the latest mainframe is considerably smaller. It is approximately the dimension of a huge refrigerator. (Laverty, n.d.)

FUNCTION

Latest mainframes exist in two forms. The first is the newly built multi-purpose machine that is no longer limited to entirely centralized computing. They can serve distributed users and the smaller servers of a computing network. The other type is the old mainframe that have been overhauled to deal with modern requirements such as running Internet-based programs. Despite forecasts that mainframes would be extinct before the turn of the last millennium, these instruments are confirming what Steve Lohr from IBM termed as "the classic survivor technology". (Schamotta, 2015)

PURPOSE

The purpose of the mainframe can be classified into handling wide-ranging processing, data storage, and others. An example of it is a bank transaction. It capable of transferring and handling large amounts of data much rapidly and more reliable to facilitate the demands of users on an enterprise scale. (Laverty, n.d.)

DATA TYPES

Mainframe stores data in one of two ways. Most of it utilize the EBCDIC code set though some may use the ASCII code set. (Schamotta, 2015)

Extended Binary Coded Decimal Interchange Code in short, EBCDIC is an 8-bit character that IBM developed for its larger operating systems (Rouse, 2007). ASCII, known as American Standard Code for Information Interchange is a character-encoding scheme for representing text as numbers with each alphabet assigned a number ranging from 0 to 127 (Beal, n.d.).

The code set relates to the way the mainframes code the alphabet internally. For instance, those using the ASCII code set store the letter "A" as the hexadecimal value 45 (65 decimal). However, in the EBCDIC code set, it is represented by the hex value C1 (193 decimal). Data cannot be transferred between mainframes using different code sets without it being converted first. (Laverty, n.d.)

OPERATING SYSTEM

The operating system installed on a mainframe differs depending on the manufacturer. The operating system of a mainframe is grouped into UNIX, Linux variants or versions of IBM's zOS. For example, IBM-made machines use the MVS operating system. MVS systems emphasize a time-sharing option environment similar to the DOS prompt familiar to PC users. (Schamotta, 2015)

Importance of Mainframe

Mainframes are very significant. The financial industry and many of the critical operations required by large enterprises relied heavily on mainframes. Virtualization is one of the importance of mainframe. Multiple operating system and multiple applications could run on a single mainframe system. With the help of virtualization, a single mainframe can serve the needs of an entire company using remote terminals. (Cartaino, 2010)

Besides, mainframe allows multi-user operations. In pre-web days, if big groups of users required access to a central database and (centralized application) mainframe systems where the only option to support such large utilization rates and large throughput. Today, the Internet connect users and data through distributed systems, which can be size according to the specific transaction levels needed. (Cartaino, 2010)

Not only that, the mainframe is important in terms of scalability. Massive up-front hardware cost and software licensing cost of mainframes give users vertical scalability (big hardware) to handle huge demand (current and future). It can perform even better as processors, memory, and storage are added, allowing them to run multiple tasks of varying complexity easily. (Cartaino, 2010)

The mainframe is still paramount in banking because of its security and reliability. It has an enormous amount of safety features available which make difficult for an intruder to hack the system. For example, user authentication, auditing, access control, and firewalls. Furthermore, the components of hardware are designed to stay and run longer than average computer parts. It is because the components are made to withstand the extra heat that are produced from the inside parts of a mainframe.

Advantages and Disadvantages of Mainframe

Advantages of Mainframe

- ✓ Support thousands of transactions per second
- ✓ Capable serve thousands of users and applications at the same time
- ✓ More speed, computation power, and graphics capabilities than ordinary personal computers
- ✓ Manage data more reliable and secure than client-server networks
- ✓ Backward compatible with legacy mainframe software
- ✓ Stable and reliable when multi-tasking
- ✓ Long lasting performance
- ✓ Operate almost 24/7 hours
- ✓ 99% uptime

(Normanton, n.d.)

Disadvantages of Mainframe

- ✓ Require backwards-compatibility with mainframe operating systems
- ✓ Require staffs with specific skills to run the mainframe system
- ✓ High cost
- ✓ Large and take up much space
- ✓ Require specialized environment management
- ✓ Time-consuming for the installation
- ✓ Complicated to set up due to the size and the hardware elements are different than a regular computer
- ✓ Difficulty to configure because it is accessed via the terminal

(Normanton, n.d.)

MAINFRAME

CPU Specification, Features and General Architecture

The zEnterprise EC12 (zEC12) has up to hexa-core in a microprocessor chip with a highest clock speed of 5.5GHz. The core itself is a dedicated co-processor (COP) that includes 16kb cache, allowing acceleration in the process of compression and cryptographic. It is an improvement over z196 where two cores shared a coprocessor. As for the processor chip, it is made up of 32nm silicon on insulator circuit that consists 15 layers of metal, 3.3 billion transistors, and 7.68km wire. An image of zEC12 hexa-core processor chip can be found in ***Figure 2.1.1***. (Raave, et al., 2013)

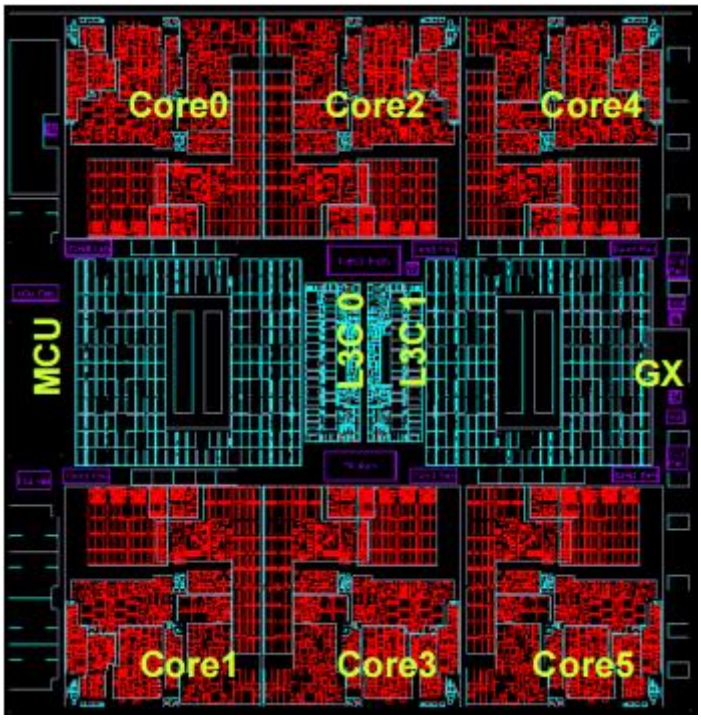

Figure 2.1.1 Image of zEC12 Hexa-core Processor Chip
(Emery, 2013)

Each chip has three level of cache. The Level 1 (L1) of the cache has a 64KB I-cache and a 96KB D-cache with a total 160KB in each core. As for Level 2 (L2), every core contains a 2MB private cache that can be split into 1MB D-cache and 1MB I-cache. However, Cache Level 3 (L3) is shared by the six core with a total of 48MB cache. (Raave, et al., 2013)

Besides, all the processor chips are located in a Multiple Chips Module (MCM) that allows six zEC12 microprocessor chips in a single module. MCM can be found in ***Figure 2.1.2***. It can be categorized as a Central Processor (CP), Integrated Facility of Linux (IFL) Processor,

Internal Coupling Facility (ICF) Processor, zApplication Assist Processor (zAAP), z10 Integrated Information Processor (zIIP) or additional System Assist Processor (SAP). All the processor features can be found in ***Table 2.1.3***. (Raave, et al., 2013)

Figure 2.1.2 Image of Multiple Chips Module (MCM)
(Raave, et al., 2013)

Classification of PUs	Features & Usage
Central processor (CP)	The standard processor. It is able to use with any supported operating system and user applications.
Integrated Facility for Linux (IFL)	Exclusively used with Linux on System z and for running the z/VM hypervisor in support of Linux. z/VM is often used to host multiple Linux virtual machines (called guests)
Internal Coupling Facility (ICF)	Used for z/OS clustering. ICFs are dedicated to the function and exclusively run the Coupling Facility Control Code (CFCC).
IBM System z Application Assist Processor (zAAP)	Used under z/OS6 for designated workloads, which include the IBM Java Virtual Machine (JVM) and XML System Services functions.
IBM System z Integrated Information Processor (zIIP)	Used under z/OS6 for designated workloads, which include various XML System Services, IPSec offload, certain parts of IBM DB2 DRDA®, star schema, IBM HiperSockets™ for large messages, and the IBM GBS Scalable Architecture for Financial Reporting.
Additional System Assist Processor (SAP),	Used by the channel subsystem.

Table 2.1.3 Features of PUs
(Doboš, et al., 2014)

Furthermore, the maximum amount of cores depends on the zEC12 model name. The number of cores available in the different model name of zEC12 can be found in ***Figure 2.1.4***.

Model	Books/ PUs	CPs	IFLs uIFLs	zAAPs	zIIPs	ICFs	Std SAPs	Optional SAPs	Std. Spares	Rsvd. PUs
H20	1/27	0-20	0-20 0-19	0-10	0-10	0-20	4	0-4	2	1
H43	2/54	0-43	0-43 0-42	0-21	0-21	0-43	8	0-8	2	1
H66	3/81	0-66	0-66 0-65	0-33	0-33	0-66	12	0-12	2	1
H89	4/108	0-89	0-89 0-88	0-44	0-44	0-89	16	0-16	2	1
HA1	4/120	0-101	0-101 0-100	0-50	0-50	0-101	16	0-16	2	1

Figure 2.1.4 Core available in zEC12 model

(Emery, 2013)

Instruction Set and Registers

The design of the superscalar processor allows zEC12 up to three instructions to be decoded per cycle and up to seven instructions or operations to be executed every cycle. Instruction and operand fetching can occur out of sequence for both execution and storage accesses. (Raave, et al., 2013)

With the support of the Extended Translation Facility (ETF), instructions have been added to z/Architecture set. They are used to operate in a data conversion for Unicode data, which increase the efficiency of the applications that are enable for Unicode. (Raave, et al., 2013)

The processor supports many instructions to assist functions like hexadecimal floating point instructions, immediate instructions, load instructions for handling unsigned halfwords, cryptographic instructions, ETF-3 instructions, and assist instructions that help to eliminate hypervisor processor usage. A superscalar processor has six execution units namely two fixed point (integer), two load or store, one decimal floating point and one binary floating point. (Raave, et al., 2013)

In ***Figure 2.2.1***, it shows the layout of the core for the each functional area while the explanation about the functional areas of each core can be found in ***Table 2.2.2*** and ***Table 2.2.3***.

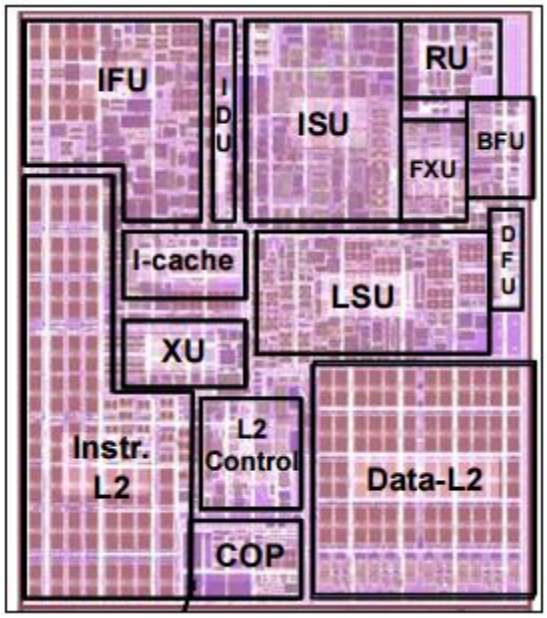

Figure 2.2.1 Image of Core Layout

Functional Areas	Features
Instruction sequence unit (ISU)	✓ Enables the out-of-order (OOO) pipeline which tracks register names, OOO instruction dependency and handling the dispatch of instruction resource.
Instruction Fetching Unit (IFU)	✓ Contains the instruction cache, branch prediction logic, instruction fetching controls and buffers.
Instruction Decode Unit (IDU)	✓ Fed from the IFU buffers ✓ Responsible for parsing and decoding of all z/Architecture operation codes.
Load-Store Unit (LSU)	✓ Contains data cache ✓ Responsible for handling all types of operand accesses of all length, modes and formats as defined in the z/Architecture
Translation Unit (XU)	✓ Has a large translation lookaside buffer (TLB) ✓ The Dynamic Address Translation (DAT) handles the dynamic translation of logical to physical addresses.
Fixed-point unit (FXU)	✓ Handles fixed-point arithmetic
Binary floating point unit (BFU)	✓ Handles all binary and hexadecimal floating point and fixed-point multiplication operations.
Decimal floating-point unit (DU)	✓ Runs both floating point and decimal fixed point operations and fixed-point division operations.

Table 2.2.2 Features of Functional Areas

(Raave, et al., 2013)

Functional Areas	Features
Recovery Unit (RU)	✓ Keep a copy of the complete state of the system that includes all registers, collect hardware fault signals and manages the hardware recovery actions.
Dedicated Co-Processor (CoP)	✓ Responsible for data compression and encryption functions for each core.

Table 2.2.3 Features of Functional Areas

(Raave, et al., 2013)

Memory Architecture/Model

Figure 2.3.1 explains about the memory architecture of zEC12 that consists of four levels and one main storage. The four level cache structure is executed within the Multiple Chips Module (MCM). The first three levels of memory can be found in each processing unit (PU) chip and the level four of memory can be found in the two storage control chips. (Raave, et al., 2013)

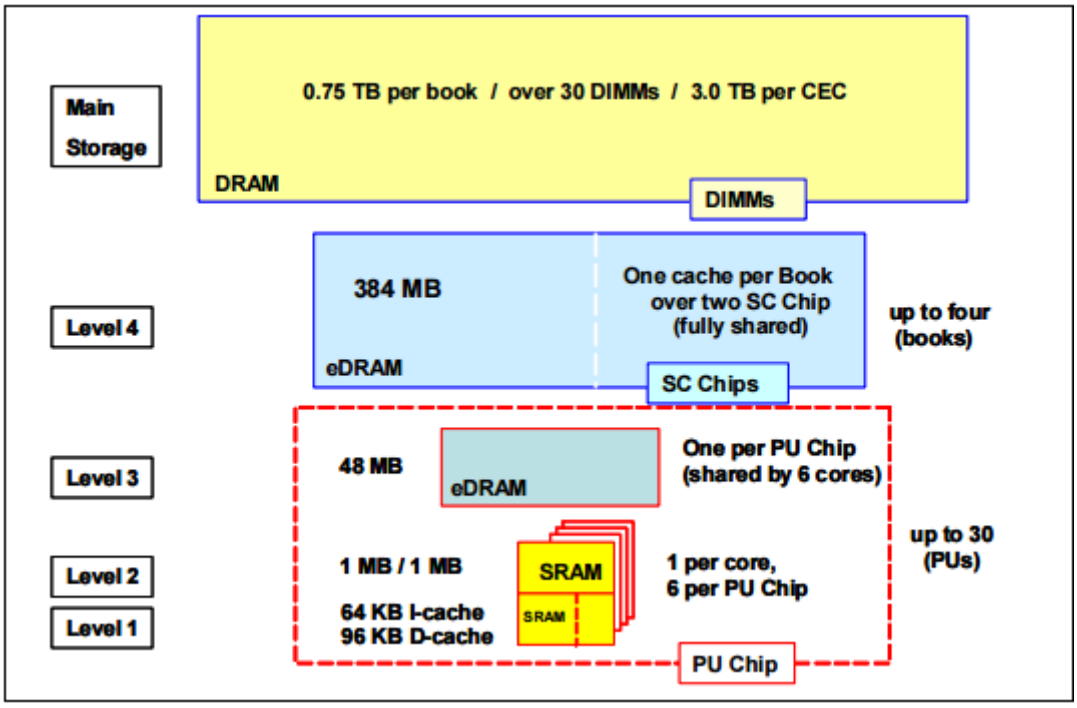

Figure 2.3.1 Image of zEC12 Memory Architecture

(Ebbers, et al., 2011)

Level 1 (L1) and Level 2 (L2) caches use static random access memory (SRAM) while Level 3 (L3) cache uses embedded dynamic static random access memory (eDRAM). The first two cache are independent for each core, but the L3 cache is shared by the six cores within the PU chip. Each book has six L3 caches. Thus, a four-book system has 24 of them, resulting in 1152MB (48 x 24 MB) of the shared PU chip-level cache. Meanwhile, the Level 4 (L4) cache uses eDRAM and is shared by all PU chips on the MCM. Main storage has up to 0.75TB per book using up 30 DIMMs. A four-book system can have up to 3TB of central storage. (Raave, et al., 2013)

zEC12 uses the redundant array of independent memory (RAIM) technology for a fully fault-tolerant N+1 design. It has five layers of memory recovery in the RAIM technology. As a result, the design will detect and recover from DIMM failures, memory channel, socket or DRAM. However, it requires the addition of one memory channel that is dedicated for RAS which can be found in ***Figure 2.3.2***. (Raave, et al., 2013)

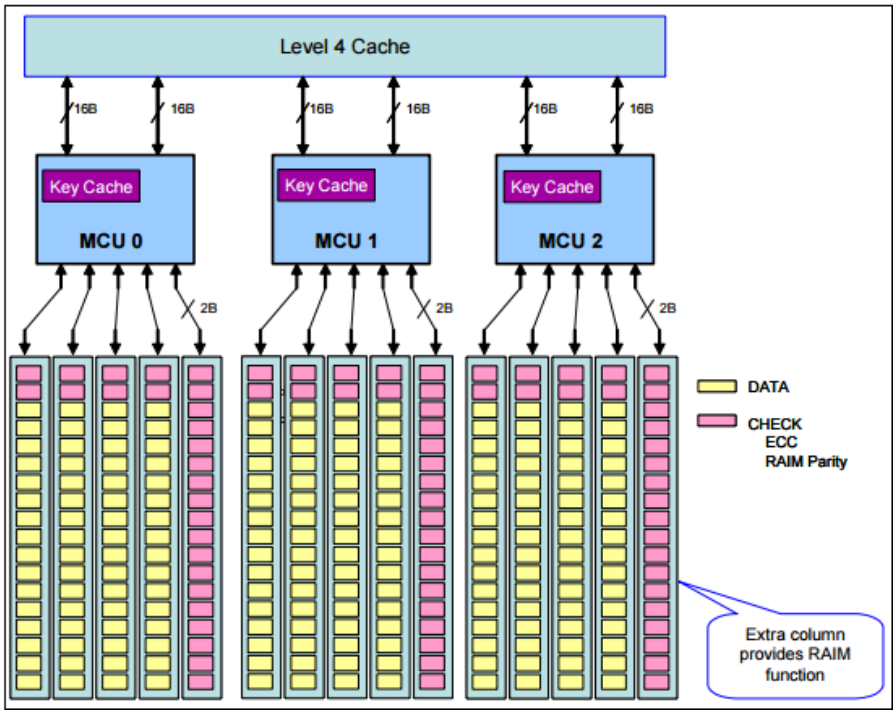

Figure 2.3.2 Image of RAIM DIMMs

(Raave, et al., 2013)

Furthermore, maximum physical memory size is directly proportional to the number of books available in the system. Each book contain up to 960GB with a total of 3.75TB of installed memory per system, but it usually depends on the model name of the zEC12. Due to part of the physical installed memory is used to implement the RAIM design, it results in up to 765GB available memory per book and up to 3TB per system. The maximum amount of memory sizes on different types of zEC12 can be found in ***Figure 2.3.3***. (Raave, et al., 2013)

Customer Memory	Model H20	Model H43		Model H66			Model H89 and Model HA1			
(GB)	Book 1	Book 1	Book 3	Book 1	Book 2	Book 3	Book 0	Book 1	Book 2	Book 3
32	80[a]	80[a]	80[a]	40	40	40	40	40	40	40
64	120	80	80	40	40	40	40	40	40	40
96	160	80	80	60	40	40	40	40	40	40
128	240	100	100	60	60	60	60	40	40	40
160	240	120	120	80	80	60	60	60	60	40
192	320	160	120	100	80	80	80	60	60	60
224	320	160	160	100	100	100	80	80	80	60
256	400	240	160	120	120	100	100	80	80	80
320	480	240	240	160	160	100	120	100	100	100
384	640	320	240	240	160	160	160	120	120	100
448	640	320	320	240	240	160	160	160	160	100
512	800	400	320	240	240	240	240	160	160	160
608	800	400	400	320	240	240	240	240	160	160
704	960	480	480	320	320	320	240	240	240	240
800	N/A	640	480	400	320	320	320	240	240	240
896	N/A	640	640	400	400	400	320	320	320	240
1008	N/A	640	640	480	400	400	320	320	320	320
1136	N/A	800	640	480	480	480	400	400	320	320
1264	N/A	800	800	640	480	480	400	400	400	400
1392	N/A	960	800	640	640	480	480	480	400	400
1520	N/A	960	960	640	640	640	480	480	480	480
1760	N/A	N/A	N/A	800	800	640	640	640	480	480
2016	N/A	N/A	N/A	960	800	800	640	640	640	640
2272	N/A	N/A	N/A	960	960	960	800	800	640	640
2528	N/A	N/A	N/A	N/A	N/A	N/A	800	800	800	800
2784	N/A	N/A	N/A	N/A	N/A	N/A	960	960	800	800
3040	N/A	N/A	N/A	N/A	N/A	N/A	960	960	960	960

Figure 2.3.3 Table of Memory Installed on zEC12 Model

(Raave, et al., 2013)

Besides, the memory subsystem of zEC12 uses high speed, differential-ended communications memory channel to link a host memory to main memory storage devices. Based on ***Figure 2.3.4***, DIMMs are connected to the MCM through three Multiple Chips Units (MCUs) on PU0, PU1 and PU2. Each MCU uses five channels and one of the channels is used for the RAIM implementation in a 4+1 (parity) design. Due to each channel has one or two chained DIMMS, a single MCU can have five or ten DIMMs. Each of the DIMMs has 4GB, 15GB or 32GB but its size cannot be combined in a book. (Raave, et al., 2013)

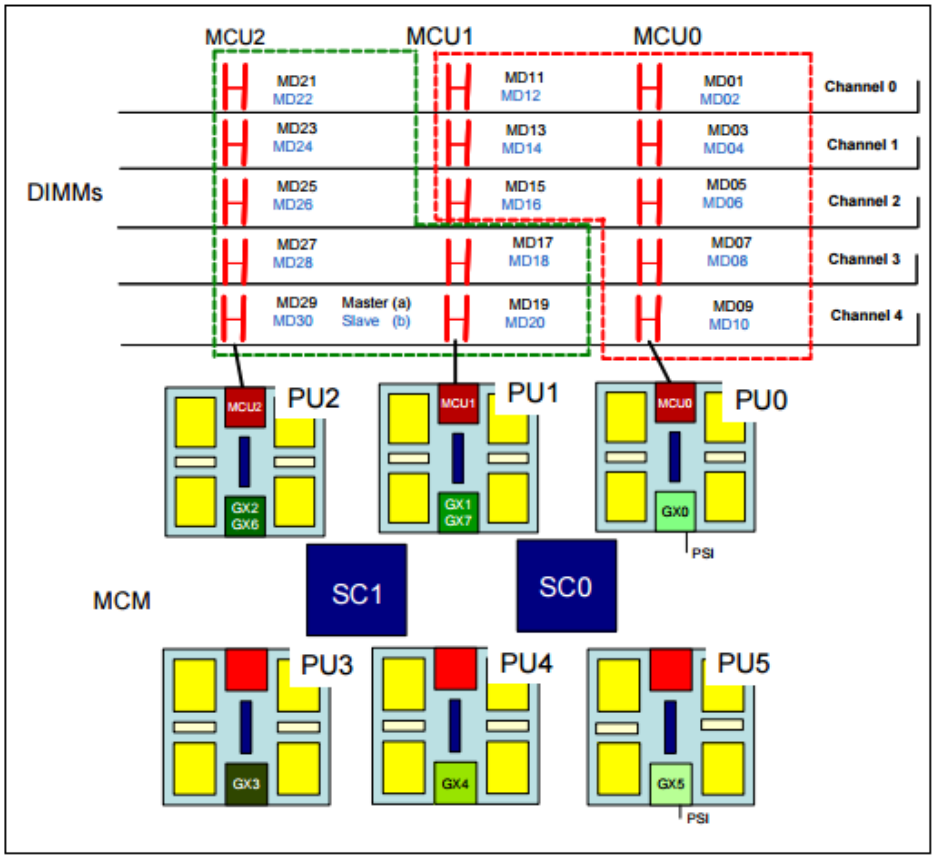

Figure 2.3.4 Overview of zEC12 Book Memory Topology

(Raave, et al., 2013)

Implementation Issues

One of the major implementation issues of zEC12 would be pipelining. Pipelining increases the performance of the mainframe by overlapping the execution of instructions thus lessening the overall execution duration. Shown in ***Figure 2.4.1***. On the left, system without pipelining, will need to complete the instructions in sequence. However, the system on the right, with pipelining, will be able to overlap the executions of the three instructions, therefore, reducing the execution time. Although pipelining increases the performance of the mainframe significantly, it still has few notable issues.

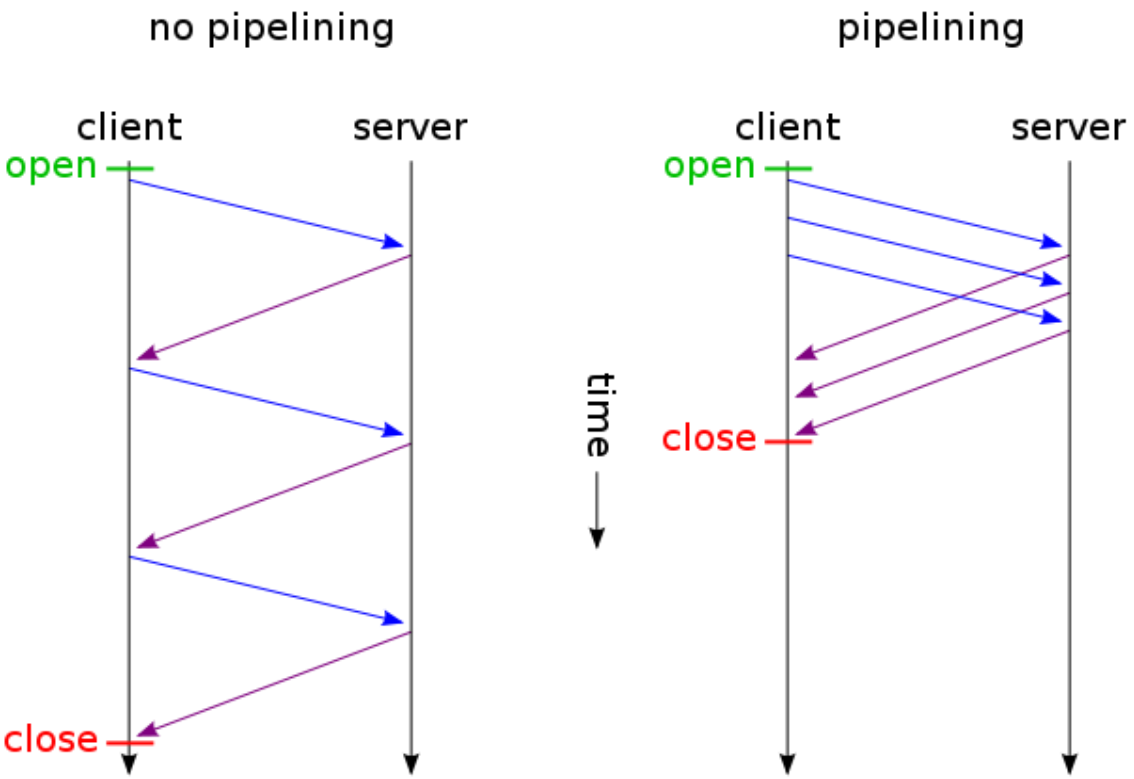

Figure 2.4.1 Concept of Pipelining
(Wikimedia Foundation Incorporation, 2015)

First of all, the existence of data dependency will arise if the mainframe is using pipelining. Data dependency is when an instruction is dependent on a result of a sequentially previous instruction before it can complete its execution. For example, we have two instructions, first one is 'movl $5, %EAX' and the second one is 'movl %EAX, %EBX'. When the first instruction proceeds to the execution stage, instruction two is reading EAX. This creates a data dependency because the first instruction has not reached the writeback stage yet, so EAX does not have the updated value. Therefore, the system will have to delay and slows down the

flow and wait till instruction 1 has completed the writeback and PC update stage before executing instruction 2. By default, programs execute the instructions in sequence but certain programs use branch instructions that cause the execution to start from a different part of the program. The pipelining structure starts working on the next instructions before the first one ended. This requires the machine to know which instructions to execute next. However, branching of instructions made it almost impossible to understand it in general. This will cause stalls as it will need to restart the pipeline over again.

The other major implementation issue of the zEC12 would be superscalar processing method. The superscalar processor implements a form of parallelism called instruction-level parallelism. It processes more than one instruction per clock cycle and separates the fetch and execute as much as possible. Superscalar also has few issues similar to pipelining such as data dependency and branch instructions. It also has issues of its own such as Out-of-order processing hazard and register access conflicts.

I/O Specifications

The zEC12 provides increased processing and I/O capacity over its predecessor, the z196 system. The capacity is achieved by increasing the performance of the individual PUs and the number of PUs per system for possible energy savings, allow fusing diverse applications on a single platform, with significant financial savings. (Raave, et al., 2013)

The zEC12 expands the sub-capacity settings, offering three sub-capacity levels for up to 20 processors that are characterized as central processors (CPs). The structure provides a total of 161 distinct capacity settings in the system and provides a range of over 1:320 in processing power. (Doboš, et al., 2014)

Each book has up to eight dual-port fanouts to support two types of I/O infrastructures for data transfer namely PCIe I/O infrastructure with bandwidth of 8 Gbps and InfiniBand I/O infrastructure with bandwidth of 6 Gbps. The zEC12 supports both a PCIe and an InfiniBand I/O infrastructure. PCIe features are installed in PCIe I/O drawers. Up to five PCIe I/O drawers are supported, providing space for up to 160 I/O features. (Raave, et al., 2013)

The zEC12 takes advantage of PCIe to implement an I/O bus that implements the PCIe infrastructure. It is preferred infrastructure and can be used with InfiniBand. Meanwhile, the zEC12 takes advantage of InfiniBand to implement a 6 Gbps I/O bus that includes the InfiniBand infrastructure, Parallel Sysplex, and host channel adapters. (Raave, et al., 2013)

There are up to 48 high-performance fan-out connections for data communications between the books and the I/O infrastructure. The multiple channel subsystem (CSS) architecture allows up to four CSSs, each with 256 channels. (Raave, et al., 2013)

Connectivities supported by zEC12 are listed in ***Table 2.5.1***.

<table>
<tr><td>Storage Connectivity</td><td colspan="2">Fibre Channel connection (FICON)
FICON Express8S 10 KM long wavelength (LX) and short wavelength (SX)
FICON Express8 10 KM LX and SX
FICON Express4 10 KM LX and SX (Four port cards only)</td></tr>
<tr><td rowspan="2">Networking Connectivity</td><td rowspan="2">Open Systems Adapter (OSA)
OSA-Express5S 10 GbE LR and SR
OSA-Express5S GbE LX and SX
OSA-Express5S 1000BASE-T Ethernet
OSA-Express4S 10 GbE LR and SR
OSA-Express4S GbE LX and SX
OSA-Express4S 1000BASE-T Ethernet
OSA-Express3 10 GbE LR and SR
OSA-Express3 GbE LX and SX
OSA-Express3 1000BASE-T Ethernet</td><td>IBM HiperSockets™</td></tr>
<tr><td>10 GbE Remote Direct Memory Access (RDMA) over Converged Ethernet (RoCE)</td></tr>
<tr><td>Coupling and STP Connectivity</td><td colspan="2">Parallel Sysplex InfiniBand coupling links (IFB)
Internal Coupling links (IC)
InterSystem Channel-3 (ISC-3), peer mode only</td></tr>
</table>

Table 2.5.1

Similarities and Difference between Architecture of the Mainframe and the General Computer Architecture that you study in class

Similarities:

- Both requires hardware (Motherboard, Processor, Bus, Memory, Storage, Display Unit, I/O Devices)
- Programmed to manipulate, store and retrieve data
- Able to responds to instructions by the programs or operating system
- Able to execute programs
- Requires operating system to function
- Requires power supply to boot up

Differences:

Architectures	**zEC12**	**General Computer**
Type of CPU	Superscalar	Microprocessor
Speed of CPU	Higher	Slower
Type of Memory	eDRAM	SRAM
Power Consumption	High	Low
Size	Large & Heavy	Small & Lightweight
Cost	High	Low
Interface	Command-line	Advanced Graphical User
Security	High	Low
Number of Cores	Up to 120	Up to 8
I/O Bandwidth	Large	Small
Number of Users	Thousands	Only one

Table 2.6.1 Differences between a zEC12 and a General Computer

FUTURE OF MAINFRAME

Mainframe technology is progressing at a much slower pace than most of the machines such as personal computer, laptop, smartphones and many more. While there is much talk about having a machine as powerful as a mainframe yet as small as a smartphone.

However, mainframe technology is about to move ahead more rapidly in the coming years with the approach of two improved technologies - Cloud Computing and User Prediction.

Throughout history, we have learned that the primary concern of technology is insufficient storage. While current mainframe technology gives us the storage we could ask for, we are still restricted to having the fixed amount of storage. Certain mainframes are not allowed to increase its storage size. If we can have a mainframe that runs entirely on the cloud, except for its operating system, with the help of advanced user predictions, it would be bringing mainframe to a whole new level.

In the near future, mainframes would be able to predict the user's action and act accordingly. For example, the mainframe will load a cached copy of all the files in the directory. However, if a user always opens the file located at "C:/Program Files/Gayxe/PinkRedGreen.xlsx", whenever the user loads to Program Files, the mainframe will automatically download a copy of PinkRedGreen.xlsx from the cloud.

LIMITATIONS OF MAINFRAME

One of the notable drawbacks of using a mainframe is the cost of maintaining it in excellent condition. Regardless of hardware or software, both are equally hard to support. The software of a mainframe are mostly custom-made and to keep it up-to-date, the organisation will need to spend a tremendous amount of expenses on it. The initial startup cost of a mainframe can be extremely high, from setting up the environment till keeping the mainframe running. The power consumption of powering up a mainframe is extremely high. According to IBM, the zEC12 might need up to 520V DC power source to keep it running efficiently. Therefore, the organisation will have to spend a lot to get the right environment for the necessary mainframe to run. Secondly, mainframe hardware occupies larger space than other computers. That large area might be a constraint for small businesses. However, that problem is not as critical as it once was because nowadays mainframes are small. Finally, one requires a specialised administrator to operate the mainframe computers. You cannot run a mainframe environment without particular training. However, as one dedicated administrator can serve a large group of mainframe users.

CONCLUSION

This documentation introduced mainframes and how they could be classified (size, purpose, operating system). We presented information about the CPU specifications and its features. We also brought up the general architecture and mentioned the implementation issue of particular characteristics of the mainframe.

FREQUENTLY ASK QUESTIONS (FAQ)

1. **What is a Mainframe?**

   Mainframe is a very huge and expensive computer that can support hundreds or even thousands of users at the same time.

2. **What is the use of Mainframe?**

   Mainframe is used to perform large-scale data processing such as enterprise transaction processing. It is capable of handling and performing thousands of data per second.

3. **What the different between a Mainframe and a General Computer?**

   A Mainframe is a large and expensive computer housed in a controlled environment that capable of supporting at least hundreds of users simultaneously while a General Computer is smaller, cheaper and undoubtedly used by only one person at a time.

4. **What type of operating system can be installed on a Mainframe?**

   UNIX, Linux variants or any versions of IBM's zOS operating system but it usually depends on the manufacturer of the Mainframe.

5. **Does a normal person own or use a Mainframe?**

   No. It usually owned and used by organizations to process and handle a large amount of data efficiently.

6. **What kind of organizations used Mainframe?**

   Mainframe is used by banks, hospitals, financial, insurance and other enterprise.

7. **Why most of the organizations choose a Mainframe instead of a general computer?**

   One of the main reason is mainframe has a high-level security system that can secure and protect the data from intruders or viruses.

8. **What are the advantages of using Mainframe?**

   It can manage huge amounts of data more reliable and secure than a client-server network.

9. **Are there any disadvantages of using a Mainframe?**

   Yes. It requires staffs with specific skills to run the system and the cost of a Mainframe is relatively high.

MINUTES OF MANDATORY MEETINGS

Minutes of Meeting 1

1st Fortnight Report

VENUE	START TIME	END TIME	DATE
Syndicate Room	4:00 PM	4:30 PM	03/08/2015

MEMBERS NAME	INTAKE NUMBER	ATTENDANCE	SIGNATURE
Albert Tan Choo Sheng	TP035578	Present	
Low Yiyiu	TP035403	Present	
Ng Hui Cheng	TP036501	Present	

What have we done?

Team members have been selected.

What are we doing?

We are gathering up to arrange our time schedule for next few weeks assignment meetings.

What will we do?

We will read our assignment questions and learn about mainframe.

Minutes of Meeting 2

2nd Fortnight Report

VENUE	START TIME	END TIME	DATE
Syndicate Room	4:00 PM	5:00 PM	17/08/2015

MEMBERS NAME	INTAKE NUMBER	ATTENDANCE	SIGNATURE
Albert Tan Choo Sheng	TP035578	Present	
Low Yiyiu	TP035403	Absent with reason	
Ng Hui Cheng	TP036501	Present	

What have we done?

We have started to read the assignment question and learnt the basic knowledge of a mainframe.

What are we doing?

We are discussing the selection of mainframes and the work breakdown structure.

What will we do?

We will do a deep research and study on the selected mainframe (IBM zEC12).

Minutes of Meeting 3

3rd Fortnight Report

VENUE	START TIME	END TIME	DATE
Syndicate Room	4:00 PM	6:00 PM	14/09/2015

MEMBERS NAME	INTAKE NUMBER	ATTENDANCE	SIGNATURE
Albert Tan Choo Sheng	TP035578	Present	
Low Yiyiu	TP035403	Present	
Ng Hui Cheng	TP036501	Present	

What have we done?

We have done researching and studying on the selected mainframe (IBM zEC12).

What are we doing?

We are gathering all the information gained from our research and summarized the results in the document.

What will we do?

We will do the final checking to make sure that we have fulfilled the assignment requirements before we submit the document.

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