KADI SARVA VISHWAVIDHYALAYA

BE III Semester Examination Dec 2023

Sub code: CT- 304-N **Sub Name: Digital Electronics**

Date: 27/12/2023 **Time:12:00 A.M to 3:00 P.M** **Total Marks:70**

Instructions:

1. Answer Each Section in Separate Answer sheet.
2. Use of Scientific Calculator is permitted. .
3. All questions are separate
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of supplementary for rough work.

SECTION I

Q.1 (a)	Convert the following numbers from the given base to the bases indicated. a) decimal 225.225 to binary, octal and hexadecimal b) binary 11010111.110 to decimal, octal and hexadecimal	**[05]**
(b)	Perform the subtraction with the following binary numbers using 2's and 1's complement a) 11010-1101 b) 11010-10000	**[05]**
(c)	Convert the decimal number 250.5 to Base 3, Base 4	**[05]**
	OR	
(c)	Explain error detection and correction codes.	**[05]**
Q.2 (a)	Find the complement of the following Boolean functions and reduce them to a minimum number of literals. a) (BC' + A'D) (AB' + CD') b) B'D + A'BC' + ACD + A'BC	**[05]**
(b)	Express the following functions in a sum of minterms and a product of maxterms F (A, B, C, D) = D(A'+B) + B'D	**[05]**
	OR	
Q.2 (a)	Obtain the truth table of the function. F = xy + xy' + y'z	**[05]**
(b)	Simplify the Boolean function F in sum of products using the don't- care conditions. a) F = y' + x'z' d = yz + xy	**[05]**
Q-3 (a)	Explain Full Adder in detail	**[05]**
(b)	Simplify the following Boolean function by using the tabulation method (QuineMcCluskey method). F = $\sum$ (0,1,2,8,10,11,14,15)	**[05]**
	OR	
Q-3 (a)	Explain: NAND and NOR implementation as an universal gate	**[05]**
(b)	Explain BCD to Excess-3 code conversion	**[05]**

SECTION II

Q.4 (a)	Write a short note on Shift Registers.	[05]
(b)	Explain Binary parallel adder	[05]
(c)	Comparison between multiplexer and de-multiplexer.	[05]
	OR	
(c)	Explain J-K Flip Flop in detail	[05]
Q.5 (a)	Explain Counter type A/D Converter.	[05]
(b)	Explain Flash Type A/D converter.	[05]
	OR	
Q.5 (a)	Explain BCD ripple counter in detail.	[05]
(b)	What do you mean by the Moore model and the Melay model of the state diagram? Draw Moore model for D flip flop	[05]
Q-6 (a)	Explain the Programmable Array Logic (PAL).	[05]
(b)	Explain D/A converter binary Weighted Resistor.	[05]
	OR	
Q-6 (a)	Write a short note on Read only memory (ROM).	[05]
(b)	What is the full form of PLD? Explain different types of PLD's in detail.	[05]

KADI SARVA VISHWAVIDHYALAYA

BE Semester III

Examination November /December – 2023

Sub Name: Digital Electronics
Sub code: CT 304 N
Date: 18/12/2023

Time: 12:00 pm to 03:00 pm
Total Marks: 70

Instructions:

1. Answer Each Section in a Separate Answer sheet.
2. Use of Scientific Calculator is permitted. .
3. All questions are separate
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of supplementary for rough work.

SECTION I

Q.1 (a)	Convert $(4F7.A8)_{16}$ to octal,binary & decimal.	[05]
(b)	Perform the subtraction with the following decimal numbers using 10's and 9's complement : 5250-321	[05]
(c)	Represent the decimal number 8620 in BCD,Excess-3 code,2,-4-2-1 code,Binary number & Gray Code	[05]
	OR	
(c)	Simplify the following Boolean functions to a maximum number of literals a) XY+XY' b) (X+Y) (X+Y')	[05]
Q.2 (a)	Implement Boolean function with only OR and NOT Gates. F = xy + x'y' + y'z	[05]
(b)	Simplify the following Boolean function by using K-MAP method. F = $\sum$ (0,1,2,8,10,11,14,15)	[05]
	OR	
Q.2 (a)	State and explain DeMorgan's law.	[05]
(b)	Obtain the simplified expressions in the product of sums. F (A,B,C,D) = $\prod$ (0, 1, 2, 3, 4, 10, 11)	[05]
Q-3 (a)	Explain In Detail with necessary diagram:Implementation of NAND as an universal gate.	[05]
(b)	Define & explain Multiplexer in detail.	[05]
	OR	
Q-3 (a)	Write a short note on BCD adder with necessary diagram.	[05]
(b)	Differentiate between encoder and decoder.	[05]

SECTION II

Q.4 (a)	Draw and explain Binary parallel adder with necessary logic diagram.	[05]
(b)	Explain J-K Flip Flop in with truth table & logic diagram.	[05]
(c)	Explain the Excitation table of S-R flip-flop in detail.	[05]
	OR	
(c)	Draw & explain 4- bit shift register.	[05]
Q.5 (a)	Define a synchronous counter and explain the 4-bit synchronous counter in detail.	[05]
(b)	Draw & explain 4-bit BCD counter.	[05]
	OR	
Q.5 (a)	Draw Mealy model for D flip flop.	[05]
(b)	Write a short note on Read only memory (ROM).	[05]
Q-6 (a)	Explain the Programmable Array Logic (PAL).	[05]
(b)	Explain D/A converter R-2R Ladder circuits.	[05]
	OR	
Q-6(a)	Explain Counter type A/D Converter.	[05]
(b)	Explain Flash Type A/D converter.	[05]

KADI SARVA VISHWAVIDYALAYA

B.E. Semester III EXAMINATION (Nov/Dec-2022)

Subject Code: CT304-N **Subject Name: Digital Electronics**
Date: 16/12/2022 **Time:10:00am to 1:00pm** **Total Marks: 70 Marks**

Instructions:
1. **All questions are compulsory.**
2. **Figures to the right indicate full marks.**
3. **Use of scientific calculator is permitted.**
4. **Indicate clearly, the options you attempt along with its respective question number.**
5. **Use the last page of main supplementary for rough work.**

Section-I

Q:1 Attempt Following.

(A) Explain excess-3 code in detail. [5]
(B) Explain D'Morgan's theorems in detail. [5]
(C) Convert the binary 1001 to gray code. [5]

OR

Q:1 (C) Convert hexadecimal 2AC5.D to decimal and octal. [5]

Q:2 Answer the following question.

(A) Implement following Boolean function using only AND and NOT gates. [5]
F=x'z'+y'z'+yz'+xyz
(B) Simplify following Boolean function using tabulation method. [5]
$F=\sum(0,1,2,8,10,11,14,15)$

OR

Q:2 (A) Obtain the simplified expressions in product of sums. [5]
$F(A,B,C,D)=\pi(0,1,2,3,4,10,11)$
(B) Prove that complement of EX-OR gate is result in EX-NOR gate. [5]

Q:3 Answer the following question.

(A) Write a short note about full subtractor with neat diagram. [5]
(B) Write a short note about decoder. [5]

OR

Q:3 (A) Design a combinational circuit to convert BCD code to excess-3 code converter. [5]
(B) Write a short note about multiplexer. [5]

Section II

Q:4 Attempt following.

(A) Write a short note about D flip flop with neat diagram. [5]

(B) Write down comparison between combinational circuits and sequential circuits. [5]

(C) Explain logic diagram of master-slave flipflop. [5]

OR

Q:4 (C) Write a short note about bidirectional shift register with parallel load with neat diagram. [5]

Q:5 Answer the following question.

(A) Write a short note about 4 bit binary ripple counter. [5]

(B) Explain state diagram of JK flipflop. [5]

OR

Q:5 (A) Write definitions about state table and state diagram. [5]

(B) What is ROM? Explain types of ROM memory. [5]

Q:6 Answer the following question.

(A) Explain difference between PLA and PAL. [5]

(B) Explain a short note about R-2R ladder type DAC. [5]

OR

Q:6 (A) Write down a short note about flash type ADC. [5]

(B) Write down a short note about successive approximation type ADC. [5]

KADI SARVA VISHWAVIDHYALAYA
BE SEMESTER III EXAMINATION JAN 2022

Sub code: CT304-N **Sub Name: Digital Electronics**

Date: 11/06/2022 **Time: 12:30 PM to 03:30 PM** **Total Marks: 70**

Instructions:

1. Answer Each Section in Separate Answer sheet.
2. Use of Scientific Calculator is permitted.
3. All questions are compulsory.
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of supplementary for rough work.

SECTION I

Q.1 (a) (1) $(64)_{10}=(?)_2$ (2) $(100100)_2=(?)_{10}=(?)_8$ (3) $(153)_8=(?)_2=(?)_{16}$ **[05]**

(b) Explain any five Logical Gates. **[05]**

(c) Explain Duality Law with example. **[05]**

OR

(c) Perform the subtraction with the following decimal numbers using A) 10's and B) 9's complement. **[05]**

3570-2100.

Q.2 (a) Convert the following to the other canonical form: **[05]**

$F(A,B,C,D)=\sum(0,1,2,3,7,8,11,12,15)$

(b) Explain Different forms of Boolean Expression with example. **[05]**

OR

Q.2 (a) Convert the function into product of max terms: xy+x'z **[05]**

(b) Prove following Boolean functions using theorems and postulates: **[05]**

(1) xyz+x'y+xyz' = y (2) xy+x'z+yz = xy+x'z

Q-3 (a) Simplify the Boolean function with k-map **[05]**

$F(x,y,z)=\sum(3,4,6,7)$

(b) Design Full-adder. **[05]**

OR

Q-3 (a) Explain 4-bit Binary Parallel adder. **[05]**

(b) Compare combinational circuit and sequential circuit. **[05]**

SECTION II

Q.4 (a)	Explain 3 to 8 line Decoder with necessary diagram.	[05]
(b)	Design Full Adder with use of Decoder.	[05]
(c)	Implement the following function with a multiplexer: $F(A,B,C)=\sum(1,2,7)$	[05]

OR

(c)	Explain R-S Flip-Flop.	[05]
Q.5 (a)	Explain 4 to 1 line multiplexer.	[05]
(b)	Explain BCD Ripple Counter.	[05]

OR

Q.5 (a)	Explain T Flip-Flop	[05]
(b)	Explain Serial in/Parallel out shift register with necessary diagram.	[05]
Q-6 (a)	Explain PLA.	[05]
(b)	Explain 4-bit synchronous binary counter.	[05]

OR

Q-6(a)	Explain Binary weighted resistor D/A converter.	[05]
(b)	Explain Moore State Machine.	[05]

KADI SARVA VISHWAVIDYALAYA
B.E.(CE/IT/CSE) SEMESTER 3rd EXAMINATION MARCH 2022

SUBJECT CODE: CT-304-N
SUBJECT NAME : DIGITAL ELECTRONICS
DATE: 03/03/2022 **TIME: 11.00 PM TO 02.00 PM** **TOTAL MARKS: 70**

Instructions:
1. Answer Each Section in Separate Answer sheet.
2. Use of Scientific Calculator is permitted.
3. All questions are compulsory.
4. Indicate **clearly**, the options you attempted along with its respective question number.
5. Use the last page of supplementary for rough work.

SECTION-1

Q.1	(A)	Convert $(96)_{10}$ to its equivalent gray code and EX-3 code.	[05]
	(B)	Convert 1000 0110 (BCD) to decimal, binary Hexadecimal & octal.	[05]
	(C)	State & prove De Morgan's theorems with the help of truth tables.	[05]
		OR	
	(C)	Using laws of Boolean algebra prove that AB + BC + A'C = AB + A'C.	[05]
Q.2	(A)	Minimize the following Boolean expression using Karnaugh Map (K-MAP) and Draw the simplified logic circuit diagram. $Y = \sum m(0,1,5,9,13,14,15) + d(3,4,7,10,11)$	[05]
	(B)	Discuss NAND gate as universal gate (implement NOT, AND, OR & NOR gate using NAND gate).	[05]
		OR	
Q.2	(A)	Design 3-bit even parity generator circuit.	[05]
	(B)	Draw the truth table of full subtractor and implement using minimum number of logic gates	[05]
Q-3	(A)	Design a BCD to excess 3 code converter using minimum number of gates.	[05]
	(B)	Distinguish between combinational and Sequential logic circuits	[05]
		OR	
Q-3	(A)	Implement 16 X 1 multiplexer using 2 X 1 multiplexers.	[05]
	(B)	Draw logic diagram of 3-line to 8-line decoder.	[05]

SECTION-2

Q.4	(A)	Draw logic circuit of Full Adder with truth table.	[05]
	(B)	Obtain canonical Sum of ~~Product~~ Minterms form of following function: F=AB+ACD	[05]
	(C)	Explain SR latch using NAND gates only.	[05]
		OR	
	(C)	Draw logic circuit for 2-Bit Magnitude Comparator.	[05]
Q.5	(A)	Implement the following function with NAND and NOR Gate. $F(a,b,c) = \Sigma (0,6)$	[05]
	(B)	Explain 3-bit synchronous Binary Up counter with timing diagram.	[05]
		OR	
Q.5	(A)	Explain D flip flop.	[05]
	(B)	With neat sketch design 4-bit bidirectional shift register	[05]
Q-6	(A)	Design a Synchronous counter to generate the repetitive sequence 0, 3, 5, 7, 4 using D FFs.	[05]
	(B)	List out the different methods of A To D converter. Explain any one in details.	[05]
		OR	
Q-6	(A)	Write short note on Programmable Logic Arrays.	[05]
	(B)	Design a Synchronous counter for following binary sequence 0-1-3-4-6-0.	[05]

KADI SARVA VISHWAVIDHYALAYA
BE SEMESTER III EXAMINATION JAN 2022

Sub code: CT304-N **Sub Name: Digital Electronics**

Date: 21 /01/2022 **Time: 12:30 PM to 03:30 PM** **Total Marks: 70**

Instructions:

1. Answer Each Section in Separate Answer sheet.
2. Use of Scientific Calculator is permitted.
3. All questions are compulsory.
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of supplementary for rough work.

SECTION I

Q.1 (a) (1) $(123)_{10}=(?)_2$ (2) $(101011)_2=(?)_{10}=(?)_8$ (3) $(153)_{10}=(?)_8=(?)_{16}$ **[05]**

(b) Justify the statement: "NAND Gate is universal gate". **[05]**

(c) Explain Gray Code. **[05]**

OR

(c) Prove (1) x+x=x (2) x+xy=x using postulates and theorems. **[05]**

Q.2 (a) Convert the following to the other canonical form: **[05]**
$F(A,B,C,D)=\sum(1,2,3,6,11,13,14)$

(b) Express following function in a sum of minterms and a product of maxterms **[05]**
F(A,B,C)=A+B'C.

OR

Q.2 (a) Show that the dual of the exclusive-OR is equal to its complement. **[05]**

(b) Simplify following Boolean functions using theorems and postulates: **[05]**
(1) A+B[AC+(B+C')D] (2) (B+BC)(B+B'C)(B+D)

Q-3 (a) Simplify the Boolean function with k-map **[05]**
$F(w,x,y,z)=\sum(0,1,2,4,5,6,8,9,12,13,14)$

(b) Design half-subtractor and full-subtractor. **[05]**

OR

Q-3 (a) Determine the prime-implicants of the function: **[05]**

$F(w,x,y,z)=\sum(1,4,6,7,8,9,10,11,15)$

(b) Explain 3 to 8 line Decoder with necessary diagram. **[05]**

SECTION II

Q.4 (a)	Compare combinational circuit and sequential circuit.	[05]
(b)	Explain magnitude comparator.	[05]
(c)	Implement the following function with a multiplexer: $F(A,B,C)=\sum(1,3,5,6)$	[05]

OR

(c)	Explain 4 to 1 line multiplexer.	[05]
Q.5 (a)	Explain D Flip-Flop	[05]
(b)	Explain 4-bit ripple binary counter with J-K Flip-Flop	[05]

OR

Q.5 (a)	Explain JK Flip-Flop	[05]
(b)	Explain Serial in/Serial out shift register with necessary diagram.	[05]
Q-6 (a)	Explain ROM.	[05]
(b)	Explain 4-bit synchronous binary counter.	[05]

OR

Q-6(a)	Explain R-2R Ladder Type DAC.	[05]
(b)	Explain PLA using suitable example.	[05]
