KADI SARVA VISHWAVIDHYALAYA

BE Semester III

Examination November /December – 2023

Sub Name: Digital Electronics
Sub code: CT 304 N
Date: 18/12/2023

Time: 12:00 pm to 03:00 pm
Total Marks: 70

Instructions:

1. Answer Each Section in a Separate Answer sheet.
2. Use of Scientific Calculator is permitted. .
3. All questions are separate
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of supplementary for rough work.

SECTION I

Q.1 (a)	Convert $(4F7.A8)_{16}$ to octal,binary & decimal.	**[05]**
(b)	Perform the subtraction with the following decimal numbers using 10's and 9's complement : 5250-321	**[05]**
(c)	Represent the decimal number 8620 in BCD,Excess-3 code,2,-4-2-1 code,Binary number & Gray Code	**[05]**
	OR	
(c)	Simplify the following Boolean functions to a maximum number of literals a) XY+XY' b) (X+Y) (X+Y')	**[05]**
Q.2 (a)	Implement Boolean function with only OR and NOT Gates. F = xy + x'y' + y'z	**[05]**
(b)	Simplify the following Boolean function by using K-MAP method. F = $\sum$ (0,1,2,8,10,11,14,15)	**[05]**
	OR	
Q.2 (a)	State and explain DeMorgan's law.	**[05]**
(b)	Obtain the simplified expressions in the product of sums. F (A,B,C,D) = $\prod$ (0, 1, 2, 3, 4, 10, 11)	**[05]**
Q-3 (a)	Explain In Detail with necessary diagram:Implementation of NAND as an universal gate.	**[05]**
(b)	Define & explain Multiplexer in detail.	**[05]**
	OR	
Q-3 (a)	Write a short note on BCD adder with necessary diagram.	**[05]**
(b)	Differentiate between encoder and decoder.	**[05]**

SECTION II

Q.4 (a)	Draw and explain Binary parallel adder with necessary logic diagram.	[05]
(b)	Explain J-K Flip Flop in with truth table & logic diagram.	[05]
(c)	Explain the Excitation table of S-R flip-flop in detail.	[05]
	OR	
(c)	Draw & explain 4- bit shift register.	[05]
Q.5 (a)	Define a synchronous counter and explain the 4-bit synchronous counter in detail.	[05]
(b)	Draw & explain 4-bit BCD counter.	[05]
	OR	
Q.5 (a)	Draw Mealy model for D flip flop.	[05]
(b)	Write a short note on Read only memory (ROM).	[05]
Q-6 (a)	Explain the Programmable Array Logic (PAL).	[05]
(b)	Explain D/A converter R-2R Ladder circuits.	[05]
	OR	
Q-6(a)	Explain Counter type A/D Converter.	[05]
(b)	Explain Flash Type A/D converter.	[05]
