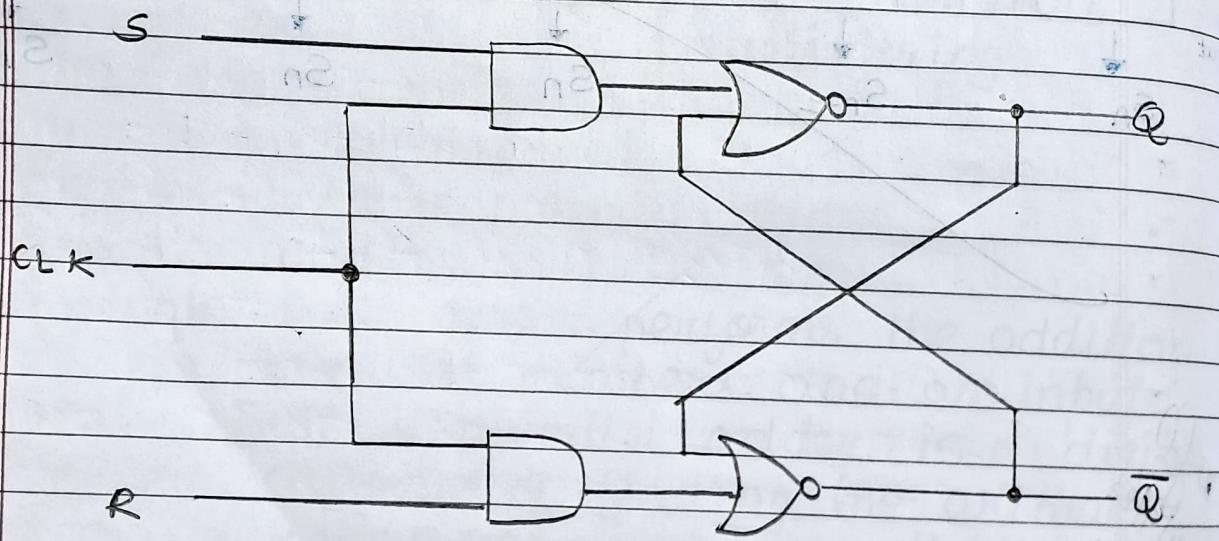


## Assignment - 4

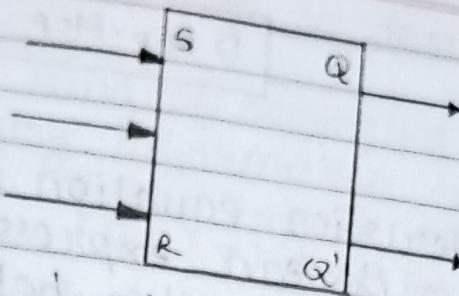
### Flip Flops and Sequential Logic and Circuit

★ Explain R-S Flip Flop in detail.

→ The SR flip-flop is also named as RS flip flop. When both the inputs of the SR flip-flop are high, then the indeterminate state is there. In other programming environments, it is required to assign determinate outputs to all flip flop condition. Hence, RS and SR flip-flops were designed. The clocked SR flip-flop is shown below.



- SR flip flop is used as a storage device for a single data bit.
- Symbol for R-S or SR flip flop is drawn further.



- Truth Table of SR Flip Flop is drawn below :

S	R	$Q_{n+1}$	State
0	0	$Q_n$	Hold
0	1	0	Reset
1	0	1	Set
1	1	X	Invalid

Here, S is the set input, R is the reset input,  $Q_{n+1}$  is the next state and state tells in which state it enters.

- ★ Explain D Flip Flop in detail.

→ D flip flop is an electronic devices that is known as "delay flip flop" OR "data flip flop" which is used to store single bit of data. D flip flops are asynchronous. The clock signal required for the asynchronous version of D flip flops but not for the synchronous one. The D flip flop has two inputs, data and clock input which controls the flip flop. When clock is high (input), the data is transferred to the output of the flip flop and when the clock is low (input), the output of the flip flop is held in its previous state.

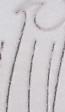
## D FLIP - HOP

- The characteristics equation of D flip flop consist of a Boolean expression that explains the relationship between the input and output of the flip flop. The characteristic equation for a D flip flop is as follows.

$$Q(n+1) = D(n)$$

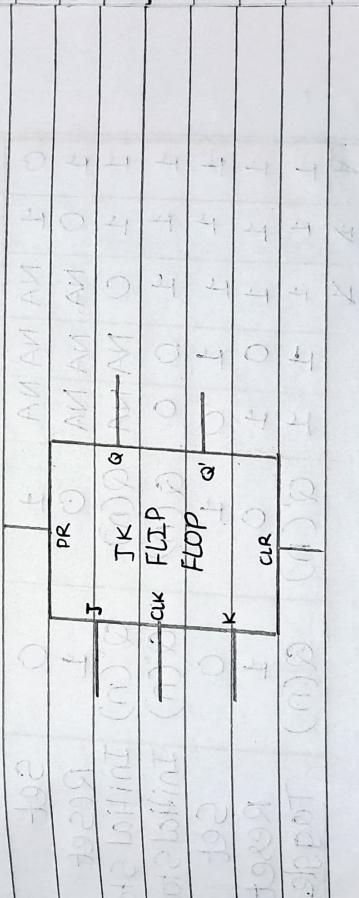
### Advantages of D Flip Flop.

- 1] D flip flop is very simple to design.
- 2] The computation speed of D flip flop is very fast compared to other flip flops.
- Disadvantages of D Flip Flop.
- 1] D flip flops are glitch prone. When input varies fast, flip flop output may glitch. Digital circuit glitches are hard to identify and fix.
- Types of D Flip Flop.
  - 1] D latch
  - 2] Edge Triggered D Flip Flop.

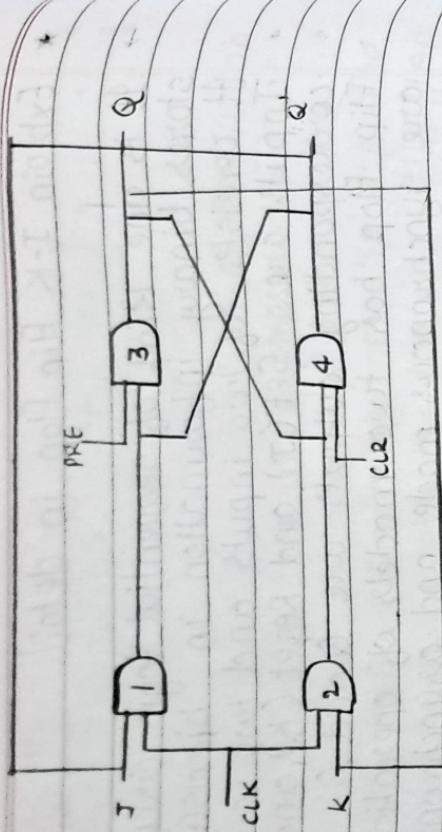


## Explain JK Flip Flop in detail.

- It is one kind of sequential logic circuit which stores binary information in bit wise manner.
- It consists of two inputs and two outputs.
- Inputs are Set (S) and Reset (R) and their corresponding outputs are Q and Q'.
- JK Flip Flop has two modes of operation which are synchronous mode and asynchronous mode.
- In synchronous mode, the state will be changed with the clock signal, and in asynchronous mode, the change of state is independent from its clock signal.



- Below is the circuit diagram of JK Flip Flop. Two 3-input NAND gates are used in place of the original two 2-input AND gates. The outputs at Q and Q' are coupled to each gate's third input. Since the two inputs are now interlocked, the SR flip-flops for cross coupling enables the previously invalid condition of (S="1", R="1") to be employed to perform the "toggle" action.

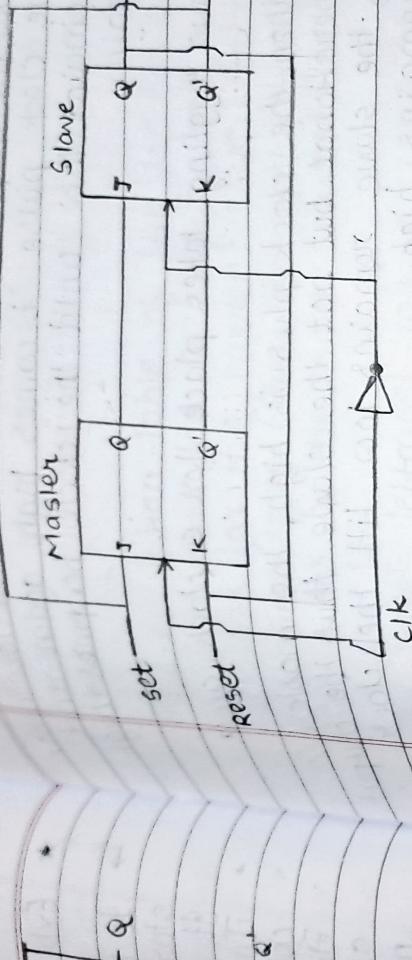


- Truth-Table of JK flip flop is given below:

INPUTS		OUTPUTS			Comments
PR	CUR	J	K	$Q(n+1)$	
0	1	NA	NA	1	0 Set
1	0	NA	NA	0	1 Reset
1	1	0	NA	$Q(n)$	$Q'(n)$ Initial Stage
1	1	1	0	$Q(n)$	$Q'(n)$ Initial Stage
1	1	1	1	0	0 Set
1	1	1	0	1	0 Reset
1	1	1	1	$Q(n)$	$Q'(n)$ Toggle
X	X	X	X	X	X

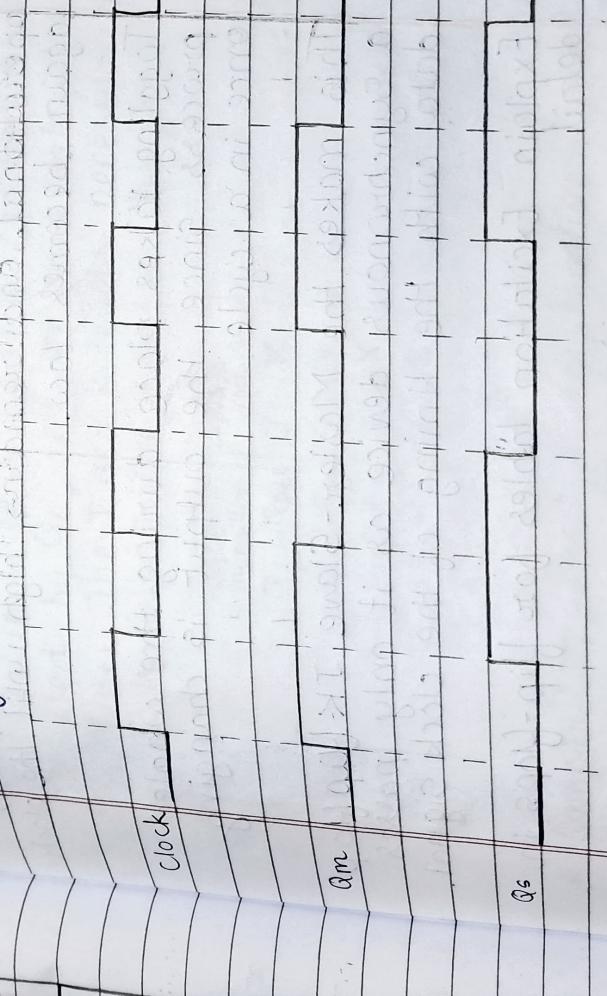
- Explain Master Slave Hip Hop in details.

- The Master Slave flip flop is basically a combination of two JK flip flops connected together in a series configuration. Out of these, one acts as the "master" and the other as a "slave".

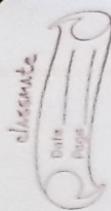


Qs:

• Timing Diagram of a Master-Slave Flip-flop.



- 1 When the clock pulse is high the output of master is high and remains high till the clock is low because the state is stored.



2) Now the output of master becomes low when the clock pulse becomes high again and remains low until the clock becomes high again.

3) Thus toggling takes place for a clock cycle.

4) When the clock plus is high, the master is operational but not the slave. Thus the output of the slave remains low till the clock remains high.

5) When the clock is low, the slave becomes operational and remains high until the clock again becomes low.

6) Toggling takes place during the whole process since the output is changing once in a cycle

- This makes the Master-Slave JK flip-flop a synchronous device as it only passes data with the timing of the clock signal.

\* Explain Excitation tables for flip-flops in detail.

→ The flip-flop must be excited by the excitation table to move from its current state to next one. It was created by using the truth table. In general, the truth table is used to illustrate how each flip-flop works.

The truth table contains all the input combinations that cause the Flip-flop to react when output the following state.

and high

- The excitation table of flip flop has one or two columns for each input and two columns for the current state ( $Q_n$ ) and the following state ( $Q_{n+1}$ ). The type of flip-flop determines by the input columns.

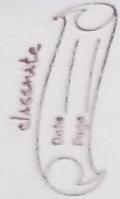
- This table's leftmost column contains a list of all feasible FF output transitions in the flip-flop excitation table. For each transition, this column lists the FF's CURRENT state, denoted by  $Q_n$ , and the NEXT state, denoted by  $Q_{n+1}$ . The J and K levels necessary for each transition are listed in the final column.

Output Transition	Flip-Flop inputs		
$Q_n$	$Q_{n+1}$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- Comparison between combinational logic and sequential logic circuit.

OR

Write difference between combinational logic and sequential logic circuit.



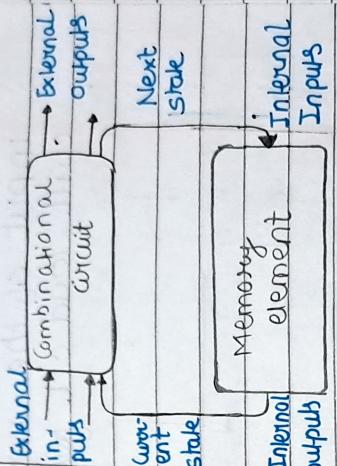
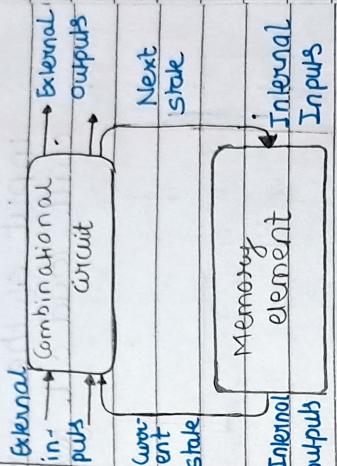
## COMBINATIONAL CIRCUIT

### SEQUENTIAL CIRCUIT

- In this output depends on this output depends upon present as well as past input.
- Speed is fast
- It is designed easy.
- There is no feed back between input and output path between input and output.
- This is time independent
- Combinational circuits
- In this output depends only upon present as well as past input.
- Speed is slow
- It is designed tough as compared to combinational circuits.
- There exists a feedback path between input and output.
- This is time dependent
- Elementary building blocks : logic gates.
- Used for arithmetic operations as well as boolean operations storing data
- Sequential circuits
- As circuits are clock dependent they need triggering

- These circuits do not have any memory element
- It is easy to use and handle it is not easy to use and handle.

### Block Diagram



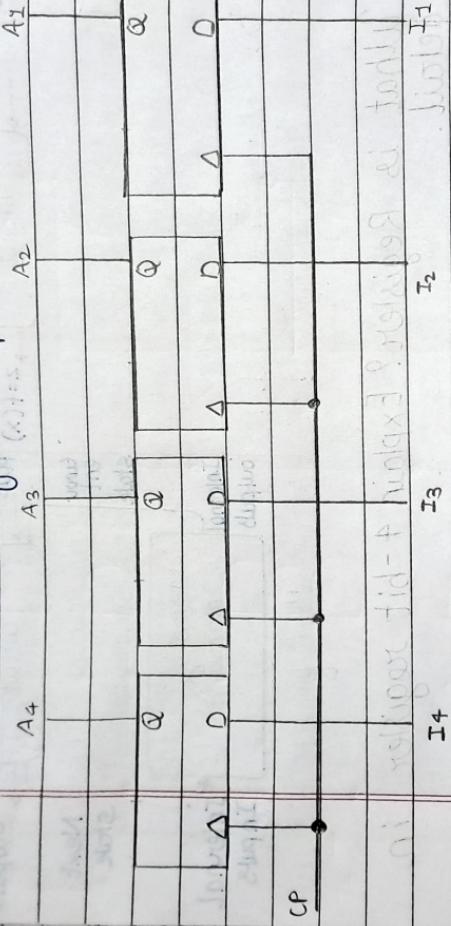
- Ques** ★ What is Register? Explain 4-bit register in detail.
- A register is a small and temporary storage unit inside a computer's central processing unit. Registers act as intermediate storage for data during arithmetic logic and other processing operations. It utilized for a variety of functions in handling and controlling instructions and data and play an important role in the operation of a computer's CPU.

Registers act as intermediate storage for data during arithmetic logic and other processing operations. It utilized for a variety of functions in handling and controlling instructions and data and play an important role in the operation of a computer's CPU.



- The clock pulse input, CP, enables all flip-flops so that the information present in the four inputs can be transferred into the 4-bit register.

- The transfer of new information into a register is referred to as loading the register. A pulse applied to the control input of the register of our 4-bit register will load all four inputs in parallel.



- A 4-bit register with a load control input using RS flip-flops is shown in the above figure.

The common clock input triggers all flip-flops on the rising edge of each pulse, and the binary data available at the four inputs are transferred into the 4-bit register.

- The four outputs can be sampled at any

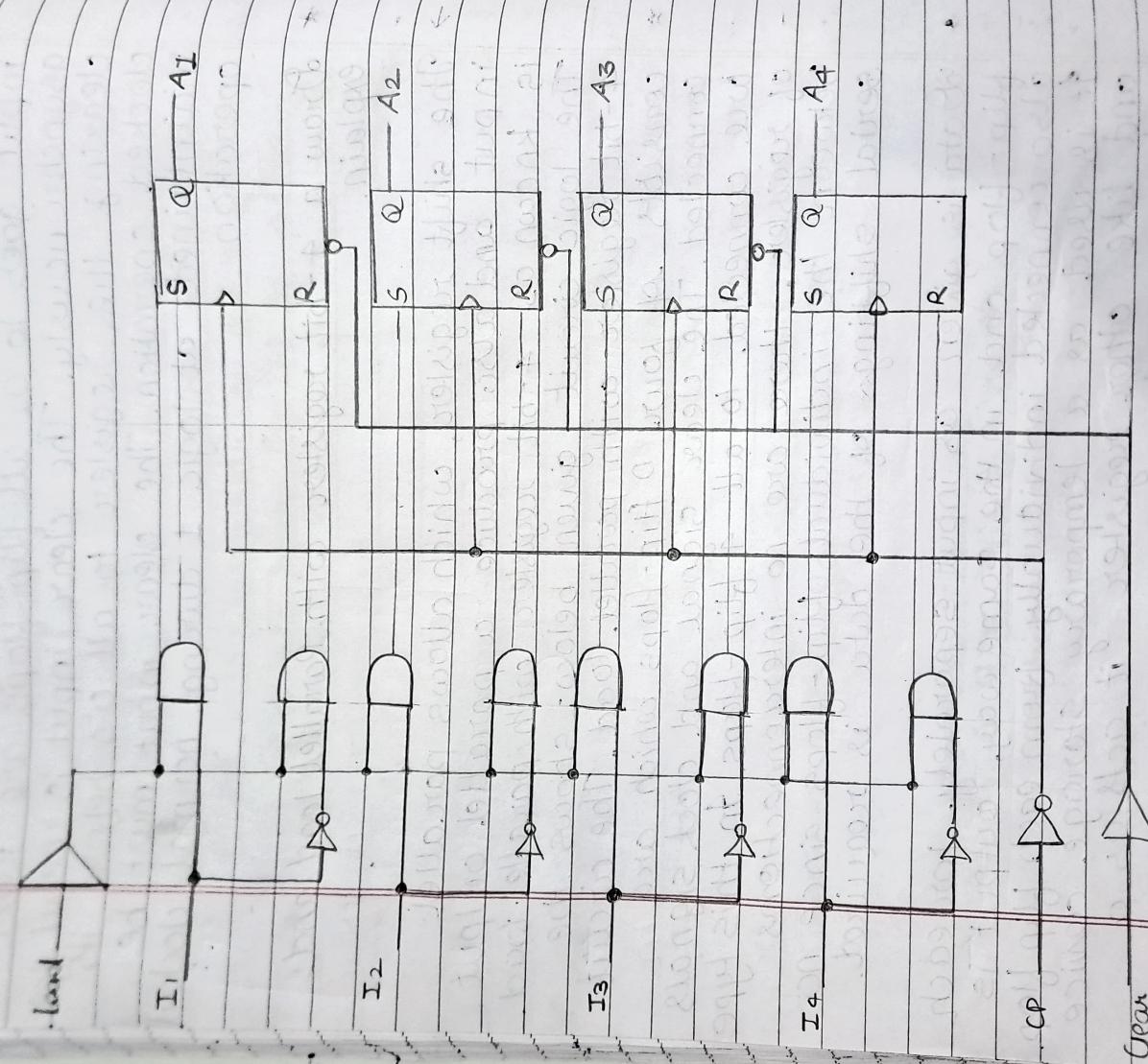
time to obtain the binary information stored in the register. The clear input goes to a special terminal in each flip-flop. When this input goes to 0, all flip-flops are reset asynchronously. The clear input is useful for clearing the register to all 0's before its clocked operation. The clear input must be maintained at logic 1 during normal clocked operation.

\* Draw a 4-bit register with parallel load and explain.

The shift register, which allows parallel input and also produce a parallel output is known as 4-bit register with parallel load. The logic circuit given below shows the 4-bit register with parallel load. The circuit consists of four D flip-flops which are connected. The clear signal and clock signals are connected to all 4 flip-flops. In this type of register, there are no interconnections between the individual flip-flops since no serial shifting of the data is required.

Data is given as input separately for each flip-flop and in the same way, output is also connected individually from each flip-flop. It is used as a temporary storage device and like other register it acts as a delay element.

- Circuit diagram of 4-bit register with parallel load is drawn below.



## Write a short note on Shift Registers.

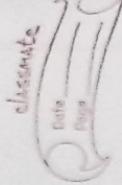
- Flip Flops can be used to store a single bit of binary data. N flip flops are to be connected in order to store n bits of data. A register is a device that is used to store such information. It is a group of flip-flops connected in series used to store multiple bits of data. The information stored within these registers can be transferred with the help of shift registers.

- Shift register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip-flop stores a single bit of data.

- The registers which will shift the bits to left are called "Shift left registers". The registers which will shift the bits to right are called "Shift right registers".

### Types of Shift Registers.

- 1) Serial In Serial Out shift register [SISO]
- 2) Serial In Parallel Out shift register [SIPO]



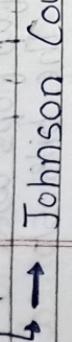
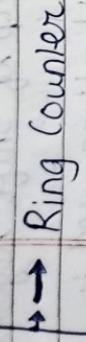
3) Parallel In Serial Out shift Register [PISO]

4) Parallel In Parallel Out shift Register [PIO]

5) Bidirectional shift register

6) Universal Shift register.

★ Shift register counter.



★ What is counter? Explain 4-bit binary ripple counter in detail.

→ A counter is a device which stores and sometime displays the number of times a particular event or process has occurred, often in relationship to a clock signal. The main properties of a counter are timing, sequencing, and counting. Counter works in two modes 1] Up counter 2] Down Counter.

→ 4-bit binary Ripple Counter

• The counter consists of four flip-flops and it can count 16 states. The clock pulse is given to the first flip flop and the normal output of the first flip flop is

3) Parallel In Serial Out shift Register [PISO]

4) Parallel In Parallel Out shift Register, [PIOPO]

5) Bidirectional Shift register

6) Universal Shift register.

7) Shift register counter.

→ Ring Counter

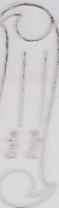
→ Johnson Counter

\* What is counter? Explain 4-bit binary ripple counter in detail.

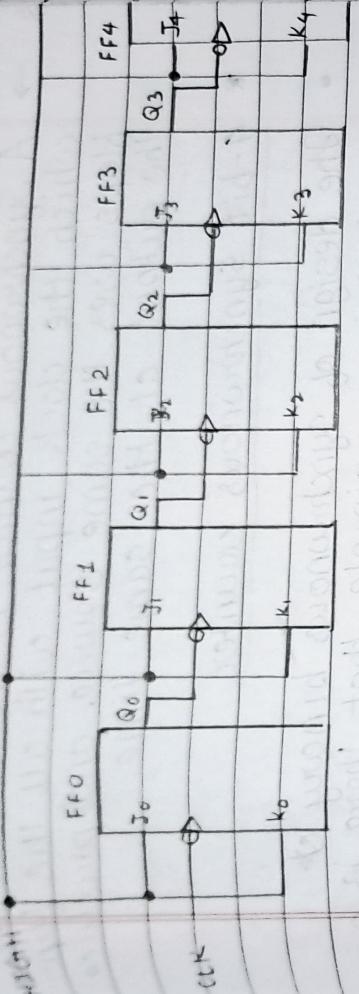
→ A counter is a device which stores and sometime displays the number of times a particular event or process has occurred, often in relationship to a clock signal. The main properties of a counter are timing, sequencing, and counting. Counter works in two modes  
1] Up counter  
2] Down Counter.

→ 4-bit binary Ripple Counter

The counter consists of four flipflops and it can count 16 states. The clock pulse is given to the first flip flop and the normal output of the first flip flop is



considered as the clock input of second flip flop and so on.



- The small circle in the CP input indicates that the flip-flop complements during a negative-going transition or when the output to which it is connected goes from 1 to 0. The lowest-order bit Q<sub>0</sub> must be complemented with each count pulse. Every time Q<sub>0</sub> goes from 1 to 0, it complements Q<sub>1</sub>. Every time Q<sub>1</sub> goes from 1 to 0, it complements Q<sub>2</sub> and so on.



Q<sub>0</sub>

Q<sub>1</sub>

Q<sub>2</sub>

Q<sub>3</sub>

Note :- In timing diagram Q<sub>0</sub> is changing as soon as the negative edge of clock pulse is encountered. Q<sub>1</sub> is changing when negative edge of Q<sub>0</sub> is encountered and so on.

★ Define a synchronous counter and explain 4-bit synchronous counter in detail.

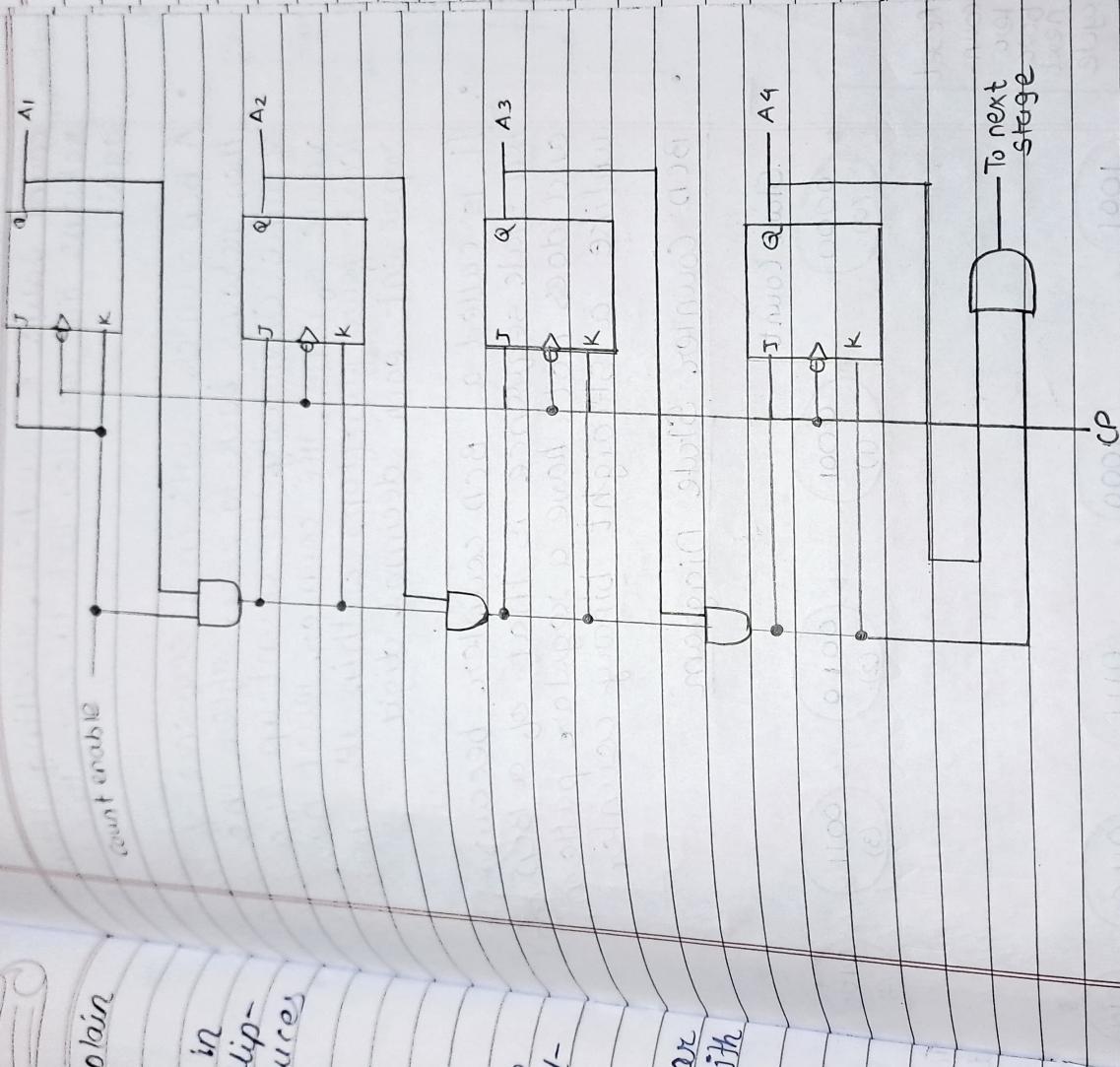
→ A Synchronous counter is the counter in which the clock input with all the flip-flops uses the same source, and produces the output at the same time.

#### \* 4-bit synchronous counter

- The design of synchronous binary counters is so simple, that there is no need to go through a rigorous sequential logic design process.
- Synchronous binary counters have a regular pattern and can easily be constructed with complementary flip-flops and gates. The regular pattern can be clearly seen from the 4-bit counter depicted in figure.
- The ce terminals of all flip-flops are connected to a common clock-pulse source. The other J and K inputs are equal to 1 if all previous low-order bits are equal to 1 and the count is enabled. The counter can be extended to any number of stages, with each stage having an additional flip-flop and an AND gate that gives an output of 1 if all previous flip-flop outputs are 1's.

classmate

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Explain

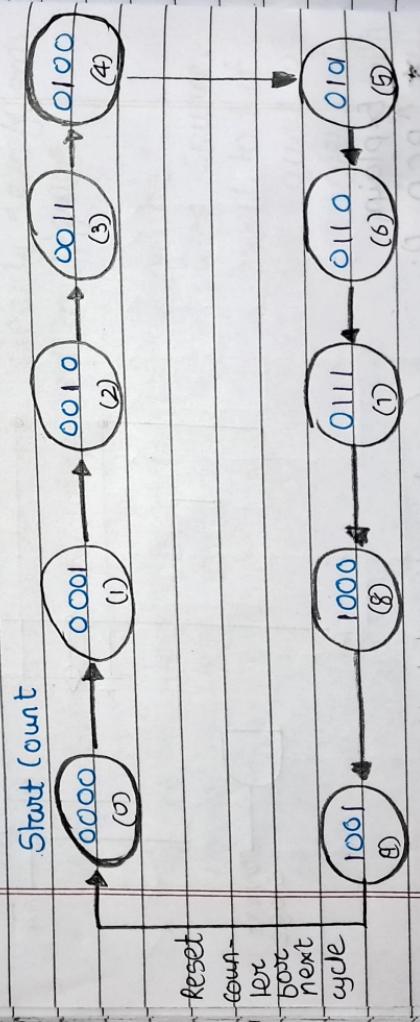
### \* BCD Ripper Counter in detail

- Digital counters count upwards from zero to some pre-determined count value on the application of a clock signal. Once the

count value is reached, resetting them returns the counter back to zero to start again.

- A BCD counter counts in a sequence of ten and then reverts back to zero after the count of nine. Obviously to count up to a binary value of nine, the counter must have at least four flip-flops within its chain to represent each decimal digit.
- It is called a BCD counter because its ten state sequence is that of a BCD code, and does not have a regular pattern, unlike a straight binary counter.

#### BCD Counter State Diagram



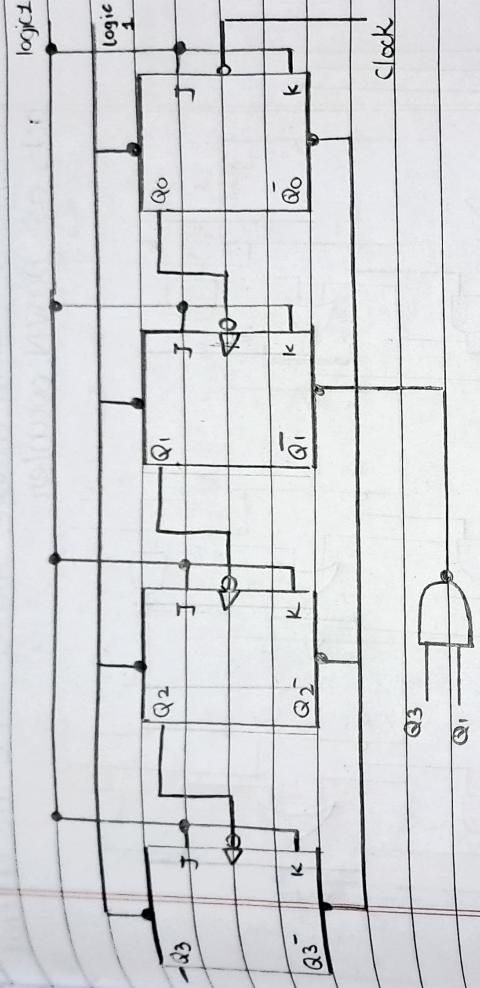
reset  
counter  
lock  
boot  
next  
cycle

- A decade counter has four flip-flops and 16 potential states, of which only 10 are used and if we connected a series of counters together we could count to



100 or 1000 or 10 whatever final count number we choose.

- Block Diagram of BCD ripple counter

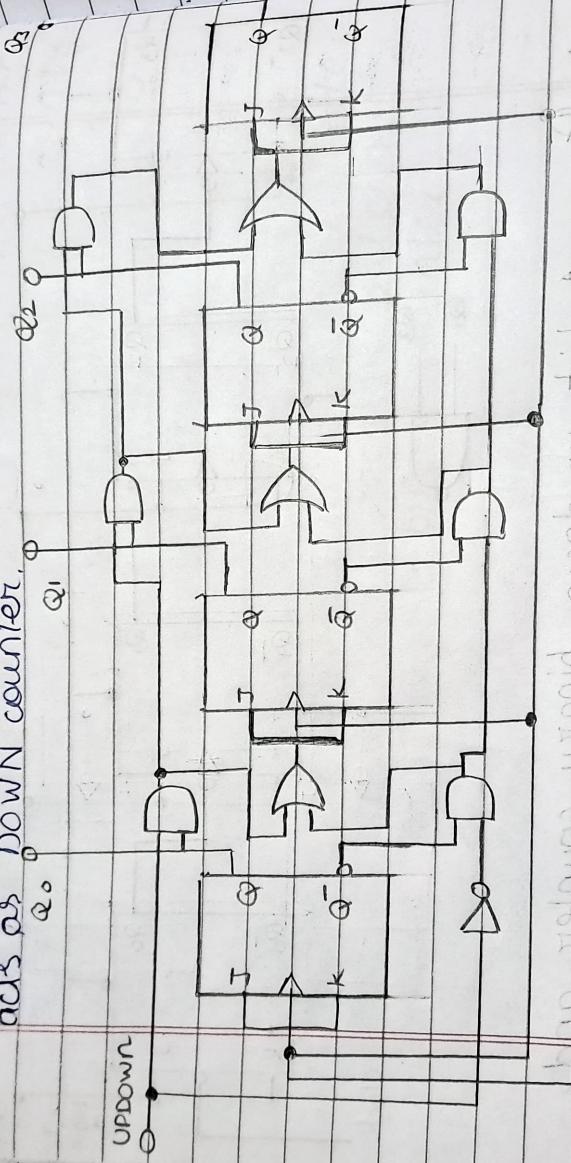


- ★ Draw 4-bit up-down binary counter and explain.

→ The up and down counters can be implemented in a single counter called up/down counter. This can be selected from its input.

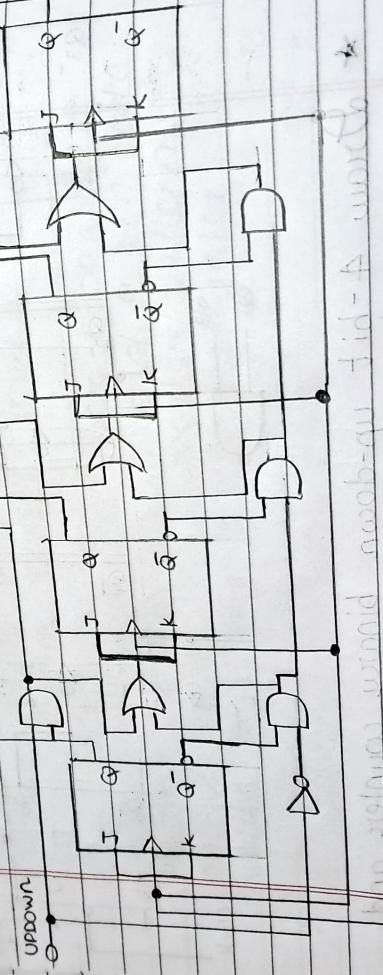
- The up/down counter has "Up" and "Down" count modes by having 2 input AND gates, which are used to detect the appropriate bit conditions for counting operation. OR gates are used to combine the outputs of AND gates, from each flip-flop.

- If the up/down control lines is set to High, Then the top AND gates are in enable state and the circuit acts as up counter. If the up/down control line is set to low, Then the bottom AND gate are in enable state and the circuit acts as down counter.



- We provide a up/down control line which enables upper or lower series of AND gates to pass the outputs of flip-flops,  $Q, Q'$  to the next stage of flip-flop, in the cascaded arrangement.

- If the control lines is set to enable state then the up/down control lines are in enable state. If the up/down AND gates are in up/down control lines are high, then the top AND gate acts as up counter from Q3 to Q0 and the circuit is set to low. Then the bottom AND gate acts as down counter.



- We provide a up/down control line which enables upper or lower series of AND gates to pass the outputs of flip flops,  $Q$ ,  $Q'$  to the next stage of flip-flop, in the cascaded arrangement.