

**ARM<sup>®</sup> Cortex<sup>®</sup>-M0**  
**32-bit Microcontroller**

**NuMicro<sup>®</sup> Family**  
**NUC100 Series BSP**  
**Revision History**

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**Revision 3.00.004 (Released 2017-11-28)**


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1. Fixed USB driver issue with zero packet.
2. Modified MFP setting style.

**Revision 3.00.003 (Released 2017-10-24)**


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3. Added CLK\_SysTickLongDelay() for long delay.
4. Fixed PLL clock source selection bug in CLK\_SetCoreClock().
5. Fixed UART\_SelectLINMode() clear enable bit setting bug.
6. Fixed a bug of u32RptDescLen calculation in USB\_GetDescriptor().
7. Fixed clear Receive Line Status interrupt flag bug in UART\_ClearIntFlag().
8. Fixed wrong SC1 and SC2 clock source select shift position in MODULE constant definitions.
9. Removed some combinations of I2C control bit settings. To avoid STOP and START write to control bit at the same time.
10. Modified to disable debug message when enabling semihost without NuLink connected.
11. Revised I2C\_START(). When set STA bit, the SI doesn't need set at the same time.
12. Added new function to control SysTick and select SysTick clock source, CLK\_EnableSysTick() and CLK\_DisableSysTick().
13. Added constant define "CLK\_CLKSEL0\_STCLK\_S\_HCLK" in CLKSEL0 constant definitions for CLK\_EnableSysTick().
14. Added ADC\_MeasureVADD sample code.

**Revision 3.00.002 (Released 2015-05-12)**


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1. Fixed SC\_SET\_STOP\_BIT\_LEN define error in SC Driver.
2. Fixed all IAR samples to set entry point from \_\_iar\_program\_start to Reset\_Handler.
3. Fixed all samples that run faster than 50MHz. (NUC100 series only support up to 50MHz).
4. Fixed UART1->IRCR setting bug in IrDA\_FunctionTxTest().
5. Fixed Flush FIFO end test message print bug in the end of RS485\_9bitModeSlave().
6. Fixed the wrong shift position for HCLK divider in main() of SYS sample code.
7. Fixed PLLCON\_SETTING constant define from SYSCLK\_PLLCON\_50MHz\_XTAL to CLK\_PLLCON\_50MHz\_HXT.
8. Fixed bug on CLKO multi-function pin configuration in SYS\_Init() of same samples.
9. Fixed UA\_LIN\_CTL[4] bit field name is "MUTE\_EN" not "WAKE\_EN" in UART LIN\_CTL Bit Field Definitions.
10. Fixed CLK\_SetCoreClock() core lock range from "25~50MHz" to "25~72MHz".
11. Fixed CLK\_SysTickDelay() bug, that COUNTFLAG(SysTick\_CTRL[16]) may not be cleared after write SysTick\_VAL.
12. Fixed typo in UA\_LIN\_CTL constants definitions of UART driver, it is "UART\_LIN\_CTL\_LIN\_BKDET\_EN" not "UART\_LIN\_CTL\_LIN\_BKDET\_ENN".
13. Fixed UA\_LIN\_CTL[4] bit field name of UART driver. It is "MUTE\_EN" not "WAKE\_EN" in UA\_LIN\_CTL constants definitions.
14. Fixed API declare name from I2C\_SetClockBusFreq() to I2C\_SetBusClockFreq() in I2C driver.
15. Fixed SYS\_IS\_SYSTEM\_RST() bug in SYS driver, it is "SYS\_RSTSRC\_RSTS\_SYS\_Msk" not "SYS\_RSTSRC\_RSTS\_MCU\_Msk".
16. Fixed typo of PD14 Multi-Function constant definitions.
17. Fixed clear Time-out flag method bug in I2C\_ClearTimeoutFlag() of I2C driver.

18. Fixed PDMA\_IS\_CH\_BUSY() definition bug in PDMA driver.
19. Removed unused PWRCON, FREQ\_72MHZ constant definitions from clock driver.
20. Removed unused constant define "RXBUFSIZE".
21. Added SPI\_SET\_SS\_LEVEL() macro definition. This macro allows user to set both SPI\_SS pins.
22. Added a lack macro, SYS\_IS\_LVR\_RST() to SYS driver.
23. Added UART FIFO size constants definitions to UART driver.
24. Added CLK\_PLLCON\_25MHz\_HXT, CLK\_PLLCON\_25MHz\_HIRC, CLK\_PLLCON\_24MHz\_HXT, and CLK\_PLLCON\_24MHz\_HIRC constant definitions to CLK driver.
25. Added FMC\_MultiBoot\_SwReset sample code to show how to boot to different AP.
26. Modified time-out counter to a fix value and not to use SystemCoreClockUpdate() in CLK\_WaitClockReady() to improve compatibility.
27. Revised the following four macro definitions to avoid affecting another SPI\_SS pin, SPI\_SET\_SS0\_HIGH(), SPI\_SET\_SS1\_HIGH(), SPI\_SET\_SS0\_LOW() and SPI\_SET\_SS1\_LOW().

#### **Revision 3.00.001** (Released 2014-11-27)

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1. First release.

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