MIA: A 16-bit RISC ISA

https://github.com/MariaElysse/archel

MIA Instruction Format

Insn	Туре	Opcode	Operation				
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ARCHEL: A MIA Implementation

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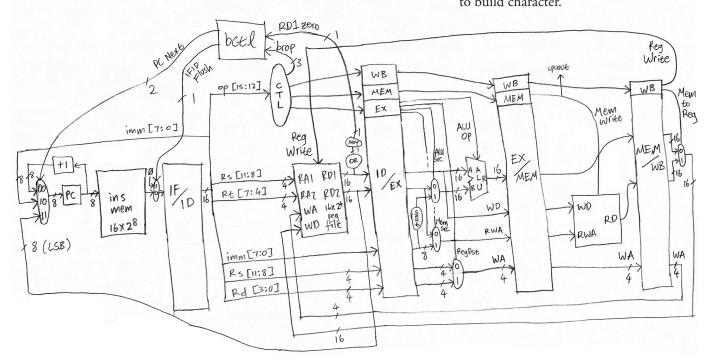
|15 : 12|11 :

MIA Register Conventions

Reg	Usage
\$0	Constant zero
\$1	Function result
\$2	Argument 1
\$3	Argument 2
\$4	Argument 3
\$5	Argument 4
\$6	Temporary
\$7	Temporary
\$8	Temporary
\$9	Temporary
\$10	Temporary
\$11	Temporary
\$12	Temporary
\$13	Temporary
\$14	Stack pointer
\$15	Return address

ARCHEL Features

Harvard architecture (separate insn & data mems).
5-stage pipeline, for extra efficiency.
Signed arithmetic 16-bit multi-operation ALU.
Fully working stack and main memory.
No compiler, no assembler, no offset addressing, to build character.



Quicksort in MIA

Memory Trace

Stack / Call Trace

