MIA: A 16-bit RISC ISA

Insn	Type	Operation
NOP	?	NOP
ADD	R	$R[rd] \leftarrow R[rs] + R[rt]$
ADDI	I	$R[rs] \leftarrow R[rs] + sextimme$
SUB	R	R[rd] <- R[rs] - R[rt]
AND	R	R[rd] <- R[rs] & R[rt]
OR	R	R[rd] <- R[rs] R[rt]
SLT	R	R[rd] <- R[rs] < R[rt]
LW	R	R[rd] <- M[rt]
SW	R	M[rt] <- R[rs]
SWI	I	M[sextimme] <- R[rs]
BEZI	I	R[rs] == 0 ? PC <- sextimme
BNZI	I	R[rs] != 0 ? PC <- sextimme
BEZR	R	R[rs] == 0 ? PC <- R[rt]
BNZR	R	R[rs] != 0 ? PC <- R[rt]

	<u> </u>			
R	op	rs	rt	rd
I	op	rs	im	m
	15 : 12	11 : 8	7 : 4	3 : 0

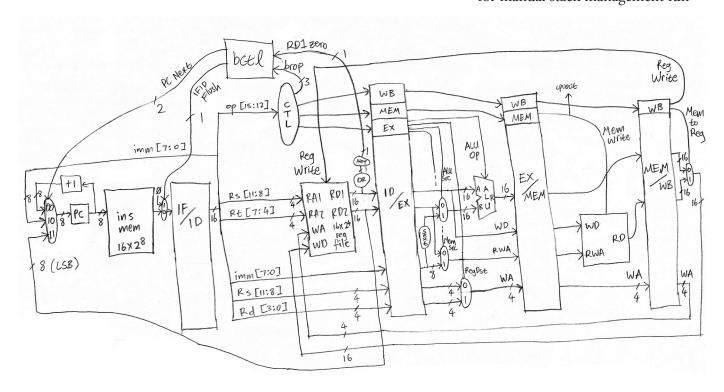
ARCHEL: A MIA Implementation

MIA Register Conventions

Reg	Usage
\$0	Constant zero
\$1	Function result
\$2	Argument 1
\$3	Argument 2
\$4	Argument 3
\$5	Argument 4
\$6	Temporary
\$7	Temporary
\$8	Temporary
\$9	Temporary
\$10	Temporary
\$11	Temporary
\$12	Temporary
\$13	Temporary
\$14	Stack pointer
\$15	Return address

MIA / ARCHEL Features

Pipelined, for extra efficiency No compiler, for extra assembly fun No assembler, for extra hand-linking fun No offset immediate addressing, for manual stack management fun



Quicksort in MIA

Memory Trace

Stack / Call Trace

