Military Institute of Science and Technology
Department of Computer Science and Engineering
CSE-21, Level-3, Term-II
CSE-316 (Digital System Design Sessional)
Project-2
Section: A (Group A7-Group A11)

Instructions:

1. Design the 4-bit ALU [Use of multiplexer is strictly prohibited].
2. Try to optimize the design.
3. The ALU design must be submitted in the 6th week in both hardcopy (on paper) and softcopy (using Circuit Maker, proteus or similar any other software). Do the following:
    a. Draw the Logic Diagram of the whole ALU design in an art paper.
    b. Determine the total number of ICs and gates used in your design.
    c. In the same art paper, write down the truth tables, equations, total number of gates, total number of ICs, and IC numbers.
4. You must submit the final hardware connection in the 8th week.
5. You have to submit a report on ALU along with the hardware connection.

Problem :

Design a 4-bit Arithmetic Logic Unit (ALU), which generates the following operations. Also show four status registers (Sign flag, Carry flag, Overflow flag, Zero flag).

Operation	Function
F = B + A	Add B with A
F = B + A + 1	Add B and A with carry
F = A - 1	Decrement A
F = A	Transfer A
F = A OR B	Logical OR
F = A NOR B	Logical NOR

Report Writing Guidelines:

Points that need to be mentioned in the report are described below:

1. **Introduction**: Basic Introduction about ALU.
2. **Design Procedure:** This section includes details about the arithmetic and Logic unit of the ALU, short description of the operations each unit is performing (description, input, selector input, output etc.)
3. **Design of Arithmetic Logic Unit (ALU):** This section includes the truth table and equation of the arithmetic and Logic Unit of the designed ALU. Describe each unit's truth table and formulation of the equation of X,Y and Z.
4. **Status Checking:** Detail description and design of the four status registers (zero, overflow, carry and sign flag).
5. **Truth Table:** Final Truth table of the ALU.
6. **IC Description:** Number of ICs used and description of each IC with pin diagram, configuration and Truth table.
7. **Conclusion**

Note: Logic Diagram and software simulation should be submitted in week 6. Hardware Implementation and report should be submitted in week 8.