



Εργασία VLSI 2022

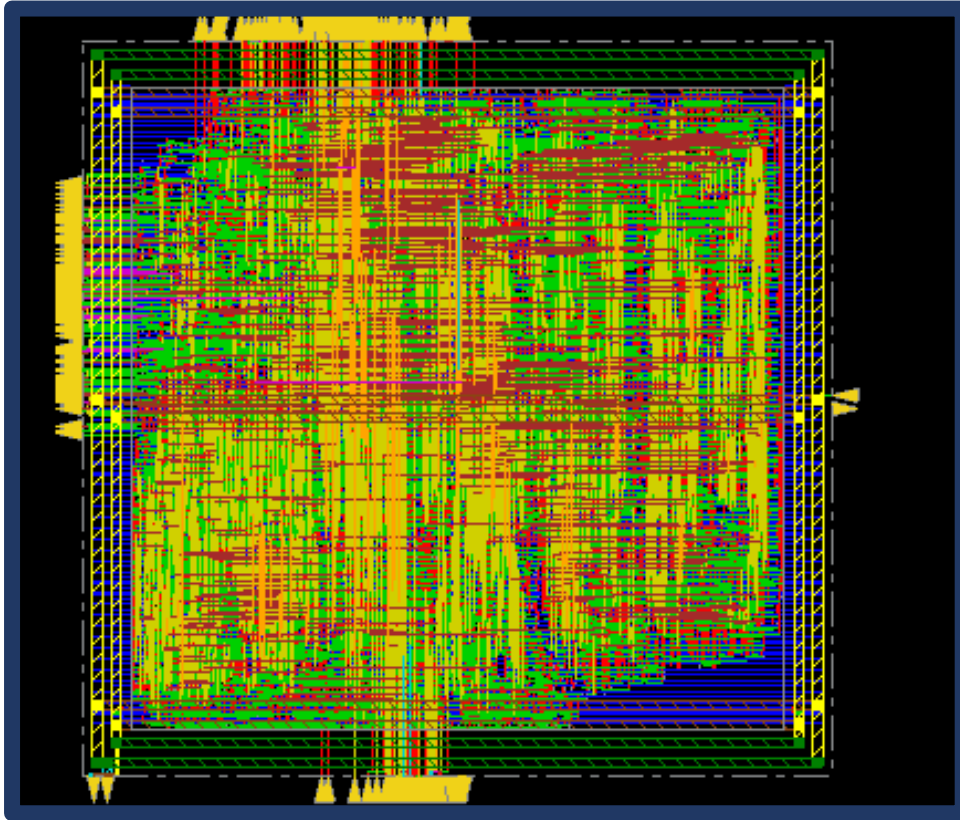
Μαρία Ξουρή AEM:10240

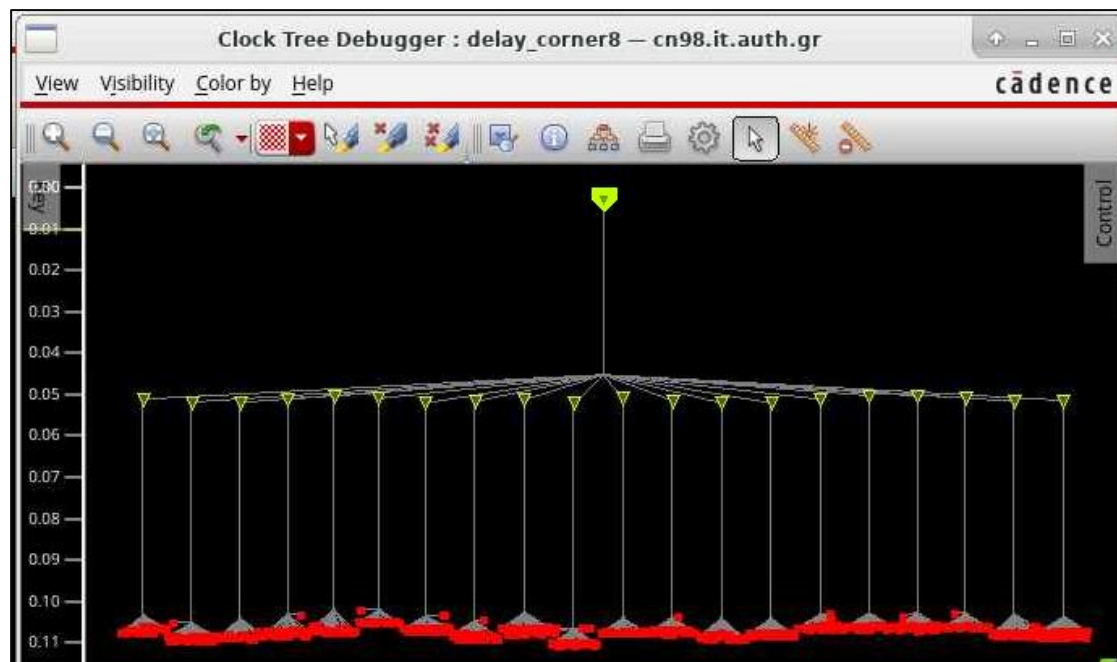
Μετρήσεις

Στις επόμενες σελίδες περιγράφονται οι μετρήσεις και
εικόνες των κυκλωμάτων

ΆΣΚΗΣΗ 1

Τα σχήματα που προκύπτουν είναι τα ακόλουθα





Οι αξιολογήσεις των αποτελεσμάτων εμφανίζονται συνολικά μετά την παρουσίαση των αποτελεσμάτων όλων των ασκήσεων.

Περιορισμοί του genus

```
create_clock [get_ports clk] -name clk -period 10 -waveform {0 5}

set_clock_latency 0.4 [get_clocks {clk}]

set_clock_uncertainty 0.05 [get_clocks clk]

set_clock_transition 0.1 [get_clocks clk]

set_output_delay -network_latency_included -max 1 -clock [get_clocks clk] [all_outputs]
set_output_delay -network_latency_included -min 0.4 -clock [get_clocks clk] [all_outputs]

set_load -max 0.5 [all_outputs]

set_load -min 0.01 [all_outputs]

set_input_delay -network_latency_included -max 1 -clock [get_clocks clk] [all_inputs]
set_input_delay -network_latency_included -min 0.4 -clock [get_clocks clk] [all_inputs]

set_driving_cell -lib_cell BUFX2 -max [all_inputs]

set_driving_cell -lib_cell BUFX16 -min [all_inputs]
```

ΒΗΜΑ 6

Τα αποτελέσματα του genus αποτελούν τα παρακάτω

AREA (μm^2)	GATES	SLACK (ps)	POWER (mW)
43707.546	8637	6036	4.18082e-03

ΒΗΜΑ 11

Το δίκτυο διανομής ισχύος είναι ικανό να τροφοδοτήσει όλο το κύκλωμα καθώς όπως φαίνεται στην διαδικασία του genus σε όσα instances υπάρχουν φορτώθηκε η VDD.

```
11707 Nodes Loaded for VDD.  
11765 Elements Loaded for VDD.  
  
Total Nodes Number: 11707.  
Total Elements Number: 11765.  
  
8850 Instances Loaded for VDD.  
  
Total Instances Number: 8850.
```

Αποτελέσματα Genus

ΒΗΜΑ 12

Τα αποτελέσματα του βήματος 12 αποτελούν τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31057.704	6.330	1.157	2.126	0.001935	3.286

ΒΗΜΑ 13

Τα αποτελέσματα του βήματος 13 είναι τα παρακάτω

METALS	VIAS	WHIRE LENGTH (μm)
1-11	78261	407605340
2-10	104792	409318590

Παρατηρήσεις: Παρατηρούμε ότι όταν μειωθεί το εύρος των μετάλλων αυξάνονται περισσότερα VIAS και WHIRES τα οποία «χωρούν» στο ίδιο area γεγονός που δημιουργεί συμφόρηση.

ΒΗΜΑ 14

Τα αποτελέσματα του βήματος 14 είναι τα παρακάτω

AREA (μm ²)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31205.106	6.312	1.192	2.317	0.001954	3.511

BUFFERS	SKEW GROUPS	MIN DEPTH	MAX DEPTH	TRUNK LENGTH	LEAVES LENGTH
21	1	2	2	667.935	7283.030

Με βάση τον πίνακα, ο στόχος για την στρέβλωση ικανοποιείται

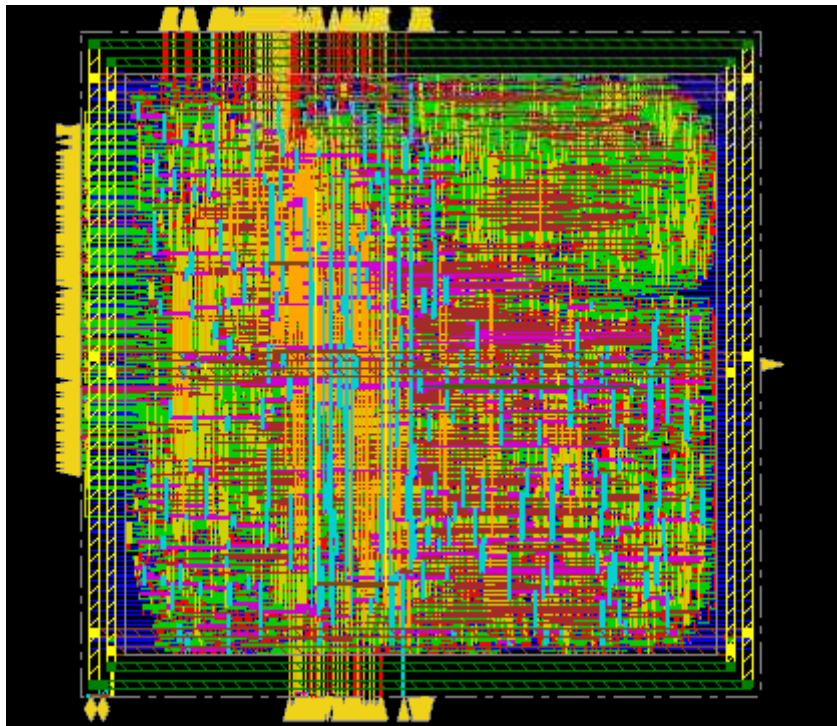
Timing Corner	Worst Rising Leaf Slew	Worst Falling Leaf Slew	Worst Rising Trunk Slew	Worst Falling Trunk Slew	Leaf Slew Target Type	Leaf Slew Target	Trunk Slew Target Type	Trunk Slew Target
delay_corner8:hold.early	0.068	0.071	0.050	0.053	ignored	-	ignored	-
delay_corner8:hold.late	0.070	0.073	0.051	0.054	ignored	-	ignored	-
delay_corner8:setup.early	0.068	0.071	0.050	0.053	ignored	-	ignored	-
delay_corner8:setup.late	0.070	0.073	0.051	0.054	explicit	0.150	explicit	0.150

* - indicates that target was not met.

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31191.768	6.318	1.18878 033	2.302039	0.001951 37	3.49277101

ΆΣΚΗΣΗ 2

Σχήμα



ΒΗΜΑ 6

Τα αποτελέσματα του genus αποτελούν τα παρακάτω

AREA (μm^2)	GATES	SLACK (ps)	POWER (mW)
43707.546	8637	6036	4.18082e-03

BHMA 12

Τα αποτελέσματα του βήματος 12 αποτελούν τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31317.624	6.332	1.113	2.118	0.001853	3.233

BHMA 14

Τα αποτελέσματα του βήματος 14 είναι τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31276.242	6.339	1.143	1.143	0.001859	3.438

BUFFERS	SKEW GROUPS	MIN DEPTH	MAX DEPTH	TRUNK LENGTH	LEAVES LENGTH
21	1	2	2	667.935	7283.030

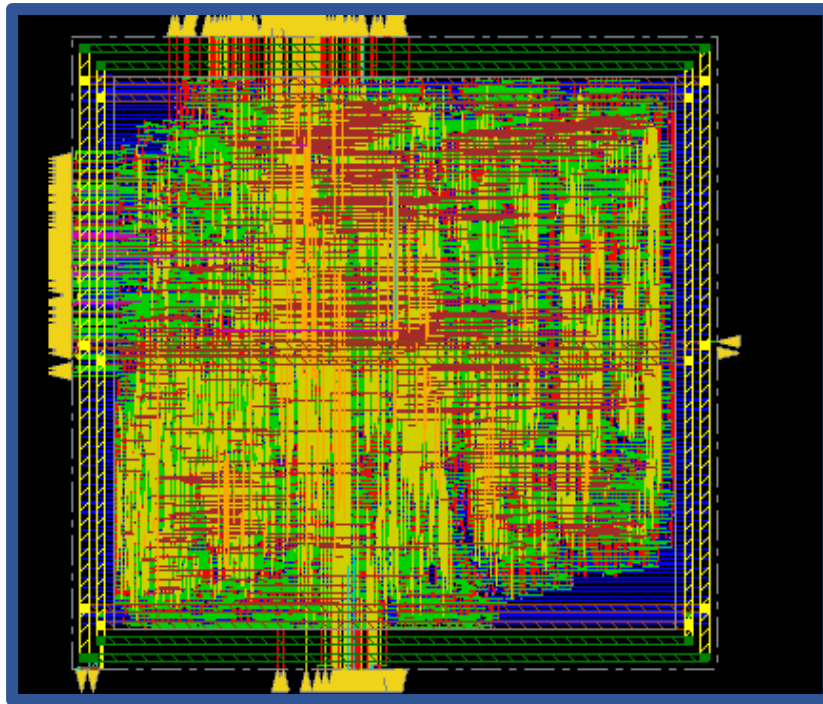
BHMA 15

Τα αποτελέσματα του βήματος 15 είναι τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31276.242	6.334	1.143	2.3	0.001859	3.445

ΆΣΚΗΣΗ 3

Σχήμα



ΒΗΜΑ 6

Τα αποτελέσματα του genus αποτελούν τα παρακάτω

AREA (μm^2)	GATES	SLACK (ps)	POWER (mW)
43707.546	8637	6036	4.18082e-03

ΒΗΜΑ 12

Τα αποτελέσματα του βήματος 12 αποτελούν τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31046.418	6.398	1.157	2.119	0.001934	3.278

BHMA 14

Τα αποτελέσματα του βήματος 14 είναι τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31276.242	6.339	1.19	2.301	0.001953	3.492

BUFFERS	SKEW GROUPS	MIN DEPTH	MAX DEPTH	TRUNK LENGTH	LEAVES LENGTH
21	1	2	2	551.19	7094.640

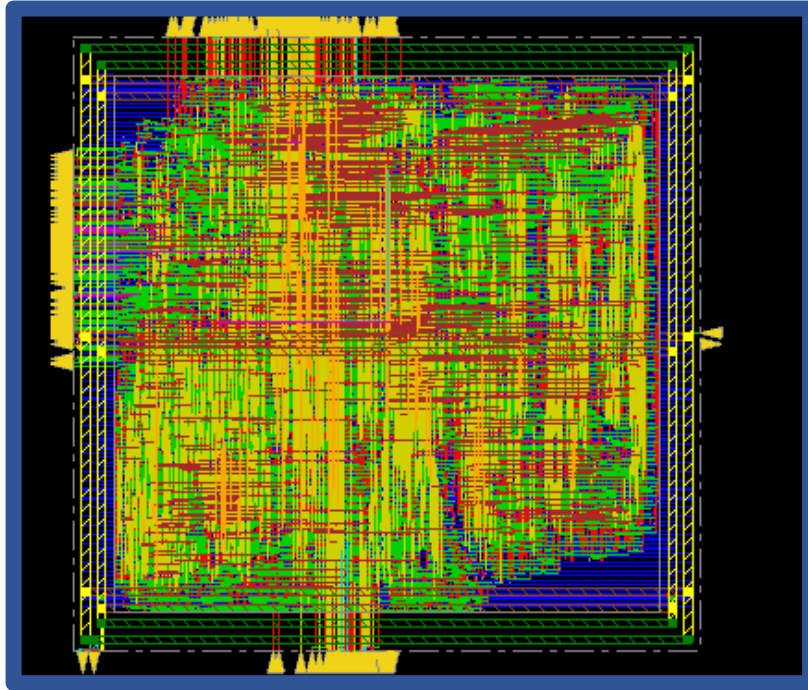
BHMA 15

Τα αποτελέσματα του βήματος 15 είναι τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31203.054	6.387	1.189	2.292	0.001952 6	3.49

ΆΣΚΗΣΗ 4

Σχήμα



Περιορισμοί

```
create_clock [get_ports clk] -name clk -period 8 -waveform {0 4}

set_clock_latency 0.4 [get_clocks {clk}]

set_clock_uncertainty 0.05 [get_clocks clk]

set_clock_transition 0.08 [get_clocks clk]

set_output_delay -network_latency_included -max 1 -clock [get_clocks clk] [all_outputs]
set_output_delay -network_latency_included -min 0.4 -clock [get_clocks clk] [all_outputs]

set_load -max 0.5 [all_outputs]
set_load -min 0.01 [all_outputs]

set_input_delay -network_latency_included -max 1 -clock [get_clocks clk] [all_inputs]
set_input_delay -network_latency_included -min 0.4 -clock [get_clocks clk] [all_inputs]

set_driving_cell -lib_cell BUFX2 -max [all_inputs]
set_driving_cell -lib_cell BUFX16 -min [all_inputs]
```

BHMA 6

Τα αποτελέσματα του genus αποτελούν τα παρακάτω

AREA (μm^2)	GATES	SLACK (ps)	POWER (mW)
43694.531	8640	4032	5.20465e-03

BHMA 12

Τα αποτελέσματα του βήματος 12 αποτελούν τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31081.302	4.416	1.445	2.664	0.001938	4.111

BHMA 14

Τα αποτελέσματα του βήματος 15 είναι τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31230.414	4.345	1.489	2.895	0.001956	4.386

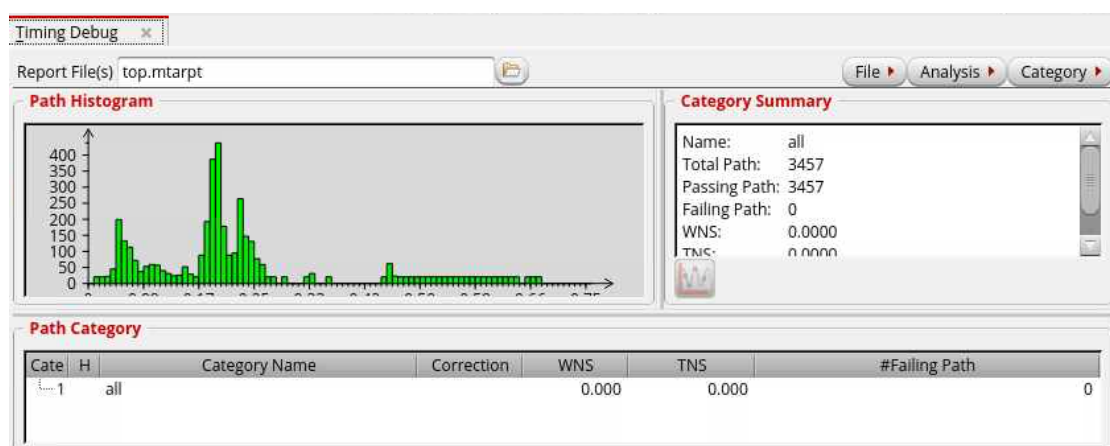
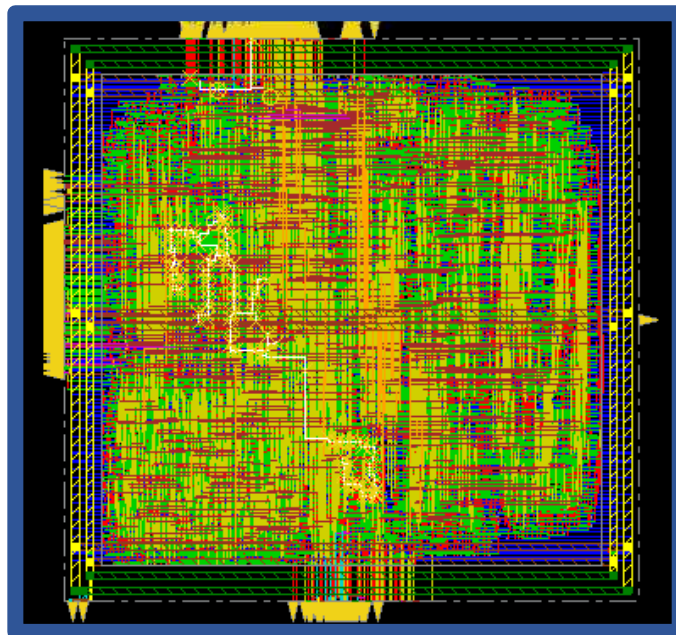
BUFFERS	SKEW GROUPS	MIN DEPTH	MAX DEPTH	TRUNK LENGTH	LEAVES LENGTH
21	1	2	2	590.305	7258.100

ΒΗΜΑ 15

Τα αποτελέσματα του βήματος 15 είναι τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31335.7	4.548	1.196	2.4856	0.0196	4.387

ΆΣΚΗΣΗ 5



Τα αποτελέσματα του genus αποτελούν τα παρακάτω

AREA (μm^2)	GATES	SLACK (ps)	POWER (mW)
46121.235	9320	5	2.58593e-03

BHMA 12

Τα αποτελέσματα του βήματος 12 αποτελούν τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31317.624	2.32	0.76	1.53	0.001931	2.29193

BHMA 14

Τα αποτελέσματα του βήματος 14 είναι τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31224.258	2.84	0.785	1.316	0.001953	2.102

BUFFERS	SKEW GROUPS	MIN DEPTH	MAX DEPTH	TRUNK LENGTH	LEAVES LENGTH
21	1	2	2	548.570	7394.720

BHMA 15

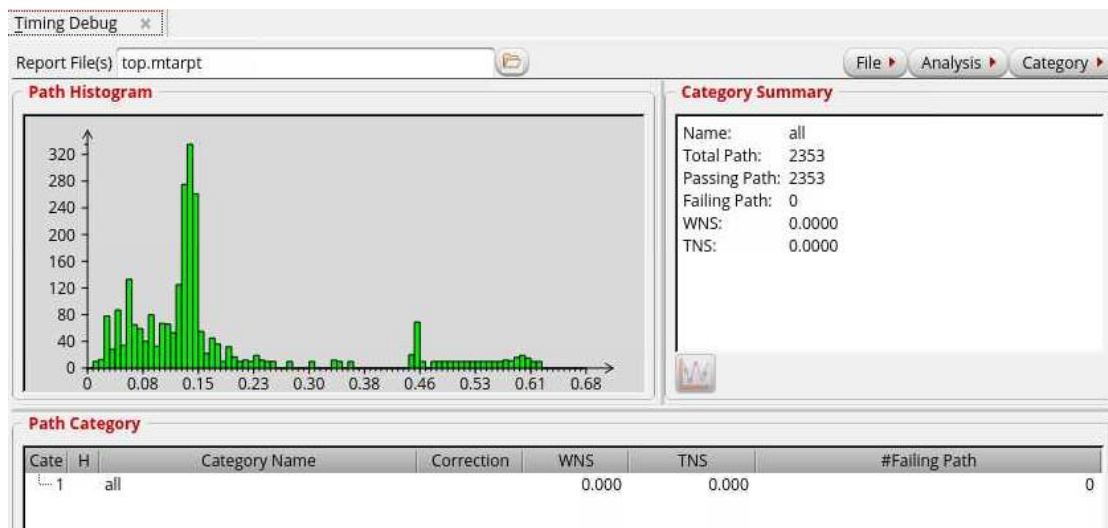
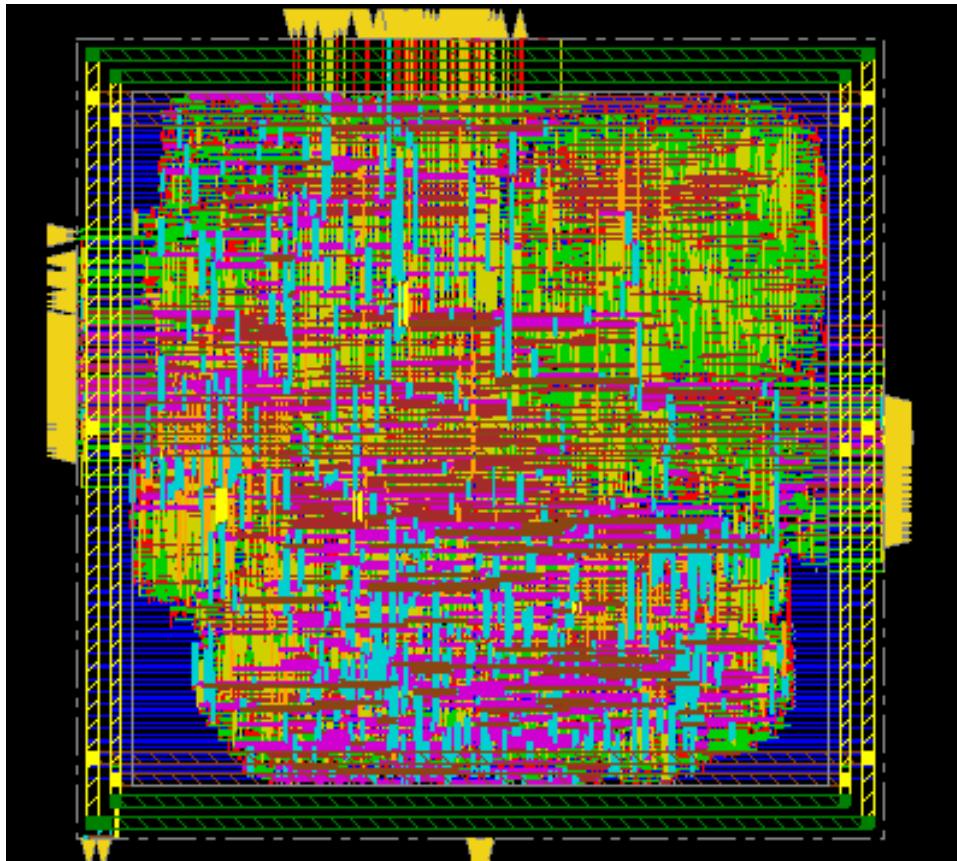
Τα αποτελέσματα του βήματος 15 είναι τα παρακάτω

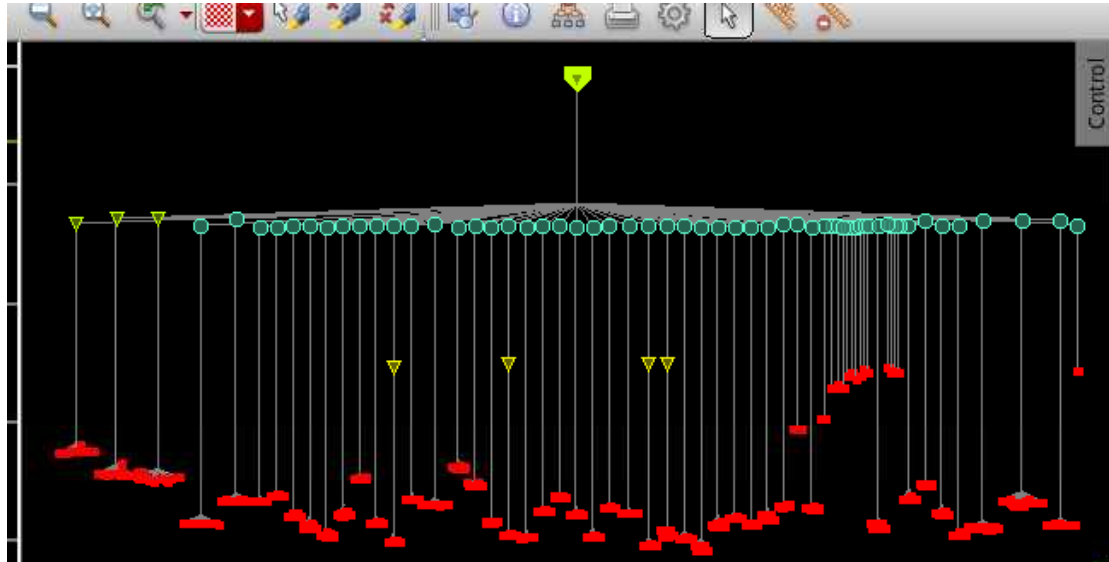
AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
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31224.258	2.37	0.638	2.32	0.001953	2.96
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ΑΣΚΗΣΗ 6

Σχήμα





BHMA 6

Τα αποτελέσματα του genus αποτελούν τα παρακάτω

AREA (μm^2)	GATES	SLACK (ps)	POWER (W)
38858.555	8521	6071	2.73848e-03

BHMA 12

Τα αποτελέσματα του βήματος 12 αποτελούν τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
27082.296	6.143	0.74867 852	2.099	0.00183568	2.849412 45

BHMA 14

Τα αποτελέσματα του βήματος 14 είναι τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
27204.048	6.133	0.7615	2.161	0.00185	2.925

BUFFERS	SKEW GROUPS	MIN DEPTH	MAX DEPTH	TRUNK LENGTH	LEAVES LENGTH
8	1	2	3	324.930	6386.655

BHMA 15

Τα αποτελέσματα του βήματος 15 είναι τα παρακάτω

AREA (μm^2)	SLACK (ns)	Internal P (mW)	Switching P (mW)	Leakage P(mW)	Total POWER (mW)
31276.242	6.127	0.7615	2.163	0.00185	2.926

Αξιολόγηση αποτελεσμάτων

Τα αποτελέσματα των reports φαίνονται συγκριτικά στους ακόλουθους πίνακες

ΑΣΚΗΣΗ	AREA (μm^2)	SLAC K (ns)	Internal P (W)	Switching P (W)	Leakage P(W)	Total POWER (W)
BHMA 12						
1	31057.704	6.330	1.157	2.126	0.001935	3.286
2	31317.624	6.332	1.113	2.118	0.001853	3.233
3	31046.418	6.398	1.157	2.119	0.001934	3.278
4	31081.302	4.416	1.445	2.664	0.001938	4.111
5	31317.624	2.32	0.76	1.53	0.001931	2.29193
6	27082.296	6.143	0.74867852	2.099	0.00183568	2.84941245
BHMA 14						
1	31205.106	6.312	1.192	2.317	0.001954	3.511
2	31276.242	6.339	1.143	1.143	0.001859	3.438
3	31276.242	6.339	1.19	2.301	0.001953	3.492
4	31230.414	4.345	1.489	2.895	0.001956	4.386
5	31224.258	2.84	0.785	1.316	0.001953	2.102
6	27204.048	6.133	0.7615	2.161	0.00185	2.925

ΒΗΜΑ 15

1	31191.768	6.318	1.18878 033	2.302039	0.00195 137	3.492771 01
2	31276.242	6.334	1.143	2.3	0.00185 9	3.445
3	31203.054	6.387	1.189	2.292	0.00195 26	3.49
4	31335.7	4.548	1.196	2.4856	0.0196	4.387
5	31224.258	2.37	0.638	2.32	0.00195 3	2.96
6	31276.242	6.127	0.7615	2.163	0.00185	2.926

Άσκηση 2: Στην άσκηση 2 έχουμε βάλει τη ρύθμιση του High Effort γεγονός που αυξάνει το slack κάνοντας το κύκλωμα γρηγορότερο.

Άσκηση 3: Στην άσκηση 3 έχουμε χρησιμοποιήσει το 85% του πυρήνα γεγονός που αυξάνει το slack καθώς χρησιμοποιούνται περισσότερα λογικά κυκλώματα και τα αποτελέσματα προκύπτουν πιο γρήγορα. Επιπλέον μειώνεται ελάχιστα το area καθώς τα στοιχεία τοποθετούνται πιο κοντά.

Άσκηση 4: Στην άσκηση 4 έχουμε μειώσει την περίοδο γεγονός που επηρεάζει σημαντικά το slack καθώς μειώνεται κατά 2 μονάδες. Αυτό οφείλεται στο γεγονός ότι το slack εξαρτάται από την περίοδο σύμφωνα με τον τύπο:

$$T_{slack} = T_{clock_path} + T_{cycle} - T_{data_path}$$

Αν μειωθεί η περίοδος μειώνεται και το slack.

Επιπλέον αυξάνεται και το power καθώς μειώνεται η περίοδος και αυξάνεται η συχνότητα.

Άσκηση 5: Στο βήμα 5 χρησιμοποιήθηκε η slow βιβλιοθήκη γεγονός που οδηγεί στην μείωση του slack. Το κύκλωμα είναι γενικά πιο αργό με την βιβλιοθήκη αυτή γεγονός που μειώνει σε μεγάλο βαθμό την ισχύ του καθώς όσο πιο ταχύ είναι το κύκλωμα τόσο μεγαλύτερη ενέργεια ξοδεύεται. Επιπλέον αυξήθηκε και το area καθώς τα πιο αργά κελιά απαιτούν περισσότερο χώρο.

Άσκηση 6: Στην άσκηση 6 χρησιμοποιήθηκε clock gating οδηγώντας στην μείωση του Internal Power καθώς αφαιρείται το σήμα του ρολογιού όταν δεν χρησιμοποιείται. Επιπλέον, έχει μειωθεί το area διότι πολλές φορές κάποια flip flop που υλοποιούν την δουλειά του clock gating αφαιρούνται.

CMD για Άσκηση 1

Genus

```
set_db init_lib_search_path
/mnt/apps/prebuilt/eda/designkits/GPDK/gsclib045/lan/flow/t1u1/reference_libs/GPDK045/gsclib045_svt_v4.4/gsclib045

set_db library
/mnt/apps/prebuilt/eda/designkits/GPDK/gsclib045/lan/flow/t1u1/reference_libs/GPDK045/gsclib045_svt_v4.4/gsclib045/
timing/fast_vdd1v0_basicCells.lib

set_db lef_library
{" /mnt/apps/prebuilt/eda/designkits/GPDK/gsclib045/lan/flow/t1u1/reference_libs/GPDK045/gsclib045_svt_v4.4/gsclib045/
5/lef/gsclib045_tech.lef"
"/mnt/apps/prebuilt/eda/designkits/GPDK/gsclib045/lan/flow/t1u1/reference_libs/GPDK045/gsclib045_svt_v4.4/gsclib045/
/lef/gsclib045_macro.lef"}

set_db script_search_path /mnt/scratch_b/users/m/marixour/Desktop/

set_db init_hdl_search_path /mnt/scratch_b/users/m/marixour/Desktop/

read_qrc
/mnt/apps/prebuilt/eda/designkits/GPDK/gsclib045/lan/flow/t1u1/reference_libs/GPDK045/gsclib045_svt_v4.4/gsclib045/
qrc/qx/gpdk045.tch

read_hdl picorv32.v

elaborate picorv32

check_design

set_db / .use_scan_seqs_for_non_dft false

read_sdc periorismoask.sdc

check_timing_intent

syn_generic

syn_map

syn_opt

report_area > /mnt/scratch_b/users/m/marixour/ASK1/report_area_g.txt

report_power > /mnt/scratch_b/users/m/marixour/ASK1/report_power_g.txt

report_gates > /mnt/scratch_b/users/m/marixour/ASK1/report_gates_g.txt

report_timing > /mnt/scratch_b/users/m/marixour/ASK1/report_timing_g.txt

write_design -base_name /mnt/scratch_b/users/m/marixour/Desktop/genus_invs_des_e1/e1_innovus picorv32

write_hdl > /mnt/scratch_b/users/m/marixour/Desktop/genus_invs_des_e1/design_e1.v

write_script > /mnt/scratch_b/users/m/marixour/Desktop/genus_invs_des_e1/constraints_e1.g

write_sdc > /mnt/scratch_b/users/m/marixour/Desktop/genus_invs_des_e1/constraints_e1.sdc

innovus
```

Innovus

```
set ::TimeLib::tsgMarkCellLatchConstructFlag 1

set _timing_enable_new_write_flow_machine_readable 1

set conf_qxconf_file NULL

set conf_qxlib_file NULL

set dbgDualViewAwareXTree 1

set defHierChar /

set distributed_client_message_echo 1

set distributed_mmmc_disable_reports_auto_redirection 0

set enable_ilm_dual_view_gui_and_attribute 1

set enc_enable_print_mode_command_reset_options 1

set init_gnd_net GND

set init_lef_file
{../../../../../apps/prebuilt/eda/designkits/GPDK/gsclib045/lan/flow/t1u1/reference_libs/G
PDK045/gsclib045_svt_v4.4/gsclib045/lef/gsclib045_tech.lef
../../../../../apps/prebuilt/eda/designkits/GPDK/gsclib045/lan/flow/t1u1/reference_libs/GP
DK045/gsclib045_svt_v4.4/gsclib045/lef/gsclib045_macro.lef}

set init_mmmc_file Default_e8.view

set init_oa_search_lib {}

set init_original_verilog_files Desktop/genus_invs_des_e8/e8.v

set init_pwr_net VDD

set init_top_cell picorv32

set init_verilog Desktop/genus_invs_des_e8/e1.v

set latch_time_borrow_mode max_borrow

set metric_page_cfg_format {html {HUDDLE {!!seq {!!map {Summary {!!seq {!!map
{summary_flow {!!map {type {!!str header} title {!!str {}}}}} {!!map {summary_flow_t
{!!map {type {!!str vertical_table} auto_hide {!!true 1} ar_metric {!!seq {!!map {metric
{!!str design.name} title {!!str Design}}} {!!map {metric {!!str flow.tool_list} title {!!str
Tools}}} {!!map {metric {!!str flow.template.type} title {!!str Flow}}} {!!map {metric {!!str
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flow.run_tag} title {!!str Tag}}} {!!map {metric {!!str flow.machine} title {!!str {Run host}}}
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{!!map {timing_setup {!!map {type {!!str header} title {!!str {Setup Timing}}}} {!!map {timing_setup_t {!!map {type {!!str table} per_snapshot {!!true 1} key {!!map {Group {!!str timing.setup.wns.path_group:*} View {!!str timing.setup.wns.analysis_view:*}} collapsible_key {!!true 1} ar_metric {!!seq {!!map {metric {!!str timing.setup.wns.path_group:%.analysis_view:%} title {!!str WNS} navigation {!!map {view {!!str default_timing} tab {!!str Timing}}}} {!!map {metric {!!str timing.setup.tns.path_group:%.analysis_view:%} title {!!str TNS} navigation {!!map {view {!!str default_timing} tab {!!str Timing}}}} {!!map {metric {!!str timing.setup.feps.path_group:%.analysis_view:%} title {!!str FEPS}}}}}} {!!map {timing_hold {!!map {type {!!str header} title {!!str {Hold Timing}}}} {!!map {timing_hold_t {!!map {type {!!str table} per_snapshot {!!true 1} key {!!map {Group {!!str timing.hold.wns.path_group:*} View {!!str timing.hold.wns.analysis_view:*}} collapsible_key {!!true 1} ar_metric {!!seq {!!map {metric {!!str timing.hold.wns.path_group:%.analysis_view:%} title {!!str WNS} navigation {!!map {view {!!str default_timing} tab {!!str Timing}}}} {!!map {metric {!!str timing.hold.tns.path_group:%.analysis_view:%} title {!!str TNS} navigation {!!map {view {!!str default_timing} tab {!!str Timing}}}} {!!map {metric {!!str timing.hold.feps.path_group:%.analysis_view:%} title {!!str FEPS}}}}}} {!!map {timing_drv {!!map {type {!!str table} per_snapshot {!!true 1} ar_metric {!!seq {!!map {metric {!!str timing.drv.max_tran.total} title {!!str Total} group {!!str Tran}} {!!map {metric {!!str timing.drv.max_tran.worst} title {!!str Worst} group {!!str Tran} link_file_metric {!!str timing.drv.report_file}} {!!map {metric {!!str timing.drv.max_cap.total} title {!!str Total} group {!!str Cap}} {!!map {metric {!!str timing.drv.max_cap.worst} title {!!str Worst} group {!!str Cap}} {!!map {metric {!!str timing.drv.max_fanout.total} title {!!str Total} group {!!str Fanout}} {!!map {metric {!!str timing.drv.max_fanout.worst} title {!!str Worst} group {!!str Fanout}}}} {!!map {metric {!!str timing.si.glitches} title {!!str Glitches} group {!!str SI}} {!!map {metric {!!str timing.si.noise} title {!!str Noise} group {!!str SI}}}}}}}} {!!map {Clock {!!seq {!!map {clock_phys {!!map {type {!!str header} title {!!str Physical}}}} {!!map {clock_phys_t {!!map {type {!!str table} per_snapshot {!!true 1} ar_metric {!!seq {!!map {metric {!!str clock.instances.total} title {!!str {Total} group {!!str Instances} graph_type {!!str none} renderer {!!str histogram}} {!!map {metric {!!str clock.instances.buffer} title {!!str #Buffers} group {!!str Instances}} {!!map {metric {!!str clock.instances.inverter} title {!!str #Inverters} group {!!str Instances}} {!!map {metric {!!str clock.instances.clkgate} title {!!str #Clock Gates} group {!!str Instances}} {!!map {metric {!!str clock.instances.nonig} title {!!str #Non Integrated} group {!!str Instances}} {!!map {metric {!!str clock.instances.logic} title {!!str #Logic} group {!!str Instances}} {!!map {metric {!!str clock.area.total} title {!!str {Total} group {!!str Area}} {!!map {metric {!!str {^.*\.(?!total\$)[^\.]\$} title {!!str { } } group {!!str Area} graph_type {!!str none} renderer {!!str histogram}} {!!map {metric {!!str clock.area.buffer} title {!!str Buffers} group {!!str Area}} {!!map {metric {!!str clock.area.inverter} title {!!str Inverters} group {!!str Area}} {!!map {metric {!!str clock.area.clkgate} title {!!str {Clock Gates} group {!!str Area}} {!!map {metric {!!str clock.area.nonig} title {!!str {Non Integrated} group {!!str Area}} {!!map {metric {!!str clock.area.logic} title {!!str Logic} group {!!str Area}} {!!map {metric {!!str clock.nets.length.total} title {!!str {Tot Clk Net Length} group {!!str Nets}}}}}}}} {!!map {clock_phys_cap {!!map {type {!!str header} title {!!str { } } {!!map {clock_phys_cap_t {!!map {type {!!str table} per_snapshot {!!true 1} ar_metric {!!seq {!!map {title {!!str { } } group {!!str Wire} graph_type {!!str none} renderer {!!str histogram}} {!!map {metric {!!str clock.capacitance.wire.top} title {!!str Top} group {!!str Wire}} {!!map {metric {!!str clock.capacitance.wire.trunk} title {!!str Trunk} group {!!str Wire}} {!!map {metric {!!str clock.capacitance.wire.leaf} title {!!str Leaf} group {!!str Wire}} {!!map {title {!!str { } } group {!!str Gate} graph_type {!!str none} renderer {!!str histogram}} {!!map {metric {!!str clock.capacitance.gate.top} title {!!str Top} group {!!str Gate}} {!!map {metric {!!str clock.capacitance.gate.trunk} title {!!str Trunk} group {!!str Gate}} {!!map {metric {!!str clock.capacitance.gate.leaf} title {!!str Leaf} group {!!str Gate}} {!!map {title {!!str { } } group {!!str Total} graph_type {!!str none} renderer {!!str histogram}} {!!map {metric {!!str clock.capacitance.total.top} title {!!str Top} group {!!str Total}} {!!map {metric {!!str clock.capacitance.total.trunk} title {!!str Trunk} group {!!str Total}} {!!map {metric {!!str clock.capacitance.total.leaf} title {!!str Leaf} group {!!str Total}} {!!map {metric {!!str clock.capacitance.sink.*} group {!!str Sink}}}}}}}} {!!map {clock_drv {!!map {type {!!str header} title {!!str DRV}}}} {!!map {clock_drv_t {!!map {type {!!str table} per_snapshot {!!true 1} ar_metric {!!seq {!!map {metric {!!str {clock.drv.nets.remaining transition.count} title {!!str Count} group {!!str {Remaining Transition}} {!!map {metric {!!str {clock.drv.nets.remaining transition.max} title {!!str Max} group {!!str {Remaining Transition}} {!!map {metric {!!str {clock.drv.nets.unfixable transition.count} title {!!str Count} group {!!str {Unfixable Transition}} {!!map {metric {!!str {clock.drv.nets.unfixable transition.max} title {!!str Max} group {!!str {Unfixable Transition}}}} {!!map {metric {!!str clock.drv.nets.capacitance.count} title {!!str Count} group {!!str Capacitance}} {!!map {metric {!!str clock.drv.nets.capacitance.max} title {!!str Max} group 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{!!str Fanout}}}}}}}} {!!map {clock_drv_tran_tar {!!map {type {!!str header} title {!!str Transition}}}} {!!map {clock_drv_tran_tar_t {!!map
{type {!!str table} auto_hide {!!true 1} ar_metric {!!seq {!!map {metric {!!str clock.transition.target.primary_half_corner.top.*} group {!!str
{Top Transition Target Stats}}}} {!!map {metric {!!str clock.transition.target.primary_half_corner.trunk.*} group {!!str {Trunk Transition Target
Stats}}}} {!!map {metric {!!str clock.transition.target.primary_half_corner.leaf.*} group {!!str {Leaf Transition Target Stats}}}}}}}} {!!map
{clock_skew {!!map {type {!!str header} title {!!str Latency/Skew}}}} {!!map {clock_skew_t {!!map {type {!!str table} auto_hide {!!true 1}
per_snapshot {!!true 1} ar_metric {!!seq {!!map {metric {!!str clock.latency.primary_reporting_skew_group.primary_half_corner.*} group
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{!!str clock.skew.primary_reporting_skew_group.primary_half_corner.skew_band.*} group {!!str {Skew Band}}}}}}}}}} {!!map {Design {!!seq
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{!!str design.instances} title {!!str {Total instances}}}} {!!map {metric {!!str design.area} title {!!str {Total area}}}} {!!map {metric {!!str
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Place}}}} {!!map {physical_check_place_t {!!map {type {!!str vertical_table} auto_hide {!!true 1} per_snapshot {!!true 1} ar_metric {!!seq
{!!map {metric {!!str check.place.*}}}}}}}} {!!map {Power {!!seq {!!map {power_power {!!map {type {!!str header} title {!!str Power}}}}
{!!map {power_power_t {!!map {type {!!str table} per_snapshot {!!true 1} ar_metric {!!seq {!!map {metric {!!str power} title {!!str Total} group
{!!str {Whole Design}}}} {!!map {metric {!!str {^power\..*$}} title {!!str { }} group {!!str {Whole Design}} graph_type {!!str none} renderer {!!str
histogram}}}} {!!map {metric {!!str power.leakage} title {!!str Leakage} group {!!str {Whole Design}}}} {!!map {metric {!!str power.internal} title
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design.congestion.hotspot.total} title {!!str Total} group {!!str Congestion}}}} {!!map {metric {!!str route.map.*} group {!!str {Congestion
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{!!str Vias}}}} {!!map {metric {!!str route.drc.antenna} title {!!str Antenna} group {!!str {Route DRC}}}} {!!map {metric {!!str route.drc} title {!!str
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check.drc} title {!!str Total} group {!!str {Check DRC}} link_file_metric {!!str check.drc.report_file}}}}}}}} {!!map {Flow {!!seq {!!map
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{!!true 1} ar_metric {!!seq {!!map {metric {!!str flow.user} title {!!str User}}}} {!!map {metric {!!str flow.log} title {!!str {Log File}}
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{Run Tag}}}} {!!map {metric {!!str flow.step.tcl} title {!!str {Step TCL}}}}}} hide_footers {!!true 1} hide_graph_footers {!!true 1}}}} {!!map
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ar_metric {!!seq {!!map {metric {!!str flow.cputime} title {!!str CPU} group {!!str Runtime}}}} {!!map {metric {!!str flow.cputime.total} title {!!str
{Total CPU}} group {!!str Runtime}}}} {!!map {metric {!!str flow.realtime} title {!!str Wall} group {!!str Runtime}}}} {!!map {metric {!!str
flow.realtime.total} title {!!str {Total Wall}} group {!!str Runtime}}}} {!!map {metric {!!str flow.memory} title {!!str Resi+Virtual} group {!!str
Memory}}}} {!!map {metric {!!str flow.memory.resident} title {!!str Resident} group {!!str Memory}}}} {!!map {metric {!!str
flow.memory.resident.peak} title {!!str {Peak Resident}} group {!!str Memory}}}}}}}}}} text {HUDDLE {!!seq {!!map {{} {!!seq {!!map
{summary_qor_t {!!map {type {!!str table} per_snapshot {!!true 1} ar_metric {!!seq {!!map {metric {!!str timing.setup.wns} title {!!str WNS}}}}
{!!map {metric {!!str timing.setup.tns} title {!!str TNS}}}} {!!map {metric {!!str timing.setup.feps} title {!!str FEPS}}}} {!!map {metric {!!str
timing.setup.wns.path_group:reg2reg} title {!!str WNS_R2R}}}} {!!map {metric {!!str timing.setup.tns.path_group:reg2reg} title {!!str
TNS_R2R}}}} {!!map {metric {!!str timing.setup.feps.path_group:reg2reg} title {!!str FEPS_R2R}}}} {!!map {metric {!!str
timing.drv.max_tran.total} title {!!str Tran} group {!!str DRV(T)}}}} {!!map {metric {!!str timing.drv.max_cap.total} title {!!str Load} group {!!str
DRV(C)}}}} {!!map {metric {!!str power.leakage} title {!!str Leakage} group {!!str POWER(L)}}}} {!!map {metric {!!str design.density} title {!!str
Density} group {!!str UTIL}}}} {!!map {metric {!!str design.instances.logical} title {!!str INSTS}}}} {!!map {metric {!!str design.area.logical} title
{!!str AREA}}}} {!!map {metric {!!str route.drc} title {!!str DRC}}}} {!!map {metric {!!str flow.cputime} title {!!str CPU}}}}}}}}}}}}

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set pegDefaultResScaleFactor 1

set pegDetailResScaleFactor 1

set pegEnableDualViewForTQuantus 1

set report_inactive_arcs_format {from to when arc_type sense reason}

set report_timing_format {timing_point flags arc edge cell fanout transition delay arrival}

set spgUnflattenImlnCheckPlace 2

suppressMessage -silent GLOBAL-100

unsuppressMessage -silent GLOBAL-100

suppressMessage -silent GLOBAL-100

unsuppressMessage -silent GLOBAL-100

set timing_enable_default_delay_arc 1

set timing_report_enable_machine_readable_arrival_calc 1

set timing_report_retime_formatting_mode retime_replace

init_design

```

getIoFlowFlag

setIoFlowFlag 0

floorPlan -site CoreSite -r 0.993763288448 0.75 15 15 15 15

uiSetTool select

getIoFlowFlag

fit

set sprCreateleRingOffset 1.0

set sprCreateleRingThreshold 1.0

set sprCreateleRingJogDistance 1.0

set sprCreateleRingLayers {}

set sprCreateleRingOffset 1.0

set sprCreateleRingThreshold 1.0

set sprCreateleRingJogDistance 1.0

set sprCreateleRingLayers {}

set sprCreateleStripeWidth 10.0

set sprCreateleStripeThreshold 1.0

set sprCreateleStripeWidth 10.0

set sprCreateleStripeThreshold 1.0

set sprCreateleRingOffset 1.0

set sprCreateleRingThreshold 1.0

set sprCreateleRingJogDistance 1.0

set sprCreateleRingLayers {}

set sprCreateleStripeWidth 10.0

set sprCreateleStripeThreshold 1.0

setAddRingMode -ring_target default -extend_over_row 0 -ignore_rows 0 -avoid_short 0 -skip_crossing_trunks none -stacked_via_top_layer
Metal11 -stacked_via_bottom_layer Metal1 -via_using_exact_crossover_size 1 -orthogonal_only true -skip_via_on_pin { standardcell } -
skip_via_on_wire_shape { noshape }

addRing -nets {VDD GND} -type core_rings -follow core -layer {top Metal11 bottom Metal11 left Metal10 right Metal10} -width {top 3 bottom
3 left 3 right 3} -spacing {top 3 bottom 3 left 3 right 3} -offset {top 1.8 bottom 1.8 left 1.8 right 1.8} -center 1 -threshold 0 -jog_distance 0 -
snap_wire_center_to_grid None

set sprCreateleRingOffset 1.0

set sprCreateleRingThreshold 1.0

set sprCreateleRingJogDistance 1.0

set sprCreateleRingLayers {}

set sprCreateleRingOffset 1.0

set sprCreateleRingThreshold 1.0

set sprCreateleRingJogDistance 1.0

set sprCreateleRingLayers {}

set sprCreateleStripeWidth 10.0

set sprCreateleStripeThreshold 1.0

set sprCreateleStripeWidth 10.0

set sprCreateleStripeThreshold 1.0

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set sprCreateeleRingOffset 1.0

set sprCreateeleRingThreshold 1.0

set sprCreateeleRingJogDistance 1.0

set sprCreateeleRingLayers {}

set sprCreateeleStripeWidth 10.0

set sprCreateeleStripeThreshold 1.0

setAddStripeMode -ignore_block_check false -break_at none -route_over_rows_only false -rows_without_stripes_only false -
extend_to_closest_target none -stop_at_last_wire_for_area false -partial_set_thru_domain false -ignore_nondefault_domains false -
trim_antenna_back_to_shape none -spacing_type edge_to_edge -spacing_from_block 0 -stripe_min_length stripe_width -
stacked_via_top_layer Metal11 -stacked_via_bottom_layer Metal1 -via_using_exact_crossover_size false -split_vias false -orthogonal_only
true -allow_jog { padcore_ring block_ring } -skip_via_on_pin { standardcell } -skip_via_on_wire_shape { noshape }

addStripe -nets {VDD GND} -layer Metal9 -direction horizontal -width 3 -spacing 3 -number_of_sets 3 -start_from bottom -
switch_layer_over_obs false -max_same_layer_jog_length 2 -padcore_ring_top_layer_limit Metal11 -padcore_ring_bottom_layer_limit
Metal1 -block_ring_top_layer_limit Metal11 -block_ring_bottom_layer_limit Metal1 -use_wire_group 0 -snap_wire_center_to_grid None

saveDesign picorv32

globalNetConnect VDD -type pgpin -pin VDD -inst *

globalNetConnect VDD -type tiehi -instanceBasename *

globalNetConnect GND -type pgpin -pin VSS -inst *

globalNetConnect GND -type tielo -instanceBasename *

createPGPin VDD -net VDD -geom Metal8 2 0 5 1

createPGPin GND -net GND -geom Metal8 6 0 9 1

setSroutemode -viaConnectToShape { padring ring stripe }

sroute -connect { blockPin padPin padRing corePin floatingStripe } -layerChangeRange { Metal1(1) Metal11(11) } -blockPinTarget {
nearestTarget } -padPinPortConnect { allPort oneGeom } -padPinTarget { nearestTarget } -corePinTarget { firstAfterRowEnd } -
floatingStripeTarget { blockring padring ring stripe ringpin blockpin followpin } -allowJogging 1 -crossoverViaLayerRange { Metal1(1)
Metal11(11) } -nets { VDD GND } -allowLayerChange 1 -blockPin useLef -targetViaLayerRange { Metal1(1) Metal11(11) }

saveDesign picorv32

setRouteMode -earlyGlobalHonorMsvRouteConstraint false -earlyGlobalRoutePartitionPinGuide true

setEndCapMode -reset

setEndCapMode -boundary_tap false

setNanoRouteMode -quiet -droutePostRouteSpreadWire 1

setNanoRouteMode -quiet -droutePostRouteWidenWireRule LEFSpecialRouteSpec

setNanoRouteMode -quiet -timingEngine {}

setUsefulSkewMode -maxSkew false -noBoundary false -useCells {DLY4X4 DLY4X1 DLY3X4 DLY3X1 DLY2X4 DLY2X1 DLY1X4 DLY1X1 CLKBUF8
CLKBUF6 CLKBUF4 CLKBUF3 CLKBUF2 CLKBUF16 CLKBUF12 BUF8 BUF6 BUF4 BUF3 BUF2 BUF16 BUF12
INVXL INVX8 INVX6 INVX4 INVX3 INVX20 INVX2 INVX16 INVX12 INVX1 CLKINVX8 CLKINVX6 CLKINVX4 CLKINVX3 CLKINVX20 CLKINVX2
CLKINVX16 CLKINVX12 CLKINVX1} -maxAllowedDelay 1

setPlaceMode -reset

setPlaceMode -congEffort auto -timingDriven 1 -clkGateAware 1 -powerDriven 1 -ignoreScan 1 -reorderScan 1 -ignoreSpare 0 -placeIOPins 1 -
moduleAwareSpare 0 -preserveRouting 1 -rmAffectedRouting 0 -checkRoute 0 -swapEEQ 0

getPlaceMode

place_opt_design

report_timing > /mnt/scratch_b/users/m/_onoma_/report_timing12.txt

report_timing > /mnt/scratch_b/users/m/marixour/ASK1/report_timing12.txt

report_area > /mnt/scratch_b/users/m/marixour/ASK1/report_area12.txt

report_power > /mnt/scratch_b/users/m/marixour/ASK1/report_power12.txt

set_power_analysis_mode -reset

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set_power_analysis_mode -method static -analysis_view View_e8 -corner max -create_binary_db true -write_static_currents true -
honor_negative_energy true -ignore_control_signals true

set_power_output_dir -reset

set_power_output_dir ./run1

set_default_switching_activity -reset

set_default_switching_activity -input_activity 0.2 -period 10.0

read_activity_file -reset

set_power -reset

set_powerup_analysis -reset

set_dynamic_power_simulation -reset

report_power -rail_analysis_format VS -outfile ./run1/picov32.rpt

set_rail_analysis_mode -method era_static -power_switch_eco false -generate_movies false -save_voltage_waveforms false -
generate_decap_eco true -accuracy xd -analysis_view View_e8 -process_techgen_em_rules false -enable_rlrp_analysis false -
extraction_tech_file
../../../../apps/prebuilt/eda/designkits/GPDK/gsclib045/lan/flow/t1u1/reference_libs/GPDK045/gsclib045_svt_v4.4/gsclib045/qrc/qx/gpdk04
5.tch -vsrsrc_search_distance 50 -ignore_shorts false -enable_manufacturing_effects false -report_via_current_direction false

setDrawView place

create_power_pads -net VDD GND -auto_fetch

create_power_pads -net VDD GND -auto_fetch

create_power_pads -net VDD GND -auto_fetch

setDrawView place

create_power_pads -net VDD GND -auto_fetch

create_power_pads -net VDD GND -auto_fetch

setDrawView place

create_power_pads -net VDD GND -auto_fetch

create_power_pads -net VDD GND -auto_fetch

create_power_pads -net VDD GND -auto_fetch

create_power_pads -net VDD GND -auto_fetch

setDrawView place

setDrawView place

set_rail_analysis_mode -method era_static -power_switch_eco false -generate_movies false -save_voltage_waveforms false -
generate_decap_eco true -accuracy xd -analysis_view View_e8 -process_techgen_em_rules false -enable_rlrp_analysis false -
extraction_tech_file
../../../../apps/prebuilt/eda/designkits/GPDK/gsclib045/lan/flow/t1u1/reference_libs/GPDK045/gsclib045_svt_v4.4/gsclib045/qrc/qx/gpdk04
5.tch -vsrsrc_search_distance 50 -ignore_shorts false -enable_manufacturing_effects false -report_via_current_direction false

setDrawView place

create_power_pads -clear

setDrawView place

create_power_pads -net VDD -auto_fetch

setDrawView place

create_power_pads -net VDD -vsrsrc_file vdd_e1__.pp

set_pg_nets -net VDD -voltage 1.1 -threshold 1

set_power_data -reset

set_power_data -format current -scale 1 run1/static_VDD.ptiavg

set_power_pads -reset

```

```

set_power_pads -net VDD -format xy -file vdd_e1__.pp

set_package -reset

set_package -spice {} -mapping {}

set_net_group -reset

set_advanced_rail_options -reset

analyze_rail -type net -results_directory ./run1 VDD

setLayerPreference powerNet -color {#0000FF #0010DE #0020BD #00319C #00417B #00525A #006239 #007318 #088300 #299400 #4AA400
#6AB400 #8BC500 #ACD500 #CDE600 #EEF600 #FFF900 #FFED00 #FFE200 #FFD600 #FFCB00 #FFBF00 #FFB400 #FFA800 #FF9500 #FF8000
#FF6A00 #FF5500 #FF4000 #FF2A00 #FF1500 #FF0000}

set_power_rail_display -plot none

setLayerPreference powerNet -color {#0000ff #0010de #0020bd #00319c #00417b #00525a #006239 #007318 #088300 #299400 #4aa400
#6ab400 #8bc500 #acd500 #cde600 #eef600 #fff900 #ffed00 #ffe200 #ffd600 #ffcb00 #ffbf00 #ffb400 #ffa800 #ff9500 #ff8000 #ffa00 #ff5500
#ff4000 #ff2a00 #ff1500 #ff0000}

set_power_rail_display -enable_voltage_sources 0

set_power_rail_display -enable_percentage_range 0

fit

set_power_rail_display -plot none

setLayerPreference powerNet -color {#0000ff #0010de #0020bd #00319c #00417b #00525a #006239 #007318 #088300 #299400 #4aa400
#6ab400 #8bc500 #acd500 #cde600 #eef600 #fff900 #ffed00 #ffe200 #ffd600 #ffcb00 #ffbf00 #ffb400 #ffa800 #ff9500 #ff8000 #ffa00 #ff5500
#ff4000 #ff2a00 #ff1500 #ff0000}

::read_power_rail_results -power_db run1/power_9.db -rail_directory run1/VDD_25C_avg_7 -instance_voltage_window { timing whole } -
instance_voltage_method { worst best avg worstavg }

set_power_rail_display -plot ir

setLayerPreference powerNet -color {#0000ff #0010de #0020bd #00319c #00417b #00525a #006239 #007318 #088300 #299400 #4aa400
#6ab400 #8bc500 #acd500 #cde600 #eef600 #fff900 #ffed00 #ffe200 #ffd600 #ffcb00 #ffbf00 #ffb400 #ffa800 #ff9500 #ff8000 #ffa00 #ff5500
#ff4000 #ff2a00 #ff1500 #ff0000}

set_power_rail_display -range_min 0 -range_max 8.44061 -advance_mode false -filter_max 8.44061 -filter_min 0

setLayerPreference powerNet -color {#0000ff #0010de #0020bd #00319c #00417b #00525a #006239 #007318 #088300 #299400 #4aa400
#6ab400 #8bc500 #acd500 #cde600 #eef600 #fff900 #ffed00 #ffe200 #ffd600 #ffcb00 #ffbf00 #ffb400 #ffa800 #ff9500 #ff8000 #ffa00 #ff5500
#ff4000 #ff2a00 #ff1500 #ff0000}

setLayerPreference powerNet -color {#0000ff #0010de #0020bd #00319c #00417b #00525a #006239 #007318 #088300 #299400 #4aa400
#6ab400 #8bc500 #acd500 #cde600 #eef600 #fff900 #ffed00 #ffe200 #ffd600 #ffcb00 #ffbf00 #ffb400 #ffa800 #ff9500 #ff8000 #ffa00 #ff5500
#ff4000 #ff2a00 #ff1500 #ff0000}

```

ΆΣΚΗΣΗ 7

Έχουν παραχθεί τα ακόλουθα:

elaborate

Verification Report		
Category		Count
1. Non-standard modeling options used:		0
Tri-stated output:	checked	
Revised X signals set to E:	yes	
Floating signals tied to Z:	yes	
Command "add clock" for clock-gating:	not used	
2. Incomplete verification:		1
All primary outputs are mapped:	yes	
Not-mapped DFF/DLAT is detected:	no	
All mapped points are added as compare points:	yes	
All compared points are compared:	yes	
User added black box:	no	
Black box mapped with different module name:	no	
Empty module is not black boxed:	no	
Command "add ignore outputs" used:	yes *	
Always false constraints detected:	no	
Verified pin-equivalent outputs are unmapped:	no	
3. User modification to design:		0
Change gate type:	no	
Change wire:	no	
Primary input added by user:	no	
4. Conformal Constraint Designer clock domain crossing checks recommended:	2	
RTL5.1 Overlapped case items in parallel case statement:	used *	
RTL5.4 Partial case items in full case statement:	used *	
Multiple clocks in the design:	no	
5. Design ambiguity:		0
Duplicate module definition:	no	
Black box due to undefined cells:	no	
Golden design has abnormal ratio of unreachable gates:	no	
Ratio of golden unreachable gates:	0%	
Revised design has abnormal ratio of unreachable gates:	no	
Ratio of revised unreachable gates:	0%	
All primary input bus ordering is consistent:	yes	
All primary output bus ordering is consistent:	yes	
6. Compare Results:		PASS
Total Equivalent modules	= 3	

Syn_generic – Syn_map

Verification Report		
Category		Count
1. Non-standard modeling options used:		1
Tri-stated output:	checked	
Revised X signals set to E:	yes	
Floating signals tied to Z:	no *	
Command "add clock" for clock-gating:	not used	
2. Incomplete verification:		0
All primary outputs are mapped:	yes	
Not-mapped DFF/DLAT is detected:	no	
All mapped points are added as compare points:	yes	
All compared points are compared:	yes	
User added black box:	no	
Black box mapped with different module name:	no	
3. User modification to design:		0
Change gate type:	no	
Change wire:	no	
Primary input added by user:	no	
4. Conformal Constraint Designer clock domain crossing checks recommended:		0
Multiple clocks in the design:	no	
5. Design ambiguity:		0
Duplicate module definition:	no	
Black box due to undefined cells:	no	
Golden design has abnormal ratio of unreachable gates:	no	
Ratio of golden unreachable gates:	1%	
Revised design has abnormal ratio of unreachable gates:	no	
5. Design ambiguity:		0
Duplicate module definition:	no	
Black box due to undefined cells:	no	
Golden design has abnormal ratio of unreachable gates:	no	
Ratio of golden unreachable gates:	1%	
Revised design has abnormal ratio of unreachable gates:	no	
Ratio of revised unreachable gates:	0%	
All primary input bus ordering is consistent:	yes	
All primary output bus ordering is consistent:	yes	
6. Compare Results:		PASS
Number of EQ compare points:	2314	
Number of NON-EQ compare points:	0	
Number of Aborted compare points:	0	
Number of Uncompared compare points :	0	
=====		
pass		

Verification Report		
Category	Count	
1. Non-standard modeling options used:	o	
Tri-stated output:	checked	
Revised X signals set to E:	yes	
Floating signals tied to Z:	yes	
Command "add clock" for clock-gating:	not used	
2. Incomplete verification:	o	
All primary outputs are mapped:	yes	
Not-mapped DFF/DLAT is detected:	no	
All mapped points are added as compare points:	yes	
All compared points are compared:	yes	
User added black box:	no	
Black box mapped with different module name:	no	
Empty module is not black boxed:	no	
Command "add ignore outputs" used:	no	
Always false constraints detected:	no	
3. User modification to design:	o	
Change gate type:	no	
Change wire:	no	
Primary input added by user:	no	
4. Conformal Constraint Designer clock domain crossing checks recommended:	o	
Multiple clocks in the design:	no	
5. Design ambiguity:	o	
Duplicate module definition:	no	
Black box due to undefined cells:	no	
Golden design has abnormal ratio of unreachable gates:	no	
Ratio of golden unreachable gates:	o%	
Revised design has abnormal ratio of unreachable gates:	no	
Ratio of revised unreachable gates:	o%	
All primary input bus ordering is consistent:	yes	
All primary output bus ordering is consistent:	yes	
6. Compare Results:	PASS	
Number of EQ compare points:	2267	
Number of NON-EQ compare points:	o	
Number of Aborted compare points:	o	
Number of Uncompared compare points :	o	
=====		
pass		
// Command: report_statistics		
Mapping and compare statistics		
=====		
Compare Result	Golden	Revised
Root module name	picorv32	picorv32
Primary inputs	102	102
Mapped	102	102
Primary outputs	307	307
Mapped	307	307
Equivalent	307	
State key points	1960	1960
Mapped	1960	1960
Equivalent	1960	
=====		

Παρατηρήσεις: Όπως είναι εμφανές τα Verifications κάνουν PASS και μετά τις συγκρίσεις ο κώδικας παραμένει ίδιος.

Άσκηση 8

Το module που χρησιμοποιήθηκε είναι:

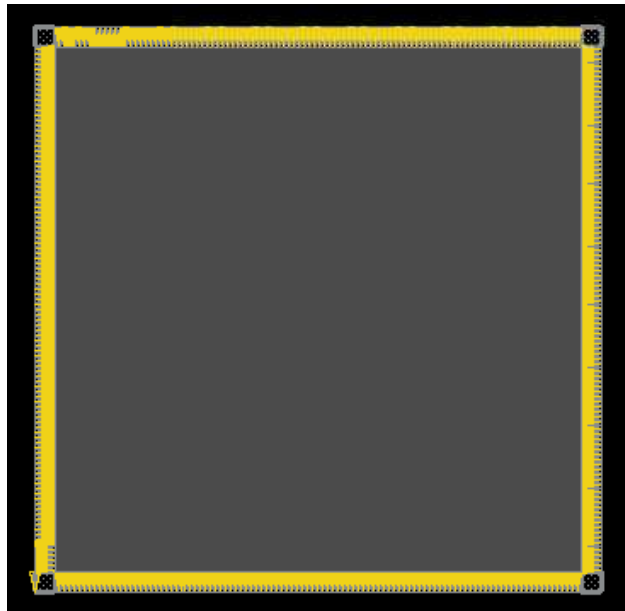
```
module example_module_pads(clk, resetn, trap, mem_valid, mem_instr, mem_ready,
    mem_addr, mem_wdata, mem_wstrb, mem_rdata, mem_la_read,
    mem_la_write, mem_la_addr, mem_la_wdata, mem_la_wstrb, pcpi_valid,
    pcpi_insn, pcpi_rsl, pcpi_rs2, pcpi_wr, pcpi_rd, pcpi_wait,
    pcpi_ready, irq, eoi, trace_valid, trace_data,VSS,VDD);
    input clk, resetn, mem_ready, pcpi_wr, pcpi_wait, pcpi_ready;
    input [31:0] mem_rdata, pcpi_rd, irq;
    output trap, mem_valid, mem_instr, mem_la_read, mem_la_write,
        pcpi_valid, trace_valid;
    output [31:0] mem_addr, mem_wdata, mem_la_addr, mem_la_wdata,

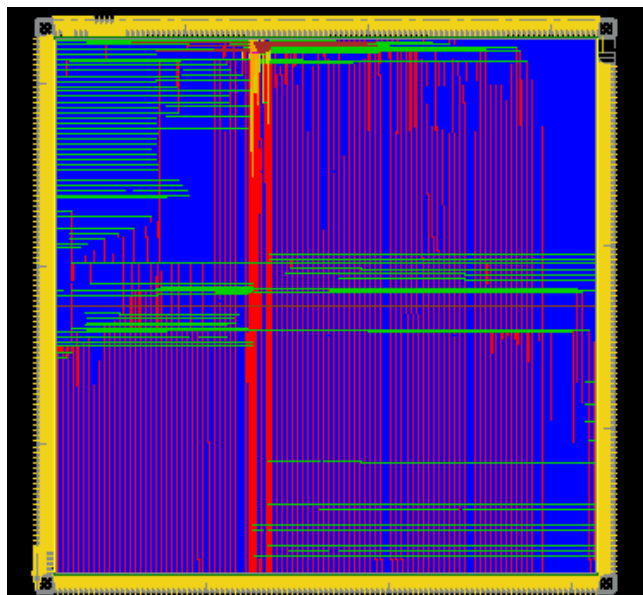
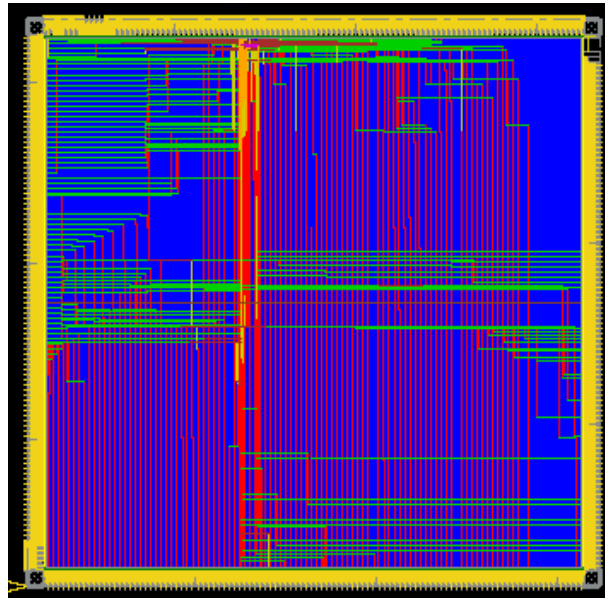
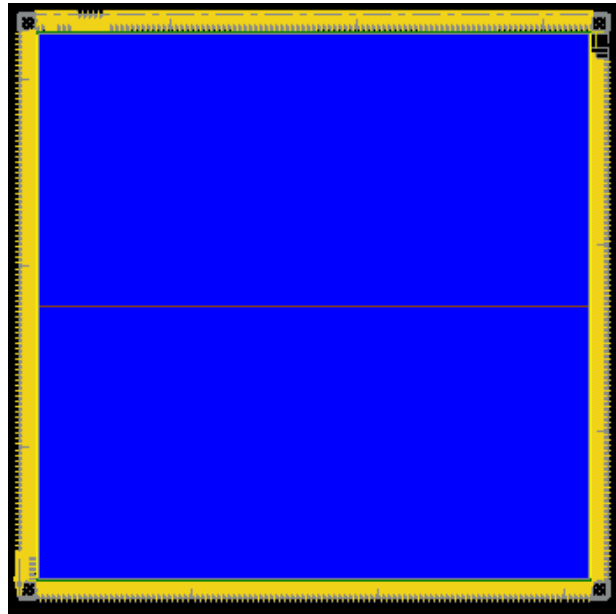
    PADVSS pad_vss(.VSS(VSS), .VDD(VDD), .VDDIOR(VDD), .VSSIOR(VSS));
    PADVDD pad_vdd(.VSS(VSS), .VDD(VDD), .VDDIOR(VDD), .VSSIOR(VSS));

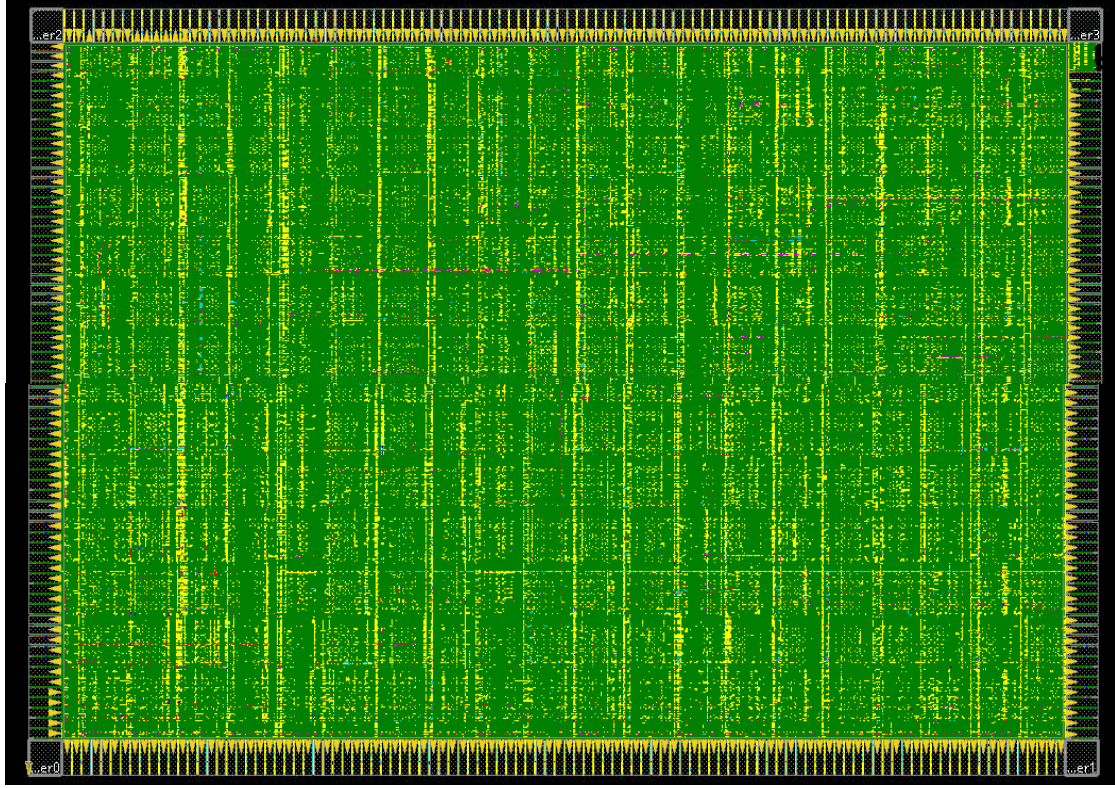
    padIORINGCORNER pad_corner0();
    padIORINGCORNER pad_corner1();
    padIORINGCORNER pad_corner2();
    padIORINGCORNER pad_corner3();

    picorv32 picorv32_design(clk, resetn, trap, mem_valid, mem_instr, mem_ready,
        mem_addr, mem_wdata, mem_wstrb, mem_rdata, mem_la_read,
        mem_la_write, mem_la_addr, mem_la_wdata, mem_la_wstrb, pcpi_valid,
        pcpi_insn, pcpi_rsl, pcpi_rs2, pcpi_wr, pcpi_rd, pcpi_wait,
```

Τα σχήματα που προέκυψαν είναι:







ΑΣΚΗΣΗ 9

```
▶ Checking DFT rules for clock pins
... Processed 250 registers
... Processed 500 registers
... Processed 1000 registers
... Processed 2000 registers
Checking DFT rules for async. pins
... Processed 250 registers
... Processed 500 registers
... Processed 1000 registers
... Processed 2000 registers
Checking DFT rules for shift registers.
Detected 0 DFT rule violation(s)
Summary of check_dft_rules
*****
Number of usable scan cells: 48
Clock Rule Violations:
-----
```

```
Clock Rule Violations:
-----
    Internally driven clock net: 0
    Tied constant clock net: 0
    Undriven clock net: 0
▶ Conflicting async & clock net: 0
    Misc. clock net: 0

Async. set/reset Rule Violations:
-----
    Internally driven async net: 0
    Tied active async net: 0
    Undriven async net: 0
    Misc. async net: 0

Total number of DFT violations: 0

Total number of Test Clock Domains: 1
Number of user specified non-Scan registers: 0
Number of registers that fail DFT rules: 0
Number of registers that pass DFT rules: 2090
Percentage of total registers that are scannable: 100%
```

```

Lint summary
Unconnected/logic driven clocks                                0
Sequential data pins driven by a clock signal                  0
Sequential clock pins without clock waveform                   0
Sequential clock pins with multiple clock waveforms            0
Generated clocks without clock waveform                        0
Generated clocks with incompatible options                     0
Generated clocks with multi-master clock                      0
Paths constrained with different clocks                        0
Loop-breaking cells for combinational feedback                0
Nets with multiple drivers                                    0
Timing exceptions with no effect                               0
Suspicious multi_cycle exceptions                             0
Pins/ports with conflicting case constants                     0
Inputs without clocked external delays                         0
Outputs without clocked external delays                       0
Inputs without external driver/transition                     0
Outputs without external load                                  0
Exceptions with invalid timing start-/endpoints                0

Total: 0

```

```

Async. set/reset Rule Violations:
-----
Internally driven async net: 0
Tied active async net: 0
Undriven async net: 0
Misc. async net: 0
Advanced DFT Rule Violations:
-----
Tristate net contention violation: 0
Potential race condition violation: 0
X-source violation: 0
Warning: There are a total of 1 undriven pins which may act as x-source generators. For the list of pins, use the command 'check_design -undriven -report_scan_pins'.

```

```

Total number of DFT violations: 0

Total number of Test Clock Domains: 1
Number of user specified non-Scan registers: 0
Number of registers that fail DFT rules: 0
Number of registers that pass DFT rules: 1960
Percentage of total registers that are scannable: 100%

```

```

-----
Undriven Port(s)/Pin(s)
-----
No undriven combinational pin in 'picorv32'

No undriven sequential pin in 'picorv32'

No undriven hierarchical pin in 'picorv32'

The following port(s) in design 'picorv32' are undriven
port:picorv32/scan_out
Total number of undriven port(s) in design 'picorv32' : 1

```



```

Async. set/reset Rule Violations:
-----
Internally driven async net: 0
Tied active async net: 0
Undriven async net: 0
Misc. async net: 0

Advanced DFT Rule Violations:
-----
Tristate net contention violation: 0
Potential race condition violation: 0
X-source violation: 0

Total number of DFT violations: 0

Total number of Test Clock Domains: 1
Number of user specified non-Scan registers: 0
Number of registers that fail DFT rules: 0
Number of registers that pass DFT rules: 1960
Percentage of total registers that are scannable: 100%
0

```

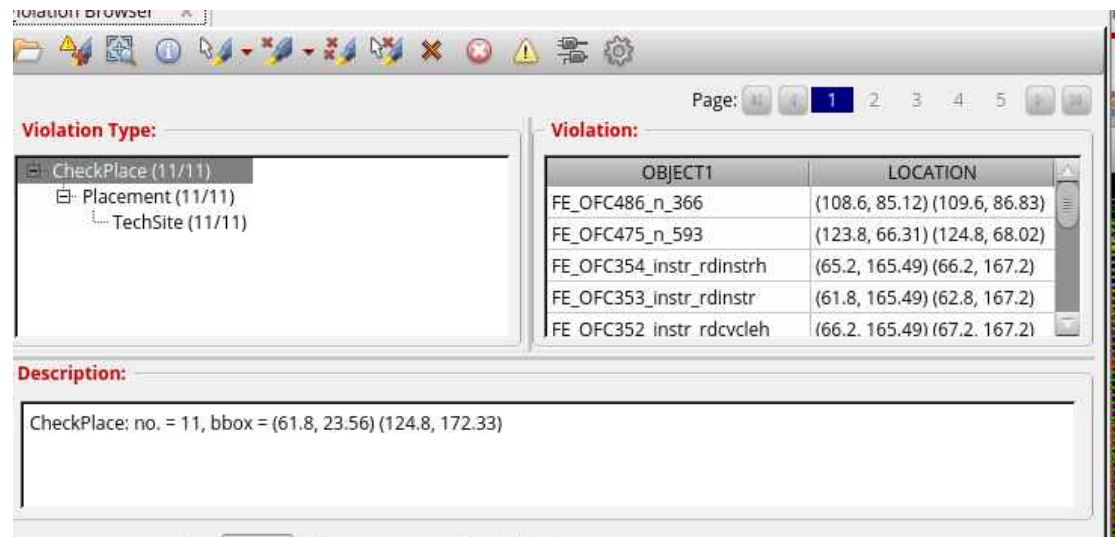
STAGES	AREA (μm^2)	GA TES	SLA CK (ns)	Inter nal P (W)	Switc hing P (W)	Leakag e P(W)	Total POWER (W)
INITIAL	82880.167	26080	6939	4.38724e-04	1.25510e-03	1.38930e-06	1.69522e-03
MAPPING	48975.666	10050	6095	1.12738e-03	3.25224e-03	2.14786e-06	4.38177e-03
OPTIMISATION	48881.258	9910	6015	1.13179e-03	3.23246e-03	2.15999e-06	4.36641e-03

Παρατηρείται ότι με τον map και opt το area μειώνεται σημαντικά γεγονός που συμβάλλει θετικά στην επιτέλεση των λειτουργιών του κυκλώματος. Επιπλέον το slack μειώνεται (γίνεται λίγο πιο αργό το κύκλωμα) ενώ το Power αυξάνεται σημαντικά.

VIOLATIONS

ΑΣΚΗΣΗ 1

Παρουσιάζονται στον BUF2



ΑΣΚΗΣΗ 2

Παρουσιάζονται στον BUF2



ΑΣΚΗΣΗ 3

Violation Browser — cn98.it.auth.gr

Violation Browser

Page: 1 2 3 4 5

Violation Type:

Violation:

LOCATION

Description:

ΑΣΚΗΣΗ 4

Violation Browser — cn98.it.auth.gr

Violation Browser

Page: 1 2 3 4 5

Violation Type:

Violation:

LOCATION

Description:

ΑΣΚΗΣΗ 5

Violation Browser — cn98.it.auth.gr

Violation Browser

Page: 1 2 3 4 5

Violation Type:

Violation:

LOCATION

Description:

ΑΣΚΗΣΗ 6

Violation Browser — cn98.it.auth.gr

Violation Browser

Page: 1 2 3 4 5

Violation Type:

Violation:

LOCATION

Description: