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ID: 2001254

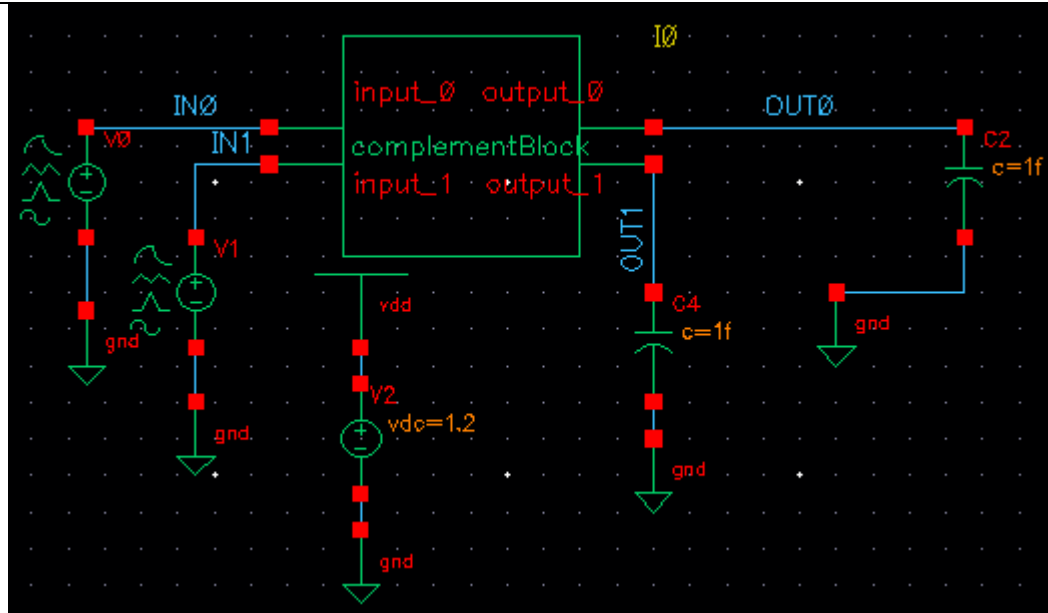
Technology used: **gpdk090**

Logical Unit Blocks

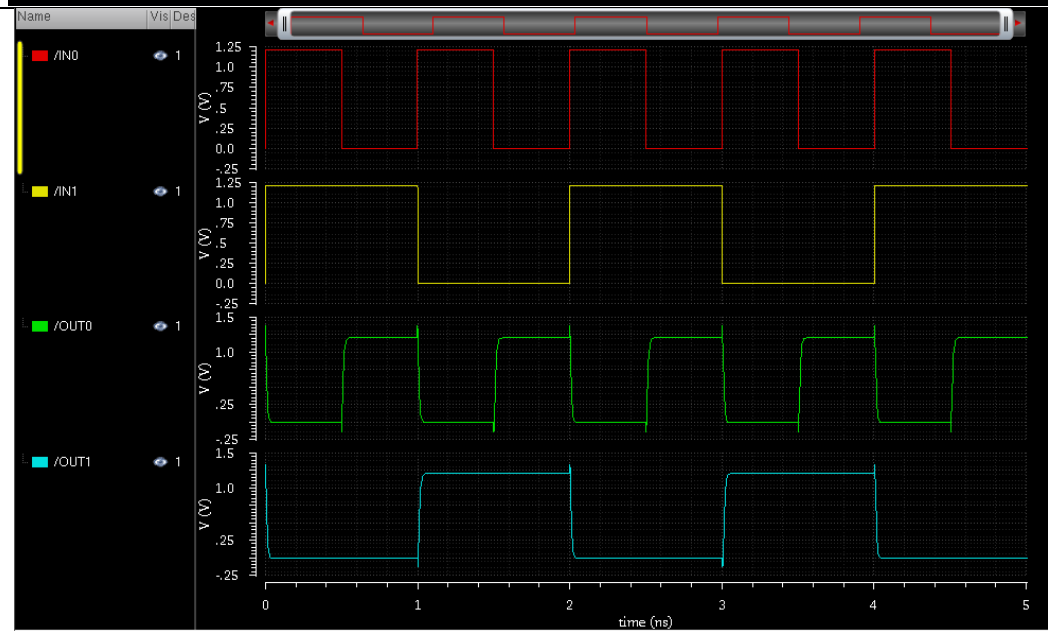
| | Schematic | Symbol |
|----------|-----------|--------|
| Inverter | | |

| | | |
|------------------|--|--|
| Complement block | | |
|------------------|--|--|

TB schematic



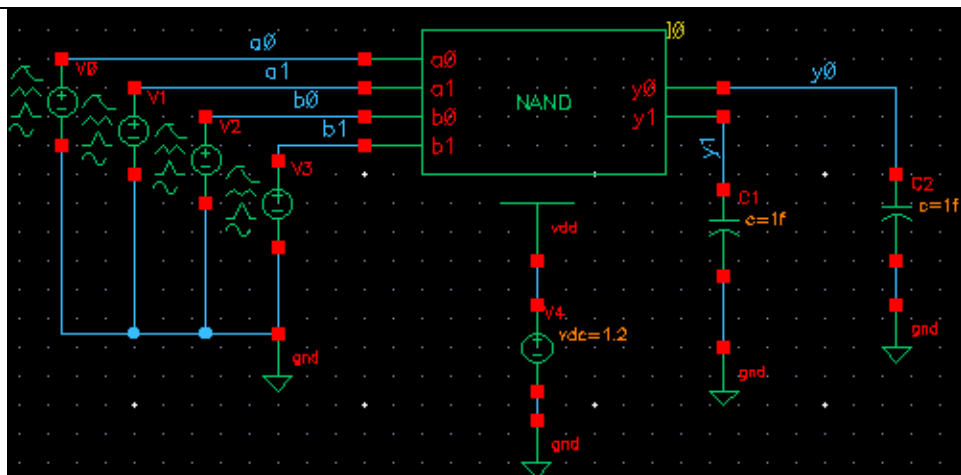
Inverter 2-bit Wave forms



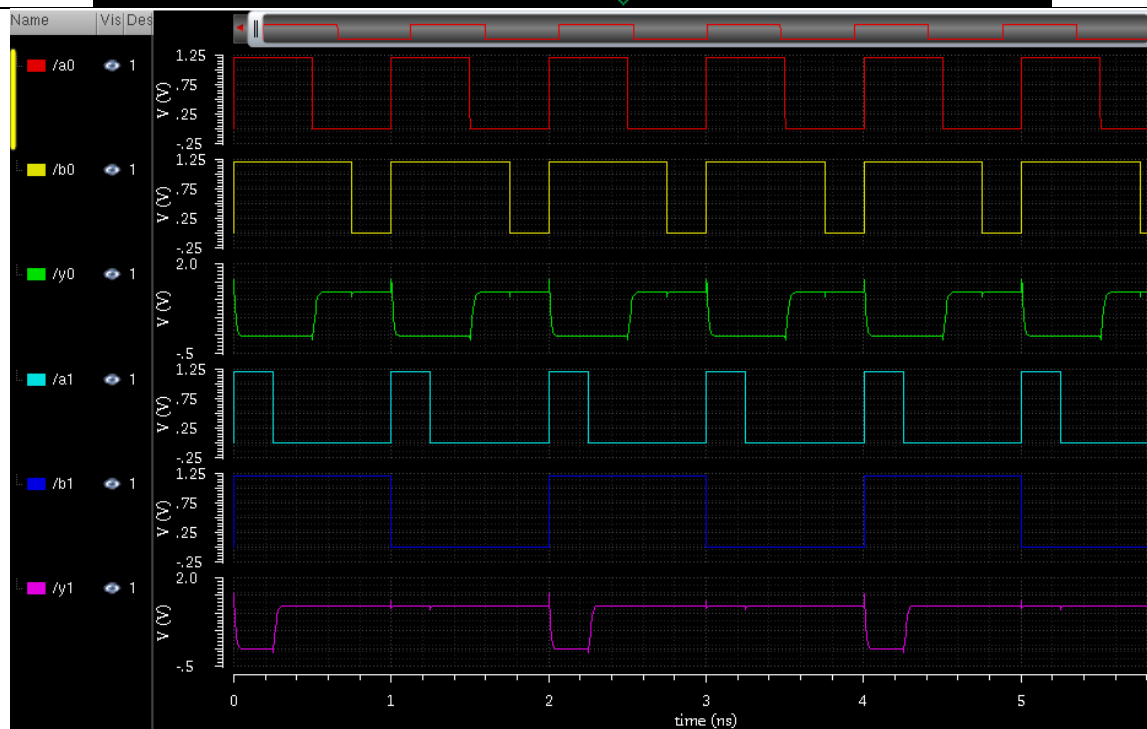
| | Schematic | Symbol |
|------|-----------|--------|
| NAND | | |

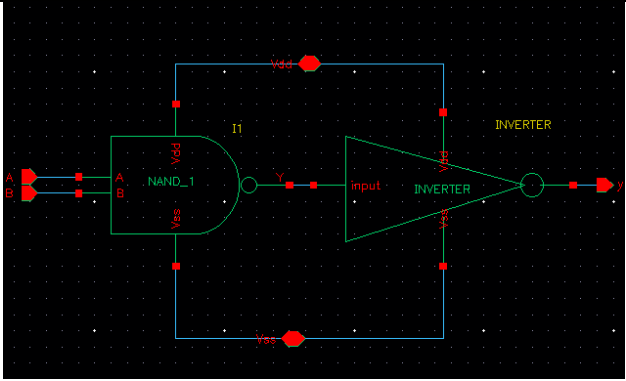
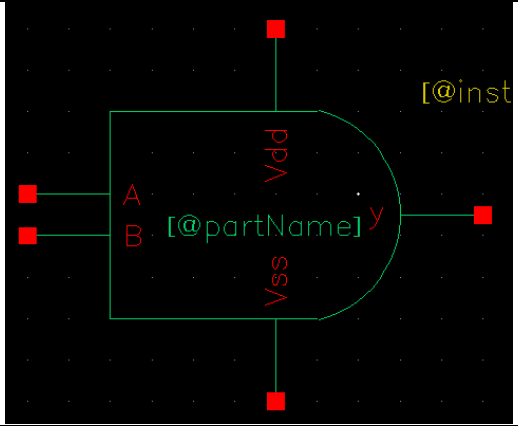
| | | |
|------------|--|--|
| NAND 2-bit | | |
|------------|--|--|

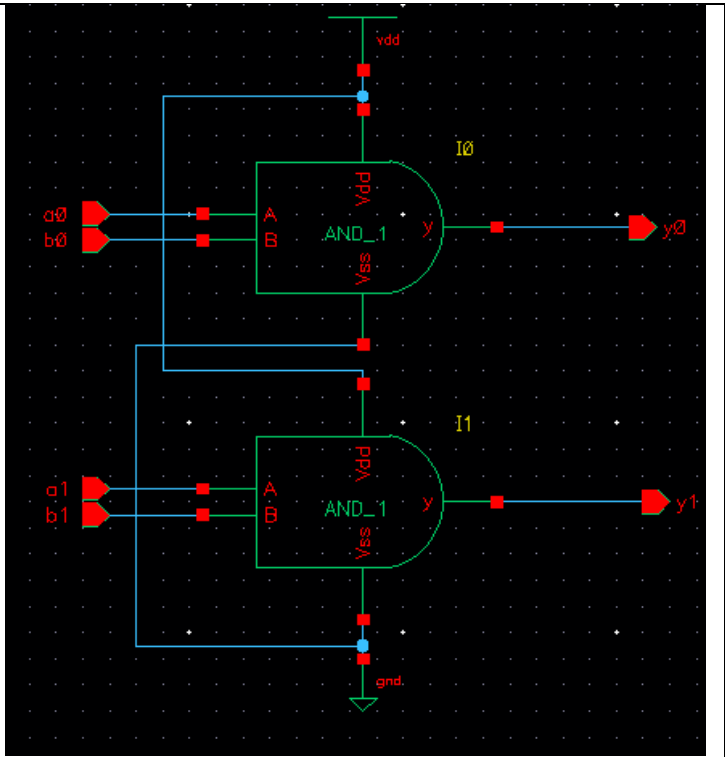
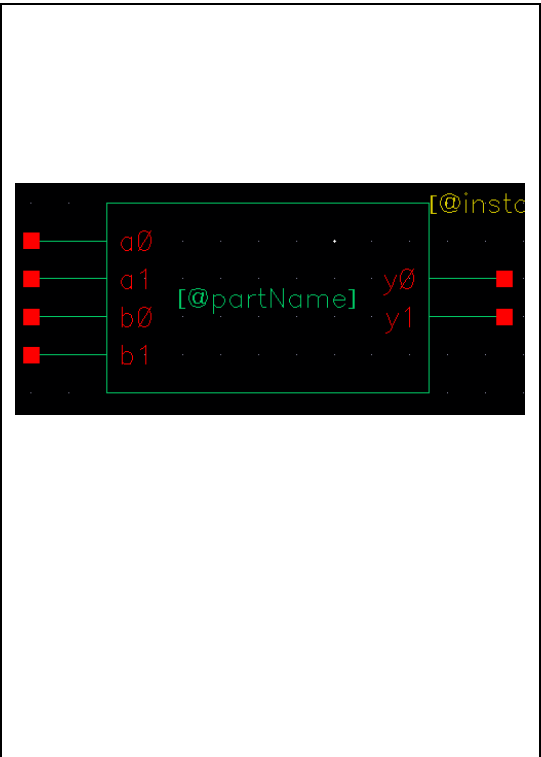
TB schematic



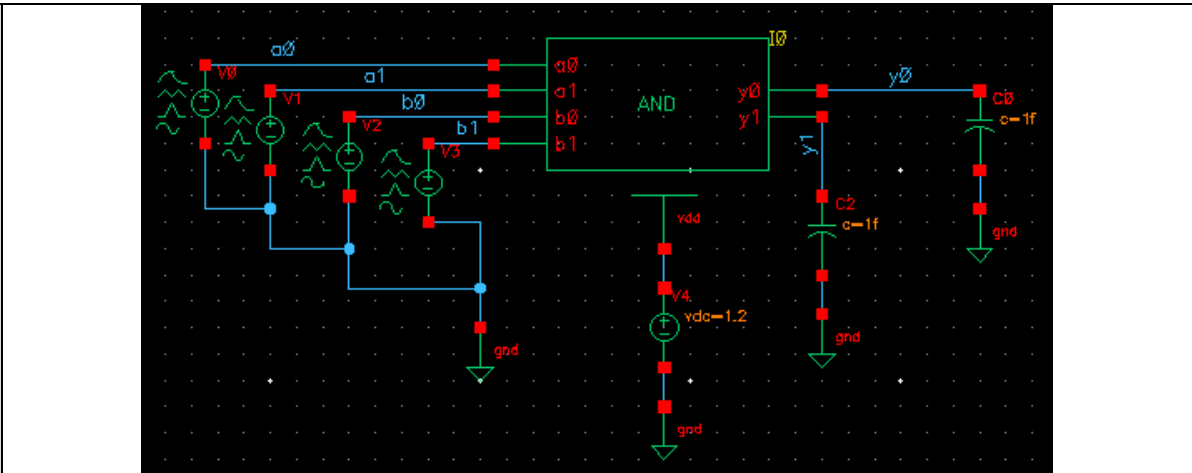
NAND 2-bit Waveforms



| gate | Schematic | Symbol |
|------|---|--|
| AND |  |  |

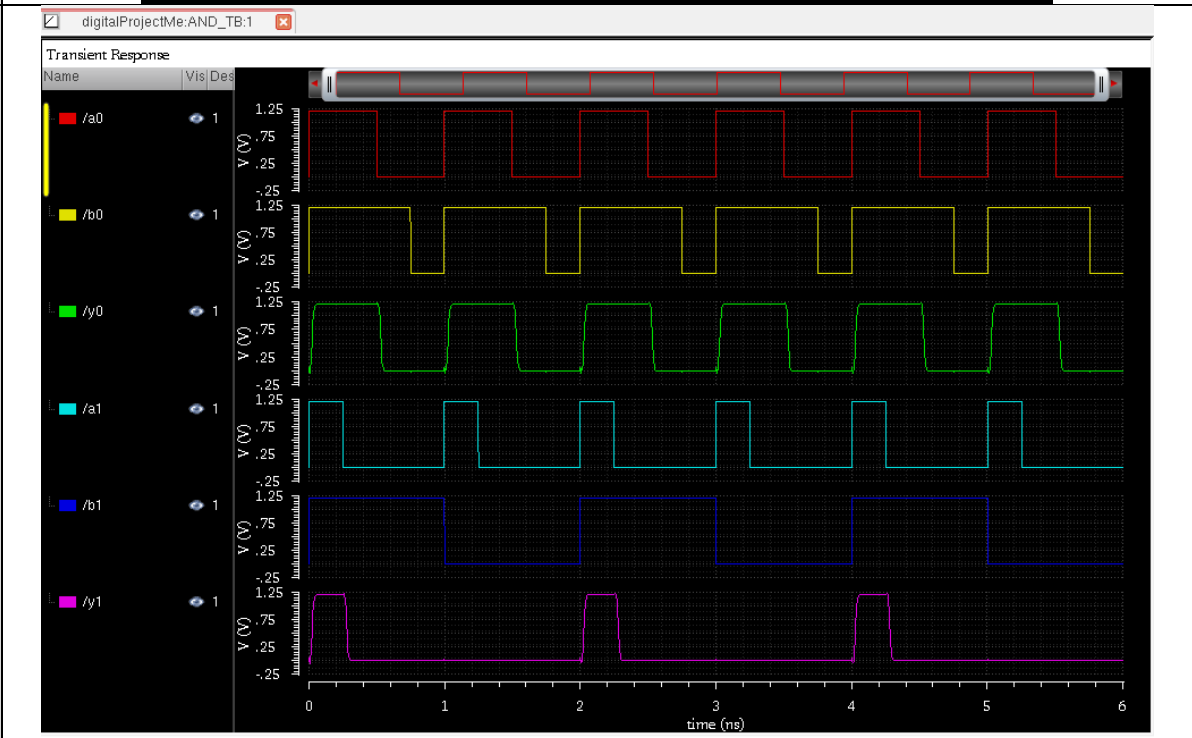
| | | |
|--------------|--|---|
| AND 2-bit |  |  |
|--------------|--|---|

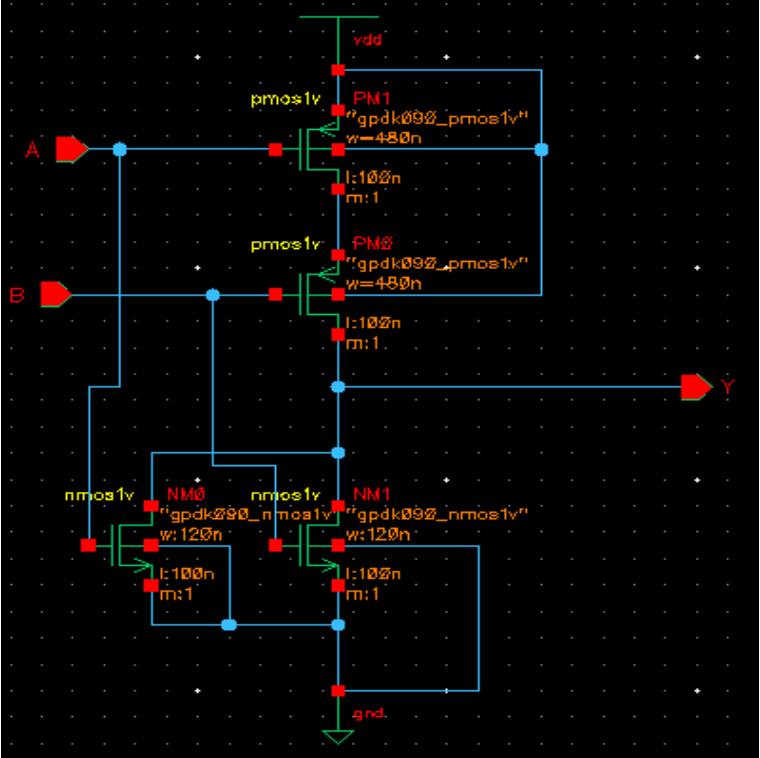
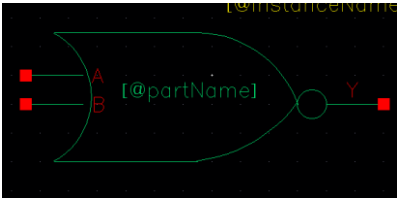
**TB
AND 2-bit**

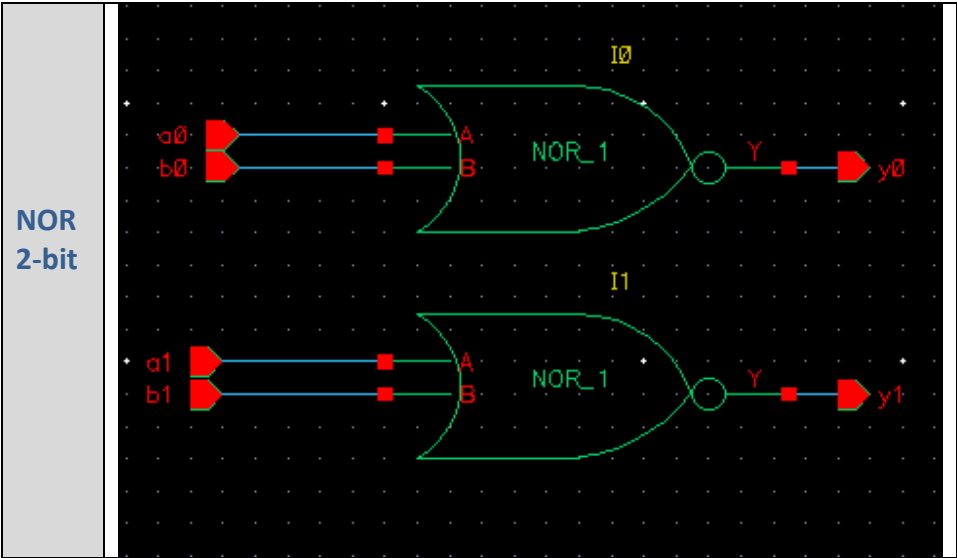


AND 2-bit

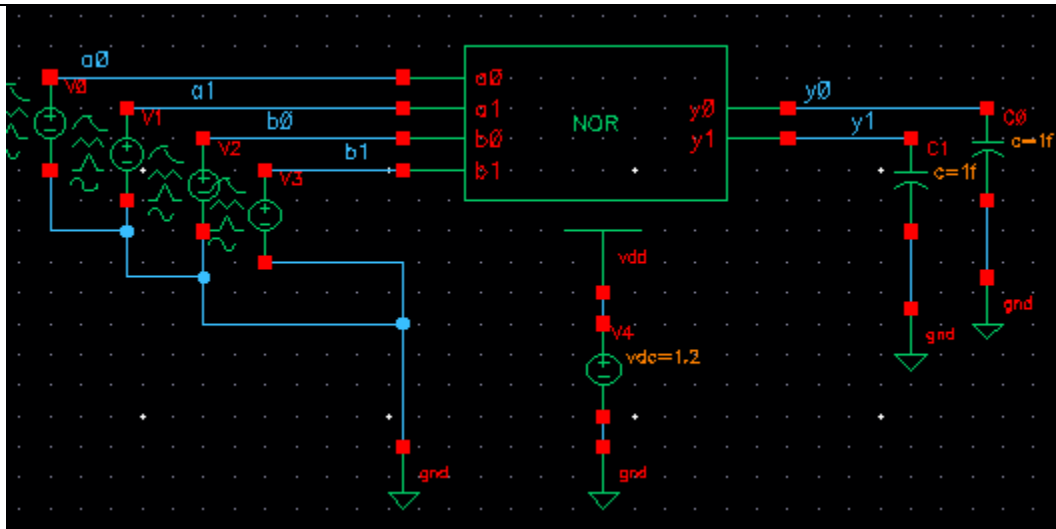
Wave forms



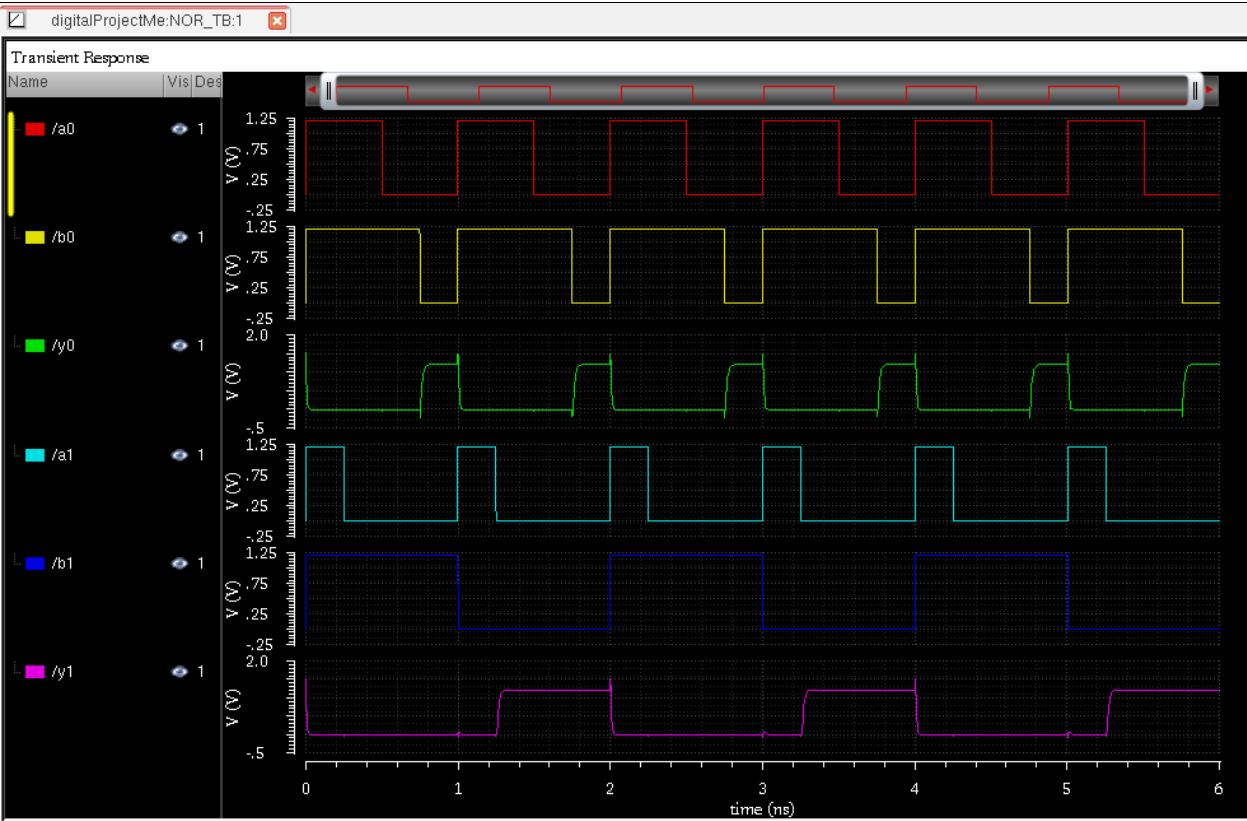
| gate | Schematic | Symbol |
|------|--|---|
| NOR |  |  |

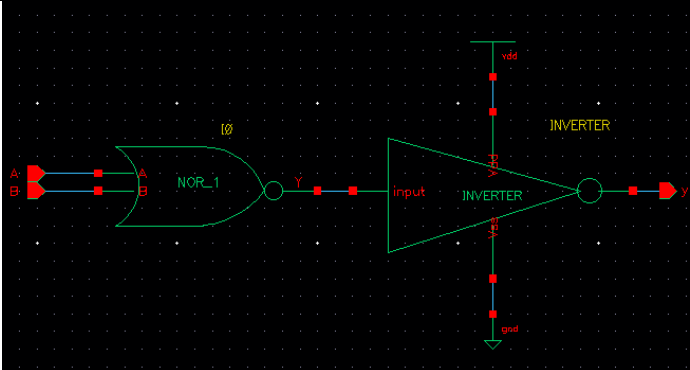
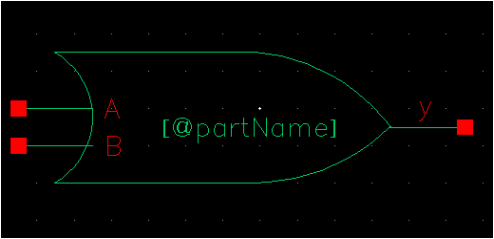


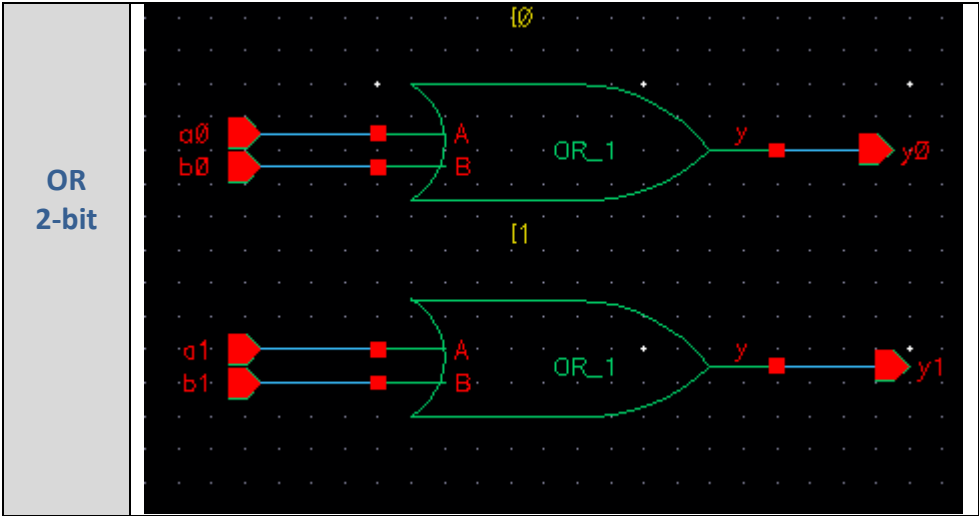
TB NOR



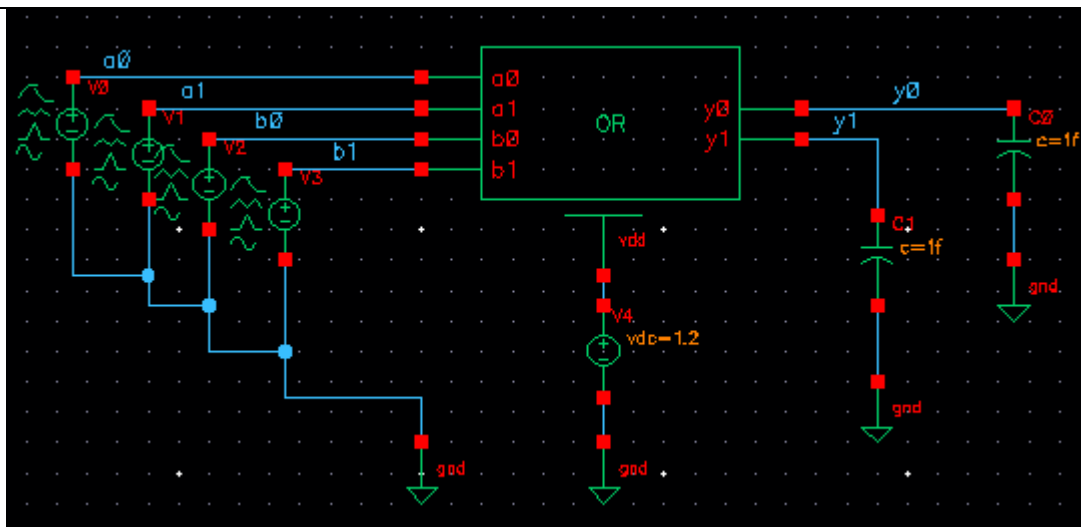
NOR 2-bit Wave form s



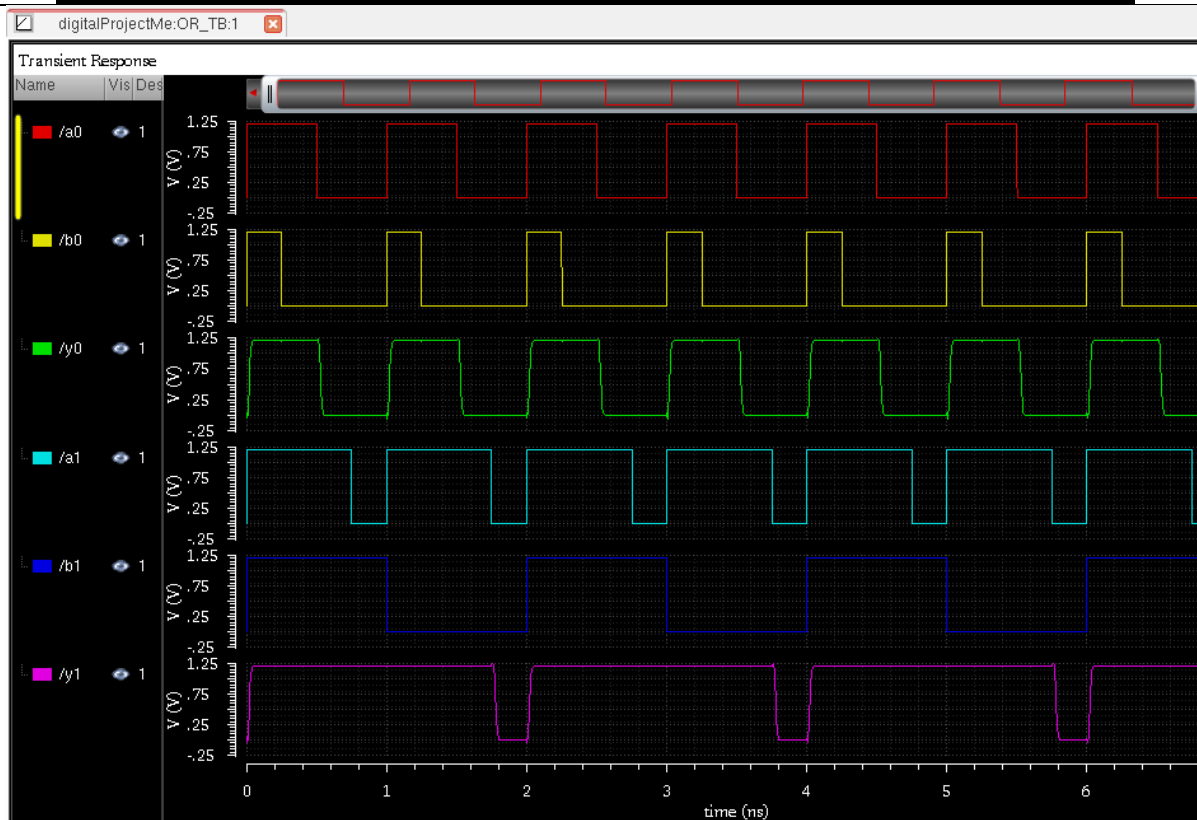
| gate | Schematic | Symbol |
|------|--|---|
| OR |  <p>The schematic shows a 1-bit OR gate implementation on a grid. It consists of a NOR gate labeled 'NOR_1' with inputs 'A' and 'B'. The output of the NOR gate is connected to the input of the first inverter, which is labeled 'INVERTER'. The output of the first inverter is connected to the input of the second inverter, which is also labeled 'INVERTER'. The final output of the second inverter is labeled 'y'. Power supply connections for 'vdd' and 'gnd' are shown at the top and bottom of the circuit.</p> |  <p>The symbolic representation of a 1-bit OR gate. It shows a standard OR gate symbol with two inputs labeled 'A' and 'B', and one output labeled 'y'. The symbol is labeled with the part name '[@partName]'.</p> |



TB
OR 2-bit



OR 2-bit
Waveforms

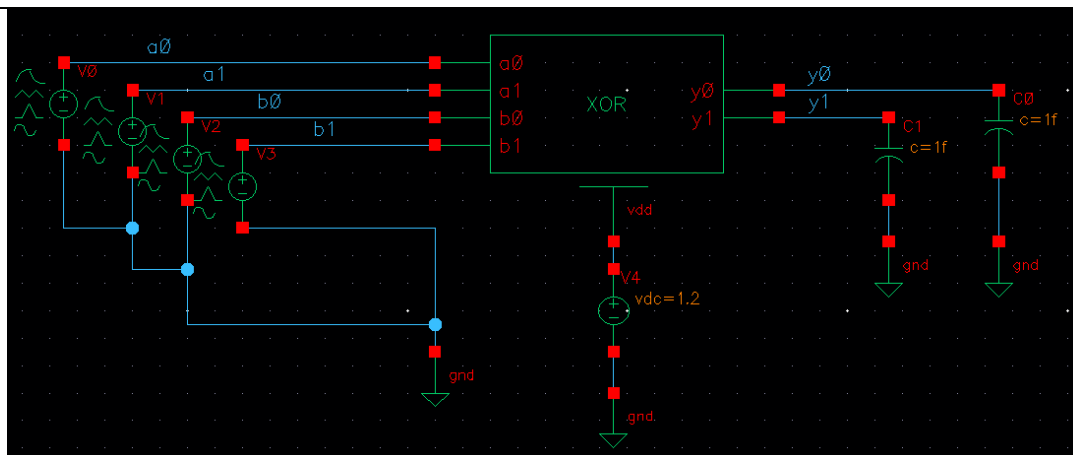


| Gate | Schematic |
|------|-----------|
| XOR | |

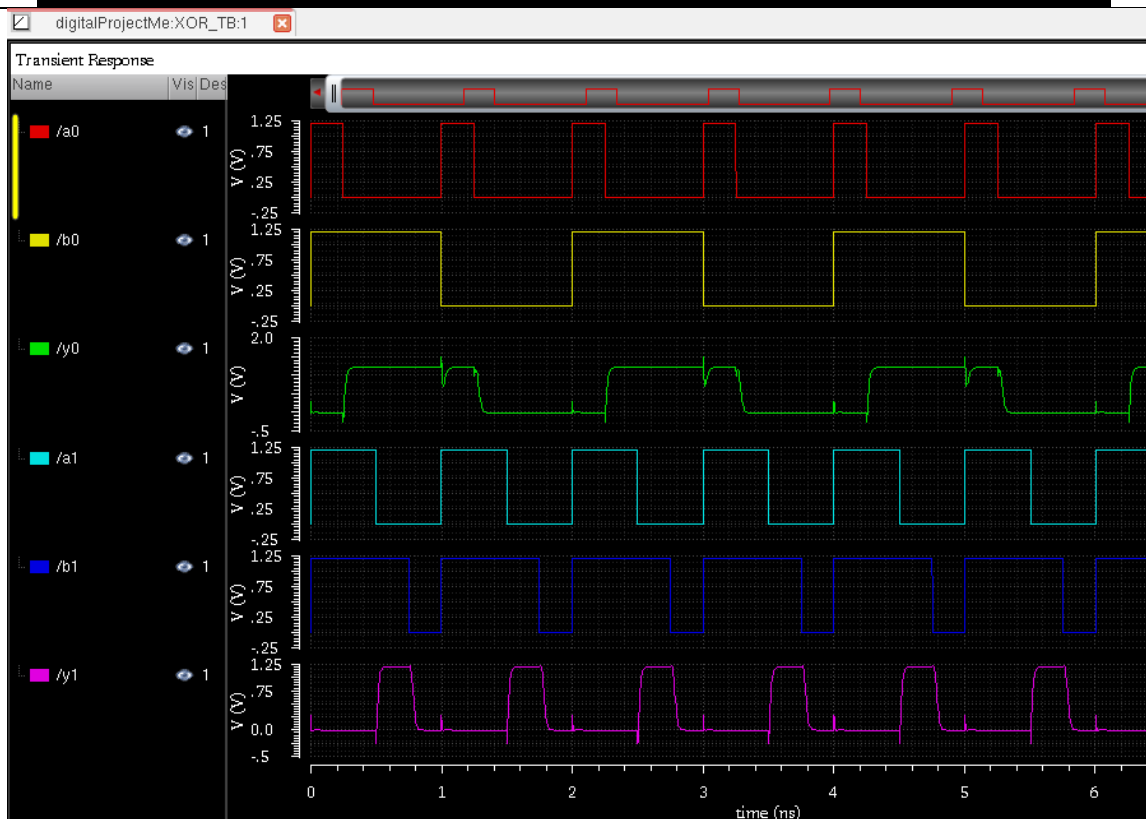
| Symbol |
|--------|
| |

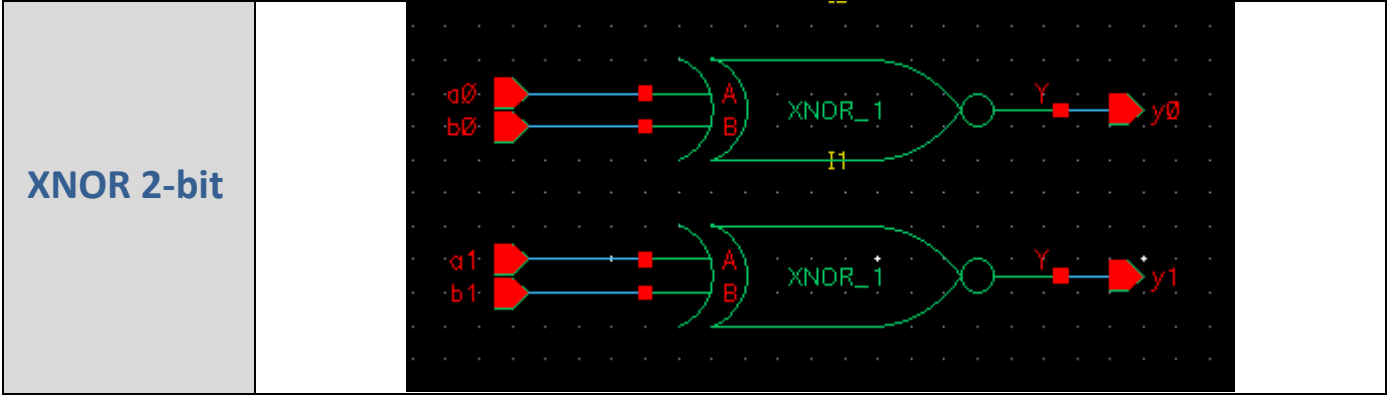
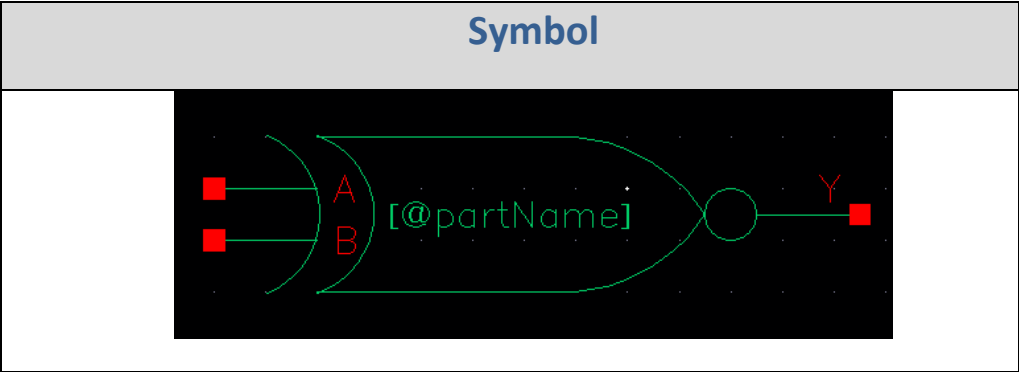
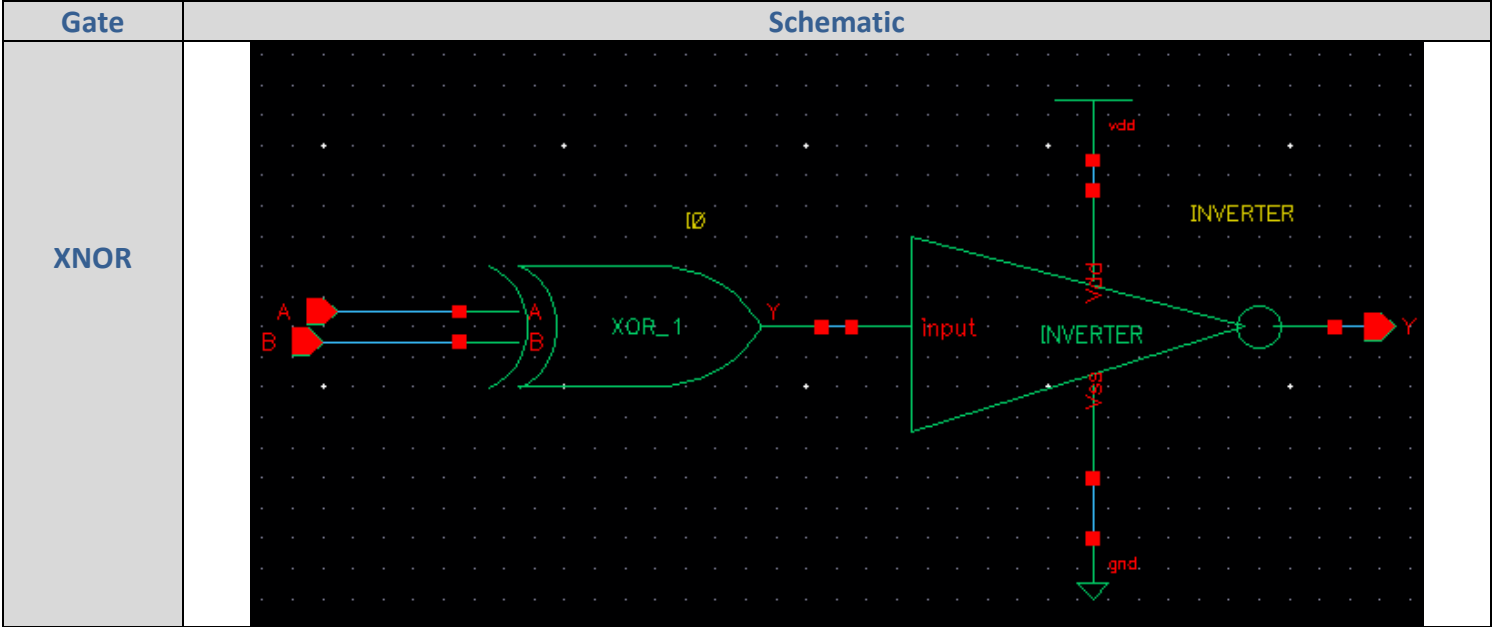
| | |
|-----------|--|
| XOR 2-bit | |
|-----------|--|

XOR 2-bit TB

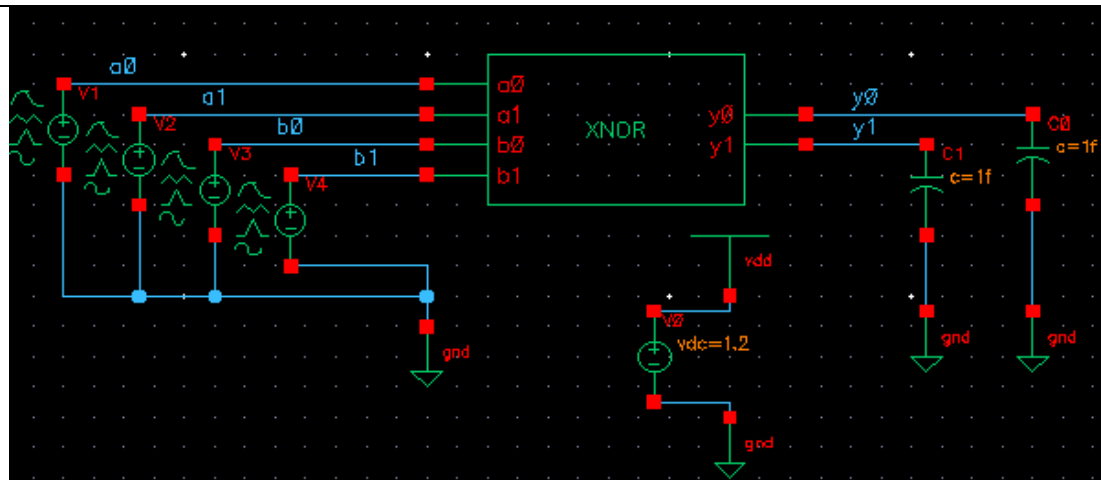


XOR 2-bit waveforms

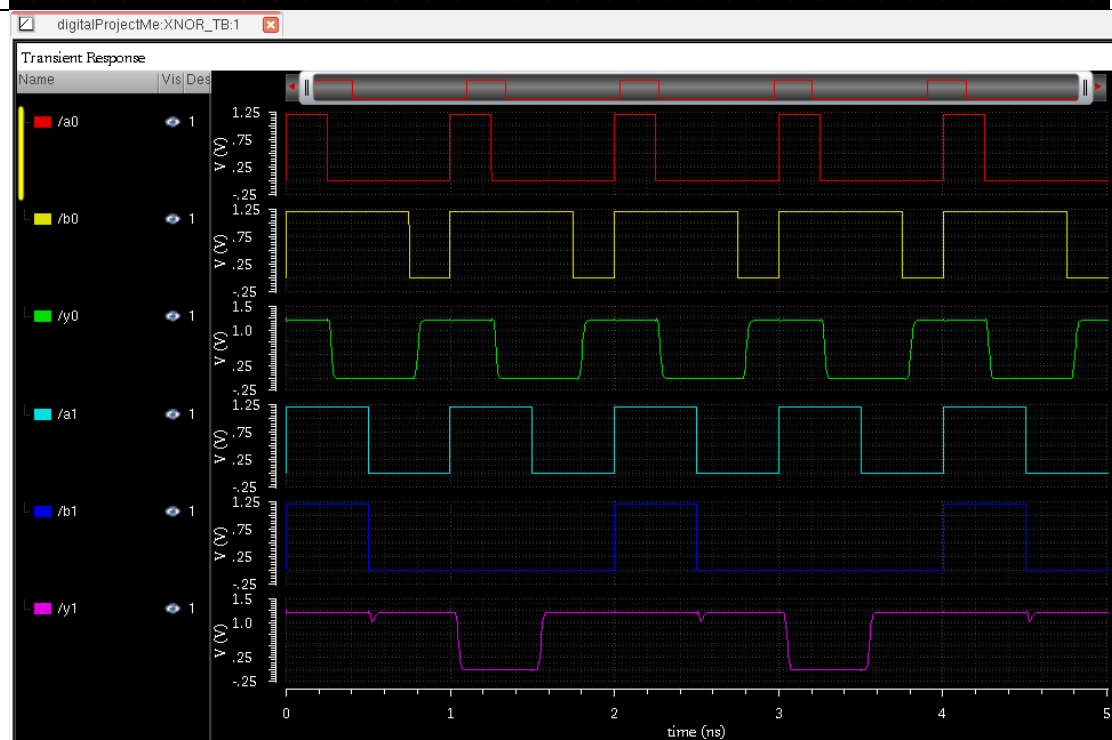




XNOR 2-bit TB

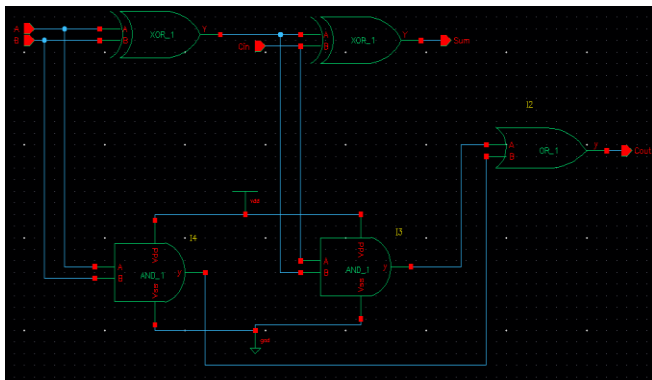


XNOR 2-bit Waveform

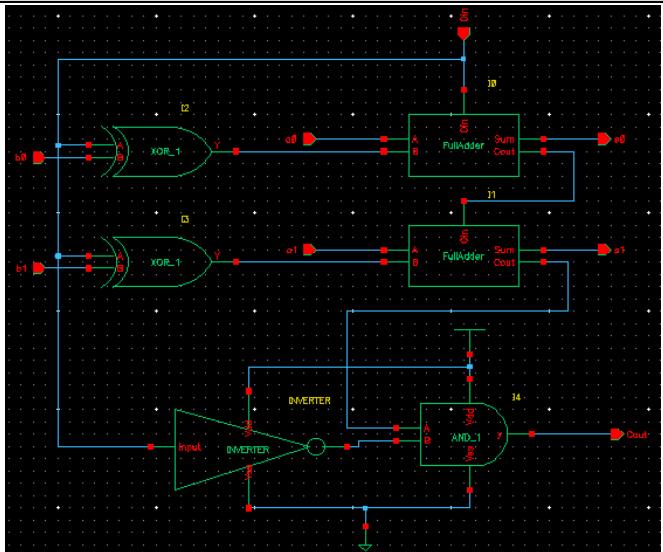


Arithmetic Unit Blocks

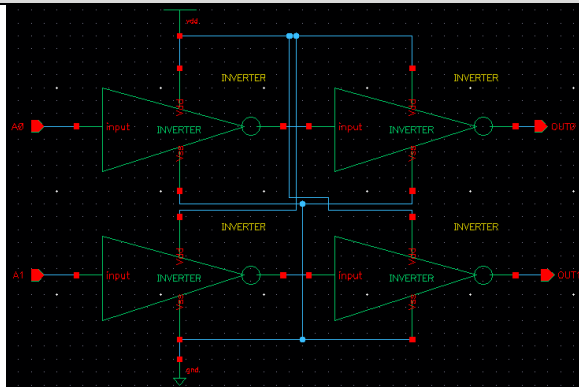
1-bit Full adder schematic



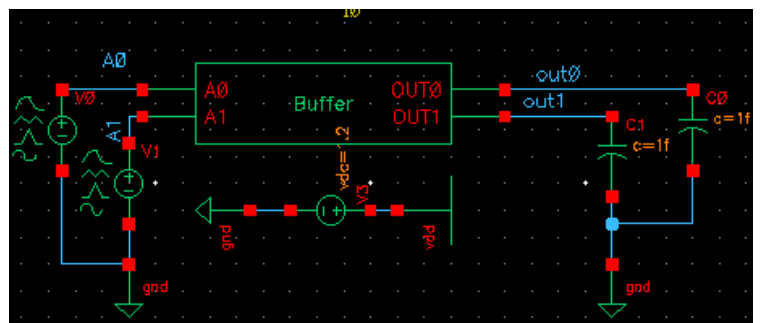
2-bit Full adder / Subtractor schematic



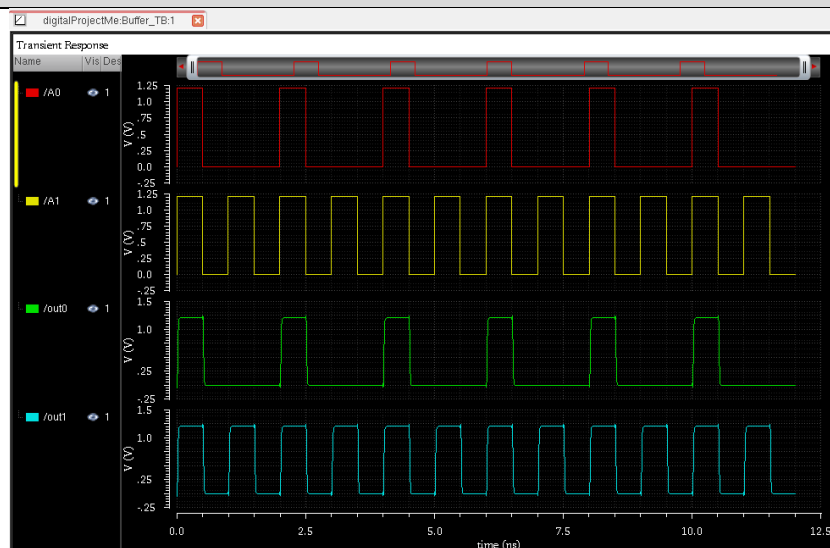
2-bit Buffer Schematic



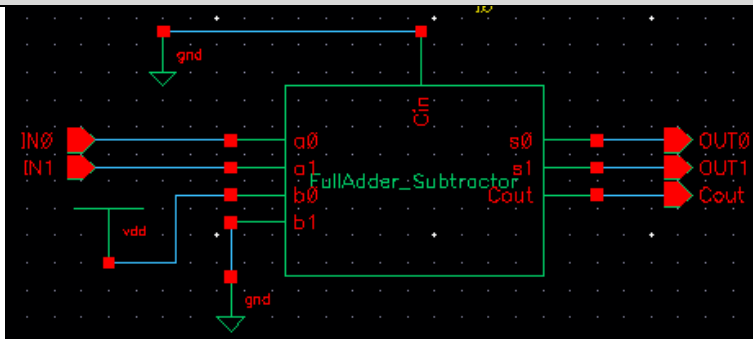
Testbench



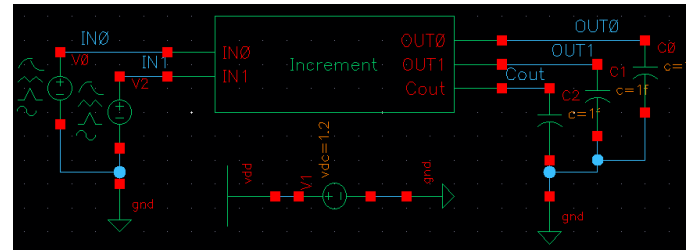
2-bit Buffer Waveforms



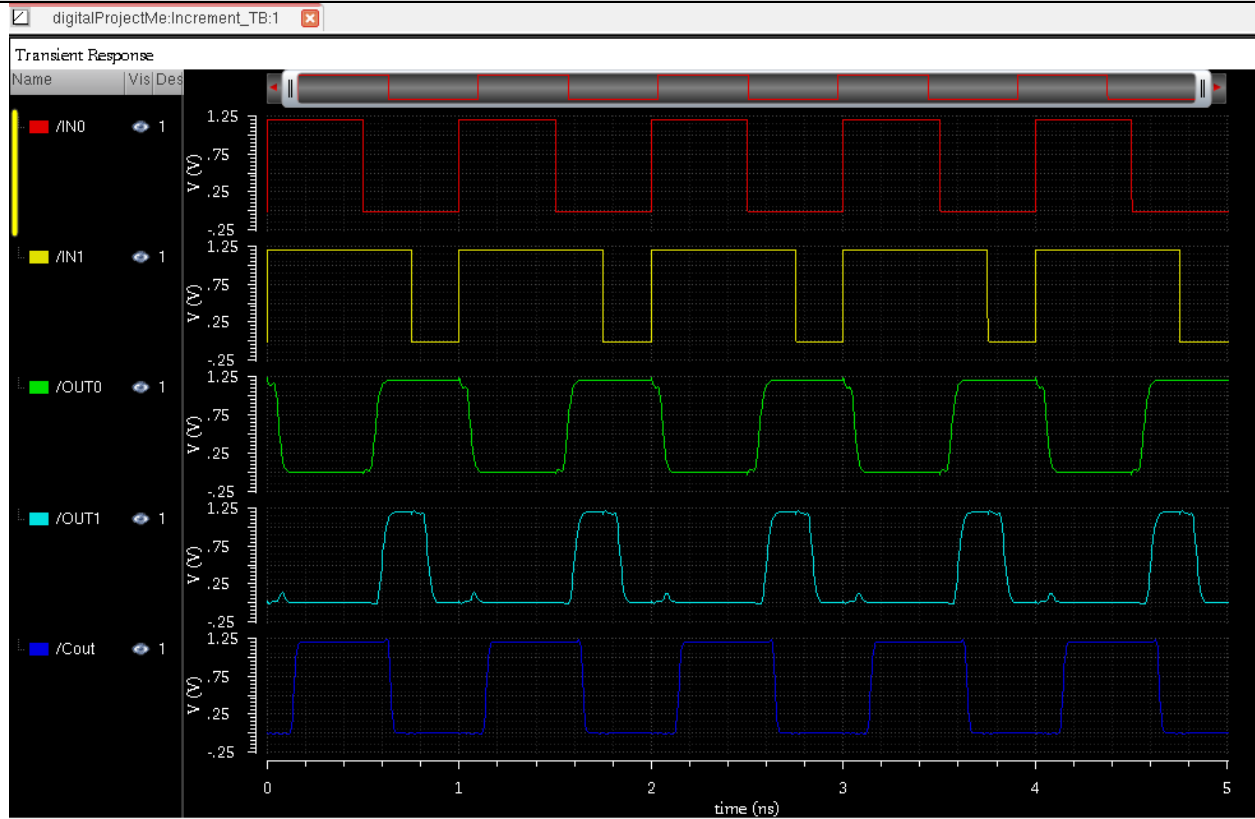
Increment Schematic



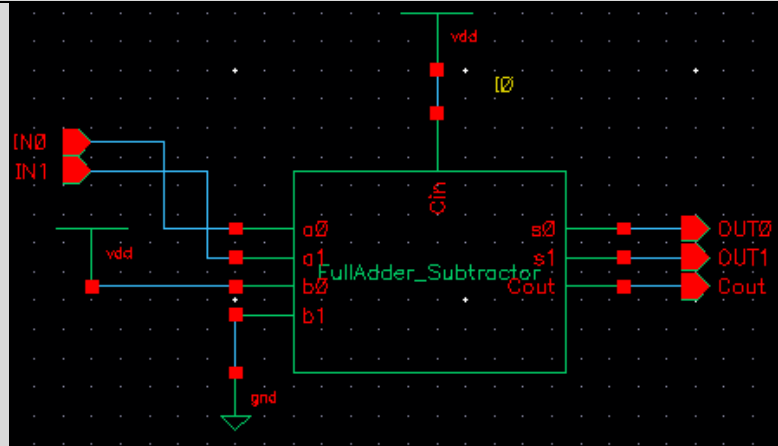
Increment Testbench



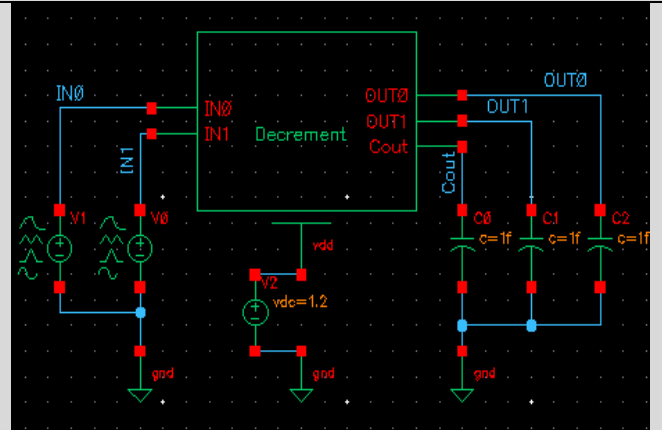
Increment waveforms



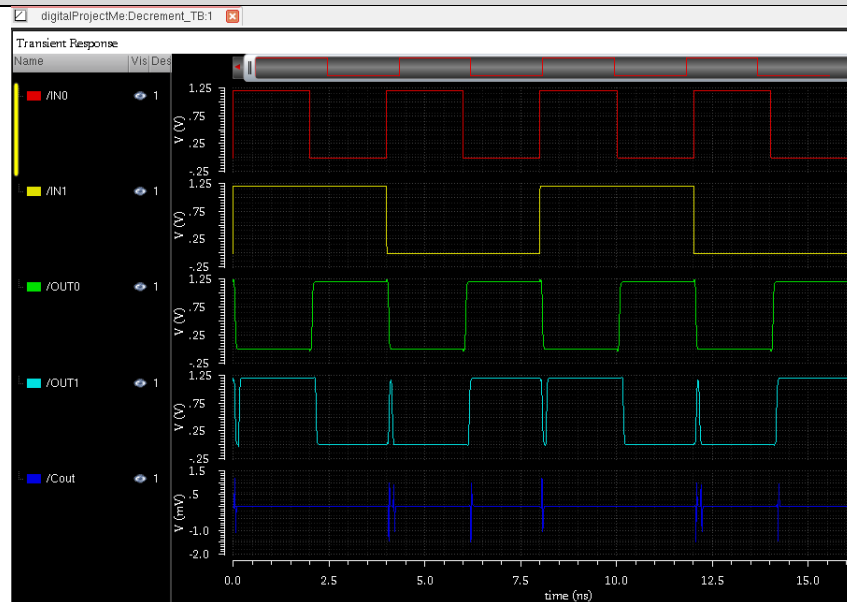
Decrement Schematic



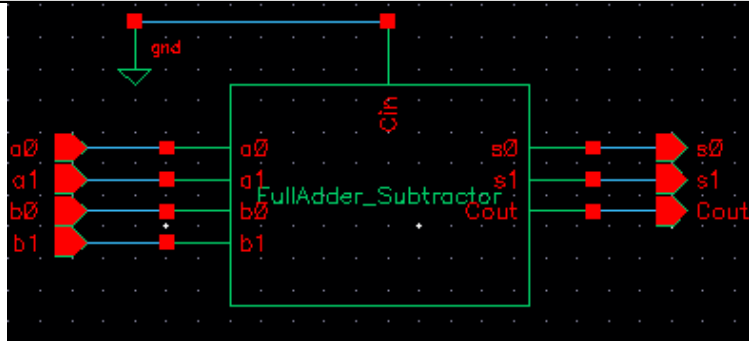
Decrement Testbench



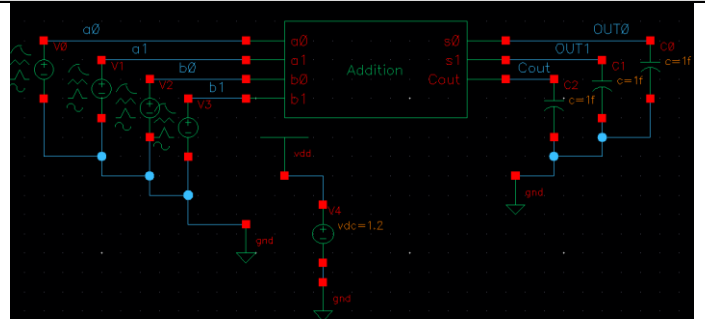
Decrement Waveforms



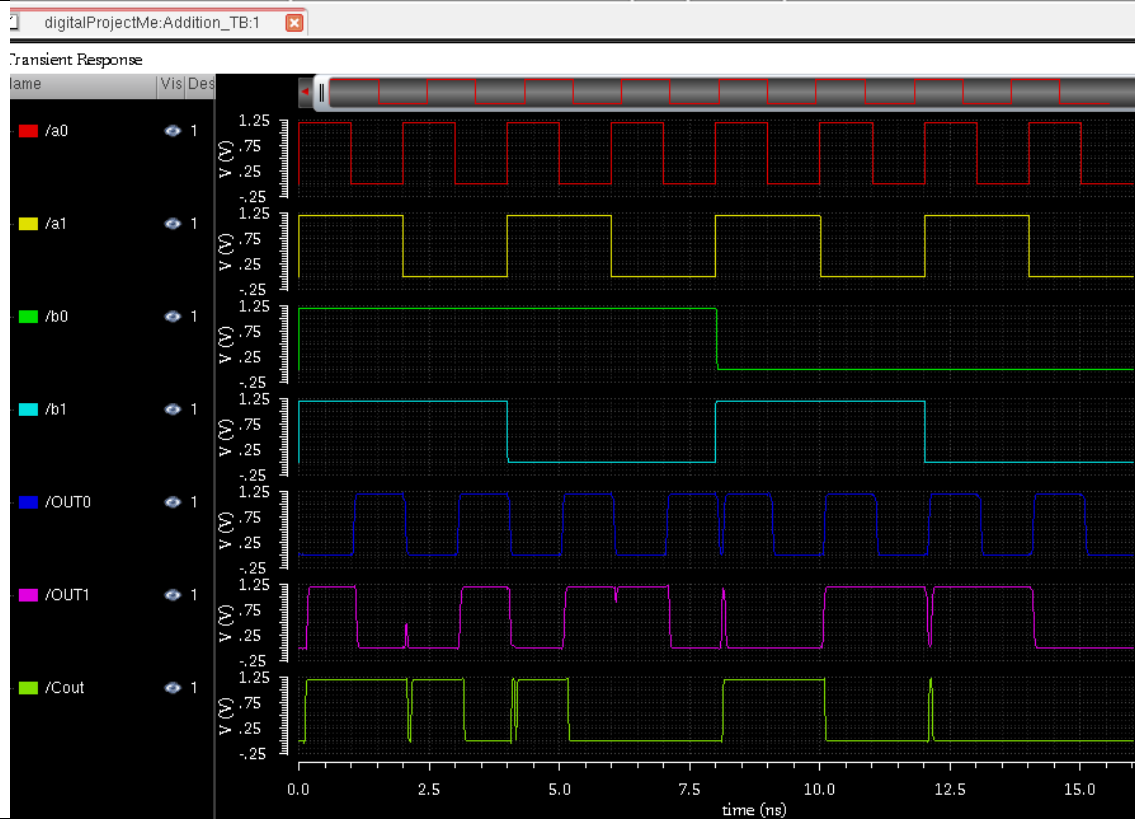
a+b schematic



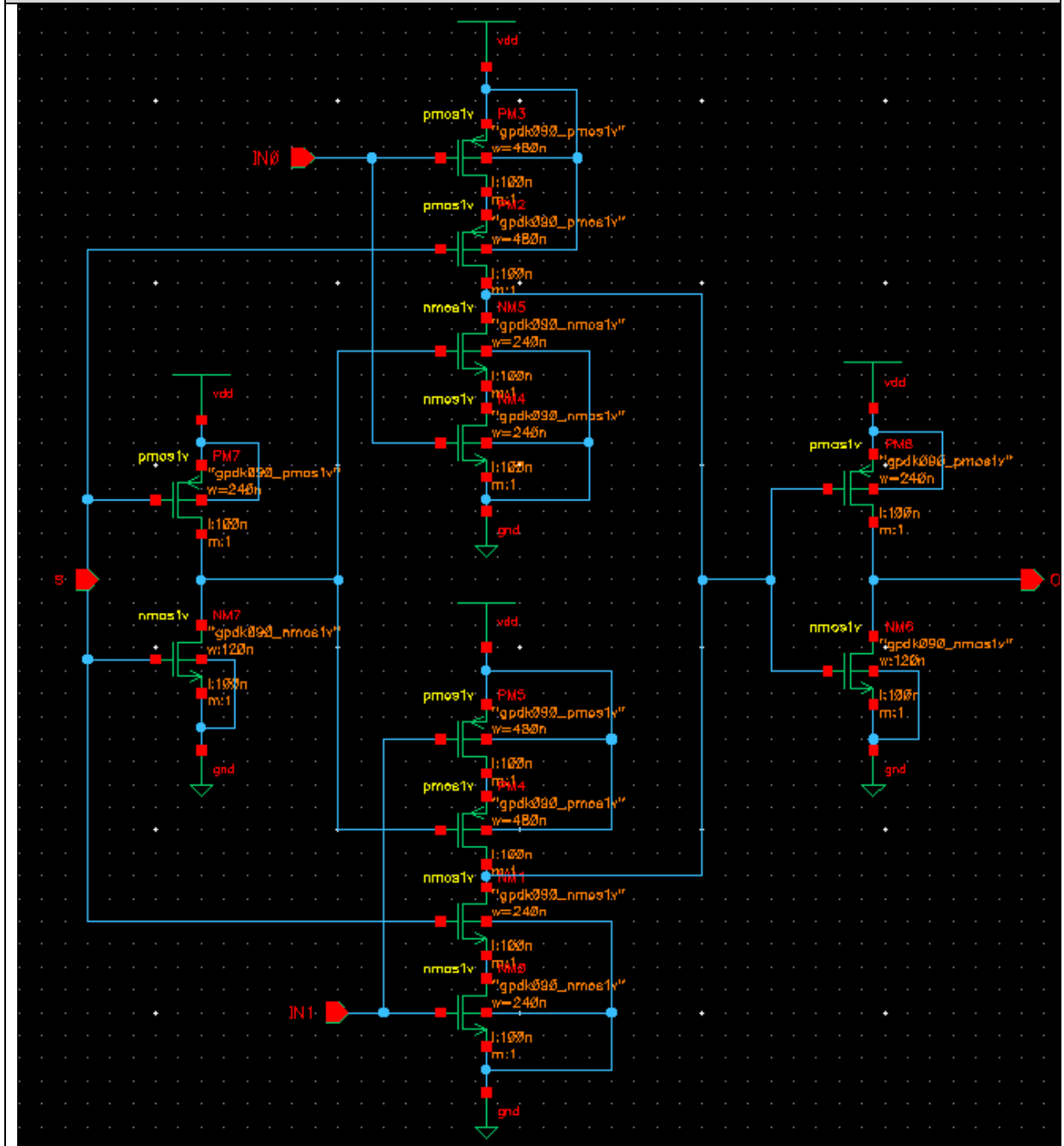
a+b Testbench



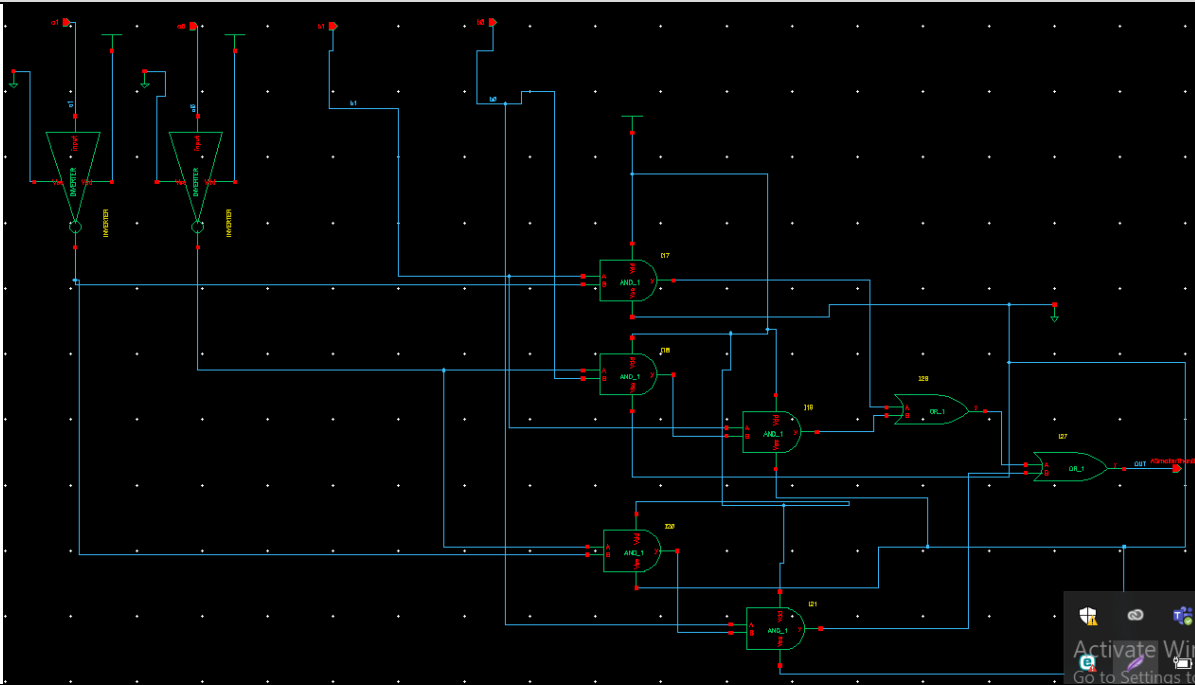
a+b Waveforms



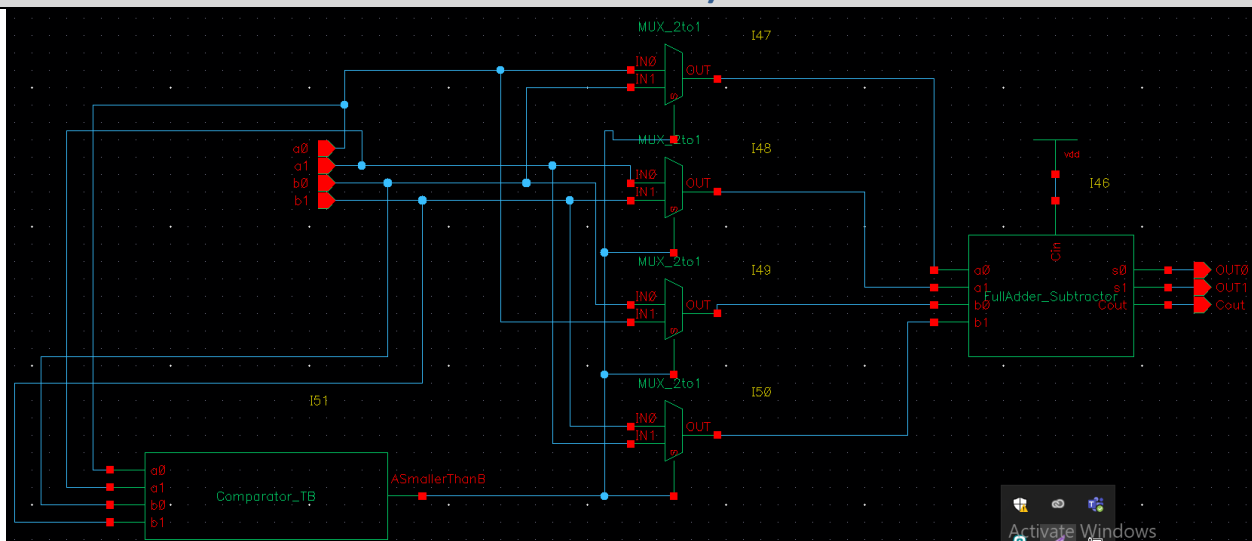
MUX 2:1 Schematic



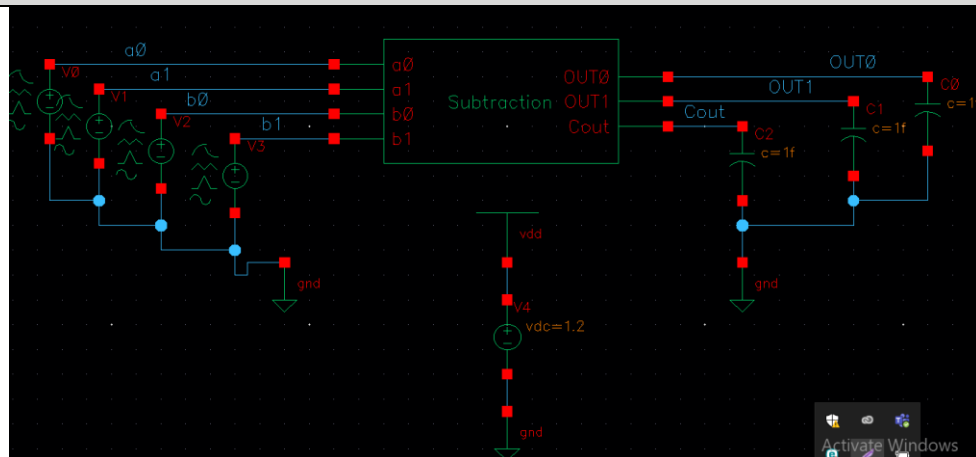
Comparator Schematic (Output = 1 if A<B)



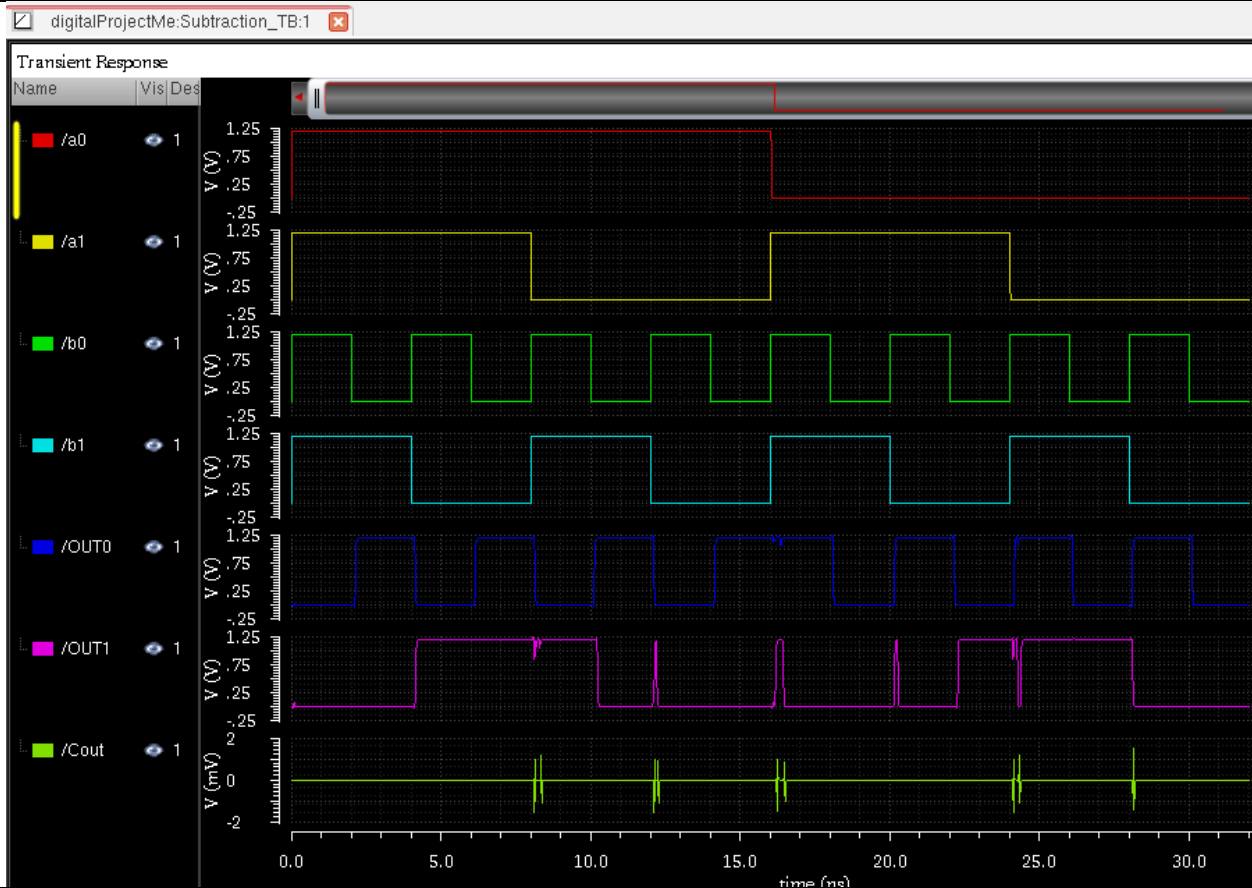
Subtraction Schematic (Comparing which is smaller and then subtracting it from the other)



Subtraction Testbench

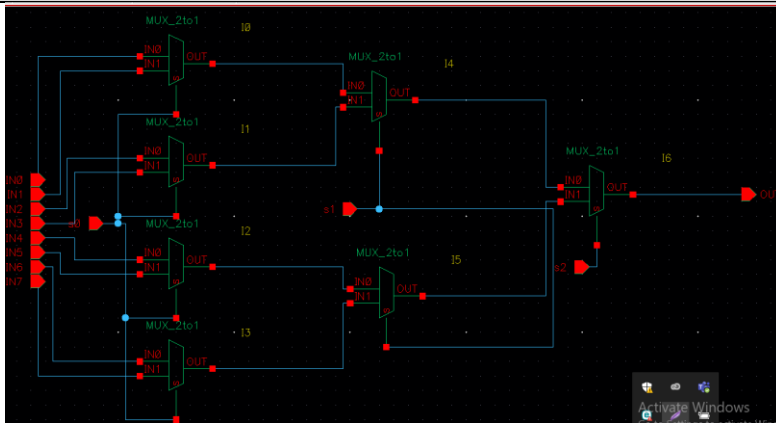


Subtraction waveforms (a-b if a>b and b-a if a<b)

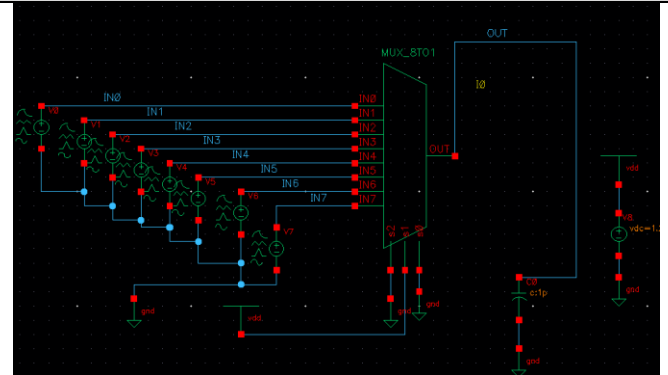


ALU

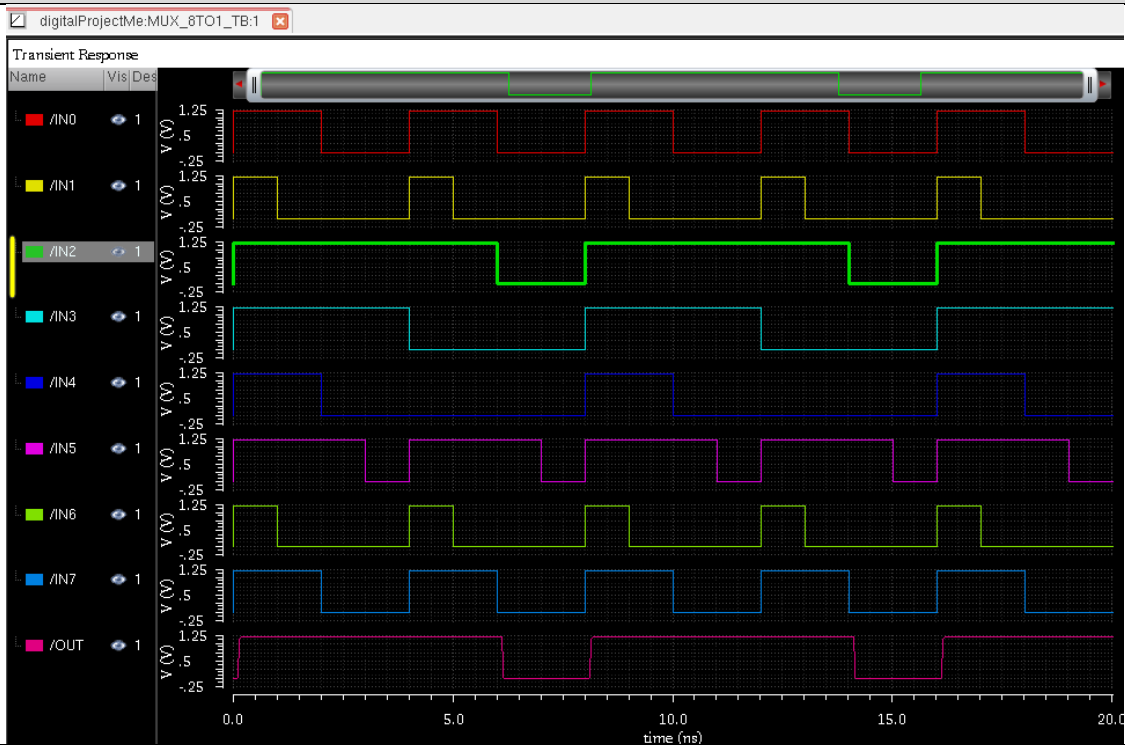
MUX 8:1 Schematic



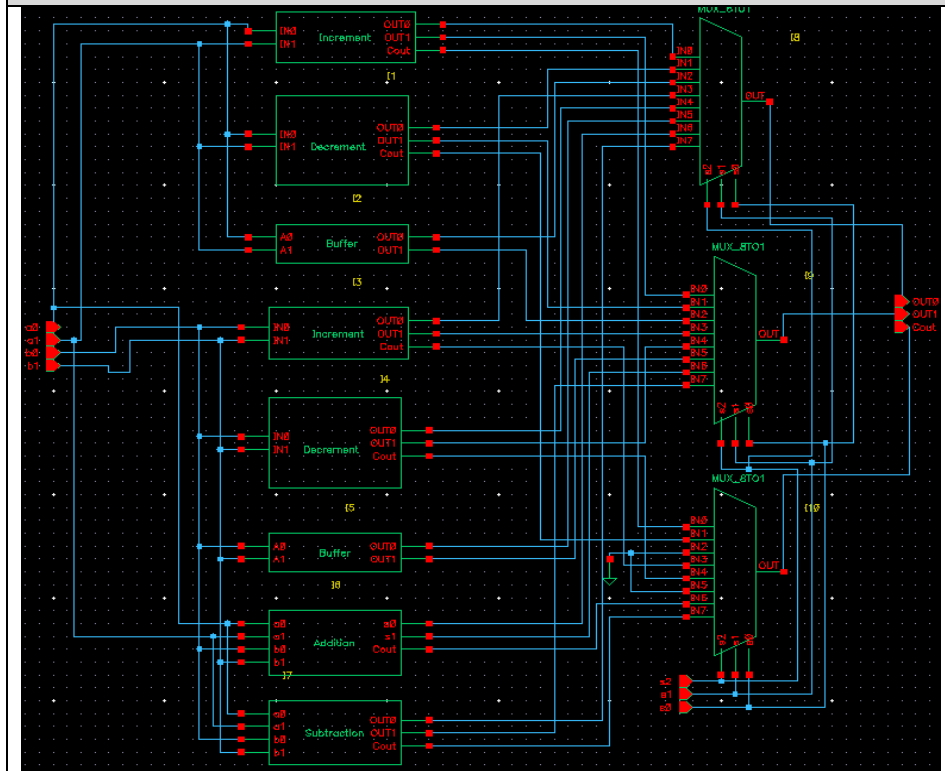
MUX 8:1 Testbench



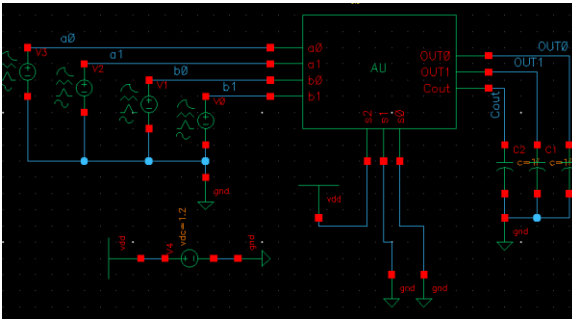
MUX 8:1 Testbench



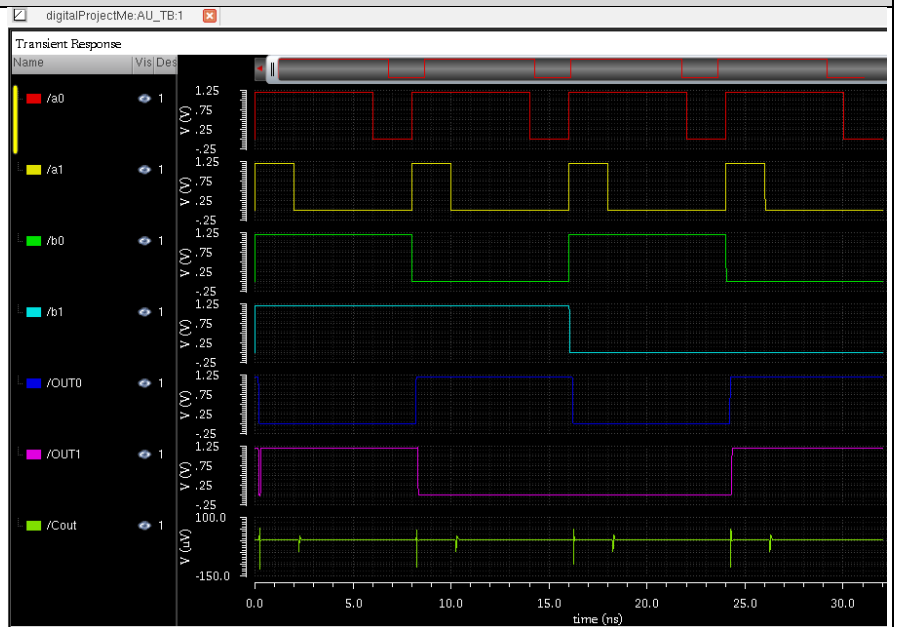
Arithmetic Unit Schematic



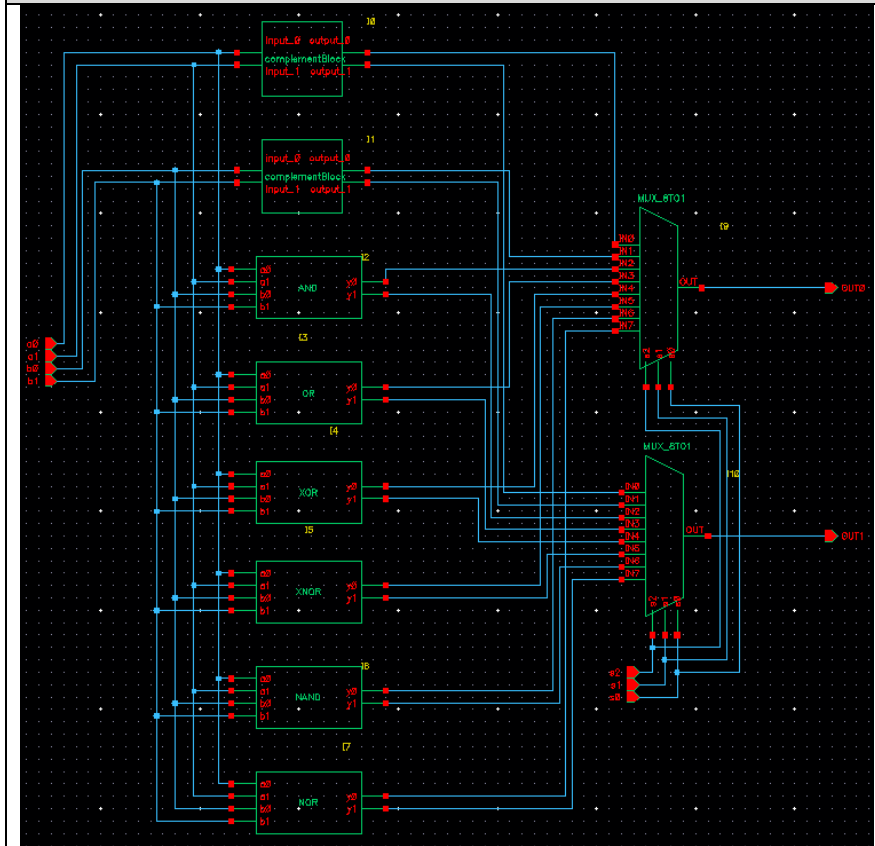
Testbench for Arithmetic Unit (S2 S1 S0 = 1 0 0) → Decrement b



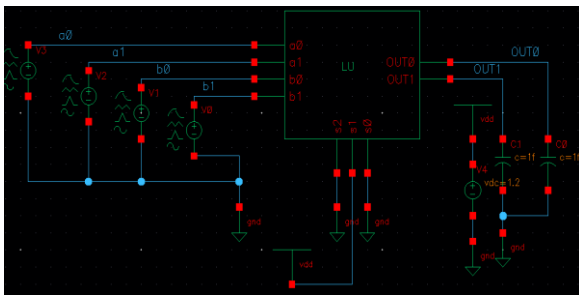
Waveforms of Decrement b Operation



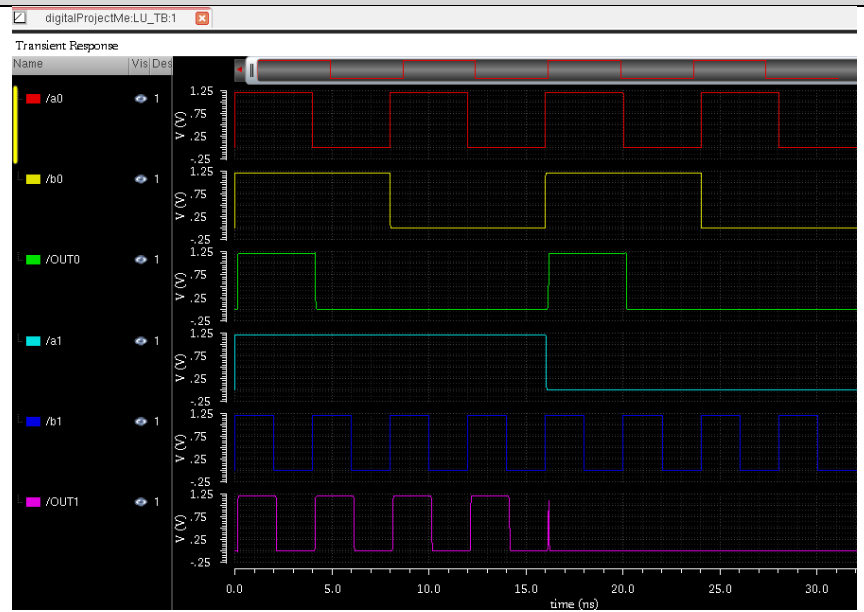
Logical Unit Schematic



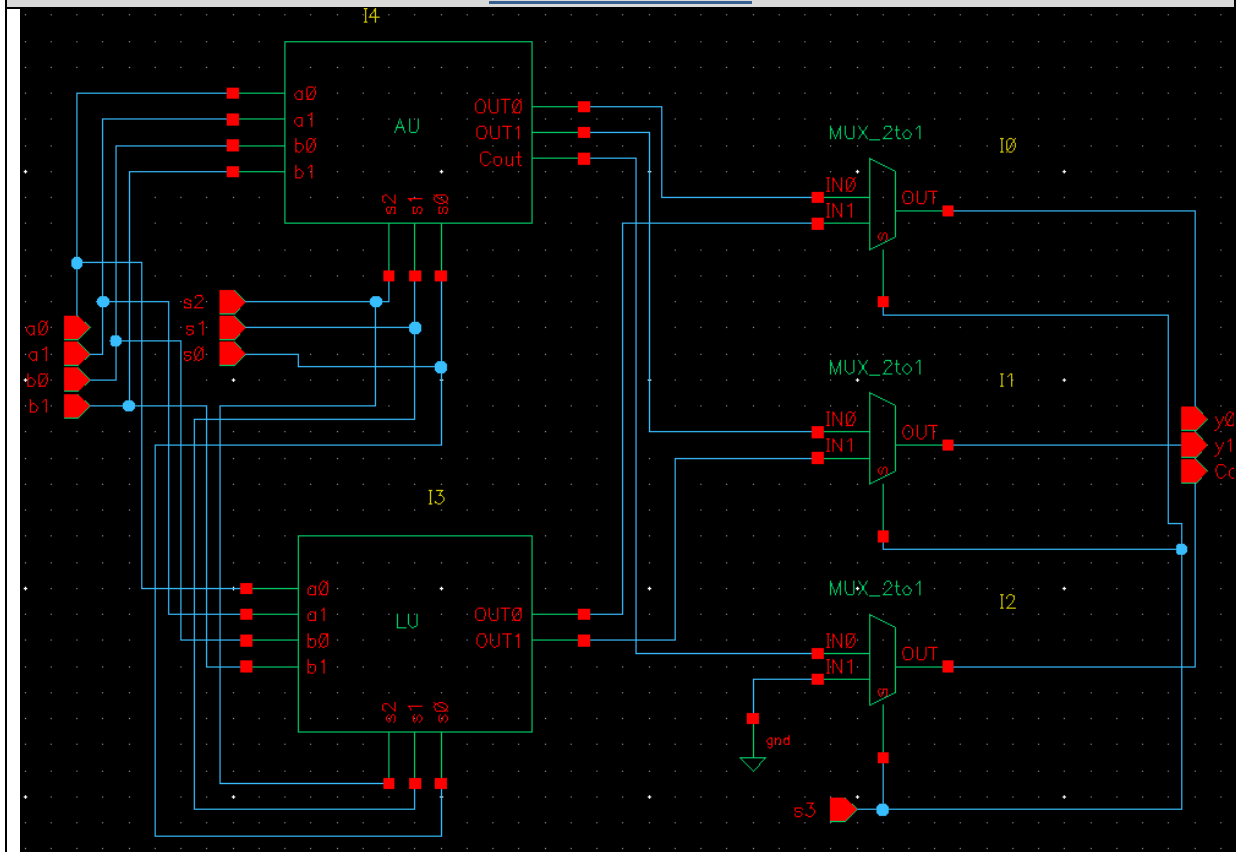
Testbench for Logical Unit (s2 s1 s0 = 0 1 0 → AND)



Waveforms of AND Operation



ALU Schematic



ALU Testbench Schematic (s3 s2 s1 s0 = 0 1 1 0 → a+b)

