```
`timescale 1 ns / 1 ns

module pol78cse4
          (
           clk,
           reset,
           clk_enable,
           ce_out,
           Out1
          );


  input   clk;
  input   reset;
  input   clk_enable;
  output  ce_out;
  output  signed [15:0] Out1;  // sfix16_En14


  wire enb_1_7_0;
  wire enb_1_8_0;
  wire enb_1_56_1;
  wire enb_1_56_0;
  wire enb_7_56_1;
  wire enb_1_8_1;
  reg signed [15:0] Sine_Wave1_out1;  // sfix16_En14
  wire signed [15:0] Downsample_out1;  // sfix16_En14
  wire signed [15:0] Subsystem5_out1;  // sfix16_En14
  reg signed [15:0] Delay_out1;  // sfix16_En14
  wire signed [15:0] Downsample1_out1;  // sfix16_En14
  wire signed [15:0] Subsystem9_out1;  // sfix16_En14
  wire signed [15:0] Add1_out1;  // sfix16_En14
  reg signed [15:0] Delay1_out1;  // sfix16_En14
  wire signed [15:0] Downsample2_out1;  // sfix16_En14
  wire signed [15:0] Subsystem2_out1;  // sfix16_En14
  wire signed [15:0] Add2_out1;  // sfix16_En14
  reg signed [15:0] Delay2_out1;  // sfix16_En14
  wire signed [15:0] Downsample3_out1;  // sfix16_En14
  wire signed [15:0] Subsystem1_out1;  // sfix16_En14
  wire signed [15:0] Add3_out1;  // sfix16_En14
  wire signed [15:0] Upsample6_out1;  // sfix16_En14
  reg signed [15:0] Delay10_out1;  // sfix16_En14
  wire signed [15:0] Subsystem6_out1;  // sfix16_En14
  wire signed [15:0] Subsystem8_out1;  // sfix16_En14
  wire signed [15:0] Add19_out1;  // sfix16_En14
  wire signed [15:0] Subsystem10_out1;  // sfix16_En14
  wire signed [15:0] Add4_out1;  // sfix16_En14
  reg signed [15:0] Delay3_out1;  // sfix16_En14
  wire signed [15:0] Downsample4_out1;  // sfix16_En14
  wire signed [15:0] Subsystem12_out1;  // sfix16_En14
  wire signed [15:0] Add7_out1;  // sfix16_En14
  reg signed [15:0] Delay4_out1;  // sfix16_En14
  wire signed [15:0] Downsample5_out1;  // sfix16_En14
  wire signed [15:0] Subsystem7_out1;  // sfix16_En14
```

```
wire signed [15:0] Add11_out1;  // sfix16_En14
wire signed [15:0] Upsample1_out1;  // sfix16_En14
wire signed [15:0] Add28_out1;  // sfix16_En14
reg signed [15:0] Delay11_out1;  // sfix16_En14
wire signed [15:0] Subsystem15_out1;  // sfix16_En14
wire signed [15:0] Subsystem18_out1;  // sfix16_En14
wire signed [15:0] Add5_out1;  // sfix16_En14
wire signed [15:0] Subsystem21_out1;  // sfix16_En14
wire signed [15:0] Add8_out1;  // sfix16_En14
wire signed [15:0] Subsystem23_out1;  // sfix16_En14
wire signed [15:0] Add12_out1;  // sfix16_En14
reg signed [15:0] Delay5_out1;  // sfix16_En14
wire signed [15:0] Downsample6_out1;  // sfix16_En14
wire signed [15:0] Subsystem25_out1;  // sfix16_En14
wire signed [15:0] Add16_out1;  // sfix16_En14
wire signed [15:0] Upsample2_out1;  // sfix16_En14
wire signed [15:0] Add29_out1;  // sfix16_En14
reg signed [15:0] Delay12_out1;  // sfix16_En14
wire signed [15:0] Subsystem27_out1;  // sfix16_En14
wire signed [15:0] Subsystem29_out1;  // sfix16_En14
wire signed [15:0] Add9_out1;  // sfix16_En14
wire signed [15:0] Subsystem31_out1;  // sfix16_En14
wire signed [15:0] Add13_out1;  // sfix16_En14
wire signed [15:0] Subsystem33_out1;  // sfix16_En14
wire signed [15:0] Add17_out1;  // sfix16_En14
reg signed [15:0] Delay6_out1;  // sfix16_En14
wire signed [15:0] Downsample9_out1;  // sfix16_En14
wire signed [15:0] Subsystem_out1;  // sfix16_En14
wire signed [15:0] Add6_out1;  // sfix16_En14
wire signed [15:0] Upsample3_out1;  // sfix16_En14
wire signed [15:0] Add30_out1;  // sfix16_En14
reg signed [15:0] Delay13_out1;  // sfix16_En14
wire signed [15:0] Subsystem35_out1;  // sfix16_En14
wire signed [15:0] Subsystem34_out1;  // sfix16_En14
wire signed [15:0] Add10_out1;  // sfix16_En14
wire signed [15:0] Subsystem32_out1;  // sfix16_En14
wire signed [15:0] Add14_out1;  // sfix16_En14
wire signed [15:0] Subsystem30_out1;  // sfix16_En14
wire signed [15:0] Add15_out1;  // sfix16_En14
reg signed [15:0] Delay7_out1;  // sfix16_En14
wire signed [15:0] Downsample8_out1;  // sfix16_En14
wire signed [15:0] Subsystem28_out1;  // sfix16_En14
wire signed [15:0] Add22_out1;  // sfix16_En14
wire signed [15:0] Upsample4_out1;  // sfix16_En14
wire signed [15:0] Add31_out1;  // sfix16_En14
reg signed [15:0] Delay14_out1;  // sfix16_En14
wire signed [15:0] Subsystem26_out1;  // sfix16_En14
wire signed [15:0] Subsystem24_out1;  // sfix16_En14
wire signed [15:0] Add18_out1;  // sfix16_En14
wire signed [15:0] Subsystem22_out1;  // sfix16_En14
wire signed [15:0] Add20_out1;  // sfix16_En14
wire signed [15:0] Subsystem19_out1;  // sfix16_En14
wire signed [15:0] Add23_out1;  // sfix16_En14
reg signed [15:0] Delay9_out1;  // sfix16_En14
```

```
wire signed [15:0] Downsample7_out1;  // sfix16_En14
wire signed [15:0] Subsystem16_out1;  // sfix16_En14
wire signed [15:0] Add25_out1;  // sfix16_En14
wire signed [15:0] Upsample5_out1;  // sfix16_En14
wire signed [15:0] Add32_out1;  // sfix16_En14
reg signed [15:0] Delay15_out1;  // sfix16_En14
wire signed [15:0] Subsystem14_out1;  // sfix16_En14
wire signed [15:0] Subsystem13_out1;  // sfix16_En14
wire signed [15:0] Add21_out1;  // sfix16_En14
wire signed [15:0] Subsystem11_out1;  // sfix16_En14
wire signed [15:0] Add24_out1;  // sfix16_En14
wire signed [15:0] Subsystem4_out1;  // sfix16_En14
wire signed [15:0] Add26_out1;  // sfix16_En14
reg signed [15:0] Delay8_out1;  // sfix16_En14
wire signed [15:0] Downsample10_out1;  // sfix16_En14
wire signed [15:0] Subsystem3_out1;  // sfix16_En14
wire signed [15:0] Add27_out1;  // sfix16_En14
wire signed [15:0] Upsample7_out1;  // sfix16_En14
wire signed [15:0] Add33_out1;  // sfix16_En14
reg [6:0] address_cnt;  // ufix7
wire signed [15:0] tmpout;  // sfix16_En14
reg signed [15:0] regout;  // sfix16_En14
wire signed [15:0] tmpout_1;  // sfix16_En14
reg signed [15:0] regout_1;  // sfix16_En14
wire signed [31:0] Add1_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast;  // sfix32_En14
wire signed [31:0] add_cast_1;  // sfix32_En14
wire signed [32:0] add_temp;  // sfix33_En14
wire signed [15:0] tmpout_2;  // sfix16_En14
reg signed [15:0] regout_2;  // sfix16_En14
wire signed [31:0] Add2_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_2;  // sfix32_En14
wire signed [31:0] add_cast_3;  // sfix32_En14
wire signed [32:0] add_temp_1;  // sfix33_En14
wire signed [15:0] tmpout_3;  // sfix16_En14
reg signed [15:0] regout_3;  // sfix16_En14
wire signed [31:0] Add3_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_4;  // sfix32_En14
wire signed [31:0] add_cast_5;  // sfix32_En14
wire signed [32:0] add_temp_2;  // sfix33_En14
// Up sample by 7 Constant Declaration
wire signed [15:0] zero;  // sfix16_En14
// Up sample by 7 Signal Declaration
wire signed [15:0] muxout;  // sfix16_En14
reg signed [15:0] regout_4;  // sfix16_En14
wire signed [31:0] Add19_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_6;  // sfix32_En14
wire signed [31:0] add_cast_7;  // sfix32_En14
wire signed [32:0] add_temp_3;  // sfix33_En14
wire signed [31:0] Add4_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_8;  // sfix32_En14
wire signed [31:0] add_cast_9;  // sfix32_En14
wire signed [32:0] add_temp_4;  // sfix33_En14
wire signed [15:0] tmpout_4;  // sfix16_En14
```

```
reg signed [15:0] regout_5;  // sfix16_En14
wire signed [31:0] Add7_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_10;  // sfix32_En14
wire signed [31:0] add_cast_11;  // sfix32_En14
wire signed [32:0] add_temp_5;  // sfix33_En14
wire signed [15:0] tmpout_5;  // sfix16_En14
reg signed [15:0] regout_6;  // sfix16_En14
wire signed [31:0] Add11_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_12;  // sfix32_En14
wire signed [31:0] add_cast_13;  // sfix32_En14
wire signed [32:0] add_temp_6;  // sfix33_En14
// Up sample by 7 Constant Declaration
wire signed [15:0] zero_1;  // sfix16_En14
// Up sample by 7 Signal Declaration
wire signed [15:0] muxout_1;  // sfix16_En14
reg signed [15:0] regout_7;  // sfix16_En14
wire signed [31:0] Add28_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_14;  // sfix32_En14
wire signed [31:0] add_cast_15;  // sfix32_En14
wire signed [32:0] add_temp_7;  // sfix33_En14
wire signed [31:0] Add5_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_16;  // sfix32_En14
wire signed [31:0] add_cast_17;  // sfix32_En14
wire signed [32:0] add_temp_8;  // sfix33_En14
wire signed [31:0] Add8_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_18;  // sfix32_En14
wire signed [31:0] add_cast_19;  // sfix32_En14
wire signed [32:0] add_temp_9;  // sfix33_En14
wire signed [31:0] Add12_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_20;  // sfix32_En14
wire signed [31:0] add_cast_21;  // sfix32_En14
wire signed [32:0] add_temp_10;  // sfix33_En14
wire signed [15:0] tmpout_6;  // sfix16_En14
reg signed [15:0] regout_8;  // sfix16_En14
wire signed [31:0] Add16_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_22;  // sfix32_En14
wire signed [31:0] add_cast_23;  // sfix32_En14
wire signed [32:0] add_temp_11;  // sfix33_En14
// Up sample by 7 Constant Declaration
wire signed [15:0] zero_2;  // sfix16_En14
// Up sample by 7 Signal Declaration
wire signed [15:0] muxout_2;  // sfix16_En14
reg signed [15:0] regout_9;  // sfix16_En14
wire signed [31:0] Add29_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_24;  // sfix32_En14
wire signed [31:0] add_cast_25;  // sfix32_En14
wire signed [32:0] add_temp_12;  // sfix33_En14
wire signed [31:0] Add9_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_26;  // sfix32_En14
wire signed [31:0] add_cast_27;  // sfix32_En14
wire signed [32:0] add_temp_13;  // sfix33_En14
wire signed [31:0] Add13_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_28;  // sfix32_En14
wire signed [31:0] add_cast_29;  // sfix32_En14
```

```
wire signed [32:0] add_temp_14;  // sfix33_En14
wire signed [31:0] Add17_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_30;  // sfix32_En14
wire signed [31:0] add_cast_31;  // sfix32_En14
wire signed [32:0] add_temp_15;  // sfix33_En14
wire signed [15:0] tmpout_7;  // sfix16_En14
reg signed [15:0] regout_10;  // sfix16_En14
wire signed [31:0] Add6_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_32;  // sfix32_En14
wire signed [31:0] add_cast_33;  // sfix32_En14
wire signed [32:0] add_temp_16;  // sfix33_En14
// Up sample by 7 Constant Declaration
wire signed [15:0] zero_3;  // sfix16_En14
// Up sample by 7 Signal Declaration
wire signed [15:0] muxout_3;  // sfix16_En14
reg signed [15:0] regout_11;  // sfix16_En14
wire signed [31:0] Add30_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_34;  // sfix32_En14
wire signed [31:0] add_cast_35;  // sfix32_En14
wire signed [32:0] add_temp_17;  // sfix33_En14
wire signed [31:0] Add10_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_36;  // sfix32_En14
wire signed [31:0] add_cast_37;  // sfix32_En14
wire signed [32:0] add_temp_18;  // sfix33_En14
wire signed [31:0] Add14_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_38;  // sfix32_En14
wire signed [31:0] add_cast_39;  // sfix32_En14
wire signed [32:0] add_temp_19;  // sfix33_En14
wire signed [31:0] Add15_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_40;  // sfix32_En14
wire signed [31:0] add_cast_41;  // sfix32_En14
wire signed [32:0] add_temp_20;  // sfix33_En14
wire signed [15:0] tmpout_8;  // sfix16_En14
reg signed [15:0] regout_12;  // sfix16_En14
wire signed [31:0] Add22_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_42;  // sfix32_En14
wire signed [31:0] add_cast_43;  // sfix32_En14
wire signed [32:0] add_temp_21;  // sfix33_En14
// Up sample by 7 Constant Declaration
wire signed [15:0] zero_4;  // sfix16_En14
// Up sample by 7 Signal Declaration
wire signed [15:0] muxout_4;  // sfix16_En14
reg signed [15:0] regout_13;  // sfix16_En14
wire signed [31:0] Add31_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_44;  // sfix32_En14
wire signed [31:0] add_cast_45;  // sfix32_En14
wire signed [32:0] add_temp_22;  // sfix33_En14
wire signed [31:0] Add18_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_46;  // sfix32_En14
wire signed [31:0] add_cast_47;  // sfix32_En14
wire signed [32:0] add_temp_23;  // sfix33_En14
wire signed [31:0] Add20_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_48;  // sfix32_En14
wire signed [31:0] add_cast_49;  // sfix32_En14
```

```
wire signed [32:0] add_temp_24;  // sfix33_En14
wire signed [31:0] Add23_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_50;  // sfix32_En14
wire signed [31:0] add_cast_51;  // sfix32_En14
wire signed [32:0] add_temp_25;  // sfix33_En14
wire signed [15:0] tmpout_9;  // sfix16_En14
reg signed [15:0] regout_14;  // sfix16_En14
wire signed [31:0] Add25_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_52;  // sfix32_En14
wire signed [31:0] add_cast_53;  // sfix32_En14
wire signed [32:0] add_temp_26;  // sfix33_En14
// Up sample by 7 Constant Declaration
wire signed [15:0] zero_5;  // sfix16_En14
// Up sample by 7 Signal Declaration
wire signed [15:0] muxout_5;  // sfix16_En14
reg signed [15:0] regout_15;  // sfix16_En14
wire signed [31:0] Add32_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_54;  // sfix32_En14
wire signed [31:0] add_cast_55;  // sfix32_En14
wire signed [32:0] add_temp_27;  // sfix33_En14
wire signed [31:0] Add21_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_56;  // sfix32_En14
wire signed [31:0] add_cast_57;  // sfix32_En14
wire signed [32:0] add_temp_28;  // sfix33_En14
wire signed [31:0] Add24_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_58;  // sfix32_En14
wire signed [31:0] add_cast_59;  // sfix32_En14
wire signed [32:0] add_temp_29;  // sfix33_En14
wire signed [31:0] Add26_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_60;  // sfix32_En14
wire signed [31:0] add_cast_61;  // sfix32_En14
wire signed [32:0] add_temp_30;  // sfix33_En14
wire signed [15:0] tmpout_10;  // sfix16_En14
reg signed [15:0] regout_16;  // sfix16_En14
wire signed [31:0] Add27_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_62;  // sfix32_En14
wire signed [31:0] add_cast_63;  // sfix32_En14
wire signed [32:0] add_temp_31;  // sfix33_En14
// Up sample by 7 Constant Declaration
wire signed [15:0] zero_6;  // sfix16_En14
// Up sample by 7 Signal Declaration
wire signed [15:0] muxout_6;  // sfix16_En14
reg signed [15:0] regout_17;  // sfix16_En14
wire signed [31:0] Add33_out1_tmp;  // sfix32_En14
wire signed [31:0] add_cast_64;  // sfix32_En14
wire signed [31:0] add_cast_65;  // sfix32_En14
wire signed [32:0] add_temp_32;  // sfix33_En14

Timing_Controller   u_Timing_Controller   (.clk(clk),
                                           .reset(reset),
                                           .clk_enable(clk_enable),
                                           .enb_1_7_0_1(enb_1_7_0),
                                           .enb_1_8_0_1(enb_1_8_0),
                                           .enb_1_8_1_1(enb_1_8_1),
```

```
                                                    .enb_1_56_0_1(enb_1_56_0),
                                                    .enb_1_56_1_1(enb_1_56_1),
                                                    .enb_7_56_1_1(enb_7_56_1)
                                                    );

  assign ce_out = enb_1_8_1;
// ADDRESS COUNTER
  always @ (posedge clk or posedge reset)
    begin: Sine_Wave1_addrcnt_temp_process6
      if (reset == 1'b1) begin
        address_cnt <= 7'b0000000;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          if (address_cnt == 7'b1100011) begin
            address_cnt <= 7'b0000000;
          end
          else begin
            address_cnt <= address_cnt + 1;
          end
        end
      end
    end // Sine_Wave1_addrcnt_temp_process6

// FULL WAVE LOOKUP TABLE
  always @(address_cnt)
  begin
    case(address_cnt)
      7'b0000000 : Sine_Wave1_out1 = 16'b0000000000000000;
      7'b0000001 : Sine_Wave1_out1 = 16'b0000010000000101;
      7'b0000010 : Sine_Wave1_out1 = 16'b0000100000000101;
      7'b0000011 : Sine_Wave1_out1 = 16'b0000101111111110;
      7'b0000100 : Sine_Wave1_out1 = 16'b0000111111101011;
      7'b0000101 : Sine_Wave1_out1 = 16'b0001001111000111;
      7'b0000110 : Sine_Wave1_out1 = 16'b0001011110001111;
      7'b0000111 : Sine_Wave1_out1 = 16'b0001101101000000;
      7'b0001000 : Sine_Wave1_out1 = 16'b0001111011010101;
      7'b0001001 : Sine_Wave1_out1 = 16'b0010001001001011;
      7'b0001010 : Sine_Wave1_out1 = 16'b0010010110011110;
      7'b0001011 : Sine_Wave1_out1 = 16'b0010100011001100;
      7'b0001100 : Sine_Wave1_out1 = 16'b0010101111010000;
      7'b0001101 : Sine_Wave1_out1 = 16'b0010111010100111;
      7'b0001110 : Sine_Wave1_out1 = 16'b0011000101010000;
      7'b0001111 : Sine_Wave1_out1 = 16'b0011001111000111;
      7'b0010000 : Sine_Wave1_out1 = 16'b0011011000001001;
      7'b0010001 : Sine_Wave1_out1 = 16'b0011100000010101;
      7'b0010010 : Sine_Wave1_out1 = 16'b0011100111101001;
      7'b0010011 : Sine_Wave1_out1 = 16'b0011101110000001;
      7'b0010100 : Sine_Wave1_out1 = 16'b0011110011011110;
      7'b0010101 : Sine_Wave1_out1 = 16'b0011110111111101;
      7'b0010110 : Sine_Wave1_out1 = 16'b0011111011011110;
      7'b0010111 : Sine_Wave1_out1 = 16'b0011111101111111;
      7'b0011000 : Sine_Wave1_out1 = 16'b0011111111100000;
      7'b0011001 : Sine_Wave1_out1 = 16'b0100000000000000;
```

```
7'b0011010 : Sine_Wave1_out1 = 16'b0011111111100000;
7'b0011011 : Sine_Wave1_out1 = 16'b0011111101111111;
7'b0011100 : Sine_Wave1_out1 = 16'b0011111011011110;
7'b0011101 : Sine_Wave1_out1 = 16'b0011110111111101;
7'b0011110 : Sine_Wave1_out1 = 16'b0011110011011110;
7'b0011111 : Sine_Wave1_out1 = 16'b0011101110000001;
7'b0100000 : Sine_Wave1_out1 = 16'b0011100111101001;
7'b0100001 : Sine_Wave1_out1 = 16'b0011100000010101;
7'b0100010 : Sine_Wave1_out1 = 16'b0011011000001001;
7'b0100011 : Sine_Wave1_out1 = 16'b0011001111000111;
7'b0100100 : Sine_Wave1_out1 = 16'b0011000101010000;
7'b0100101 : Sine_Wave1_out1 = 16'b0010111010100111;
7'b0100110 : Sine_Wave1_out1 = 16'b0010101111010000;
7'b0100111 : Sine_Wave1_out1 = 16'b0010100011001100;
7'b0101000 : Sine_Wave1_out1 = 16'b0010010110011110;
7'b0101001 : Sine_Wave1_out1 = 16'b0010001001001011;
7'b0101010 : Sine_Wave1_out1 = 16'b0001111011010101;
7'b0101011 : Sine_Wave1_out1 = 16'b0001101101000000;
7'b0101100 : Sine_Wave1_out1 = 16'b0001011110001111;
7'b0101101 : Sine_Wave1_out1 = 16'b0001001111000111;
7'b0101110 : Sine_Wave1_out1 = 16'b0000111111101011;
7'b0101111 : Sine_Wave1_out1 = 16'b0000101111111110;
7'b0110000 : Sine_Wave1_out1 = 16'b0000100000000101;
7'b0110001 : Sine_Wave1_out1 = 16'b0000010000000101;
7'b0110010 : Sine_Wave1_out1 = 16'b0000000000000000;
7'b0110011 : Sine_Wave1_out1 = 16'b1111101111111011;
7'b0110100 : Sine_Wave1_out1 = 16'b1111011111111011;
7'b0110101 : Sine_Wave1_out1 = 16'b1111010000000010;
7'b0110110 : Sine_Wave1_out1 = 16'b1111000000010101;
7'b0110111 : Sine_Wave1_out1 = 16'b1110110000111001;
7'b0111000 : Sine_Wave1_out1 = 16'b1110100001110001;
7'b0111001 : Sine_Wave1_out1 = 16'b1110010011000000;
7'b0111010 : Sine_Wave1_out1 = 16'b1110000100101011;
7'b0111011 : Sine_Wave1_out1 = 16'b1101110110110101;
7'b0111100 : Sine_Wave1_out1 = 16'b1101101001100010;
7'b0111101 : Sine_Wave1_out1 = 16'b1101011100110100;
7'b0111110 : Sine_Wave1_out1 = 16'b1101010000110000;
7'b0111111 : Sine_Wave1_out1 = 16'b1101000101011001;
7'b1000000 : Sine_Wave1_out1 = 16'b1100111010110000;
7'b1000001 : Sine_Wave1_out1 = 16'b1100110000111001;
7'b1000010 : Sine_Wave1_out1 = 16'b1100100111110111;
7'b1000011 : Sine_Wave1_out1 = 16'b1100011111101011;
7'b1000100 : Sine_Wave1_out1 = 16'b1100011000010111;
7'b1000101 : Sine_Wave1_out1 = 16'b1100010001111111;
7'b1000110 : Sine_Wave1_out1 = 16'b1100001100100010;
7'b1000111 : Sine_Wave1_out1 = 16'b1100001000000011;
7'b1001000 : Sine_Wave1_out1 = 16'b1100000100100010;
7'b1001001 : Sine_Wave1_out1 = 16'b1100000010000001;
7'b1001010 : Sine_Wave1_out1 = 16'b1100000000100000;
7'b1001011 : Sine_Wave1_out1 = 16'b1100000000000000;
7'b1001100 : Sine_Wave1_out1 = 16'b1100000000100000;
7'b1001101 : Sine_Wave1_out1 = 16'b1100000010000001;
7'b1001110 : Sine_Wave1_out1 = 16'b1100000100100010;
7'b1001111 : Sine_Wave1_out1 = 16'b1100001000000011;
```

```
      7'b1010000 : Sine_Wave1_out1 = 16'b1100001100100010;
      7'b1010001 : Sine_Wave1_out1 = 16'b1100010001111111;
      7'b1010010 : Sine_Wave1_out1 = 16'b1100011000010111;
      7'b1010011 : Sine_Wave1_out1 = 16'b1100011111101011;
      7'b1010100 : Sine_Wave1_out1 = 16'b1100100111110111;
      7'b1010101 : Sine_Wave1_out1 = 16'b1100110000111001;
      7'b1010110 : Sine_Wave1_out1 = 16'b1100111010110000;
      7'b1010111 : Sine_Wave1_out1 = 16'b1101000101011001;
      7'b1011000 : Sine_Wave1_out1 = 16'b1101010000110000;
      7'b1011001 : Sine_Wave1_out1 = 16'b1101011100110100;
      7'b1011010 : Sine_Wave1_out1 = 16'b1101101001100010;
      7'b1011011 : Sine_Wave1_out1 = 16'b1101110110110101;
      7'b1011100 : Sine_Wave1_out1 = 16'b1110000100101011;
      7'b1011101 : Sine_Wave1_out1 = 16'b1110010011000000;
      7'b1011110 : Sine_Wave1_out1 = 16'b1110100001110001;
      7'b1011111 : Sine_Wave1_out1 = 16'b1110110000111001;
      7'b1100000 : Sine_Wave1_out1 = 16'b1111000000010101;
      7'b1100001 : Sine_Wave1_out1 = 16'b1111010000000010;
      7'b1100010 : Sine_Wave1_out1 = 16'b1111011111111011;
      7'b1100011 : Sine_Wave1_out1 = 16'b1111101111111011;
      default : Sine_Wave1_out1 = 16'b1111101111111011;
    endcase
  end

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process7
      if (reset == 1'b1) begin
        regout <= 0;
      end
      else begin
        if (enb_1_56_1 == 1'b1) begin
          regout <= Sine_Wave1_out1;
        end
      end
    end // DataHoldRegister_temp_process7

  assign tmpout = (enb_1_56_1 == 1'b1) ? Sine_Wave1_out1 :
           regout;
  assign Downsample_out1 = tmpout;

  Subsystem5   u_Subsystem5   (.In1(Downsample_out1),  // sfix16_En14
                               .Out1(Subsystem5_out1)  // sfix16_En14
                               );


  always @ (posedge clk or posedge reset)
    begin: Delay_process
      if (reset == 1'b1) begin
        Delay_out1 <= 0;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          Delay_out1 <= Sine_Wave1_out1;
```

```
        end
      end
    end // Delay_process

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process8
      if (reset == 1'b1) begin
        regout_1 <= 0;
      end
      else begin
        if (enb_1_56_1 == 1'b1) begin
          regout_1 <= Delay_out1;
        end
      end
    end // DataHoldRegister_temp_process8

  assign tmpout_1 = (enb_1_56_1 == 1'b1) ? Delay_out1 :
              regout_1;
  assign Downsample1_out1 = tmpout_1;

  Subsystem9   u_Subsystem9   (.In1(Downsample1_out1),  // sfix16_En14
                               .Out1(Subsystem9_out1)  // sfix16_En14
                               );

  assign add_cast = $signed({{16{Subsystem5_out1[15]}},
Subsystem5_out1});
  assign add_cast_1 = $signed({{16{Subsystem9_out1[15]}},
Subsystem9_out1});
  assign add_temp = add_cast + add_cast_1;
  assign Add1_out1_tmp = add_temp[31:0];

  assign Add1_out1 = Add1_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay1_process
      if (reset == 1'b1) begin
        Delay1_out1 <= 0;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          Delay1_out1 <= Delay_out1;
        end
      end
    end // Delay1_process

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process9
      if (reset == 1'b1) begin
        regout_2 <= 0;
      end
      else begin
```

```
        if (enb_1_56_1 == 1'b1) begin
          regout_2 <= Delay1_out1;
        end
      end
    end // DataHoldRegister_temp_process9

  assign tmpout_2 = (enb_1_56_1 == 1'b1) ? Delay1_out1 :
              regout_2;
  assign Downsample2_out1 = tmpout_2;

  Subsystem2   u_Subsystem2   (.In1(Downsample2_out1),  // sfix16_En14
                               .Out1(Subsystem2_out1)  // sfix16_En14
                               );

  assign add_cast_2 = $signed({{16{Add1_out1[15]}}, Add1_out1});
  assign add_cast_3 = $signed({{16{Subsystem2_out1[15]}},
Subsystem2_out1});
  assign add_temp_1 = add_cast_2 + add_cast_3;
  assign Add2_out1_tmp = add_temp_1[31:0];

  assign Add2_out1 = Add2_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay2_process
      if (reset == 1'b1) begin
        Delay2_out1 <= 0;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          Delay2_out1 <= Delay1_out1;
        end
      end
    end // Delay2_process

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process10
      if (reset == 1'b1) begin
        regout_3 <= 0;
      end
      else begin
        if (enb_1_56_1 == 1'b1) begin
          regout_3 <= Delay2_out1;
        end
      end
    end // DataHoldRegister_temp_process10

  assign tmpout_3 = (enb_1_56_1 == 1'b1) ? Delay2_out1 :
              regout_3;
  assign Downsample3_out1 = tmpout_3;

  Subsystem1   u_Subsystem1   (.In1(Downsample3_out1),  // sfix16_En14
                               .Out1(Subsystem1_out1)  // sfix16_En14
```

```
                                );

  assign add_cast_4 = $signed({{16{Add2_out1[15]}}, Add2_out1});
  assign add_cast_5 = $signed({{16{Subsystem1_out1[15]}},
Subsystem1_out1});
  assign add_temp_2 = add_cast_4 + add_cast_5;
  assign Add3_out1_tmp = add_temp_2[31:0];

  assign Add3_out1 = Add3_out1_tmp[15:0];

// %%%% Up sample by 7, Sample offset 0 %%%%
  assign zero = 16'b0000000000000000;
  assign muxout = (enb_1_56_1 == 1'b1) ? Add3_out1 :
            zero;

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process11
      if (reset == 1'b1) begin
        regout_4 <= 0;
      end
      else begin
        if (enb_7_56_1 == 1'b1) begin
          regout_4 <= muxout;
        end
      end
    end // DataHoldRegister_temp_process11

  assign Upsample6_out1 = (enb_7_56_1 == 1'b1) ? muxout :
                   regout_4;

  always @ (posedge clk or posedge reset)
    begin: Delay10_process
      if (reset == 1'b1) begin
        Delay10_out1 <= 0;
      end
      else begin
        if (enb_1_8_0 == 1'b1) begin
          Delay10_out1 <= Upsample6_out1;
        end
      end
    end // Delay10_process

  Subsystem6   u_Subsystem6   (.In1(Downsample1_out1),  // sfix16_En14
                               .Out1(Subsystem6_out1)  // sfix16_En14
                               );

  Subsystem8   u_Subsystem8   (.In1(Downsample2_out1),  // sfix16_En14
                               .Out1(Subsystem8_out1)  // sfix16_En14
                               );

  assign add_cast_6 = $signed({{16{Subsystem6_out1[15]}},
Subsystem6_out1});
```

```
  assign add_cast_7 = $signed({{16{Subsystem8_out1[15]}},
Subsystem8_out1});
  assign add_temp_3 = add_cast_6 + add_cast_7;
  assign Add19_out1_tmp = add_temp_3[31:0];

  assign Add19_out1 = Add19_out1_tmp[15:0];

  Subsystem10   u_Subsystem10   (.In1(Downsample3_out1),  // sfix16_En14
                                 .Out1(Subsystem10_out1)  // sfix16_En14
                                 );

  assign add_cast_8 = $signed({{16{Add19_out1[15]}}, Add19_out1});
  assign add_cast_9 = $signed({{16{Subsystem10_out1[15]}},
Subsystem10_out1});
  assign add_temp_4 = add_cast_8 + add_cast_9;
  assign Add4_out1_tmp = add_temp_4[31:0];

  assign Add4_out1 = Add4_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay3_process
      if (reset == 1'b1) begin
        Delay3_out1 <= 0;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          Delay3_out1 <= Delay2_out1;
        end
      end
    end // Delay3_process

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process12
      if (reset == 1'b1) begin
        regout_5 <= 0;
      end
      else begin
        if (enb_1_56_1 == 1'b1) begin
          regout_5 <= Delay3_out1;
        end
      end
    end // DataHoldRegister_temp_process12

  assign tmpout_4 = (enb_1_56_1 == 1'b1) ? Delay3_out1 :
              regout_5;
  assign Downsample4_out1 = tmpout_4;

  Subsystem12   u_Subsystem12   (.In1(Downsample4_out1),  // sfix16_En14
                                 .Out1(Subsystem12_out1)  // sfix16_En14
                                 );

  assign add_cast_10 = $signed({{16{Add4_out1[15]}}, Add4_out1});
```

```
  assign add_cast_11 = $signed({{16{Subsystem12_out1[15]}},
Subsystem12_out1});
  assign add_temp_5 = add_cast_10 + add_cast_11;
  assign Add7_out1_tmp = add_temp_5[31:0];

  assign Add7_out1 = Add7_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay4_process
      if (reset == 1'b1) begin
        Delay4_out1 <= 0;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          Delay4_out1 <= Delay3_out1;
        end
      end
    end // Delay4_process

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process13
      if (reset == 1'b1) begin
        regout_6 <= 0;
      end
      else begin
        if (enb_1_56_1 == 1'b1) begin
          regout_6 <= Delay4_out1;
        end
      end
    end // DataHoldRegister_temp_process13

  assign tmpout_5 = (enb_1_56_1 == 1'b1) ? Delay4_out1 :
              regout_6;
  assign Downsample5_out1 = tmpout_5;

  Subsystem7   u_Subsystem7   (.In1(Downsample5_out1),  // sfix16_En14
                               .Out1(Subsystem7_out1)  // sfix16_En14
                               );

  assign add_cast_12 = $signed({{16{Add7_out1[15]}}, Add7_out1});
  assign add_cast_13 = $signed({{16{Subsystem7_out1[15]}},
Subsystem7_out1});
  assign add_temp_6 = add_cast_12 + add_cast_13;
  assign Add11_out1_tmp = add_temp_6[31:0];

  assign Add11_out1 = Add11_out1_tmp[15:0];

// %%%% Up sample by 7, Sample offset 0 %%%%
  assign zero_1 = 16'b0000000000000000;
  assign muxout_1 = (enb_1_56_1 == 1'b1) ? Add11_out1 :
              zero_1;
```

```
// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process14
      if (reset == 1'b1) begin
        regout_7 <= 0;
      end
      else begin
        if (enb_7_56_1 == 1'b1) begin
          regout_7 <= muxout_1;
        end
      end
    end // DataHoldRegister_temp_process14

  assign Upsample1_out1 = (enb_7_56_1 == 1'b1) ? muxout_1 :
                    regout_7;
  assign add_cast_14 = $signed({{16{Delay10_out1[15]}}, Delay10_out1});
  assign add_cast_15 = $signed({{16{Upsample1_out1[15]}},
Upsample1_out1});
  assign add_temp_7 = add_cast_14 + add_cast_15;
  assign Add28_out1_tmp = add_temp_7[31:0];

  assign Add28_out1 = Add28_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay11_process
      if (reset == 1'b1) begin
        Delay11_out1 <= 0;
      end
      else begin
        if (enb_1_8_0 == 1'b1) begin
          Delay11_out1 <= Add28_out1;
        end
      end
    end // Delay11_process

  Subsystem15   u_Subsystem15   (.In1(Downsample2_out1),  // sfix16_En14
                                 .Out1(Subsystem15_out1)  // sfix16_En14
                                 );

  Subsystem18   u_Subsystem18   (.In1(Downsample3_out1),  // sfix16_En14
                                 .Out1(Subsystem18_out1)  // sfix16_En14
                                 );

  assign add_cast_16 = $signed({{16{Subsystem15_out1[15]}},
Subsystem15_out1});
  assign add_cast_17 = $signed({{16{Subsystem18_out1[15]}},
Subsystem18_out1});
  assign add_temp_8 = add_cast_16 + add_cast_17;
  assign Add5_out1_tmp = add_temp_8[31:0];

  assign Add5_out1 = Add5_out1_tmp[15:0];

  Subsystem21   u_Subsystem21   (.In1(Downsample4_out1),  // sfix16_En14
```

```
                                    .Out1(Subsystem21_out1)  // sfix16_En14
                                    );

  assign add_cast_18 = $signed({{16{Add5_out1[15]}}, Add5_out1});
  assign add_cast_19 = $signed({{16{Subsystem21_out1[15]}},
Subsystem21_out1});
  assign add_temp_9 = add_cast_18 + add_cast_19;
  assign Add8_out1_tmp = add_temp_9[31:0];

  assign Add8_out1 = Add8_out1_tmp[15:0];

  Subsystem23   u_Subsystem23   (.In1(Downsample5_out1),  // sfix16_En14
                                    .Out1(Subsystem23_out1)  // sfix16_En14
                                    );

  assign add_cast_20 = $signed({{16{Add8_out1[15]}}, Add8_out1});
  assign add_cast_21 = $signed({{16{Subsystem23_out1[15]}},
Subsystem23_out1});
  assign add_temp_10 = add_cast_20 + add_cast_21;
  assign Add12_out1_tmp = add_temp_10[31:0];

  assign Add12_out1 = Add12_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay5_process
      if (reset == 1'b1) begin
        Delay5_out1 <= 0;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          Delay5_out1 <= Delay4_out1;
        end
      end
    end // Delay5_process

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process15
      if (reset == 1'b1) begin
        regout_8 <= 0;
      end
      else begin
        if (enb_1_56_1 == 1'b1) begin
          regout_8 <= Delay5_out1;
        end
      end
    end // DataHoldRegister_temp_process15

  assign tmpout_6 = (enb_1_56_1 == 1'b1) ? Delay5_out1 :
              regout_8;
  assign Downsample6_out1 = tmpout_6;

  Subsystem25   u_Subsystem25   (.In1(Downsample6_out1),  // sfix16_En14
```

```
                                  .Out1(Subsystem25_out1)  // sfix16_En14
                                  );

  assign add_cast_22 = $signed({{16{Add12_out1[15]}}, Add12_out1});
  assign add_cast_23 = $signed({{16{Subsystem25_out1[15]}},
Subsystem25_out1});
  assign add_temp_11 = add_cast_22 + add_cast_23;
  assign Add16_out1_tmp = add_temp_11[31:0];

  assign Add16_out1 = Add16_out1_tmp[15:0];

// %%%% Up sample by 7, Sample offset 0 %%%%
  assign zero_2 = 16'b0000000000000000;
  assign muxout_2 = (enb_1_56_1 == 1'b1) ? Add16_out1 :
              zero_2;

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process16
      if (reset == 1'b1) begin
        regout_9 <= 0;
      end
      else begin
        if (enb_7_56_1 == 1'b1) begin
          regout_9 <= muxout_2;
        end
      end
    end // DataHoldRegister_temp_process16

  assign Upsample2_out1 = (enb_7_56_1 == 1'b1) ? muxout_2 :
                    regout_9;
  assign add_cast_24 = $signed({{16{Delay11_out1[15]}}, Delay11_out1});
  assign add_cast_25 = $signed({{16{Upsample2_out1[15]}},
Upsample2_out1});
  assign add_temp_12 = add_cast_24 + add_cast_25;
  assign Add29_out1_tmp = add_temp_12[31:0];

  assign Add29_out1 = Add29_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay12_process
      if (reset == 1'b1) begin
        Delay12_out1 <= 0;
      end
      else begin
        if (enb_1_8_0 == 1'b1) begin
          Delay12_out1 <= Add29_out1;
        end
      end
    end // Delay12_process

  Subsystem27   u_Subsystem27   (.In1(Downsample3_out1),  // sfix16_En14
                                  .Out1(Subsystem27_out1)  // sfix16_En14
```

```
                                );

  Subsystem29   u_Subsystem29   (.In1(Downsample4_out1),  // sfix16_En14
                                 .Out1(Subsystem29_out1)  // sfix16_En14
                                 );

  assign add_cast_26 = $signed({{16{Subsystem27_out1[15]}},
Subsystem27_out1});
  assign add_cast_27 = $signed({{16{Subsystem29_out1[15]}},
Subsystem29_out1});
  assign add_temp_13 = add_cast_26 + add_cast_27;
  assign Add9_out1_tmp = add_temp_13[31:0];

  assign Add9_out1 = Add9_out1_tmp[15:0];

  Subsystem31   u_Subsystem31   (.In1(Downsample5_out1),  // sfix16_En14
                                 .Out1(Subsystem31_out1)  // sfix16_En14
                                 );

  assign add_cast_28 = $signed({{16{Add9_out1[15]}}, Add9_out1});
  assign add_cast_29 = $signed({{16{Subsystem31_out1[15]}},
Subsystem31_out1});
  assign add_temp_14 = add_cast_28 + add_cast_29;
  assign Add13_out1_tmp = add_temp_14[31:0];

  assign Add13_out1 = Add13_out1_tmp[15:0];

  Subsystem33   u_Subsystem33   (.In1(Downsample6_out1),  // sfix16_En14
                                 .Out1(Subsystem33_out1)  // sfix16_En14
                                 );

  assign add_cast_30 = $signed({{16{Add13_out1[15]}}, Add13_out1});
  assign add_cast_31 = $signed({{16{Subsystem33_out1[15]}},
Subsystem33_out1});
  assign add_temp_15 = add_cast_30 + add_cast_31;
  assign Add17_out1_tmp = add_temp_15[31:0];

  assign Add17_out1 = Add17_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay6_process
      if (reset == 1'b1) begin
        Delay6_out1 <= 0;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          Delay6_out1 <= Delay5_out1;
        end
      end
    end // Delay6_process

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
```

```
    begin: DataHoldRegister_temp_process17
      if (reset == 1'b1) begin
        regout_10 <= 0;
      end
      else begin
        if (enb_1_56_1 == 1'b1) begin
          regout_10 <= Delay6_out1;
        end
      end
    end // DataHoldRegister_temp_process17

  assign tmpout_7 = (enb_1_56_1 == 1'b1) ? Delay6_out1 :
              regout_10;
  assign Downsample9_out1 = tmpout_7;

  Subsystem   u_Subsystem   (.In1(Downsample9_out1),  // sfix16_En14
                             .Out1(Subsystem_out1)  // sfix16_En14
                             );

  assign add_cast_32 = $signed({{16{Add17_out1[15]}}, Add17_out1});
  assign add_cast_33 = $signed({{16{Subsystem_out1[15]}},
Subsystem_out1});
  assign add_temp_16 = add_cast_32 + add_cast_33;
  assign Add6_out1_tmp = add_temp_16[31:0];

  assign Add6_out1 = Add6_out1_tmp[15:0];

// %%%% Up sample by 7, Sample offset 0 %%%%
  assign zero_3 = 16'b0000000000000000;
  assign muxout_3 = (enb_1_56_1 == 1'b1) ? Add6_out1 :
              zero_3;

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process18
      if (reset == 1'b1) begin
        regout_11 <= 0;
      end
      else begin
        if (enb_7_56_1 == 1'b1) begin
          regout_11 <= muxout_3;
        end
      end
    end // DataHoldRegister_temp_process18

  assign Upsample3_out1 = (enb_7_56_1 == 1'b1) ? muxout_3 :
                    regout_11;
  assign add_cast_34 = $signed({{16{Delay12_out1[15]}}, Delay12_out1});
  assign add_cast_35 = $signed({{16{Upsample3_out1[15]}},
Upsample3_out1});
  assign add_temp_17 = add_cast_34 + add_cast_35;
  assign Add30_out1_tmp = add_temp_17[31:0];

  assign Add30_out1 = Add30_out1_tmp[15:0];
```

```
  always @ (posedge clk or posedge reset)
    begin: Delay13_process
      if (reset == 1'b1) begin
        Delay13_out1 <= 0;
      end
      else begin
        if (enb_1_8_0 == 1'b1) begin
          Delay13_out1 <= Add30_out1;
        end
      end
    end // Delay13_process

  Subsystem35   u_Subsystem35   (.In1(Downsample4_out1),  // sfix16_En14
                                 .Out1(Subsystem35_out1)  // sfix16_En14
                                 );

  Subsystem34   u_Subsystem34   (.In1(Downsample5_out1),  // sfix16_En14
                                 .Out1(Subsystem34_out1)  // sfix16_En14
                                 );

  assign add_cast_36 = $signed({{16{Subsystem35_out1[15]}},
Subsystem35_out1});
  assign add_cast_37 = $signed({{16{Subsystem34_out1[15]}},
Subsystem34_out1});
  assign add_temp_18 = add_cast_36 + add_cast_37;
  assign Add10_out1_tmp = add_temp_18[31:0];

  assign Add10_out1 = Add10_out1_tmp[15:0];

  Subsystem32   u_Subsystem32   (.In1(Downsample6_out1),  // sfix16_En14
                                 .Out1(Subsystem32_out1)  // sfix16_En14
                                 );

  assign add_cast_38 = $signed({{16{Add10_out1[15]}}, Add10_out1});
  assign add_cast_39 = $signed({{16{Subsystem32_out1[15]}},
Subsystem32_out1});
  assign add_temp_19 = add_cast_38 + add_cast_39;
  assign Add14_out1_tmp = add_temp_19[31:0];

  assign Add14_out1 = Add14_out1_tmp[15:0];

  Subsystem30   u_Subsystem30   (.In1(Downsample9_out1),  // sfix16_En14
                                 .Out1(Subsystem30_out1)  // sfix16_En14
                                 );

  assign add_cast_40 = $signed({{16{Add14_out1[15]}}, Add14_out1});
  assign add_cast_41 = $signed({{16{Subsystem30_out1[15]}},
Subsystem30_out1});
  assign add_temp_20 = add_cast_40 + add_cast_41;
  assign Add15_out1_tmp = add_temp_20[31:0];

  assign Add15_out1 = Add15_out1_tmp[15:0];
```

```
  always @ (posedge clk or posedge reset)
    begin: Delay7_process
      if (reset == 1'b1) begin
        Delay7_out1 <= 0;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          Delay7_out1 <= Delay6_out1;
        end
      end
    end // Delay7_process

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process19
      if (reset == 1'b1) begin
        regout_12 <= 0;
      end
      else begin
        if (enb_1_56_1 == 1'b1) begin
          regout_12 <= Delay7_out1;
        end
      end
    end // DataHoldRegister_temp_process19

  assign tmpout_8 = (enb_1_56_1 == 1'b1) ? Delay7_out1 :
              regout_12;
  assign Downsample8_out1 = tmpout_8;

  Subsystem28   u_Subsystem28   (.In1(Downsample8_out1),  // sfix16_En14
                                 .Out1(Subsystem28_out1)  // sfix16_En14
                                 );

  assign add_cast_42 = $signed({{16{Add15_out1[15]}}, Add15_out1});
  assign add_cast_43 = $signed({{16{Subsystem28_out1[15]}},
Subsystem28_out1});
  assign add_temp_21 = add_cast_42 + add_cast_43;
  assign Add22_out1_tmp = add_temp_21[31:0];

  assign Add22_out1 = Add22_out1_tmp[15:0];

// %%%% Up sample by 7, Sample offset 0 %%%%
  assign zero_4 = 16'b0000000000000000;
  assign muxout_4 = (enb_1_56_1 == 1'b1) ? Add22_out1 :
              zero_4;

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process20
      if (reset == 1'b1) begin
        regout_13 <= 0;
      end
```

```
      else begin
        if (enb_7_56_1 == 1'b1) begin
          regout_13 <= muxout_4;
        end
      end
    end // DataHoldRegister_temp_process20

  assign Upsample4_out1 = (enb_7_56_1 == 1'b1) ? muxout_4 :
                    regout_13;
  assign add_cast_44 = $signed({{16{Delay13_out1[15]}}, Delay13_out1});
  assign add_cast_45 = $signed({{16{Upsample4_out1[15]}},
Upsample4_out1});
  assign add_temp_22 = add_cast_44 + add_cast_45;
  assign Add31_out1_tmp = add_temp_22[31:0];

  assign Add31_out1 = Add31_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay14_process
      if (reset == 1'b1) begin
        Delay14_out1 <= 0;
      end
      else begin
        if (enb_1_8_0 == 1'b1) begin
          Delay14_out1 <= Add31_out1;
        end
      end
    end // Delay14_process

  Subsystem26   u_Subsystem26   (.In1(Downsample5_out1),  // sfix16_En14
                                 .Out1(Subsystem26_out1)  // sfix16_En14
                                 );

  Subsystem24   u_Subsystem24   (.In1(Downsample6_out1),  // sfix16_En14
                                 .Out1(Subsystem24_out1)  // sfix16_En14
                                 );

  assign add_cast_46 = $signed({{16{Subsystem26_out1[15]}},
Subsystem26_out1});
  assign add_cast_47 = $signed({{16{Subsystem24_out1[15]}},
Subsystem24_out1});
  assign add_temp_23 = add_cast_46 + add_cast_47;
  assign Add18_out1_tmp = add_temp_23[31:0];

  assign Add18_out1 = Add18_out1_tmp[15:0];

  Subsystem22   u_Subsystem22   (.In1(Downsample9_out1),  // sfix16_En14
                                 .Out1(Subsystem22_out1)  // sfix16_En14
                                 );

  assign add_cast_48 = $signed({{16{Add18_out1[15]}}, Add18_out1});
  assign add_cast_49 = $signed({{16{Subsystem22_out1[15]}},
Subsystem22_out1});
```

```
  assign add_temp_24 = add_cast_48 + add_cast_49;
  assign Add20_out1_tmp = add_temp_24[31:0];

  assign Add20_out1 = Add20_out1_tmp[15:0];

  Subsystem19   u_Subsystem19   (.In1(Downsample8_out1),  // sfix16_En14
                                 .Out1(Subsystem19_out1)  // sfix16_En14
                                 );

  assign add_cast_50 = $signed({{16{Add20_out1[15]}}, Add20_out1});
  assign add_cast_51 = $signed({{16{Subsystem19_out1[15]}},
Subsystem19_out1});
  assign add_temp_25 = add_cast_50 + add_cast_51;
  assign Add23_out1_tmp = add_temp_25[31:0];

  assign Add23_out1 = Add23_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay9_process
      if (reset == 1'b1) begin
        Delay9_out1 <= 0;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          Delay9_out1 <= Delay7_out1;
        end
      end
    end // Delay9_process

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process21
      if (reset == 1'b1) begin
        regout_14 <= 0;
      end
      else begin
        if (enb_1_56_1 == 1'b1) begin
          regout_14 <= Delay9_out1;
        end
      end
    end // DataHoldRegister_temp_process21

  assign tmpout_9 = (enb_1_56_1 == 1'b1) ? Delay9_out1 :
              regout_14;
  assign Downsample7_out1 = tmpout_9;

  Subsystem16   u_Subsystem16   (.In1(Downsample7_out1),  // sfix16_En14
                                 .Out1(Subsystem16_out1)  // sfix16_En14
                                 );

  assign add_cast_52 = $signed({{16{Add23_out1[15]}}, Add23_out1});
  assign add_cast_53 = $signed({{16{Subsystem16_out1[15]}},
Subsystem16_out1});
```

```
  assign add_temp_26 = add_cast_52 + add_cast_53;
  assign Add25_out1_tmp = add_temp_26[31:0];

  assign Add25_out1 = Add25_out1_tmp[15:0];

// %%%% Up sample by 7, Sample offset 0 %%%%
  assign zero_5 = 16'b0000000000000000;
  assign muxout_5 = (enb_1_56_1 == 1'b1) ? Add25_out1 :
              zero_5;

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process22
      if (reset == 1'b1) begin
        regout_15 <= 0;
      end
      else begin
        if (enb_7_56_1 == 1'b1) begin
          regout_15 <= muxout_5;
        end
      end
    end // DataHoldRegister_temp_process22

  assign Upsample5_out1 = (enb_7_56_1 == 1'b1) ? muxout_5 :
                    regout_15;
  assign add_cast_54 = $signed({{16{Delay14_out1[15]}}, Delay14_out1});
  assign add_cast_55 = $signed({{16{Upsample5_out1[15]}},
Upsample5_out1});
  assign add_temp_27 = add_cast_54 + add_cast_55;
  assign Add32_out1_tmp = add_temp_27[31:0];

  assign Add32_out1 = Add32_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay15_process
      if (reset == 1'b1) begin
        Delay15_out1 <= 0;
      end
      else begin
        if (enb_1_8_0 == 1'b1) begin
          Delay15_out1 <= Add32_out1;
        end
      end
    end // Delay15_process

  Subsystem14   u_Subsystem14   (.In1(Downsample6_out1),  // sfix16_En14
                                 .Out1(Subsystem14_out1)  // sfix16_En14
                                 );

  Subsystem13   u_Subsystem13   (.In1(Downsample9_out1),  // sfix16_En14
                                 .Out1(Subsystem13_out1)  // sfix16_En14
                                 );
```

```
  assign add_cast_56 = $signed({{16{Subsystem14_out1[15]}},
Subsystem14_out1});
  assign add_cast_57 = $signed({{16{Subsystem13_out1[15]}},
Subsystem13_out1});
  assign add_temp_28 = add_cast_56 + add_cast_57;
  assign Add21_out1_tmp = add_temp_28[31:0];

  assign Add21_out1 = Add21_out1_tmp[15:0];

  Subsystem11   u_Subsystem11   (.In1(Downsample8_out1),  // sfix16_En14
                                 .Out1(Subsystem11_out1)  // sfix16_En14
                                 );

  assign add_cast_58 = $signed({{16{Add21_out1[15]}}, Add21_out1});
  assign add_cast_59 = $signed({{16{Subsystem11_out1[15]}},
Subsystem11_out1});
  assign add_temp_29 = add_cast_58 + add_cast_59;
  assign Add24_out1_tmp = add_temp_29[31:0];

  assign Add24_out1 = Add24_out1_tmp[15:0];

  Subsystem4   u_Subsystem4   (.In1(Downsample7_out1),  // sfix16_En14
                               .Out1(Subsystem4_out1)  // sfix16_En14
                               );

  assign add_cast_60 = $signed({{16{Add24_out1[15]}}, Add24_out1});
  assign add_cast_61 = $signed({{16{Subsystem4_out1[15]}},
Subsystem4_out1});
  assign add_temp_30 = add_cast_60 + add_cast_61;
  assign Add26_out1_tmp = add_temp_30[31:0];

  assign Add26_out1 = Add26_out1_tmp[15:0];


  always @ (posedge clk or posedge reset)
    begin: Delay8_process
      if (reset == 1'b1) begin
        Delay8_out1 <= 0;
      end
      else begin
        if (enb_1_7_0 == 1'b1) begin
          Delay8_out1 <= Delay9_out1;
        end
      end
    end // Delay8_process

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process23
      if (reset == 1'b1) begin
        regout_16 <= 0;
      end
      else begin
        if (enb_1_56_1 == 1'b1) begin
```

```
          regout_16 <= Delay8_out1;
        end
      end
    end // DataHoldRegister_temp_process23

  assign tmpout_10 = (enb_1_56_1 == 1'b1) ? Delay8_out1 :
              regout_16;
  assign Downsample10_out1 = tmpout_10;

  Subsystem3   u_Subsystem3   (.In1(Downsample10_out1),  // sfix16_En14
                               .Out1(Subsystem3_out1)  // sfix16_En14
                               );

  assign add_cast_62 = $signed({{16{Add26_out1[15]}}, Add26_out1});
  assign add_cast_63 = $signed({{16{Subsystem3_out1[15]}},
Subsystem3_out1});
  assign add_temp_31 = add_cast_62 + add_cast_63;
  assign Add27_out1_tmp = add_temp_31[31:0];

  assign Add27_out1 = Add27_out1_tmp[15:0];

// %%%% Up sample by 7, Sample offset 0 %%%%
  assign zero_6 = 16'b0000000000000000;
  assign muxout_6 = (enb_1_56_1 == 1'b1) ? Add27_out1 :
             zero_6;

// %%%% Bypass Register %%%%
  always @ (posedge clk or posedge reset)
    begin: DataHoldRegister_temp_process24
      if (reset == 1'b1) begin
        regout_17 <= 0;
      end
      else begin
        if (enb_7_56_1 == 1'b1) begin
          regout_17 <= muxout_6;
        end
      end
    end // DataHoldRegister_temp_process24

  assign Upsample7_out1 = (enb_7_56_1 == 1'b1) ? muxout_6 :
                   regout_17;
  assign add_cast_64 = $signed({{16{Delay15_out1[15]}}, Delay15_out1});
  assign add_cast_65 = $signed({{16{Upsample7_out1[15]}},
Upsample7_out1});
  assign add_temp_32 = add_cast_64 + add_cast_65;
  assign Add33_out1_tmp = add_temp_32[31:0];

  assign Add33_out1 = Add33_out1_tmp[15:0];

  assign Out1 = Add33_out1;

endmodule  // pol78cse4
```