```
`timescale 1 ns / 1 ns

module caspol
          (
           clk,
           reset,
           clk_enable,
           ce_out,
           Out1
          );


  input   clk;
  input   reset;
  input   clk_enable;
  output  ce_out;
  output  signed [95:0] Out1;  // sfix96_En60


  wire enb_1_147_0;
  wire enb_1_735_1;
  wire enb_1_105_0;
  wire enb_1_105_1;
  wire enb_1_840_1;
  wire enb_1_120_0;
  wire enb_1_120_1;
  wire enb_1_480_1;
  wire enb_1_160_0;
  wire enb_1_160_1;
  wire signed [31:0] Subsystem_out1;  // sfix32_En29
  wire signed [63:0] Subsystem1_out1;  // sfix64_En44
  wire signed [95:0] Subsystem2_out1;  // sfix96_En60


  caspol_tc   u_caspol_tc   (.clk(clk),
                             .reset(reset),
                             .clk_enable(clk_enable),
                             .enb_1_105_0(enb_1_105_0),
                             .enb_1_105_1(enb_1_105_1),
                             .enb_1_120_0(enb_1_120_0),
                             .enb_1_120_1(enb_1_120_1),
                             .enb_1_147_0(enb_1_147_0),
                             .enb_1_160_0(enb_1_160_0),
                             .enb_1_160_1(enb_1_160_1),
                             .enb_1_480_1(enb_1_480_1),
                             .enb_1_735_1(enb_1_735_1),
                             .enb_1_840_1(enb_1_840_1)
                             );

  Subsystem   u_Subsystem   (.clk(clk),
                             .reset(reset),
                             .enb_1_147_0(enb_1_147_0),
                             .enb_1_735_1(enb_1_735_1),
                             .enb_1_105_0(enb_1_105_0),
```

```
                              .enb_1_105_1(enb_1_105_1),
                              .Out1(Subsystem_out1)  // sfix32_En29
                              );

  Subsystem1   u_Subsystem1   (.clk(clk),
                               .reset(reset),
                               .enb_1_105_0(enb_1_105_0),
                               .enb_1_840_1(enb_1_840_1),
                               .enb_1_120_0(enb_1_120_0),
                               .enb_1_120_1(enb_1_120_1),
                               .In1(Subsystem_out1),  // sfix32_En29
                               .Out1(Subsystem1_out1)  // sfix64_En44
                               );

  Subsystem2   u_Subsystem2   (.clk(clk),
                               .reset(reset),
                               .enb_1_120_0(enb_1_120_0),
                               .enb_1_480_1(enb_1_480_1),
                               .enb_1_160_0(enb_1_160_0),
                               .enb_1_160_1(enb_1_160_1),
                               .In1(Subsystem1_out1),  // sfix64_En44
                               .Out1(Subsystem2_out1)  // sfix96_En60
                               );

  assign Out1 = Subsystem2_out1;

  assign ce_out = enb_1_160_1;

endmodule  // caspol
```