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ASSIGNMENT_3_Extended

Question 1

I. RTL Design

```
module queue;
int j = 1;
int q[$] = {0,2,5};
initial begin
q. insert(1, j);
$display("The Queue = %0p", q); // q = (0,1,2,5)
q. delete(1);
$display("The Queue = %0p", q); // q = (0,2,5)
q. push_front(7);
$display("The Queue = %0p", q); // q = (7,0,2,5)
q. push_back(9);
$display("The Queue = %0p", q); // q = (7,0,2,5,9)
j = q. pop_back();
$display("The Queue = %0p & j =
j,=qq.jpop/front();7,0,2,5) & j = 9
$display("The Queue = %0p & j =
q, qevpse();q = (0,2,5) & j = 7
$display("The Queue = %0p After Reverse", q); // q = (5,2,0)
q. sort();
$display("The Queue = %0p After Sort", q); // q = (0,2,5)
q. rsort();
$display("The Queue = %0p After Reverse Sort", q); // q = (5,2,0)
q. shuffle();
$display("The Queue = %0p After Shuffle", q); // q = Random like (2,0,5)
$stop;
end
endmodule
```

```
# The Queue = 0 1 2 5
# The Queue = 0 2 5
# The Queue = 7 0 2 5
# The Queue = 7 0 2 5 9
# The Queue = 7 0 2 5 & j = 9
# The Queue = 0 2 5 & j = 7
# The Queue = 5 2 0 After Reverse
# The Queue = 0 2 5 After Sort
# The Queue = 5 2 0 After Reverse Sort
# The Queue = 2 0 5 After Shuffle
```

Question 2

I. Verification Plan

Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check
ADDER_1	When the reset is asserted, the output C should be zero.	reset signal is randomized and set high during certain periods to simulate reset events.	Ensure reset transitions are covered and the impact on the output C is observed.	A checker ensures that C is set to zero when reset is high.
ADDER_2	The output C should equal the sum of the inputs A and B.	Randomized values for A and B are generated for each clock cycle.	Ensure all possible combinations of A and B values (including boundary conditions) are covered.	A checker verifies if C matches A + B after each clock cycle.
ADDER_3	Ensure correct output when input values A and B include both positive and negative values (2's complement).	Randomized signed values of A and B are applied, ensuring both positive and negative values are tested.	Functional coverage for positive, negative, and zero values of A and B.	A checker validates that C correctly handles signed addition, ensuring 2's complement behavior is correct.
ADDER_4	Ensure the design can handle multiple consecutive additions without reset (clock toggling under random conditions).	clk is toggled with random inputs for A and B over multiple iterations.	Coverage includes consecutive additions, ensuring the design remains stable under continuous operation without reset.	A checker ensures that the output C is correct after each addition across multiple clock cycles.
ADDER_5	Ensure functionality under rapid toggle rate for the clock and random inputs for A and B.	The clk, A, and B values are toggled frequently to simulate rapid input changes.	Functional coverage for rapid input changes and clock frequency variations.	A checker ensures the output C remains valid under rapid input changes and fast clock toggling, without introducing errors.
ADDER_6	Ensure that the error count is correctly incremented when the output does not match the expected sum of A and B.	Randomized input values for A, B, and reset are generated, and output is compared to the expected result.	Ensure full functional coverage of cases where errors occur, tracking incorrect results across multiple test iterations.	A checker increments error_count whenever the output does not match the expected value, and correct_count for valid outputs.

II. RTL Design

```
module adder (
    input  clk,
    input  reset,
    input  signed [3:0] A, // Input data A in 2's complement
    input  signed [3:0] B, // Input data B in 2's complement
    output reg signed [4:0] C // Adder output in 2's complement
        );

   // Register output C
   always @(posedge clk or posedge reset) begin
      if (reset)
        C <= 5'b0;
      else
        C <= A + B;
   end

endmodule

```

III. Package

```
package pck;
typedef enum bit signed [3:0] {MAXNEG=-4'd8, MAXPOS=4'd7,ZERO=4'd0} values_p;
class addr;
rand bit reset_c;
bit clk;
rand bit signed [3:0] A_c, B_c;
constraint c_reset {reset_c dist {0:/90, 1:/10};}
constraint A_c_dist {A_c dist { MAXPOS :/ 30,ZERO   :/ 30, MAXNEG :/ 30,[1:6] :/ 5,[-7:-1] :/ 5};}
constraint B_c_dist {B_c dist { MAXPOS :/ 30,ZERO   :/ 30, MAXNEG :/ 30,[1:6] :/ 5,[-7:-1] :/ 5};}
covergroup Covgrp_A @(posedge clk);
    Covgrp_A_cp1: coverpoint A_c {
        bins data_0 ={ZERO};
        bins data_max ={MAXPOS};
        bins data_min ={MAXNEG};
        bins data_default = {[1:6],[-7:-1]} ;
    }
    Covgrp_A_cp2: coverpoint A_c {
        bins data_0max = (ZERO => MAXPOS);
        bins data_maxmin = (MAXPOS => MAXNEG);
        bins data_minmax = (MAXNEG => MAXPOS);
    }
    endgroup
    covergroup Covgrp_B @(posedge clk);
    Covgrp_B_cp1: coverpoint B_c {
        bins data_0 ={ZERO};
        bins data_max ={MAXPOS};
        bins data_min ={MAXNEG};
        bins data_default = {[1:6],[-7:-1]} ;
    }
    Covgrp_B_cp2: coverpoint B_c {
        bins data_0max = (ZERO => MAXPOS);
        bins data_maxmin = (MAXPOS => MAXNEG);
        bins data_minmax = (MAXNEG => MAXPOS);
    }
    endgroup
    function new();
        Covgrp_A  = new();
        Covgrp_B  = new();
    endfunction
    task sample_adder();
      if (!reset_c == 0) begin
        Covgrp_A.sample();
        Covgrp_B.sample();
      end
    endtask
endclass
endpackage
```

IV. Test Bench

```
import pck::*;
module ADDER_TB;
     logic clk;
     logic reset;
     logic signed [3:0] A;  // Input data A in 2's complement
     logic signed [3:0] B; // Input data B in 2's complement
     logic signed [4:0] C;     // Adder output in 2's complement
  adder DUT (.*);
 initial begin
    clk = 0;
    forever begin
    #1 clk = ~clk;
    obj.clk=clk;
    end
end
addr obj= new;
int error_count;
int correct_count;
initial begin
correct_count=0;
error_count=0;
repeat(40)begin
assert (obj.randomize());
A=obj.A_c;
B=obj.B_c;
reset=obj.reset_c;
@(negedge clk);
check_result(A + B);
end
$display("error_count=%d , correct_count=%d",error_count,correct_count);
$stop;
end
task check_result(input signed [4:0] expected_result);
 @(negedge clk);
if (reset)
 expected_result=0;
if(expected_result !== C )begin
 $display ("incorrect result");
error_count++;
end
else correct_count++;
endtask
endmodule
```

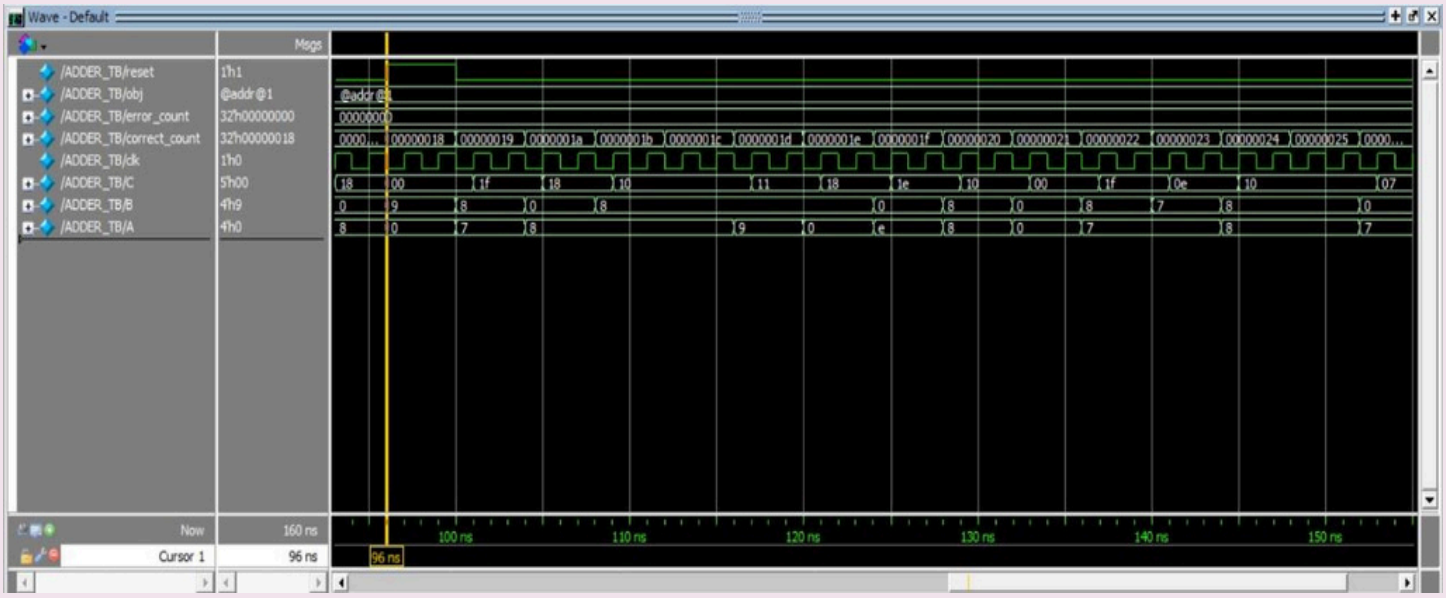
V. Do file

```
vlib work
vlog adder.v package.svh ADDER_TB.sv  +cover -covercells
vsim -voptargs=+acc work.ADDER_TB -cover
add wave *
coverage save ADDER_TB.ucdb -onexit
run -all
```

VI. Counters

```
# error_count=          0 , correct_count=          40
```

VII. Waveform



VIII. Functional Coverage Report

```
Coverage Report by instance with details

================================================================================
=== Instance: /pck
=== Design Unit: work.pck
================================================================================

Covergroup Coverage:
    Covergroups                     2        na        na   100.00%
        Coverpoints/Crosses         4        na        na        na
            Covergroup Bins        14        14         0   100.00%
--------------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

--------------------------------------------------------------------------------------------------------
 TYPE /pck/addr/Covgrp_A                          100.00%        100          -    Covered
    covered/total bins:                                 7          7          -
    missing/total bins:                                 0          7          -
    % Hit:                                       100.00%        100          -
    Coverpoint Covgrp_A_cp1                      100.00%        100          -    Covered
        covered/total bins:                             4          4          -
        missing/total bins:                             0          4          -
        % Hit:                                   100.00%        100          -
    Coverpoint Covgrp_A_cp2                      100.00%        100          -    Covered
        covered/total bins:                             3          3          -
        missing/total bins:                             0          3          -
        % Hit:                                   100.00%        100          -
 Covergroup instance \/pck::addr::Covgrp_A       100.00%        100          -    Covered
    covered/total bins:                                 7          7          -
    missing/total bins:                                 0          7          -
    % Hit:                                       100.00%        100          -
    Coverpoint Covgrp_A_cp1                      100.00%        100          -    Covered
        covered/total bins:                             4          4          -
        missing/total bins:                             0          4          -
        % Hit:                                   100.00%        100          -
        bin data_0                                     26          1          -    Covered
        bin data_max                                   24          1          -    Covered
        bin data_min                                   24          1          -    Covered
        bin data_default                                6          1          -    Covered
    Coverpoint Covgrp_A_cp2                      100.00%        100          -    Covered
        covered/total bins:                             3          3          -
        missing/total bins:                             0          3          -
        % Hit:                                   100.00%        100          -
        bin data_0max                                   5          1          -    Covered
        bin data_maxmin                                 4          1          -    Covered
        bin data_minmax                                 2          1          -    Covered
 TYPE /pck/addr/Covgrp_B                          100.00%        100          -    Covered
    covered/total bins:                                 7          7          -
    missing/total bins:                                 0          7          -
    % Hit:                                       100.00%        100          -
    Coverpoint Covgrp_B_cp1                      100.00%        100          -    Covered
        covered/total bins:                             4          4          -
        missing/total bins:                             0          4          -
        % Hit:                                   100.00%        100          -
    Coverpoint Covgrp_B_cp2                      100.00%        100          -    Covered
        covered/total bins:                             3          3          -
        missing/total bins:                             0          3          -
        % Hit:                                   100.00%        100          -
 Covergroup instance \/pck::addr::Covgrp_B       100.00%        100          -    Covered
    covered/total bins:                                 7          7          -
    missing/total bins:                                 0          7          -
    % Hit:                                       100.00%        100          -
```

```
    covered/total bins:                    7          7          -
    missing/total bins:                    0          7          -
    % Hit:                            100.00%        100          -
    Coverpoint Covgrp_B_cp1           100.00%        100          -    Covered
        covered/total bins:                4          4          -
        missing/total bins:                0          4          -
        % Hit:                        100.00%        100          -
        bin data_0                        26          1          -    Covered
        bin data_max                      16          1          -    Covered
        bin data_min                      32          1          -    Covered
        bin data_default                   6          1          -    Covered
    Coverpoint Covgrp_B_cp2           100.00%        100          -    Covered
        covered/total bins:                3          3          -
        missing/total bins:                0          3          -
        % Hit:                        100.00%        100          -
        bin data_0max                      2          1          -    Covered
        bin data_maxmin                    4          1          -    Covered
        bin data_minmax                    6          1          -    Covered

COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------
Covergroup                                Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------
 TYPE /pck/addr/Covgrp_A                  100.00%        100          -    Covered
    covered/total bins:                    7          7          -
    missing/total bins:                    0          7          -
    % Hit:                            100.00%        100          -
    Coverpoint Covgrp_A_cp1           100.00%        100          -    Covered
        covered/total bins:                4          4          -
        missing/total bins:                0          4          -
        % Hit:                        100.00%        100          -
    Coverpoint Covgrp_A_cp2           100.00%        100          -    Covered
        covered/total bins:                3          3          -
        missing/total bins:                0          3          -
        % Hit:                        100.00%        100          -
 Covergroup instance \/pck::addr::Covgrp_A 100.00%        100          -    Covered
    covered/total bins:                    7          7          -
    missing/total bins:                    0          7          -
    % Hit:                            100.00%        100          -
    Coverpoint Covgrp_A_cp1           100.00%        100          -    Covered
        covered/total bins:                4          4          -
        missing/total bins:                0          4          -
        % Hit:                        100.00%        100          -
        bin data_0                        26          1          -    Covered
        bin data_max                      24          1          -    Covered
        bin data_min                      24          1          -    Covered
        bin data_default                   6          1          -    Covered
    Coverpoint Covgrp_A_cp2           100.00%        100          -    Covered
        covered/total bins:                3          3          -
        missing/total bins:                0          3          -
        % Hit:                        100.00%        100          -
        bin data_0max                      5          1          -    Covered
        bin data_maxmin                    4          1          -    Covered
        bin data_minmax                    2          1          -    Covered
 TYPE /pck/addr/Covgrp_B                  100.00%        100          -    Covered
    covered/total bins:                    7          7          -
    missing/total bins:                    0          7          -
    % Hit:                            100.00%        100          -
    Coverpoint Covgrp_B_cp1           100.00%        100          -    Covered
        covered/total bins:                4          4          -
        missing/total bins:                0          4          -
        % Hit:                        100.00%        100          -
    Coverpoint Covgrp_B_cp2           100.00%        100          -    Covered
```

```
        % Hit:                                  100.00%        100          -
    Coverpoint Covgrp_B_cp2                    100.00%        100          -    Covered
        covered/total bins:                          3          3          -
        missing/total bins:                          0          3          -
        % Hit:                                 100.00%        100          -
 Covergroup instance \/pck::addr::Covgrp_B     100.00%        100          -    Covered
    covered/total bins:                              7          7          -
    missing/total bins:                              0          7          -
    % Hit:                                     100.00%        100          -
    Coverpoint Covgrp_B_cp1                    100.00%        100          -    Covered
        covered/total bins:                          4          4          -
        missing/total bins:                          0          4          -
        % Hit:                                 100.00%        100          -
        bin data_0                                  26          1          -    Covered
        bin data_max                                16          1          -    Covered
        bin data_min                                32          1          -    Covered
        bin data_default                             6          1          -    Covered
    Coverpoint Covgrp_B_cp2                    100.00%        100          -    Covered
        covered/total bins:                          3          3          -
        missing/total bins:                          0          3          -
        % Hit:                                 100.00%        100          -
        bin data_0max                                2          1          -    Covered
        bin data_maxmin                              4          1          -    Covered
        bin data_minmax                              6          1          -    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 2

Total Coverage By Instance (filtered view): 100.00%
```

IX. Coverage Report

```
Coverage Report by instance with details

================================================================================
=== Instance: /\ADDER_TB#DUT
=== Design Unit: work.adder
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         2         2         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\ADDER_TB#DUT

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File adder.v
-----------------------------------IF Branch-----------------------------------
    11                                        73     Count coming in to IF
    11              1                          6
    13              1                         67
Branch totals: 2 hits of 2 branches = 100.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       3         3         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\ADDER_TB#DUT  --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File adder.v
    10              1                         73
    12              1                          6
    14              1                         67
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         30        30         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\ADDER_TB#DUT  --

                                    Node      1H->0L      0L->1H  "Coverage"
                                    ----------------------------------------
                                   A[0-3]           1           1      100.00
                                   B[0-3]           1           1      100.00
                                   C[4-0]           1           1      100.00
                                      clk           1           1      100.00
                                    reset           1           1      100.00

Total Node Count     =         15
Toggled Node Count   =         15
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (30 of 30 bins)


Total Coverage By Instance (filtered view): 100.00%
```

Question 3

I. Verification plan

Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check
FSM_1	When the reset (rst) is asserted, the output y and users_count should be set to initial values (0 or expected value).	rst is set high at the start of the simulation. Then randomized with constraints to be high 90% of the time to simulate reset events.	Ensure coverage of rst transitions and the effect on y and users_count.	A checker in the testbench ensures y and users_count are set correctly when rst is asserted.
FSM_2	The output y should match the expected y_expected when the system processes the input x.	Randomized input values for x are generated at each clock cycle.	Ensure x values are covered, and the effect on y is observed during each iteration.	A checker verifies if y matches y_expected during every input change.
FSM_3	The users_count output should increment or behave according to the FSM state machine based on the input x and the FSM's internal states.	Randomized values for x and users_count are generated during the simulation.	Cover all FSM state transitions and the effect on users_count, ensuring boundary conditions like overflow are included.	A checker ensures users_count matches the expected count, and there are no overflow errors during the FSM's operation.
FSM_4	Ensure the FSM transitions between states IDLE, ZERO, ONE, and STORE based on the input x and other conditions like reset.	Randomized transitions between states are driven by input x and rst.	Ensure full coverage of FSM state transitions, including edge cases like rapid switching between states.	A checker validates that the FSM transitions to the correct state based on x, and outputs the correct values for each state.
FSM_5	Ensure functionality under random high toggle rate for clock and inputs (x).	Toggle clk and x frequently to simulate rapid input changes and clock toggling.	Functional coverage for high-frequency inputs and clock changes, ensuring the FSM handles rapid changes without failure.	A checker ensures the FSM outputs remain consistent and valid even under rapid input changes and clock toggling.

II. RTL Design

```
module FSM(clk, rst, x, y, users_count);
    parameter IDLE  = 2'b00;
    parameter ZERO  = 2'b01;
    parameter ONE   = 2'b10;
    parameter STORE = 2'b11;
    input clk, rst, x;
    output y;
    output reg [9:0] users_count;
    reg [1:0] cs, ns;
    always @(*) begin
        case (cs)
            IDLE:
                if (x)
                    ns = IDLE;
                else
                    ns = ZERO;
            ZERO:
                if (x)
                    ns = ONE;
                else
                    ns = ZERO;
            ONE:
                if (x)
                    ns = IDLE;
                else
                    ns = STORE;
            STORE:
                if (x)
                    ns = IDLE;
                else
                    ns = ZERO;
            default: ns = IDLE;
        endcase
    end
    always @(posedge clk or posedge rst) begin
        if (rst) begin
            cs <= IDLE;
            users_count <= 10'b0;
        end else begin
            cs <= ns;
        end
    end
    always @(posedge clk or posedge rst) begin
        if (rst) begin
            users_count <= 10'b0;
        end else begin
            if (cs == STORE)
                users_count <= users_count + 1;
        end
    end
    assign y = (cs == STORE) ? 1 : 0;
endmodule
```

III. Golden Model

```
module FSM_GM(x, clk, rst, y_exp, count_exp);
    parameter STORE = 2'b00;
    parameter IDLE = 2'b01;
    parameter ZERO = 2'b10;
    parameter ONE = 2'b11;
    input x, clk, rst;
    output reg y_exp;
    output reg [9:0] count_exp;
    reg [1:0] cs, ns;
    // Next state Logic
    always @(cs or x) begin
        case (cs)
            STORE :
                if (x)
                    ns = IDLE;
                else
                    ns = ZERO;
            IDLE :
                if (x)
                    ns = IDLE;
                else
                    ns = ZERO;
            ZERO :
                if (x)
                    ns = ONE;
                else
                    ns = ZERO;
            ONE :
                if (x)
                    ns = IDLE;
                else
                    ns = STORE;
            default : ns = IDLE;
        endcase
    end
    // State Memory
    always @(posedge clk or posedge rst) begin
        if (rst) begin
            cs <= IDLE;
            count_exp <= 10'b0;
        end else
            cs <= ns;
    end
    always @(cs) begin
        case (cs)
            STORE : begin
                y_exp = 1;
                count_exp = count_exp + 1;
            end
            IDLE, ZERO, ONE : y_exp = 0;
        endcase
    end
endmodule
```

IV. Package

```
package pck;

typedef enum logic[1:0] {IDLE , ZERO ,ONE , STORE}  state_e ;

class fsm_trs;
rand bit rst_c , x_c ;
bit y_exp,clk ;
bit [9: 0] users_count_exp ;
constraint C_inputs { rst_c dist {0:= 90 , 1:= 10};x_c dist {0:/67 , 1:/33};}
covergroup cg_x_transition@(posedge clk);

    x_transition: coverpoint x_c {
        bins x_0_to_1_to_0 = (0 => 1 => 0);
    }
endgroup
function new ;
cg_x_transition = new();
endfunction

endclass

endpackage
```

V. Test bench

```
import pck::*;
module FSM_TB;
// Parameters
parameter IDLE = 2'b00;
parameter ZERO = 2'b01;
parameter ONE = 2'b10;
parameter STORE = 2'b11;
// Signal declarations
bit clk, rst, x;
bit y, y_expected;
bit [9:0] users_count, users_count_expected;
int error_counter, correct_counter;
// FSM transaction object
fsm_trs obj=new; // create object from the class
// DUT instantiation
FSM #(.IDLE(IDLE), .ZERO(ZERO), .ONE(ONE), .STORE(STORE))
DUT_Design (clk, rst, x, y, users_count);
FSM_GM #(.IDLE(IDLE), .ZERO(ZERO), .ONE(ONE), .STORE(STORE))
DUT_GOLD (x, clk, rst, y_expected, users_count_expected);
// Clock generation
initial begin
    clk = 0;
    forever begin #1 clk = ~clk;
    obj.clk=clk;
end
end
// Testbench logic
initial begin
    error_counter = 0;
    correct_counter = 0;
    // Generate random inputs and apply them
    repeat (20000) begin
        assert(obj.randomize());  // Randomize inputs
          rst = obj.rst_c;
          x = obj.x_c;
        obj.users_count_exp = users_count_expected;
        obj.y_exp = y_expected;
        check_result();          // Check results
    end

    $display("Error_Counter =
 , Correct_Counter =
", error_counter, correct_counter);
    // Check Result Task
    task check_result();
        @(negedge clk);
       if ((y !== y_expected) && (users_count !== users_count_expected)) begin
    error_counter++;
end
else
correct_counter++;
    endtask
endmodule
```

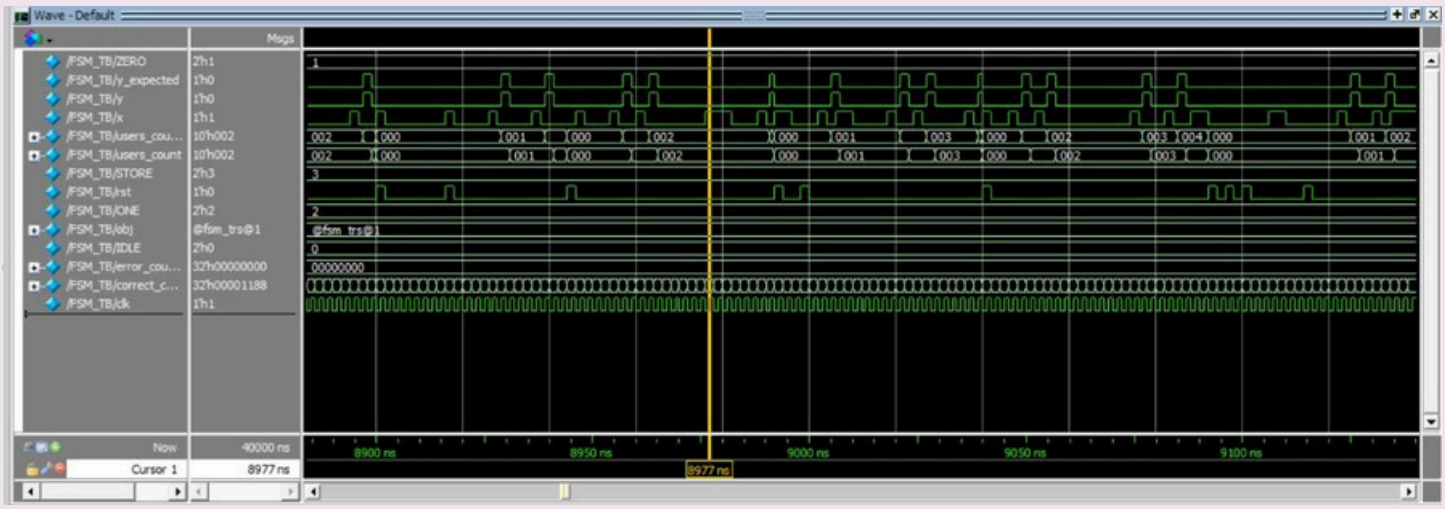
VI. Counters

```
# Error_Counter = 0 , Correct_Counter = 20000
```

VII. Do file

```
vlib work
vlog FSM.v FSM_TB.sv FSM_GM.v pck.sv  +cover -covercells
vsim -voptargs=+acc work.FSM_TB -cover
add wave *
coverage save FSM_TB.ucdb -onexit
run -all
```

VIII. Waveform



IX. Functional Coverage report

```
Coverage Report by instance with details

================================================================================
=== Instance: /pck
=== Design Unit: work.pck
================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na   100.00%
        Coverpoints/Crosses     1        na        na        na
            Covergroup Bins     1         1         0   100.00%
--------------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

--------------------------------------------------------------------------------------------------------
 TYPE /pck/fsm_trs/cg_x_transition                 100.00%        100          -    Covered
    covered/total bins:                                  1          1          -
    missing/total bins:                                  0          1          -
    % Hit:                                         100.00%        100          -
    Coverpoint x_transition                        100.00%        100          -    Covered
        covered/total bins:                              1          1          -
        missing/total bins:                              0          1          -
        % Hit:                                     100.00%        100          -
 Covergroup instance \/pck::fsm_trs::cg_x_transition
                                                   100.00%        100          -    Covered
    covered/total bins:                                  1          1          -
    missing/total bins:                                  0          1          -
    % Hit:                                         100.00%        100          -
    Coverpoint x_transition                        100.00%        100          -    Covered
        covered/total bins:                              1          1          -
        missing/total bins:                              0          1          -
        % Hit:                                     100.00%        100          -
        bin x_0_to_1_to_0                             3011          1          -    Covered

COVERGROUP COVERAGE:
--------------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

--------------------------------------------------------------------------------------------------------
 TYPE /pck/fsm_trs/cg_x_transition                 100.00%        100          -    Covered
    covered/total bins:                                  1          1          -
    missing/total bins:                                  0          1          -
    % Hit:                                         100.00%        100          -
    Coverpoint x_transition                        100.00%        100          -    Covered
        covered/total bins:                              1          1          -
        missing/total bins:                              0          1          -
        % Hit:                                     100.00%        100          -
 Covergroup instance \/pck::fsm_trs::cg_x_transition
                                                   100.00%        100          -    Covered
    covered/total bins:                                  1          1          -
    missing/total bins:                                  0          1          -
    % Hit:                                         100.00%        100          -
    Coverpoint x_transition                        100.00%        100          -    Covered
        covered/total bins:                              1          1          -
        missing/total bins:                              0          1          -
        % Hit:                                     100.00%        100          -
        bin x_0_to_1_to_0                             3011          1          -    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 100.00%
```

X. Coverage Report

```
Coverage Report by instance with details

================================================================================
=== Instance: /\FSM_TB#DUT_Design
=== Design Unit: work.FSM
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        21        21         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\FSM_TB#DUT_Design

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File FSM.v
-----------------------------------CASE Branch-----------------------------------
    11                                     20983     Count coming in to CASE
    12              1                       5760
    17              1                       7532
    22              1                       5201
    27              1                       2489
    32              1                          1
Branch totals: 5 hits of 5 branches = 100.00%

-------------------------------------IF Branch-------------------------------------
    13                                      5760     Count coming in to IF
    13              1                       2386
    15              1                       3374
Branch totals: 2 hits of 2 branches = 100.00%

-------------------------------------IF Branch-------------------------------------
    18                                      7532     Count coming in to IF
    18              1                       3429
    20              1                       4103
Branch totals: 2 hits of 2 branches = 100.00%

-------------------------------------IF Branch-------------------------------------
    23                                      5201     Count coming in to IF
    23              1                       3107
    25              1                       2094
Branch totals: 2 hits of 2 branches = 100.00%

-------------------------------------IF Branch-------------------------------------
    28                                      2489     Count coming in to IF
    28              1                        597
    30              1                       1892
Branch totals: 2 hits of 2 branches = 100.00%

-------------------------------------IF Branch-------------------------------------
    36                                     17678     Count coming in to IF
    36              1                       3701
    39              1                      13977
Branch totals: 2 hits of 2 branches = 100.00%

-------------------------------------IF Branch-------------------------------------
    44                                     14879     Count coming in to IF
    44              1                       3598
    46              1                      11281
Branch totals: 2 hits of 2 branches = 100.00%

-------------------------------------IF Branch-------------------------------------
    47                                     11281     Count coming in to IF
    47              1                       1708
                                            9573     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-------------------------------------IF Branch-------------------------------------
    51                                     12022     Count coming in to IF
    51              1                       1892
    51              2                      10130
Branch totals: 2 hits of 2 branches = 100.00%
```

```
Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                       2         2         0   100.00%

================================Condition Details================================

Condition Coverage for instance /\FSM_TB#DUT_Design  --

  File FSM.v
----------------Focused Condition View-------------------
Line       47 Item    1  (cs == 3)
Condition totals: 1 of 1 input term covered = 100.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  -------------
   (cs == 3)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (cs == 3)_0           -
  Row   2:          1  (cs == 3)_1           -

----------------Focused Condition View-------------------
Line       51 Item    1  (cs == 3)
Condition totals: 1 of 1 input term covered = 100.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  -------------
   (cs == 3)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (cs == 3)_0           -
  Row   2:          1  (cs == 3)_1           -


FSM Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    FSM States                       4         4         0   100.00%
    FSM Transitions                  7         7         0   100.00%

================================FSM Details================================

FSM Coverage for instance /\FSM_TB#DUT_Design  --

FSM_ID: cs
    Current State Object : cs
    ---------------------
    State Value MapInfo :
    ---------------------
Line           State Name               Value
----           ----------               -----
  12                 IDLE                   0
  17                 ZERO                   1
  22                  ONE                   2
  27                STORE                   3
    Covered States :
    ----------------
                   State           Hit_count
                   -----           ---------
                    IDLE                6127
                    ZERO                6552
                     ONE                3107
                   STORE                1892
    Covered Transitions :
    ---------------------
Line            Trans_ID           Hit_count          Transition
----            --------           ---------          ----------
  16                   0                2920          IDLE -> ZERO
  19                   1                3107          ZERO -> ONE
  37                   2                 995          ZERO -> IDLE
  26                   3                1892          ONE -> STORE
  24                   4                1215          ONE -> IDLE
  31                   5                1183          STORE -> ZERO
  29                   6                 709          STORE -> IDLE
```

```
    Summary                       Bins      Hits    Misses  Coverage
    -------                       ----      ----    ------  --------
        FSM States                   4         4         0   100.00%
        FSM Transitions              7         7         0   100.00%
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                     18        18         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\FSM_TB#DUT_Design  --

    Line         Item                     Count     Source
    ----         ----                     -----     ------
  File FSM.v
    10              1                     20983
    14              1                      2386
    16              1                      3374
    19              1                      3429
    21              1                      4103
    24              1                      3107
    26              1                      2094
    29              1                       597
    31              1                      1892
    32              1                         1
    35              1                     17678
    37              1                      3701
    38              1                      3701
    40              1                     13977
    43              1                     14879
    45              1                      3598
    48              1                      1708
    51              1                     12023
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                        24        24         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\FSM_TB#DUT_Design  --

                                          Node      1H->0L      0L->1H  "Coverage"
                                          ----------------------------------------
                                           clk           1           1      100.00
                                        cs[1-0]          1           1      100.00
                                        ns[1-0]          1           1      100.00
                                           rst           1           1      100.00
                                 users_count[3-0]        1           1      100.00
                                             x           1           1      100.00
                                             y           1           1      100.00

Total Node Count     =         12
Toggled Node Count   =         12
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (24 of 24 bins)


Total Coverage By Instance (filtered view): 100.00%
```

XI. Comment

Since the total number of possibilities for the users_count counter is \(2^{10} = 1024\), achieving 100% toggle coverage across all states is not feasible. However, by excluding bits [4-9], the number of states to be covered is reduced, which allows us to achieve 100% toggle coverage for the remaining bits.