MARIAM MOHAMED MARZOUK

ASSIGNMENT_1_extended

Question 1

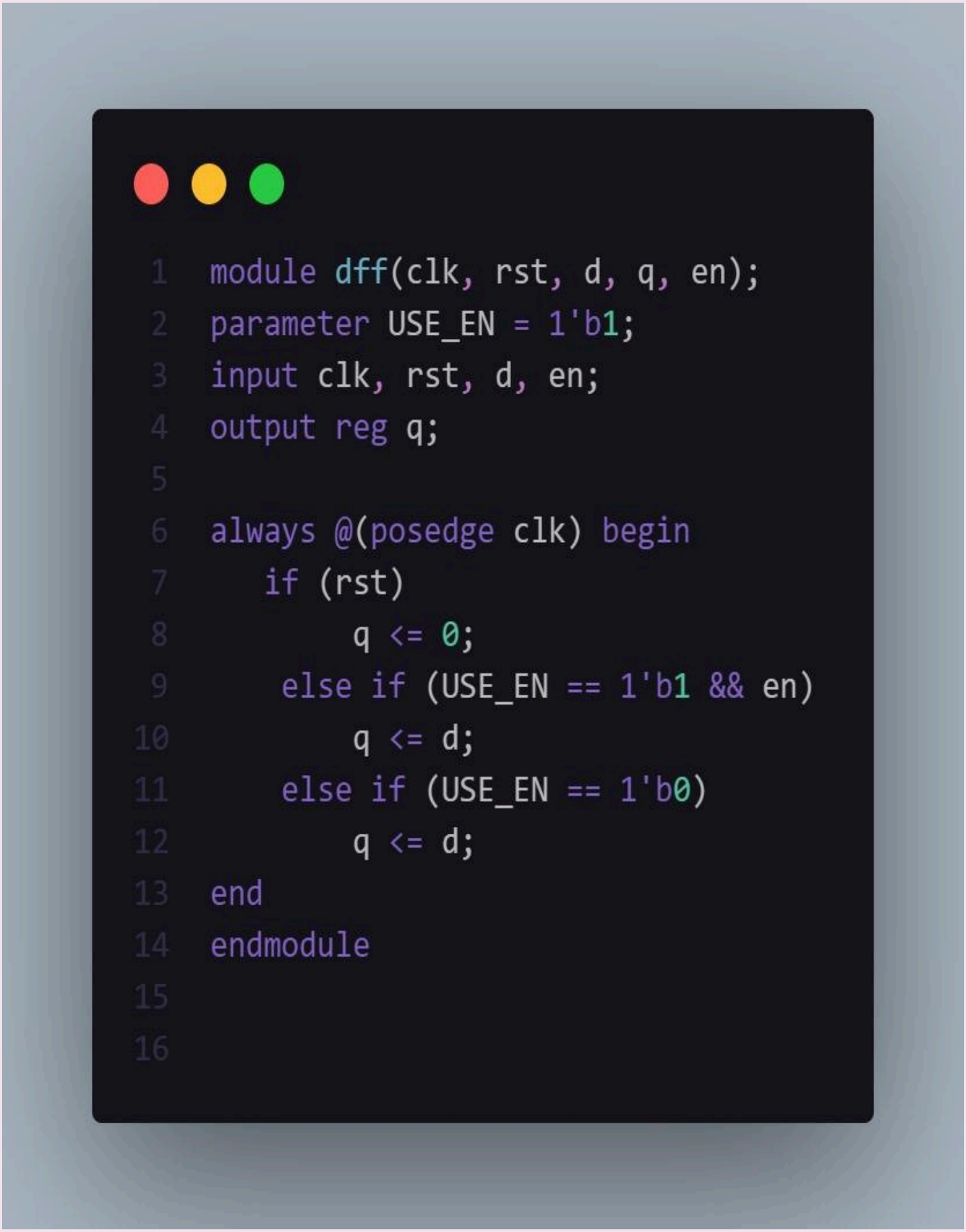
1)

Verify the functionality of the following D-FF:

- **Inputs:** clk, rst (active high sync), d, en
- **Outputs:** q
- **Parameters:** USE_EN (if equals 1 then use the enable to update the q output when the reset is deasserted, else ignore the en input)

Since the design has a parameter, we need to verify the functionality of both modes when the USE_EN equals 1 and zero.

I. RTL design



```
module dff(clk, rst, d, q, en);
parameter USE_EN = 1'b1;
input clk, rst, d, en;
output reg q;

always @(posedge clk) begin
   if (rst)
        q <= 0;
    else if (USE_EN == 1'b1 && en)
        q <= d;
    else if (USE_EN == 1'b0)
        q <= d;
end
endmodule
```

II. Test bench 1

```
module dff_tb_1;
parameter USE_EN = 0;
logic clk, rst, d, en, q, q_expected;
dff #(.USE_EN(USE_EN)) DUT1 (.clk(clk), .rst(rst), .d(d), .en(en), .q(q));
integer error_count; // 32-bit signed integer
integer correct_count; // 32-bit signed integer
// Clock generation
initial begin
    clk = 0;
    forever #25 clk = ~clk;
end
// Generate expected q
always @(posedge clk or posedge rst) begin
    if (rst)
        q_expected <= 0;
    else if (en || USE_EN == 0) // only update q_expected if en is high or USE_EN is 0
        q_expected <= d;
end
// Main testbench sequence
initial begin
    error_count = 0;
    correct_count = 0;
    d = 0; en = 0;
    check_reset;
    d = 0; en = 0; check_result(d);
    d = 1; en = 1; check_result(d);
    d = 0; en = 1; check_result(d);
    d = 1; en = 0; check_result(d);
    check_reset;
    $display ("%0t: At the end of the test, error count = %0d and correct count = %0d", $time, error_count, correct_count);
    $stop;
end
// Task to check the result
task check_result(input logic expected_result);
    @(negedge clk);
    if (q !== expected_result) begin
        error_count = error_count + 1;
        $display("%0t: Error: For D = %0b and en = %0d, q should be %0b but is %0b", $time, d, en, expected_result, q);
    end else begin
        correct_count = correct_count + 1;
    end
endtask
// Task to check reset behavior
task check_reset();
    // Assert reset
    rst = 1;
    @(negedge clk);
    if (q !== 0) begin
        error_count = error_count + 1;
        $display("%0t: Error: Reset asserted, but q is not 0", $time);
    end else begin
        correct_count = correct_count + 1;
    end
    // Deassert reset
    rst = 0;
endtask
endmodule
```

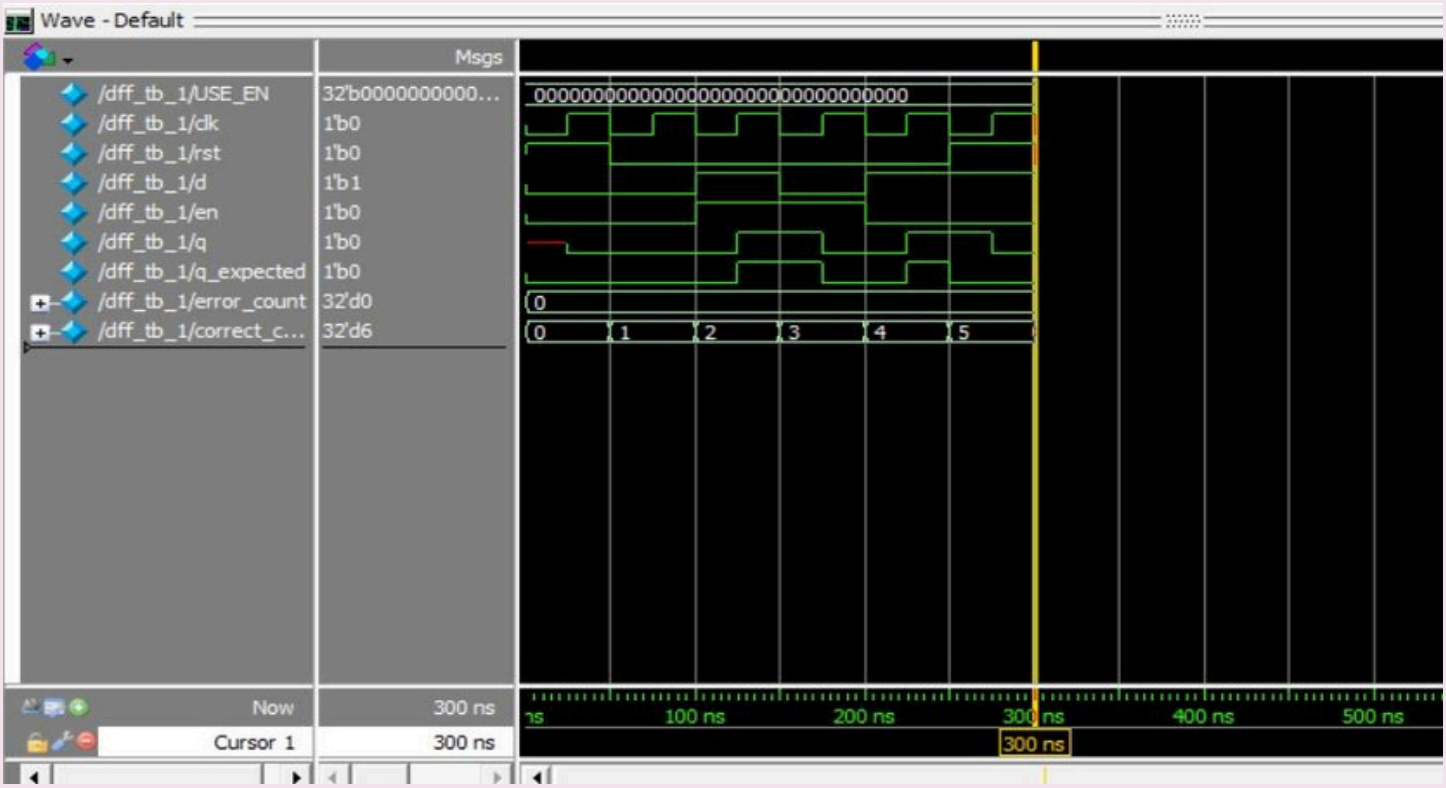
III. Counter

```
# 300: At the end of the test, error count = 0 and correct count = 6
```

IV. Do File

```
vlib work
vlog dff.v dff_tb_1.sv  +cover -covercells
vsim -voptargs=+acc work.dff_tb_1 -cover
add wave *
coverage save dff_tb_1.ucdb -onexit -du work.dff
run -all
```

V. Waveform



VI. Coverage Report

```
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         2         2         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\dff_tb_1#DUT1

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File dff.v
-----------------------------------IF Branch-----------------------------------
    7                                          6     Count coming in to IF
    7              1                           2
    9              1                           4
Branch totals: 2 hits of 2 branches = 100.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       3         3         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\dff_tb_1#DUT1  --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File dff.v
    6              1                           6
    8              1                           2
    12             1                           4
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         10        10         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\dff_tb_1#DUT1  --

                                     Node      1H->0L      0L->1H  "Coverage"
                                     ----------------------------------------
                                      clk           1           1     100.00
                                        d           1           1     100.00
                                       en           1           1     100.00
                                        q           1           1     100.00
                                      rst           1           1     100.00

Total Node Count     =          5
Toggled Node Count   =          5
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (10 of 10 bins)

Total Coverage By Instance (filtered view): 100.00%
```

I. Test Bench 2

```
module dff_tb_2;
parameter USE_EN = 1;
logic clk, rst, d, en, q, q_expected;
dff #(.USE_EN(USE_EN)) DUT2 (.clk(clk), .rst(rst), .d(d), .en(en), .q(q));
integer error_count; // 32-bit signed integer
integer correct_count; // 32-bit signed integer
// Clock generation
initial begin
    clk = 0;
    forever #25 clk = ~clk;
end
// Generate expected q
always @(posedge clk or posedge rst) begin
    if (rst)
        q_expected <= 0;
    else if (USE_EN && en)
        q_expected <= d;
    // Do not change q_expected if en is low
end
// Main testbench sequence
initial begin
    error_count = 0;
    correct_count = 0;
    d = 0; en = 0;
    // Test reset
    check_reset;
    // Test cases for USE_EN = 1
    d = 0; en = 0; #50; check_result(q_expected); // Initial value with en = 0
    d = 1; en = 1; #50; check_result(q_expected); // Update d with en = 1
    d = 0; en = 1; #50; check_result(q_expected); // Update d with en = 1
    d = 1; en = 0; #50; check_result(q_expected); // Check with en = 0
    // Check reset again
    check_reset;
    $display("%0t: At the end of the test, error count = %0d and correct count = %0d", $time, error_count, correct_count);
    $stop;
end
```

```
// Task to check the result
task check_result(input logic expected_result);
    @(negedge clk);  // Wait for a clock edge
    #1;              // Small delay to allow for settling
    if (q !== expected_result) begin
        error_count = error_count + 1;
        $display("%0t: Error: For D = %0b and en = %0d, q should be %0b but is %0b", $time, d, en, expected_result, q);
    end else begin
        correct_count = correct_count + 1;
    end
endtask
// Task to check reset behavior
task check_reset();
    // Assert reset
    rst = 1;
    @(negedge clk);  // Wait for clock edge to see reset effect
    #1;              // Small delay to allow for settling
    if (q !== 0) begin
        error_count = error_count + 1;
        $display("%0t: Error: Reset asserted, but q is not 0", $time);
    end else begin
        correct_count = correct_count + 1;
    end
    // Deassert reset
    rst = 0;
endtask
endmodule
```

II. Counter

```
# 501: At the end of the test, error count = 0 and correct count = 6
```

III. Do File

```
vlib work
vlog dff.v dff_tb_2.sv  +cover -covercells
vsim -voptargs=+acc work.dff_tb_2 -cover
add wave *
coverage save dff_tb_2.ucdb -onexit -du work.dff
run -all
```

IV. Waveform

V. Coverage Report

```
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         3         3         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\dff_tb_2#DUT2

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File dff.v
------------------------------------IF Branch------------------------------------
    7                                        8     Count coming in to IF
    7              1                         2
    9              1                         4
    11             1                         2
Branch totals: 3 hits of 3 branches = 100.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       3         3         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\dff_tb_2#DUT2  --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File dff.v
    6              1                         8
    8              1                         2
    10             1                         4
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         10        10         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\dff_tb_2#DUT2  --

                                    Node      1H->0L      0L->1H  "Coverage"
                                    ----------------------------------------
                                     clk           1           1      100.00
                                       d           1           1      100.00
                                      en           1           1      100.00
                                       q           1           1      100.00
                                     rst           1           1      100.00

Total Node Count     =          5
Toggled Node Count   =          5
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (10 of 10 bins)
Total Coverage By Instance (filtered view): 100.00%
```

V. Merged Coverage Report

```
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         2         2         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\work.dff

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File dff.v
-----------------------------------IF Branch-----------------------------------
    7                                          6     Count coming in to IF
    7              1                           2
    9              1                           4
Branch totals: 2 hits of 2 branches = 100.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       3         3         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\work.dff  --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File dff.v
    6              1                           6
    8              1                           2
    12             1                           4
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         10        10         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\work.dff  --

                                          Node      1H->0L      0L->1H  "Coverage"
                                          ----------------------------------------
                                           clk           2           2      100.00
                                             d           2           2      100.00
                                            en           2           2      100.00
                                             q           2           2      100.00
                                           rst           2           2      100.00

Total Node Count     =          5
Toggled Node Count   =          5
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (10 of 10 bins)


Total Coverage By Instance (filtered view): 100.00%
```