Misr University for Science and Technology
Faculty of Engineering
Electronics and communication department

ECE 462 Project (Electronics V)

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RISC-V Principle:

1)Open Source: RISC-V is open-source, meaning anyone can access, modify, and implement it without needing to pay royalties. This fosters collaboration, innovation, and avoids vendor lock-in.

2)Modularity: RISC-V's modular design allows for customization and optimization for specific tasks or applications. Developers can choose and implement only the instructions they need, which can lead to more efficient and tailored designs.

3)Scalability: RISC-V supports various implementations, from tiny microcontrollers to high-performance server processors. This scalability makes it suitable for a wide range of devices and applications.

4)Community Support: RISC-V has a growing community of developers, researchers, and companies contributing to its ecosystem. This support ensures continuous improvement, updates, and a rich set of tools and resources.

5)Flexibility: RISC-V's design allows for easy adaptation to new technologies and requirements. This flexibility makes it suitable for emerging trends like Internet of Things (IoT), artificial intelligence (AI), and edge computing.

6)Reduced Complexity: Compared to complex instruction set computing (CISC) architectures, RISC-V's simplified instruction set makes it easier to design, optimize, and debug hardware and software.

7)Education: RISC-V's open nature and simplicity make it an excellent platform for educational purposes, allowing students and researchers to gain insights into computer architecture and design.

Architecture:

1)RISC Principles: RISC-V follows the principles of Reduced Instruction Set Computing (RISC), emphasizing simplicity, efficiency, and regularity in instruction set design.

2)Instruction Set: RISC-V defines a base integer instruction set (RV32I, RV64I, RV128I) along with optional extensions for floating-point operations (F), atomic operations (A), multiplication and division (M), and more.

3)Privileged Architecture: RISC-V defines a privileged architecture with supervisor, hypervisor, and machine-level privilege modes, allowing for secure and efficient execution of operating systems and virtualization.

Ecosystem:

1)Tools: There's a growing ecosystem of compilers, assemblers, debuggers, simulators, and profiling tools for RISC-V, including GCC, LLVM, QEMU, Spike, and more.

2)Operating Systems: RISC-V supports various operating systems including Linux, FreeBSD, and embedded real-time operating systems (RTOS) like Free RTOS and Zephyr.

3)Development Boards: Several RISC-V development boards are available, such as SiFive HiFive, Kendryte K210, and BeagleV, enabling developers to prototype and test RISC-V designs.

Implementation:

1)Core Designs: Companies like SiFive, Andes Technology, and Western Digital offer RISC-V core designs ranging from simple microcontrollers to high-performance application processors.

2)Customization: RISC-V's modular design allows for customization of core features and extensions based on specific application requirements, leading to more efficient and tailored designs.

3)Fabrication: RISC-V cores can be implemented in various fabrication processes, including ASIC (Application-Specific Integrated Circuit) and FPGA (Field-Programmable Gate Array), providing flexibility in hardware development. (Xc7a35ticp)

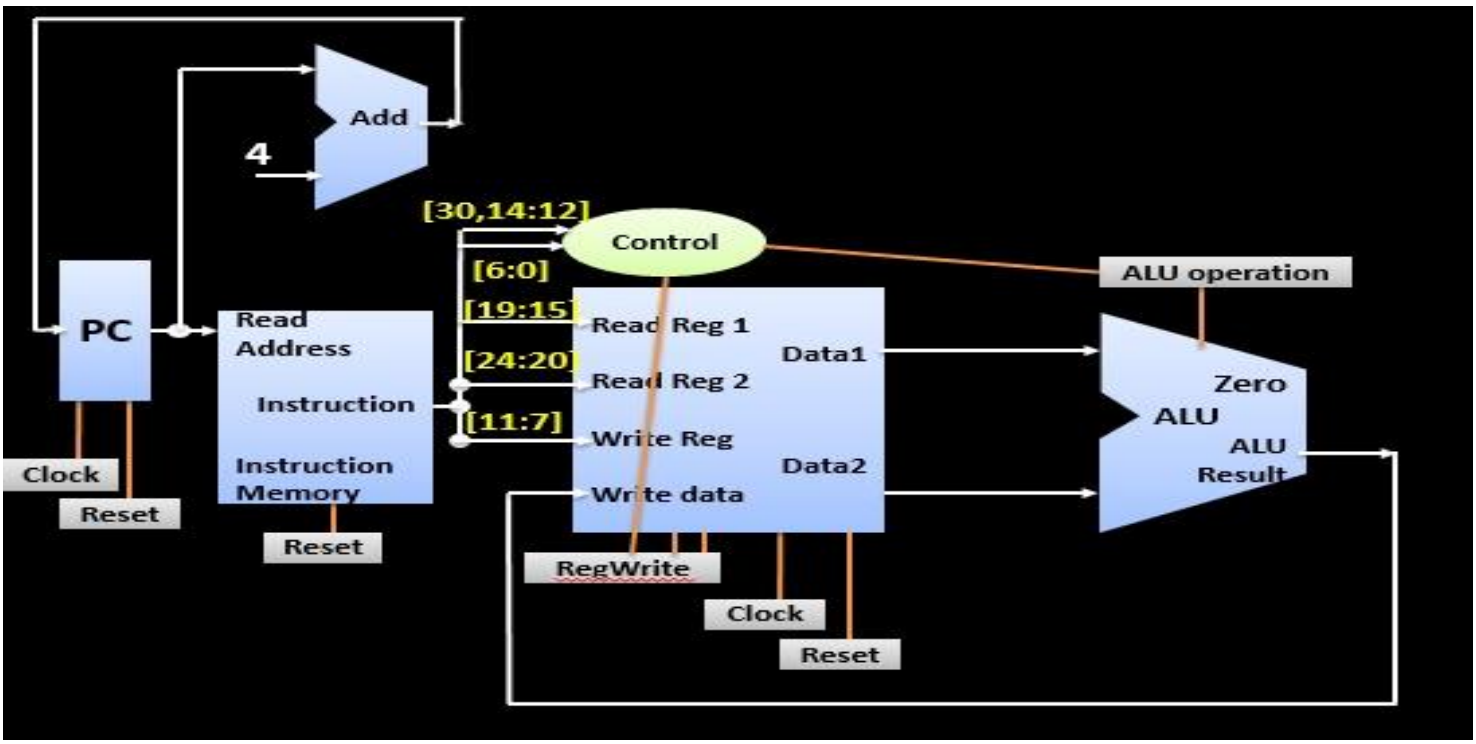
Applications:

1)Embedded Systems: RISC-V is well-suited for embedded systems due to its low-power design, customizable features, and support for real-time operations.

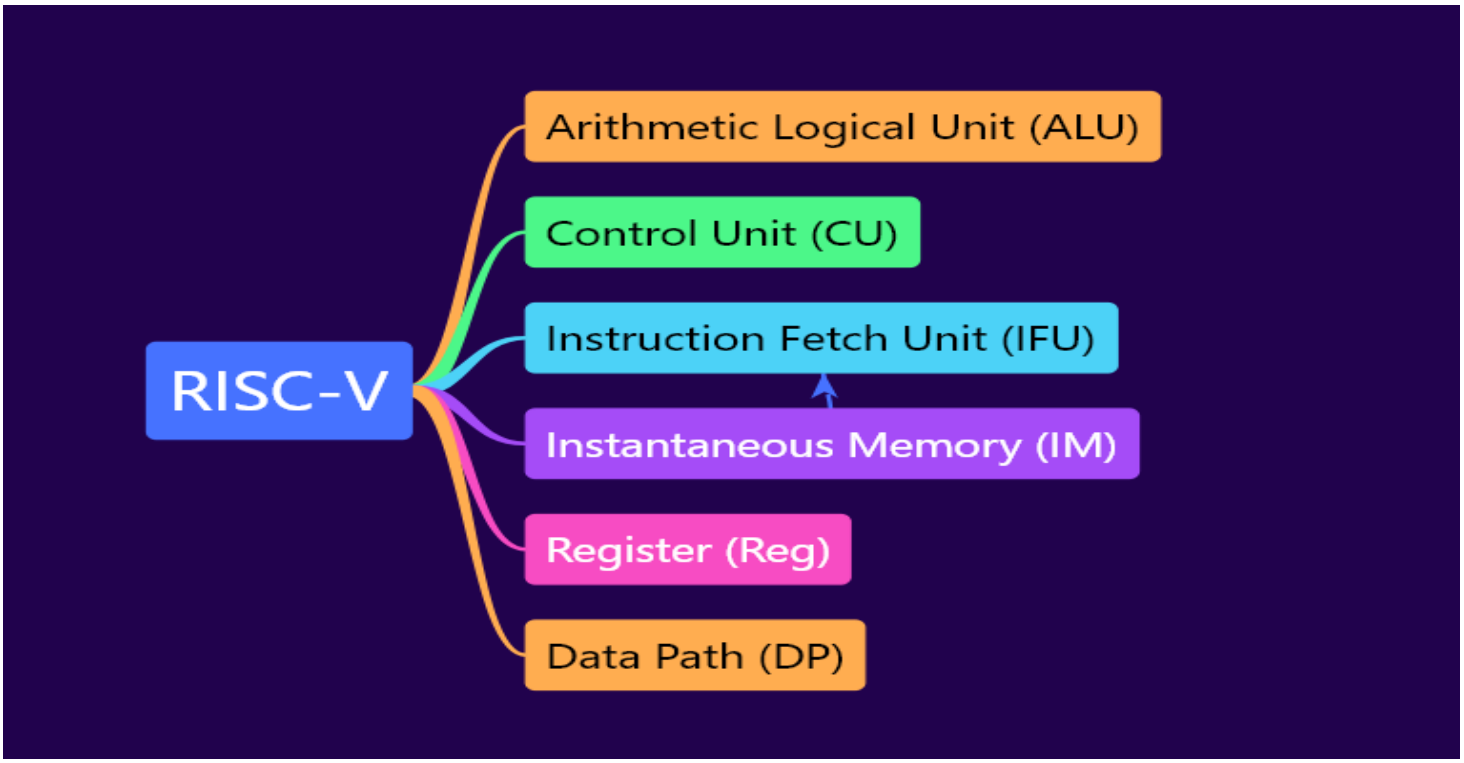
2)IoT Devices: The scalability and modularity of RISC-V make it suitable for IoT devices, enabling efficient processing and connectivity in edge devices.

3)High-Performance Computing: RISC-V is gaining traction in high-performance computing (HPC) and data centers, offering energy-efficient processing and potential cost savings.

RISC-V Block Diagram:

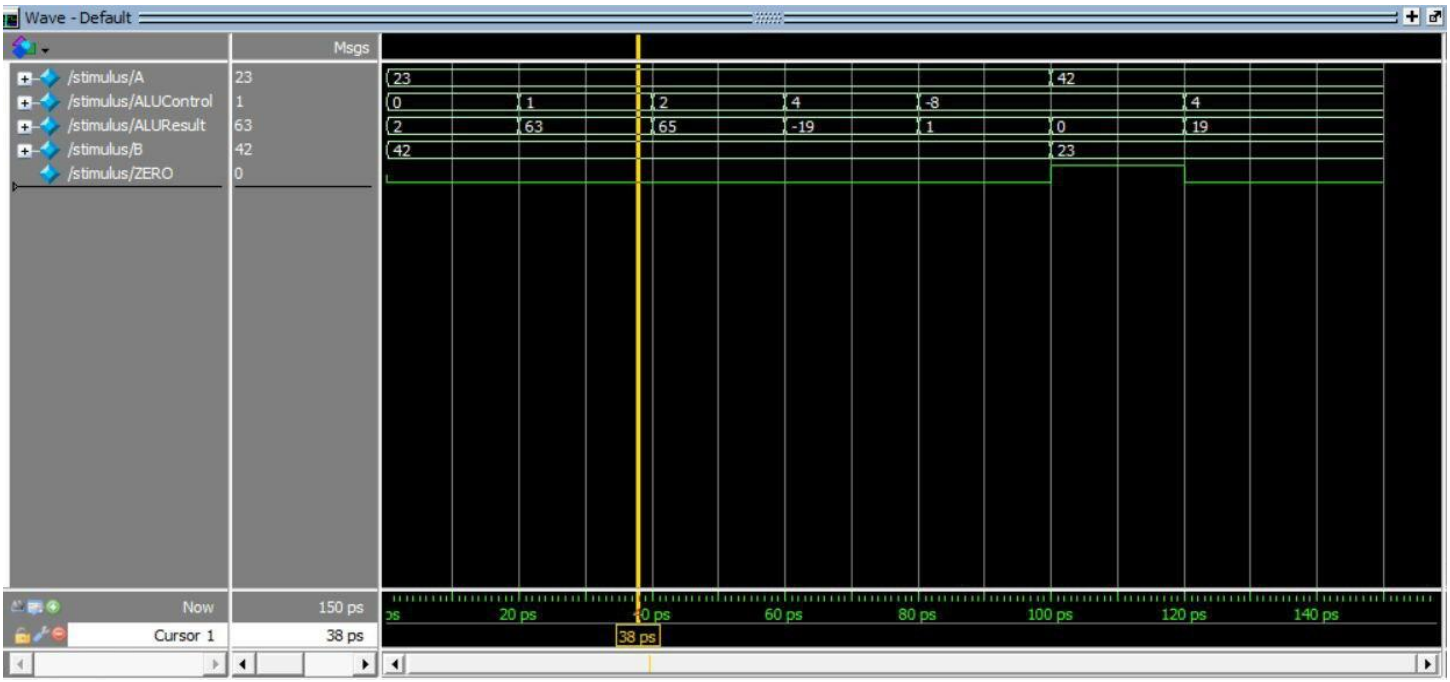


Embedded Blocks:

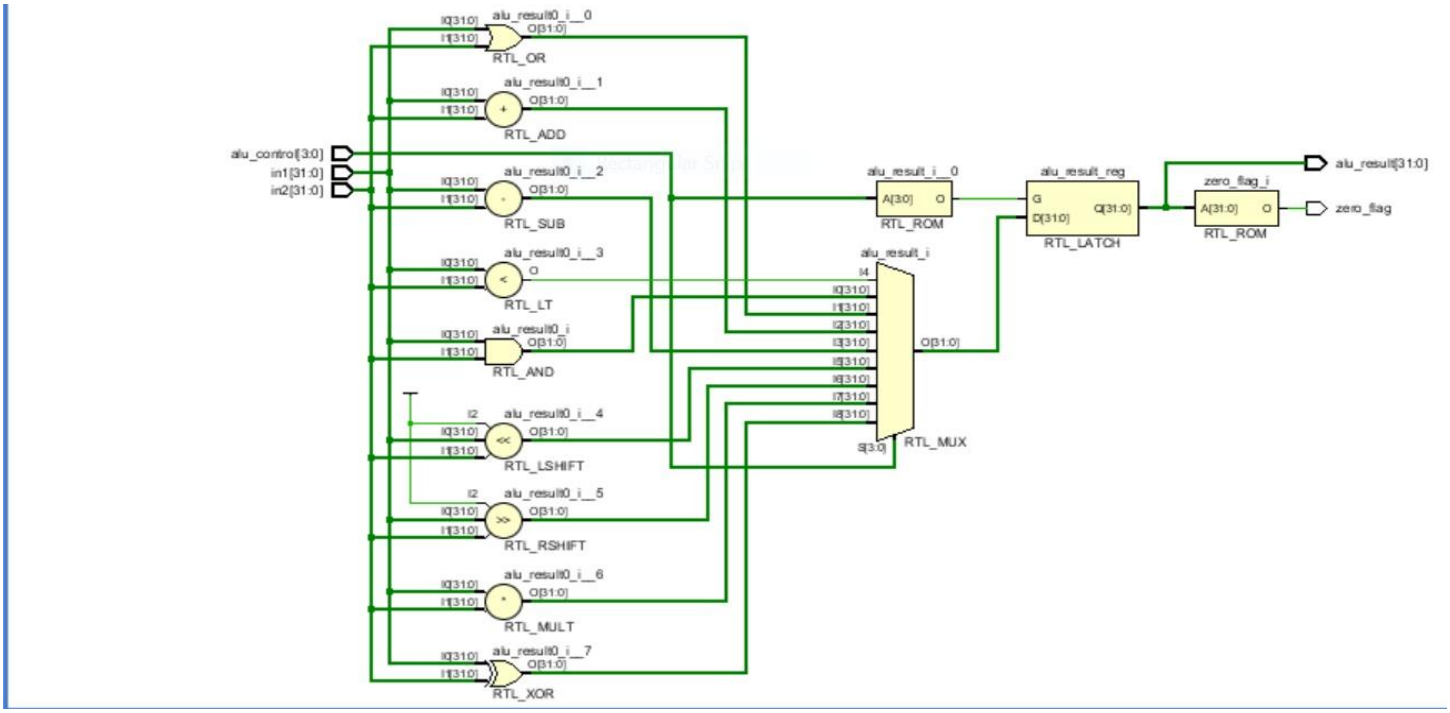


Arithmetic Logical Unit (ALU)

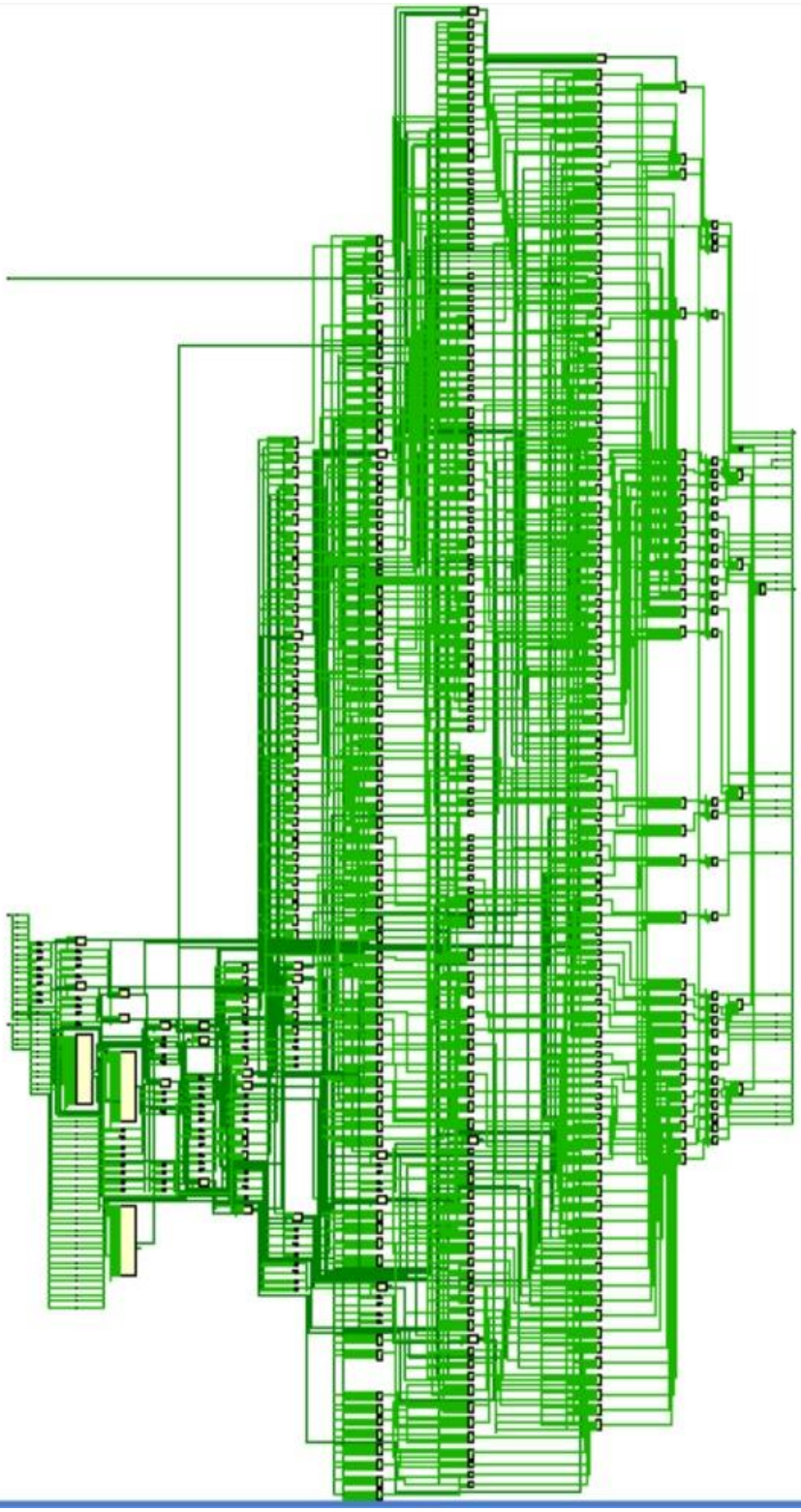
Timing Diagram:



RTL Schematic:



Synthesis Design:



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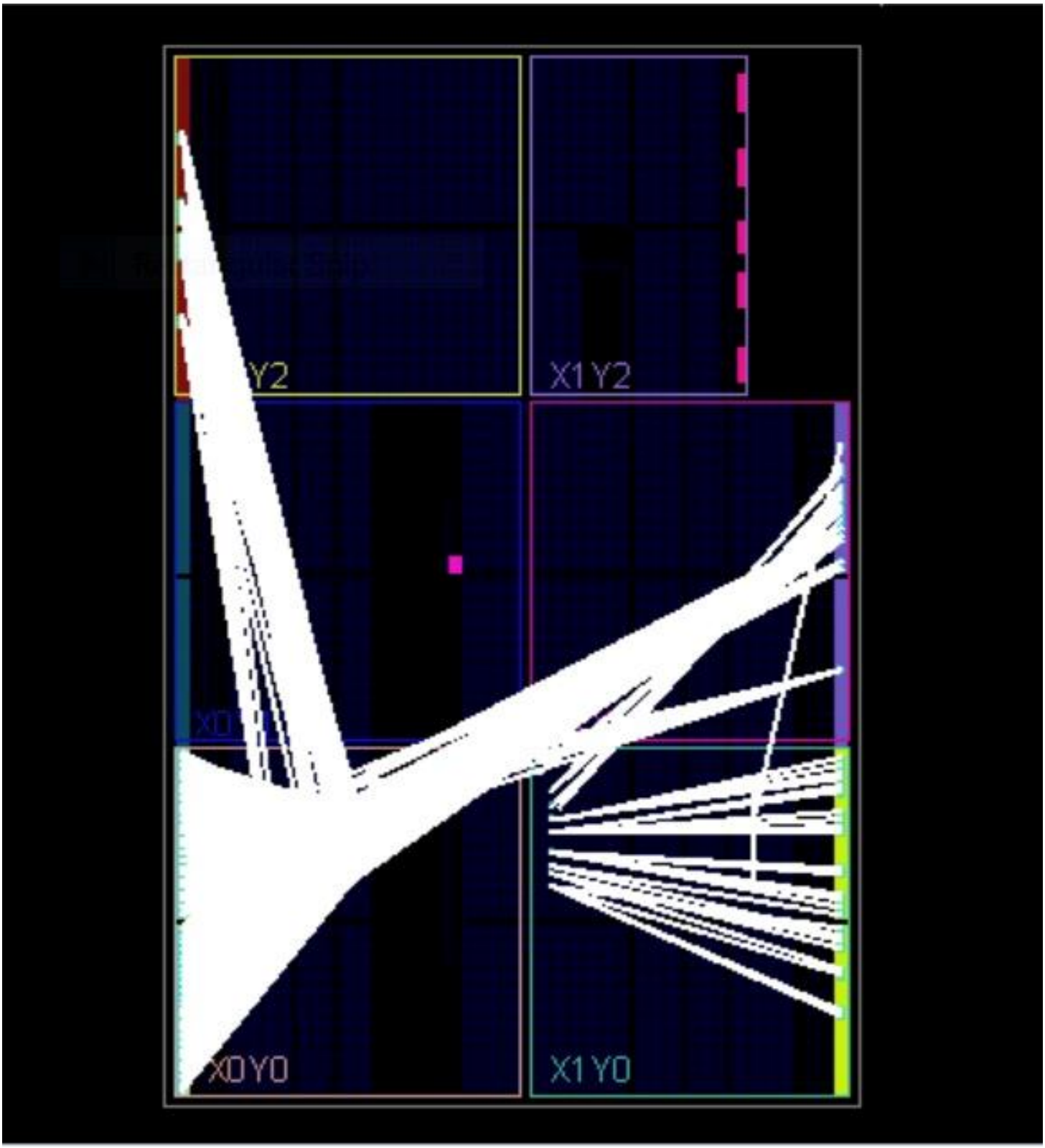
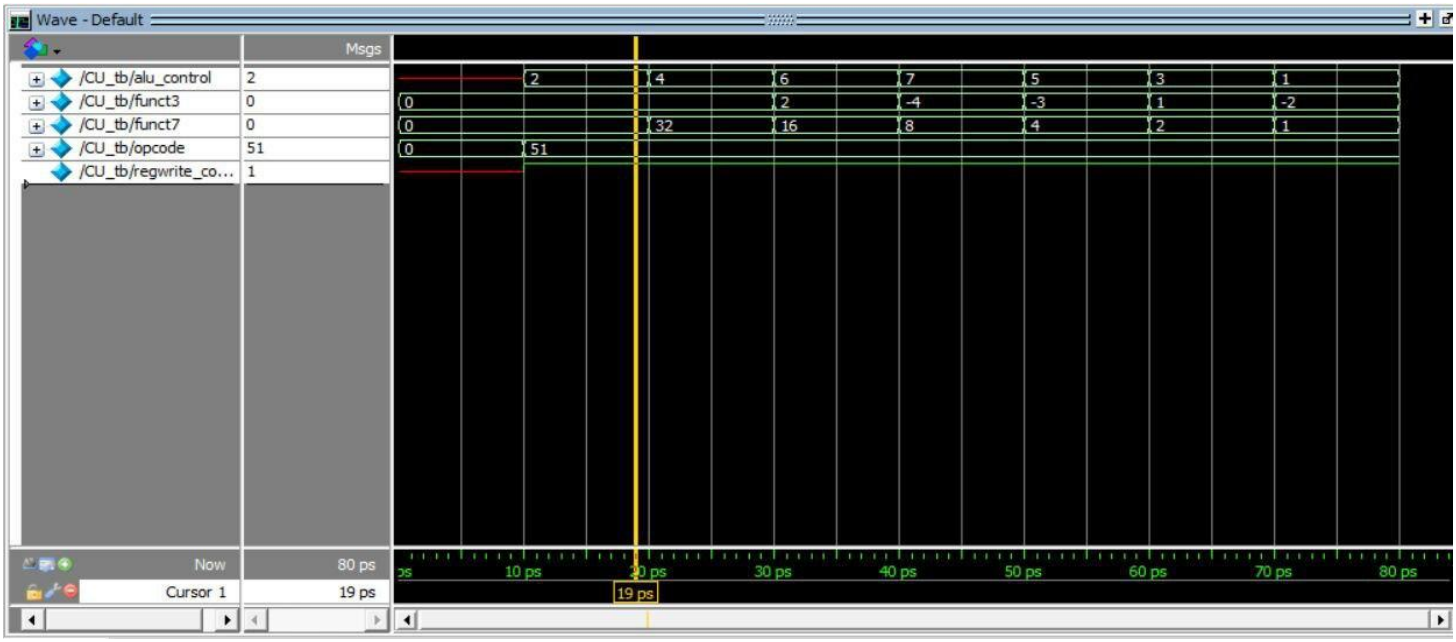


Control Unit (CU)

Timing Diagram:



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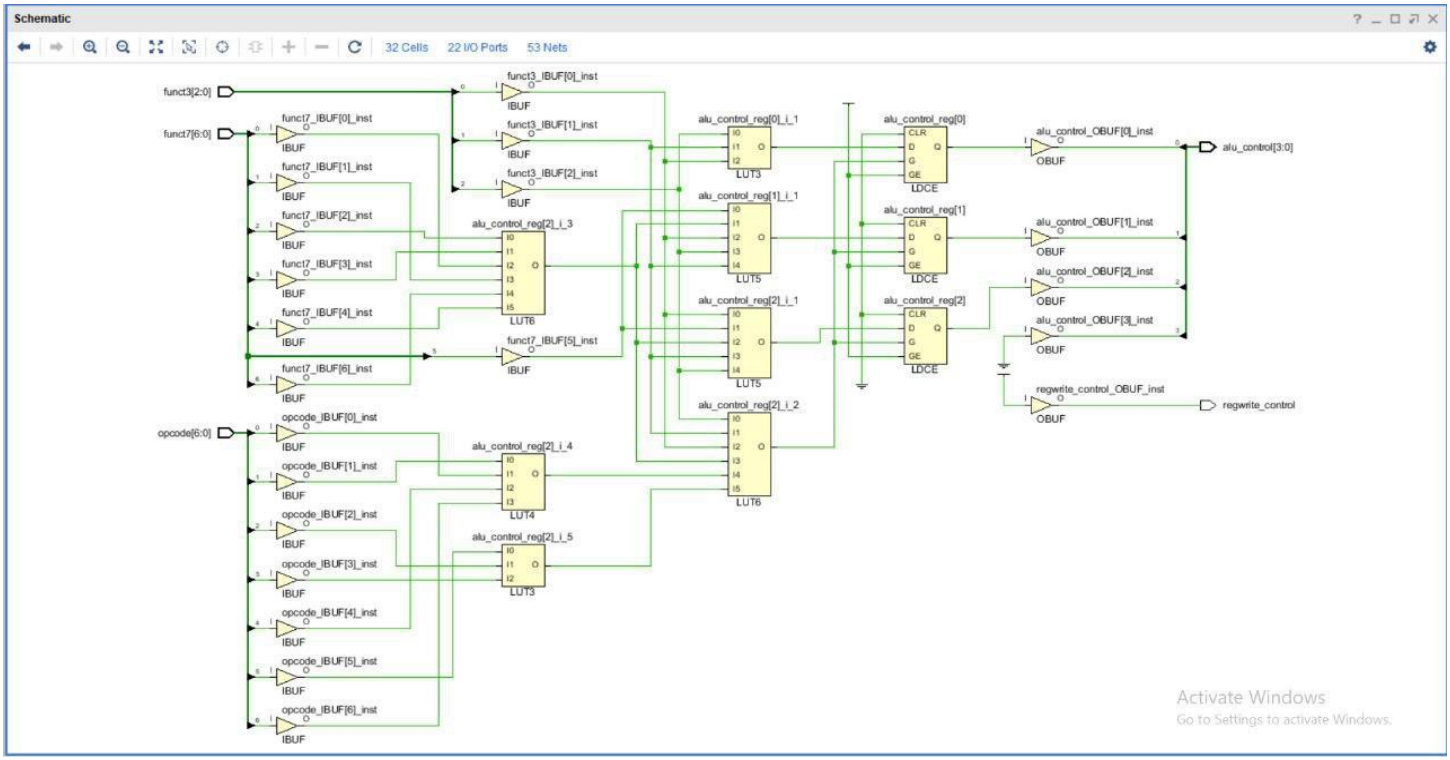

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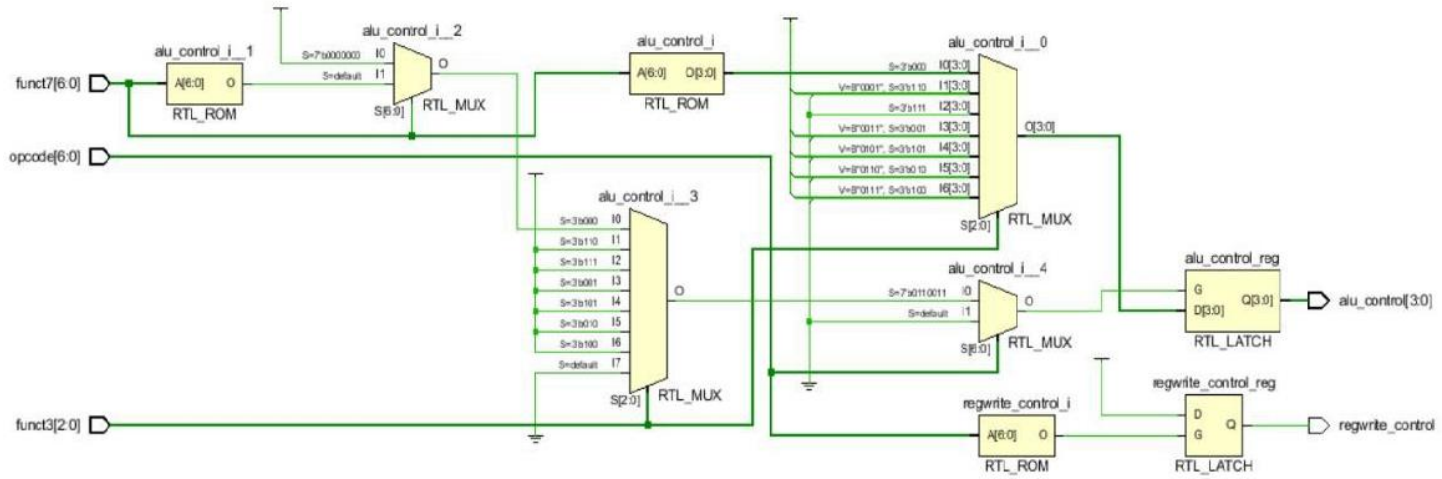

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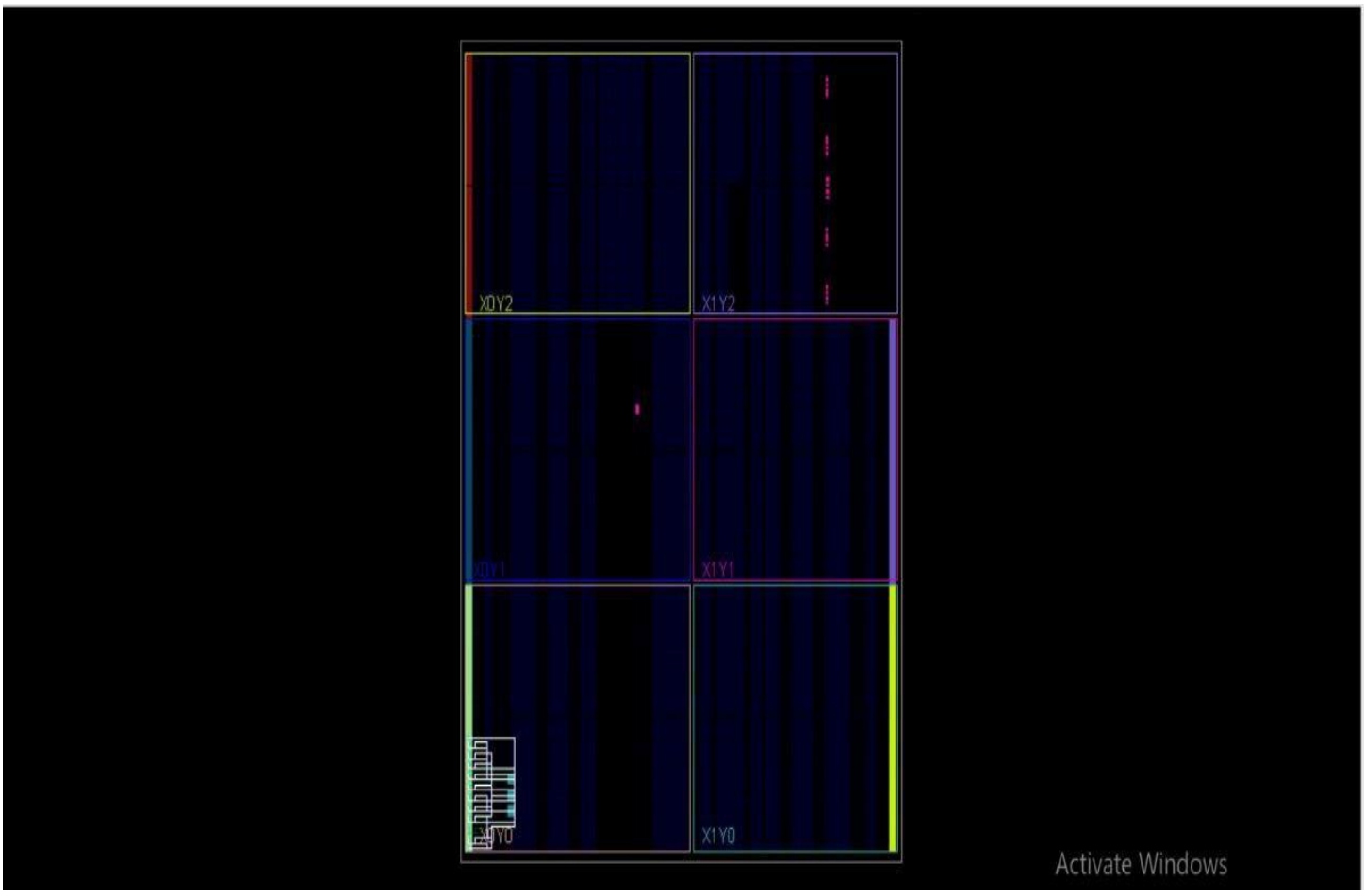
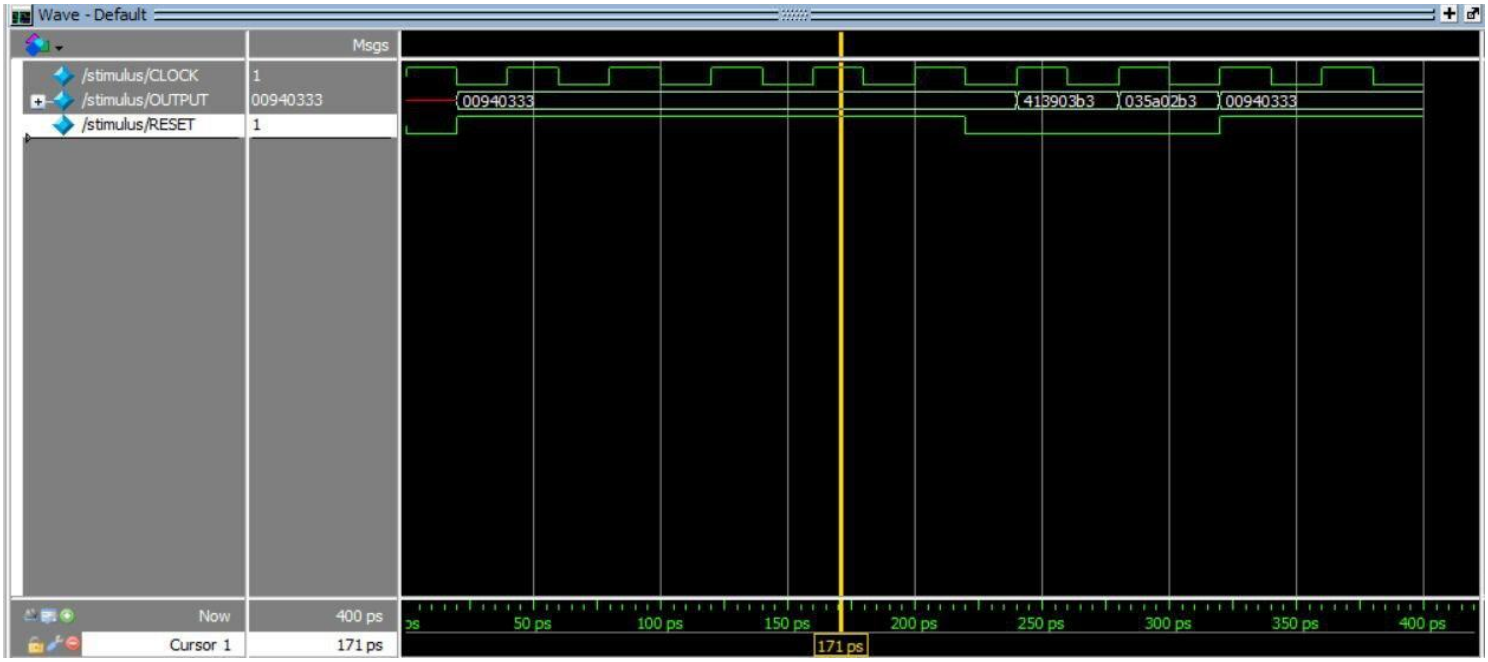


Instruction Fetch Unit (IFU) Instantaneous Memory (IM)

Timing Diagram:



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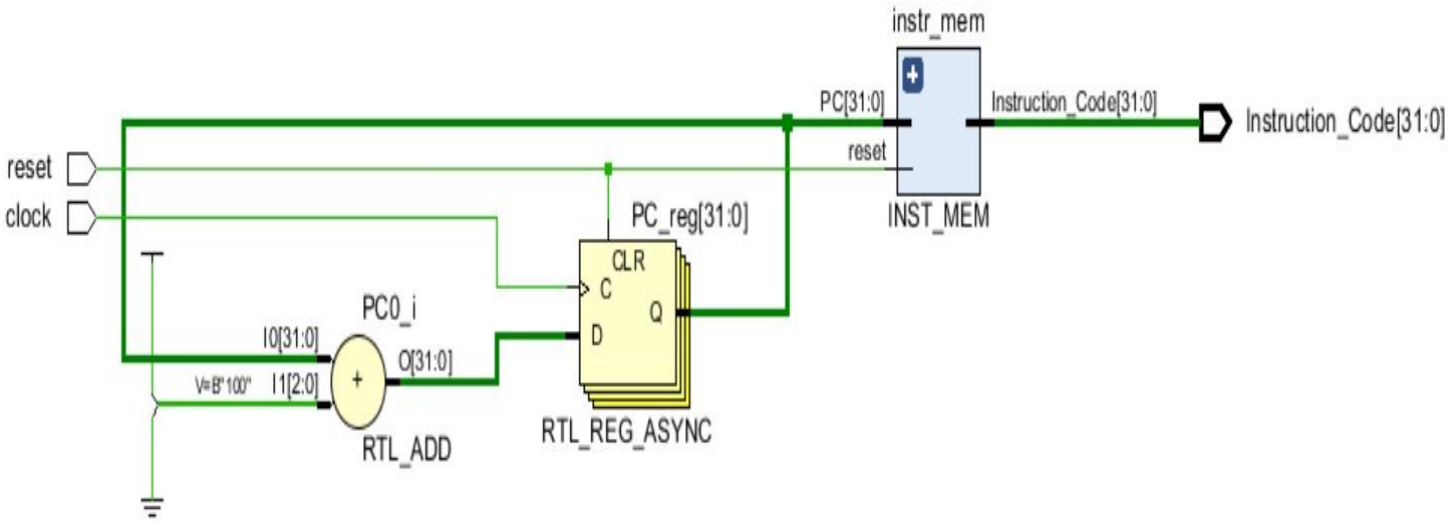

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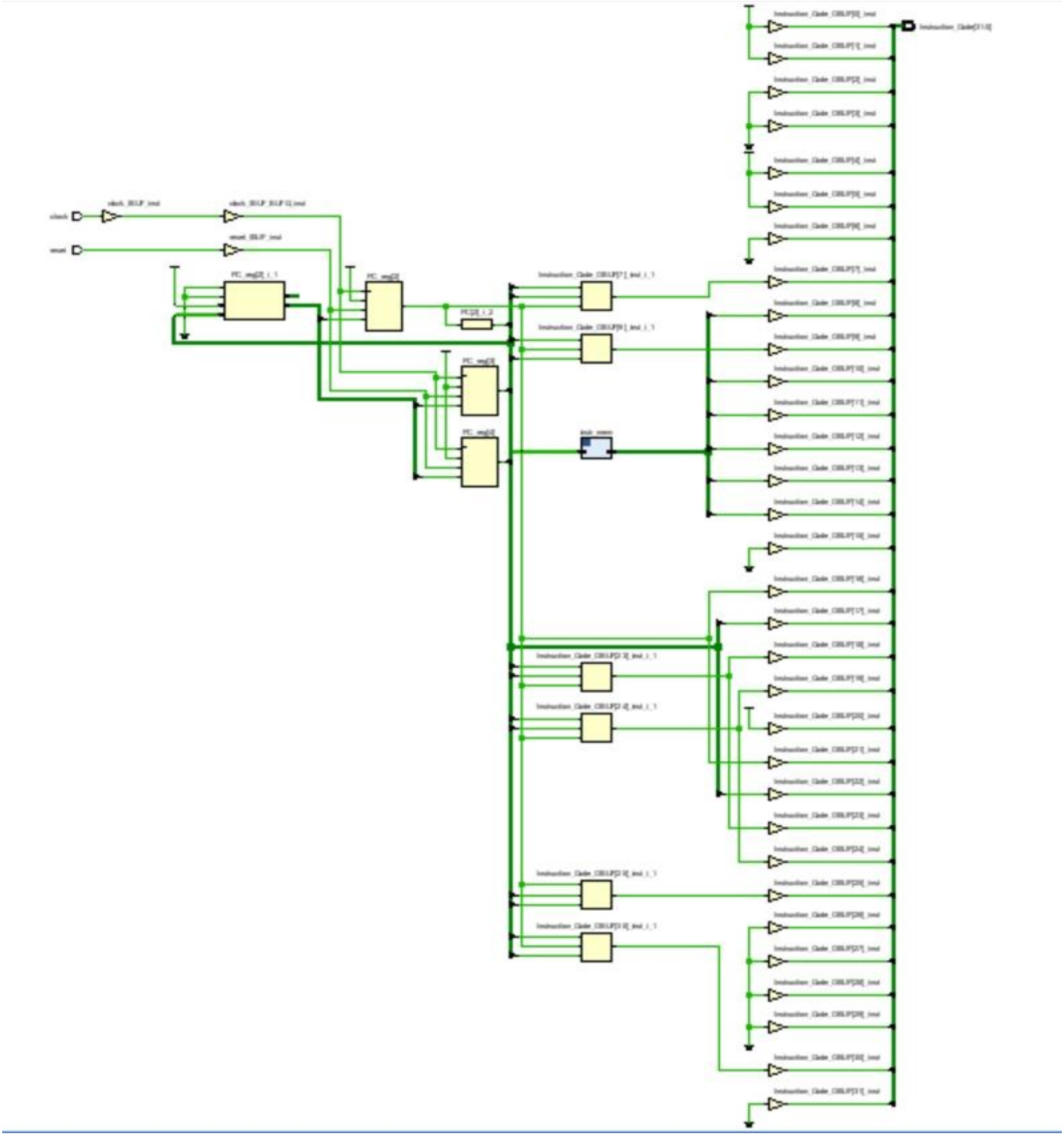

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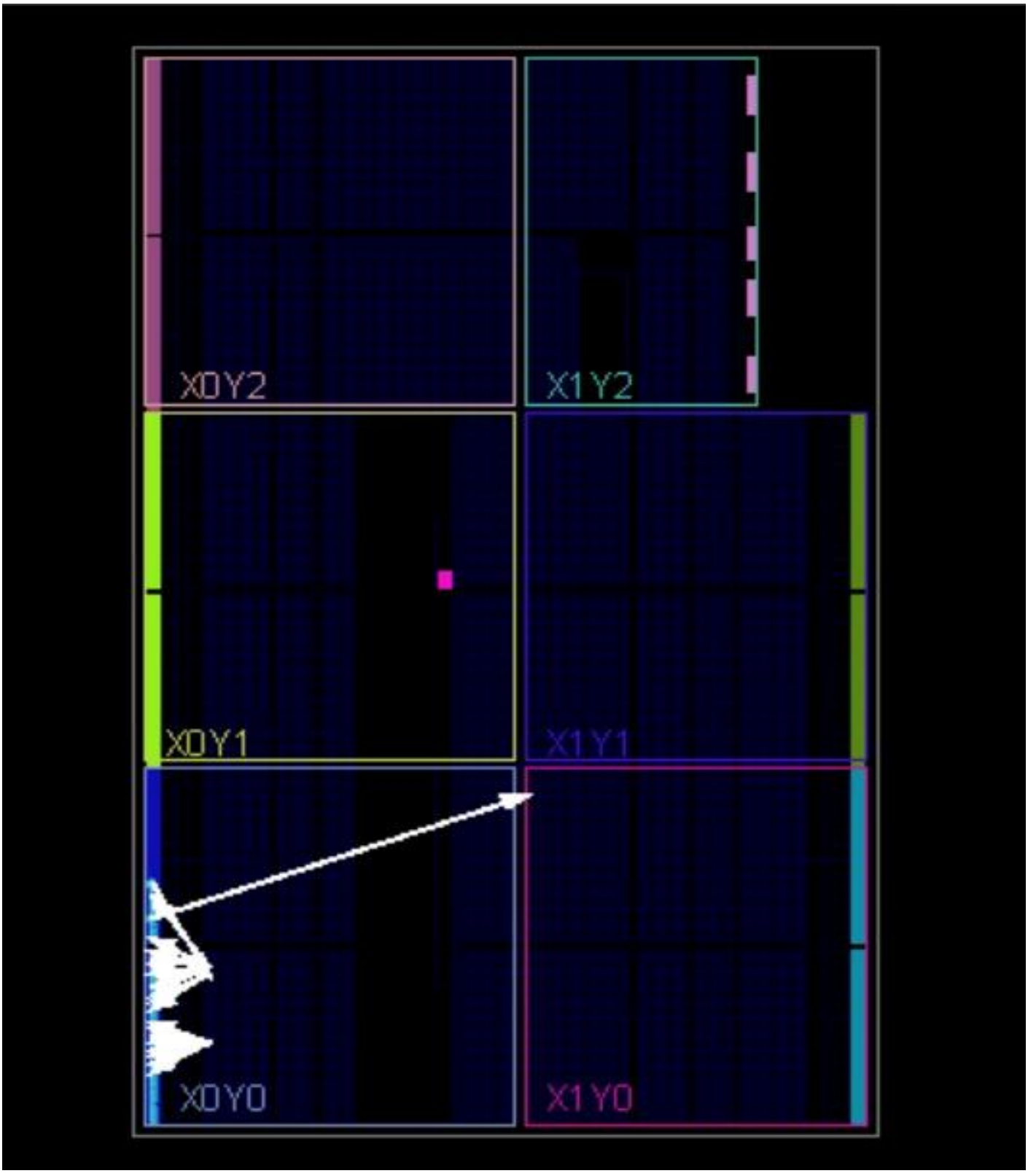
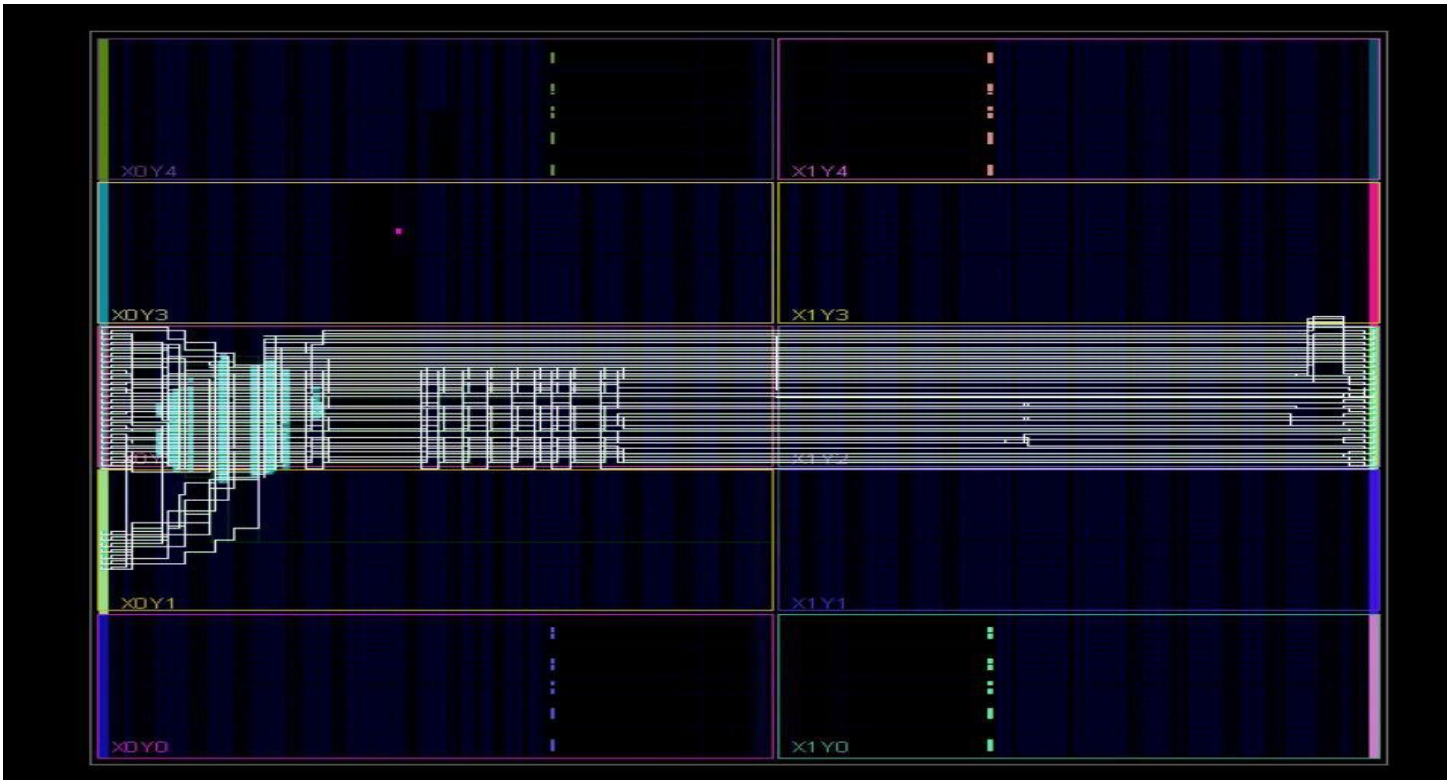


Register (Reg)

Timing Diagram:

Implemented Device:



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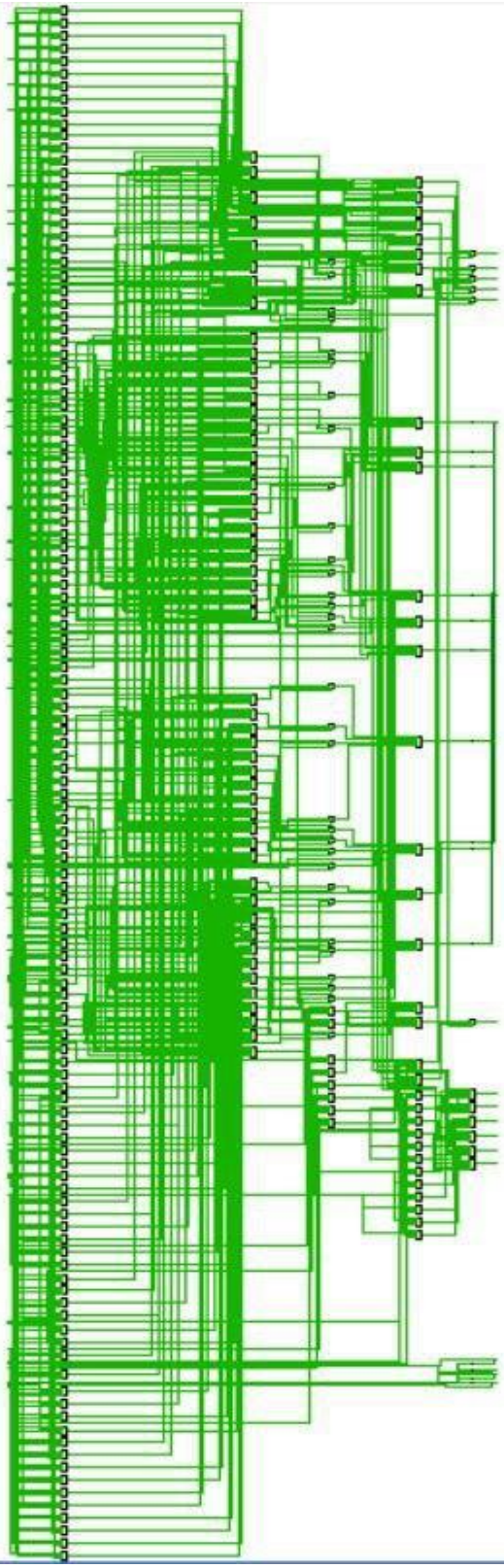

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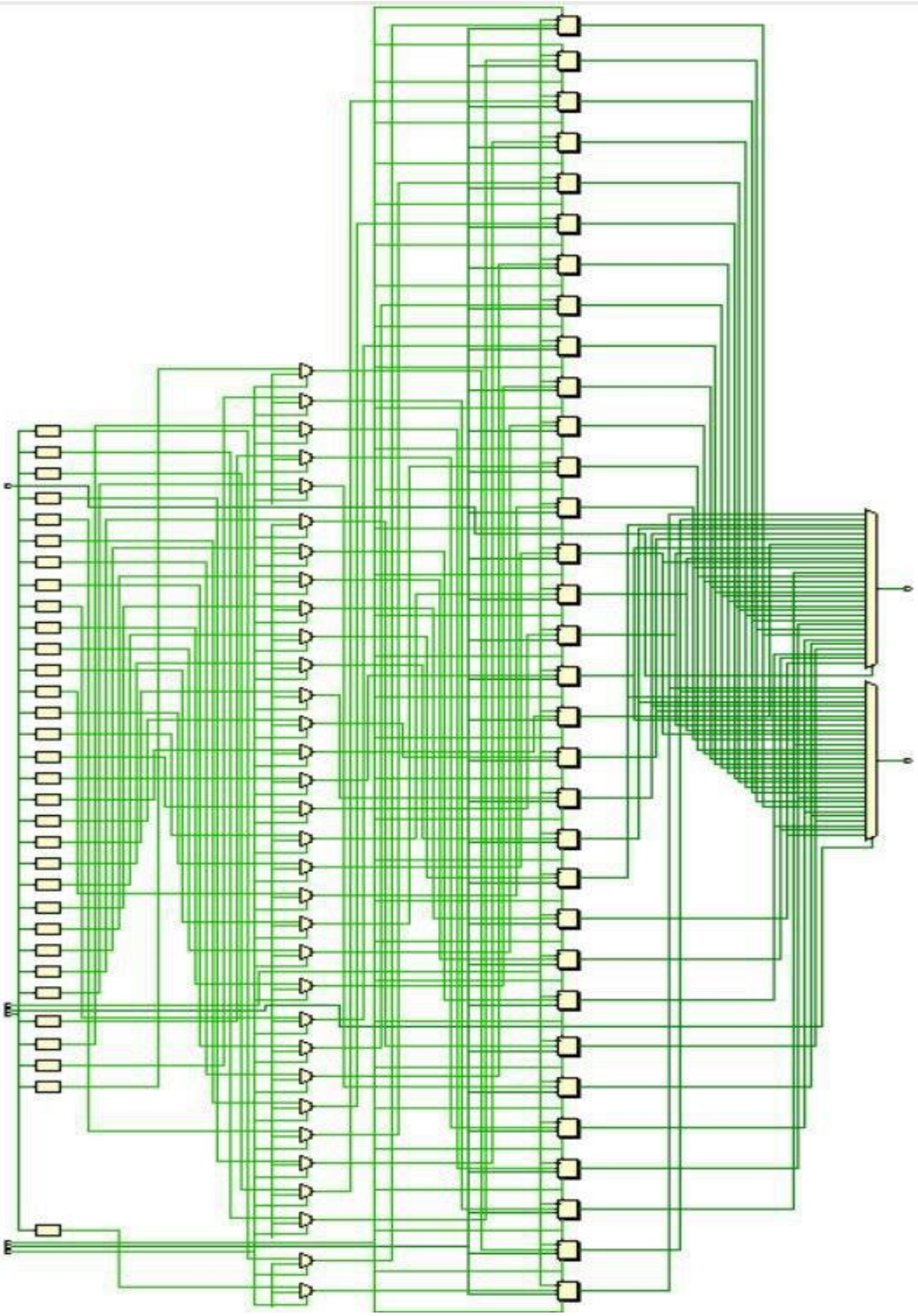
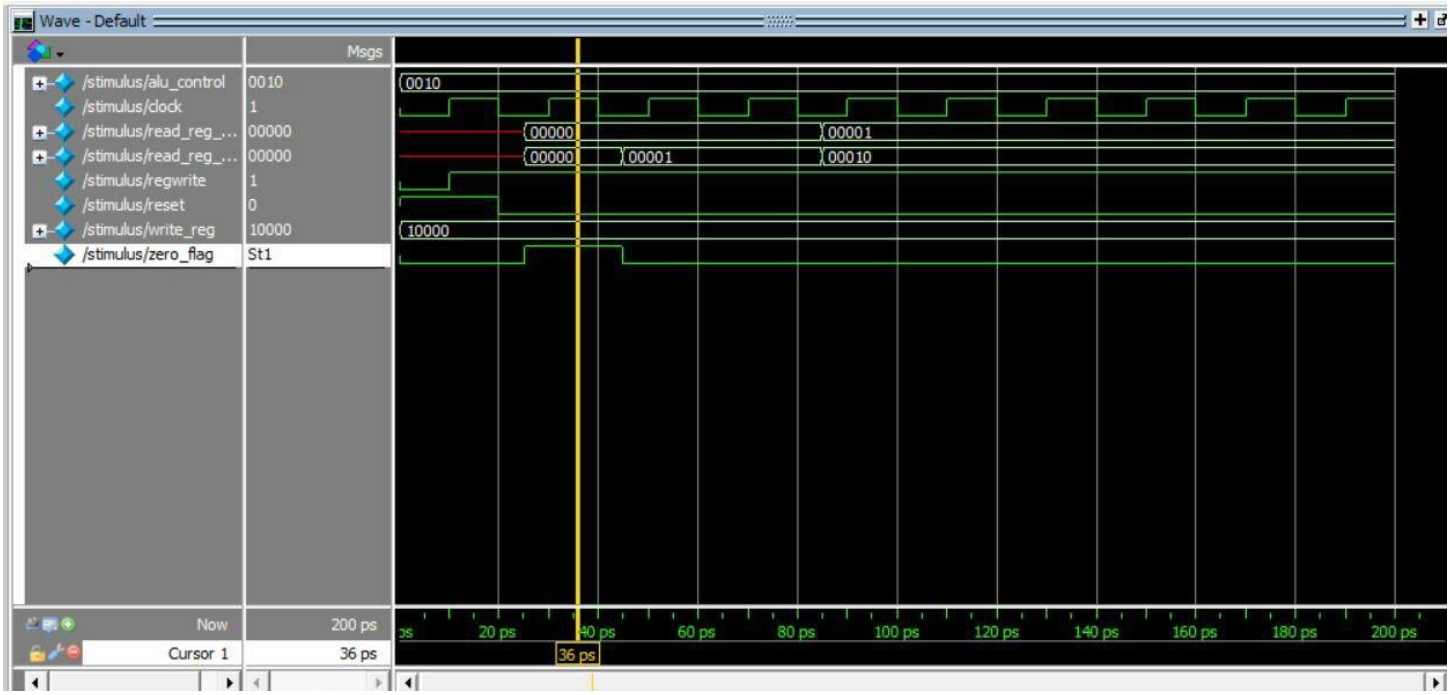


Data Path (DP)

Timing Diagram:



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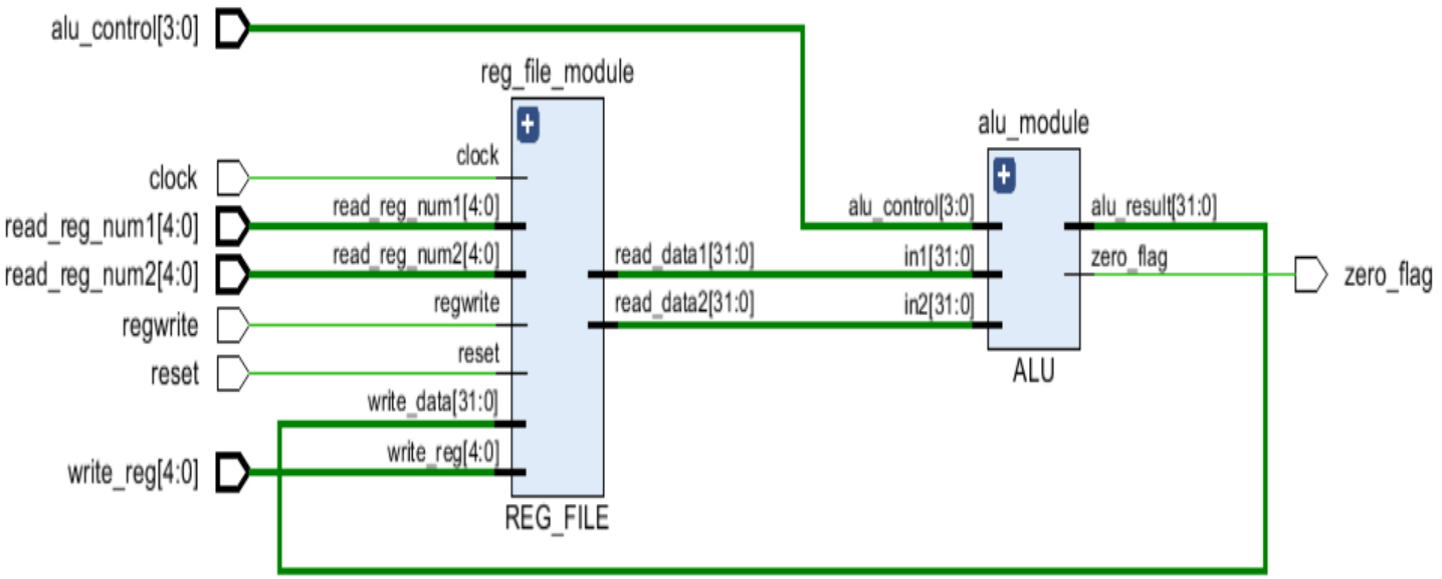

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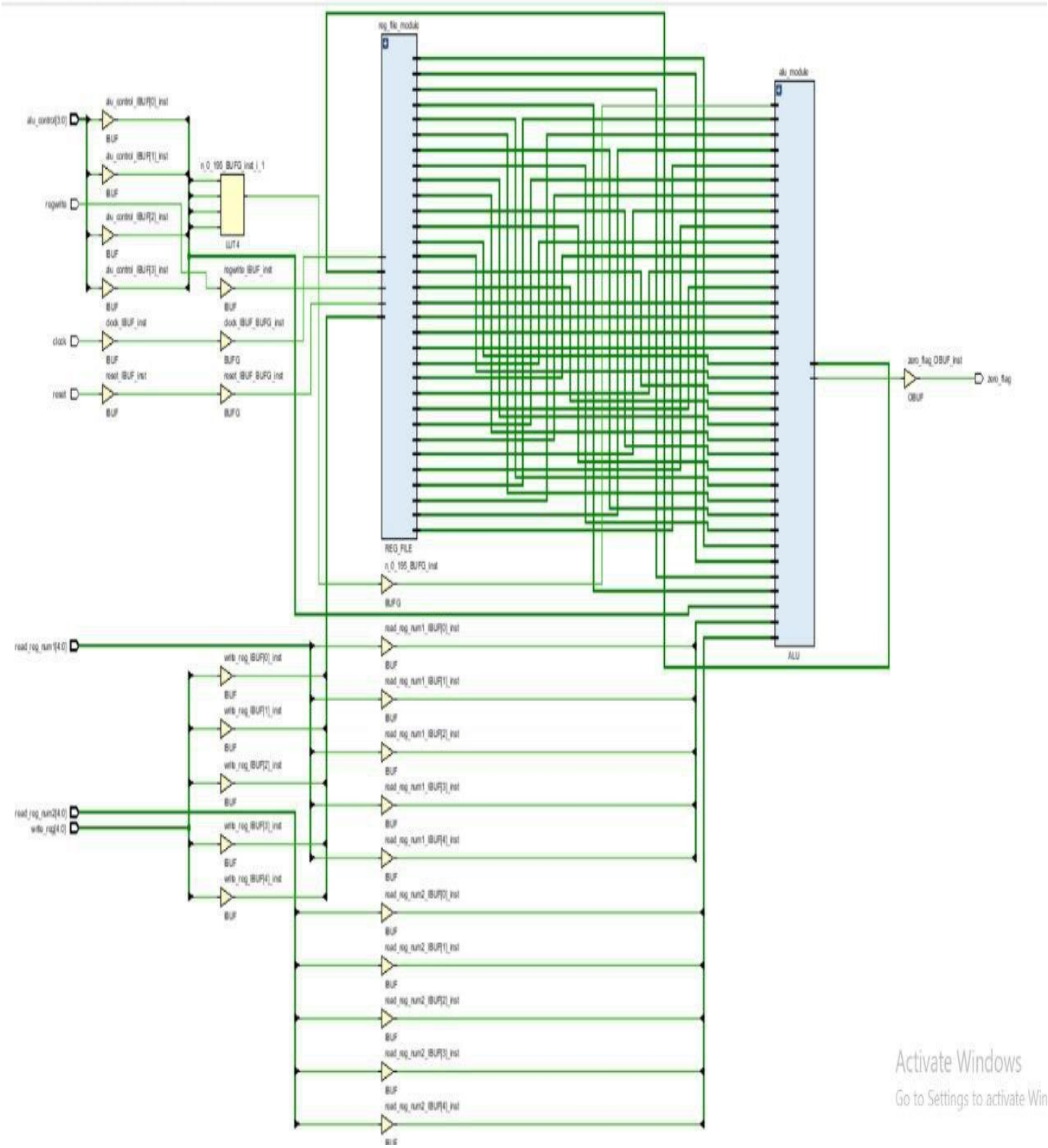

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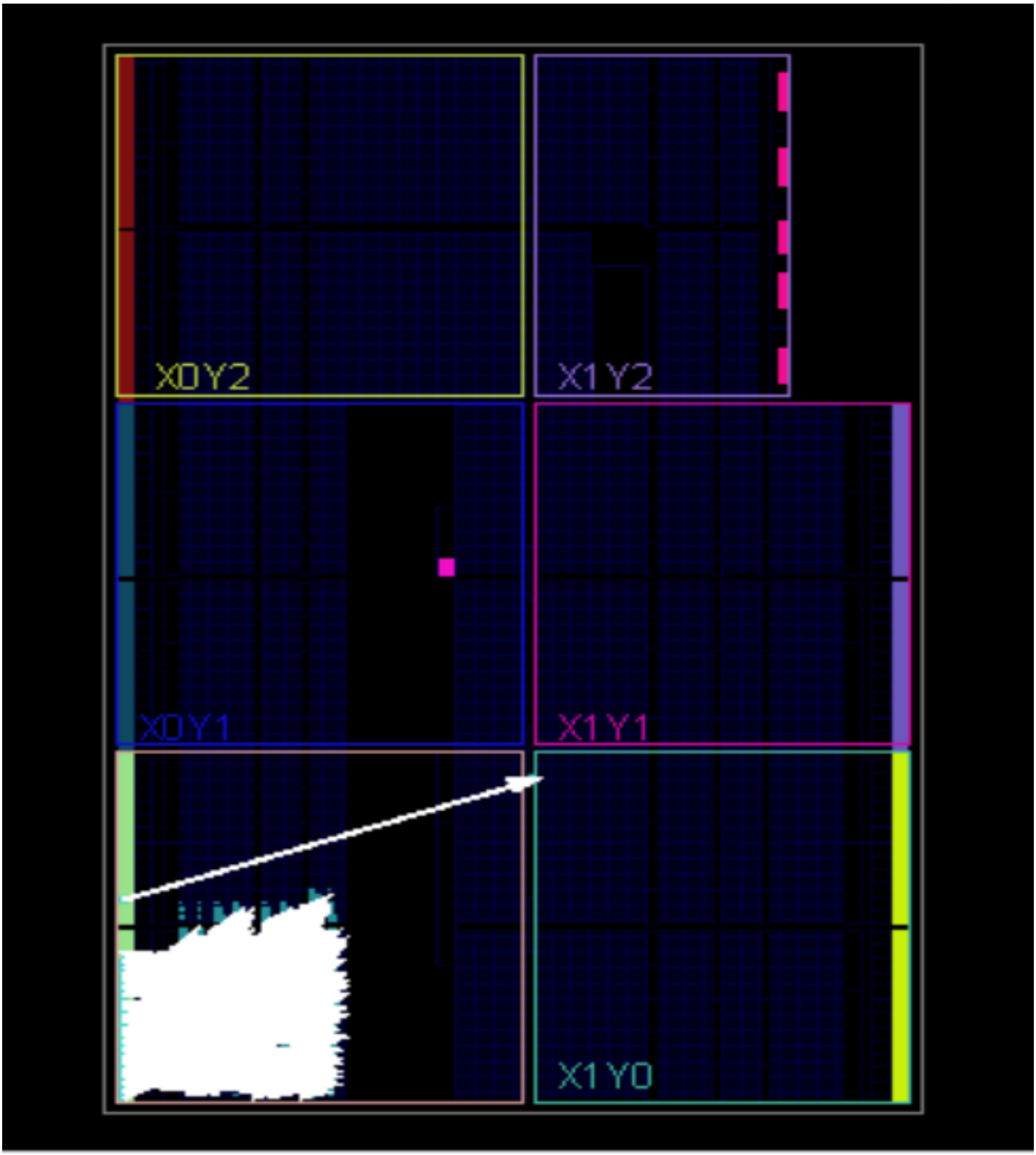
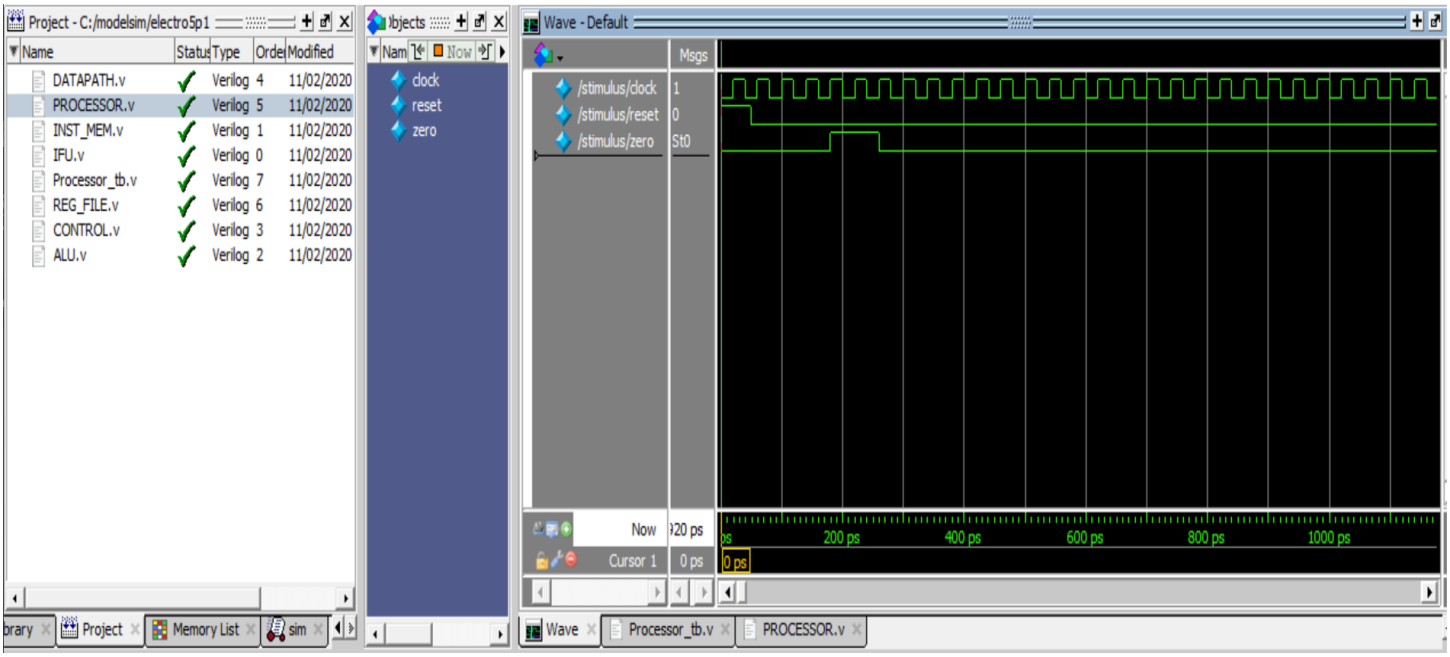


RISC-V Processor

Timing Diagram:



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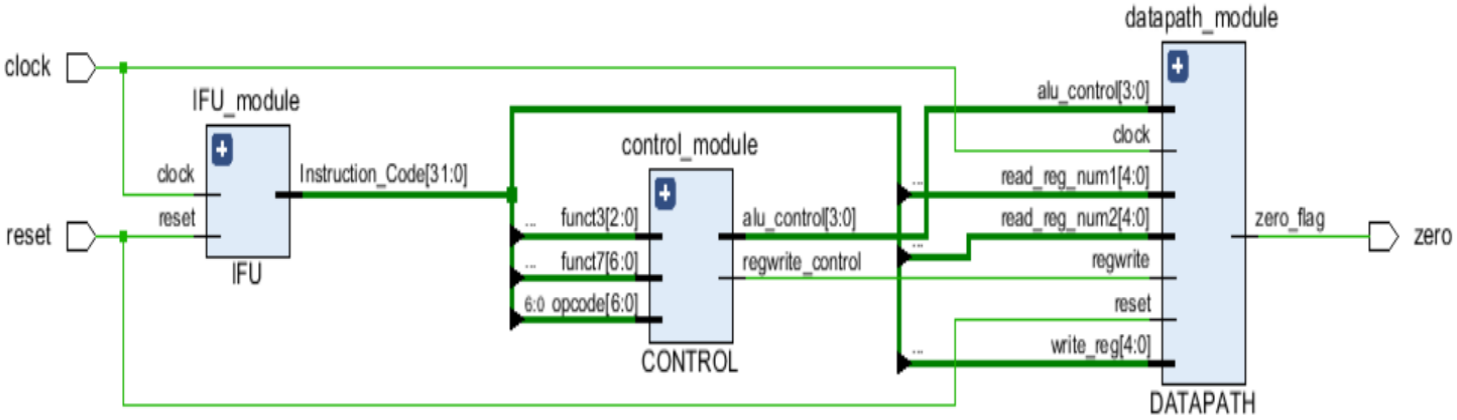

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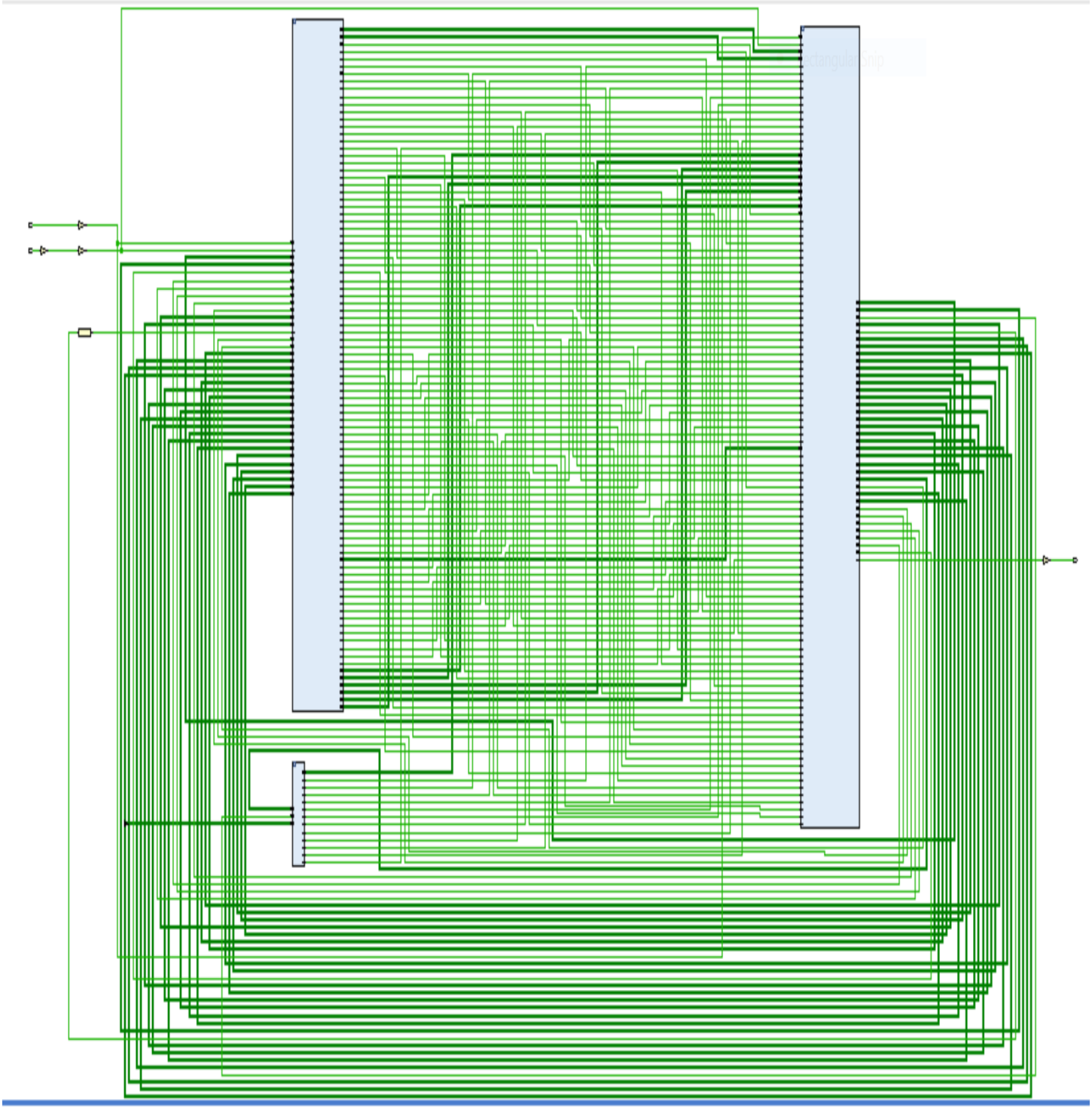

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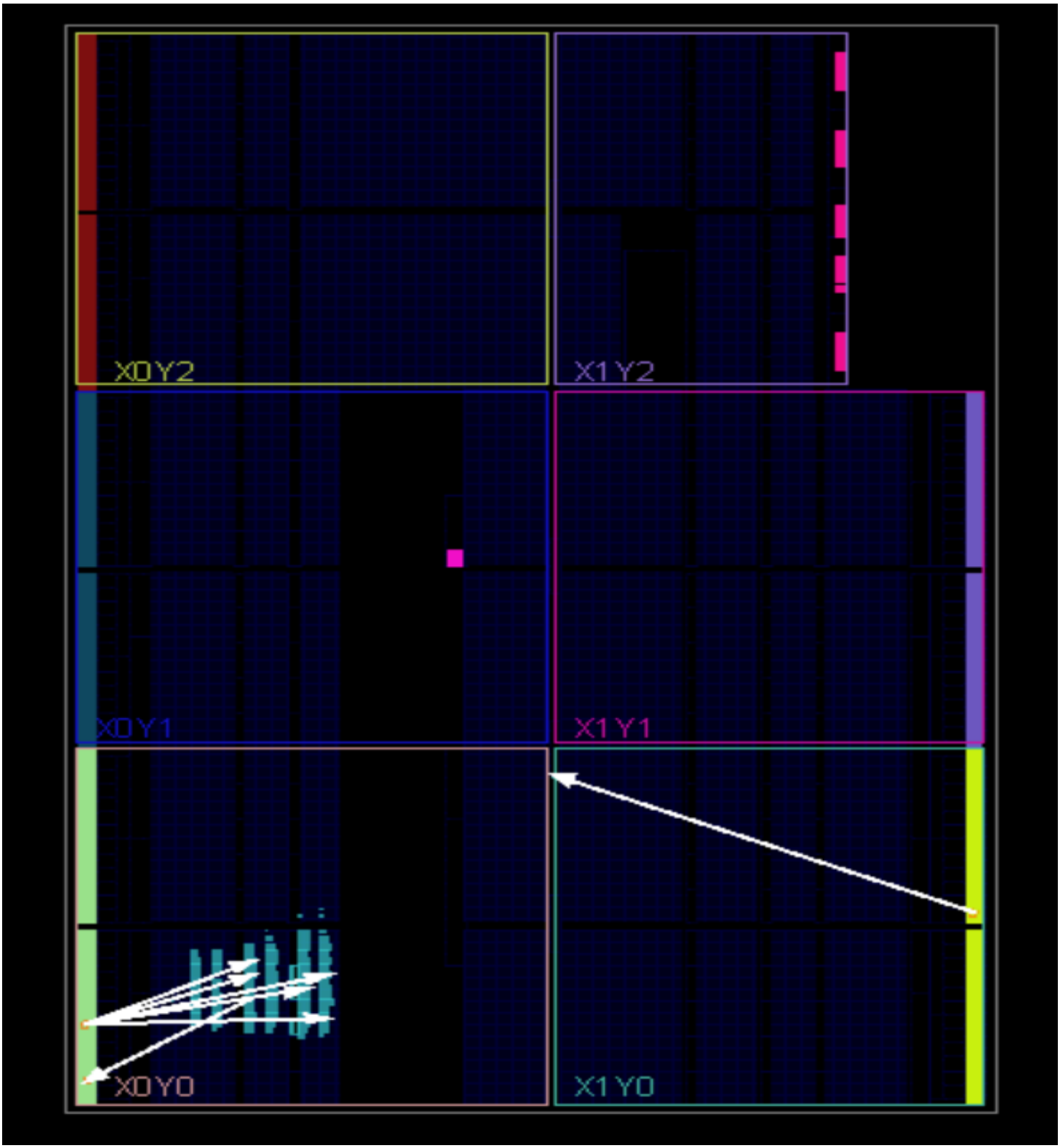
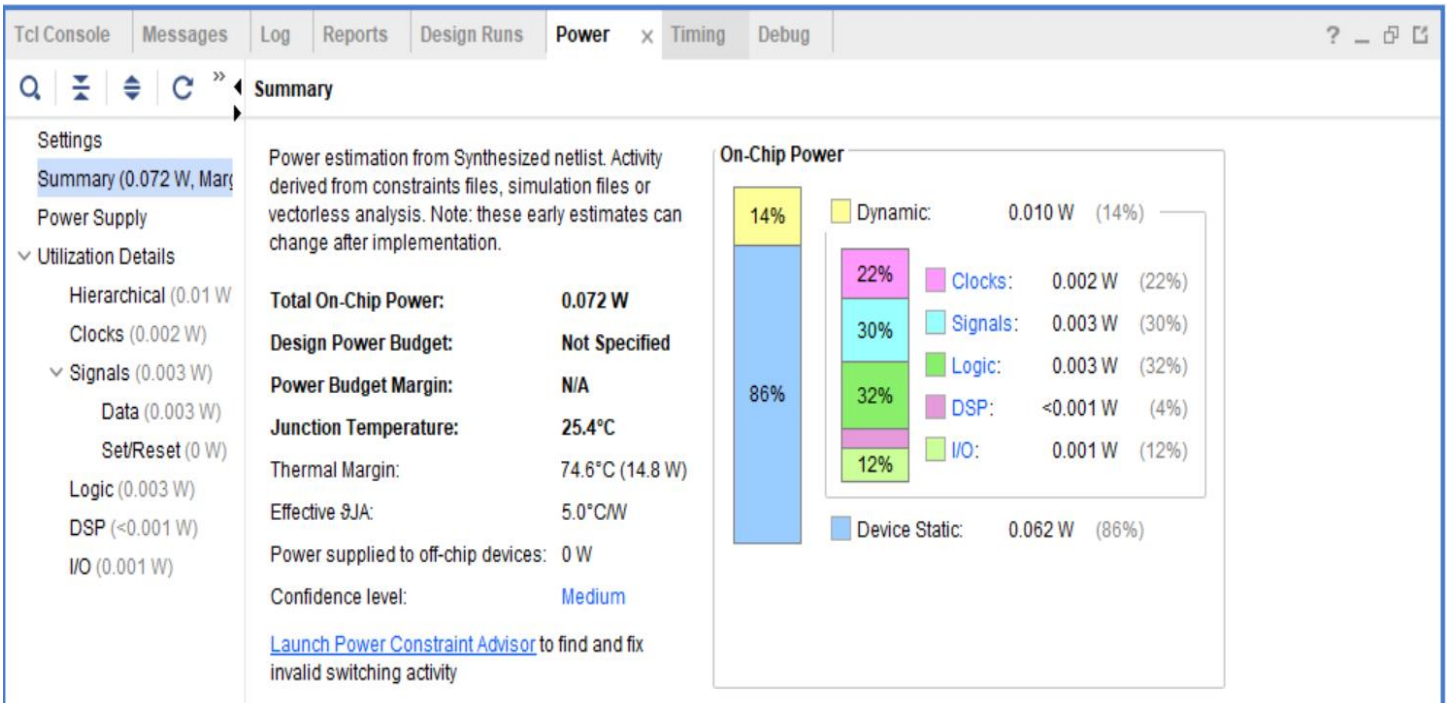


Power Consumption Report:



Bit Stream Check to Implement on FPGA: