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ASSIGNMENT_4

Question 1

Cross Coverage & SVA Assignment

Q1. Add the following cross coverage in the class of the ALSU of the last assignment:

1. When the ALU is addition or multiplication, A and B should have taken all permutations of maxpos, maxneg and zero.
2. When the ALU is addition, c_in should have taken 0 or 1
3. When the ALSU is shifting, then shift_in must take 0 or 1
4. When the ALSU is shifting or rotating, then direction must take 0 or 1
5. When the ALSU is OR or XOR and red_op_A is asserted, then A took all walking one patterns (001, 010, and 100) while B is taking the value 0
6. When the ALSU is OR or XOR and red_op_B is asserted, then B took all walking one patterns (001, 010, and 100) while A is taking the value 0
7. Covering the invalid case: reduction operation is activated while the opcode is not OR or XOR

Note: You are free to add more cross coverage but make sure to document them in your verification plan. Also, you can breakdown any coverpoints in the class into multiple coverpoints if needed.

I. Verification plan

Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check
ALSU_1	When reset is asserted, the output (out) and the LEDs should be set to zero.	Directed at the start of the simulation. Randomized inputs with reset driven high at least 90% of the time to ensure proper reset testing.	Coverage for reset high condition with various A, B, opcode, and control inputs.	A checker in the testbench ensures out and leds are zero when reset is high.
ALSU_2	When reset is deasserted, the out should correctly compute based on A, B, and the opcode.	Randomized values of A, B, opcode, and control signals. reset deasserted 90% of the time.	Coverage for all possible values of A, B, and opcode.	A checker in the testbench ensures that out matches the expected result based on the opcode, A, and B.
ALSU_3	Ensure correct functionality for all combinations of opcodes (OR, XOR, ADD, MULT, SHIFT, ROTATE) under randomized conditions.	Fully randomized A, B, opcode, and control signals for multiple clock cycles.	Coverage for transitions between different opcodes and their effects on out and leds.	A checker ensures the out value corresponds to the correct operation based on the opcode and inputs (A, B).
ALSU_4	Ensure correct functionality when reduction operations and bypass signals are active (red_op_A, red_op_B, bypass_A, bypass_B).	Force red_op_A, red_op_B, bypass_A, and bypass_B to zeros and one to test both bypass and reduction.	Coverage of red_op_A, red_op_B, bypass_A, and bypass_B toggle states combined with other signals.	A checker in the testbench ensures that the reduction operations and bypass correctly modify the output as expected.
ALSU_5	Validate the correct handling of boundary cases such as overflow or underflow in ADD, MULT, and shift operations.	Randomized test cases with boundary conditions, especially for large values of A and B and opcode corresponding to ADD, MULT, and SHIFT.	Coverage for boundary conditions (e.g., overflow/underflow in ADD, MULT) combined with random values of A and B.	A checker in the testbench verifies that the results of arithmetic and shift operations match expected values, even in overflow/underflow cases.
ALSU_6	Ensure correct operation under high-frequency toggling of clk, A, and B.	Toggle clk, A, and B frequently with randomized values. Test high toggle rates for inputs and clock.	Functional coverage for frequent changes in inputs and clock and the effect on output.	A checker ensures the design operates correctly and produces valid results under rapid changes in inputs.

II. RTL Design

```
module ALSU(A, B, cin, serial_in, red_op_A, red_op_B, opcode, bypass_A, bypass_B, clk, rst, direction, leds, out);
parameter INPUT_PRIORITY = "A";
parameter FULL_ADDER = "ON";
input clk, rst, red_op_A, red_op_B, bypass_A, bypass_B, direction, serial_in;
input [2:0] opcode;
input signed cin;
input signed [2:0] A, B;
output reg [15:0] leds;
output reg signed [5:0] out;
reg red_op_A_reg, red_op_B_reg, bypass_A_reg, bypass_B_reg, direction_reg, serial_in_reg;
reg [2:0] opcode_reg;
reg signed [2:0] A_reg, B_reg;
reg signed [1:0] cin_reg ;
wire invalid_red_op, invalid_opcode, invalid;
//Invalid handling
assign invalid_red_op = (red_op_A_reg | red_op_B_reg) & (opcode_reg[1] | opcode_reg[2]);
assign invalid_opcode = opcode_reg[1] & opcode_reg[2];
assign invalid = invalid_red_op | invalid_opcode;
//Registering input signals
always @(posedge clk or posedge rst) begin
  if(rst) begin
     cin_reg <= 0;
     red_op_B_reg <= 0;
     red_op_A_reg <= 0;
     bypass_B_reg <= 0;
     bypass_A_reg <= 0;
     direction_reg <= 0;
     serial_in_reg <= 0;
     opcode_reg <= 0;
     A_reg <= 0;
     B_reg <= 0;
  end else begin
     cin_reg <= cin;
     red_op_B_reg <= red_op_B;
     red_op_A_reg <= red_op_A;
     bypass_B_reg <= bypass_B;
     bypass_A_reg <= bypass_A;
```

```
        direction_reg <= direction;
        serial_in_reg <= serial_in;
        opcode_reg <= opcode;
        A_reg <= A;
        B_reg <= B;
    end
end
//leds output blinking
always @(posedge clk or posedge rst) begin
    if(rst) begin
        leds <= 0;
    end else begin
        if (invalid)
          leds <= ~leds;
        else
          leds <= 0;
    end
end
//ALSU output processing
always @(posedge clk or posedge rst) begin
    if(rst) begin
      out <= 0;
    end
    else begin
      if (invalid)
          out <= 0;
      else if (bypass_A_reg && bypass_B_reg)
        out <= (INPUT_PRIORITY == "A")? A_reg: B_reg;
      else if (bypass_A_reg)
        out <= A_reg;
      else if (bypass_B_reg)
        out <= B_reg;
      else begin
          case (opcode_reg)
    3'h0: begin
      if (red_op_A_reg && red_op_B_reg)
        out <= (INPUT_PRIORITY == "A") ? |A_reg : |B_reg;
      else if (red_op_A_reg)
        out <= |A_reg;
      else if (red_op_B_reg)
        out <= |B_reg;
      else
        out <= A_reg | B_reg;
    end
    3'h1: begin
      if (red_op_A_reg && red_op_B_reg)
        out <= (INPUT_PRIORITY == "A") ? ^A_reg : ^B_reg;
      else if (red_op_A_reg)
        out <= ^A_reg;
      else if (red_op_B_reg)
        out <= ^B_reg;
      else
        out <= A_reg ^ B_reg;
    end
          3'h2: begin
             if (FULL_ADDER == "ON")
             out <= A_reg + B_reg + cin_reg;
             else out <= A_reg + B_reg;
          end
          3'h3: out <= A_reg * B_reg;
          3'h4: begin
            if (direction_reg)
              out <= {out[4:0], serial_in_reg};
            else
              out <= {serial_in_reg, out[5:1]};
          end
          3'h5: begin
            if (direction_reg)
              out <= {out[4:0], out[5]};
            else
              out <= {out[0], out[5:1]};
          end
```

```
109             end
110              default : out <= 0;
111
112         endcase
113       end
114     end
115   end
116   endmodule
```

III. Golden Model

```
1  module ALSU_GM(A, B, cin, serial_in, red_op_A, red_op_B, opcode, bypass_A, bypass_B, clk, rst, direction, leds_expected, out_expected);
2  input clk, rst, red_op_A, red_op_B, bypass_A, bypass_B, direction, serial_in;
3  input [2: 0] opcode;
4  input signed cin;
5  input signed [2: 0] A, B;
6  output reg [15: 0] leds_expected;
7  output reg signed [5: 0] out_expected;
8  reg red_op_A_reg, red_op_B_reg, bypass_A_reg, bypass_B_reg, direction_reg, serial_in_reg;
9  reg [2: 0] opcode_reg;
10 reg signed [2: 0] A_reg,B_reg;
11 reg signed cin_reg;
12 wire invalid_red_op, invalid_opcode, invalid;
13 assign invalid_red_op = (red_op_A_reg | red_op_B_reg) & (opcode_reg[1] | opcode_reg[2]);
14 assign invalid_opcode = opcode_reg[1] & opcode_reg[2];
15 assign invalid = invalid_red_op | invalid_opcode;
16 always @(posedge clk or posedge rst) begin
17 if(rst) begin
18 cin_reg <= 0;
19 red_op_B_reg <= 0;
20 red_op_A_reg <= 0;
21 bypass_B_reg <= 0;
22 bypass_A_reg <= 0;
23 direction_reg <= 0;
24 serial_in_reg <= 0;
25 opcode_reg <= 0;
26 A_reg <= 0;
27 B_reg <= 0;
28 end else begin
29 cin_reg <= cin;
30 red_op_B_reg <= red_op_B;
31 red_op_A_reg <= red_op_A;
32 bypass_B_reg <= bypass_B;
33 bypass_A_reg <= bypass_A;
34 direction_reg <= direction;
35 serial_in_reg <= serial_in;
36 opcode_reg <= opcode;
37 A_reg <= A;
```

```
38  B_reg <= B;
39  end
40  end
41  always @(posedge clk or posedge rst) begin
42  if(rst) begin
43  leds_expected <= 0;
44  end else begin
45  if (invalid)
46  leds_expected <= ~leds_expected;
47  else
48  leds_expected <= 0;
49  end
50  end
51  always @(posedge clk or posedge rst) begin
52  if(rst) begin
53  out_expected <= 0;
54  end
55  else begin
56  if (invalid)
57  out_expected <= 0;
58  else if (bypass_A_reg && bypass_B_reg)
59  out_expected <= A_reg ;
60  else if (bypass_A_reg)
61  out_expected <= A_reg ;
62  else if (bypass_B_reg)
63  out_expected <= B_reg ;
64  else begin
65  case (opcode_reg)
66  3'h0:
67  if (red_op_A_reg && red_op_B_reg)
68  out_expected = |A_reg;
69  else if (red_op_A_reg)
70  out_expected <= |A_reg;
71  else if (red_op_B_reg)
72  out_expected <= |B_reg;
73  else
```

```
74    out_expected <= A_reg | B_reg;
75    3'h1:
76    if (red_op_A_reg && red_op_B_reg)
77    out_expected <= ^A_reg;
78    else if (red_op_A_reg)
79    out_expected <= ^A_reg;
80    else if (red_op_B_reg)
81    out_expected <= ^B_reg;
82    else
83    out_expected <= A_reg ^ B_reg;
84    3'h2: out_expected <= A_reg + B_reg + cin_reg ;
85    3'h3: out_expected <= A_reg * B_reg;
86    3'h4:
87    if (direction_reg)
88    out_expected <= {out_expected[4: 0], serial_in_reg};
89    else
90    out_expected <= {serial_in_reg, out_expected[5: 1]};
91    3'h5:
92    if (direction_reg)
93    out_expected <= {out_expected[4: 0], out_expected[5]};
94    else
95    out_expected <= {out_expected[0], out_expected[5: 1]};
96    default: out_expected <= 0 ;
97    endcase
98    end
99    end
100   end
101   endmodule
```

IV. Package

```
package pck;
typedef enum bit [2:0] {OR, XOR, ADD, MULT, SHIFT, ROTATE, INVALID_6, INVALID_7} opcode_e;
typedef enum bit [2:0] {Or, Xor, Add, Mult, Shift, Rotate} opcode_valid_e;
localparam MAXPOS = 3;
localparam MAXNEG = -4;
localparam ZERO = 0;
class Z;
  rand bit rst_c, red_op_A_c, red_op_B_c, cin_c, serial_in_c, direction_c, bypass_A_c, bypass_B_c;
  rand bit signed [2:0] A_c, B_c;
  rand opcode_e opcode_c;
  rand opcode_valid_e array[6];
  constraint c_rst { rst_c dist {0:/90, 1:/10}; }
  constraint c_input_A {
    if (opcode_c == ADD || opcode_c == MULT) {
      A_c dist {
        MAXPOS / 25,
        MAXNEG / 25,
        ZERO / 25,
        {3'b001, 3'b010, 3'b101, 3'b110, 3'b111} / 25
      };
    } else if ((opcode_c == OR || opcode_c == XOR) && red_op_A_c == 1) {
      B_c == 0;
      A_c dist {
        {3'b001, 3'b010, 3'b100} := 80,
        {3'b000, 3'b011, 3'b101, 3'b110, 3'b111} := 20};} else { A_c inside {[MAXNEG: MAXPOS]};}}
  constraint c_input_B {
    if (opcode_c == ADD || opcode_c == MULT) {
      B_c dist {
        MAXPOS / 25,
        MAXNEG / 25,
        ZERO / 25,
        {3'b001, 3'b010, 3'b101, 3'b110, 3'b111} / 25};} else if ((opcode_c == OR || opcode_c == XOR) && red_op_A_c == 1) {
      A_c == 0;
      B_c dist {
        {3'b001, 3'b010, 3'b100} := 80,
        {3'b000, 3'b011, 3'b101, 3'b110, 3'b111} := 20};} else {B_c inside {[MAXNEG: MAXPOS]};}}
  constraint c_opcode { opcode_c dist {[0:5]:/ 90, [6:7] :/ 10}; }
```

```
    constraint c_bypass_signals {
      bypass_A_c dist {0:/90, 1:/10};
      bypass_B_c dist {0:/90, 1:/10};}
    constraint all_branches {
      if (opcode_c == ADD || opcode_c == MULT) {
        red_op_A_c dist {0:/50, 1:/50};
        red_op_B_c dist {0:/50, 1:/50};}
      if (opcode_c == OR || opcode_c == XOR) {
        if (red_op_A_c == 1) {
          A_c dist {
            {3'b001, 3'b010, 3'b100} := 80,
            {3'b000, 3'b011, 3'b101, 3'b110, 3'b111} := 20};B_c == 0;}
        if (red_op_B_c == 1) {
          B_c dist {
            {3'b001, 3'b010, 3'b100} := 80,
            {3'b000, 3'b011, 3'b101, 3'b110, 3'b111} := 20};A_c == 0;}}}
    constraint c_array {
      foreach (array[i]) {
        foreach (array[j]) {
          if (i != j) {
            array[i] != array[j];}}}}
    covergroup cg;
      A_cp: coverpoint A_c {
        bins data_0 = {ZERO};
        bins data_max = {MAXPOS};
        bins data_min = {MAXNEG};
        bins data_walkingones = {3'b001, 3'b010, 3'b100};
        bins data_default = default;}
      B_cp: coverpoint B_c {
        bins data_0 = {ZERO};
        bins data_max = {MAXPOS};
        bins data_min = {MAXNEG};
        bins data_walkingones = {3'b001, 3'b010, 3'b100};
        bins data_default = default;}
```

```
72    ALU_cp: coverpoint opcode_c {
73      bins Bins_shift[] = {SHIFT, ROTATE};
74      bins Bins_arith[] = {ADD, MULT};
75      bins Bins_bitwise[] = {OR, XOR};
76      illegal_bins Bins_invalid = {INVALID_6, INVALID_7};
77      bins Bins_trans = (OR => XOR => ADD => MULT => SHIFT => ROTATE);}
78    red_A_cp: coverpoint red_op_A_c {
79      bins Bins_red_A = {0, 1};}
80    red_B_cp: coverpoint red_op_B_c {
81      bins Bins_red_B = {0, 1};}
82    cin_cp: coverpoint cin_c {
83      bins Bins_Cin = {0, 1};}
84    serial_in_cp: coverpoint serial_in_c {
85      bins Bins_serial_in = {0, 1};}
86    direction_cp: coverpoint direction_c {
87      bins Bins_Direction = {0, 1};}
88    ALU_cross1: cross A_cp, B_cp, ALU_cp {
89      bins cross_ab_arith = binsof(ALU_cp.Bins_arith) && binsof(A_cp) intersect {ZERO, MAXNEG, MAXPOS}
90        && binsof(B_cp) intersect {ZERO, MAXNEG, MAXPOS};
91    ignore_bins ignore_ab_arith=! binsof(ALU_cp.Bins_arith) && binsof(A_cp) intersect {ZERO, MAXNEG, MAXPOS}&& binsof(B_cp) intersect {ZERO, MAXNEG, MAXPOS} ;
92    ignore_bins ignore_trans_opcode = binsof(ALU_cp. Bins_trans) ;}
93    ALU_cross2: cross ALU_cp, cin_cp {
94      bins cross_cin_arith = binsof(ALU_cp.Bins_arith) && binsof(cin_cp.Bins_Cin);}
95    ALU_cross3: cross ALU_cp, serial_in_cp, direction_cp {
96    bins cross_serial_shift = binsof(ALU_cp.Bins_shift) && binsof(serial_in_cp.Bins_serial_in);
97    bins cross_shift_direction = binsof(ALU_cp.Bins_shift) && binsof(direction_cp.Bins_Direction);
98    ignore_bins ignore_serial_shift = !binsof(ALU_cp.Bins_shift);
99    ignore_bins ignore_shift_direction = !binsof(ALU_cp.Bins_shift);}
100   ALU_cross4: cross A_cp, B_cp, ALU_cp, red_A_cp, red_B_cp {
101     bins cross_bitwise_redA = binsof(ALU_cp.Bins_bitwise) && binsof(red_A_cp.Bins_red_A[1])
102       && binsof(A_cp.data_walkingones) && binsof(B_cp.data_0);
103     bins cross_bitwise_redB = binsof(ALU_cp.Bins_bitwise) && binsof(red_B_cp.Bins_red_B[1])
104       && binsof(B_cp.data_walkingones) && binsof(A_cp.data_0);
```



```
105         illegal_bins cross_red_A_not_bitwise
106           = binsof(ALU_cp) intersect {ADD, MULT, SHIFT, ROTATE} && binsof(red_A_cp.Bins_red_A[1]);
107         illegal_bins cross_red_B_not_bitwise
108           = binsof(ALU_cp) intersect {ADD, MULT, SHIFT, ROTATE} && binsof(red_B_cp.Bins_red_B[1]);}
109     endgroup
110     function new();
111       cg = new();
112     endfunction
113   endclass
114   endpackage
115
```

V. Test Bench

```
import pck::*;
module ALSU_TB;
    // Parameters declaration
    parameter INPUT_PRIORITY = "A";
    parameter FULL_ADDER = "ON";
    // Inputs/Outputs declaration
    logic clk, rst, cin, red_op_A, red_op_B, bypass_A, bypass_B, direction, serial_in;
    logic [2:0] opcode;
    logic signed [2:0] A, B;
    logic [15:0] leds;
    logic signed [5:0] out;
    logic signed [5:0] out_expected;
    logic [15:0] leds_expected;
    opcode_valid_e opvalid[6];
    // Create object from the class
    Z obj;
    int error_count, correct_count;
    // Module instantiation for Design and Golden Model
    ALSU #(.INPUT_PRIORITY(INPUT_PRIORITY), .FULL_ADDER(FULL_ADDER)) DUT (.*);
    ALSU_GM DUT2(.*);
    // Clock generation
    initial begin
        clk = 0;
        forever #25 clk = ~clk;
    end
    // Main program block
    initial begin
        obj = new();
        error_count = 0;
        correct_count = 0;
        // First part with loop
        obj.c_array.constraint_mode(0);
        for(int i = 0; i < 10000; i++) begin
            @(negedge clk);
            assert(obj.randomize());
            rst = obj.rst_c;
            cin = obj.cin_c;
```

```
            red_op_A = obj.red_op_A_c;
            red_op_B = obj.red_op_B_c;
            bypass_A = obj.bypass_A_c;
            bypass_B = obj.bypass_B_c;
            direction = obj.direction_c;
            serial_in = obj.serial_in_c;
            opcode = obj.opcode_c;
            A = obj.A_c;
            B = obj.B_c;
            sample_data();
            golden_model();
        end
        // Second part with loop
        obj.constraint_mode(0);
        obj.c_array.constraint_mode(1);
        // Force reduction operation and bypass to zeros
        red_op_A = 0;
        red_op_B = 0;
        bypass_A = 0;
        bypass_B = 0;
        for(int i = 0; i < 10000; i++) begin
            @(negedge clk);
            assert(obj.randomize());
            rst = obj.rst_c;
            cin = obj.cin_c;
            red_op_A = obj.red_op_A_c;
            red_op_B = obj.red_op_B_c;
            bypass_A = obj.bypass_A_c;
            bypass_B = obj.bypass_B_c;
            direction = obj.direction_c;
            serial_in = obj.serial_in_c;
            A = obj.A_c;
            B = obj.B_c;
            for(int j = 0; j < 6; j++) begin
                opvalid[j] = obj.array[j];
```

```
                    opcode = opvalid[j];
                    #25 sample_data();
                end
                sample_data();
                golden_model();
            end
        // Direct case to hit the transition bin
            // Initialize coverage collection
            obj.cg.start();
            // Test transitions from opcode 0 to 5
            obj.opcode_c = opcode_e'(3'b000);  // OR
            opcode = 3'b000;
            @(negedge clk);
            #25;  // Wait for half a clock period
            obj.cg.sample();
            obj.opcode_c = opcode_e'(3'b001);  // XOR
            opcode = 3'b001;
            @(negedge clk);
            #25;
            obj.cg.sample();
            obj.opcode_c = opcode_e'(3'b010);  // ADD
            opcode = 3'b010;
            @(negedge clk);
            #25;
            obj.cg.sample();
            obj.opcode_c = opcode_e'(3'b011);  // MULT
            opcode = 3'b011;
            @(negedge clk);
            #25;
            obj.cg.sample();
            obj.opcode_c = opcode_e'(3'b100);  // SHIFT
            opcode = 3'b100;
            @(negedge clk);
            #25;
            obj.cg.sample();
```

```
        obj.opcode_c = opcode_e'(3'b101);  // ROTATE
        opcode = 3'b101;
        @(negedge clk);
        #25;
        obj.cg.sample();
        $display("correct counter = %0d , error counter = %0d", correct_count, error_count);
        $stop;
    end
    task sample_data();
        if (rst == 1 || bypass_A == 1 || bypass_B == 1) begin
            obj.cg.stop();
        end else begin
            obj.cg.start();
            obj.cg.sample();
        end
    endtask
    task golden_model();
        @(negedge clk);
        if (out != out_expected || leds != leds_expected) begin
            $display("Incorrect result!! A=%0d, B=%0d, opcode=%0b, out=%0d, out_expected=%0d, leds=%0b, leds_expected=%0b",
            A, B, opcode, out, out_expected, leds, leds_expected);
            error_count++;
        end else begin
            correct_count++;
        end
    endtask
endmodule
```

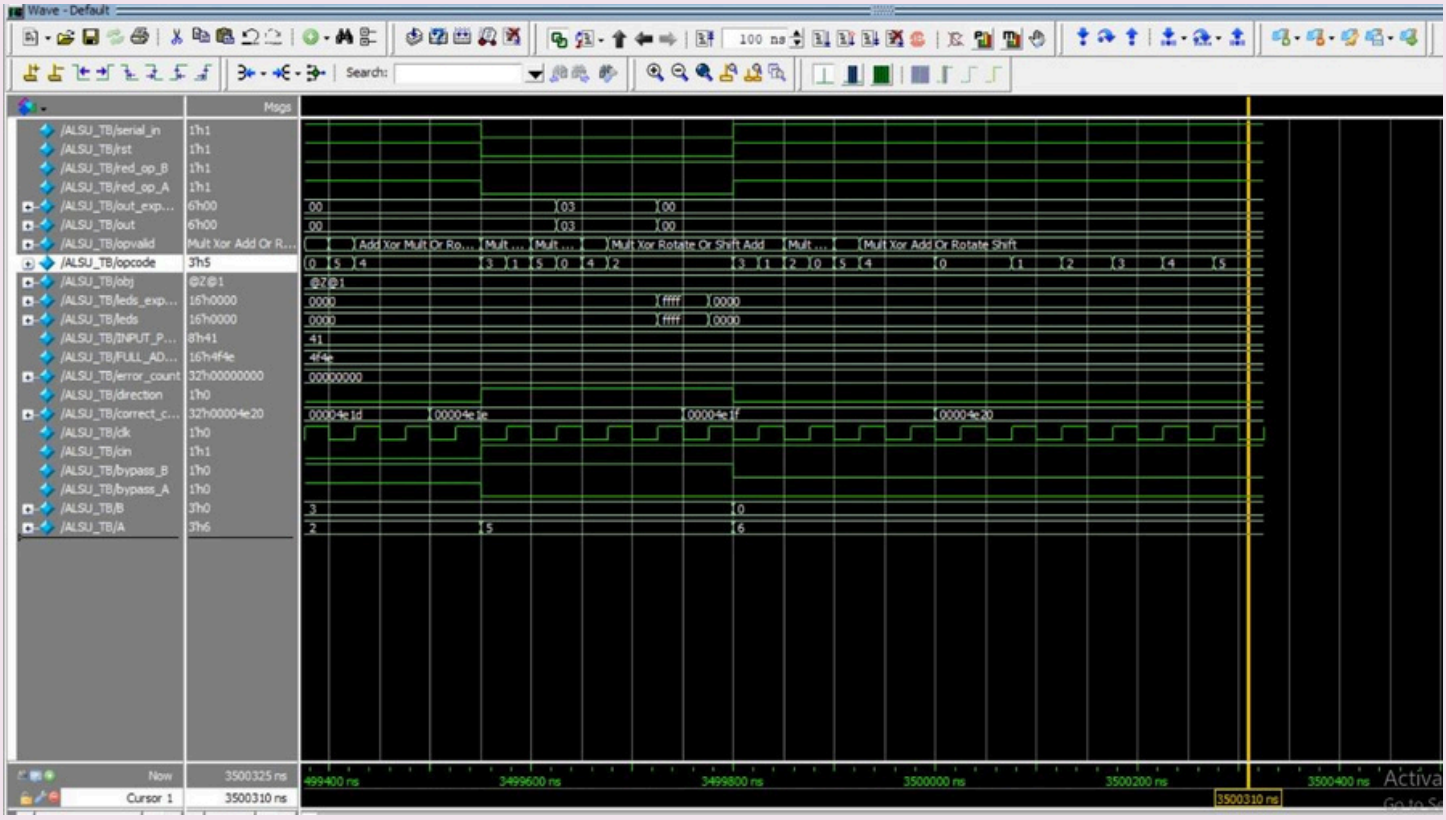
VI. Counter

```
# correct counter = 20000 , error counter = 0
```

VII. Do file

```
vlib work
vlog ALSU.sv Package.sv ALSU_GM.sv ALSU_TB.sv  +cover -covercells
vsim -voptargs=+acc work.ALSU_TB -cover
add wave *
coverage save ALSU_TB.ucdb -onexit -du work.ALSU
run -all
```

VIII. Waveform



IX. Functional Coverage Report

```
Coverage Report by instance with details

================================================================================
=== Instance: /pck
=== Design Unit: work.pck
================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na   100.00%
        Coverpoints/Crosses    12        na        na        na
            Covergroup Bins   106       106         0   100.00%
----------------------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------------------
 TYPE /pck/Z/cg                                   100.00%        100          -    Covered
    covered/total bins:                               106        106          -
    missing/total bins:                                 0        106          -
    % Hit:                                         100.00%        100          -
    Coverpoint A_cp                                100.00%        100          -    Covered
        covered/total bins:                               4          4          -
        missing/total bins:                               0          4          -
        % Hit:                                     100.00%        100          -
    Coverpoint B_cp                                100.00%        100          -    Covered
        covered/total bins:                               4          4          -
        missing/total bins:                               0          4          -
        % Hit:                                     100.00%        100          -
    Coverpoint ALU_cp                              100.00%        100          -    Covered
        covered/total bins:                               7          7          -
        missing/total bins:                               0          7          -
        % Hit:                                     100.00%        100          -
    Coverpoint red_A_cp                            100.00%        100          -    Covered
        covered/total bins:                               1          1          -
        missing/total bins:                               0          1          -
        % Hit:                                     100.00%        100          -
    Coverpoint red_B_cp                            100.00%        100          -    Covered
        covered/total bins:                               1          1          -
        missing/total bins:                               0          1          -
        % Hit:                                     100.00%        100          -
    Coverpoint cin_cp                              100.00%        100          -    Covered
        covered/total bins:                               1          1          -
        missing/total bins:                               0          1          -
        % Hit:                                     100.00%        100          -
    Coverpoint serial_in_cp                        100.00%        100          -    Covered
        covered/total bins:                               1          1          -
        missing/total bins:                               0          1          -
        % Hit:                                     100.00%        100          -
    Coverpoint direction_cp                        100.00%        100          -    Covered
        covered/total bins:                               1          1          -
        missing/total bins:                               0          1          -
        % Hit:                                     100.00%        100          -
    Cross ALU_cross1                               100.00%        100          -    Covered
        covered/total bins:                              43         43          -
        missing/total bins:                               0         43          -
        % Hit:                                     100.00%        100          -
    Cross ALU_cross2                               100.00%        100          -    Covered
        covered/total bins:                               6          6          -
        missing/total bins:                               0          6          -
        % Hit:                                     100.00%        100          -
    Cross ALU_cross3                               100.00%        100          -    Covered
        covered/total bins:                               7          7          -
        missing/total bins:                               0          7          -
        % Hit:                                     100.00%        100          -
    Cross ALU_cross4                               100.00%        100          -    Covered
        covered/total bins:                              30         30          -
        missing/total bins:                               0         30          -
        % Hit:                                     100.00%        100          -
 Covergroup instance \/pck::Z::cg                  100.00%        100          -    Covered
    covered/total bins:                               106        106          -
    missing/total bins:                                 0        106          -
    % Hit:                                         100.00%        100          -
    Coverpoint A_cp                                100.00%        100          -    Covered
        covered/total bins:                               4          4          -
        missing/total bins:                               0          4          -
        % Hit:                                     100.00%        100          -
        bin data_0                                    3913          1          -    Covered
        bin data_max                                  1928          1          -    Covered
        bin data_min                                  1761          1          -    Covered
```

```
    bin data_min                                1761          1          -    Covered
    bin data_walkingones                        3529          1          -    Covered
    default bin data_default                    5231                     -    Occurred
Coverpoint B_cp                               100.00%        100          -    Covered
    covered/total bins:                             4          4          -
    missing/total bins:                             0          4          -
    % Hit:                                    100.00%        100          -
    bin data_0                                  3964          1          -    Covered
    bin data_max                                1739          1          -    Covered
    bin data_min                                1706          1          -    Covered
    bin data_walkingones                        3321          1          -    Covered
    default bin data_default                    5632                     -    Occurred
Coverpoint ALU_cp                             100.00%        100          -    Covered
    covered/total bins:                             7          7          -
    missing/total bins:                             0          7          -
    % Hit:                                    100.00%        100          -
    illegal_bin Bins_invalid                    2939                     -    Occurred
    bin Bins_shift[SHIFT]                       2238          1          -    Covered
    bin Bins_shift[ROTATE]                      2144          1          -    Covered
    bin Bins_arith[ADD]                         2209          1          -    Covered
    bin Bins_arith[MULT]                        2390          1          -    Covered
    bin Bins_bitwise[OR]                        2240          1          -    Covered
    bin Bins_bitwise[XOR]                       2202          1          -    Covered
    bin Bins_trans                                 1          1          -    Covered
Coverpoint red_A_cp                           100.00%        100          -    Covered
    covered/total bins:                             1          1          -
    missing/total bins:                             0          1          -
    % Hit:                                    100.00%        100          -
    bin Bins_red_A                              16362          1          -    Covered
Coverpoint red_B_cp                           100.00%        100          -    Covered
    covered/total bins:                             1          1          -
    missing/total bins:                             0          1          -
    % Hit:                                    100.00%        100          -
    bin Bins_red_B                              16362          1          -    Covered
Coverpoint cin_cp                             100.00%        100          -    Covered
    covered/total bins:                             1          1          -
    missing/total bins:                             0          1          -
    % Hit:                                    100.00%        100          -
    bin Bins_Cin                                16362          1          -    Covered
Coverpoint serial_in_cp                       100.00%        100          -    Covered
    covered/total bins:                             1          1          -
    missing/total bins:                             0          1          -
    % Hit:                                    100.00%        100          -
    bin Bins_serial_in                          16362          1          -    Covered
Coverpoint direction_cp                       100.00%        100          -    Covered
    covered/total bins:                             1          1          -
    missing/total bins:                             0          1          -
    % Hit:                                    100.00%        100          -
    bin Bins_Direction                          16362          1          -    Covered
Cross ALU_cross1                              100.00%        100          -    Covered
    covered/total bins:                            43         43          -
    missing/total bins:                             0         43          -
    % Hit:                                    100.00%        100          -
    Auto, Default and User Defined Bins:
        bin cross_ab_arith                      2469          1          -    Covered
        bin <data_walkingones,data_walkingones,Bins_bitwise[XOR]>
                                                 139          1          -    Covered
        bin <data_walkingones,data_walkingones,Bins_bitwise[OR]>
                                                 131          1          -    Covered
        bin <data_walkingones,data_max,Bins_bitwise[XOR]>
                                                  78          1          -    Covered
        bin <data_walkingones,data_max,Bins_bitwise[OR]>
                                                  72          1          -    Covered
        bin <data_walkingones,data_min,Bins_bitwise[XOR]>
                                                  63          1          -    Covered
        bin <data_walkingones,data_min,Bins_bitwise[OR]>
                                                  82          1          -    Covered
        bin <data_walkingones,data_0,Bins_bitwise[XOR]>
                                                  75          1          -    Covered
        bin <data_walkingones,data_0,Bins_bitwise[OR]>
                                                  74          1          -    Covered
        bin <data_min,data_walkingones,Bins_bitwise[XOR]>
                                                  61          1          -    Covered
        bin <data_min,data_walkingones,Bins_bitwise[OR]>
                                                  69          1          -    Covered
        bin <data_max,data_walkingones,Bins_bitwise[XOR]>
                                                  44          1          -    Covered
        bin <data_max,data_walkingones,Bins_bitwise[OR]>
                                                  74          1          -    Covered
        bin <data_0,data_walkingones,Bins_bitwise[XOR]>
```

```
                                                    64          1          -    Covered
        bin <data_0,data_walkingones,Bins_bitwise[OR]>
                                                    41          1          -    Covered
        bin <data_walkingones,data_walkingones,Bins_arith[MULT]>
                                                    21          1          -    Covered
        bin <data_walkingones,data_walkingones,Bins_shift[ROTATE]>
                                                   134          1          -    Covered
        bin <data_walkingones,data_walkingones,Bins_arith[ADD]>
                                                    77          1          -    Covered
        bin <data_walkingones,data_walkingones,Bins_shift[SHIFT]>
                                                   145          1          -    Covered
        bin <data_walkingones,data_max,Bins_arith[MULT]>
                                                    28          1          -    Covered
        bin <data_walkingones,data_max,Bins_shift[ROTATE]>
                                                    60          1          -    Covered
        bin <data_walkingones,data_max,Bins_arith[ADD]>
                                                    42          1          -    Covered
        bin <data_walkingones,data_max,Bins_shift[SHIFT]>
                                                    86          1          -    Covered
        bin <data_walkingones,data_min,Bins_arith[MULT]>
                                                    21          1          -    Covered
        bin <data_walkingones,data_min,Bins_shift[ROTATE]>
                                                    53          1          -    Covered
        bin <data_walkingones,data_min,Bins_arith[ADD]>
                                                    49          1          -    Covered
        bin <data_walkingones,data_min,Bins_shift[SHIFT]>
                                                    83          1          -    Covered
        bin <data_walkingones,data_0,Bins_arith[MULT]>
                                                    70          1          -    Covered
        bin <data_walkingones,data_0,Bins_shift[ROTATE]>
                                                    69          1          -    Covered
        bin <data_walkingones,data_0,Bins_arith[ADD]>
                                                    42          1          -    Covered
        bin <data_walkingones,data_0,Bins_shift[SHIFT]>
                                                    48          1          -    Covered
        bin <data_min,data_walkingones,Bins_arith[MULT]>
                                                    56          1          -    Covered
        bin <data_min,data_walkingones,Bins_shift[ROTATE]>
                                                    76          1          -    Covered
        bin <data_min,data_walkingones,Bins_arith[ADD]>
                                                    14          1          -    Covered
        bin <data_min,data_walkingones,Bins_shift[SHIFT]>
                                                    71          1          -    Covered
        bin <data_max,data_walkingones,Bins_arith[MULT]>
                                                    77          1          -    Covered
        bin <data_max,data_walkingones,Bins_shift[ROTATE]>
                                                    76          1          -    Covered
        bin <data_max,data_walkingones,Bins_arith[ADD]>
                                                    42          1          -    Covered
        bin <data_max,data_walkingones,Bins_shift[SHIFT]>
                                                    75          1          -    Covered
        bin <data_0,data_walkingones,Bins_arith[MULT]>
                                                    49          1          -    Covered
        bin <data_0,data_walkingones,Bins_shift[ROTATE]>
                                                    48          1          -    Covered
        bin <data_0,data_walkingones,Bins_arith[ADD]>
                                                    42          1          -    Covered
        bin <data_0,data_walkingones,Bins_shift[SHIFT]>
                                                    47          1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin ignore_trans_opcode               0                     -    ZERO
        ignore_bin ignore_ab_arith                1259                     -    Occurred
Cross ALU_cross2                                100.00%        100          -    Covered
    covered/total bins:                               6          6          -
    missing/total bins:                               0          6          -
    % Hit:                                      100.00%        100          -
    Auto, Default and User Defined Bins:
        bin cross_cin_arith                        4599          1          -    Covered
        bin <Bins_bitwise[XOR],Bins_Cin>           2202          1          -    Covered
        bin <Bins_shift[ROTATE],Bins_Cin>          2144          1          -    Covered
        bin <Bins_trans,Bins_Cin>                     1          1          -    Covered
        bin <Bins_bitwise[OR],Bins_Cin>            2240          1          -    Covered
        bin <Bins_shift[SHIFT],Bins_Cin>           2238          1          -    Covered
Cross ALU_cross3                                100.00%        100          -    Covered
    covered/total bins:                               7          7          -
    missing/total bins:                               0          7          -
    % Hit:                                      100.00%        100          -
    Auto, Default and User Defined Bins:
        bin cross_serial_shift                     4382          1          -    Covered
        bin cross_shift_direction                  4382          1          -    Covered
```

```
                                                  64          1          -    Covered
        bin <data_0,data_walkingones,Bins_bitwise[OR]>
                                                  41          1          -    Covered
        bin <data_walkingones,data_walkingones,Bins_arith[MULT]>
                                                  21          1          -    Covered
        bin <data_walkingones,data_walkingones,Bins_shift[ROTATE]>
                                                 134          1          -    Covered
        bin <data_walkingones,data_walkingones,Bins_arith[ADD]>
                                                  77          1          -    Covered
        bin <data_walkingones,data_walkingones,Bins_shift[SHIFT]>
                                                 145          1          -    Covered
        bin <data_walkingones,data_max,Bins_arith[MULT]>
                                                  28          1          -    Covered
        bin <data_walkingones,data_max,Bins_shift[ROTATE]>
                                                  60          1          -    Covered
        bin <data_walkingones,data_max,Bins_arith[ADD]>
                                                  42          1          -    Covered
        bin <data_walkingones,data_max,Bins_shift[SHIFT]>
                                                  86          1          -    Covered
        bin <data_walkingones,data_min,Bins_arith[MULT]>
                                                  21          1          -    Covered
        bin <data_walkingones,data_min,Bins_shift[ROTATE]>
                                                  53          1          -    Covered
        bin <data_walkingones,data_min,Bins_arith[ADD]>
                                                  49          1          -    Covered
        bin <data_walkingones,data_min,Bins_shift[SHIFT]>
                                                  83          1          -    Covered
        bin <data_walkingones,data_0,Bins_arith[MULT]>
                                                  70          1          -    Covered
        bin <data_walkingones,data_0,Bins_shift[ROTATE]>
                                                  69          1          -    Covered
        bin <data_walkingones,data_0,Bins_arith[ADD]>
                                                  42          1          -    Covered
        bin <data_walkingones,data_0,Bins_shift[SHIFT]>
                                                  48          1          -    Covered
        bin <data_min,data_walkingones,Bins_arith[MULT]>
                                                  56          1          -    Covered
        bin <data_min,data_walkingones,Bins_shift[ROTATE]>
                                                  76          1          -    Covered
        bin <data_min,data_walkingones,Bins_arith[ADD]>
                                                  14          1          -    Covered
        bin <data_min,data_walkingones,Bins_shift[SHIFT]>
                                                  71          1          -    Covered
        bin <data_max,data_walkingones,Bins_arith[MULT]>
                                                  77          1          -    Covered
        bin <data_max,data_walkingones,Bins_shift[ROTATE]>
                                                  76          1          -    Covered
        bin <data_max,data_walkingones,Bins_arith[ADD]>
                                                  42          1          -    Covered
        bin <data_max,data_walkingones,Bins_shift[SHIFT]>
                                                  75          1          -    Covered
        bin <data_0,data_walkingones,Bins_arith[MULT]>
                                                  49          1          -    Covered
        bin <data_0,data_walkingones,Bins_shift[ROTATE]>
                                                  48          1          -    Covered
        bin <data_0,data_walkingones,Bins_arith[ADD]>
                                                  42          1          -    Covered
        bin <data_0,data_walkingones,Bins_shift[SHIFT]>
                                                  47          1          -    Covered

    Illegal and Ignore Bins:
        ignore_bin ignore_trans_opcode             0                     -    ZERO
        ignore_bin ignore_ab_arith              1259                     -    Occurred
Cross ALU_cross2                             100.00%        100          -    Covered
    covered/total bins:                            6          6          -
    missing/total bins:                            0          6          -
    % Hit:                                   100.00%        100          -
    Auto, Default and User Defined Bins:
        bin cross_cin_arith                     4599          1          -    Covered
        bin <Bins_bitwise[XOR],Bins_Cin>        2202          1          -    Covered
        bin <Bins_shift[ROTATE],Bins_Cin>       2144          1          -    Covered
        bin <Bins_trans,Bins_Cin>                  1          1          -    Covered
        bin <Bins_bitwise[OR],Bins_Cin>         2240          1          -    Covered
        bin <Bins_shift[SHIFT],Bins_Cin>        2238          1          -    Covered
Cross ALU_cross3                             100.00%        100          -    Covered
    covered/total bins:                            7          7          -
    missing/total bins:                            0          7          -
    % Hit:                                   100.00%        100          -
    Auto, Default and User Defined Bins:
        bin cross_serial_shift                  4382          1          -    Covered
        bin cross_shift_direction               4382          1          -    Covered
```

```
            bin <Bins_trans,Bins_serial_in,Bins_Direction>
                                                      1          1          -    Covered
            bin <Bins_bitwise[XOR],Bins_serial_in,Bins_Direction>
                                                   2202          1          -    Covered
            bin <Bins_bitwise[OR],Bins_serial_in,Bins_Direction>
                                                   2240          1          -    Covered
            bin <Bins_arith[MULT],Bins_serial_in,Bins_Direction>
                                                   2390          1          -    Covered
            bin <Bins_arith[ADD],Bins_serial_in,Bins_Direction>
                                                   2209          1          -    Covered
    Cross ALU_cross4                             100.00%        100          -    Covered
        covered/total bins:                           30         30          -
        missing/total bins:                            0         30          -
        % Hit:                                   100.00%        100          -
        Auto, Default and User Defined Bins:
            bin cross_bitwise_redA                   149          1          -    Covered
            bin cross_bitwise_redB                   105          1          -    Covered
            bin <data_walkingones,data_walkingones,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                   139          1          -    Covered
            bin <data_min,data_walkingones,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    61          1          -    Covered
            bin <data_walkingones,data_walkingones,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                   131          1          -    Covered
            bin <data_min,data_walkingones,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    69          1          -    Covered
            bin <data_max,data_walkingones,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    44          1          -    Covered
            bin <data_max,data_walkingones,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    74          1          -    Covered
            bin <data_walkingones,data_min,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    63          1          -    Covered
            bin <data_max,data_min,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    41          1          -    Covered
            bin <data_min,data_min,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    54          1          -    Covered
            bin <data_0,data_min,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    45          1          -    Covered
            bin <data_walkingones,data_min,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    82          1          -    Covered
            bin <data_max,data_min,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    29          1          -    Covered
            bin <data_min,data_min,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    25          1          -    Covered
            bin <data_0,data_min,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    46          1          -    Covered
            bin <data_walkingones,data_max,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    78          1          -    Covered
            bin <data_max,data_max,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    23          1          -    Covered
            bin <data_min,data_max,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    24          1          -    Covered
            bin <data_0,data_max,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    24          1          -    Covered
            bin <data_walkingones,data_max,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    72          1          -    Covered
            bin <data_max,data_max,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    36          1          -    Covered
            bin <data_min,data_max,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    50          1          -    Covered
            bin <data_0,data_max,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    26          1          -    Covered
            bin <data_min,data_0,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    21          1          -    Covered
            bin <data_min,data_0,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    29          1          -    Covered
            bin <data_max,data_0,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    25          1          -    Covered
            bin <data_0,data_0,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    27          1          -    Covered
            bin <data_max,data_0,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    41          1          -    Covered
            bin <data_0,data_0,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    24          1          -    Covered
        Illegal and Ignore Bins:
            illegal_bin cross_red_B_not_bitwise    4839                     -    Occurred
            illegal_bin cross_red_A_not_bitwise    4839                     -    Occurred

COVERGROUP COVERAGE:
--------------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status
```

```
COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------
 TYPE /pck/Z/cg                                   100.00%        100          -    Covered
    covered/total bins:                               106        106          -
    missing/total bins:                                 0        106          -
    % Hit:                                        100.00%        100          -
    Coverpoint A_cp                               100.00%        100          -    Covered
        covered/total bins:                             4          4          -
        missing/total bins:                             0          4          -
        % Hit:                                    100.00%        100          -
    Coverpoint B_cp                               100.00%        100          -    Covered
        covered/total bins:                             4          4          -
        missing/total bins:                             0          4          -
        % Hit:                                    100.00%        100          -
    Coverpoint ALU_cp                             100.00%        100          -    Covered
        covered/total bins:                             7          7          -
        missing/total bins:                             0          7          -
        % Hit:                                    100.00%        100          -
    Coverpoint red_A_cp                           100.00%        100          -    Covered
        covered/total bins:                             1          1          -
        missing/total bins:                             0          1          -
        % Hit:                                    100.00%        100          -
    Coverpoint red_B_cp                           100.00%        100          -    Covered
        covered/total bins:                             1          1          -
        missing/total bins:                             0          1          -
        % Hit:                                    100.00%        100          -
    Coverpoint cin_cp                             100.00%        100          -    Covered
        covered/total bins:                             1          1          -
        missing/total bins:                             0          1          -
        % Hit:                                    100.00%        100          -
    Coverpoint serial_in_cp                       100.00%        100          -    Covered
        covered/total bins:                             1          1          -
        missing/total bins:                             0          1          -
        % Hit:                                    100.00%        100          -
    Coverpoint direction_cp                       100.00%        100          -    Covered
        covered/total bins:                             1          1          -
        missing/total bins:                             0          1          -
        % Hit:                                    100.00%        100          -
    Cross ALU_cross1                              100.00%        100          -    Covered
        covered/total bins:                            43         43          -
        missing/total bins:                             0         43          -
        % Hit:                                    100.00%        100          -
    Cross ALU_cross2                              100.00%        100          -    Covered
        covered/total bins:                             6          6          -
        missing/total bins:                             0          6          -
        % Hit:                                    100.00%        100          -
    Cross ALU_cross3                              100.00%        100          -    Covered
        covered/total bins:                             7          7          -
        missing/total bins:                             0          7          -
        % Hit:                                    100.00%        100          -
    Cross ALU_cross4                              100.00%        100          -    Covered
        covered/total bins:                            30         30          -
        missing/total bins:                             0         30          -
        % Hit:                                    100.00%        100          -
 Covergroup instance \/pck::Z::cg                 100.00%        100          -    Covered
    covered/total bins:                               106        106          -
    missing/total bins:                                 0        106          -
    % Hit:                                        100.00%        100          -
    Coverpoint A_cp                               100.00%        100          -    Covered
        covered/total bins:                             4          4          -
        missing/total bins:                             0          4          -
        % Hit:                                    100.00%        100          -
        bin data_0                                   3913          1          -    Covered
        bin data_max                                 1928          1          -    Covered
        bin data_min                                 1761          1          -    Covered
        bin data_walkingones                         3529          1          -    Covered
        default bin data_default                     5231                     -    Occurred
    Coverpoint B_cp                               100.00%        100          -    Covered
        covered/total bins:                             4          4          -
        missing/total bins:                             0          4          -
        % Hit:                                    100.00%        100          -
        bin data_0                                   3964          1          -    Covered
        bin data_max                                 1739          1          -    Covered
        bin data_min                                 1706          1          -    Covered
        bin data_walkingones                         3321          1          -    Covered
        default bin data_default                     5632                     -    Occurred
    Coverpoint ALU_cp                             100.00%        100          -    Covered
```

```
    covered/total bins:                    7          7          -
    missing/total bins:                    0          7          -
    % Hit:                            100.00%        100         -
    illegal_bin Bins_invalid               2939                  -    Occurred
    bin Bins_shift[SHIFT]                  2238          1       -    Covered
    bin Bins_shift[ROTATE]                 2144          1       -    Covered
    bin Bins_arith[ADD]                    2209          1       -    Covered
    bin Bins_arith[MULT]                   2390          1       -    Covered
    bin Bins_bitwise[OR]                   2240          1       -    Covered
    bin Bins_bitwise[XOR]                  2202          1       -    Covered
    bin Bins_trans                            1          1       -    Covered
Coverpoint red_A_cp                       100.00%        100         -    Covered
    covered/total bins:                       1          1       -
    missing/total bins:                       0          1       -
    % Hit:                            100.00%        100         -
    bin Bins_red_A                        16362          1       -    Covered
Coverpoint red_B_cp                       100.00%        100         -    Covered
    covered/total bins:                       1          1       -
    missing/total bins:                       0          1       -
    % Hit:                            100.00%        100         -
    bin Bins_red_B                        16362          1       -    Covered
Coverpoint cin_cp                         100.00%        100         -    Covered
    covered/total bins:                       1          1       -
    missing/total bins:                       0          1       -
    % Hit:                            100.00%        100         -
    bin Bins_Cin                          16362          1       -    Covered
Coverpoint serial_in_cp                   100.00%        100         -    Covered
    covered/total bins:                       1          1       -
    missing/total bins:                       0          1       -
    % Hit:                            100.00%        100         -
    bin Bins_serial_in                    16362          1       -    Covered
Coverpoint direction_cp                   100.00%        100         -    Covered
    covered/total bins:                       1          1       -
    missing/total bins:                       0          1       -
    % Hit:                            100.00%        100         -
    bin Bins_Direction                    16362          1       -    Covered
Cross ALU_cross1                          100.00%        100         -    Covered
    covered/total bins:                      43         43       -
    missing/total bins:                       0         43       -
    % Hit:                            100.00%        100         -
    Auto, Default and User Defined Bins:
        bin cross_ab_arith                 2469          1       -    Covered
        bin <data_walkingones,data_walkingones,Bins_bitwise[XOR]>
                                            139          1       -    Covered
        bin <data_walkingones,data_walkingones,Bins_bitwise[OR]>
                                            131          1       -    Covered
        bin <data_walkingones,data_max,Bins_bitwise[XOR]>
                                             78          1       -    Covered
        bin <data_walkingones,data_max,Bins_bitwise[OR]>
                                             72          1       -    Covered
        bin <data_walkingones,data_min,Bins_bitwise[XOR]>
                                             63          1       -    Covered
        bin <data_walkingones,data_min,Bins_bitwise[OR]>
                                             82          1       -    Covered
        bin <data_walkingones,data_0,Bins_bitwise[XOR]>
                                             75          1       -    Covered
        bin <data_walkingones,data_0,Bins_bitwise[OR]>
                                             74          1       -    Covered
        bin <data_min,data_walkingones,Bins_bitwise[XOR]>
                                             61          1       -    Covered
        bin <data_min,data_walkingones,Bins_bitwise[OR]>
                                             69          1       -    Covered
        bin <data_max,data_walkingones,Bins_bitwise[XOR]>
                                             44          1       -    Covered
        bin <data_max,data_walkingones,Bins_bitwise[OR]>
                                             74          1       -    Covered
        bin <data_0,data_walkingones,Bins_bitwise[XOR]>
                                             64          1       -    Covered
        bin <data_0,data_walkingones,Bins_bitwise[OR]>
                                             41          1       -    Covered
        bin <data_walkingones,data_walkingones,Bins_arith[MULT]>
                                             21          1       -    Covered
        bin <data_walkingones,data_walkingones,Bins_shift[ROTATE]>
                                            134          1       -    Covered
        bin <data_walkingones,data_walkingones,Bins_arith[ADD]>
                                             77          1       -    Covered
        bin <data_walkingones,data_walkingones,Bins_shift[SHIFT]>
                                            145          1       -    Covered
        bin <data_walkingones,data_max,Bins_arith[MULT]>
                                             28          1       -    Covered
```

```
        bin <data_walkingones,data_max,Bins_shift[ROTATE]>
                                                    60          1          -    Covered
        bin <data_walkingones,data_max,Bins_arith[ADD]>
                                                    42          1          -    Covered
        bin <data_walkingones,data_max,Bins_shift[SHIFT]>
                                                    86          1          -    Covered
        bin <data_walkingones,data_min,Bins_arith[MULT]>
                                                    21          1          -    Covered
        bin <data_walkingones,data_min,Bins_shift[ROTATE]>
                                                    53          1          -    Covered
        bin <data_walkingones,data_min,Bins_arith[ADD]>
                                                    49          1          -    Covered
        bin <data_walkingones,data_min,Bins_shift[SHIFT]>
                                                    83          1          -    Covered
        bin <data_walkingones,data_0,Bins_arith[MULT]>
                                                    70          1          -    Covered
        bin <data_walkingones,data_0,Bins_shift[ROTATE]>
                                                    69          1          -    Covered
        bin <data_walkingones,data_0,Bins_arith[ADD]>
                                                    42          1          -    Covered
        bin <data_walkingones,data_0,Bins_shift[SHIFT]>
                                                    48          1          -    Covered
        bin <data_min,data_walkingones,Bins_arith[MULT]>
                                                    56          1          -    Covered
        bin <data_min,data_walkingones,Bins_shift[ROTATE]>
                                                    76          1          -    Covered
        bin <data_min,data_walkingones,Bins_arith[ADD]>
                                                    14          1          -    Covered
        bin <data_min,data_walkingones,Bins_shift[SHIFT]>
                                                    71          1          -    Covered
        bin <data_max,data_walkingones,Bins_arith[MULT]>
                                                    77          1          -    Covered
        bin <data_max,data_walkingones,Bins_shift[ROTATE]>
                                                    76          1          -    Covered
        bin <data_max,data_walkingones,Bins_arith[ADD]>
                                                    42          1          -    Covered
        bin <data_max,data_walkingones,Bins_shift[SHIFT]>
                                                    75          1          -    Covered
        bin <data_0,data_walkingones,Bins_arith[MULT]>
                                                    49          1          -    Covered
        bin <data_0,data_walkingones,Bins_shift[ROTATE]>
                                                    48          1          -    Covered
        bin <data_0,data_walkingones,Bins_arith[ADD]>
                                                    42          1          -    Covered
        bin <data_0,data_walkingones,Bins_shift[SHIFT]>
                                                    47          1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin ignore_trans_opcode               0                     -    ZERO
        ignore_bin ignore_ab_arith                1259                     -    Occurred
Cross ALU_cross2                                100.00%        100          -    Covered
    covered/total bins:                               6          6          -
    missing/total bins:                               0          6          -
    % Hit:                                      100.00%        100          -
    Auto, Default and User Defined Bins:
        bin cross_cin_arith                       4599          1          -    Covered
        bin <Bins_bitwise[XOR],Bins_Cin>          2202          1          -    Covered
        bin <Bins_shift[ROTATE],Bins_Cin>         2144          1          -    Covered
        bin <Bins_trans,Bins_Cin>                    1          1          -    Covered
        bin <Bins_bitwise[OR],Bins_Cin>           2240          1          -    Covered
        bin <Bins_shift[SHIFT],Bins_Cin>          2238          1          -    Covered
Cross ALU_cross3                                100.00%        100          -    Covered
    covered/total bins:                               7          7          -
    missing/total bins:                               0          7          -
    % Hit:                                      100.00%        100          -
    Auto, Default and User Defined Bins:
        bin cross_serial_shift                    4382          1          -    Covered
        bin cross_shift_direction                 4382          1          -    Covered
        bin <Bins_trans,Bins_serial_in,Bins_Direction>
                                                     1          1          -    Covered
        bin <Bins_bitwise[XOR],Bins_serial_in,Bins_Direction>
                                                  2202          1          -    Covered
        bin <Bins_bitwise[OR],Bins_serial_in,Bins_Direction>
                                                  2240          1          -    Covered
        bin <Bins_arith[MULT],Bins_serial_in,Bins_Direction>
                                                  2390          1          -    Covered
        bin <Bins_arith[ADD],Bins_serial_in,Bins_Direction>
                                                  2209          1          -    Covered
Cross ALU_cross4                                100.00%        100          -    Covered
    covered/total bins:                              30         30          -
    missing/total bins:                               0         30          -
```

```
            bin <Bins_bitwise[XOR],Bins_serial_in,Bins_Direction>
                                                  2202          1          -    Covered
            bin <Bins_bitwise[OR],Bins_serial_in,Bins_Direction>
                                                  2240          1          -    Covered
            bin <Bins_arith[MULT],Bins_serial_in,Bins_Direction>
                                                  2390          1          -    Covered
            bin <Bins_arith[ADD],Bins_serial_in,Bins_Direction>
                                                  2209          1          -    Covered
    Cross ALU_cross4                            100.00%        100          -    Covered
        covered/total bins:                          30         30          -
        missing/total bins:                           0         30          -
        % Hit:                                  100.00%        100          -
        Auto, Default and User Defined Bins:
            bin cross_bitwise_redA                  149          1          -    Covered
            bin cross_bitwise_redB                  105          1          -    Covered
            bin <data_walkingones,data_walkingones,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                    139          1          -    Covered
            bin <data_min,data_walkingones,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     61          1          -    Covered
            bin <data_walkingones,data_walkingones,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                    131          1          -    Covered
            bin <data_min,data_walkingones,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     69          1          -    Covered
            bin <data_max,data_walkingones,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     44          1          -    Covered
            bin <data_max,data_walkingones,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     74          1          -    Covered
            bin <data_walkingones,data_min,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     63          1          -    Covered
            bin <data_max,data_min,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     41          1          -    Covered
            bin <data_min,data_min,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     54          1          -    Covered
            bin <data_0,data_min,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     45          1          -    Covered
            bin <data_walkingones,data_min,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     82          1          -    Covered
            bin <data_max,data_min,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     29          1          -    Covered
            bin <data_min,data_min,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     25          1          -    Covered
            bin <data_0,data_min,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     46          1          -    Covered
            bin <data_walkingones,data_max,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     78          1          -    Covered
            bin <data_max,data_max,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     23          1          -    Covered
            bin <data_min,data_max,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     24          1          -    Covered
            bin <data_0,data_max,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     24          1          -    Covered
            bin <data_walkingones,data_max,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     72          1          -    Covered
            bin <data_max,data_max,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     36          1          -    Covered
            bin <data_min,data_max,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     50          1          -    Covered
            bin <data_0,data_max,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     26          1          -    Covered
            bin <data_min,data_0,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     21          1          -    Covered
            bin <data_min,data_0,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     29          1          -    Covered
            bin <data_max,data_0,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     25          1          -    Covered
            bin <data_0,data_0,Bins_bitwise[XOR],Bins_red_A,Bins_red_B>
                                                     27          1          -    Covered
            bin <data_max,data_0,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     41          1          -    Covered
            bin <data_0,data_0,Bins_bitwise[OR],Bins_red_A,Bins_red_B>
                                                     24          1          -    Covered
        Illegal and Ignore Bins:
            illegal_bin cross_red_B_not_bitwise   4839                     -    Occurred
            illegal_bin cross_red_A_not_bitwise   4839                     -    Occurred

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 100.00%
```

X. Coverage Report

```
Coverage Report by instance with details

================================================================================
=== Instance: /\ALSU_TB#DUT
=== Design Unit: work.ALSU
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        32        32         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\ALSU_TB#DUT

    Line          Item                      Count     Source
    ----          ----                      -----     ------
  File ALSU.sv
------------------------------------IF Branch------------------------------------
    25                                      57411     Count coming in to IF
    25              1                       19406
    36              1                       38005
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    52                                      73450     Count coming in to IF
    52              1                       30396
    54              1                       43054
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                      43054     Count coming in to IF
    55              1                       20642
    57              1                       22412
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    64                                      40383     Count coming in to IF
    64              1                        6888
    67              1                       33495
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                      33495     Count coming in to IF
    68              1                       14570
    70              1                        2052
    72              1                        2736
    74              1                        2711
    76              1                       11426
Branch totals: 5 hits of 5 branches = 100.00%

----------------------------------CASE Branch----------------------------------
    77                                      11426     Count coming in to CASE
    78              1                        6246
    88              1                        2688
    98              1                         632
    103             1                         594
    104             1                         646
    110             1                         618
    116             1                           2
Branch totals: 7 hits of 7 branches = 100.00%

------------------------------------IF Branch------------------------------------
    79                                       6246     Count coming in to IF
    79              1                         215
    81              1                         188
    83              1                         204
    85              1                        5639
Branch totals: 4 hits of 4 branches = 100.00%

------------------------------------IF Branch------------------------------------
    89                                       2688     Count coming in to IF
    89              1                         172
    91              1                         180
    93              1                         158
    95              1                        2178
Branch totals: 4 hits of 4 branches = 100.00%

------------------------------------IF Branch------------------------------------
    105                                       646     Count coming in to IF
    105             1                         327
    107             1                         319
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    111                                       618     Count coming in to IF
    111             1                         308
    113             1                         310
Branch totals: 2 hits of 2 branches = 100.00%
```

```
Condition Coverage:
    Enabled Coverage              Bins    Covered    Misses  Coverage
    ----------------              ----    -------    ------  --------
    Conditions                       6          6         0   100.00%

================================Condition Details================================

Condition Coverage for instance /\ALSU_TB#DUT  --

  File ALSU.sv
----------------Focused Condition View-------------------
Line       70 Item    1  (bypass_A_reg && bypass_B_reg)
Condition totals: 2 of 2 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
    ----------  --------  ----------------------  --------------
  bypass_A_reg         Y
  bypass_B_reg         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  --------------------------
  Row   1:          1  bypass_A_reg_0        -
  Row   2:          1  bypass_A_reg_1        bypass_B_reg
  Row   3:          1  bypass_B_reg_0        bypass_A_reg
  Row   4:          1  bypass_B_reg_1        bypass_A_reg

----------------Focused Condition View-------------------
Line       79 Item    1  (red_op_A_reg && red_op_B_reg)
Condition totals: 2 of 2 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
    ----------  --------  ----------------------  --------------
  red_op_A_reg         Y
  red_op_B_reg         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  --------------------------
  Row   1:          1  red_op_A_reg_0        -
  Row   2:          1  red_op_A_reg_1        red_op_B_reg
  Row   3:          1  red_op_B_reg_0        red_op_A_reg
  Row   4:          1  red_op_B_reg_1        red_op_A_reg

----------------Focused Condition View-------------------
Line       89 Item    1  (red_op_A_reg && red_op_B_reg)
Condition totals: 2 of 2 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
    ----------  --------  ----------------------  --------------
  red_op_A_reg         Y
  red_op_B_reg         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  --------------------------
  Row   1:          1  red_op_A_reg_0        -
  Row   2:          1  red_op_A_reg_1        red_op_B_reg
  Row   3:          1  red_op_B_reg_0        red_op_A_reg
  Row   4:          1  red_op_B_reg_1        red_op_A_reg


Expression Coverage:
    Enabled Coverage              Bins    Covered    Misses  Coverage
    ----------------              ----    -------    ------  --------
    Expressions                      8          8         0   100.00%

================================Expression Details================================

Expression Coverage for instance /\ALSU_TB#DUT  --

  File ALSU.sv
----------------Focused Expression View-----------------
Line       19 Item    1  ((red_op_A_reg | red_op_B_reg) & (opcode_reg[1] | opcode_reg[2]))
Expression totals: 4 of 4 input terms covered = 100.00%

     Input Term   Covered  Reason for no coverage   Hint
     ----------  --------  ----------------------  --------------
   red_op_A_reg         Y
   red_op_B_reg         Y
  opcode_reg[1]         Y
  opcode_reg[2]         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  --------------------------
  Row   1:          1  red_op_A_reg_0        ((opcode_reg[1] | opcode_reg[2]) && ~red_op_B_reg)
  Row   2:          1  red_op_A_reg_1        ((opcode_reg[1] | opcode_reg[2]) && ~red_op_B_reg)
  Row   3:          1  red_op_B_reg_0        ((opcode_reg[1] | opcode_reg[2]) && ~red_op_A_reg)
  Row   4:          1  red_op_B_reg_1        ((opcode_reg[1] | opcode_reg[2]) && ~red_op_A_reg)
  Row   5:          1  opcode_reg[1]_0       ((red_op_A_reg | red_op_B_reg) && ~opcode_reg[2])
  Row   6:          1  opcode_reg[1]_1       ((red_op_A_reg | red_op_B_reg) && ~opcode_reg[2])
  Row   7:          1  opcode_reg[2]_0       ((red_op_A_reg | red_op_B_reg) && ~opcode_reg[1])
  Row   8:          1  opcode_reg[2]_1       ((red_op_A_reg | red_op_B_reg) && ~opcode_reg[1])

----------------Focused Expression View-----------------
Line       20 Item    1  (opcode_reg[1] & opcode_reg[2])
Expression totals: 2 of 2 input terms covered = 100.00%
```

```
      Input Term   Covered  Reason for no coverage   Hint
     -----------  --------  ----------------------  --------------
   opcode_reg[1]         Y
   opcode_reg[2]         Y

      Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
   Row   1:          1  opcode_reg[1]_0       opcode_reg[2]
   Row   2:          1  opcode_reg[1]_1       opcode_reg[2]
   Row   3:          1  opcode_reg[2]_0       opcode_reg[1]
   Row   4:          1  opcode_reg[2]_1       opcode_reg[1]

----------------Focused Expression View-----------------
Line       21 Item    1  (invalid_red_op | invalid_opcode)
Expression totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
     -----------  --------  ----------------------  --------------
   invalid_red_op        Y
   invalid_opcode        Y

      Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
   Row   1:          1  invalid_red_op_0      ~invalid_opcode
   Row   2:          1  invalid_red_op_1      ~invalid_opcode
   Row   3:          1  invalid_opcode_0      ~invalid_red_op
   Row   4:          1  invalid_opcode_1      ~invalid_red_op


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      49        49         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\ALSU_TB#DUT  --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File ALSU.sv
    19              1                      26320
    20              1                      24812
    21              1                      13629
    24              1                      57411
    26              1                      19406
    27              1                      19406
    28              1                      19406
    29              1                      19406
    30              1                      19406
    31              1                      19406
    32              1                      19406
    33              1                      19406
    34              1                      19406
    35              1                      19406
    37              1                      38005
    38              1                      38005
    39              1                      38005
    40              1                      38005
    41              1                      38005
    42              1                      38005
    43              1                      38005
    44              1                      38005
    45              1                      38005
    46              1                      38005
    51              1                      73450
    53              1                      30396
    56              1                      20642
    58              1                      22412
    63              1                      40383
    65              1                       6888
    69              1                      14570
    71              1                       2052
    73              1                       2736
    75              1                       2711
    80              1                        215
    82              1                        188
    84              1                        204
    86              1                       5639
    90              1                        172
    92              1                        180
    94              1                        158
    96              1                       2178
    100             1                        632
    103             1                        594
    106             1                        327
    108             1                        319
    112             1                        308
    114             1                        310
    116             1                          2
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                        120       120         0   100.00%
```

```
    116             1                       2
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                        120       120         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\ALSU_TB#DUT  --

                                          Node      1H->0L      0L->1H  "Coverage"
                                          ----------------------------------------
                                          A[0-2]           1           1      100.00
                                       A_reg[2-0]          1           1      100.00
                                          B[0-2]           1           1      100.00
                                       B_reg[2-0]          1           1      100.00
                                        bypass_A           1           1      100.00
                                    bypass_A_reg           1           1      100.00
                                        bypass_B           1           1      100.00
                                    bypass_B_reg           1           1      100.00
                                             cin           1           1      100.00
                                         cin_reg           1           1      100.00
                                             clk           1           1      100.00
                                       direction           1           1      100.00
                                   direction_reg           1           1      100.00
                                         invalid           1           1      100.00
                                  invalid_opcode           1           1      100.00
                                  invalid_red_op           1           1      100.00
                                        leds[15-0]         1           1      100.00
                                      opcode[0-2]          1           1      100.00
                                   opcode_reg[2-0]         1           1      100.00
                                         out[5-0]          1           1      100.00
                                        red_op_A           1           1      100.00
                                    red_op_A_reg           1           1      100.00
                                        red_op_B           1           1      100.00
                                    red_op_B_reg           1           1      100.00
                                             rst           1           1      100.00
                                       serial_in           1           1      100.00
                                   serial_in_reg           1           1      100.00

Total Node Count     =         60
Toggled Node Count   =         60
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (120 of 120 bins)


Total Coverage By Instance (filtered view): 100.00%
```

Question 2

Q2. Write assertions for the following:

1) Write assert property statement, if signal a is high in a positive edge of a clock then signal b should be high after 2 clock cycles
2) Write assert property statement, If signal a is high and signal b is high then signal c should be high 1 to 3 clock cycle later
3) Write a sequence s11b, after 2 positive clock edges, signal b should be low 4) Write a property for the following specs:
    - 3-to-8 decoder output **Y**
        i. At each positive edge of clock, Y output must be only one bit high.
    - 4-to-2 priority encoder output **valid** (refer to assignment 1)
        i. At each positive edge of clock, if the input D bits are low then after one clock cycle, output valid must be low.

```
1  //QUESTION 2
2
3  //1
4  assert property (@(posedge clk) (a |-> ##2 b));
5  assert property (@(posedge clk)(a |=> ##1 b));
6
7  //2
8  assert property (@(posedge clk) (a && b) |-> ##[1:3] c);
9
10 //3
11 sequence s11b;
12 (repeat(2)@(posedge clk) (b == 0));
13 endsequence
14
15 //4-a
16  property 4a (@(posedge clk) $onehot(y_out)); endproperty
17
18 //4-b
19 property 4b (@(posedge clk) (d==0) |=> (output_valid==0));endproperty
```

Question 3

Q3. Modify the testbenches for the **priority encoder** and the **ALU** in assignment 1 adding assertions making sure that all outputs are correct in all cases instead of using a task for checking the output. Generate code coverage and make sure to get 100% code and assertion coverage.

a) ALU

I. Verification plan

Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check
ALU_1	When reset is asserted, output C should hold its previous value or reset to 0 based on the ALU design.	Directed at the start of the simulation. Randomized reset values with reset high at least 50% of the time.	Coverage of reset high and low states with various combinations of A, B, and Opcode.	A checker in the testbench ensures C is reset or holds the previous value when reset is high.
ALU_2	When reset is deasserted, perform an addition operation when Opcode == Add.	Randomized values of A, B, and Opcode. reset deasserted.	Coverage of all possible values of A, B, and Opcode = Add.	Property Addition_Prop ensures that C = A + B when Opcode == Add.
ALU_3	Perform subtraction operation when Opcode == Sub.	Randomized values of A, B, and Opcode with a focus on Opcode == Sub.	Coverage of all possible values of A, B, and Opcode = Sub.	Property Subtraction_Prop ensures that C = A - B when Opcode == Sub.
ALU_4	Perform NOT operation on A when Opcode == Not_A.	Randomized values of A and Opcode with a focus on Opcode == Not_A.	Coverage for all values of A and Opcode = Not_A.	Property Not_A_Prop ensures that C = ~A when Opcode == Not_A.
ALU_5	Perform reduction OR operation on B when Opcode == ReductionOR_B.	Randomized values of B and Opcode with a focus on Opcode == ReductionOR_B.	Coverage for all values of B and Opcode = ReductionOR_B.	Property ReductionOR_B_Prop ensures that `C =
ALU_6	Ensure correct functionality under randomized combinations of A, B, and Opcode.	Fully randomized A, B, Opcode, and reset for 50 cycles.	Coverage for all possible combinations of inputs and control signals.	A checker in the testbench prints the result for each combination to verify correctness manually.

II. RTL Design

```
module ALU (
    input  clk,
    input  reset,
    input  [1:0] Opcode,    // The opcode
    input  signed [3:0] A, // Input data A in 2's complement
    input  signed [3:0] B, // Input data B in 2's complement
    output reg signed [4:0] C // ALU output in 2's complement
        );

    reg signed [4:0]      Alu_out; // ALU output in 2's complement

    localparam         Add             = 2'b00; // A + B
    localparam              Sub              = 2'b01; // A - B
    localparam         Not_A      = 2'b10; // ~A
    localparam         ReductionOR_B  = 2'b11; // |B
    // Do the operation
    always @* begin
       case (Opcode)
          Add:            Alu_out = A + B;
          Sub:            Alu_out = A - B;
          Not_A:          Alu_out =~A;
          ReductionOR_B:  Alu_out = |B;
         default:  Alu_out = 5'b0;
       endcase
    end // always @ *
    // Register output C
    always @(posedge clk or posedge reset) begin
       if (reset)
         C <= 5'b0;
       else
         C<= Alu_out;
    end
endmodule
```

III. Package

```
package pck;

typedef enum logic [1:0] {Add , Sub ,Not_A , ReductionOR_B} opcode_e;
class M;
rand bit signed [3: 0] a , b;
rand opcode_e opcode;
rand bit rst;
constraint c_rst {rst dist{0 :/ 90, 1 :/ 10};}
endclass

endpackage
```

IV. Test bench

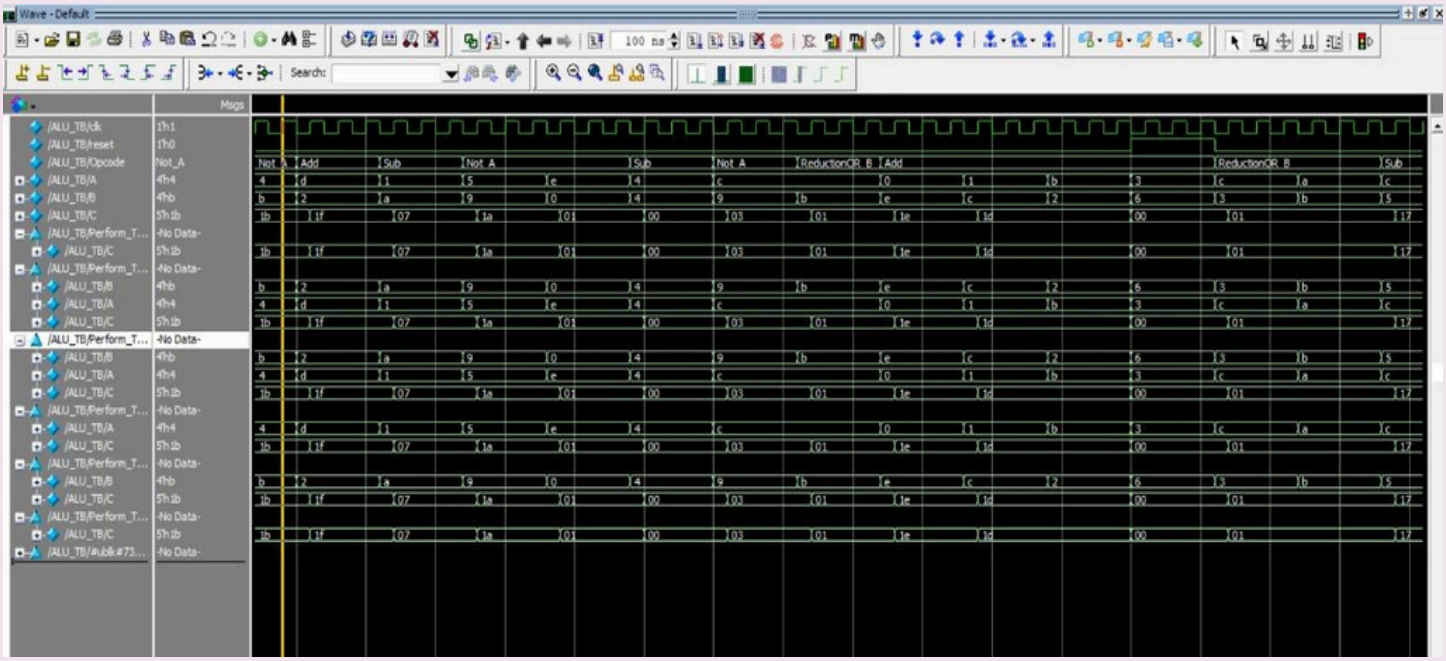
```
import pck::*;
module ALU_TB;
  // Input and output declarations
  logic clk, reset;
  opcode_e Opcode;
  logic signed [3:0] A, B;
  logic signed [4:0] C;
  // Creation of object from class
  M obj;
  // Module Instantiation
  ALU DUT (.*);
  // Clock declaration
  initial begin
      clk = 0;forever #1 clk = ~clk;
  end
  // Testbench initialization
  initial begin
      obj = new();
      reset = 0;
      // Randomized Testing
      repeat (50) begin
      @(negedge clk);
      assert(obj.randomize());
      A = obj.a;
      B = obj.b;
      Opcode = obj.opcode;
      reset = obj.rst;
      @(negedge clk);
      $display("%0t: For Inputs A = %0d, B = %0d, Opcode = %0b, Reset = %0b,Output C = %0d",
      $time, A, B, Opcode, reset, C);
      end
      $stop;
  end
```

```
  property Addition_Prop;
      @(negedge clk) !reset && (Opcode == Add) |-> (C == A + B);
  endproperty
  property Subtraction_Prop;
      @(negedge clk) !reset && (Opcode == Sub) |-> (C == A - B);
  endproperty
  property Not_A_Prop;
      @(negedge clk) !reset && (Opcode == Not_A) |-> (C == ~A);
  endproperty
  property ReductionOR_B_Prop;
      @(negedge clk) !reset && (Opcode == ReductionOR_B) |-> (C == |B);
  endproperty
  assert property (Addition_Prop);
  assert property (Subtraction_Prop);
  assert property (Not_A_Prop);
  assert property (ReductionOR_B_Prop);
  endmodule
```

V. Do file

```
vlib work
vlog ALU.v pck.svh ALU_TB.svh  +cover -covercells
vsim -voptargs=+acc work.ALU_TB -cover
add wave *
coverage save ALU_TB.ucdb -onexit -du work.ALU
run -all
```

VI. Waveform



VII. Coverage Report

```
Coverage Report by instance with details

================================================================================
=== Instance: /ALU_TB/DUT
=== Design Unit: work.ALU
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         6         6         0   100.00%

================================Branch Details================================

Branch Coverage for instance /ALU_TB/DUT

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File ALU.sv
------------------------------------CASE Branch------------------------------------
    18                                        50     Count coming in to CASE
    19              1                         10
    20              1                          8
    21              1                         14
    22              1                         18
Branch totals: 4 hits of 4 branches = 100.00%

------------------------------------IF Branch------------------------------------
    28                                        90     Count coming in to IF
    28              1                          6
    30              1                         84
Branch totals: 2 hits of 2 branches = 100.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       8         8         0   100.00%

================================Statement Details================================

Statement Coverage for instance /ALU_TB/DUT --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File ALU.sv
    17              1                         50
    19              1                         10
    20              1                          8
    21              1                         14
    22              1                         18
    27              1                         90
    29              1                          6
    31              1                         84
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         44        44         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /ALU_TB/DUT --

                                      Node      1H->0L      0L->1H                            "Coverage"
                                      ----------------------------------------------------------------
                                    A[0-3]           1           1                              100.00
                                 Alu_out[4-0]        1           1                              100.00
                                    B[0-3]           1           1                              100.00
                                    C[4-0]           1           1                              100.00
                                 Opcode[0-1]         1           1                              100.00
                                       clk           1           1                              100.00
                                     reset           1           1                              100.00

Total Node Count     =         22
Toggled Node Count   =         22
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (44 of 44 bins)

================================================================================
=== Instance: /ALU_TB
=== Design Unit: work.ALU_TB
================================================================================

Assertion Coverage:
    Assertions                       5         5         0   100.00%
--------------------------------------------------------------------
Name                 File(Line)                   Failure      Pass
                                                  Count        Count
--------------------------------------------------------------------
/ALU_TB/assert__ReductionOR_B_Prop
                     ALU_TB.sv(63)                    0            1
/ALU_TB/assert__Not_A_Prop
                     ALU_TB.sv(62)                    0            1
/ALU_TB/assert__Subtraction_Prop
```

```
----------------------------------------------------------------
/ALU_TB/assert__ReductionOR_B_Prop
                    ALU_TB.sv(63)                    0          1
/ALU_TB/assert__Not_A_Prop
                    ALU_TB.sv(62)                    0          1
/ALU_TB/assert__Subtraction_Prop
                    ALU_TB.sv(61)                    0          1
/ALU_TB/assert__Addition_Prop
                    ALU_TB.sv(60)                    0          1
/ALU_TB/#ublk#73512066#29/immed__31
                    ALU_TB.sv(31)                    0          1
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      15        15         0   100.00%

================================Statement Details================================

Statement Coverage for instance /ALU_TB --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File ALU_TB.sv
    18              1                          1
    19              1                          1
    19              2                        201
    19              3                        200
    24              1                          1
    25              1                          1
    29              1                         50
    30              1                         50
    32              1                         50
    33              1                         50
    34              1                         50
    35              1                         50
    36              1                         50
    37              1                         50
    40              1                          1
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         34        34         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /ALU_TB --

                                       Node      1H->0L      0L->1H                        "Coverage"
                                       ----------------------------------------------------------------
                                      A[3-0]          1           1                             100.00
                                      B[3-0]          1           1                             100.00
                                      C[4-0]          1           1                             100.00
                                      Opcode                ENUM type       Value       Count
                                                                  Add           1      100.00
                                                                  Sub           1      100.00
                                                                Not_A           1      100.00
                                                        ReductionOR_B           3      100.00
                                        clk           1           1                             100.00
                                      reset           1           1                             100.00

Total Node Count     =         19
Toggled Node Count   =         19
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (34 of 34 bins)


ASSERTION RESULTS:
----------------------------------------------------------------
Name                File(Line)                   Failure      Pass
                                                 Count        Count
----------------------------------------------------------------
/ALU_TB/assert__ReductionOR_B_Prop
                    ALU_TB.sv(63)                    0          1
/ALU_TB/assert__Not_A_Prop
                    ALU_TB.sv(62)                    0          1
/ALU_TB/assert__Subtraction_Prop
                    ALU_TB.sv(61)                    0          1
/ALU_TB/assert__Addition_Prop
                    ALU_TB.sv(60)                    0          1
/ALU_TB/#ublk#73512066#29/immed__31
                    ALU_TB.sv(31)                    0          1

Total Coverage By Instance (filtered view): 100.00%
```

b) Priority encode

I. Verification plan

Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check
PE_1	On reset (rst), the output Y should be 0 and valid should be 0.	The testbench applies a reset signal at the start and end of the simulation.	Coverage of rst signal being high and low at different times.	Task checkreset and property p_reset ensure that Y == 0 and valid == 0 during reset.
PE_2	When D = 4'b0000, the output valid should be 0 and Y should be 0.	The testbench directly applies D = 4'b0000 as a test case.	Coverage for the case when no inputs are asserted (D = 4'b0000).	Task checkzerovalid and property p_case_0000 ensure Y == 2'b00 and valid == 0.
PE_3	When D = 4'b1000, the output Y should be 00 and valid should be 1.	The testbench directly applies D = 4'b1000 as a test case.	Coverage for the case when D = 4'b1000.	Task checkresult and property p_case_1000 ensure Y == 2'b00 and valid == 1.
PE_4	When D = 4'b0100, the output Y should be 01 and valid should be 1.	The testbench directly applies D = 4'b0100 as a test case.	Coverage for the case when D = 4'b0100.	Task checkresult and property p_case_0100 ensure Y == 2'b01 and valid == 1.
PE_5	When D = 4'b0010, the output Y should be 10 and valid should be 1.	The testbench directly applies D = 4'b0010 as a test case.	Coverage for the case when D = 4'b0010.	Task checkresult and property p_case_0010 ensure Y == 2'b10 and valid == 1.
PE_6	When D = 4'b0001, the output Y should be 11 and valid should be 1.	The testbench directly applies D = 4'b0001 as a test case.	Coverage for the case when D = 4'b0001.	Task checkresult and property p_case_0001 ensure Y == 2'b11 and valid == 1.
PE_7	If multiple bits of D are high, the output Y should correspond to the highest priority bit and valid should be 1.	Test cases with multiple high bits, such as D = 4'b0110, D = 4'b0011, etc.	Coverage for all combinations of multiple high bits.	Task checkresult ensures that the highest-priority bit wins in multiple high-bit cases.
PE_8	The testbench should cover all valid and invalid cases of input D and validate correct functionality across all clock cycles.	Randomized test cases covering all possible D values and edge cases with the rst signal.	Functional coverage across all possible combinations of D and rst.	Assertions (p_case_*) ensure correct functionality, while the testbench tasks print any errors.

II. RTL Design

```
module priority_enc (
  input  clk,
  input  rst,
  input  [3:0] D,
  output reg [1:0] Y,
  output reg valid
);

always @(posedge clk or posedge rst) begin
  if (rst) begin
    Y <= 2'b00;     // Reset output Y
    valid <= 1'b0;  // Reset valid signal
  end else begin
    // Priority encoding
    casex (D)
      4'b1xxx: Y <= 2'b00; // Highest priority
      4'b01xx: Y <= 2'b01;
      4'b001x: Y <= 2'b10;
      4'b0001: Y <= 2'b11;
      default: Y <= 2'b00; // No valid input
    endcase
    valid <= (|D) ? 1'b1 : 1'b0; // Set valid based on non-zero D
  end
end

endmodule
```

III. Test Bench

```
module PE_TB;
  logic clk, rst;
  logic [3:0] D;
  logic [1:0] Y;
  logic valid;
  integer error_count, correct_count;
  // Instantiate the priority_enc module
  priority_enc test (
    .clk(clk),
    .rst(rst),
    .D(D),
    .Y(Y),
    .valid(valid));
  // Clock generation
  initial begin
    clk = 0;
    forever #5 clk = ~clk; // Clock period of 10 time units
  end
  // Testbench initial block
  initial begin
    error_count = 0;
    correct_count = 0;

    // Apply reset and check
    checkreset;
    // Apply test cases with extended time
    D = 4'b0000; #20; checkzerovalid(0);
    D = 4'b1000; #20; checkresult(2'b00, 1'b1);
    D = 4'b0100; #20; checkresult(2'b01, 1'b1);
    D = 4'b0010; #20; checkresult(2'b10, 1'b1);
    D = 4'b0001; #20; checkresult(2'b11, 1'b1);
    D = 4'b1000; #20; checkresult(2'b00, 1'b1);
    // Additional test cases
    D = 4'b0110; #20; checkresult(2'b01, 1'b1); // Test case where two bits are high
    D = 4'b0011; #20; checkresult(2'b10, 1'b1); // Another case with multiple bits high
    D = 4'b1111; #20; checkresult(2'b00, 1'b1); // All bits are high, higher priority should win
    D = 4'b0101; #20; checkresult(2'b01, 1'b1); // Mixed high bits

    // End simulation
    checkreset;
    $stop;
  end

  // Task for reset check
  task checkreset;
    rst = 1;
    repeat (2) @(negedge clk); // Extend reset for two cycles
    if (Y !== 2'b00 || valid !== 1'b0) begin
      $display("Error during reset: Y = %b, valid = %b at time %0t", Y, valid, $time);
      error_count = error_count + 1;
    end else begin
      correct_count = correct_count + 1;
    end
    rst = 0;
  endtask

  // Task for checking valid signal
  task checkzerovalid;
    input expected_valid;
    @(negedge clk);
    if (valid !== expected_valid) begin
      $display("Error: valid = %b, expected = %b at time %0t", valid, expected_valid, $time);
      error_count = error_count + 1;
    end else begin
      correct_count = correct_count + 1;
    end
  endtask

  // Task for checking output results
  task checkresult;
    input [1:0] expected_Y;
    input expected_valid;
    @(negedge clk);
```

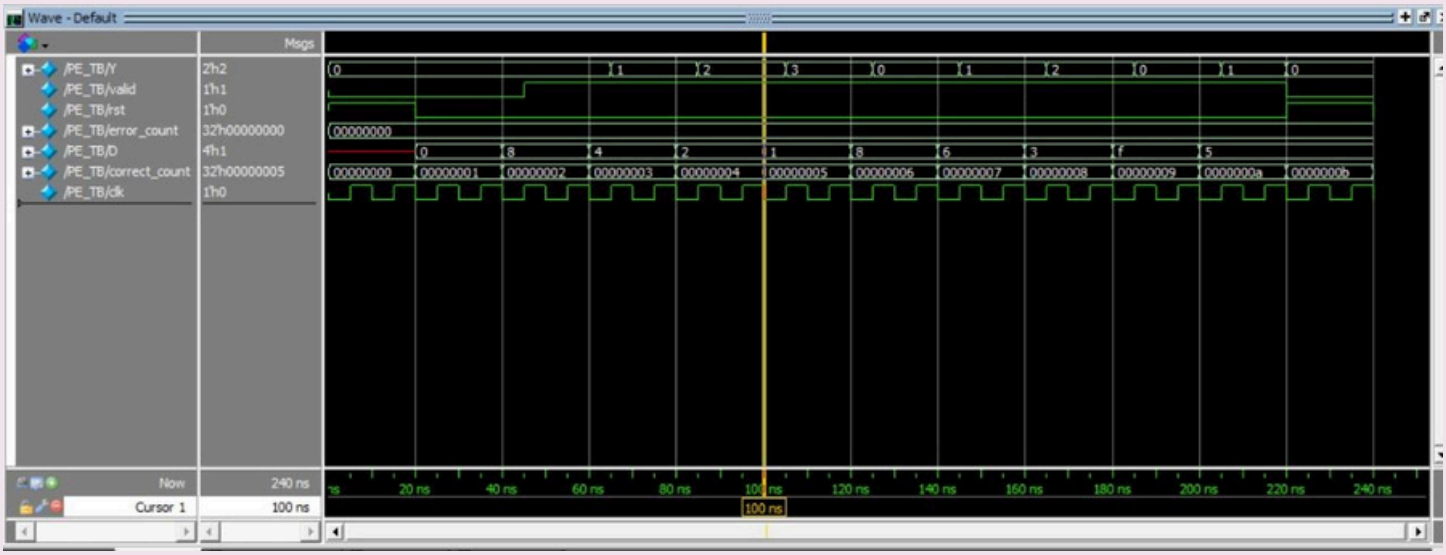
```
    @(negedge clk);
    if (Y !== expected_Y || valid !== expected_valid) begin
    $display("Error: Y = %b, valid = %b, expected Y = %b,
    expected valid = %b at time %0t", Y, valid, expected_Y, expected_valid, $time);
      error_count = error_count + 1;
    end else begin
      correct_count = correct_count + 1;
    end
  endtask
  // Assertions for checking the design
  property p_reset;
    @(posedge clk) rst |-> (Y == 2'b00 && valid == 1'b0);
  endproperty
  property p_case_1000;
    @(posedge clk) disable iff (rst) (D == 4'b1000) |-> (Y == 2'b00 && valid == 1'b1);
  endproperty
  property p_case_0100;
    @(posedge clk) disable iff (rst) (D == 4'b0100) |-> (Y == 2'b01 && valid == 1'b1);
  endproperty
  property p_case_0010;
    @(posedge clk) disable iff (rst) (D == 4'b0010) |-> (Y == 2'b10 && valid == 1'b1);
  endproperty
  property p_case_0001;
    @(posedge clk) disable iff (rst) (D == 4'b0001) |-> (Y == 2'b11 && valid == 1'b1);
  endproperty
  property p_case_0000;
    @(posedge clk) disable iff (rst) (D == 4'b0000) |-> (Y == 2'b00 && valid == 1'b0);
  endproperty
  // Assertion checks
  initial begin
    assert property (p_reset) else $fatal("Assertion failed during reset: Y = %b, valid = %b", Y, valid);
    assert property (p_case_1000) else $fatal("Assertion failed for D = 1000: Y = %b, valid = %b", Y, valid);
    assert property (p_case_0100) else $fatal("Assertion failed for D = 0100: Y = %b, valid = %b", Y, valid);
    assert property (p_case_0010) else $fatal("Assertion failed for D = 0010: Y = %b, valid = %b", Y, valid);
    assert property (p_case_0001) else $fatal("Assertion failed for D = 0001: Y = %b, valid = %b", Y, valid);
```

```
    assert property (p_case_0001) else $fatal("Assertion failed for D = 0001: Y = %b, valid = %b", Y, valid);
    assert property (p_case_0000) else $fatal("Assertion failed for D = 0000: Y = %b, valid = %b", Y, valid);
  end

  // Cover properties for monitoring coverage
  cover property (p_case_1000);
  cover property (p_case_0100);
  cover property (p_case_0010);
  cover property (p_case_0001);
  cover property (p_case_0000);

endmodule
```

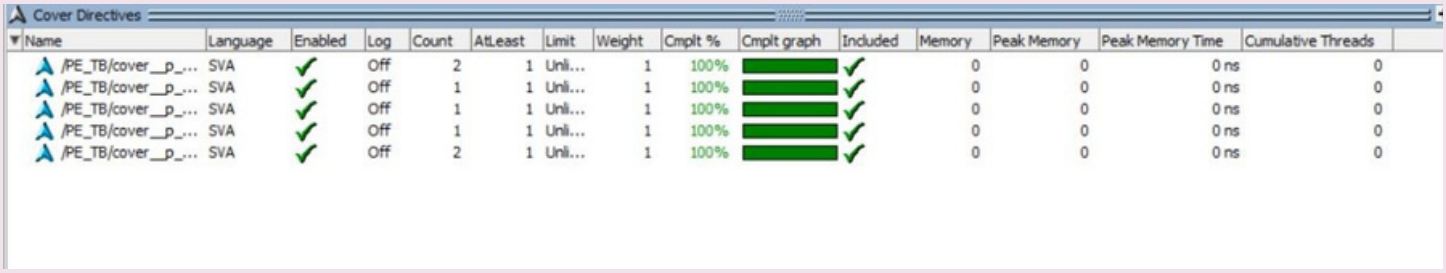
IV. Do file

```
vlib work
vlog priority_enc.sv PE_TB.sv  +cover -covercells
vsim -voptargs=+acc work.PE_TB -cover
add wave *
coverage save PE_TB.ucdb -onexit
run -all
```

V. Waveform



VI. Assertions



VII. Coverage Report

```
Coverage Report by instance with details

================================================================================
=== Instance: /\PE_TB#test
=== Design Unit: work.priority_enc
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         7         7         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\PE_TB#test

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File priority_enc.sv
-----------------------------------IF Branch-----------------------------------
    10                                        23     Count coming in to IF
    10              1                          4
    13              1                         19
Branch totals: 2 hits of 2 branches = 100.00%

----------------------------------CASE Branch----------------------------------
    15                                        19     Count coming in to CASE
    16              1                          6
    17              1                          6
    18              1                          4
    19              1                          2
    20              1                          1
Branch totals: 5 hits of 5 branches = 100.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       9         9         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\PE_TB#test  --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File priority_enc.sv
    9               1                         23
    11              1                          4
    12              1                          4
    16              1                          6
    17              1                          6
    18              1                          4
    19              1                          2
    20              1                          1
    22              1                         19
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         18        18         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\PE_TB#test  --

                                     Node      1H->0L      0L->1H  "Coverage"
                                     ----------------------------------------
                                   D[0-3]           1           1      100.00
                                   Y[1-0]           1           1      100.00
                                      clk           1           1      100.00
                                      rst           1           1      100.00
                                    valid           1           1      100.00

Total Node Count     =          9
Toggled Node Count   =          9
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (18 of 18 bins)


Total Coverage By Instance (filtered view): 100.00%
```

Question 4

Q4. Verify the functionality of counter provided in the assignment 2 by adding assertions to the design. Change the reset of the design to asynchronous.

- To check the asynchronous reset, you can use the following example

```
always_comb begin
if(reset)   a_reset: assert final(
== 0);
end
```

The above will check the value of the output of C when the reset is activated, since we want to check the value of the output after it has been changed, we will add a modified "final" after the keyword assert

1- Adjust your verification requirements document in the functionality check column, add if the requirement is checked against golden model, assertion or both. In case of assertion then mention its label used in your SVA module

2- Create an interface with DUT and TEST modports

3- Create the testbench as instructed in assignment 2 pdf but modify it to take an interface with modport TEST and do the necessary modifications in the testbench as we have done in the class

4- Create a top module where clock gen will take place and connections of interface.

5- Create SVA module and bind it in the top module with the following assertions (feel free to add more to enrich your verification process)

   i. When the load control signal is active, then the dout has the value of the din

   ii. When the load control signal is not active, and the enable is off then the dout does not change

   iii. When the load control signal is not active and the enable is active, and the up_down is high then the dout is incremented.

   - **Note:** to check for the increment, please use 1'b1 and do not use 1 since the simulator does not behave as expected for assertions using a 32-bit decimal iv. When the load control signal is not active and the enable is active, and the up_down is low then the dout is decremented.
   - **Note:** to check for the decrement, please use 1'b1 and do not use 1 since the simulator does not behave as expected for assertions using a 32-bit decimal

   v. When the asynchronous reset is asserted then the counter output is tied to low at the same instant. Note that you can use assert final to sample the new value of a signal.

   vi. max_count output is high when the counter output is maximum.

   vii. zero output is high when the counter output is zero.

6. Generate the coverage report and make sure to reach 100% code coverage, functional coverage and assertion coverage.

I. Verification plan

Label	Design Requirement Description	Stimulus Generation	Functional Coverage	Functionality Check
COUNTER_RST	When reset (rst_n) is asserted (low), the counter should reset, and the output should be zero.	Directed at the start of the simulation with reset assertion, and randomization afterward.	Coverpoint for reset deassertion. count_out must be 0 after reset is applied.	Check the output using assert_rst task, and also use reset_assertion as the first assertion in the SVA module.
COUNTER_LOAD	When load (load_n) is asserted (low), the counter should load the value on data_load.	Randomized under constraints so that load_n is active for 70% of the simulation time.	Included in coverpoints for load_n and data_load signal with cross-coverage between them to verify the load functionality.	Check the output against the expected load value using data_load_assertion.
COUNTER_UP	When up_down is high and ce is active, the counter should increment.	Randomized so that ce is high 70% of the time, and up_down is active during increment tests.	Coverpoint for ce high, up_down high, and cross with count_out to verify that counting increments correctly.	Check the output using increment_assertion in the SVA module. Make sure the counter increases as expected when conditions are met.
COUNTER_DOWN	When up_down is low and ce is active, the counter should decrement.	Randomized so that ce is high 70% of the time, and up_down is low during decrement tests.	Coverpoint for ce high, up_down low, and cross with count_out to verify that counting decrements correctly.	Check the output using decrement_assertion in the SVA module. Make sure the counter decreases as expected when conditions are met.
MAX_COUNT	When the counter reaches its maximum value, the max_count_exp signal should assert.	Directed test to set the counter near its maximum value and randomize to check overflow.	Coverpoint for count_out reaching its maximum, cross-checked with max_count_exp.	Check if max_count_exp is asserted when count_out reaches the maximum, verified against a golden model and via max_count_assertion in the SVA module.
ZERO_COUNT	When the counter reaches zero, the zero_exp signal should assert.	Directed test to set the counter near zero and randomize to check underflow.	Coverpoint for count_out reaching zero, cross-checked with zero_exp.	Check if zero_exp is asserted when count_out reaches zero, verified against a golden model and via zero_count_assertion in the SVA module.

II. RTL design

```
1
2  module counter (counter_if.DUT counterif);
3
4
5  always @(posedge counterif.clk or negedge counterif.rst_n) begin
6      if (!counterif.rst_n)
7          counterif.count_out <= 0;
8      else if (!counterif.load_n)
9          counterif.count_out <= counterif.data_load;
10     else if (counterif.ce)
11         if (counterif.up_down)
12             counterif.count_out <= counterif.count_out + 1;
13         else
14             counterif.count_out <= counterif.count_out - 1;
15 end
16
17 assign counterif.max_count = (counterif.count_out == {counterif.WIDTH{1'b1}})? 1:0;
18 assign counterif.zero = (counterif.count_out == 0)? 1:0;
19
20 endmodule
```

III. Package

```
package PCK;
  parameter WIDTH = 4;
  localparam ZERO =0;
  localparam MAX_COUNT = {WIDTH{1'b1}};
  class E2;
    rand bit rst_n_c, load_n_c, ce_c, up_down_c;
    rand bit [WIDTH-1:0] data_load_c;
    logic [WIDTH-1:0] count_out_c;

    // Constraints for the random variables
    constraint c_rst { rst_n_c dist {0 := 5, 1 := 95}; }
    constraint c_load { load_n_c dist {0 := 70, 1 := 30}; }
    constraint c_enable { ce_c dist {0 := 30, 1 := 70}; }
    covergroup cg ;
      load_cp : coverpoint data_load_c iff(!load_n_c);
      count_up_c1 : coverpoint count_out_c iff(rst_n_c && ce_c && up_down_c);
      count_up_c2 : coverpoint count_out_c iff(rst_n_c && ce_c && up_down_c){
      bins trans_overflow = (MAX_COUNT => ZERO);}
      count_down_c1: coverpoint count_out_c iff(rst_n_c && ce_c && ! up_down_c);
      count_down_c2 : coverpoint count_out_c iff(rst_n_c && ce_c && ! up_down_c){
      bins trans_underflow = (ZERO => MAX_COUNT);}
      endgroup
      function new ;
      cg = new();
      endfunction
  endclass
endpackage
```

IV. SVA module

```
module counter_sva (counter_if.DUT counterif);
    // Assertion: When load control signal is active, dout should be equal to din
    property p_load_control;
        @(posedge counterif.clk) disable iff (!counterif.rst_n)
        (counterif.load_n == 0) |=> (counterif.count_out == $past(counterif.data_load));
    endproperty
    assert property (p_load_control)
        else $fatal(1, "Load control assertion failed");
    cover property (p_load_control);
    // Assertion: When load control signal is not active, and enable is off, dout should not change
    property p_no_change;
        @(posedge counterif.clk) disable iff (!counterif.rst_n)
        (counterif.load_n == 1 && counterif.ce == 0) |=> $stable(counterif.count_out);
    endproperty
    assert property (p_no_change)
        else $fatal(1, "Load control no change assertion failed");
    cover property (p_no_change);
   // Assertion: When load control is inactive, enable is active, and up_down is high, dout should increment
property p_increment;
   @(posedge counterif.clk) disable iff(!counterif.rst_n) (counterif.load_n && counterif.ce && counterif.up_down)|=> (counterif.count_out === $past(counterif.count_out) + 4'b0001);
endproperty
assert property (p_increment)
    else $fatal(1, "Increment assertion failed");
cover property (p_increment);
    // Assertion: When load control is inactive, enable is active, and up_down is low, dout should decrement
    property p_decrement;
        @(posedge counterif.clk) disable iff (!counterif.rst_n)
        (counterif.load_n == 1 && counterif.ce == 1 && counterif.up_down == 0) |=> (counterif.count_out === $past(counterif.count_out) - 4'b0001);
    endproperty
    assert property (p_decrement)
        else $fatal(1, "Decrement assertion failed");
    cover property (p_decrement);
   always_comb begin
   if(!counterif.rst_n)
      assert_reset: assert final(counterif.count_out == 0);
   if(counterif.count_out == 0)
      assert_zero: assert (counterif.zero == 1);
   if(counterif.count_out == {counterif.WIDTH{1'b1}})
      assert_max: assert (counterif.max_count == 1);
   end
endmodule


```

V. Interface module

```
interface counter_if (clk);
// parameter declaration
parameter WIDTH = 4;
// input & output declaration
logic rst_n, load_n, up_down, ce;
logic [WIDTH-1: 0] data_load, count_out;
logic max_count, zero;
input bit clk;

modport DUT (input clk, rst_n, load_n, up_down, ce, data_load, output count_out, max_count, zero);
modport TEST (output rst_n, load_n, up_down, ce, data_load, input clk, count_out, max_count, zero);

endinterface

```

VI. Top module

```
module TOP;

bit clk;
always #50 clk=~clk;

// interface object
counter_if counterif(clk);
// DUT instantiation
counter DUT(counterif);
// testbench instantiation
counter_tb TEST(counterif);
// binding the assertions
bind counter counter_sva T(counterif);
endmodule

```

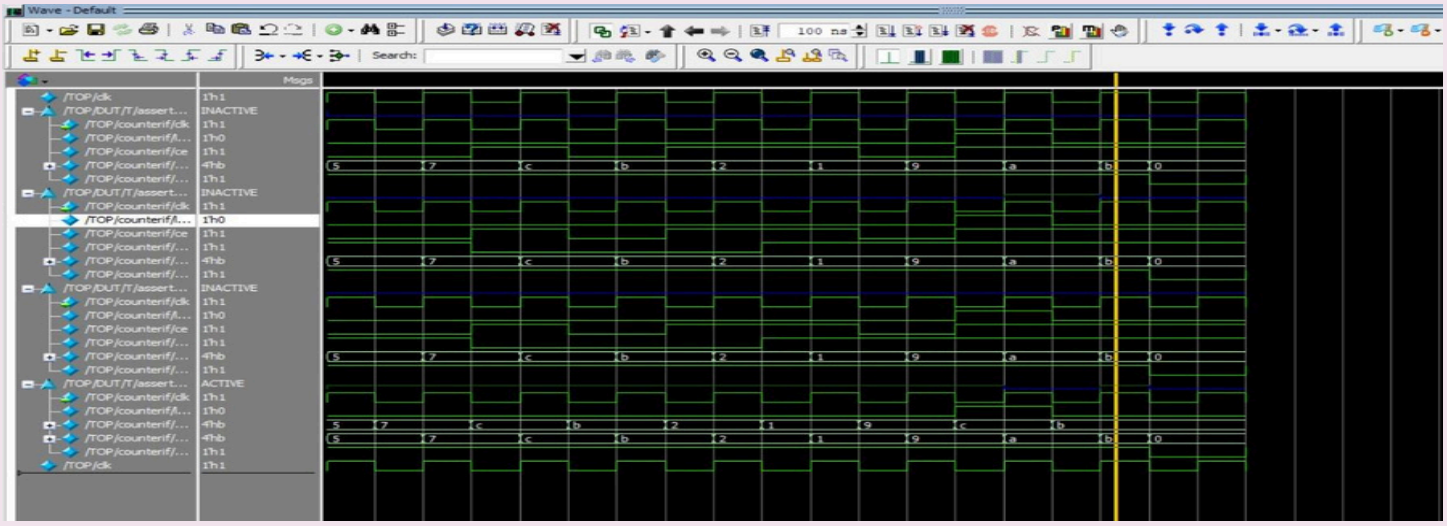
VII. Test bench

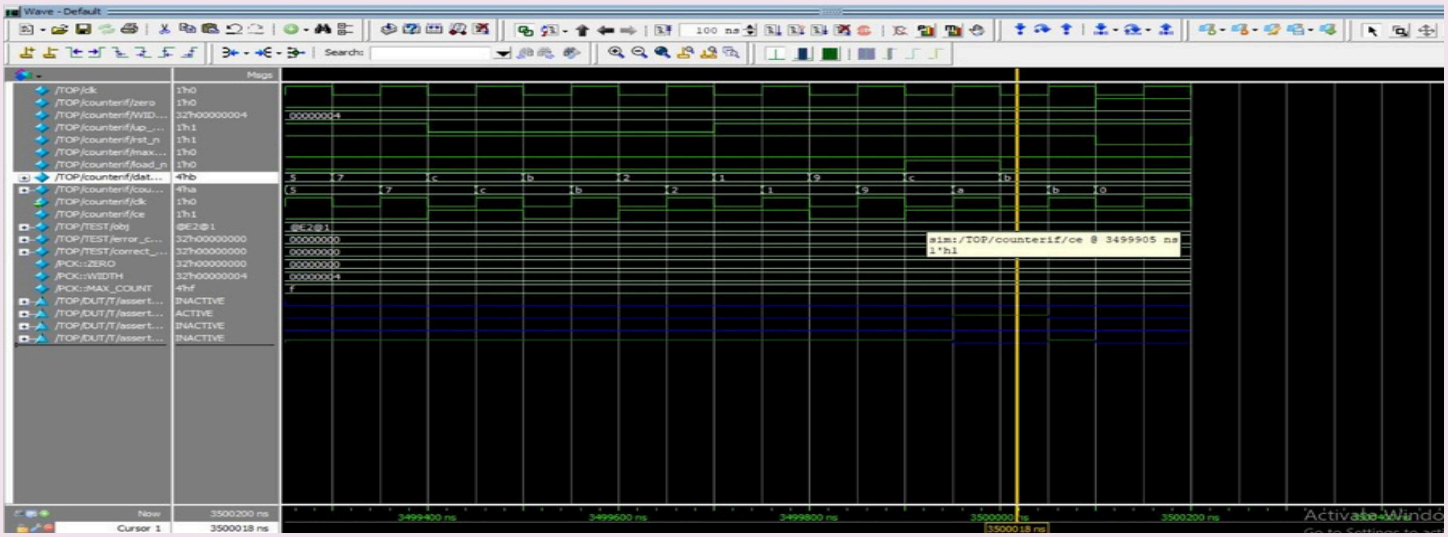
```
import PCK::*;
module counter_tb(counter_if.TEST counterif);
 // Create an instance of the transaction class
  E2 obj = new();
  // Stimulus Generation
  initial begin
    assert_rst;
    repeat (35000) begin
      assert(obj.randomize()) else $fatal("Randomization failed.");
      // Apply randomized values
      counterif.rst_n = obj.rst_n_c;
      counterif.load_n = obj.load_n_c;
      counterif.up_down = obj.up_down_c;
      counterif.ce = obj.ce_c;
      counterif.data_load = obj.data_load_c;
      @(negedge counterif.clk);
      obj.count_out_c = counterif.count_out;
      // Sample the coverage
      obj.cg.sample();
    end
    assert_rst;
    $stop;
  end
task assert_rst;
counterif.rst_n=0;
@(negedge counterif.clk);
counterif.rst_n=1;
endtask

endmodule

```

VIII. Do file

```
vlib work
vlog PCK.sv INTERFACE.sv TOP.sv SVA.sv counter.sv counter_tb.sv  +cover -covercells
vsim -voptargs=+acc work.TOP -cover
add wave *
add wave /TOP/DUT/T/assert__p_no_change /TOP/DUT/T/assert__p_increment
/TOP/DUT/T/assert__p_decrement /TOP/DUT/T/assert__p_load_control
add wave -position insertpoint  \
sim:/TOP/clk
coverage save counter_tb.ucdb -onexit
run -all
```

IX. Waveform





X. Functional Coverage Report

```
Coverage Report by instance with details

================================================================================
=== Instance: /TOP/DUT/T
=== Design Unit: work.counter_sva
================================================================================

Directive Coverage:
    Directives                       4         4         0   100.00%

DIRECTIVE COVERAGE:
--------------------------------------------------------------------------------------------------
Name                                 Design Design   Lang File(Line)      Hits Status
                                     Unit   UnitType
--------------------------------------------------------------------------------------------------
/TOP/DUT/T/cover__p_decrement        counter_sva Verilog  SVA  SVA.sv(32)      3366 Covered
/TOP/DUT/T/cover__p_increment        counter_sva Verilog  SVA  SVA.sv(24)      3268 Covered
/TOP/DUT/T/cover__p_no_change        counter_sva Verilog  SVA  SVA.sv(17)      2796 Covered
/TOP/DUT/T/cover__p_load_control     counter_sva Verilog  SVA  SVA.sv(9)       22081 Covered

================================================================================
=== Instance: /PCK
=== Design Unit: work.PCK
================================================================================

Covergroup Coverage:
    Covergroups                      1        na        na   100.00%
        Coverpoints/Crosses          5        na        na        na
            Covergroup Bins         50        50         0   100.00%
--------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

--------------------------------------------------------------------------------------------------
 TYPE /PCK/E2/cg                                  100.00%        100          -    Covered
    covered/total bins:                                50         50          -
    missing/total bins:                                 0         50          -
    % Hit:                                         100.00%        100          -
    Coverpoint load_cp                             100.00%        100          -    Covered
        covered/total bins:                            16         16          -
        missing/total bins:                             0         16          -
        % Hit:                                     100.00%        100          -
    Coverpoint count_up_c1                         100.00%        100          -    Covered
        covered/total bins:                            16         16          -
        missing/total bins:                             0         16          -
        % Hit:                                     100.00%        100          -
    Coverpoint count_up_c2                         100.00%        100          -    Covered
        covered/total bins:                             1          1          -
        missing/total bins:                             0          1          -
        % Hit:                                     100.00%        100          -
    Coverpoint count_down_c1                       100.00%        100          -    Covered
        covered/total bins:                            16         16          -
        missing/total bins:                             0         16          -
        % Hit:                                     100.00%        100          -
    Coverpoint count_down_c2                       100.00%        100          -    Covered
        covered/total bins:                             1          1          -
        missing/total bins:                             0          1          -
        % Hit:                                     100.00%        100          -
 Covergroup instance \/PCK::E2::cg                 100.00%        100          -    Covered
    covered/total bins:                                50         50          -
    missing/total bins:                                 0         50          -
    % Hit:                                         100.00%        100          -
    Coverpoint load_cp                             100.00%        100          -    Covered
        covered/total bins:                            16         16          -
        missing/total bins:                             0         16          -
        % Hit:                                     100.00%        100          -
        bin auto[0]                                  1493          1          -    Covered
        bin auto[1]                                  1533          1          -    Covered
        bin auto[2]                                  1574          1          -    Covered
        bin auto[3]                                  1499          1          -    Covered
        bin auto[4]                                  1528          1          -    Covered
        bin auto[5]                                  1508          1          -    Covered
        bin auto[6]                                  1512          1          -    Covered
        bin auto[7]                                  1565          1          -    Covered
        bin auto[8]                                  1504          1          -    Covered
        bin auto[9]                                  1565          1          -    Covered
        bin auto[10]                                 1548          1          -    Covered
        bin auto[11]                                 1513          1          -    Covered
        bin auto[12]                                 1466          1          -    Covered
        bin auto[13]                                 1521          1          -    Covered
        bin auto[14]                                 1525          1          -    Covered
        bin auto[15]                                 1537          1          -    Covered
    Coverpoint count_up_c1                         100.00%        100          -    Covered
        covered/total bins:                            16         16          -
        missing/total bins:                             0         16          -
        % Hit:                                     100.00%        100          -
        bin auto[0]                                   727          1          -    Covered
        bin auto[1]                                   876          1          -    Covered
        bin auto[2]                                   762          1          -    Covered
        bin auto[3]                                   708          1          -    Covered
        bin auto[4]                                   713          1          -    Covered
        bin auto[5]                                   689          1          -    Covered
        bin auto[6]                                   707          1          -    Covered
        bin auto[7]                                   700          1          -    Covered
        bin auto[8]                                   728          1          -    Covered
```

```
        bin auto[9]                              683          1          -    Covered
        bin auto[10]                             711          1          -    Covered
        bin auto[11]                             695          1          -    Covered
        bin auto[12]                             720          1          -    Covered
        bin auto[13]                             734          1          -    Covered
        bin auto[14]                             674          1          -    Covered
        bin auto[15]                             710          1          -    Covered
    Coverpoint count_up_c2                    100.00%        100          -    Covered
        covered/total bins:                         1          1          -
        missing/total bins:                         0          1          -
        % Hit:                                100.00%        100          -
        bin trans_overflow                        122          1          -    Covered
    Coverpoint count_down_c1                  100.00%        100          -    Covered
        covered/total bins:                        16         16          -
        missing/total bins:                         0         16          -
        % Hit:                                100.00%        100          -
        bin auto[0]                               715          1          -    Covered
        bin auto[1]                               730          1          -    Covered
        bin auto[2]                               713          1          -    Covered
        bin auto[3]                               712          1          -    Covered
        bin auto[4]                               709          1          -    Covered
        bin auto[5]                               692          1          -    Covered
        bin auto[6]                               709          1          -    Covered
        bin auto[7]                               726          1          -    Covered
        bin auto[8]                               696          1          -    Covered
        bin auto[9]                               744          1          -    Covered
        bin auto[10]                              686          1          -    Covered
        bin auto[11]                              683          1          -    Covered
        bin auto[12]                              694          1          -    Covered
        bin auto[13]                              683          1          -    Covered
        bin auto[14]                              752          1          -    Covered
        bin auto[15]                              886          1          -    Covered
    Coverpoint count_down_c2                  100.00%        100          -    Covered
        covered/total bins:                         1          1          -
        missing/total bins:                         0          1          -
        % Hit:                                100.00%        100          -
        bin trans_underflow                       119          1          -    Covered

COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------------------
Covergroup                                      Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------------------
 TYPE /PCK/E2/cg                              100.00%        100          -    Covered
    covered/total bins:                            50         50          -
    missing/total bins:                             0         50          -
    % Hit:                                    100.00%        100          -
    Coverpoint load_cp                        100.00%        100          -    Covered
        covered/total bins:                        16         16          -
        missing/total bins:                         0         16          -
        % Hit:                                100.00%        100          -
    Coverpoint count_up_c1                    100.00%        100          -    Covered
        covered/total bins:                        16         16          -
        missing/total bins:                         0         16          -
        % Hit:                                100.00%        100          -
    Coverpoint count_up_c2                    100.00%        100          -    Covered
        covered/total bins:                         1          1          -
        missing/total bins:                         0          1          -
        % Hit:                                100.00%        100          -
    Coverpoint count_down_c1                  100.00%        100          -    Covered
        covered/total bins:                        16         16          -
        missing/total bins:                         0         16          -
        % Hit:                                100.00%        100          -
    Coverpoint count_down_c2                  100.00%        100          -    Covered
        covered/total bins:                         1          1          -
        missing/total bins:                         0          1          -
        % Hit:                                100.00%        100          -
 Covergroup instance \/PCK::E2::cg            100.00%        100          -    Covered
    covered/total bins:                            50         50          -
    missing/total bins:                             0         50          -
    % Hit:                                    100.00%        100          -
    Coverpoint load_cp                        100.00%        100          -    Covered
        covered/total bins:                        16         16          -
        missing/total bins:                         0         16          -
        % Hit:                                100.00%        100          -
        bin auto[0]                              1493          1          -    Covered
        bin auto[1]                              1533          1          -    Covered
        bin auto[2]                              1574          1          -    Covered
        bin auto[3]                              1499          1          -    Covered
        bin auto[4]                              1528          1          -    Covered
        bin auto[5]                              1508          1          -    Covered
        bin auto[6]                              1512          1          -    Covered
        bin auto[7]                              1565          1          -    Covered
        bin auto[8]                              1504          1          -    Covered
        bin auto[9]                              1565          1          -    Covered
        bin auto[10]                             1548          1          -    Covered
        bin auto[11]                             1513          1          -    Covered
        bin auto[12]                             1466          1          -    Covered
        bin auto[13]                             1521          1          -    Covered
        bin auto[14]                             1525          1          -    Covered
        bin auto[15]                             1537          1          -    Covered
    Coverpoint count_up_c1                    100.00%        100          -    Covered
        covered/total bins:                        16         16          -
        missing/total bins:                         0         16          -
        % Hit:                                100.00%        100          -
        bin auto[0]                               727          1          -    Covered
```

```
        bin auto[0]                                  727          1          -    Covered
        bin auto[1]                                  876          1          -    Covered
        bin auto[2]                                  762          1          -    Covered
        bin auto[3]                                  708          1          -    Covered
        bin auto[4]                                  713          1          -    Covered
        bin auto[5]                                  689          1          -    Covered
        bin auto[6]                                  707          1          -    Covered
        bin auto[7]                                  700          1          -    Covered
        bin auto[8]                                  728          1          -    Covered
        bin auto[9]                                  683          1          -    Covered
        bin auto[10]                                 711          1          -    Covered
        bin auto[11]                                 695          1          -    Covered
        bin auto[12]                                 720          1          -    Covered
        bin auto[13]                                 734          1          -    Covered
        bin auto[14]                                 674          1          -    Covered
        bin auto[15]                                 710          1          -    Covered
    Coverpoint count_up_c2                       100.00%        100          -    Covered
        covered/total bins:                            1          1          -
        missing/total bins:                            0          1          -
        % Hit:                                   100.00%        100          -
        bin trans_overflow                           122          1          -    Covered
    Coverpoint count_down_c1                     100.00%        100          -    Covered
        covered/total bins:                           16         16          -
        missing/total bins:                            0         16          -
        % Hit:                                   100.00%        100          -
        bin auto[0]                                  715          1          -    Covered
        bin auto[1]                                  730          1          -    Covered
        bin auto[2]                                  713          1          -    Covered
        bin auto[3]                                  712          1          -    Covered
        bin auto[4]                                  709          1          -    Covered
        bin auto[5]                                  692          1          -    Covered
        bin auto[6]                                  709          1          -    Covered
        bin auto[7]                                  726          1          -    Covered
        bin auto[8]                                  696          1          -    Covered
        bin auto[9]                                  744          1          -    Covered
        bin auto[10]                                 686          1          -    Covered
        bin auto[11]                                 683          1          -    Covered
        bin auto[12]                                 694          1          -    Covered
        bin auto[13]                                 683          1          -    Covered
        bin auto[14]                                 752          1          -    Covered
        bin auto[15]                                 886          1          -    Covered
    Coverpoint count_down_c2                     100.00%        100          -    Covered
        covered/total bins:                            1          1          -
        missing/total bins:                            0          1          -
        % Hit:                                   100.00%        100          -
        bin trans_underflow                          119          1          -    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

DIRECTIVE COVERAGE:
--------------------------------------------------------------------------------------------
Name                                 Design Design   Lang File(Line)      Hits Status
                                     Unit   UnitType
--------------------------------------------------------------------------------------------
/TOP/DUT/T/cover__p_decrement        counter_sva Verilog  SVA  SVA.sv(32)      3366 Covered
/TOP/DUT/T/cover__p_increment        counter_sva Verilog  SVA  SVA.sv(24)      3268 Covered
/TOP/DUT/T/cover__p_no_change        counter_sva Verilog  SVA  SVA.sv(17)      2796 Covered
/TOP/DUT/T/cover__p_load_control     counter_sva Verilog  SVA  SVA.sv(9)       22081 Covered

TOTAL DIRECTIVE COVERAGE: 100.00%  COVERS: 4

Total Coverage By Instance (filtered view): 100.00%
```

XI. Coverage Report

```
Coverage Report by instance with details

================================================================================
=== Instance: /TOP/counterif
=== Design Unit: work.counter_if
================================================================================
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         30        30         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /TOP/counterif --

                                          Node      1H->0L      0L->1H  "Coverage"
                                          ----------------------------------------
                                            ce           1           1      100.00
                                           clk           1           1      100.00
                                 count_out[3-0]          1           1      100.00
                                 data_load[3-0]          1           1      100.00
                                        load_n           1           1      100.00
                                     max_count           1           1      100.00
                                         rst_n           1           1      100.00
                                       up_down           1           1      100.00
                                          zero           1           1      100.00

Total Node Count     =          15
Toggled Node Count   =          15
Untoggled Node Count =           0

Toggle Coverage      =     100.00% (30 of 30 bins)

================================================================================
=== Instance: /TOP/DUT/T
=== Design Unit: work.counter_sva
================================================================================

Assertion Coverage:
    Assertions                       7         7         0   100.00%
--------------------------------------------------------------------
Name                 File(Line)                   Failure      Pass
                                                  Count        Count
--------------------------------------------------------------------
/TOP/DUT/T/assert__p_decrement
                     SVA.sv(30)                           0          1
/TOP/DUT/T/assert__p_increment
                     SVA.sv(22)                           0          1
/TOP/DUT/T/assert__p_no_change
                     SVA.sv(15)                           0          1
/TOP/DUT/T/assert__p_load_control
                     SVA.sv(7)                            0          1
/TOP/DUT/T/assert_reset
                     SVA.sv(35)                           0          1
/TOP/DUT/T/assert_zero
                     SVA.sv(37)                           0          1
/TOP/DUT/T/assert_max
                     SVA.sv(39)                           0          1
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         6         6         0   100.00%

================================Branch Details================================

Branch Coverage for instance /TOP/DUT/T

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File SVA.sv
------------------------------------IF Branch------------------------------------
    34                                     33819     Count coming in to IF
    34             1                        3296
                                           30523     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    36                                     33819     Count coming in to IF
    36             1                        5122
                                           28697     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    38                                     33819     Count coming in to IF
    38             1                        2069
                                           31750     All False Count
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                       2         2         0   100.00%
```

```
Condition Coverage for instance /TOP/DUT/T --

  File SVA.sv
----------------Focused Condition View-------------------
Line       36 Item    1  (counterif.count_out == 0)
Condition totals: 1 of 1 input term covered = 100.00%

                 Input Term   Covered  Reason for no coverage   Hint
                -----------  --------  ----------------------  --------------
  (counterif.count_out == 0)         Y

     Rows:       Hits  FEC Target                  Non-masking condition(s)
 ---------  ---------  --------------------        -------------------------
  Row   1:          1  (counterif.count_out == 0)_0  -
  Row   2:          1  (counterif.count_out == 0)_1  -

----------------Focused Condition View-------------------
Line       38 Item    1  (counterif.count_out == {4{1}})
Condition totals: 1 of 1 input term covered = 100.00%

                     Input Term   Covered  Reason for no coverage   Hint
                    -----------  --------  ----------------------  --------------
  (counterif.count_out == {4{1}})         Y

     Rows:       Hits  FEC Target                        Non-masking condition(s)
 ---------  ---------  --------------------              -------------------------
  Row   1:          1  (counterif.count_out == {4{1}})_0  -
  Row   2:          1  (counterif.count_out == {4{1}})_1  -


Directive Coverage:
    Directives                       4         4         0   100.00%

DIRECTIVE COVERAGE:
--------------------------------------------------------------------------------------------
Name                                     Design Design   Lang File(Line)      Hits Status
                                         Unit   UnitType
--------------------------------------------------------------------------------------------
/TOP/DUT/T/cover__p_decrement            counter_sva Verilog  SVA  SVA.sv(32)      3366 Covered
/TOP/DUT/T/cover__p_increment            counter_sva Verilog  SVA  SVA.sv(24)      3268 Covered
/TOP/DUT/T/cover__p_no_change            counter_sva Verilog  SVA  SVA.sv(17)      2796 Covered
/TOP/DUT/T/cover__p_load_control         counter_sva Verilog  SVA  SVA.sv(9)       22081 Covered
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       1         1         0   100.00%

================================Statement Details================================

Statement Coverage for instance /TOP/DUT/T --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File SVA.sv
    33              1                      33819

================================================================================
=== Instance: /TOP/DUT
=== Design Unit: work.counter
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        10        10         0   100.00%

================================Branch Details================================

Branch Coverage for instance /TOP/DUT

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File counter.sv
------------------------------------IF Branch------------------------------------
    6                                     36704     Count coming in to IF
    6               1                      3492
    8               1                     23229
    10              1                      7028
                                           2955     All False Count
Branch totals: 4 hits of 4 branches = 100.00%

------------------------------------IF Branch------------------------------------
    11                                     7028     Count coming in to IF
    11              1                      3469
    13              1                      3559
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    17                                    30416     Count coming in to IF
    17              1                      1964
    17              2                     28452
Branch totals: 2 hits of 2 branches = 100.00%
```

```
------------------------------------IF Branch------------------------------------
    18                                  30416     Count coming in to IF
    18              1                    3313
    18              2                   27103
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----   -------    ------  --------
    Conditions                       2         2         0   100.00%

================================Condition Details================================

Condition Coverage for instance /TOP/DUT --

  File counter.sv
----------------Focused Condition View-------------------
Line       17 Item    1  (counterif.count_out == {counterif.WIDTH{1}})
Condition totals: 1 of 1 input term covered = 100.00%

                                  Input Term   Covered  Reason for no coverage   Hint
                                 -----------  --------  ----------------------  --------------
  (counterif.count_out == {counterif.WIDTH{1}})         Y

     Rows:       Hits  FEC Target                                         Non-masking condition(s)
 ---------  ---------  --------------------                               -------------------------
  Row   1:          1  (counterif.count_out == {counterif.WIDTH{1}})_0  -
  Row   2:          1  (counterif.count_out == {counterif.WIDTH{1}})_1  -

----------------Focused Condition View-------------------
Line       18 Item    1  (counterif.count_out == 0)
Condition totals: 1 of 1 input term covered = 100.00%

                 Input Term   Covered  Reason for no coverage   Hint
                -----------  --------  ----------------------  --------------
  (counterif.count_out == 0)         Y

     Rows:       Hits  FEC Target                   Non-masking condition(s)
 ---------  ---------  --------------------         -------------------------
  Row   1:          1  (counterif.count_out == 0)_0  -
  Row   2:          1  (counterif.count_out == 0)_1  -


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       7         7         0   100.00%

================================Statement Details================================

Statement Coverage for instance /TOP/DUT --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File counter.sv
    5               1                      36704
    7               1                       3492
    9               1                      23229
    12              1                       3469
    14              1                       3559
    17              1                      30417
    18              1                      30417

================================================================================
=== Instance: /TOP/TEST
=== Design Unit: work.counter_tb
================================================================================

Assertion Coverage:
    Assertions                       1         1         0   100.00%
--------------------------------------------------------------------
Name                 File(Line)                    Failure      Pass
                                                   Count        Count
--------------------------------------------------------------------
/TOP/TEST/#ublk#95084642#14/immed__15
                     counter_tb.sv(15)                   0          1
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      18        18         0   100.00%

================================Statement Details================================

Statement Coverage for instance /TOP/TEST --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File counter_tb.sv
    7               1                          1
    11              1                          1
    12              1                          1
    13              1                          1
    14              1                      35000
    17              1                      35000
    18              1                      35000
```

```
    21              1                       35000
    22              1                       35000
    23              1                       35000
    25              1                       35000
    27              1                           1
    28              1                           1
    31              1                           2
    32              1                           2
    33              1                           2

================================================================================
=== Instance: /TOP
=== Design Unit: work.TOP
================================================================================
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       2         2         0   100.00%

================================Statement Details================================

Statement Coverage for instance /TOP --

    Line         Item                     Count     Source
    ----         ----                     -----     ------
  File TOP.sv
    4               1                     70005
    4               2                     70004
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                          2         2         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /TOP --

                                       Node      1H->0L      0L->1H  "Coverage"
                                       ----------------------------------------
                                       clk            1           1      100.00

Total Node Count     =          1
Toggled Node Count   =          1
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (2 of 2 bins)

================================================================================
=== Instance: /PCK
=== Design Unit: work.PCK
================================================================================

Covergroup Coverage:
    Covergroups                     1        na        na   100.00%
        Coverpoints/Crosses         5        na        na        na
            Covergroup Bins        50        50         0   100.00%
--------------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

--------------------------------------------------------------------------------------------------------
 TYPE /PCK/E2/cg                                   100.00%        100          -    Covered
    covered/total bins:                                 50         50          -
    missing/total bins:                                  0         50          -
    % Hit:                                          100.00%        100          -
    Coverpoint load_cp                              100.00%        100          -    Covered
        covered/total bins:                              16         16          -
        missing/total bins:                               0         16          -
        % Hit:                                      100.00%        100          -
    Coverpoint count_up_c1                          100.00%        100          -    Covered
        covered/total bins:                              16         16          -
        missing/total bins:                               0         16          -
        % Hit:                                      100.00%        100          -
    Coverpoint count_up_c2                          100.00%        100          -    Covered
        covered/total bins:                               1          1          -
        missing/total bins:                               0          1          -
        % Hit:                                      100.00%        100          -
    Coverpoint count_down_c1                        100.00%        100          -    Covered
        covered/total bins:                              16         16          -
        missing/total bins:                               0         16          -
        % Hit:                                      100.00%        100          -
    Coverpoint count_down_c2                        100.00%        100          -    Covered
        covered/total bins:                               1          1          -
        missing/total bins:                               0          1          -
        % Hit:                                      100.00%        100          -
 Covergroup instance \/PCK::E2::cg                  100.00%        100          -    Covered
    covered/total bins:                                 50         50          -
    missing/total bins:                                  0         50          -
    % Hit:                                          100.00%        100          -
    Coverpoint load_cp                              100.00%        100          -    Covered
        covered/total bins:                              16         16          -
        missing/total bins:                               0         16          -
        % Hit:                                      100.00%        100          -
        bin auto[0]                                    1493          1          -    Covered
        bin auto[1]                                    1533          1          -    Covered
        bin auto[2]                                    1574          1          -    Covered
        bin auto[3]                                    1499          1          -    Covered
```

```
        bin auto[6]                                 1512          1          -    Covered
        bin auto[7]                                 1565          1          -    Covered
        bin auto[8]                                 1504          1          -    Covered
        bin auto[9]                                 1565          1          -    Covered
        bin auto[10]                                1548          1          -    Covered
        bin auto[11]                                1513          1          -    Covered
        bin auto[12]                                1466          1          -    Covered
        bin auto[13]                                1521          1          -    Covered
        bin auto[14]                                1525          1          -    Covered
        bin auto[15]                                1537          1          -    Covered
    Coverpoint count_up_c1                        100.00%        100          -    Covered
        covered/total bins:                            16         16          -
        missing/total bins:                             0         16          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                  727          1          -    Covered
        bin auto[1]                                  876          1          -    Covered
        bin auto[2]                                  762          1          -    Covered
        bin auto[3]                                  708          1          -    Covered
        bin auto[4]                                  713          1          -    Covered
        bin auto[5]                                  689          1          -    Covered
        bin auto[6]                                  707          1          -    Covered
        bin auto[7]                                  700          1          -    Covered
        bin auto[8]                                  728          1          -    Covered
        bin auto[9]                                  683          1          -    Covered
        bin auto[10]                                 711          1          -    Covered
        bin auto[11]                                 695          1          -    Covered
        bin auto[12]                                 720          1          -    Covered
        bin auto[13]                                 734          1          -    Covered
        bin auto[14]                                 674          1          -    Covered
        bin auto[15]                                 710          1          -    Covered
    Coverpoint count_up_c2                        100.00%        100          -    Covered
        covered/total bins:                             1          1          -
        missing/total bins:                             0          1          -
        % Hit:                                    100.00%        100          -
        bin trans_overflow                           122          1          -    Covered
    Coverpoint count_down_c1                      100.00%        100          -    Covered
        covered/total bins:                            16         16          -
        missing/total bins:                             0         16          -
        % Hit:                                    100.00%        100          -
        bin auto[0]                                  715          1          -    Covered
        bin auto[1]                                  730          1          -    Covered
        bin auto[2]                                  713          1          -    Covered
        bin auto[3]                                  712          1          -    Covered
        bin auto[4]                                  709          1          -    Covered
        bin auto[5]                                  692          1          -    Covered
        bin auto[6]                                  709          1          -    Covered
        bin auto[7]                                  726          1          -    Covered
        bin auto[8]                                  696          1          -    Covered
        bin auto[9]                                  744          1          -    Covered
        bin auto[10]                                 686          1          -    Covered
        bin auto[11]                                 683          1          -    Covered
        bin auto[12]                                 694          1          -    Covered
        bin auto[13]                                 683          1          -    Covered
        bin auto[14]                                 752          1          -    Covered
        bin auto[15]                                 886          1          -    Covered
    Coverpoint count_down_c2                      100.00%        100          -    Covered
        covered/total bins:                             1          1          -
        missing/total bins:                             0          1          -
        % Hit:                                    100.00%        100          -
        bin trans_underflow                          119          1          -    Covered
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       1         1         0   100.00%

================================Statement Details================================

Statement Coverage for instance /PCK --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File PCK.sv
    24              1                          1

COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------------
Covergroup                                             Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------------
 TYPE /PCK/E2/cg                                     100.00%        100          -    Covered
    covered/total bins:                                   50         50          -
    missing/total bins:                                    0         50          -
    % Hit:                                            100.00%        100          -
    Coverpoint load_cp                                100.00%        100          -    Covered
        covered/total bins:                               16         16          -
        missing/total bins:                                0         16          -
        % Hit:                                        100.00%        100          -
    Coverpoint count_up_c1                            100.00%        100          -    Covered
        covered/total bins:                               16         16          -
        missing/total bins:                                0         16          -
        % Hit:                                        100.00%        100          -
    Coverpoint count_up_c2                            100.00%        100          -    Covered
        covered/total bins:                                1          1          -
        missing/total bins:                                0          1          -
        % Hit:                                        100.00%        100          -
    Coverpoint count_down_c1                          100.00%        100          -    Covered
```

```
        bin auto[10]                              1548          1          -    Covered
        bin auto[11]                              1513          1          -    Covered
        bin auto[12]                              1466          1          -    Covered
        bin auto[13]                              1521          1          -    Covered
        bin auto[14]                              1525          1          -    Covered
        bin auto[15]                              1537          1          -    Covered
    Coverpoint count_up_c1                      100.00%        100          -    Covered
        covered/total bins:                          16         16          -
        missing/total bins:                           0         16          -
        % Hit:                                  100.00%        100          -
        bin auto[0]                                727          1          -    Covered
        bin auto[1]                                876          1          -    Covered
        bin auto[2]                                762          1          -    Covered
        bin auto[3]                                708          1          -    Covered
        bin auto[4]                                713          1          -    Covered
        bin auto[5]                                689          1          -    Covered
        bin auto[6]                                707          1          -    Covered
        bin auto[7]                                700          1          -    Covered
        bin auto[8]                                728          1          -    Covered
        bin auto[9]                                683          1          -    Covered
        bin auto[10]                               711          1          -    Covered
        bin auto[11]                               695          1          -    Covered
        bin auto[12]                               720          1          -    Covered
        bin auto[13]                               734          1          -    Covered
        bin auto[14]                               674          1          -    Covered
        bin auto[15]                               710          1          -    Covered
    Coverpoint count_up_c2                      100.00%        100          -    Covered
        covered/total bins:                           1          1          -
        missing/total bins:                           0          1          -
        % Hit:                                  100.00%        100          -
        bin trans_overflow                         122          1          -    Covered
    Coverpoint count_down_c1                    100.00%        100          -    Covered
        covered/total bins:                          16         16          -
        missing/total bins:                           0         16          -
        % Hit:                                  100.00%        100          -
        bin auto[0]                                715          1          -    Covered
        bin auto[1]                                730          1          -    Covered
        bin auto[2]                                713          1          -    Covered
        bin auto[3]                                712          1          -    Covered
        bin auto[4]                                709          1          -    Covered
        bin auto[5]                                692          1          -    Covered
        bin auto[6]                                709          1          -    Covered
        bin auto[7]                                726          1          -    Covered
        bin auto[8]                                696          1          -    Covered
        bin auto[9]                                744          1          -    Covered
        bin auto[10]                               686          1          -    Covered
        bin auto[11]                               683          1          -    Covered
        bin auto[12]                               694          1          -    Covered
        bin auto[13]                               683          1          -    Covered
        bin auto[14]                               752          1          -    Covered
        bin auto[15]                               886          1          -    Covered
    Coverpoint count_down_c2                    100.00%        100          -    Covered
        covered/total bins:                           1          1          -
        missing/total bins:                           0          1          -
        % Hit:                                  100.00%        100          -
        bin trans_underflow                        119          1          -    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

DIRECTIVE COVERAGE:
-----------------------------------------------------------------------------------------
Name                                    Design Design   Lang File(Line)      Hits Status
                                        Unit   UnitType
-----------------------------------------------------------------------------------------
/TOP/DUT/T/cover__p_decrement           counter_sva Verilog  SVA  SVA.sv(32)      3366 Covered
/TOP/DUT/T/cover__p_increment           counter_sva Verilog  SVA  SVA.sv(24)      3268 Covered
/TOP/DUT/T/cover__p_no_change           counter_sva Verilog  SVA  SVA.sv(17)      2796 Covered
/TOP/DUT/T/cover__p_load_control        counter_sva Verilog  SVA  SVA.sv(9)       22081 Covered

TOTAL DIRECTIVE COVERAGE: 100.00%  COVERS: 4

ASSERTION RESULTS:
---------------------------------------------------------------------
Name                File(Line)                   Failure      Pass
                                                 Count        Count
---------------------------------------------------------------------
/TOP/DUT/T/assert__p_decrement
                    SVA.sv(30)                          0          1
/TOP/DUT/T/assert__p_increment
                    SVA.sv(22)                          0          1
/TOP/DUT/T/assert__p_no_change
                    SVA.sv(15)                          0          1
/TOP/DUT/T/assert__p_load_control
                    SVA.sv(7)                           0          1
/TOP/DUT/T/assert_reset
                    SVA.sv(35)                          0          1
/TOP/DUT/T/assert_zero
                    SVA.sv(37)                          0          1
/TOP/DUT/T/assert_max
                    SVA.sv(39)                          0          1
/TOP/TEST/#ublk#95084642#14/immed__15
                    counter_tb.sv(15)                   0          1

Total Coverage By Instance (filtered view): 100.00%
```

```
        bin auto[10]                              1548          1          -    Covered
        bin auto[11]                              1513          1          -    Covered
        bin auto[12]                              1466          1          -    Covered
        bin auto[13]                              1521          1          -    Covered
        bin auto[14]                              1525          1          -    Covered
        bin auto[15]                              1537          1          -    Covered
    Coverpoint count_up_c1                      100.00%        100          -    Covered
        covered/total bins:                          16         16          -
        missing/total bins:                           0         16          -
        % Hit:                                  100.00%        100          -
        bin auto[0]                                727          1          -    Covered
        bin auto[1]                                876          1          -    Covered
        bin auto[2]                                762          1          -    Covered
        bin auto[3]                                708          1          -    Covered
        bin auto[4]                                713          1          -    Covered
        bin auto[5]                                689          1          -    Covered
        bin auto[6]                                707          1          -    Covered
        bin auto[7]                                700          1          -    Covered
        bin auto[8]                                728          1          -    Covered
        bin auto[9]                                683          1          -    Covered
        bin auto[10]                               711          1          -    Covered
        bin auto[11]                               695          1          -    Covered
        bin auto[12]                               720          1          -    Covered
        bin auto[13]                               734          1          -    Covered
        bin auto[14]                               674          1          -    Covered
        bin auto[15]                               710          1          -    Covered
    Coverpoint count_up_c2                      100.00%        100          -    Covered
        covered/total bins:                           1          1          -
        missing/total bins:                           0          1          -
        % Hit:                                  100.00%        100          -
        bin trans_overflow                         122          1          -    Covered
    Coverpoint count_down_c1                    100.00%        100          -    Covered
        covered/total bins:                          16         16          -
        missing/total bins:                           0         16          -
        % Hit:                                  100.00%        100          -
        bin auto[0]                                715          1          -    Covered
        bin auto[1]                                730          1          -    Covered
        bin auto[2]                                713          1          -    Covered
        bin auto[3]                                712          1          -    Covered
        bin auto[4]                                709          1          -    Covered
        bin auto[5]                                692          1          -    Covered
        bin auto[6]                                709          1          -    Covered
        bin auto[7]                                726          1          -    Covered
        bin auto[8]                                696          1          -    Covered
        bin auto[9]                                744          1          -    Covered
        bin auto[10]                               686          1          -    Covered
        bin auto[11]                               683          1          -    Covered
        bin auto[12]                               694          1          -    Covered
        bin auto[13]                               683          1          -    Covered
        bin auto[14]                               752          1          -    Covered
        bin auto[15]                               886          1          -    Covered
    Coverpoint count_down_c2                    100.00%        100          -    Covered
        covered/total bins:                           1          1          -
        missing/total bins:                           0          1          -
        % Hit:                                  100.00%        100          -
        bin trans_underflow                        119          1          -    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

DIRECTIVE COVERAGE:
-------------------------------------------------------------------------------------------
Name                                    Design Design   Lang File(Line)      Hits Status
                                        Unit   UnitType
-------------------------------------------------------------------------------------------
/TOP/DUT/T/cover__p_decrement           counter_sva Verilog  SVA  SVA.sv(32)      3366 Covered
/TOP/DUT/T/cover__p_increment           counter_sva Verilog  SVA  SVA.sv(24)      3268 Covered
/TOP/DUT/T/cover__p_no_change           counter_sva Verilog  SVA  SVA.sv(17)      2796 Covered
/TOP/DUT/T/cover__p_load_control        counter_sva Verilog  SVA  SVA.sv(9)       22081 Covered

TOTAL DIRECTIVE COVERAGE: 100.00%  COVERS: 4

ASSERTION RESULTS:
---------------------------------------------------------------------
Name                 File(Line)                   Failure      Pass
                                                  Count        Count
---------------------------------------------------------------------
/TOP/DUT/T/assert__p_decrement
                     SVA.sv(30)                          0          1
/TOP/DUT/T/assert__p_increment
                     SVA.sv(22)                          0          1
/TOP/DUT/T/assert__p_no_change
                     SVA.sv(15)                          0          1
/TOP/DUT/T/assert__p_load_control
                     SVA.sv(7)                           0          1
/TOP/DUT/T/assert_reset
                     SVA.sv(35)                          0          1
/TOP/DUT/T/assert_zero
                     SVA.sv(37)                          0          1
/TOP/DUT/T/assert_max
                     SVA.sv(39)                          0          1
/TOP/TEST/#ublk#95084642#14/immed__15
                     counter_tb.sv(15)                   0          1

Total Coverage By Instance (filtered view): 100.00%
```