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Project_1

I. Verification plan

Label	Description	Stimulus Generation	Functional Coverage	Functionality Check
FIFO_RST	When the reset (rst_n) is asserted (high), all FIFO entries should be cleared, and the output signals should be zero.	Initial testing involves directly asserting the reset signal to clear the FIFO, followed by randomized testing.	Functional coverage is not applied to the reset signal.	The output should be zero; this is validated by the check_data function to ensure proper reset behavior.
FIFO_WRITE	If wr_en is active and rd_en is deasserted, the FIFO should store the incoming data_in if it's not full.	Random stimuli are generated with constraints on the wr_en and data_in signals to simulate various write conditions.	A coverpoint for both wr_en and the full signal is included to verify the functionality when writing data into the FIFO.	The output is validated using the check_data function, ensuring the data is properly written when conditions are met.
FIFO_READ	When rd_en is active and wr_en is deasserted, the FIFO should output the stored data if it's not empty.	Random stimulus generated under constraints on the rd_en signal to simulate reading conditions.	A coverpoint for the rd_en and empty signal is included to verify proper reading functionality when enabled.	The output is cross-checked using the check_data function to ensure correct data retrieval from the FIFO.
FIFO_RW	When both rd_en and wr_en are active, priority is given based on the FIFO's state: read operation occurs if it's full, otherwise write.	No randomization occurs here as specific directed tests are performed to ensure simultaneous read and write operations behave correctly.	Nine coverpoints for both rd_en, wr_en, and various output flags, alongside cross-coverage for different scenarios.	The functionality is checked using the check_data function to verify behavior in all possible simultaneous read/write operations.

II. RTL Design

```
1  module FIFO(FIFO_if.DUT if_obj);
2  // declaration of max. FIFO address
3  localparam max_fifo_addr = $clog2(if_obj.FIFO_DEPTH);
4  // declaration of Memory (FIFO)
5  reg [if_obj.FIFO_WIDTH-1:0] mem [if_obj.FIFO_DEPTH-1:0];
6  // Declaration of read & write pointers
7  reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
8  reg [max_fifo_addr:0] count;
9  // always block specialized for writing operation
10 always @(posedge if_obj.clk or negedge if_obj.rst_n) begin
11     if (!if_obj.rst_n) begin
12         wr_ptr <= 0;
13         if_obj.overflow <= 0;
14         if_obj.wr_ack <= 0;
15     end
16     else if (if_obj.wr_en && count < if_obj.FIFO_DEPTH) begin
17         mem[wr_ptr] <= if_obj.data_in;
18         if_obj.wr_ack <= 1;
19         wr_ptr <= wr_ptr + 1;
20     end
21     else begin
22         if_obj.wr_ack <= 0;
23         if (if_obj.full && if_obj.wr_en)
24             if_obj.overflow <= 1;
25         else
26             if_obj.overflow <= 0;
27     end
28 end
29 // always block specialized for reading operation
30 always @(posedge if_obj.clk or negedge if_obj.rst_n) begin
31     if (!if_obj.rst_n) begin
32         rd_ptr <= 0;
33         if_obj.underflow <= 0;
34         if_obj.data_out <= 0;
35     end
36     else if (if_obj.rd_en && count != 0) begin
37         if_obj.data_out <= mem[rd_ptr];
38         rd_ptr <= rd_ptr + 1;
39     end
40     else
41     begin
42         if(if_obj.empty && if_obj.rd_en)
43             if_obj.underflow <= 1;
44         else
45             if_obj.underflow <= 0;
46     end
47 end
```

```

1 // always block specialized for counter signal
2 always @(posedge if_obj.clk or negedge if_obj.rst_n) begin
3     if (!if_obj.rst_n) begin
4         count <= 0;
5     end
6     else begin
7         if (({if_obj.wr_en, if_obj.rd_en} == 2'b10) && !if_obj.full)
8             count <= count + 1;
9         else if (({if_obj.wr_en, if_obj.rd_en} == 2'b01) && !if_obj.empty)
10            count <= count - 1;
11        else if (({if_obj.wr_en, if_obj.rd_en} == 2'b11) && if_obj.full)      // priority for write operation
12            count <= count - 1;
13        else if (({if_obj.wr_en, if_obj.rd_en} == 2'b11) && if_obj.empty)      // priority for read operation
14            count <= count + 1;
15    end
16 end
17 // continuous assignment for the combinational outputs
18 assign if_obj.full = (count == if_obj.FIFO_DEPTH)? 1 : 0;
19 assign if_obj.empty = (count == 0)? 1 : 0;
20 assign if_obj.almostfull = (count == if_obj.FIFO_DEPTH-1)? 1 : 0;
21 assign if_obj.almostempty = (count == 1)? 1 : 0;
22 // Assertions to the DUT
23 // ifdef SIM
24 property p1;
25 @(posedge if_obj.clk) disable iff(!if_obj.rst_n) (if_obj.wr_en && !if_obj.full) |=> if_obj.wr_ack ;
26 endproperty
27 write_acknowledge : assert property(p1);
28 write_acknowledge_cover : cover property(p1);
29 property p2;
30 @(posedge if_obj.clk) disable iff(!if_obj.rst_n) (if_obj.empty && if_obj.rd_en) |=> if_obj.underflow ;
31 endproperty
32 underflow_assertion : assert property(p2);
33 underflow_cover : cover property(p2);
34 property p3;
35 @(posedge if_obj.clk) disable iff(!if_obj.rst_n) (if_obj.full & if_obj.wr_en) |=> if_obj.overflow ;
36 endproperty
37 overflow_assertion : assert property(p3);
38 overflow_cover : cover property(p3);
39 property p4;
40 @(posedge if_obj.clk) disable iff(!if_obj.rst_n) (!if_obj.full & if_obj.wr_en & !if_obj.rd_en) |=> (count == $past(count) + 4'b0001 ) ;
41 endproperty
42 increment_assertion : assert property(p4);
43 increment_cover : cover property(p4);
44 property p5;
45 @(posedge if_obj.clk) disable iff(!if_obj.rst_n) (!if_obj.empty && if_obj.rd_en && !if_obj.wr_en) |=> (count == $past(count) - 4'b0001 ) ;
46 endproperty
47 decrement_assertion : assert property(p5);
48 decrement_cover : cover property(p5);
49 property p6;
50 @(posedge if_obj.clk) disable iff(!if_obj.rst_n) (count == if_obj.FIFO_DEPTH) |-> if_obj.full ;
51 endproperty
52 full_assertion : assert property(p6);
53 full_cover : cover property(p6);
54 property p7;
55 @(posedge if_obj.clk) disable iff(!if_obj.rst_n) (count == 0) |-> if_obj.empty ;
56 endproperty
57 empty_assertion : assert property(p7);
58 empty_cover : cover property(p7);
59 property p8;
60 @(posedge if_obj.clk) disable iff(!if_obj.rst_n) (count == if_obj.FIFO_DEPTH-1) |-> if_obj.almostfull ;
61 endproperty
62 almostfull_assertion : assert property(p8);
63 almostfull_cover : cover property(p8);
64 property p9;
65 @(posedge if_obj.clk) disable iff(!if_obj.rst_n) (count == 1) |-> if_obj.almostempty ;
66 endproperty
67 almostempty_assertion : assert property(p9);
68 almostempty_cover : cover property(p9);
69 //`endif
70 endmodule

```

III. Shared Package

```
1 package shared_pkg;
2
3 bit test_finished; // signal refer to the end of the test bench
4 //counters declaration
5 int error_count, correct_count;
6 endpackage
7
```

IV. Package 1

```
1 package FIFO_transaction_pkg;
2
3 class FIFO_transaction;
4
5 parameter FIFO_WIDTH = 16 ;
6 parameter FIFO_DEPTH = 8 ;
7
8 rand bit [FIFO_WIDTH-1:0] data_in;
9 rand bit rst_n, wr_en, rd_en;
10 Logic [FIFO_WIDTH-1:0] data_out;
11 Logic wr_ack, overflow;
12 Logic full, empty, almostfull, almostempty, underflow;
13
14 // weighted dist. for the read & write enables
15 int WR_EN_ON_DIST = 70 ;
16 int RD_EN_ON_DIST = 30 ;
17
18 // constraint blocks for the read_enable & write_enable & reset
19 constraint c_reset { rst_n dist{ 0:/2 , 1:/98 }; }
20
21 constraint c_write { wr_en dist { 0:/(100-WR_EN_ON_DIST) , 1:/(WR_EN_ON_DIST) }; }
22
23 constraint c_read { rd_en dist { 0:/(100-RD_EN_ON_DIST) , 1:/(RD_EN_ON_DIST) }; }
24
25 // Extra constraint block for write operation only
26 constraint write_only { rst_n == 1; wr_en == 1; rd_en == 0; }
27
28 // Extra constraint block for read operation only
29 constraint read_only { rst_n == 1; wr_en == 0; rd_en == 1; }
30
31 endclass
32
33 endpackage
34
```

V. Package 2

```
1 package FIFO_coverage_pkg ;
2 import FIFO_transaction_pkg ::*;
3 class FIFO_coverage;
4 FIFO_transaction F_cvg_txn ;
5 function void sample_data (input FIFO_transaction F_txn );
6 F_cvg_txn = F_txn ;
7 cg.sample();
8 endfunction
9 covergroup cg ;
10
11 // Here we create cover point for each signal to be used in the cross coverage
12 wr_en_cp : coverpoint F_cvg_txn.wr_en;
13 rd_en_cp : coverpoint F_cvg_txn.rd_en;
14 wr_ack_cp : coverpoint F_cvg_txn.wr_ack;
15 full_cp : coverpoint F_cvg_txn.full;
16 empty_cp : coverpoint F_cvg_txn.empty;
17 almostfull_cp : coverpoint F_cvg_txn.almostfull;
18 almostempty_cp : coverpoint F_cvg_txn.almostempty;
19 overflow_cp : coverpoint F_cvg_txn.overflow;
20 underflow_cp : coverpoint F_cvg_txn.underflow;
21
22 // Here we create cross coverage for each output with read enable & write enable except(dout)
23 wr_rd_wr_ack_cross : cross wr_en_cp , rd_en_cp , wr_ack_cp
24 {
25     ignore_bins write_active_with_wr_ack = ! binsof(wr_en_cp) intersect {1} && binsof(wr_ack_cp) intersect {1};
26     ignore_bins read_write_active_with_wr_ack = ! binsof(wr_en_cp) intersect {1} && binsof(rd_en_cp) intersect {1} && binsof(wr_ack_cp) intersect {1};
27 }
28
29 wr_rd_full_cross : cross wr_en_cp , rd_en_cp , full_cp
30 {
31     ignore_bins write_active_with_full = ! binsof(wr_en_cp) intersect {1} && binsof(full_cp) intersect {1};
32     ignore_bins read_active_with_full = binsof(rd_en_cp) intersect {1} && binsof(full_cp) intersect {1};
33 }
34
35 wr_rd_empty_cross : cross wr_en_cp , rd_en_cp , empty_cp
36 {
37     ignore_bins read_active_with_empty = ! binsof(rd_en_cp) intersect {1} && binsof(empty_cp) intersect {1};
38 }
39
40 wr_rd_overflow_cross : cross wr_en_cp , rd_en_cp , overflow_cp
41 {
42     ignore_bins write_active_with_overflow = ! binsof(wr_en_cp) intersect {1} && binsof(overflow_cp) intersect {1};
43 }
44
45 wr_rd_underflow_cross : cross wr_en_cp , rd_en_cp , underflow_cp
46 {
47     ignore_bins read_active_with_underflow = ! binsof(rd_en_cp) intersect {1} && binsof(underflow_cp) intersect {1};
48 }
49
50 wr_rd_almostfull_cross : cross wr_en_cp , rd_en_cp , almostfull_cp
51 {
52     ignore_bins write_active_with_almostfull = ! binsof(wr_en_cp) intersect {1} && binsof(almostfull_cp) intersect {1};
53     ignore_bins read_write_active_with_almostfull = ! binsof(wr_en_cp) intersect {1} && binsof(rd_en_cp) intersect {1} && binsof(almostfull_cp) intersect {1};
54 }
55
56 wr_rd_almostempty_cross : cross wr_en_cp , rd_en_cp , almostempty_cp
57 {
58     ignore_bins read_active_with_almostempty = ! binsof(rd_en_cp) intersect {1} && binsof(almostempty_cp) intersect {1};
59     ignore_bins read_write_active_with_almostempty = ! binsof(wr_en_cp) intersect {1} && binsof(rd_en_cp) intersect {1} && binsof(almostempty_cp) intersect {1};
60 }
61
62 endgroup
63 function new();
64     cg = new ;
65     F_cvg_txn = new;
66 endfunction
67 endclass
68 endpackage
69
```

VI. Package 3

```
1 package FIFO_scoreboard_pkg ;
2 import FIFO_transaction_pkg ::::*;
3 import shared_pkg::*;
4 class FIFO_scoreboard ;
5 parameter FIFO_WIDTH = 16 ;
6 parameter FIFO_DEPTH = 8 ;
7 bit [FIFO_WIDTH-1 : 0] data_out_ref;
8 bit wr_ack_ref, overflow_ref;
9 bit full_ref, empty_ref, almostfull_ref, almostempty_ref, underflow_ref;
10 int counter ;
11 bit [FIFO_WIDTH-1:0] queue[$] ; // declared queue to check the FIFO
12 FIFO_transaction obj = new();
13 function void flags();
14 full_ref = (counter == FIFO_DEPTH)? 1 : 0;
15 empty_ref = (counter == 0)? 1 : 0;
16 almostfull_ref = (counter == FIFO_DEPTH-1)? 1 : 0;
17 almostempty_ref = (counter == 1)? 1 : 0;
18 endfunction
19 function void check_data(input FIFO_transaction obj);
20 logic [6:0] flags_ref , flags_dut;
21 reference_model(obj);
22 flags_ref = {wr_ack_ref, overflow_ref, full_ref, empty_ref, almostfull_ref, almostempty_ref, underflow_ref};
23 flags_dut = {obj.wr_ack, obj.overflow, obj.full, obj.empty, obj.almostfull, obj.almostempty, obj.underflow};
24
25 if( (obj.data_out == data_out_ref) && (flags_dut == flags_ref) ) begin
26 $display("At time = %0t , The queue = %p",$time,queue);
27 correct_count++;
28 end
29 else begin
30 error_count++;
31 $display("at time = %0t , the outputs of the DUT doesn't Match with the Golden model outputs",$time);
32 end
33 endfunction
34 function void reference_model(input FIFO_transaction obj_gold);
35 fork
36 begin
37 if (!obj_gold.rst_n) begin
```



```
1      wr_ack_ref = 0;
2      full_ref = 0;
3      almostfull_ref = 0;
4      overflow_ref = 0;
5      counter = 0;
6      queue.delete();
7  end
8  else if (obj_gold.wr_en && counter < obj_gold.FIFO_DEPTH) begin
9      queue.push_back(obj_gold.data_in) ;
10     wr_ack_ref = 1;
11  end
12  else begin
13      wr_ack_ref = 0;
14      if (full_ref && obj_gold.wr_en)
15          overflow_ref = 1;
16      else
17          overflow_ref = 0;
18  end
19 end
20 begin  if(!obj_gold.rst_n) begin
21     data_out_ref = 0;
22     empty_ref = 1;
23     almostempty_ref = 0;
24     underflow_ref = 0;
25 end
26 else if ( obj_gold.rd_en && counter != 0 ) begin
27     data_out_ref = queue.pop_front();
28 end
29 else begin
30     if(empty_ref && obj_gold.rd_en)
31         underflow_ref = 1 ;
32     else
33         underflow_ref = 0 ;
34 end
35 end
36 join
37 if(!obj_gold.rst_n) begin
38     counter = 0;
39 end
40 else if ( ({obj_gold.wr_en, obj_gold.rd_en} == 2'b10) && !full_ref)
41     counter = counter + 1;
42 else if ( ({obj_gold.wr_en, obj_gold.rd_en} == 2'b01) && !empty_ref)
43     counter = counter - 1;
44 else if ( ({obj_gold.wr_en, obj_gold.rd_en} == 2'b11) && full_ref)
45     counter = counter - 1;
46 else if ( ({obj_gold.wr_en, obj_gold.rd_en} == 2'b11) && empty_ref)
47     counter = counter + 1;
48 flags();
49 endfunction
50 endclass
51 endpackage
```

VII. Monitor

```
1 import shared_pkg ::*;
2
3 import FIFO_transaction_pkg ::*;
4
5 import FIFO_coverage_pkg ::*;
6
7 import FIFO_scoreboard_pkg ::*;
8
9 module FIFO_monitor (FIFO_if.MONITOR if_obj);
10
11 // create obj for each class
12 FIFO_transaction obj_trans ;
13 FIFO_scoreboard obj_score ;
14 FIFO_coverage obj_cov ;
15
16 initial begin
17
18     obj_trans = new();
19     obj_score = new();
20     obj_cov = new();
21
22 forever begin
23
24     @(negedge if_obj.clk);
25
26     // sample input data
27     obj_trans.data_in = if_obj.data_in ;
28     obj_trans.rst_n = if_obj.rst_n ;
29     obj_trans.wr_en = if_obj.wr_en ;
30     obj_trans.rd_en = if_obj.rd_en ;
31
32     // sample output data
33     obj_trans.data_out = if_obj.data_out ;
34     obj_trans.wr_ack = if_obj.wr_ack ;
35     obj_trans.overflow = if_obj.overflow ;
36     obj_trans.full = if_obj.full ;
37     obj_trans.empty = if_obj.empty ;
38     obj_trans.almostfull = if_obj.almostfull ;
39     obj_trans.almostempty = if_obj.almostempty ;
40     obj_trans.underflow = if_obj.underflow ;
41
42 fork
43
44     begin
45         obj_cov.sample_data(obj_trans);
46     end
47
48     begin
49         @(posedge if_obj.clk);
50         #10;
51         obj_score.check_data(obj_trans);
52     end
53
54 join
55
56 if(test_finished == 1) begin
57     $display("Final values stored in the queue = %p ",obj_score.queue);
58     $display("no.of error_count :");
59     ,no$eforcorrect_count :
60     #error_count , correct_count);
61
62 end
63
64 end
65 endmodule
66
```

VIII. Interface module

```
1 interface FIFO_if (input bit clk);
2 // parameter Declaration
3 parameter FIFO_WIDTH = 16;
4 parameter FIFO_DEPTH = 8;
5 //input declaration
6 logic [FIFO_WIDTH-1:0] data_in;
7 logic rst_n, wr_en, rd_en;
8 //output declaration
9 logic [FIFO_WIDTH-1:0] data_out;
10 logic wr_ack, overflow;
11 logic full, empty, almostfull, almostempty, underflow;
12
13
14 modport DUT (input clk, data_in, rst_n, wr_en, rd_en, output data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow);
15
16 modport TEST (input clk, data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow, output data_in, rst_n, wr_en, rd_en);
17
18 modport MONITOR (input clk, data_in, rst_n, wr_en, rd_en, data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow);
19
20 endinterface
21
```

IX. Top module

```
1 module TOP;
2
3 bit clk ;
4 initial begin
5     clk = 0;
6     forever begin
7         #25;
8         clk = ~clk;
9     end
10 end
11
12 FIFO_if if_obj(clk);
13
14 FIFO DUT (if_obj);
15
16 FIFO_tb TEST (if_obj);
17
18 FIFO_monitor MONITOR(if_obj);
19
20 endmodule
21
```

X. Test bench

```
1 import shared_pkg::*;
2 import FIFO_transaction_pkg::*;
3 module FIFO_tb(FIFO_if.TEST if_obj);
4 FIFO_transaction obj_test ;
5 // we choose values
6 localparam MIXED_TESTS = 9900;
7 localparam WRITE_TESTS = 50;
8 localparam READ_TESTS = 50;
9
10 initial begin
11   obj_test = new();
12   if_obj.rst_n = 0;
13   repeat(2) @(negedge if_obj.clk);
14   if_obj.rst_n = 1;
15   obj_test.constraint_mode(0);
16   obj_test.write_only.constraint_mode(1);
17   repeat(WRITE_TESTS) begin
18     assert(obj_test.randomize());
19     if_obj.rst_n = obj_test.rst_n ;
20     if_obj.rd_en = obj_test.rd_en ;
21     if_obj.wr_en = obj_test.wr_en ;
22     if_obj.data_in = obj_test.data_in ;
23     @(negedge if_obj.clk);
24   end
25   obj_test.constraint_mode(0);
26   obj_test.read_only.constraint_mode(1);
27   obj_test.data_in.rand_mode(0);
28   repeat(READ_TESTS) begin
29     assert(obj_test.randomize());
30     if_obj.rst_n = obj_test.rst_n ;
31     if_obj.rd_en = obj_test.rd_en ;
32     if_obj.wr_en = obj_test.wr_en ;
33     if_obj.data_in = obj_test.data_in ;
34     @(negedge if_obj.clk);
35   end
36
37   obj_test.constraint_mode(1);
38   obj_test.data_in.rand_mode(1);
39   obj_test.read_only.constraint_mode(0);
40   obj_test.write_only.constraint_mode(0);
41   repeat(MIXED_TESTS) begin
42     assert(obj_test.randomize());
43     if_obj.rst_n = obj_test.rst_n ;
44     if_obj.rd_en = obj_test.rd_en ;
45     if_obj.wr_en = obj_test.wr_en ;
46     if_obj.data_in = obj_test.data_in ;
47     @(negedge if_obj.clk);
48   end
49
50   test_finished = 1 ;
51
52 end
53 endmodule
54
55
```

XI. Print


```

# At time = 419885 , The queue = '{22926, 46462, 51512, 26239, 6984}
# At time = 419935 , The queue = '{22926, 46462, 51512, 26239, 6984}
# At time = 419985 , The queue = '{}'
# At time = 420035 , The queue = '{}'
# At time = 420085 , The queue = '{}'
# At time = 420135 , The queue = '{}'
# At time = 420185 , The queue = '{}'
# At time = 420235 , The queue = '{}'
# At time = 420285 , The queue = '{55520}'
# At time = 420335 , The queue = '{55520}'
# At time = 420385 , The queue = '{55520}'
# At time = 420435 , The queue = '{55520}'
# At time = 420485 , The queue = '{55520, 8803}'
# At time = 420535 , The queue = '{55520, 8803, 36777}'
# At time = 420585 , The queue = '{55520, 8803, 36777, 23021}'
# At time = 420635 , The queue = '{8803, 36777, 23021}'
# At time = 420685 , The queue = '{8803, 36777, 23021, 2478}'
# At time = 420735 , The queue = '{8803, 36777, 23021, 2478}'
# At time = 420785 , The queue = '{8803, 36777, 23021, 2478}'
# At time = 420835 , The queue = '{8803, 36777, 23021, 2478, 54191}'
# At time = 420885 , The queue = '{8803, 36777, 23021, 2478, 54191, 28618}'
# At time = 420935 , The queue = '{36777, 23021, 2478, 54191, 28618}'
# At time = 420985 , The queue = '{36777, 23021, 2478, 54191, 28618}'
# At time = 421035 , The queue = '{36777, 23021, 2478, 54191, 28618, 15131}'
# At time = 421085 , The queue = '{23021, 2478, 54191, 28618, 15131, 41437}'
# At time = 421135 , The queue = '{23021, 2478, 54191, 28618, 15131, 41437}'
# At time = 421185 , The queue = '{23021, 2478, 54191, 28618, 15131, 41437}'
# At time = 421235 , The queue = '{23021, 2478, 54191, 28618, 15131, 41437, 37800}'
# At time = 421285 , The queue = '{23021, 2478, 54191, 28618, 15131, 41437, 37800}'
# At time = 421335 , The queue = '{2478, 54191, 28618, 15131, 41437, 37800, 34178}'
# At time = 421385 , The queue = '{54191, 28618, 15131, 41437, 37800, 34178, 6568}'
# At time = 421435 , The queue = '{28618, 15131, 41437, 37800, 34178, 6568, 50272}'
# At time = 421485 , The queue = '{28618, 15131, 41437, 37800, 34178, 6568, 50272}'
# At time = 421535 , The queue = '{28618, 15131, 41437, 37800, 34178, 6568, 50272, 12926}'
# At time = 421585 , The queue = '{}'
# At time = 421635 , The queue = '{18279}'
# At time = 421685 , The queue = '{18279}'
# At time = 421735 , The queue = '{18742}'
# At time = 421785 , The queue = '{18742}'
# At time = 421835 , The queue = '{13014}'
# At time = 421885 , The queue = '{13014, 38116}'
# At time = 421935 , The queue = '{13014, 38116, 34402}'
# At time = 421985 , The queue = '{13014, 38116, 34402, 35436}'
# At time = 422035 , The queue = '{13014, 38116, 34402, 35436}'
# At time = 422085 , The queue = '{38116, 34402, 35436, 21502}'
# At time = 422135 , The queue = '{38116, 34402, 35436, 21502, 43728}'
# At time = 422185 , The queue = '{34402, 35436, 21502, 43728, 52243}'
# At time = 422235 , The queue = '{35436, 21502, 43728, 52243, 35991}'
# At time = 422285 , The queue = '{35436, 21502, 43728, 52243, 35991, 52254}'
# At time = 422335 , The queue = '{21502, 43728, 52243, 35991, 52254, 5789}'
# At time = 422385 , The queue = '{21502, 43728, 52243, 35991, 52254, 5789, 1344}'
# At time = 422435 , The queue = '{21502, 43728, 52243, 35991, 52254, 5789, 1344, 49840}'
# At time = 422485 , The queue = '{43728, 52243, 35991, 52254, 5789, 1344, 49840}'
# At time = 422535 , The queue = '{52243, 35991, 52254, 5789, 1344, 49840, 13873}'
# At time = 422585 , The queue = '{52243, 35991, 52254, 5789, 1344, 49840, 13873, 10161}'
# At time = 422635 , The queue = '{52243, 35991, 52254, 5789, 1344, 49840, 13873, 10161}'
# At time = 422685 , The queue = '{52243, 35991, 52254, 5789, 1344, 49840, 13873, 10161}'
# At time = 422735 , The queue = '{35991, 52254, 5789, 1344, 49840, 13873, 10161}'
# At time = 422785 , The queue = '{}'
# At time = 422835 , The queue = '{}'
# At time = 422885 , The queue = '{41225}'
# At time = 422935 , The queue = '{36704}'
# At time = 422985 , The queue = '{30098}'
# At time = 423035 , The queue = '{30098, 33417}'
# At time = 423085 , The queue = '{30098, 33417, 2581}'
# At time = 423135 , The queue = '{30098, 33417, 2581, 64092}'
# At time = 423185 , The queue = '{33417, 2581, 64092, 52105}'
# At time = 423235 , The queue = '{33417, 2581, 64092, 52105, 33514}'
# At time = 423285 , The queue = '{33417, 2581, 64092, 52105, 33514, 56196}'
# At time = 423335 , The queue = '{33417, 2581, 64092, 52105, 33514, 56196}'
# At time = 423385 , The queue = '{2581, 64092, 52105, 33514, 56196}'
# At time = 423435 , The queue = '{2581, 64092, 52105, 33514, 56196}'
# At time = 423485 , The queue = '{2581, 64092, 52105, 33514, 56196, 3392}'
# At time = 423535 , The queue = '{2581, 64092, 52105, 33514, 56196, 3392, 49580}'
# At time = 423585 , The queue = '{2581, 64092, 52105, 33514, 56196, 3392, 49580, 39015}'
# At time = 423635 , The queue = '{64092, 52105, 33514, 56196, 3392, 49580, 39015}'
# At time = 423685 , The queue = '{64092, 52105, 33514, 56196, 3392, 49580, 39015}'
# At time = 423735 , The queue = '{64092, 52105, 33514, 56196, 3392, 49580, 39015, 37648}'
# At time = 423785 , The queue = '{64092, 52105, 33514, 56196, 3392, 49580, 39015, 37648}'
# At time = 423835 , The queue = '{64092, 52105, 33514, 56196, 3392, 49580, 39015, 37648}'
# At time = 423885 , The queue = '{64092, 52105, 33514, 56196, 3392, 49580, 39015, 37648}'
# At time = 423935 , The queue = '{64092, 52105, 33514, 56196, 3392, 49580, 39015, 37648}'
# At time = 423985 , The queue = '{52105, 33514, 56196, 3392, 49580, 39015, 37648}'
# At time = 424035 , The queue = '{52105, 33514, 56196, 3392, 49580, 39015, 37648, 48066}'
# At time = 424085 , The queue = '{}'
# At time = 424135 , The queue = '{34791}'
# At time = 424185 , The queue = '{}'
# At time = 424235 , The queue = '{56744}'
# At time = 424285 , The queue = '{56744, 55386}'
# At time = 424335 , The queue = '{56744, 55386, 4124}'
# At time = 424385 , The queue = '{55386, 4124, 23422}'
# At time = 424435 , The queue = '{55386, 4124, 23422, 1485}'
# At time = 424485 , The queue = '{4124, 23422, 1485}'
# At time = 424535 , The queue = '{4124, 23422, 1485}'
# At time = 424585 , The queue = '{23422, 1485, 12809}'
# At time = 424635 , The queue = '{23422, 1485, 12809}

```



```

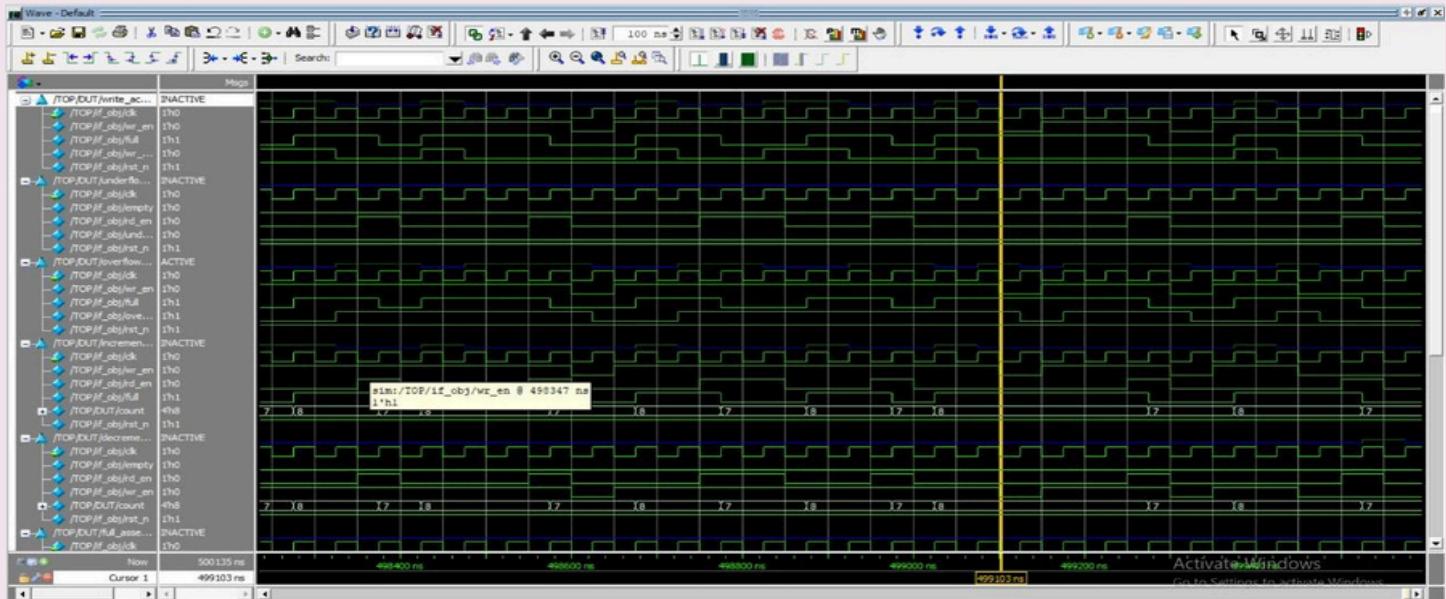
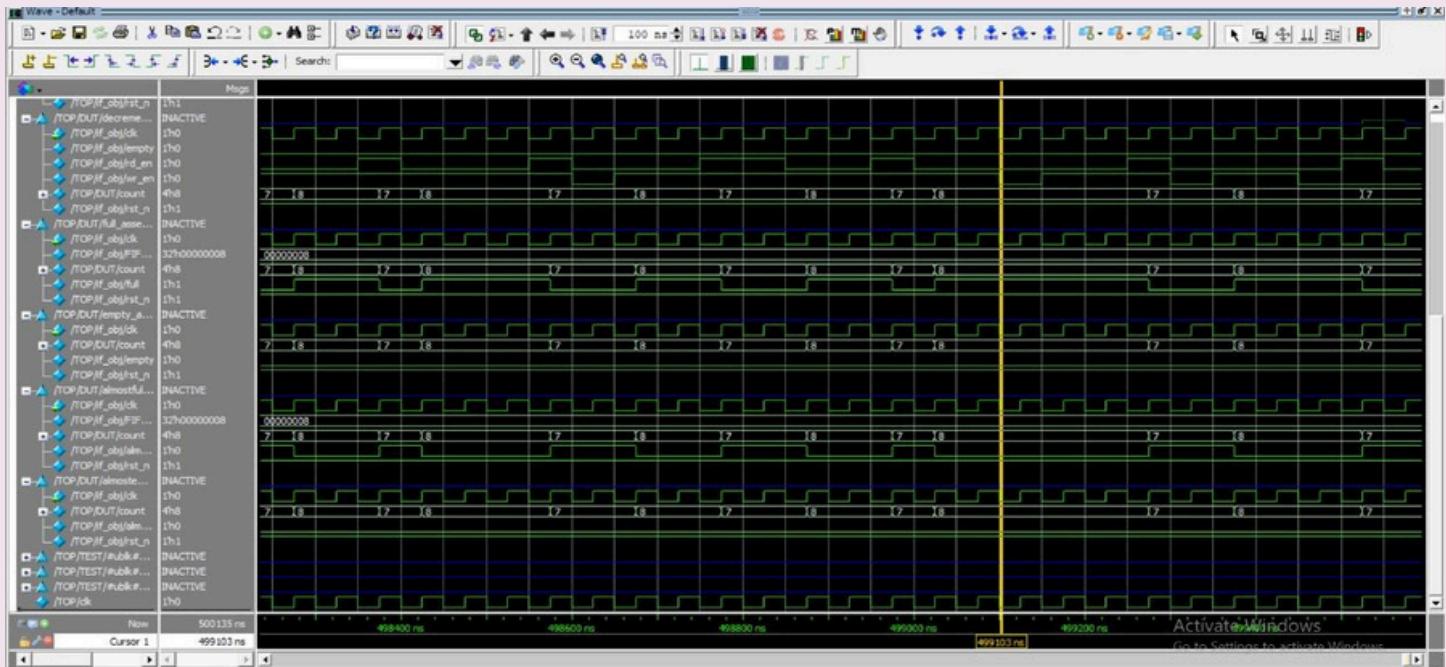
# At time = 495835 , The queue = '{59203, 52534, 24913, 17216, 23449}
# At time = 495885 , The queue = '{59203, 52534, 24913, 17216, 23449}
# At time = 495935 , The queue = '{59203, 52534, 24913, 17216, 23449}
# At time = 495985 , The queue = '{52534, 24913, 17216, 23449}
# At time = 496035 , The queue = '{52534, 24913, 17216, 23449}
# At time = 496085 , The queue = '{52534, 24913, 17216, 23449}
# At time = 496135 , The queue = '{24913, 17216, 23449, 44200}
# At time = 496185 , The queue = '{24913, 17216, 23449, 44200}
# At time = 496235 , The queue = '{24913, 17216, 23449, 44200, 15115}
# At time = 496285 , The queue = '{17216, 23449, 44200, 15115}
# At time = 496335 , The queue = '{23449, 44200, 15115}
# At time = 496385 , The queue = '{23449, 44200, 15115, 1012}
# At time = 496435 , The queue = '{23449, 44200, 15115, 1012}
# At time = 496485 , The queue = '{44200, 15115, 1012}
# At time = 496535 , The queue = '{44200, 15115, 1012, 22197}
# At time = 496585 , The queue = '{44200, 15115, 1012, 22197, 51008}
# At time = 496635 , The queue = '{44200, 15115, 1012, 22197, 51008, 16745}
# At time = 496685 , The queue = '{44200, 15115, 1012, 22197, 51008, 16745}
# At time = 496735 , The queue = '{44200, 15115, 1012, 22197, 51008, 16745}
# At time = 496785 , The queue = '{15115, 1012, 22197, 51008, 16745, 57217}
# At time = 496835 , The queue = '{15115, 1012, 22197, 51008, 16745, 57217, 54876}
# At time = 496885 , The queue = '{15115, 1012, 22197, 51008, 16745, 57217, 54876, 54165}
# At time = 496935 , The queue = '{15115, 1012, 22197, 51008, 16745, 57217, 54876, 54165}
# At time = 496985 , The queue = '{15115, 1012, 22197, 51008, 16745, 57217, 54876, 54165}
# At time = 497035 , The queue = '{15115, 1012, 22197, 51008, 16745, 57217, 54876, 54165}
# At time = 497085 , The queue = '{1012, 22197, 51008, 16745, 57217, 54876, 54165}
# At time = 497135 , The queue = '{22197, 51008, 16745, 57217, 54876, 54165}
# At time = 497185 , The queue = '{22197, 51008, 16745, 57217, 54876, 54165, 53636}
# At time = 497235 , The queue = '{51008, 16745, 57217, 54876, 54165, 53636, 60332}
# At time = 497285 , The queue = '{51008, 16745, 57217, 54876, 54165, 53636, 60332, 38115}
# At time = 497335 , The queue = '{51008, 16745, 57217, 54876, 54165, 53636, 60332, 38115}
# At time = 497385 , The queue = '{}'
# At time = 497435 , The queue = '{50267}
# At time = 497485 , The queue = '{6182}
# At time = 497535 , The queue = '{6182, 53165}
# At time = 497585 , The queue = '{6182, 53165}
# At time = 497635 , The queue = '{}'
# At time = 497685 , The queue = '{22885}
# At time = 497735 , The queue = '{22885}
# At time = 497785 , The queue = '{22885}
# At time = 497835 , The queue = '{22885}
# At time = 497885 , The queue = '{22885, 41413}
# At time = 497935 , The queue = '{41413, 62184}
# At time = 497985 , The queue = '{41413, 62184, 15617}
# At time = 498035 , The queue = '{62184, 15617, 64402}
# At time = 498085 , The queue = '{62184, 15617, 64402, 10781}
# At time = 498135 , The queue = '{62184, 15617, 64402, 10781, 50738}
# At time = 498185 , The queue = '{62184, 15617, 64402, 10781, 50738}
# At time = 498235 , The queue = '{62184, 15617, 64402, 10781, 50738, 20724}
# At time = 498285 , The queue = '{62184, 15617, 64402, 10781, 50738, 20724, 19169}
# At time = 498335 , The queue = '{62184, 15617, 64402, 10781, 50738, 20724, 19169, 36425}
# At time = 498385 , The queue = '{62184, 15617, 64402, 10781, 50738, 20724, 19169, 36425}
# At time = 498435 , The queue = '{15617, 64402, 10781, 50738, 20724, 19169, 36425}
# At time = 498485 , The queue = '{15617, 64402, 10781, 50738, 20724, 19169, 36425, 29577}
# At time = 498535 , The queue = '{15617, 64402, 10781, 50738, 20724, 19169, 36425, 29577}
# At time = 498585 , The queue = '{15617, 64402, 10781, 50738, 20724, 19169, 36425, 29577}
# At time = 498635 , The queue = '{64402, 10781, 50738, 20724, 19169, 36425, 29577}
# At time = 498685 , The queue = '{64402, 10781, 50738, 20724, 19169, 36425, 29577}
# At time = 498735 , The queue = '{64402, 10781, 50738, 20724, 19169, 36425, 29577, 337}
# At time = 498785 , The queue = '{64402, 10781, 50738, 20724, 19169, 36425, 29577, 337}
# At time = 498835 , The queue = '{10781, 50738, 20724, 19169, 36425, 29577, 337}
# At time = 498885 , The queue = '{50738, 20724, 19169, 36425, 29577, 337, 4213}
# At time = 498935 , The queue = '{50738, 20724, 19169, 36425, 29577, 337, 4213, 22658}
# At time = 498985 , The queue = '{50738, 20724, 19169, 36425, 29577, 337, 4213, 22658}
# At time = 499035 , The queue = '{20724, 19169, 36425, 29577, 337, 4213, 22658}
# At time = 499085 , The queue = '{20724, 19169, 36425, 29577, 337, 4213, 22658, 25004}
# At time = 499135 , The queue = '{20724, 19169, 36425, 29577, 337, 4213, 22658, 25004}
# At time = 499185 , The queue = '{20724, 19169, 36425, 29577, 337, 4213, 22658, 25004}
# At time = 499235 , The queue = '{20724, 19169, 36425, 29577, 337, 4213, 22658, 25004}
# At time = 499285 , The queue = '{20724, 19169, 36425, 29577, 337, 4213, 22658, 25004}
# At time = 499335 , The queue = '{19169, 36425, 29577, 337, 4213, 22658, 25004}
# At time = 499385 , The queue = '{19169, 36425, 29577, 337, 4213, 22658, 25004}
# At time = 499435 , The queue = '{19169, 36425, 29577, 337, 4213, 22658, 25004, 59877}
# At time = 499485 , The queue = '{19169, 36425, 29577, 337, 4213, 22658, 25004, 59877}
# At time = 499535 , The queue = '{19169, 36425, 29577, 337, 4213, 22658, 25004, 59877}
# At time = 499585 , The queue = '{36425, 29577, 337, 4213, 22658, 25004, 59877}
# At time = 499635 , The queue = '{36425, 29577, 337, 4213, 22658, 25004, 59877}
# At time = 499685 , The queue = '{36425, 29577, 337, 4213, 22658, 25004, 59877, 49196}
# At time = 499735 , The queue = '{36425, 29577, 337, 4213, 22658, 25004, 59877, 49196}
# At time = 499785 , The queue = '{29577, 337, 4213, 22658, 25004, 59877, 49196}
# At time = 499835 , The queue = '{29577, 337, 4213, 22658, 25004, 59877, 49196}
# At time = 499885 , The queue = '{29577, 337, 4213, 22658, 25004, 59877, 49196}
# At time = 499935 , The queue = '{29577, 337, 4213, 22658, 25004, 59877, 49196, 14466}
# At time = 499985 , The queue = '{29577, 337, 4213, 22658, 25004, 59877, 49196, 14466}
# At time = 500035 , The queue = '{}'
# At time = 500085 , The queue = '{}'
# At time = 500135 , The queue = '{23142}
# Final values stored in the queue = '{23142}
# no.of.error_count :0 ,no.of.correct_count :10000
# ** Note: $stop : D:/Verification course/PROJECT1/MONITOR.sv(59)
# Time: 500135 ns Iteration: 0 Instance: /TOP/MONITOR
# Break in Module FIFO_monitor at D:/Verification course/PROJECT1/MONITOR.sv line 59
coverage report -detail -cvg -directive -comments -output fcover_report.txt {}
# Causality operation skipped due to absence of debug database file
# Printing not supported.

```

XII. Do file

```
vlib work
vlog FIFO.sv package1.sv package2.sv package3.sv shared_package.sv testbench.sv MONITOR.sv interface.sv TOP.sv +cover -covercells
vsim -voptargs+=acc work.TOP -cover
add wave *
coverage save testbench.ucdb -onexit
run -all
```

XIII. Wave form



XIV. Functional Coverage Report

```
Coverage Report by instance with details

=====
== Instance: /TOP/DUT
== Design Unit: work.FIFO
=====

Directive Coverage:
  Directives      9      9      0  100.00%
DIRECTIVE COVERAGE:
-----

| Name                             | Design Unit | Design UnitType | Lang | File(Line)                                   | Hits | Status  |
|----------------------------------|-------------|-----------------|------|----------------------------------------------|------|---------|
| /TOP/DUT/write_acknowledge_cover | FIFO        | Verilog         | SVA  | D:/Verification course/PROJECT1/FIFO.sv(84)  | 3886 | Covered |
| /TOP/DUT/underflow_cover         | FIFO        | Verilog         | SVA  | D:/Verification course/PROJECT1/FIFO.sv(90)  | 154  | Covered |
| /TOP/DUT/overflow_cover          | FIFO        | Verilog         | SVA  | D:/Verification course/PROJECT1/FIFO.sv(96)  | 2753 | Covered |
| /TOP/DUT/increment_cover         | FIFO        | Verilog         | SVA  | D:/Verification course/PROJECT1/FIFO.sv(102) | 2743 | Covered |
| /TOP/DUT/decrement_cover         | FIFO        | Verilog         | SVA  | D:/Verification course/PROJECT1/FIFO.sv(108) | 831  | Covered |
| /TOP/DUT/full_cover              | FIFO        | Verilog         | SVA  | D:/Verification course/PROJECT1/FIFO.sv(114) | 4842 | Covered |
| /TOP/DUT/empty_cover             | FIFO        | Verilog         | SVA  | D:/Verification course/PROJECT1/FIFO.sv(120) | 394  | Covered |
| /TOP/DUT/almostfull_cover        | FIFO        | Verilog         | SVA  | D:/Verification course/PROJECT1/FIFO.sv(126) | 2512 | Covered |
| /TOP/DUT/almostempty_cover       | FIFO        | Verilog         | SVA  | D:/Verification course/PROJECT1/FIFO.sv(132) | 451  | Covered |


=====
== Instance: /FIFO_coverage_pkg
== Design Unit: work.FIFO_coverage_pkg
=====

Covergroup Coverage:
  Covergroups      1      na      na  100.00%
  Coverpoints/Crosses   16      na      na      na
  Covergroup Bins     58      58      0  100.00%
-----

| Covergroup                               | Metric  | Goal | Bins | Status  |
|------------------------------------------|---------|------|------|---------|
| TYPE /FIFO_coverage_pkg/FIFO_coverage/cg | 100.00% | 100  | -    | Covered |
| covered/total bins:                      | 58      | 58   | -    |         |
| missing/total bins:                      | 0       | 58   | -    |         |
| % Hit:                                   | 100.00% | 100  | -    |         |
| Coverpoint wr_en_cp                      | 100.00% | 100  | -    | Covered |
| covered/total bins:                      | 2       | 2    | -    |         |
| missing/total bins:                      | 0       | 2    | -    |         |
| % Hit:                                   | 100.00% | 100  | -    |         |
| bin auto[0]                              | 3089    | 1    | -    | Covered |
| bin auto[1]                              | 6913    | 1    | -    | Covered |
| Coverpoint rd_en_cp                      | 100.00% | 100  | -    | Covered |
| covered/total bins:                      | 2       | 2    | -    |         |
| missing/total bins:                      | 0       | 2    | -    |         |
| % Hit:                                   | 100.00% | 100  | -    |         |
| bin auto[0]                              | 7052    | 1    | -    | Covered |
| bin auto[1]                              | 2950    | 1    | -    | Covered |
| Coverpoint wr_ack_cp                     | 100.00% | 100  | -    | Covered |
| covered/total bins:                      | 2       | 2    | -    |         |
| missing/total bins:                      | 0       | 2    | -    |         |
| % Hit:                                   | 100.00% | 100  | -    |         |
| bin auto[0]                              | 6041    | 1    | -    | Covered |
| bin auto[1]                              | 3961    | 1    | -    | Covered |
| Coverpoint full_cp                       | 100.00% | 100  | -    | Covered |
| covered/total bins:                      | 2       | 2    | -    |         |
| missing/total bins:                      | 0       | 2    | -    |         |
| % Hit:                                   | 100.00% | 100  | -    |         |
| bin auto[0]                              | 5879    | 1    | -    | Covered |
| bin auto[1]                              | 4123    | 1    | -    | Covered |
| Coverpoint empty_cp                      | 100.00% | 100  | -    | Covered |
| covered/total bins:                      | 2       | 2    | -    |         |
| missing/total bins:                      | 0       | 2    | -    |         |
| % Hit:                                   | 100.00% | 100  | -    |         |
| bin auto[0]                              | 9600    | 1    | -    | Covered |
| bin auto[1]                              | 402     | 1    | -    | Covered |
| Coverpoint almostfull_cp                 | 100.00% | 100  | -    | Covered |
| covered/total bins:                      | 2       | 2    | -    |         |
| missing/total bins:                      | 0       | 2    | -    |         |
| % Hit:                                   | 100.00% | 100  | -    |         |
| bin auto[0]                              | 7437    | 1    | -    | Covered |
| bin auto[1]                              | 2565    | 1    | -    | Covered |
| Coverpoint almostempty_cp                | 100.00% | 100  | -    | Covered |
| covered/total bins:                      | 2       | 2    | -    |         |
| missing/total bins:                      | 0       | 2    | -    |         |
| % Hit:                                   | 100.00% | 100  | -    |         |
| bin auto[0]                              | 9545    | 1    | -    | Covered |
| bin auto[1]                              | 457     | 1    | -    | Covered |
| Coverpoint overflow_cp                   | 100.00% | 100  | -    | Covered |


```

Coverpoint overflow_cp	100.00%	100	-	Covered		
covered/total bins:	2	2	-			
missing/total bins:	0	2	-			
% Hit:	100.00%	100	-			
bin auto[0]	6488	1	-	Covered		
bin auto[1]	3514	1	-	Covered		
Coverpoint underflow_cp	100.00%	100	-	Covered		
covered/total bins:	2	2	-			
missing/total bins:	0	2	-			
% Hit:	100.00%	100	-			
bin auto[0]	9814	1	-	Covered		
bin auto[1]	188	1	-	Covered		
Cross wr_rd_wr_ack_cross	100.00%	100	-	Covered		
covered/total bins:	6	6	-			
missing/total bins:	0	6	-			
% Hit:	100.00%	100	-			
Auto, Default and User Defined Bins:						
bin <auto[1],auto[1],auto[1]>	1161	1	-	Covered		
bin <auto[1],auto[0],auto[1]>	2800	1	-	Covered		
bin <auto[1],auto[1],auto[0]>	850	1	-	Covered		
bin <auto[1],auto[0],auto[0]>	2102	1	-	Covered		
bin <auto[0],auto[1],auto[0]>	939	1	-	Covered		
bin <auto[0],auto[0],auto[0]>	2150	1	-	Covered		
Illegal and Ignore Bins:						
ignore_bin read_write_active_with_wr_ack	0	-	ZERO			
ignore_bin write_active_with_wr_ack	0	-	ZERO			
Cross wr_rd_full_cross	100.00%	100	-	Covered		
covered/total bins:	5	5	-			
missing/total bins:	0	5	-			
% Hit:	100.00%	100	-			
Auto, Default and User Defined Bins:						
bin <auto[1],auto[0],auto[1]>	3246	1	-	Covered		
bin <auto[1],auto[1],auto[0]>	2011	1	-	Covered		
bin <auto[0],auto[1],auto[0]>	939	1	-	Covered		
bin <auto[1],auto[0],auto[0]>	1656	1	-	Covered		
bin <auto[0],auto[0],auto[0]>	1273	1	-	Covered		
Illegal and Ignore Bins:						
ignore_bin read_active_with_full	0	-	ZERO			
ignore_bin write_active_with_full	877	-	Occurred			
Cross wr_rd_empty_cross	100.00%	100	-	Covered		
covered/total bins:	6	6	-			
missing/total bins:	0	6	-			
% Hit:	100.00%	100	-			
Auto, Default and User Defined Bins:						
bin <auto[1],auto[1],auto[1]>	39	1	-	Covered		
bin <auto[1],auto[1],auto[0]>	1972	1	-	Covered		
bin <auto[0],auto[1],auto[1]>	141	1	-	Covered		
bin <auto[0],auto[1],auto[0]>	798	1	-	Covered		
bin <auto[1],auto[0],auto[0]>	4797	1	-	Covered		
bin <auto[0],auto[0],auto[0]>	2033	1	-	Covered		
Illegal and Ignore Bins:						
ignore_bin read_active_with_empty	222	-	Occurred			
Cross wr_rd_overflow_cross	100.00%	100	-	Covered		
covered/total bins:	6	6	-			
missing/total bins:	0	6	-			
% Hit:	100.00%	100	-			
Auto, Default and User Defined Bins:						
bin <auto[1],auto[1],auto[1]>	1027	1	-	Covered		
bin <auto[1],auto[0],auto[1]>	2487	1	-	Covered		
bin <auto[1],auto[1],auto[0]>	984	1	-	Covered		
bin <auto[0],auto[1],auto[0]>	939	1	-	Covered		
bin <auto[1],auto[0],auto[0]>	2415	1	-	Covered		
bin <auto[0],auto[0],auto[0]>	2150	1	-	Covered		
Illegal and Ignore Bins:						
ignore_bin write_active_with_overflow	0	-	ZERO			
Cross wr_rd_underflow_cross	100.00%	100	-	Covered		
covered/total bins:	6	6	-			
missing/total bins:	0	6	-			
% Hit:	100.00%	100	-			
Auto, Default and User Defined Bins:						
bin <auto[1],auto[1],auto[1]>	97	1	-	Covered		
bin <auto[1],auto[1],auto[0]>	1914	1	-	Covered		
bin <auto[0],auto[1],auto[1]>	91	1	-	Covered		
bin <auto[0],auto[1],auto[0]>	848	1	-	Covered		
bin <auto[1],auto[0],auto[0]>	4902	1	-	Covered		
bin <auto[0],auto[0],auto[0]>	2150	1	-	Covered		
Illegal and Ignore Bins:						
ignore_bin read_active_with_underflow	0	-	ZERO			
Cross wr_rd_almostfull_cross	100.00%	100	-	Covered		
covered/total bins:	6	6	-			
missing/total bins:	0	6	-			
% Hit:	100.00%	100	-			
Auto, Default and User Defined Bins:						
bin <auto[1],auto[1],auto[1]>	1325	1	-	Covered		
bin <auto[1],auto[0],auto[1]>	368	1	-	Covered		
bin <auto[1],auto[1],auto[0]>	686	1	-	Covered		
bin <auto[1],auto[0],auto[0]>	4534	1	-	Covered		
bin <auto[0],auto[1],auto[0]>	582	1	-	Covered		
bin <auto[0],auto[0],auto[0]>	1635	1	-	Covered		
Illegal and Ignore Bins:						
ignore_bin read_write_active_with_almostfull	357	-	Occurred			
ignore_bin write_active_with_almostfull	872	-	Occurred			
Cross wr rd almostempty cross	100.00%	100	-	Covered		

covered/total bins:	5	5	-
missing/total bins:	0	5	-
% Hit:	100.00%	100	-
Auto, Default and User Defined Bins:			
bin <auto[1],auto[1],auto[1]>	168	1	- Covered
bin <auto[1],auto[1],auto[0]>	1843	1	- Covered
bin <auto[1],auto[0],auto[0]>	4747	1	- Covered
bin <auto[0],auto[1],auto[0]>	898	1	- Covered
bin <auto[0],auto[0],auto[0]>	2057	1	- Covered
Illegal and Ignore Bins:			
ignore_bin read_write_active_with_almostempty	41	-	Occurred
ignore_bin read_active_with_almostempty	248	-	Occurred

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/cg	100.00%	100	-	Covered
covered/total bins:	58	58	-	
missing/total bins:	0	58	-	
% Hit:	100.00%	100	-	
Coverpoint wr_en_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	3089	1	-	Covered
bin auto[1]	6913	1	-	Covered
Coverpoint rd_en_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	7052	1	-	Covered
bin auto[1]	2950	1	-	Covered
Coverpoint wr_ack_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	6041	1	-	Covered
bin auto[1]	3961	1	-	Covered
Coverpoint full_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	5879	1	-	Covered
bin auto[1]	4123	1	-	Covered
Coverpoint empty_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	9600	1	-	Covered
bin auto[1]	402	1	-	Covered
Coverpoint almostfull_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	7437	1	-	Covered
bin auto[1]	2565	1	-	Covered
Coverpoint almostempty_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	9545	1	-	Covered
bin auto[1]	457	1	-	Covered
Coverpoint overflow_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	6488	1	-	Covered
bin auto[1]	3514	1	-	Covered
Coverpoint underflow_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	9814	1	-	Covered
bin auto[1]	188	1	-	Covered
Cross wr_rd_wr_ack_cross	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	1161	1	-	Covered
bin <auto[1],auto[0],auto[1]>	2800	1	-	Covered
bin <auto[1],auto[1],auto[0]>	850	1	-	Covered
bin <auto[1],auto[0],auto[0]>	2102	1	-	Covered
bin <auto[0],auto[1],auto[0]>	939	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2150	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin read_write_active_with_wr_ack	0	-	ZERO	
ignore_bin write_active_with_wr_ack	0	-	ZERO	
Cross wr_rd_full_cross	100.00%	100	-	Covered
covered/total bins:	5	5	-	
missing/total bins:	0	5	-	

bin <auto[1],auto[1],auto[0]>	1972	1	-	Covered
bin <auto[0],auto[1],auto[1]>	141	1	-	Covered
bin <auto[0],auto[1],auto[0]>	798	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4797	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2033	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin read_active_with_empty	222		-	Occurred
Cross wr_rd_overflow_cross	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	1027	1	-	Covered
bin <auto[1],auto[0],auto[1]>	2487	1	-	Covered
bin <auto[1],auto[1],auto[0]>	984	1	-	Covered
bin <auto[0],auto[1],auto[0]>	939	1	-	Covered
bin <auto[1],auto[0],auto[0]>	2415	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2150	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin write_active_with_overflow	0		-	ZERO
Cross wr_rd_underflow_cross	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	97	1	-	Covered
bin <auto[1],auto[1],auto[0]>	1914	1	-	Covered
bin <auto[0],auto[1],auto[1]>	91	1	-	Covered
bin <auto[0],auto[1],auto[0]>	848	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4982	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2150	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin read_active_with_underflow	0		-	ZERO
Cross wr_rd_almostfull_cross	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	1325	1	-	Covered
bin <auto[1],auto[0],auto[1]>	368	1	-	Covered
bin <auto[1],auto[1],auto[0]>	686	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4534	1	-	Covered
bin <auto[0],auto[1],auto[0]>	582	1	-	Covered
bin <auto[0],auto[0],auto[0]>	1635	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin read_write_active_with_almostfull	357		-	Occurred
ignore_bin write_active_with_almostfull	872		-	Occurred
Cross wr_rd_almostempty_cross	100.00%	100	-	Covered
covered/total bins:	5	5	-	
missing/total bins:	0	5	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	168	1	-	Covered
bin <auto[1],auto[1],auto[0]>	1843	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4747	1	-	Covered
bin <auto[0],auto[1],auto[0]>	898	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2057	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin read_write_active_with_almostempty	41		-	Occurred
ignore_bin read_active_with_almostempty	248		-	Occurred

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 1

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
<hr/>						
/TOP/DUT/write_acknowledge_cover	FIPO	Verilog	SVA	D:/Verification course/PROJECT1/FIFO.sv(84)	3886	Covered
/TOP/DUT/underflow_cover	FIPO	Verilog	SVA	D:/Verification course/PROJECT1/FIFO.sv(90)	154	Covered
/TOP/DUT/overflow_cover	FIPO	Verilog	SVA	D:/Verification course/PROJECT1/FIFO.sv(96)	2753	Covered
/TOP/DUT/increment_cover	FIPO	Verilog	SVA	D:/Verification course/PROJECT1/FIFO.sv(102)	2743	Covered
/TOP/DUT/decrement_cover	FIPO	Verilog	SVA	D:/Verification course/PROJECT1/FIFO.sv(108)	831	Covered
/TOP/DUT/full_cover	FIPO	Verilog	SVA	D:/Verification course/PROJECT1/FIFO.sv(114)	4042	Covered
/TOP/DUT/empty_cover	FIPO	Verilog	SVA	D:/Verification course/PROJECT1/FIFO.sv(120)	394	Covered
/TOP/DUT/almostfull_cover	FIPO	Verilog	SVA	D:/Verification course/PROJECT1/FIFO.sv(126)	2512	Covered
/TOP/DUT/almostempty_cover	FIPO	Verilog	SVA	D:/Verification course/PROJECT1/FIFO.sv(132)	451	Covered

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 9

Total Coverage By Instance (filtered view): 100.00%

XV. Coverage report

```
Coverage Report by instance with details
=====
== Instance: /TOP/if_obj
== Design Unit: work.FIFO_if
=====
Toggle Coverage:
  Enabled Coverage      Bins    Hits    Misses   Coverage
  -----      -----
  Toggles          86      86        0   100.00%
=====
=====Toggle Details=====
Toggle Coverage for instance /TOP/if_obj --
      Node      1H->0L      0L->1H  "Coverage"
  -----
  almostempty      1          1   100.00
  almostfull      1          1   100.00
  clk              1          1   100.00
  data_in[15:0]    1          1   100.00
  data_out[15:0]   1          1   100.00
  empty            1          1   100.00
  full             1          1   100.00
  overflow         1          1   100.00
  rd_en            1          1   100.00
  rst_n            1          1   100.00
  underflow        1          1   100.00
  wr_ack           1          1   100.00
  wr_en            1          1   100.00
Total Node Count = 43
Toggled Node Count = 43
Untoggled Node Count = 0
Toggle Coverage = 100.00% (86 of 86 bins)
=====
== Instance: /TOP/DUT
== Design Unit: work.FIFO
=====
Assertion Coverage:
  Assertions      9      9        0   100.00%
  -----
  Name      File(Line)      Failure      Pass
  Count      Count
  -----
  /TOP/DUT/write_acknowledge      FIFO.sv(83)      0          1
  /TOP/DUT/underflow_assertion   FIFO.sv(89)      0          1
  /TOP/DUT/overflow_assertion   FIFO.sv(95)      0          1
  /TOP/DUT/increment_assertion  FIFO.sv(101)     0          1
  /TOP/DUT/decrement_assertion FIFO.sv(107)     0          1
  /TOP/DUT/full_assertion       FIFO.sv(113)     0          1
  /TOP/DUT/empty_assertion      FIFO.sv(119)     0          1
  /TOP/DUT/almostfull_assertion FIFO.sv(125)     0          1
  /TOP/DUT/almostempty_assertion FIFO.sv(131)     0          1
Branch Coverage:
  Enabled Coverage      Bins    Hits    Misses   Coverage
  -----      -----
  Branches          25      25        0   100.00%
=====
=====Branch Details=====
Branch Coverage for instance /TOP/DUT
      Line      Item      Count      Source
  -----
  File FIFO.sv
      -----IF Branch-----
  15                      10192  Count coming in to IF
  15          1            383
  20          1            3962
  25          1            5847
Branch totals: 3 hits of 3 branches = 100.00%
      -----IF Branch-----
  27                      5847  Count coming in to IF
  27          1            2888
  29          1            3039
Branch totals: 2 hits of 2 branches = 100.00%
      -----IF Branch-----
  36                      10192  Count coming in to IF
  36          1            383
```

```

36      1      383 |
41      1      2739
45      1      7070
Branch totals: 3 hits of 3 branches = 100.00%
-----IF Branch-----
47          7070  Count coming in to IF
47      1      159
49      1      6911
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch-----
56          8479  Count coming in to IF
56      1      380
59      1      8099
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch-----
60          8099  Count coming in to IF
60      1      2801
62      1      847
64      1      811
66      1      80
3560  All False Count
Branch totals: 5 hits of 5 branches = 100.00%
-----IF Branch-----
72          4725  Count coming in to IF
72      1      1249
72      2      3476
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch-----
73          4725  Count coming in to IF
73      1      235
73      2      4490
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch-----
74          4725  Count coming in to IF
74      1      1536
74      2      3189
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch-----
75          4725  Count coming in to IF
75      1      276
75      2      4449
Branch totals: 2 hits of 2 branches = 100.00%
Condition Coverage:
  Enabled Coverage      Bins  Covered    Misses  Coverage
  -----  -----  -----  -----
  Conditions           24      24       0   100.00%
=====
=====Condition Details=====
Condition Coverage for instance /TOP/DUT --
File FIFO.sv
-----Focused Condition View-----
Line  20 Item  1 (if_obj.wr_en && (count < if_obj.FIFO_DEPTH))
Condition totals: 2 of 2 input terms covered = 100.00%
  Input Term  Covered  Reason for no coverage  Hint
  -----  -----
  if_obj.wr_en      Y
  (count < if_obj.FIFO_DEPTH)      Y
  Rows:  Hits  FEC Target            Non-masking condition(s)
  -----  -----
  Row  1:  1  if_obj.wr_en_0        -
  Row  2:  1  if_obj.wr_en_1        (count < if_obj.FIFO_DEPTH)
  Row  3:  1  (count < if_obj.FIFO_DEPTH)_0  if_obj.wr_en
  Row  4:  1  (count < if_obj.FIFO_DEPTH)_1  if_obj.wr_en
-----Focused Condition View-----
Line  27 Item  1 (if_obj.full && if_obj.wr_en)
Condition totals: 2 of 2 input terms covered = 100.00%
  Input Term  Covered  Reason for no coverage  Hint
  -----  -----
  if_obj.full      Y
  if_obj.wr_en      Y
  Rows:  Hits  FEC Target            Non-masking condition(s)
  -----  -----
  Row  1:  1  if_obj.full_0        -
  Row  2:  1  if_obj.full_1        if_obj.wr_en
  Row  3:  1  if_obj.wr_en_0        if_obj.full
  Row  4:  1  if_obj.wr_en_1        if_obj.full
-----Focused Condition View-----
Line  41 Item  1 (if_obj.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

```

```

-----  

if_obj.rd_en      Y  

(count != 0)      Y  

-----  

  Rows:    Hits  FEC Target      Non-masking condition(s)  

-----  

Row 1:          1 if_obj.rd_en_0      -  

Row 2:          1 if_obj.rd_en_1      (count != 0)  

Row 3:          1 (count != 0)_0      if_obj.rd_en  

Row 4:          1 (count != 0)_1      if_obj.rd_en  

-----  

-----Focused Condition View-----  

Line     47 Item   1 (if_obj.empty && if_obj.rd_en)  

Condition totals: 2 of 2 input terms covered = 100.00%  

-----  

  Input Term  Covered  Reason for no coverage  Hint  

-----  

if_obj.empty      Y  

if_obj.rd_en      Y  

-----  

  Rows:    Hits  FEC Target      Non-masking condition(s)  

-----  

Row 1:          1 if_obj.empty_0      -  

Row 2:          1 if_obj.empty_1      if_obj.rd_en  

Row 3:          1 if_obj.rd_en_0      if_obj.empty  

Row 4:          1 if_obj.rd_en_1      if_obj.empty  

-----  

-----Focused Condition View-----  

Line     60 Item   1 ((~if_obj.rd_en && if_obj.wr_en) && ~if_obj.full)  

Condition totals: 3 of 3 input terms covered = 100.00%  

-----  

  Input Term  Covered  Reason for no coverage  Hint  

-----  

if_obj.rd_en      Y  

if_obj.wr_en      Y  

if_obj.full      Y  

-----  

  Rows:    Hits  FEC Target      Non-masking condition(s)  

-----  

Row 1:          1 if_obj.rd_en_0      (~if_obj.full && if_obj.wr_en)  

Row 2:          1 if_obj.rd_en_1      -  

Row 3:          1 if_obj.wr_en_0      (~if_obj.rd_en  

Row 4:          1 if_obj.wr_en_1      (~if_obj.full && ~if_obj.rd_en)  

Row 5:          1 if_obj.full_0      (~if_obj.rd_en && if_obj.wr_en)  

Row 6:          1 if_obj.full_1      (~if_obj.rd_en && if_obj.wr_en)  

-----  

-----Focused Condition View-----  

Line     62 Item   1 ((if_obj.rd_en && ~if_obj.wr_en) && ~if_obj.empty)  

Condition totals: 3 of 3 input terms covered = 100.00%  

-----  

  Input Term  Covered  Reason for no coverage  Hint  

-----  

if_obj.rd_en      Y  

if_obj.wr_en      Y  

if_obj.empty      Y  

-----  

  Rows:    Hits  FEC Target      Non-masking condition(s)  

-----  

Row 1:          1 if_obj.rd_en_0      -  

Row 2:          1 if_obj.rd_en_1      (~if_obj.empty && ~if_obj.wr_en)  

Row 3:          1 if_obj.wr_en_0      (~if_obj.empty && if_obj.rd_en)  

Row 4:          1 if_obj.wr_en_1      if_obj.rd_en  

Row 5:          1 if_obj.empty_0      (if_obj.rd_en && ~if_obj.wr_en)  

Row 6:          1 if_obj.empty_1      (if_obj.rd_en && ~if_obj.wr_en)  

-----  

-----Focused Condition View-----  

Line     64 Item   1 ((if_obj.rd_en && if_obj.wr_en) && if_obj.full)  

Condition totals: 3 of 3 input terms covered = 100.00%  

-----  

  Input Term  Covered  Reason for no coverage  Hint  

-----  

if_obj.rd_en      Y  

if_obj.wr_en      Y  

if_obj.full      Y  

-----  

  Rows:    Hits  FEC Target      Non-masking condition(s)  

-----  

Row 1:          1 if_obj.rd_en_0      -  

Row 2:          1 if_obj.rd_en_1      (if_obj.full && if_obj.wr_en)  

Row 3:          1 if_obj.wr_en_0      if_obj.rd_en  

Row 4:          1 if_obj.wr_en_1      (if_obj.full && if_obj.rd_en)  

Row 5:          1 if_obj.full_0      (if_obj.rd_en && if_obj.wr_en)  

Row 6:          1 if_obj.full_1      (if_obj.rd_en && if_obj.wr_en)  

-----  

-----Focused Condition View-----  

Line     66 Item   1 ((if_obj.rd_en && if_obj.wr_en) && if_obj.empty)  

Condition totals: 3 of 3 input terms covered = 100.00%  

-----  

  Input Term  Covered  Reason for no coverage  Hint  

-----  

if_obj.rd_en      Y  

if_obj.wr_en      Y  

if_obj.empty      Y  

-----  

  Rows:    Hits  FEC Target      Non-masking condition(s)

```

```

Row  3:      1 if_obj.wr_en_0      if_obj.rd_en
Row  4:      1 if_obj.wr_en_1      (if_obj.empty & if_obj.rd_en)
Row  5:      1 if_obj.empty_0      (if_obj.rd_en & if_obj.wr_en)
Row  6:      1 if_obj.empty_1      (if_obj.rd_en & if_obj.wr_en)

```

-----Focused Condition View-----

```

Line    72 Item  1 (count == if_obj.FIFO_DEPTH)
Condition totals: 1 of 1 input term covered = 100.00%

```

Input Term	Covered	Reason for no coverage	Hint
(count == if_obj.FIFO_DEPTH)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == if_obj.FIFO_DEPTH)_0	-
Row 2:	1	(count == if_obj.FIFO_DEPTH)_1	-

-----Focused Condition View-----

```

Line    73 Item  1 (count == 0)
Condition totals: 1 of 1 input term covered = 100.00%

```

Input Term	Covered	Reason for no coverage	Hint
(count == 0)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == 0)_0	-
Row 2:	1	(count == 0)_1	-

-----Focused Condition View-----

```

Line    74 Item  1 (count == (if_obj.FIFO_DEPTH - 1))
Condition totals: 1 of 1 input term covered = 100.00%

```

Input Term	Covered	Reason for no coverage	Hint
(count == (if_obj.FIFO_DEPTH - 1))	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == (if_obj.FIFO_DEPTH - 1))_0	-
Row 2:	1	(count == (if_obj.FIFO_DEPTH - 1))_1	-

-----Focused Condition View-----

```

Line    75 Item  1 (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

```

Input Term	Covered	Reason for no coverage	Hint
(count == 1)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == 1)_0	-
Row 2:	1	(count == 1)_1	-

Directive Coverage:

Directives	9	9	0	100.00%
------------	---	---	---	---------

DIRECTIVE COVERAGE:

Name	Design Unit	Design Unit	Lang	File(Line)	Hits	Status
/TOP/DUT/write_acknowledge_cover	FIFO	Verilog	SVA	FIFO.sv(84)	3886	Covered
/TOP/DUT/underflow_cover	FIFO	Verilog	SVA	FIFO.sv(98)	154	Covered
/TOP/DUT/overflow_cover	FIFO	Verilog	SVA	FIFO.sv(96)	2753	Covered
/TOP/DUT/increment_cover	FIFO	Verilog	SVA	FIFO.sv(102)	2743	Covered
/TOP/DUT/decrement_cover	FIFO	Verilog	SVA	FIFO.sv(188)	831	Covered
/TOP/DUT/full_cover	FIFO	Verilog	SVA	FIFO.sv(114)	4042	Covered
/TOP/DUT/empty_cover	FIFO	Verilog	SVA	FIFO.sv(120)	394	Covered
/TOP/DUT/almostfull_cover	FIFO	Verilog	SVA	FIFO.sv(126)	2512	Covered
/TOP/DUT/almostempty_cover	FIFO	Verilog	SVA	FIFO.sv(132)	451	Covered

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

=====Statement Details=====

Statement Coverage for instance /TOP/DUT --

Line	Item	Count	Source
14	1	10192	
16	1	383	
17	1	383	
18	1	383	
21	1	3962	
22	1	3962	
23	1	3962	
26	1	5847	

```

35      1          10192
37      1          383
38      1          383
39      1          383
42      1          2739
43      1          2739
48      1          159
50      1          6911
55      1          8479
57      1          388
61      1          2881
63      1          847
65      1          811
67      1          88
72      1          4726
73      1          4726
74      1          4726
75      1          4726
Toggle Coverage:
  Enabled Coverage      Bins    Hits    Misses   Coverage
  -----  -----
  Toggles           20      20       0   100.00%
=====
=====Toggle Details=====
Toggle Coverage for instance /TOP/DUT --
          Node     1H->0L     0L->1H "Coverage"
  -----
  count[3-0]           1       1   100.00
  rd_ptr[2-0]          1       1   100.00
  wr_ptr[2-0]          1       1   100.00

Total Node Count      =      10
Toggled Node Count   =      10
Untoggled Node Count =       0

Toggle Coverage      =      100.00% (20 of 20 bins)
=====
== Instance: /TOP/TEST
== Design Unit: work.FIFO_tb
=====

Assertion Coverage:
  Assertions      3      3       0   100.00%
  -----
  Name      File(line)      Failure      Pass
           Count        Count
  -----
  /TOP/TEST/#ublk#182146786#17/immed_18
           testbench.sv(18)      0       1
  /TOP/TEST/#ublk#182146786#28/immed_29
           testbench.sv(29)      0       1
  /TOP/TEST/#ublk#182146786#41/immed_42
           testbench.sv(42)      0       1

Statement Coverage:
  Enabled Coverage      Bins    Hits    Misses   Coverage
  -----  -----
  Statements           33      33       0   100.00%
=====
=====Statement Details=====
Statement Coverage for instance /TOP/TEST --
  Line      Item      Count      Source
  ----  -----
  File testbench.sv
  11      1          1
  12      1          1
  13      1          2
  13      2          2
  14      1          1
  15      1          1
  16      1          1
  17      1          50
  19      1          50
  20      1          50
  21      1          50
  22      1          50
  23      1          50
  25      1          1
  26      1          1
  27      1          1
  28      1          50
  30      1          50
  31      1          50
  32      1          50
  33      1          50
  34      1          50
  37      1          1
  38      1          1
  39      1          1
  40      1          1
  41      1          9900
  43      1          9900

```

```

43      1      9900
44      1      9900
45      1      9900
46      1      9900
47      1      9900
50      1      1

=====
== Instance: /TOP/MONITOR
== Design Unit: work.FIFO_monitor
=====

Branch Coverage:
  Enabled Coverage      Bins      Hits      Misses   Coverage
  -----      -----      -----      -----      -----
  Branches          2        2        0    100.00%
=====

Branch Details:
Branch Coverage for instance /TOP/MONITOR

  Line      Item      Count      Source
  ----      ----      -----      -----
  File MONITOR.sv
  -----      IF Branch-----
  56      10002      Count coming in to IF
  56      1          1
  56      10001      All False Count
Branch totals: 2 hits of 2 branches = 100.00%

Statement Coverage:
  Enabled Coverage      Bins      Hits      Misses   Coverage
  -----      -----      -----      -----      -----
  Statements         24        24        0    100.00%
=====

Statement Details:
Statement Coverage for instance /TOP/MONITOR --

  Line      Item      Count      Source
  ----      ----      -----      -----
  File MONITOR.sv
  18      1          1
  19      1          1
  20      1          1
  22      1          1
  24      10002
  27      10002
  28      10002
  29      10002
  30      10002
  33      10002
  34      10002
  35      10002
  36      10002
  37      10002
  38      10002
  39      10002
  40      10002
  45      10002
  49      10002
  50      10002
  51      10002
  57      1          1
  58      1          1
  59      1          1

=====
== Instance: /TOP
== Design Unit: work.TOP
=====

Statement Coverage:
  Enabled Coverage      Bins      Hits      Misses   Coverage
  -----      -----      -----      -----      -----
  Statements         4        4        0    100.00%
=====

Statement Details:
Statement Coverage for instance /TOP --

  Line      Item      Count      Source
  ----      ----      -----      -----
  File TOP.sv
  5      1          1
  6      1          1
  7      1      20006
  8      1      20005

Toggle Coverage:
  Enabled Coverage      Bins      Hits      Misses   Coverage
  -----      -----      -----      -----      -----
  Toggles          2        2        0    100.00%
=====

Toggle Details:
Toggle Coverage for instance /TOP --

```

	clk	1	1	100.00
Total Node Count	=	1		
Toggled Node Count	=	1		
Untoggled Node Count	=	0		
Toggle Coverage	=	100.00% (2 of 2 bins)		
=====				
== Instance: /FIFO_scoreboard_pkg				
== Design Unit: work.FIFO_scoreboard_pkg				
=====				
Branch Coverage:				
Enabled Coverage	Bins	Hits	Misses	Coverage
-----	---	---	---	-----
Branches	25	25	0	100.00%
=====Branch Details=====				
Branch Coverage for instance /FIFO_scoreboard_pkg				
Line	Item	Count	Source	
---	---	---	---	
File package3.sv				
-----IF Branch-----				
21		10002	Count coming in to IF	
21	1	4123		
21	2	5879		
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
22		10002	Count coming in to IF	
22	1	402		
22	2	9600		
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
23		10002	Count coming in to IF	
23	1	2565		
23	2	7437		
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
24		10002	Count coming in to IF	
24	1	457		
24	2	9545		
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
37		10002	Count coming in to IF	
37	1	10002		
Branch totals: 1 hit of 1 branch = 100.00%				
-----IF Branch-----				
53		10002	Count coming in to IF	
53	1	194		
61	1	3961		
65	1	5847		
Branch totals: 3 hits of 3 branches = 100.00%				
-----IF Branch-----				
67		5847	Count coming in to IF	
67	1	2088		
69	1	3039		
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
77		10002	Count coming in to IF	
77	1	194		
83	1	2739		
86	1	7069		
Branch totals: 3 hits of 3 branches = 100.00%				
-----IF Branch-----				
87		7069	Count coming in to IF	
87	1	159		
89	1	6910		
Branch totals: 2 hits of 2 branches = 100.00%				
-----IF Branch-----				
96		10002	Count coming in to IF	
96	1	194		
99	1	2880		
101	1	847		
103	1	811		
105	1	88		
		5270	All False Count	
Branch totals: 6 hits of 6 branches = 100.00%				
Condition Coverage:				
Enabled Coverage	Bins	Covered	Misses	Coverage
-----	---	---	---	-----
Conditions	24	24	0	100.00%
=====Condition Details=====				

```

File package3.sv
-----Focused Condition View-----
Line    21 Item   1 (this.counter == 8)
Condition totals: 1 of 1 input term covered = 100.00%
      Input Term  Covered  Reason for no coverage  Hint
      -----  -----
      (this.counter == 8)      Y

      Rows:     Hits  FEC Target          Non-masking condition(s)
      -----  -----
      Row  1:      1  (this.counter == 8)_0  -
      Row  2:      1  (this.counter == 8)_1  -

-----Focused Condition View-----
Line    22 Item   1 (this.counter == 0)
Condition totals: 1 of 1 input term covered = 100.00%
      Input Term  Covered  Reason for no coverage  Hint
      -----  -----
      (this.counter == 0)      Y

      Rows:     Hits  FEC Target          Non-masking condition(s)
      -----  -----
      Row  1:      1  (this.counter == 0)_0  -
      Row  2:      1  (this.counter == 0)_1  -

-----Focused Condition View-----
Line    23 Item   1 (this.counter == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%
      Input Term  Covered  Reason for no coverage  Hint
      -----  -----
      (this.counter == (8 - 1))      Y

      Rows:     Hits  FEC Target          Non-masking condition(s)
      -----  -----
      Row  1:      1  (this.counter == (8 - 1))_0  -
      Row  2:      1  (this.counter == (8 - 1))_1  -

-----Focused Condition View-----
Line    24 Item   1 (this.counter == 1)
Condition totals: 1 of 1 input term covered = 100.00%
      Input Term  Covered  Reason for no coverage  Hint
      -----  -----
      (this.counter == 1)      Y

      Rows:     Hits  FEC Target          Non-masking condition(s)
      -----  -----
      Row  1:      1  (this.counter == 1)_0  -
      Row  2:      1  (this.counter == 1)_1  -

-----Focused Condition View-----
Line    61 Item   1 (obj_gold.wr_en && (this.counter < 8))
Condition totals: 2 of 2 input terms covered = 100.00%
      Input Term  Covered  Reason for no coverage  Hint
      -----  -----
      obj_gold.wr_en      Y
      (this.counter < 8)      Y

      Rows:     Hits  FEC Target          Non-masking condition(s)
      -----  -----
      Row  1:      1  obj_gold.wr_en_0  -
      Row  2:      1  obj_gold.wr_en_1  (this.counter < 8)
      Row  3:      1  (this.counter < 8)_0  obj_gold.wr_en
      Row  4:      1  (this.counter < 8)_1  obj_gold.wr_en

-----Focused Condition View-----
Line    67 Item   1 (this.full_ref && obj_gold.wr_en)
Condition totals: 2 of 2 input terms covered = 100.00%
      Input Term  Covered  Reason for no coverage  Hint
      -----  -----
      this.full_ref      Y
      obj_gold.wr_en      Y

      Rows:     Hits  FEC Target          Non-masking condition(s)
      -----  -----
      Row  1:      1  this.full_ref_0  -
      Row  2:      1  this.full_ref_1  obj_gold.wr_en
      Row  3:      1  obj_gold.wr_en_0  this.full_ref
      Row  4:      1  obj_gold.wr_en_1  this.full_ref

-----Focused Condition View-----
Line    83 Item   1 (obj_gold.rd_en && (this.counter != 0))
Condition totals: 2 of 2 input terms covered = 100.00%
      Input Term  Covered  Reason for no coverage  Hint
      -----  -----
      obj_gold.rd_en      Y
      (this.counter != 0)      Y

      Rows:     Hits  FEC Target          Non-masking condition(s)

```

```

Rows:     Hits FEC Target      Non-masking condition(s)
----- -----
Row 1:     1 obj_gold.rd_en_0   -
Row 2:     1 obj_gold.rd_en_1   (this.counter != 0)
Row 3:     1 (this.counter != 0)_0 obj_gold.rd_en
Row 4:     1 (this.counter != 0)_1 obj_gold.rd_en

-----Focused Condition View-----
Line    87 Item  1 (this.empty_ref && obj_gold.rd_en)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term  Covered  Reason for no coverage  Hint
----- -----
this.empty_ref  Y
obj_gold.rd_en  Y

Rows:     Hits FEC Target      Non-masking condition(s)
----- -----
Row 1:     1 this.empty_ref_0   -
Row 2:     1 this.empty_ref_1   obj_gold.rd_en
Row 3:     1 obj_gold.rd_en_0   this.empty_ref
Row 4:     1 obj_gold.rd_en_1   this.empty_ref

-----Focused Condition View-----
Line    99 Item  1 (~obj_gold.rd_en && obj_gold.wr_en && ~this.full_ref)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term  Covered  Reason for no coverage  Hint
----- -----
obj_gold.rd_en  Y
obj_gold.wr_en  Y
this.full_ref   Y

Rows:     Hits FEC Target      Non-masking condition(s)
----- -----
Row 1:     1 obj_gold.rd_en_0   (obj_gold.wr_en && ~this.full_ref)
Row 2:     1 obj_gold.rd_en_1   -
Row 3:     1 obj_gold.wr_en_0   ~obj_gold.rd_en
Row 4:     1 obj_gold.wr_en_1   (~obj_gold.rd_en && ~this.full_ref)
Row 5:     1 this.full_ref_0   (~obj_gold.rd_en && obj_gold.wr_en)
Row 6:     1 this.full_ref_1   (~obj_gold.rd_en && obj_gold.wr_en)

-----Focused Condition View-----
Line    101 Item  1 (obj_gold.rd_en && ~obj_gold.wr_en && ~this.empty_ref)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term  Covered  Reason for no coverage  Hint
----- -----
obj_gold.rd_en  Y
obj_gold.wr_en  Y
this.empty_ref  Y

Rows:     Hits FEC Target      Non-masking condition(s)
----- -----
Row 1:     1 obj_gold.rd_en_0   -
Row 2:     1 obj_gold.rd_en_1   (~obj_gold.wr_en && ~this.empty_ref)
Row 3:     1 obj_gold.wr_en_0   (obj_gold.rd_en && ~this.empty_ref)
Row 4:     1 obj_gold.wr_en_1   obj_gold.rd_en
Row 5:     1 this.empty_ref_0   (obj_gold.rd_en && ~obj_gold.wr_en)
Row 6:     1 this.empty_ref_1   (obj_gold.rd_en && ~obj_gold.wr_en)

-----Focused Condition View-----
Line    103 Item  1 (obj_gold.rd_en && obj_gold.wr_en && this.full_ref)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term  Covered  Reason for no coverage  Hint
----- -----
obj_gold.rd_en  Y
obj_gold.wr_en  Y
this.full_ref   Y

Rows:     Hits FEC Target      Non-masking condition(s)
----- -----
Row 1:     1 obj_gold.rd_en_0   -
Row 2:     1 obj_gold.rd_en_1   (obj_gold.wr_en && this.full_ref)
Row 3:     1 obj_gold.wr_en_0   obj_gold.rd_en
Row 4:     1 obj_gold.wr_en_1   (obj_gold.rd_en && this.full_ref)
Row 5:     1 this.full_ref_0   (obj_gold.rd_en && obj_gold.wr_en)
Row 6:     1 this.full_ref_1   (obj_gold.rd_en && obj_gold.wr_en)

-----Focused Condition View-----
Line    105 Item  1 (obj_gold.rd_en && obj_gold.wr_en && this.empty_ref)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term  Covered  Reason for no coverage  Hint
----- -----
obj_gold.rd_en  Y
obj_gold.wr_en  Y
this.empty_ref  Y

Rows:     Hits FEC Target      Non-masking condition(s)
----- -----
Row 1:     1 obj_gold.rd_en_0   -
Row 2:     1 obj_gold.rd_en_1   (obj_gold.wr_en && this.empty_ref)
Row 3:     1 obj_gold.wr_en_0   obj_gold.rd_en
Row 4:     1 obj_gold.wr_en_1   (obj_gold.rd_en && this.empty_ref)

```

```

Statement Coverage:
  Enabled Coverage      Bins    Hits    Misses  Coverage
  -----  -----  -----  -----
  Statements          33      33       0   100.00%
-----=Statement Details=-----
Statement Coverage for instance /FIFO_scoreboard_pkg --
Line     Item      Count  Source
----  -----
File package3.sv
 21      1        10002
 22      1        10002
 23      1        10002
 24      1        10002
 31      1        10002
 33      1        10002
 35      1        10002
 38      1        10002
 39      1        10002
 54      1         194
 55      1         194
 56      1         194
 57      1         194
 58      1         194
 59      1         194
 62      1        3961
 63      1        3961
 66      1        5847
 68      1        2808
 70      1        3039
 78      1         194
 79      1         194
 80      1         194
 81      1         194
 84      1        2739
 88      1         159
 90      1        6910
 97      1         194
100      1        2800
102      1         847
104      1         811
106      1          88
107      1        10002
-----=-----
== Instance: /FIFO_coverage_pkg
== Design Unit: work.FIFO_coverage_pkg
=====

Covergroup Coverage:
  Covergroups      1      na      na  100.00%
  Coverpoints/Crosses  16      na      na      na
  Covergroup Bins    58      58       0  100.00%
-----=-----
Covergroup
  Metric      Goal      Bins  Status
-----=-----
TYPE /FIFO_coverage_pkg/FIFO_coverage/cg      100.00%      100      -  Covered
  covered/total bins:                      58      58      -
  missing/total bins:                      0      58      -
  % Hit:                                100.00%      100      -
Coverpoint wr_en_cp      100.00%      100      -  Covered
  covered/total bins:                      2      2      -
  missing/total bins:                      0      2      -
  % Hit:                                100.00%      100      -
    bin auto[0]                         3089      1      -  Covered
    bin auto[1]                         6913      1      -  Covered
Coverpoint rd_en_cp      100.00%      100      -  Covered
  covered/total bins:                      2      2      -
  missing/total bins:                      0      2      -
  % Hit:                                100.00%      100      -
    bin auto[0]                         7052      1      -  Covered
    bin auto[1]                         2958      1      -  Covered
Coverpoint wr_ack_cp      100.00%      100      -  Covered
  covered/total bins:                      2      2      -
  missing/total bins:                      0      2      -
  % Hit:                                100.00%      100      -
    bin auto[0]                         6641      1      -  Covered
    bin auto[1]                         3961      1      -  Covered
Coverpoint full_cp      100.00%      100      -  Covered
  covered/total bins:                      2      2      -
  missing/total bins:                      0      2      -
  % Hit:                                100.00%      100      -
    bin auto[0]                         5879      1      -  Covered
    bin auto[1]                         4123      1      -  Covered
Coverpoint empty_cp      100.00%      100      -  Covered
  covered/total bins:                      2      2      -
  missing/total bins:                      0      2      -
  % Hit:                                100.00%      100      -
    bin auto[0]                         9608      1      -  Covered
    bin auto[1]                         402      1      -  Covered
Coverpoint almostfull_cp 100.00%      100      -  Covered
  covered/total bins:                      2      2      -

```

bin auto[1]	2565	1	-	Covered
Coverpoint almostempty_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	9545	1	-	Covered
bin auto[1]	457	1	-	Covered
Coverpoint overflow_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	6488	1	-	Covered
bin auto[1]	3514	1	-	Covered
Coverpoint underflow_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	9814	1	-	Covered
bin auto[1]	188	1	-	Covered
Cross wr_rd_wr_ack_cross	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	1161	1	-	Covered
bin <auto[1],auto[0],auto[1]>	2800	1	-	Covered
bin <auto[1],auto[1],auto[0]>	850	1	-	Covered
bin <auto[1],auto[0],auto[0]>	2102	1	-	Covered
bin <auto[0],auto[1],auto[0]>	939	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2150	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin read_active_with_wr_ack	0	-	ZERO	
ignore_bin write_active_with_wr_ack	0	-	ZERO	
Cross wr_rd_full_cross	100.00%	100	-	Covered
covered/total bins:	5	5	-	
missing/total bins:	0	5	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[0],auto[1]>	3246	1	-	Covered
bin <auto[1],auto[1],auto[0]>	2011	1	-	Covered
bin <auto[0],auto[1],auto[0]>	939	1	-	Covered
bin <auto[1],auto[0],auto[0]>	1656	1	-	Covered
bin <auto[0],auto[0],auto[0]>	1273	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin read_active_with_full	0	-	ZERO	
ignore_bin write_active_with_full	877	-	Occurred	
Cross wr_rd_empty_cross	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	39	1	-	Covered
bin <auto[1],auto[1],auto[0]>	1972	1	-	Covered
bin <auto[0],auto[1],auto[1]>	141	1	-	Covered
bin <auto[0],auto[1],auto[0]>	798	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4797	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2833	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin read_active_with_empty	222	-	Occurred	
Cross wr_rd_overflow_cross	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	1027	1	-	Covered
bin <auto[1],auto[0],auto[1]>	2487	1	-	Covered
bin <auto[1],auto[1],auto[0]>	984	1	-	Covered
bin <auto[0],auto[1],auto[0]>	939	1	-	Covered
bin <auto[1],auto[0],auto[0]>	2415	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2150	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin write_active_with_overflow	0	-	ZERO	
Cross wr_rd_underflow_cross	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	97	1	-	Covered
bin <auto[1],auto[1],auto[0]>	1914	1	-	Covered
bin <auto[0],auto[1],auto[1]>	91	1	-	Covered
bin <auto[0],auto[1],auto[0]>	848	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4982	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2150	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin read_active_with_underflow	0	-	ZERO	
Cross wr_rd_almostfull_cross	100.00%	100	-	Covered
covered/total bins:	6	6	-	
missing/total bins:	0	6	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	1325	1	-	Covered
bin <auto[1],auto[0],auto[1]>	368	1	-	Covered
bin <auto[1],auto[1],auto[0]>	686	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4534	1	-	Covered
bin <auto[0],auto[1],auto[0]>	582	1	-	Covered

	357		-	Occurred
ignore_bin write_active_with_almostfull				
	872		-	Occurred
Cross wr_rd_almostempty_cross	100.00%	100	-	Covered
covered/total bins:	5	5	-	Covered
missing/total bins:	0	5	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	168	1	-	Covered
bin <auto[1],auto[1],auto[0]>	1843	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4747	1	-	Covered
bin <auto[0],auto[1],auto[0]>	898	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2057	1	-	Covered
Illegal and Ignore Bins:				
ignore_bin read_write_active_with_almostempty	41		-	Occurred
ignore_bin read_active_with_almostempty	248		-	Occurred
Statement Coverage:				
Enabled Coverage	Bins	Hits	Misses	Coverage
-----	---	---	---	-----
Statements	4	4	0	100.00%

=====Statement Details=====

Statement Coverage for instance /FIFO_coverage_pkg --

Line	Item	Count	Source
---	---	---	---
File package2.sv			
11	1	10002	
13	1	10002	
73	1	1	
74	1	1	

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/cg	100.00%	100	-	Covered
covered/total bins:	58	58	-	
missing/total bins:	0	58	-	
% Hit:	100.00%	100	-	
Coverpoint wr_en_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	3889	1	-	Covered
bin auto[1]	6913	1	-	Covered
Coverpoint rd_en_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	7052	1	-	Covered
bin auto[1]	2958	1	-	Covered
Coverpoint wr_ack_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	6841	1	-	Covered
bin auto[1]	3961	1	-	Covered
Coverpoint full_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	5879	1	-	Covered
bin auto[1]	4123	1	-	Covered
Coverpoint empty_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	9600	1	-	Covered
bin auto[1]	492	1	-	Covered
Coverpoint almostfull_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	7437	1	-	Covered
bin auto[1]	2565	1	-	Covered
Coverpoint almostempty_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	9545	1	-	Covered
bin auto[1]	457	1	-	Covered
Coverpoint overflow_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin auto[0]	6488	1	-	Covered
bin auto[1]	3514	1	-	Covered
Coverpoint underflow_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	

```

ignore_bin read_write_active_with_almostempty      41      - Occurred
ignore_bin read_active_with_almostempty           248      - Occurred

```

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 1

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
/TOP/DUT/write_acknowledge_cover	FIFO	Verilog	SVA	FIFO.sv(84)	3886	Covered
/TOP/DUT/underflow_cover	FIFO	Verilog	SVA	FIFO.sv(98)	154	Covered
/TOP/DUT/overflow_cover	FIFO	Verilog	SVA	FIFO.sv(96)	2753	Covered
/TOP/DUT/increment_cover	FIFO	Verilog	SVA	FIFO.sv(102)	2743	Covered
/TOP/DUT/decrement_cover	FIFO	Verilog	SVA	FIFO.sv(108)	831	Covered
/TOP/DUT/full_cover	FIFO	Verilog	SVA	FIFO.sv(114)	4842	Covered
/TOP/DUT/empty_cover	FIFO	Verilog	SVA	FIFO.sv(128)	394	Covered
/TOP/DUT/almostfull_cover	FIFO	Verilog	SVA	FIFO.sv(126)	2512	Covered
/TOP/DUT/almostempty_cover	FIFO	Verilog	SVA	FIFO.sv(132)	451	Covered

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 9

ASSERTION RESULTS:

Name	File(Line)	Failure Count	Pass Count
/TOP/DUT/write_acknowledge	FIFO.sv(83)	0	1
/TOP/DUT/underflow_assertion	FIFO.sv(89)	0	1
/TOP/DUT/overflow_assertion	FIFO.sv(95)	0	1
/TOP/DUT/increment_assertion	FIFO.sv(101)	0	1
/TOP/DUT/decrement_assertion	FIFO.sv(107)	0	1
/TOP/DUT/full_assertion	FIFO.sv(113)	0	1
/TOP/DUT/empty_assertion	FIFO.sv(119)	0	1
/TOP/DUT/almostfull_assertion	FIFO.sv(125)	0	1
/TOP/DUT/almostempty_assertion	FIFO.sv(131)	0	1
/TOP/TEST#ublk#182146786#17/immed_18	testbench.sv(18)	0	1
/TOP/TEST#ublk#182146786#28/immed_29	testbench.sv(29)	0	1
/TOP/TEST#ublk#182146786#41/immed_42	testbench.sv(42)	0	1

Total Coverage By Instance (filtered view): 100.00%