Es concepts

Computing system divides into

1. General purpose
2. Specific purpose

Computing system contains

1.processor

2. Memory

3. Input/output

Es constraints

1.power

2.Performance

3.cost

4.size

- system board (applicable or config ability)
- System on chip ex: VLSI (from 10.000 to 100.000 gate) which improve size and functionality

MPU (microprocessor unit)

1. Processor

2. Micro processor

3. CPU

MCU - computing system

1. MPU
2. Memory
3. I/O

(system on chip)Soc : it's MCU but with high performance

App

- Bare metal
- OS app

Processor

1. ALU
2. Control unit
3. Registers

Buses

- Address
- Data
- Control

Control unit cycle

1. Fetch

The control unit fetch the instruction from the memory in PC which include the address of next instruction and put it in IR register and increase PC

2.Decode

1. Instruction set
2. Instruction format

3. Execute

ISA (instruction set architecture)

1. RISC
2. CISC

Instruction decoder

1. Hard wired (logic gates) which use in RISC and use strong compiler
2. Memory mapped which use in CISC and use simple compiler

Registers file

- GPR (temporary)
- SPR / SFR

SFR

- pc (program counter)
- SP (stack pointer)
- ACC (accumulator)
- IR (instruction register)
- PSW (process status word) include flags(sign - zero - overflow - negative)
- that contain last process in ALU

Memory

1 location = 1 byte = 8 bit

Basic memory element is D flip flop

In memory

1. Capacity
2. Speed
3. Organization

- Volatile memory (RAM) when power is off the data will be deleted and it's faster than ROM
- Nonvolatile memory (ROM) when power is off the data will not be deleted
- Hybrid

- Volatile (RAM / RWM)
  Static RAM based on transistor use minimum 6 transistors and faster because it doesn't use refreshment circuit but it's high cost

- Dynamic RAM
  based on cap and simple mosfet
  It's slow because refreshment circuit has priority than CPU so access time will increase but advantages are it's simple, low cost per bit, high density which means big size and low power consumption

- Non volatile (ROM) read only memory for processor - program memory, it's based on floating gate mosfet
  In floating gate for -ve charge (zero) programing state
  for +ve charge (one) erasing state

ROM types

- Mask programmable ROM (can't change) (OTP)
- PROM (OTP) it contains fuses which the user(programmable) burn the code and the burned one means zero and non-burned means one
- EPROM - erasable prom by UV and can save data for years but it effected by noise and radiation

Hybrid

1. EEPROM electrical EPROM endurance 100,000 read and write times, and it's byte access, high cost per bit

   Internal EEPROM

   External EEPROM

2. Flash faster than EEPROM because it block access (sector by sector) with endurance 10,000 , low cost per bit

3. NVRAM (SRAM + battery) or (SRAM + EEPROM + low battery)

Cache memory

- It can be hit or miss it's SRAM + controller.
- We use cache coherence to change RAM with all caches in other cores know what is the updated RAM.
- FPU (floating point unit) use in floating numbers.
- MPU (memory protection unit) it put between cache and main RAM , It use to divide RAM to ranges.
- MMU(memory management unit).

Architecture

1. Von Neumann (one memory system) in PC

2. Harvard (more than one memory) in microwave controller because it's faster Which can access RAM by c language which translated into load / store , can access ROM by read / write in assembly .

- Pipeline : make fetch, decode , execute in one cycle.
- Von Neumann : can't support pipeline.
- Harvard : can support pipeline.
- RISC : can support pipeline.
- CISC : can't support pipeline.

RISC -> 1 instruction -> 1 cycle.

Clock systems

1. Electrical -> RC-oscillator (low cost , low accuracy , high settling time , low temperature noise immunity ,low electric magnetic interface noise immunity , high vibration noise immunity)

2. Mechanical -> material -> ceramic or crystal oscillator

crystal oscillator (high cost , high accuracy , low settling time , high temperature noise immunity , high electric magnetic interface noise immunity, low vibration noise immunity)

Connection

- Port mapped
- Memory mapped

Every device has range of address -> base address + offset address.

Peripheral -> hardware circuit + register.

- TRM -> technical reference manual that includes the specs which include memory map (base , end) and base , offset for the peripheral.

- CPU initiate transaction write (address, data , size).

- Bus bridges -> change from one system bus protocol to another.