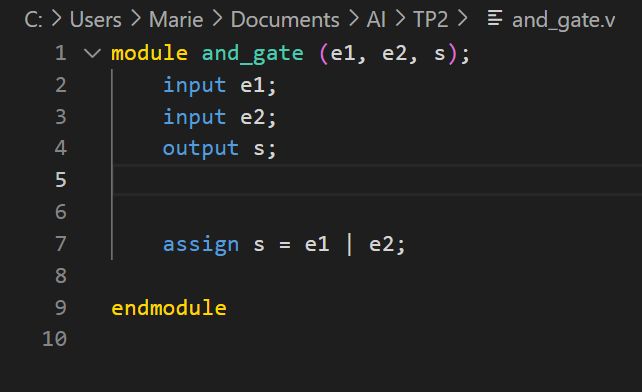
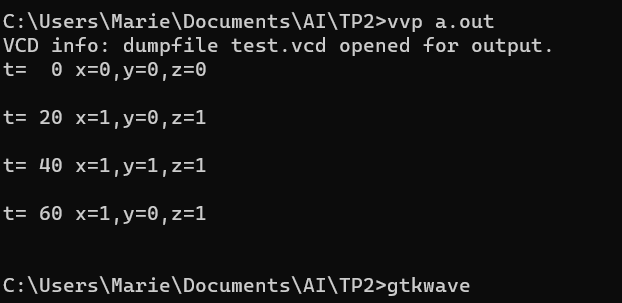
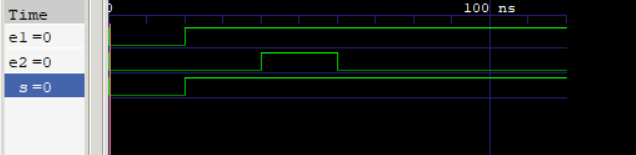


Exercice 2





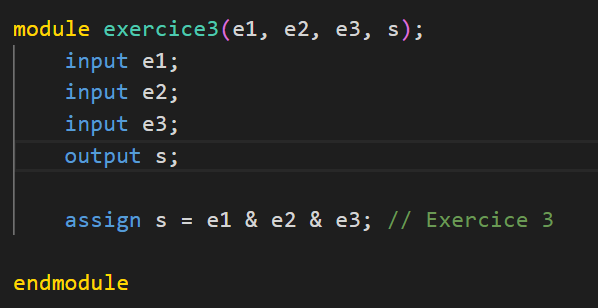




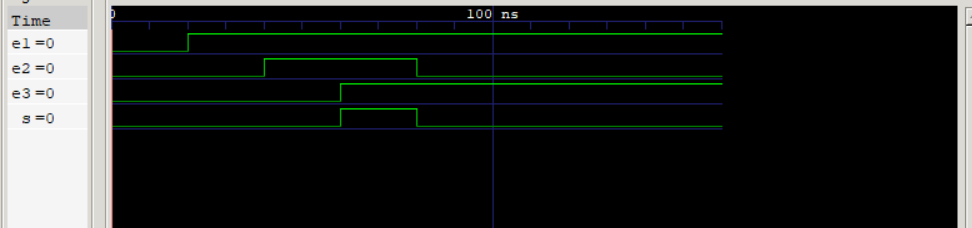
Exercice Reg vs wire

Exercice – assign vs always

Exercice 3







Additionneur 1 Bit

