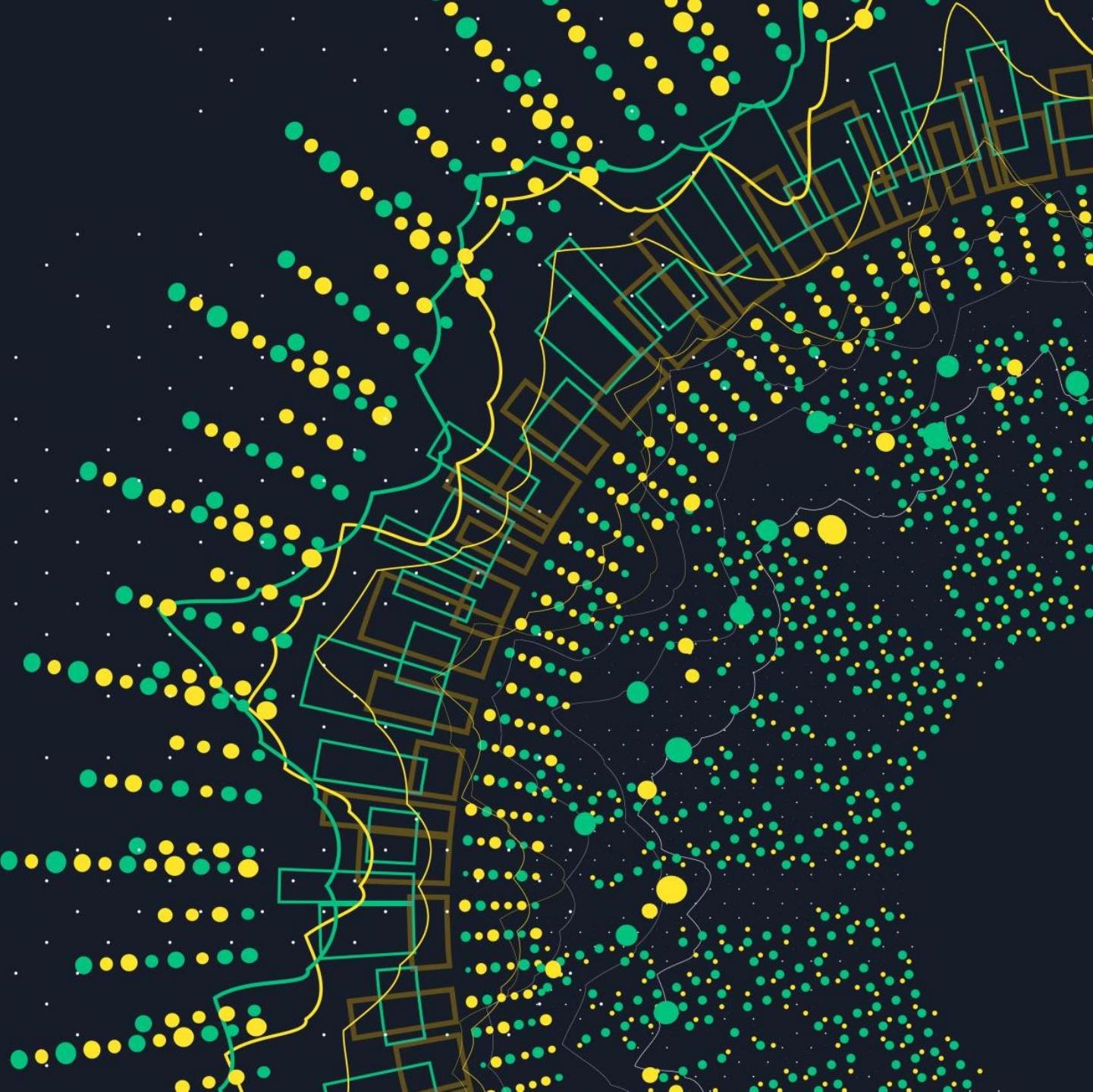

64-TAP 16-BIT FINITE IMPULSE RESPONSE IMPLEMENTATION

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ARCHITECTURE OF OUR FIR CORE

FIR Core Modules in Testbench

1. FIFO:

1. Buffers input data and synchronizes it between the 10 kHz input sampling clock (clk1) and the 10 MHz core processing clock (clk2).
2. Provides FIFO_full and FIFO_empty status signals.

2. Coefficient Memory (CMEM):

1. Stores the preloaded filter coefficients accessed during FIR operation.
2. Addressed using the tap count from the controller.

3. ALU:

1. Performs multiplication of input data with coefficients and accumulates results to compute the filtered output.

4. Accumulator:

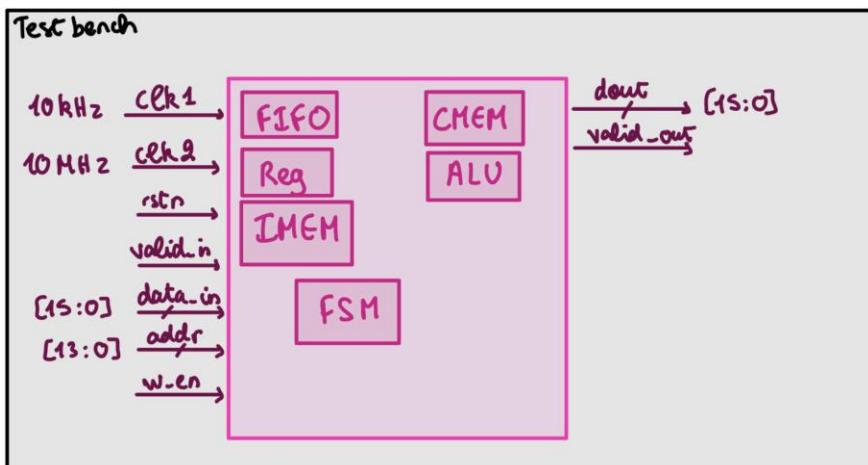
1. Temporarily stores intermediate results during the filter's convolution operation.

5. Controller (FSM):

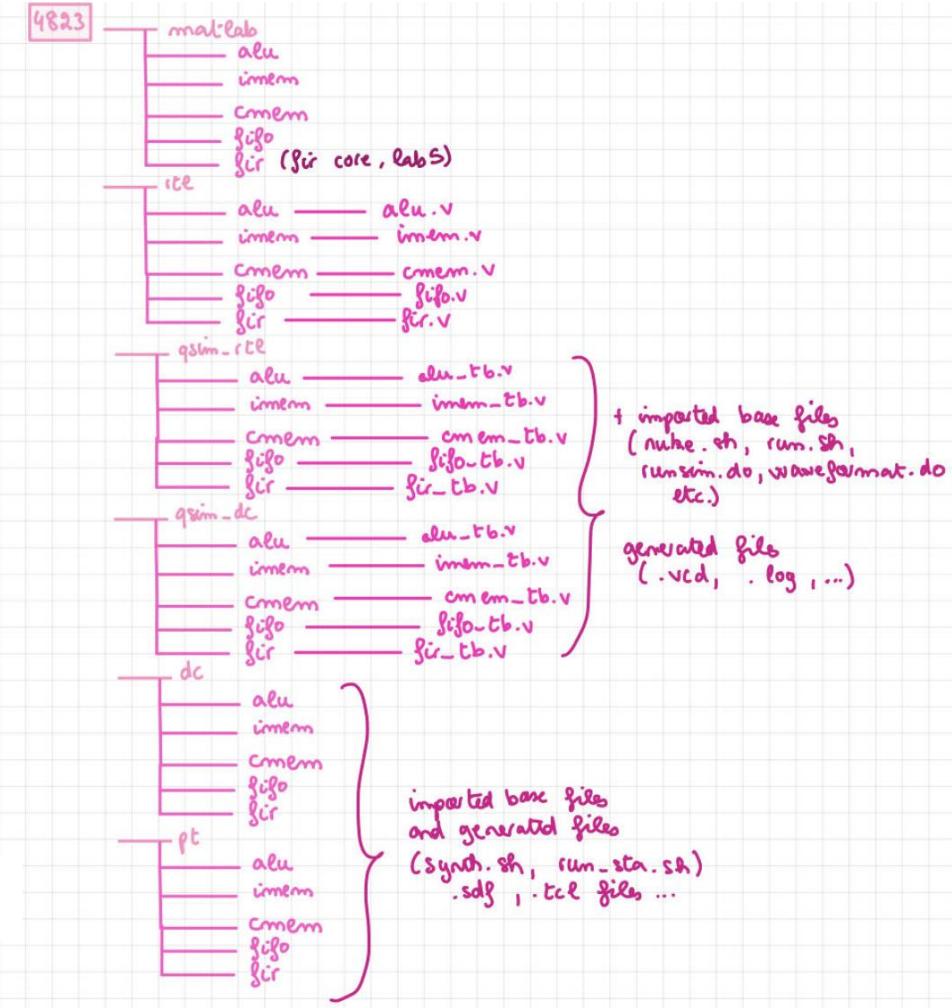
1. Coordinates operations between FIFO, CMEM, and ALU.
2. Provides controller_enable and monitors datapath_done.
3. Signals valid_out when the filtered output is ready.

6. Top-Level FIR Core:

1. Instantiates the **Datapath** (FIFO, CMEM, ALU, Accumulator) and **Controller** modules.
2. Outputs the 16-bit filtered result (dout) and indicates when it is valid (valid_out).



Project Structure Hierarchy



FIR FILTER DESIGN: KEY METRICS

Methods:

- **Input:** Randomly generated 10k 16-bit real-valued numbers.
- **RTL Coding:** Designed entirely from scratch.
- **Throughput:** Calculated using PrimeTime (PT) with DC-generated SDF annotation.
- **Maximum Clock Frequency:** Determined via PT with DC-generated SDF annotation.
- **Energy Efficiency:** Measured using PT with DC-generated SDF and QS-generated VCD annotations.
- **Area:** Calculated using the DC-generated report.
- **Accuracy:** Evaluated using RMSE against MATLAB results (32-bit floating-point numbers, inputs are 16-bit, generated via MATLAB random function).

Results:

- **Throughput:** 10 kS/s.
- **Maximum Clock Frequency:** 11.06 GHz.
- **Energy Efficiency:** 0.5487 pJ/sample.
- **Area:** 0.7704 mm².
- **Accuracy:**
 - Worst Case: 83.3%.
 - Average Case: 87.5%.