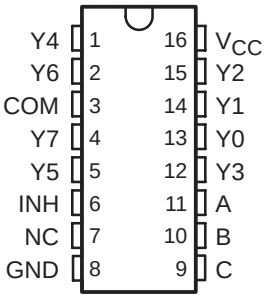
- **Injection-Current Cross Coupling <1mV/mA (see Figure 1)**
- **Low Crosstalk Between Switches**
- **Pin Compatible With SN74HC4051, SN74LV4051A, and CD4051B**
- **2-V to 6-V V_{CC} Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

D, DGV, N, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

This eight-channel CMOS analog multiplexer/demultiplexer is pin compatible with the ’4051 function and, additionally, features injection-current effect control, which has excellent value in automotive applications where voltages in excess of normal supply voltages are common.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply-voltage range.

ORDERING INFORMATION

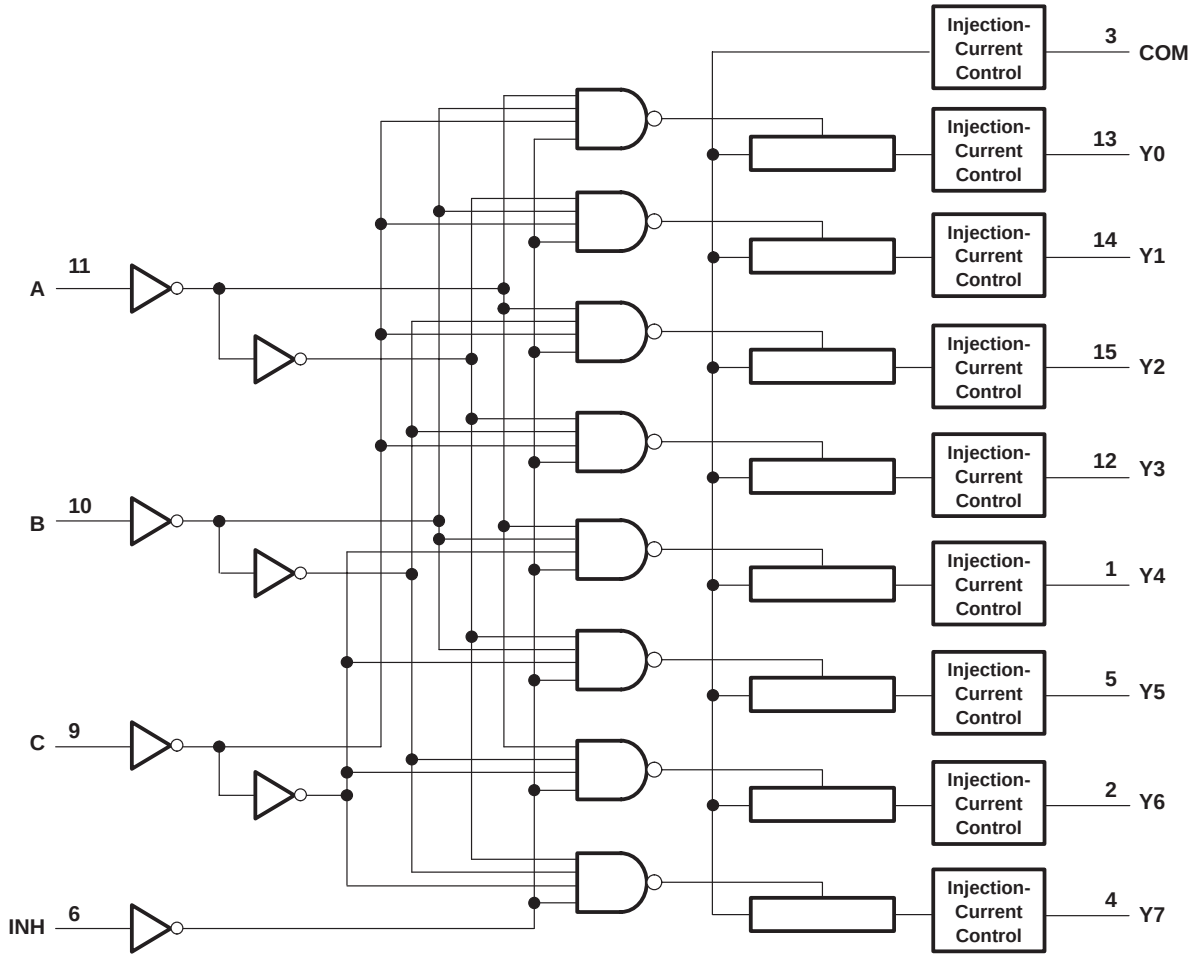
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	PDIP − N	Tube	SN74HC4851N	HC4851N
	SOIC − D	Tube	SN74HC4851D	HC4851
		Tape and reel	SN74HC4851DR	
	TSSOP − PW	Tube	SN74HC4851PW	HC4851
		Tape and reel	SN74HC4851PWR	
	TVSOP − DGV	Tape and reel	SN74HC4851DGVR	HC4851

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
I/O diode current, I_{IOK} (V_{IO} < 0 or V_{IO} > V_{CC}) . . . . . ±20 mA
Switch through current, I_T (V_{IO} = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 73°C/W
DGV package . . . . . 120°C/W
N package . . . . . 67°C/W
PW package . . . . . 108°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 3.3 V	2.3		
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 3.3 V		1	
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Control input voltage		0	V_{CC}	V
V_{IO}	Input/output voltage		0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall time	V_{CC} = 2 V		1000	ns
		V_{CC} = 3 V		800	
		V_{CC} = 3.3 V		700	
		V_{CC} = 4.5 V		500	
		V_{CC} = 6 V		400	
T_A	Operating free-air temperature		−40	125	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r_{on}	On-state switch resistance	$I_T \le 2$ mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$ (see Figure 5)	2.V		500	650		670		700	Ω
			3 V		215	280		320		360	
			3.3 V		210	270		305		345	
			4.5 V		160	210		240		270	
			6 V		150	195		220		250	
Δr_{on}	Difference in on-state resistance between switches	$I_T \le 2$ mA, $V_I = V_{CC}/2$, $V_{INH} = V_{IL}$	2.V		4	10		15		20	Ω
			3 V		2	8		12		16	
			3.3 V		2	8		12		16	
			4.5 V		2	8		12		16	
			6 V		3	9		13		18	
I_I	Control input current	$V_I = V_{CC}$ or GND	6 V			±0.1		±0.1		±1	μA
$I_{S(off)}$	Off-state switch leakage current (any one channel)	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IH}$ (see Figure 6)	6 V			±0.1		±0.5		±1	μA
	Off-state switch leakage current (common channel)	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IH}$ (see Figure 7)				±0.2		±2		±4	
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 8)	6 V			±0.1		±0.5		±1	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	6 V			2		20		40	μA
C_{IC}	Control input capacitance	A, B, C, INH			3.5	10		10		10	pF
C_{IS}	Common terminal capacitance	Switch off			22	40		40		40	pF
C_{OS}	Switch terminal capacitance	Switch off			6.7	15		15		15	pF

injection current coupling specifications, T_A = −40°C to 125°C

PARAMETER		V_{CC}	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V\Delta_{out}$	Maximum shift of output voltage of enabled analog channel	3.3 V	$R_S \le 3.9$ kΩ	I_I‡ ≤ 1 mA		0.05	1	mV
		5 V				0.1	1	
		3.3 V		I_I‡ ≤ 10 mA		0.345	5	
		5 V				0.067	5	
		3.3 V	$R_S \le 20$ kΩ	I_I‡ ≤ 1 mA		0.05	2	
		5 V				0.11	2	
		3.3 V		I_I‡ ≤ 10 mA		0.05	20	
		5 V				0.024	20	

† Typical values are measured at T_A = 25°C.
‡ I_I = total current injected into all disabled channels

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2 V, C_L = 50 pF (unless otherwise noted) (see Figures 9−14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM		19.5	25		29		32	ns
t_{PLH} t_{PHL}	Propagation delay time	Channel Select	COM or Yn		23	30		35		40	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn			95		105		115	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn			95		105		115	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3 V, C_L = 50 pF (unless otherwise noted) (see Figures 9−14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM		12	15.5		17.5		19.5	ns
t_{PLH} t_{PHL}	Propagation delay time	Channel Select	COM or Yn		13.5	17.5		20		23	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn			90		100		110	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn			90		100		110	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V, C_L = 50 pF (unless otherwise noted) (see Figures 9−14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM		11	14.5		16.5		18.5	ns
t_{PLH} t_{PHL}	Propagation delay time	Channel Select	COM or Yn		12.5	16.5		19		22	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn			85		95		105	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn			85		95		105	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V, C_L = 50 pF (unless otherwise noted) (see Figures 9−14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM		8.6	11.5		12.5		13.5	ns
t_{PLH} t_{PHL}	Propagation delay time	Channel Select	COM or Yn		10	13		15		17	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn			80		90		100	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn			80		90		100	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, C_L = 50 pF (unless otherwise noted) (see Figures 9−14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM		8	10		11		12	ns
t_{PLH} t_{PHL}	Propagation delay time	Channel Select	COM or Yn		9.5	12.5		14.5		16.5	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn			78		80		80	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn			78		80		80	ns

operating characteristics, T_A = 25°C (see Figure 15)

PARAMETER		V_{CC}	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	3.3 V	No load	32	pF
		5 V		37	

APPLICATION INFORMATION

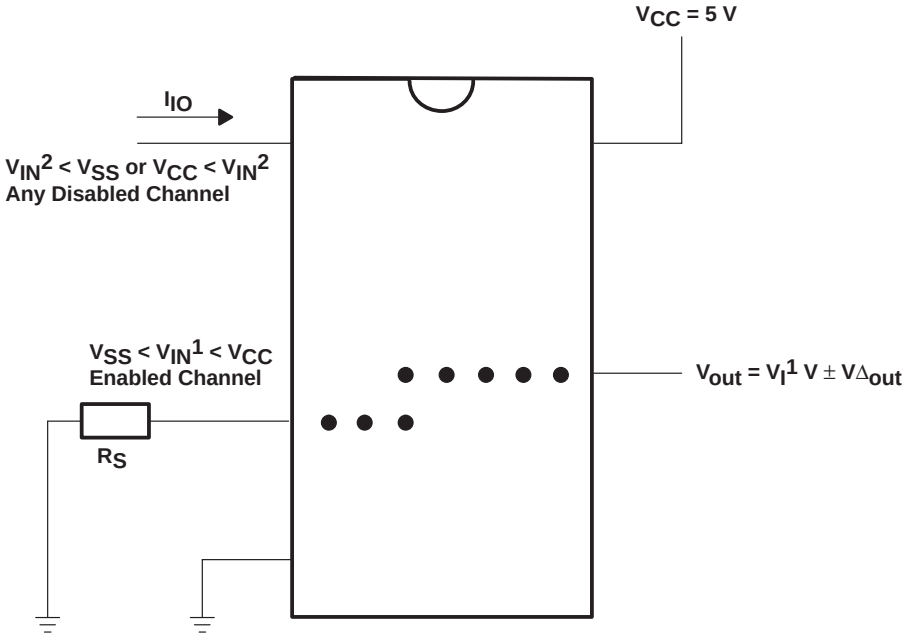


Figure 1. Injection-Current Coupling Specification

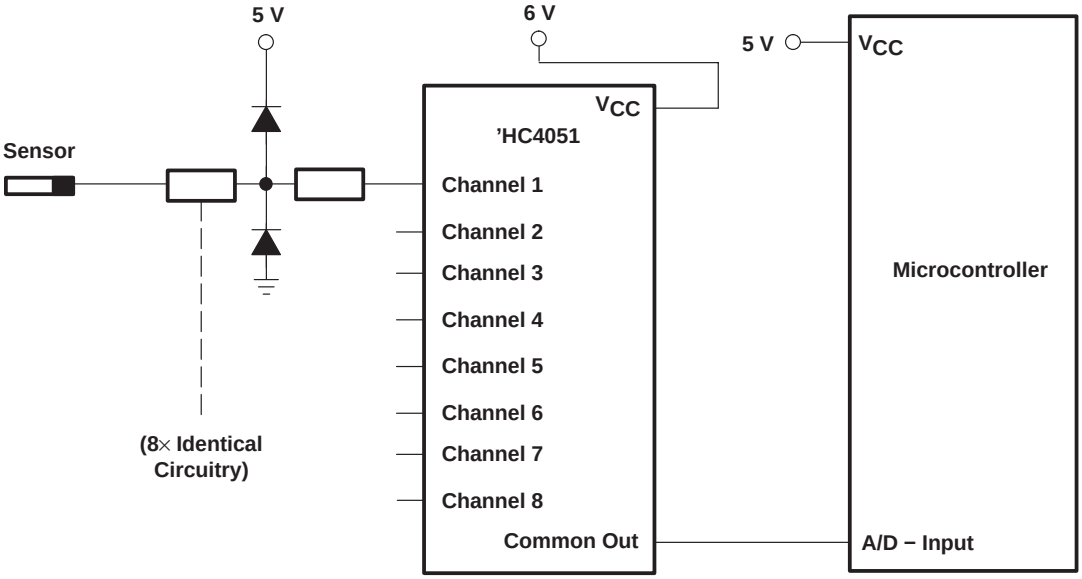


Figure 2. Alternate Solution Requires 32 Passive Components and One Extra 6-V Regulator to Suppress Injection Current Into a Standard 'HC4051 Multiplexer

APPLICATION INFORMATION

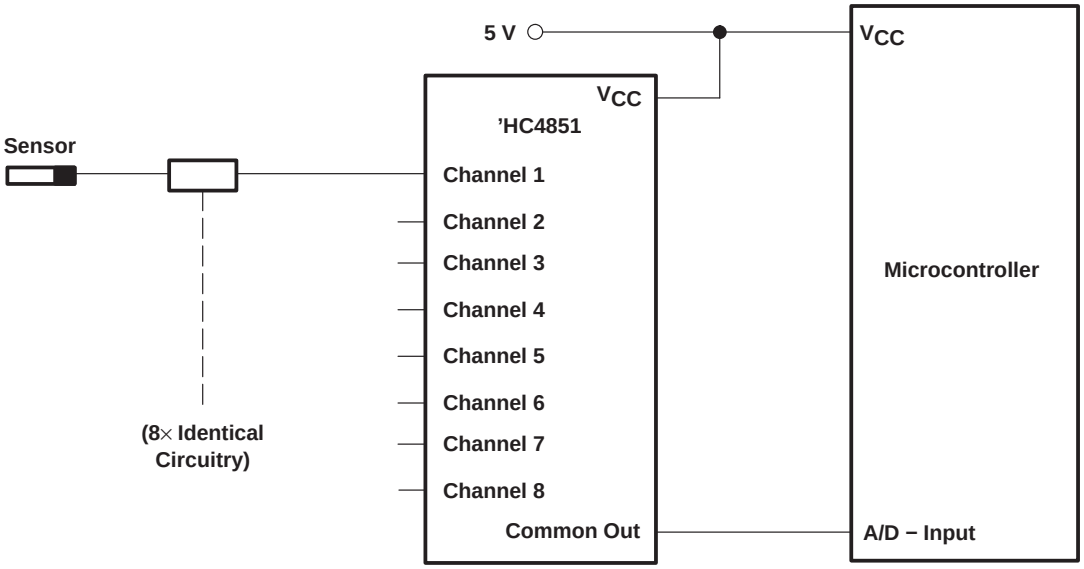


Figure 3. Solution by Applying the 'HC4851 Multiplexer

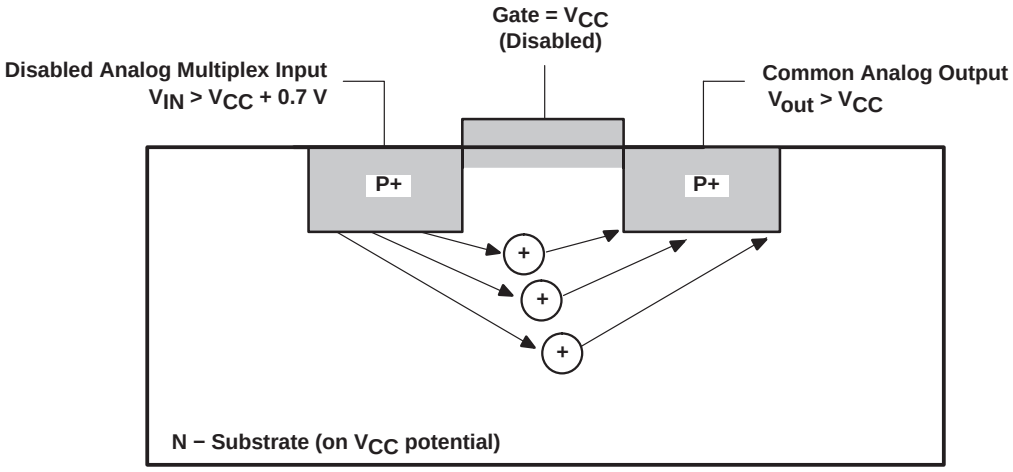


Figure 4. Diagram of Bipolar Coupling Mechanism (Appears if V_{IN} Exceeds V_{CC}, Driving Injection Current Into the Substrate)

PARAMETER MEASUREMENT INFORMATION

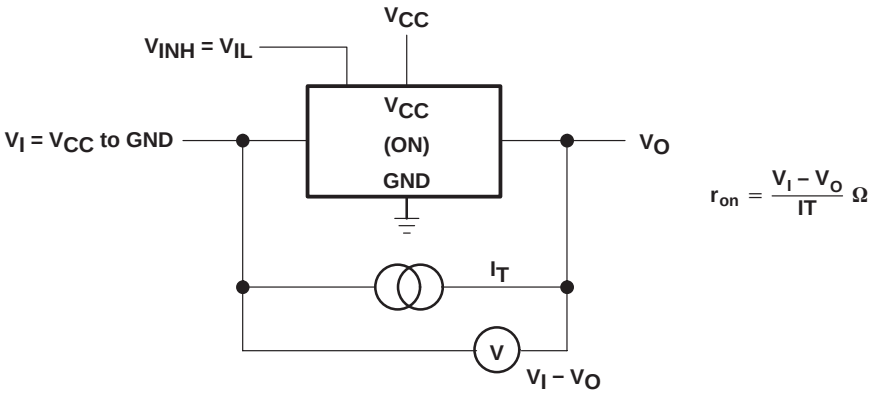


Figure 5. On-State-Resistance Test Circuit

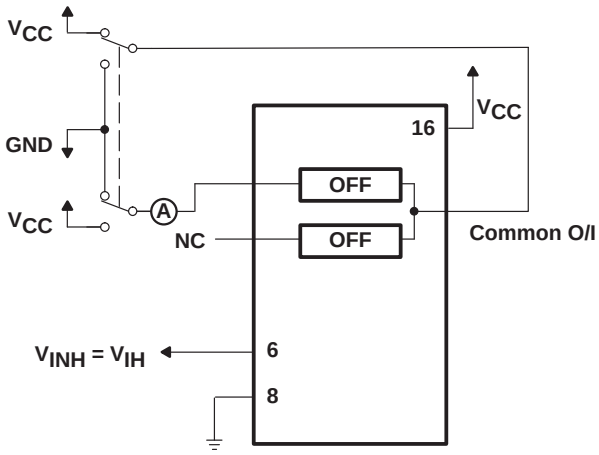


Figure 6. Maximum Off-Channel Leakage Current, Any One Channel, Test Setup

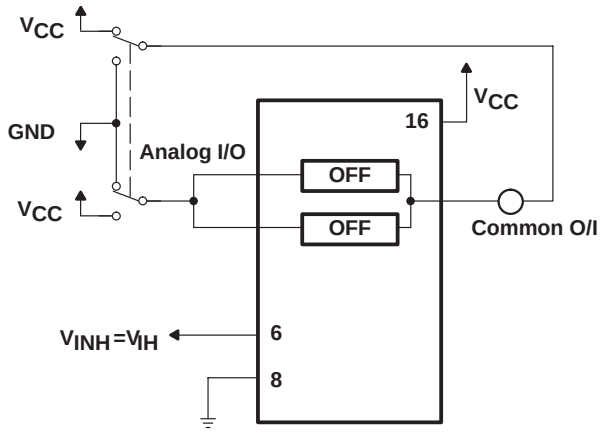


Figure 7. Maximum Off-Channel Leakage Current, Common Channel, Test Setup

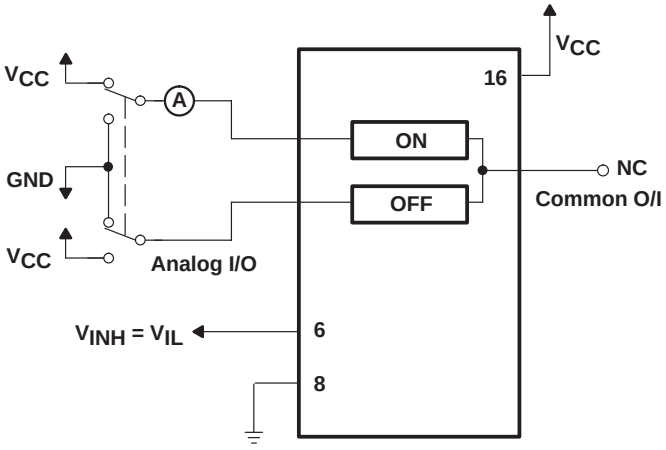


Figure 8. Maximum On-Channel Leakage Current, Channel To Channel, Test Setup

PARAMETER MEASUREMENT INFORMATION

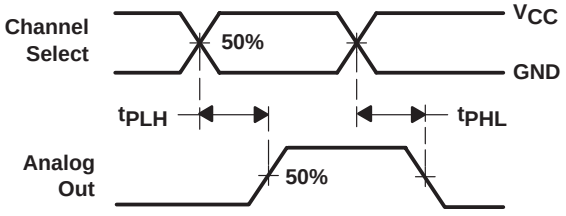
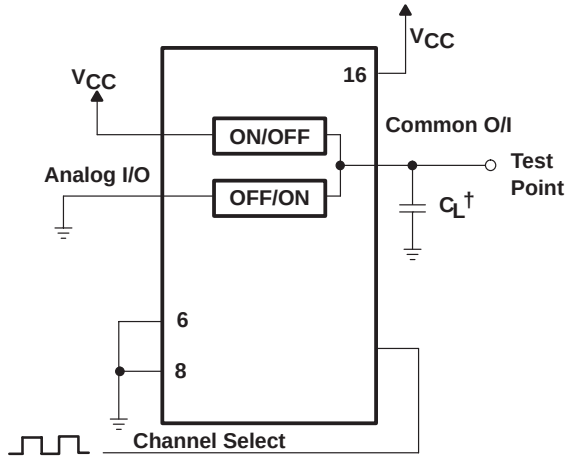


Figure 9. Propagation Delays, Channel Select to Analog Out



† Includes all probe and jig capacitance

Figure 10. Propagation-Delay Test Setup, Channel Select to Analog Out

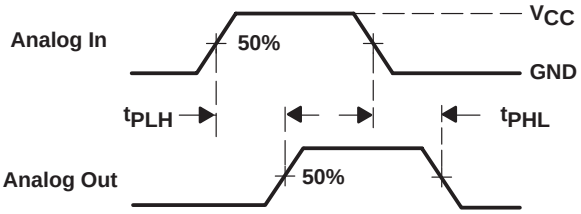
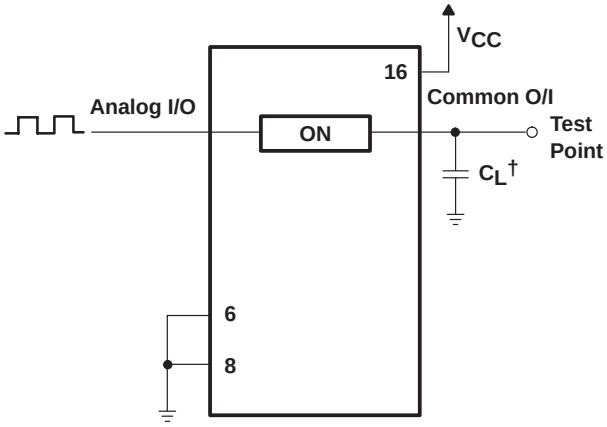


Figure 11. Propagation Delays, Analog In to Analog Out



† Includes all probe and jig capacitance

Figure 12. Propagation-Delay Test Setup, Analog In to Analog Out

PARAMETER MEASUREMENT INFORMATION

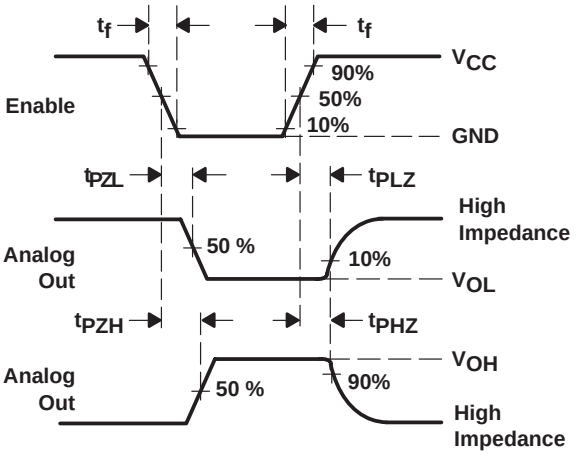


Figure 13. Propagation Delays, Enable to Analog Out

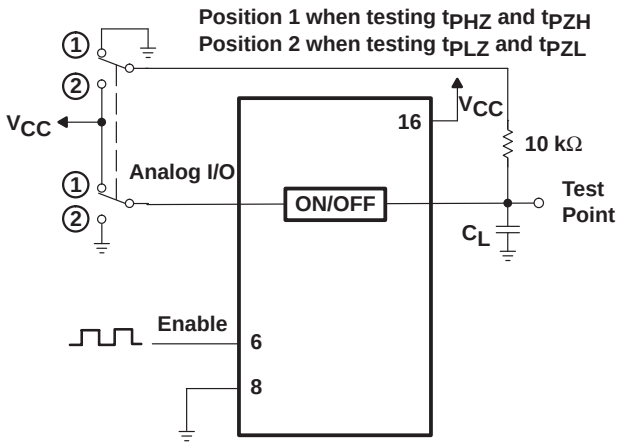


Figure 14. Propagation-Delay Test Setup, Enable to Analog Out

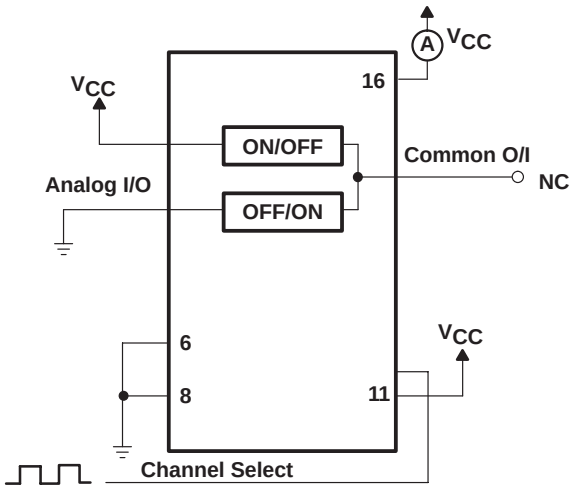


Figure 15. Power-Dissipation Capacitance Test Setup

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC4851D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4851	Samples
SN74HC4851DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4851	Samples
SN74HC4851DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HC4851	Samples
SN74HC4851DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4851	Samples
SN74HC4851DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4851	Samples
SN74HC4851N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC4851N	Samples
SN74HC4851PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4851	Samples
SN74HC4851PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HC4851	Samples
SN74HC4851PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4851	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74HC4851 :

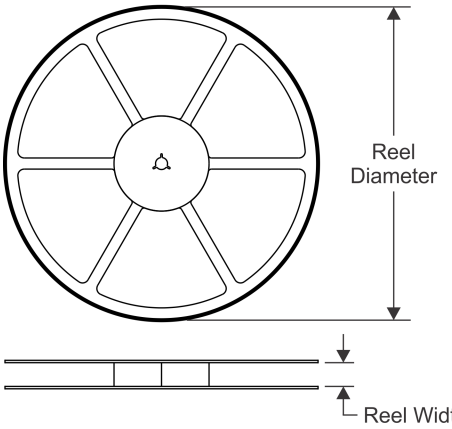
- Automotive: SN74HC4851-Q1

NOTE: Qualified Version Definitions:

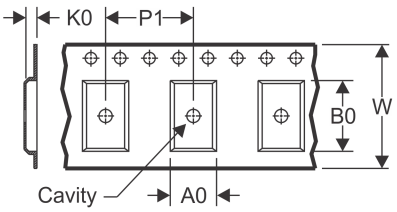
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

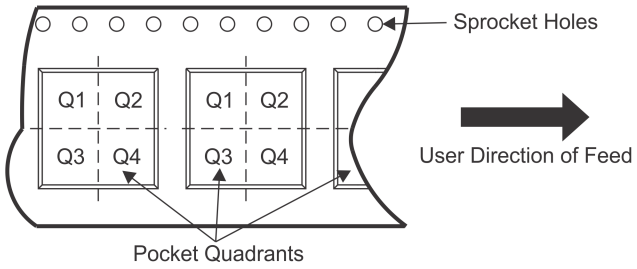


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

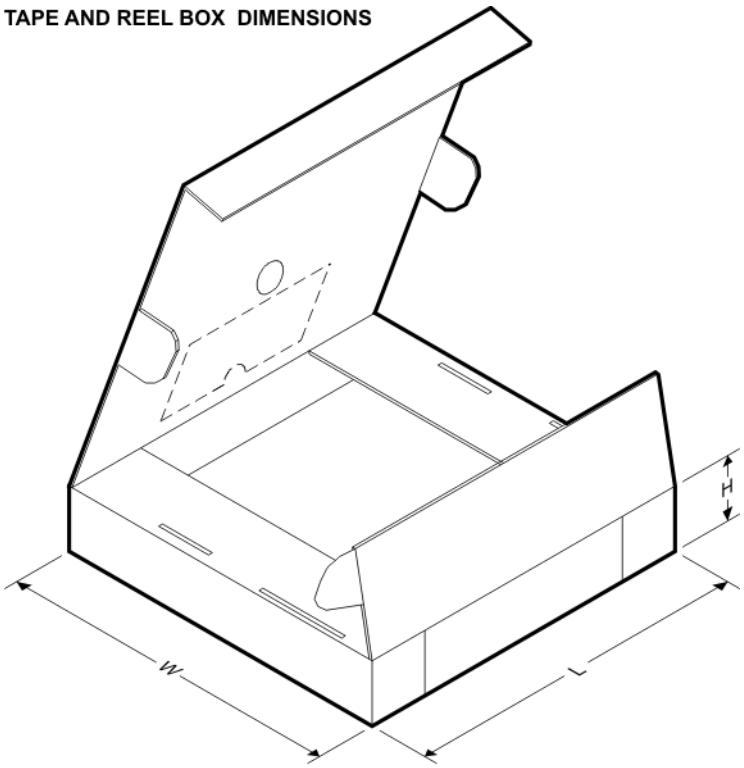
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4851DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74HC4851DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4851DR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4851DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4851PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4851PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4851PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

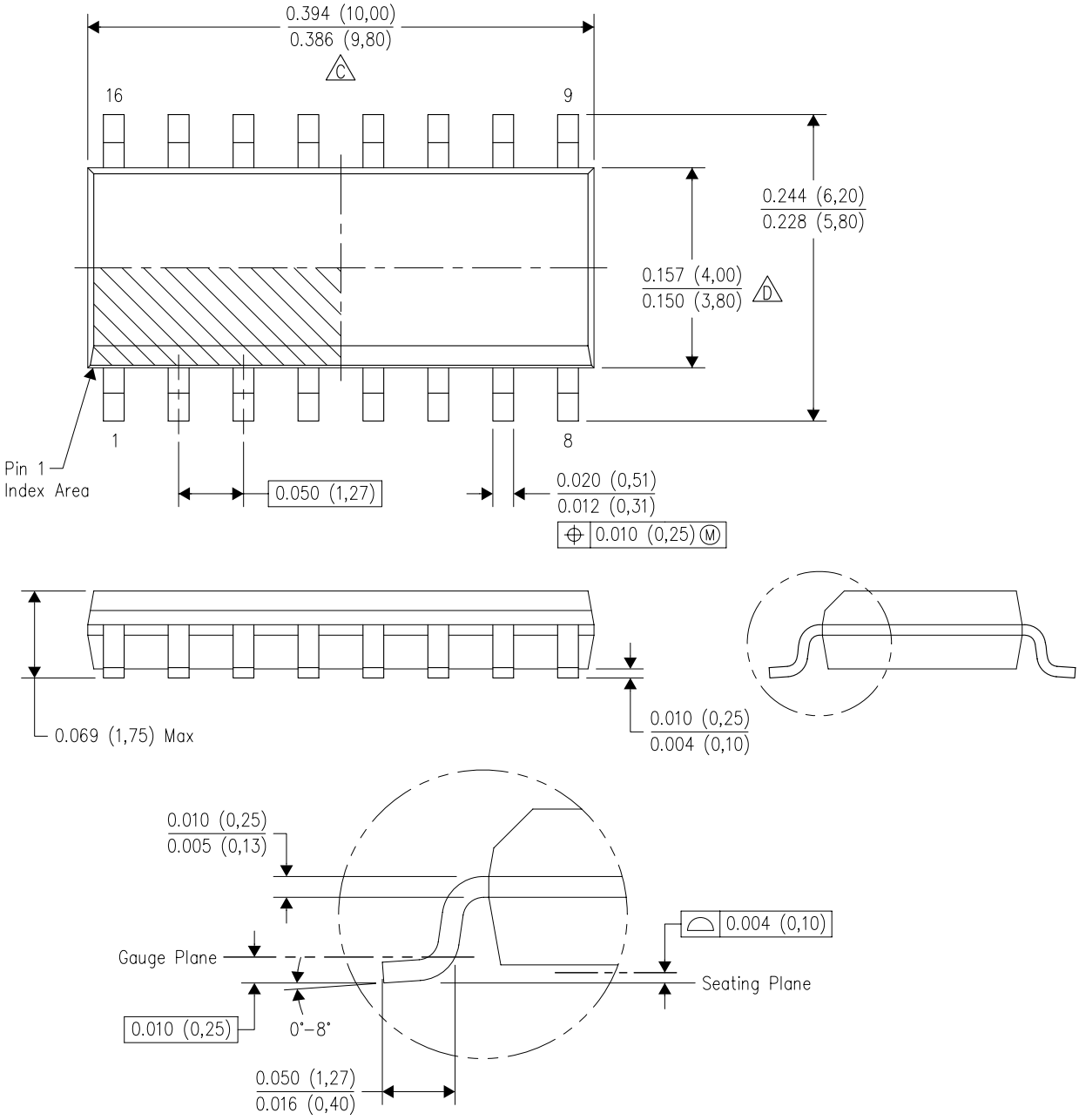
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

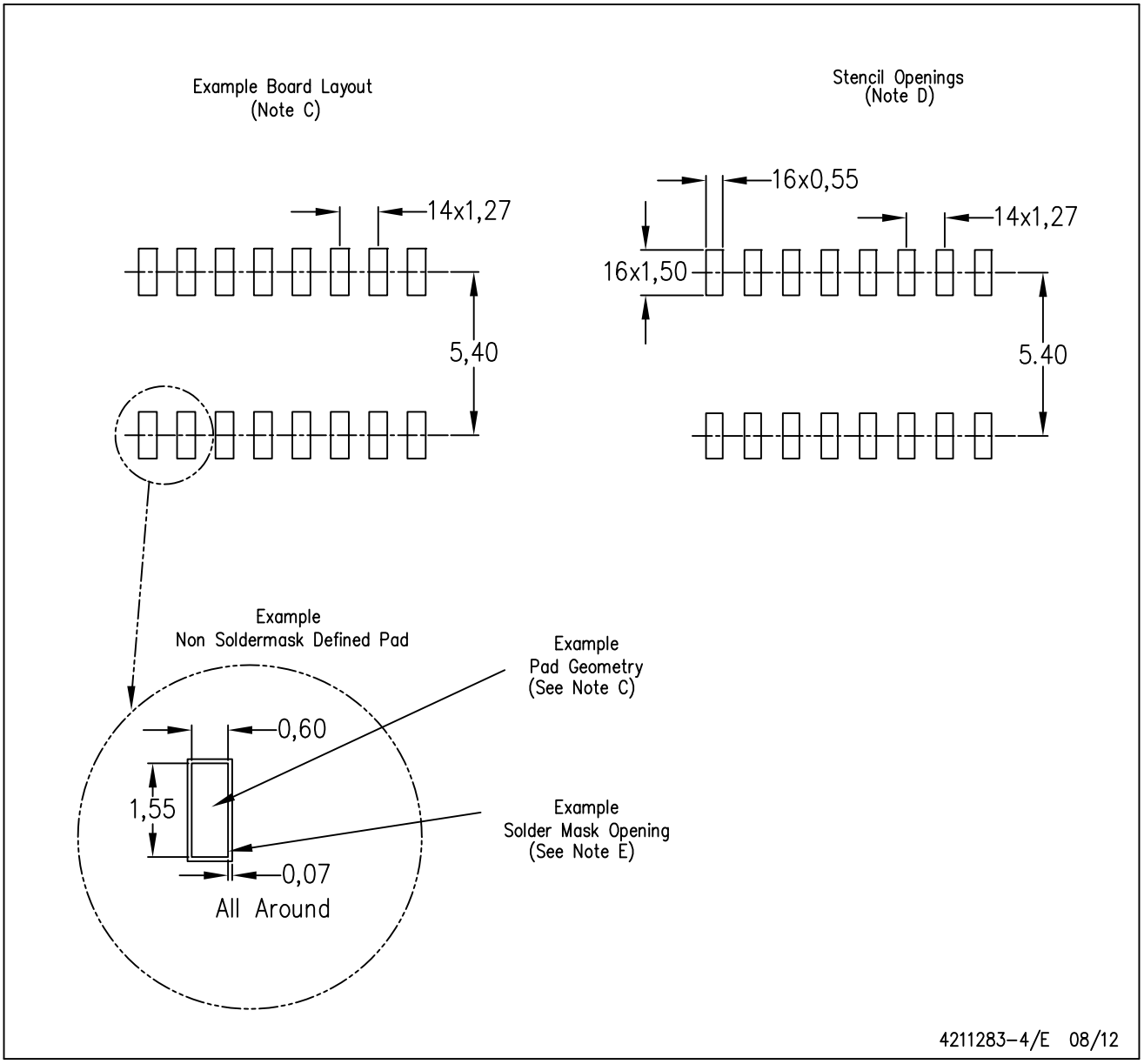
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4851DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74HC4851DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC4851DR	SOIC	D	16	2500	364.0	364.0	27.0
SN74HC4851DRG4	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC4851PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74HC4851PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74HC4851PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



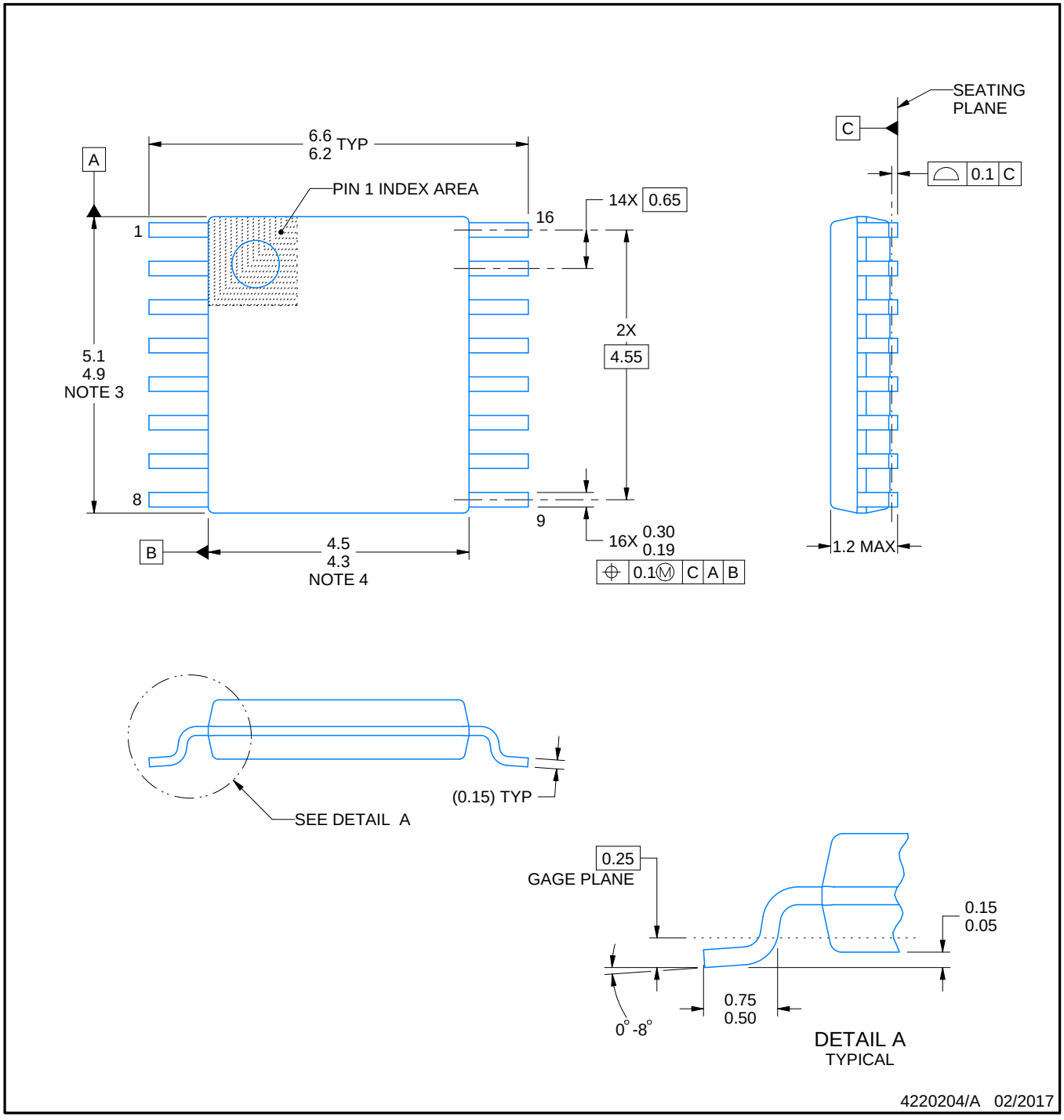
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

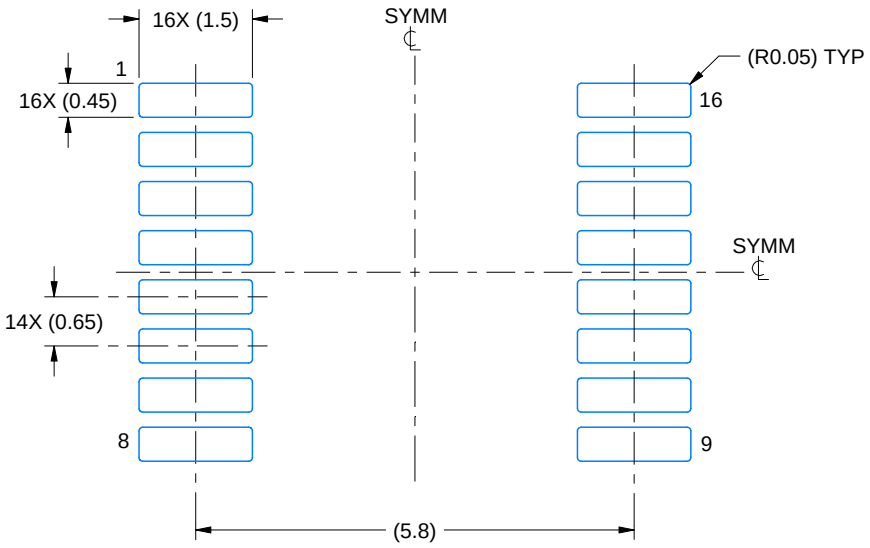
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

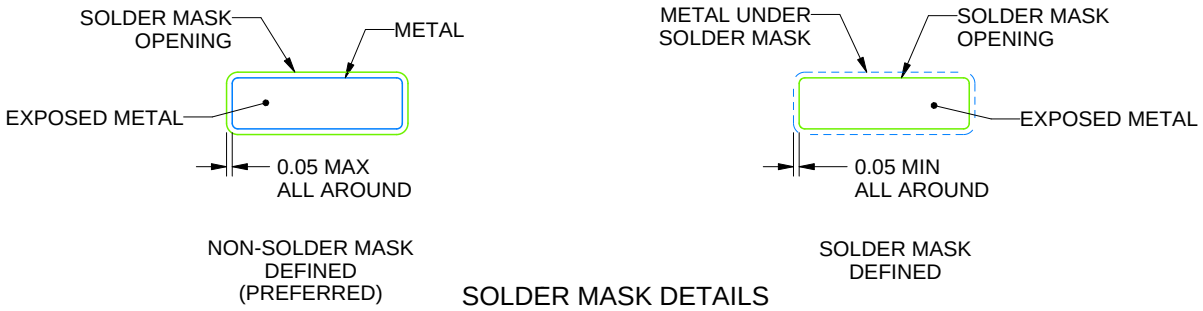


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

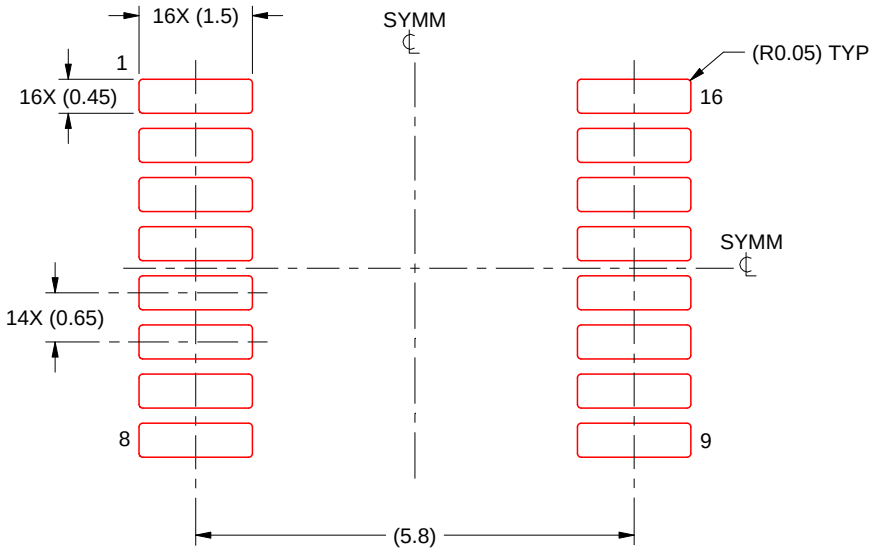


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

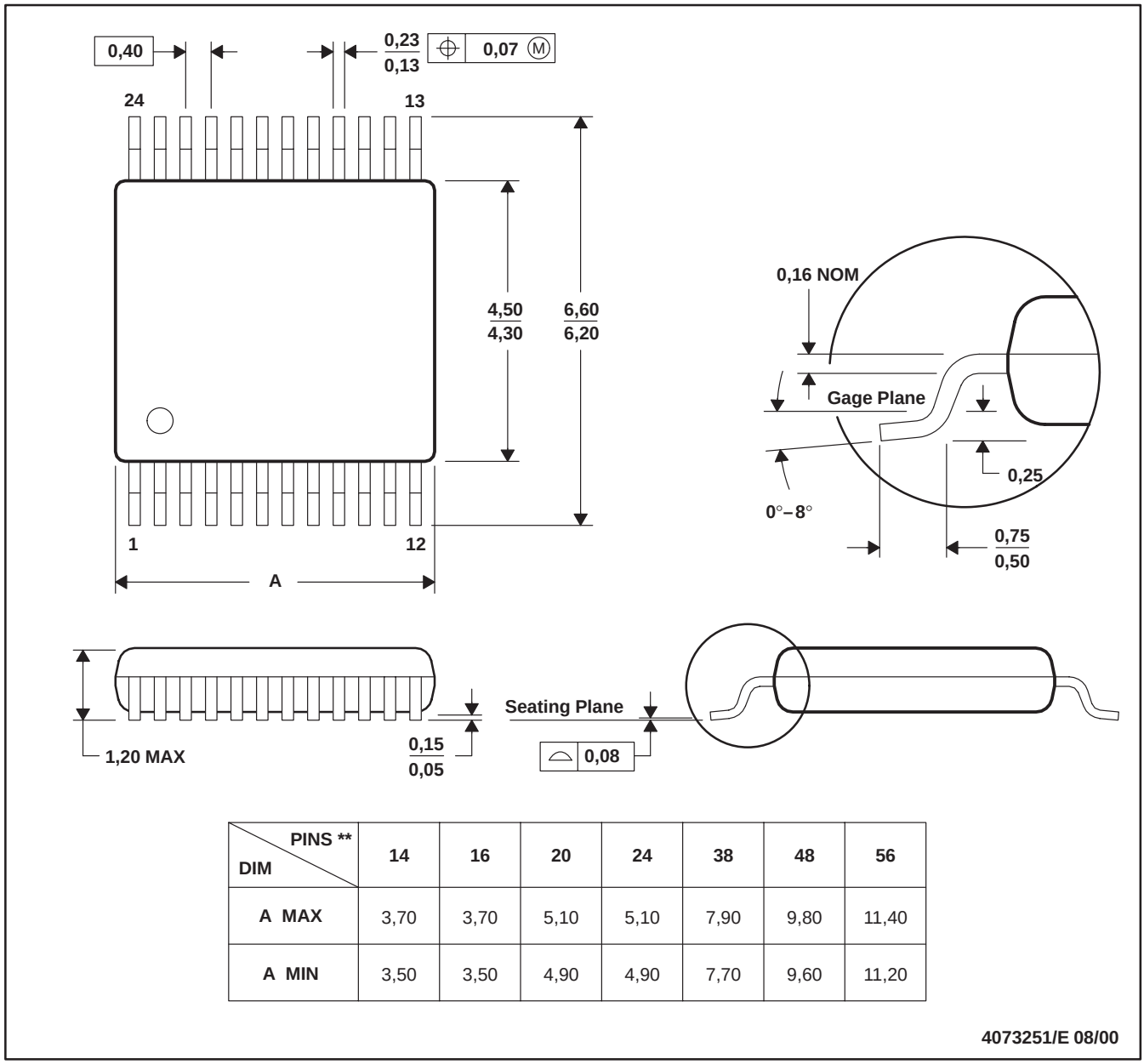
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

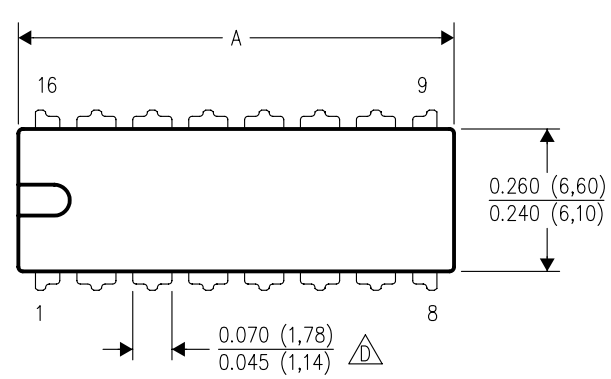
4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

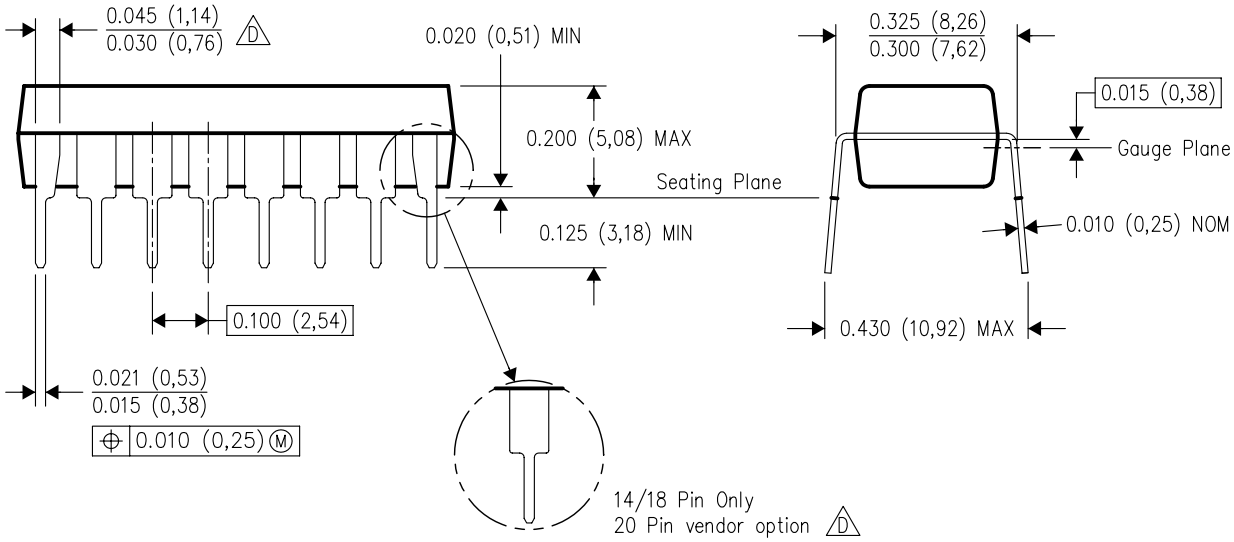
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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