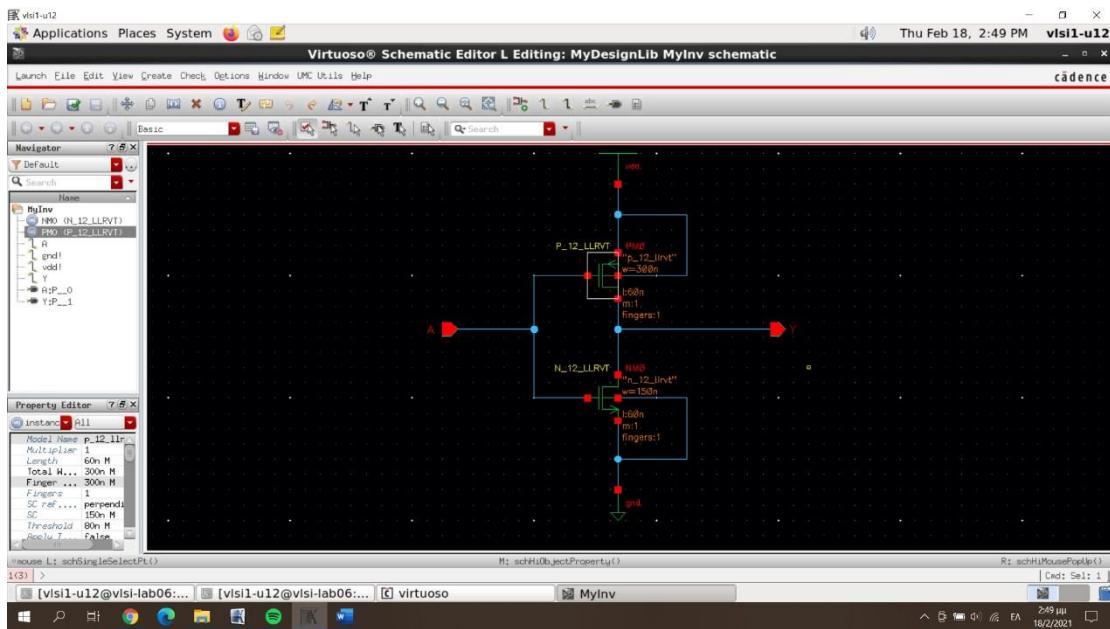


# VLSI

## ΑΝΑΦΟΡΑ

### ΓΚΙΖΑΣ ΜΑΡΙΝΟΣ

#### Άσκηση 1



- Trans-DC-Analysis



- Rise-Fall time των εξόδων

Rise time: 2.58927ns



Fall time: 2.44294ns



- Propagation delay των πυλών

Propagation delay high-low: 1.63082ns

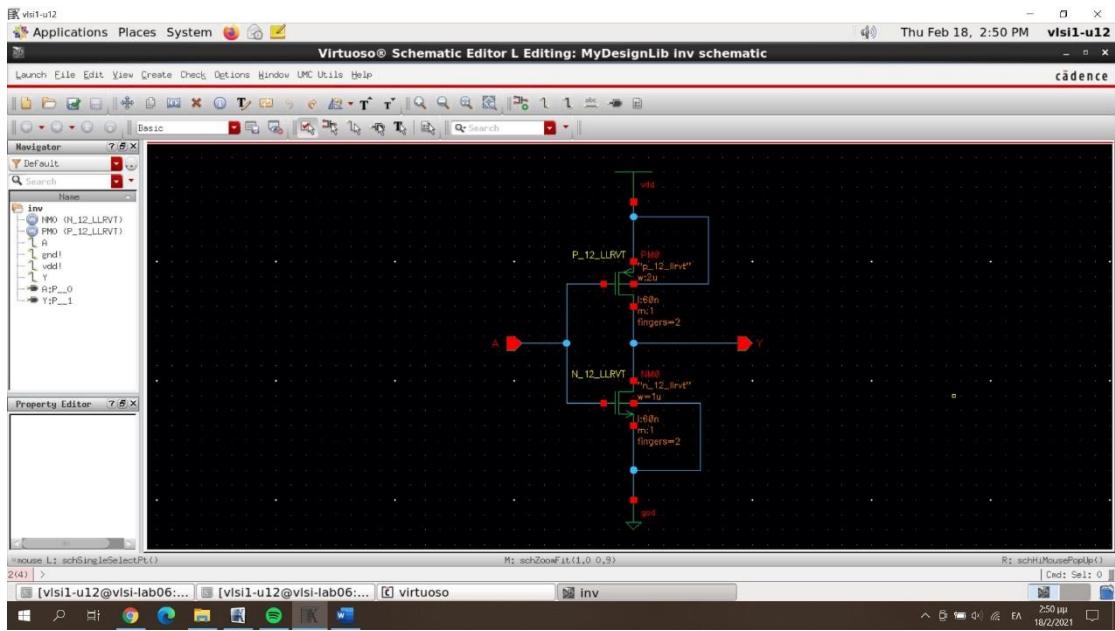


Propagation delay low-high: 2.3019ns

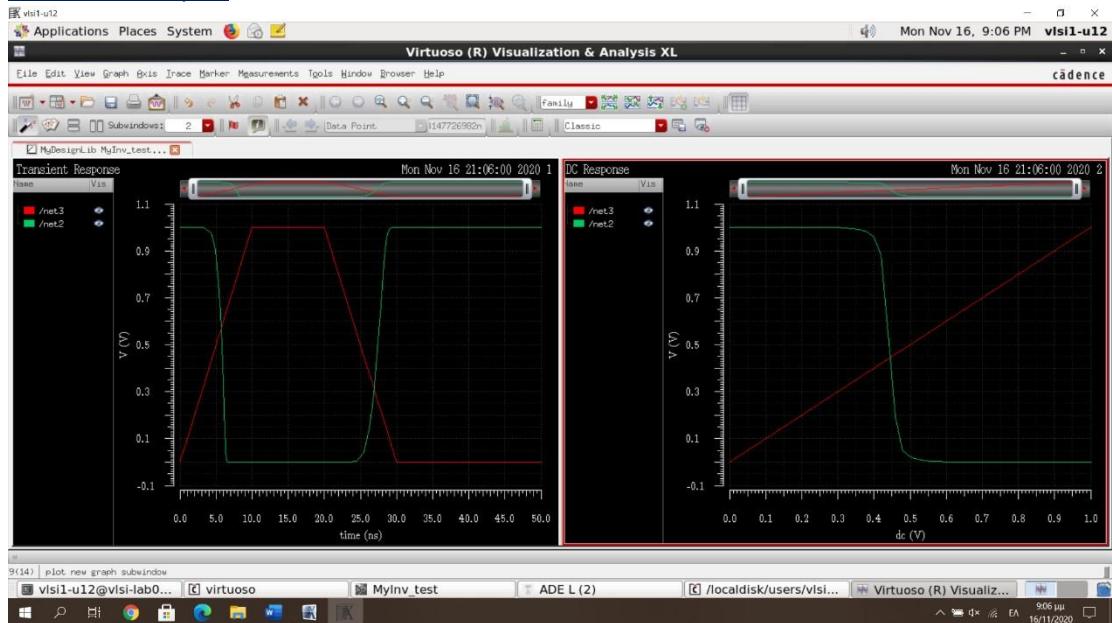


Total Propagation delay:  $t = (\text{Propagation delay low-high} + \text{Propagation delay high-low})/2 = 3.93272/2 = 1.96636\text{ns}$

Εργασία για το σπίτι(1)



- Trans-DC-Analysis:



- Rise-Fall time των εξόδων:

Rise time: 1.33337ns



Fall time: 1.31102ns



- Propagation delay των πυλών:

Propagation delay high-low: 345.597ps



Propagation delay low-high:680.704ps



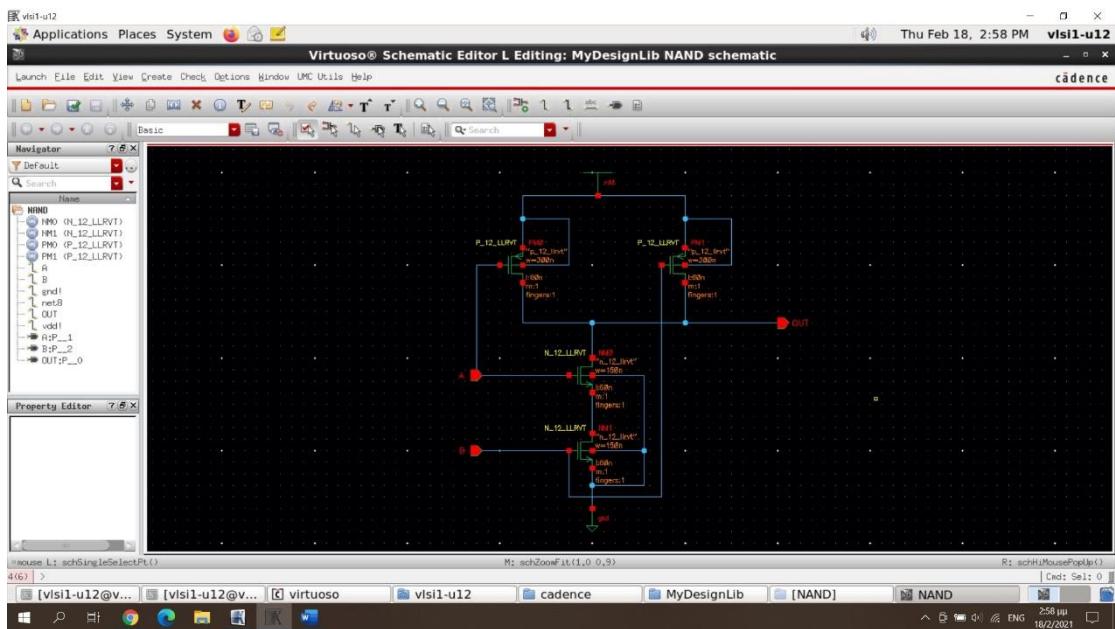
Total Propagation delay:  $t = (\text{Propagation delay low-high} + \text{Propagation delay high-low})/2 = 1.026.301/2 = 513.1505\text{ps}$

### Παρατηρήσεις:

1. Όταν το πλάτος είναι μεγαλύτερο και έχουμε 1 finger/transistor, η κλίση στην έξοδο είναι μεγαλύτερη απότι όταν έχουμε μικρότερο πλάτος και 2 finger.
2. Όταν το πλάτος είναι μεγαλύτερο και έχουμε 1 finger/transistor, το rise time είναι μεγαλύτερο από το fall time ενώ στην δεύτερη περίπτωση το rise time με το fall time είναι παρόμοια.
3. Το propagation delay στην πρώτη περίπτωση είναι μεγαλύτερο απότι στην δεύτερη περίπτωση

## Άσκηση 2

### NAND



### Trans-Analysis:



### DC-Analysis:



- Rise-Fall time των εξόδων

Rise time: 1.341386ns



Fall time: 1.8113261ns



- Propagation delay των πυλών:

Propagation delay high-low: 1.91999ns



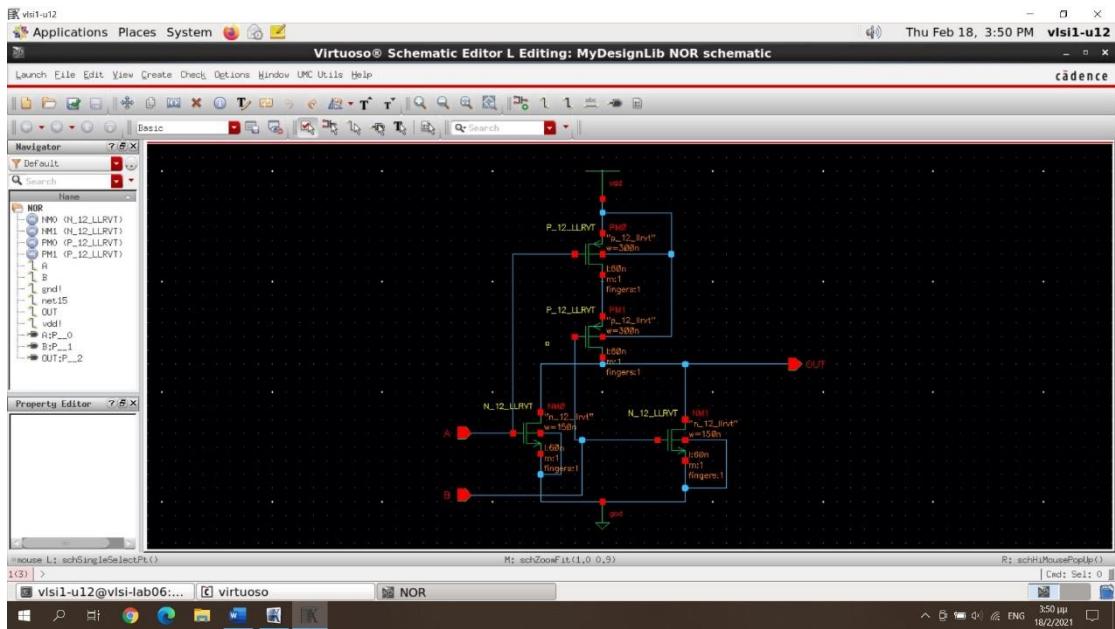
Propagation delay low- high: 1.13812ns



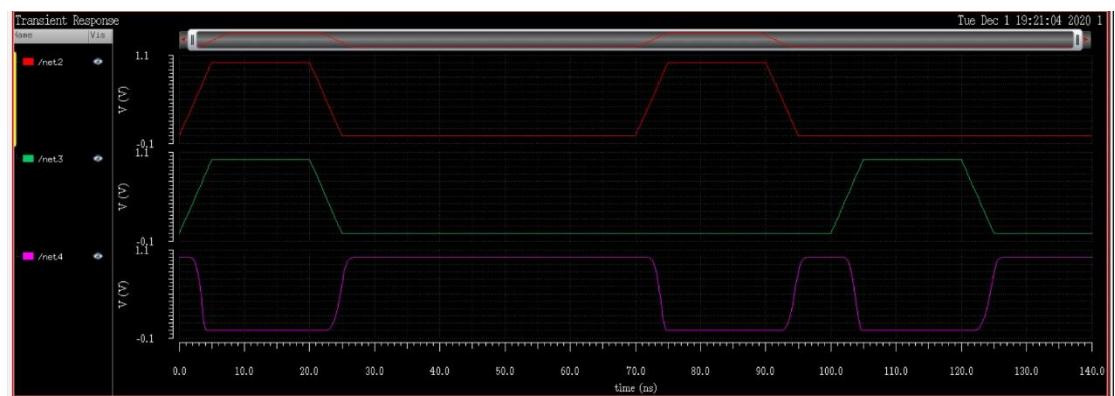
Total Propagation delay:  $t = (\text{Propagation delay low-high} + \text{Propagation delay high-low})/2 = 3.05811/2 = 1.529055\text{ns}$

**Εργασία για το σπίτι:**

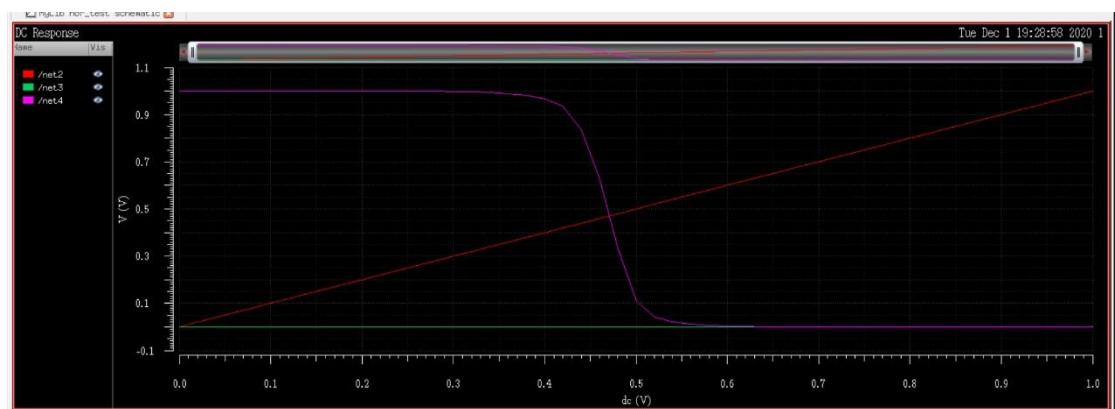
**NOR**



### Trans-Analysis:



### DC-Analysis:



- Rise-Fall time των εξόδων

Rise time: 1.96692ns

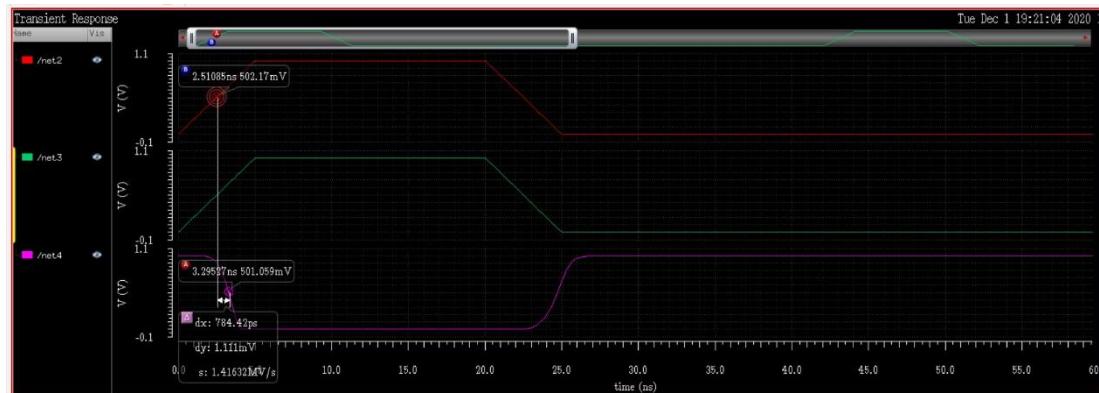


Fall time: 1.28145ns

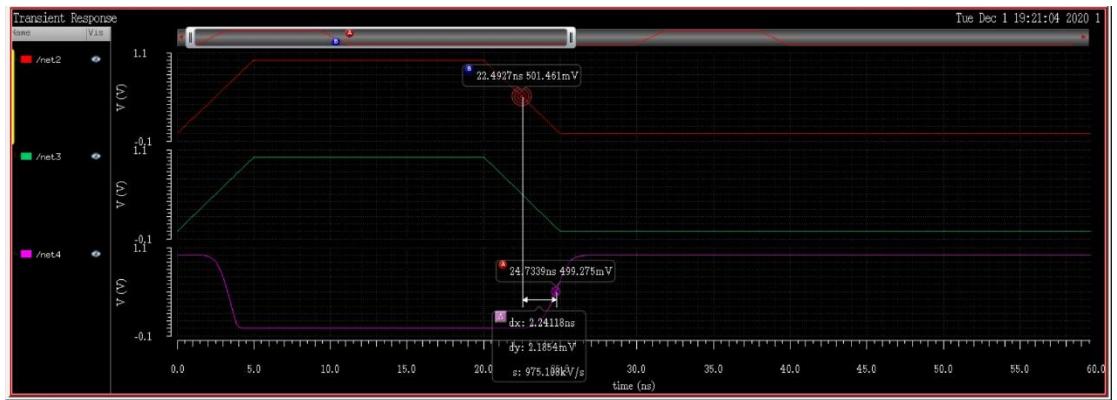


- Propagation delay των πυλών:

Propagation delay high-low: 784.42ps

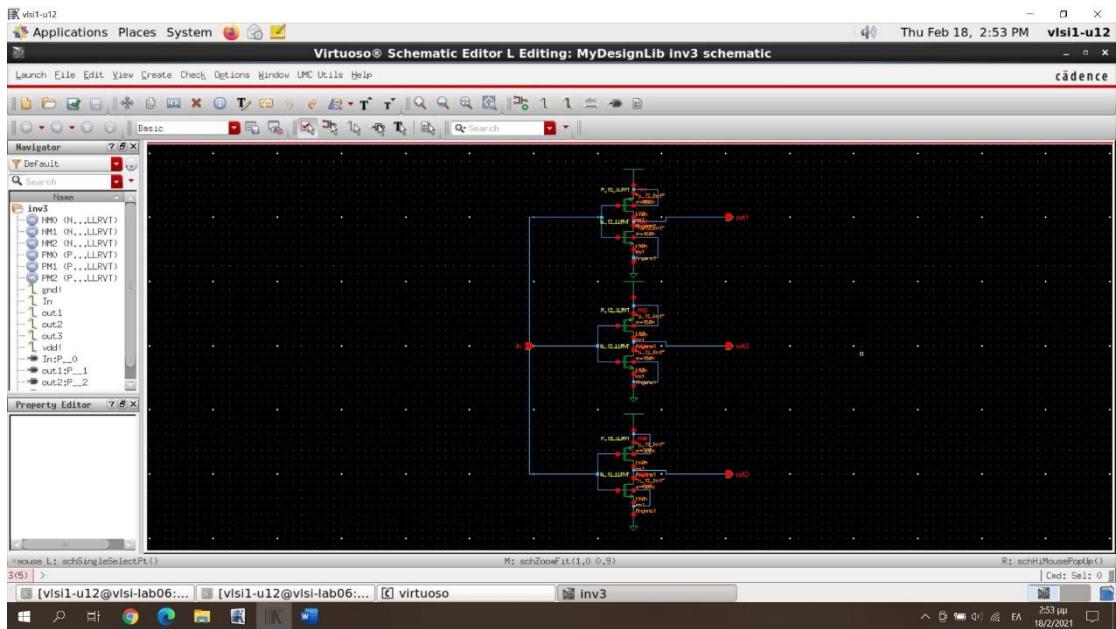


Propagation delay low- high: 2.24118ns



Total Propagation delay:  $t = (\text{Propagation delay low-high} + \text{Propagation delay high-low})/2 = 3.0256/2 = 1.5128\text{ns}$

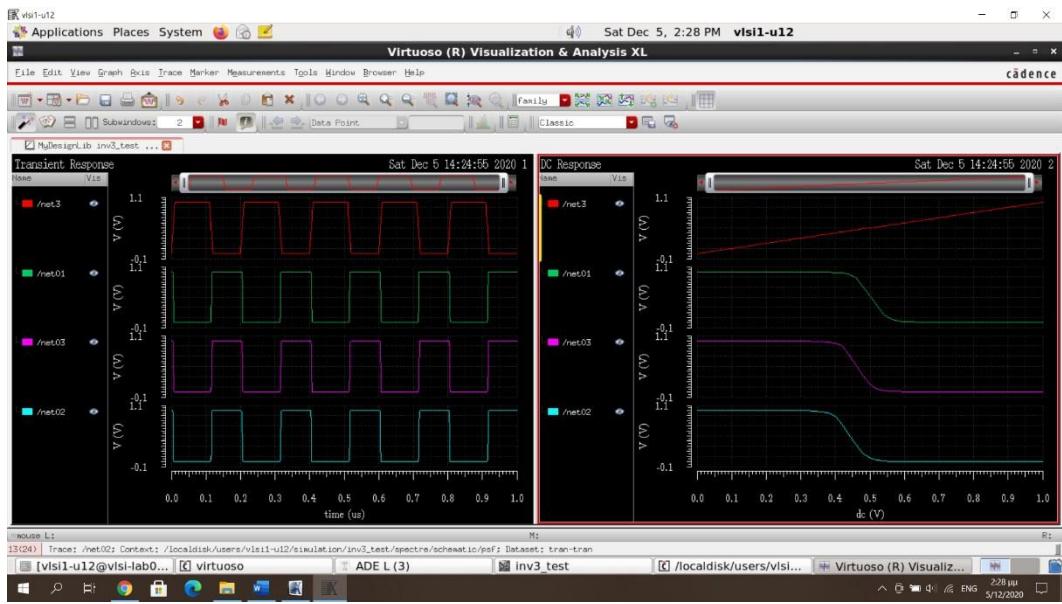
### Άσκηση 3



## Waveforms:

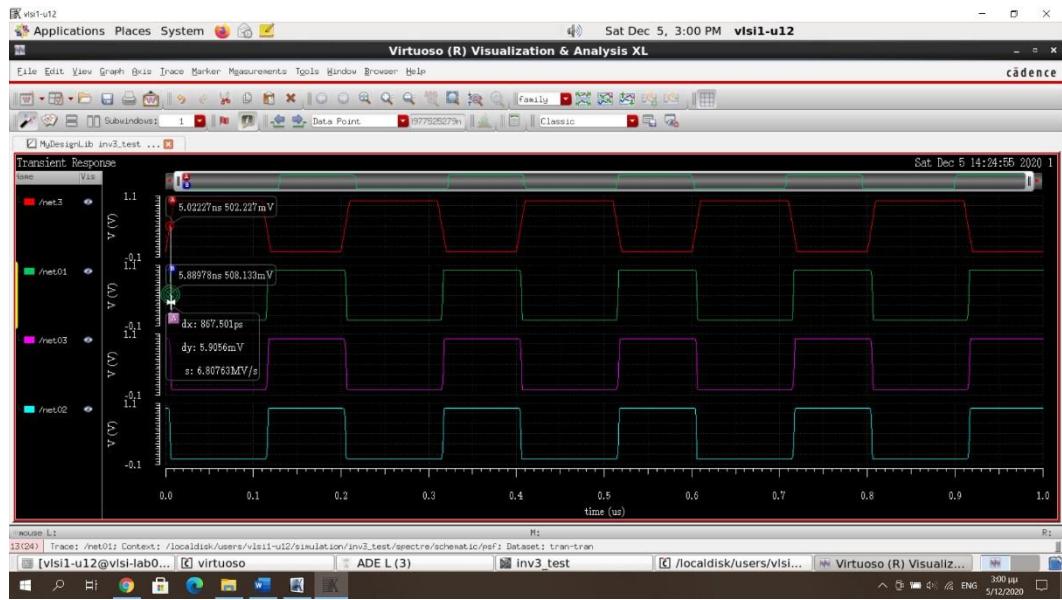


### Transient-DC analysis(10f):

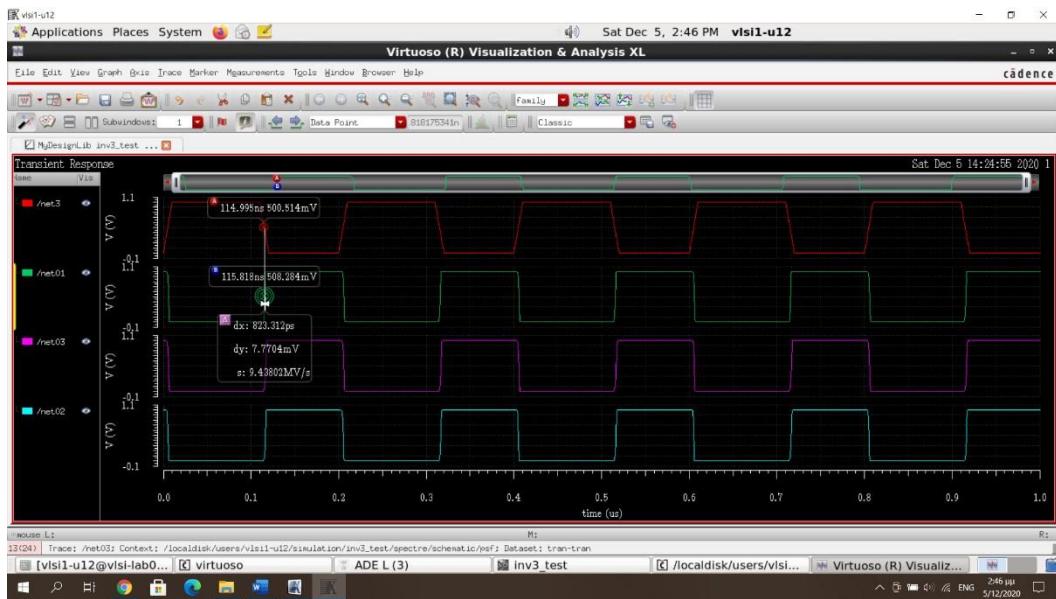


### Propagation delay (1rst inverter):

- 1->0 είναι 867.501ps



- 0->1 είναι 823.312ps



### Propagation delay (2nd inverter):

- 1->0 είναι 740.005ps

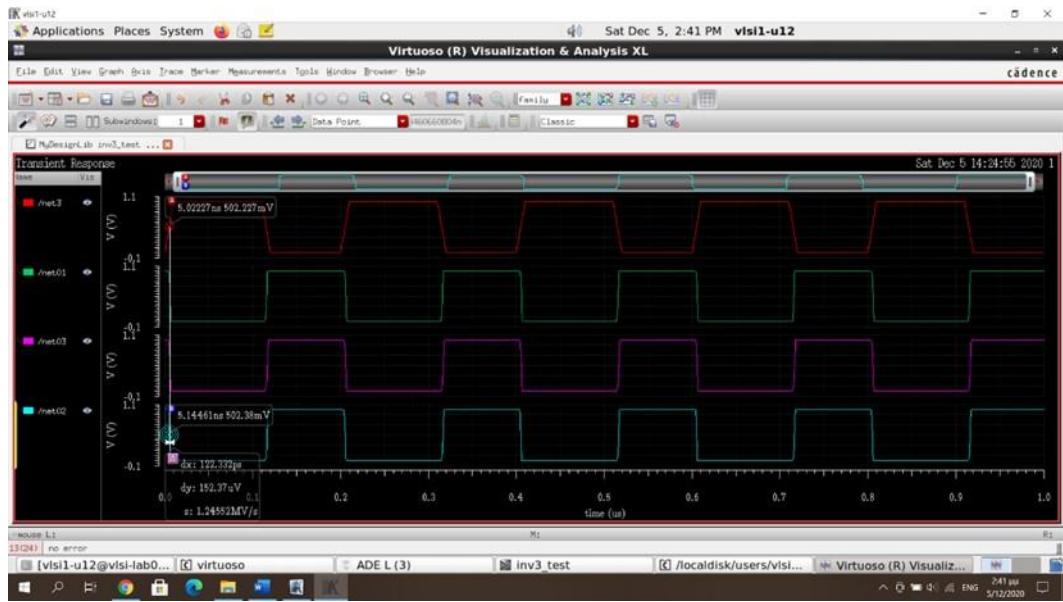


- 0->1 είναι 1.73218ns

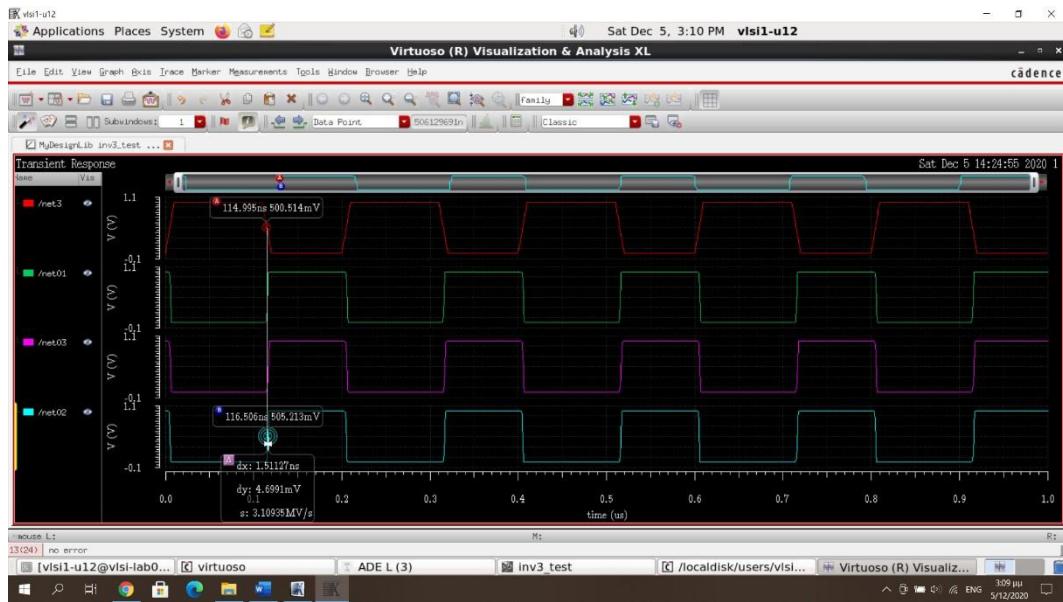


### Propagation delay (3rd inverter):

- 1->0 είναι 122.332ps



- $0 \rightarrow 1$  είναι  $1.51127\text{ns}$



### Rise-Fall time των εξόδων:

1rst inverter rise time: 1.59328ns



1rst inverter fall time: 1.64067ns



2nd inverter rise time: 1.98984ns



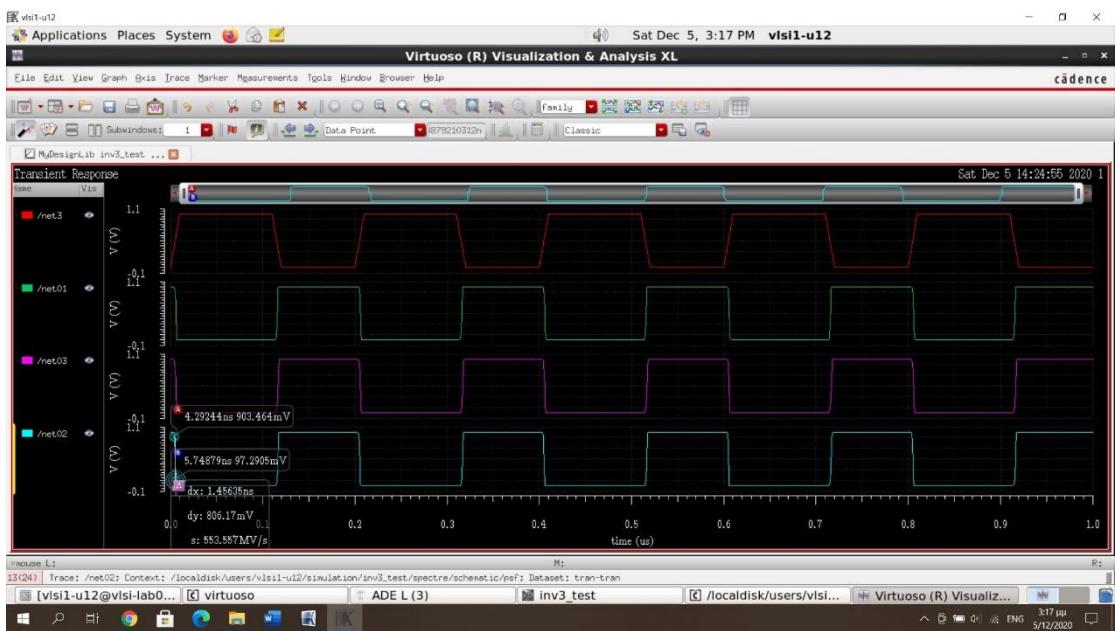
2nd inverter fall time: 1.76714ns



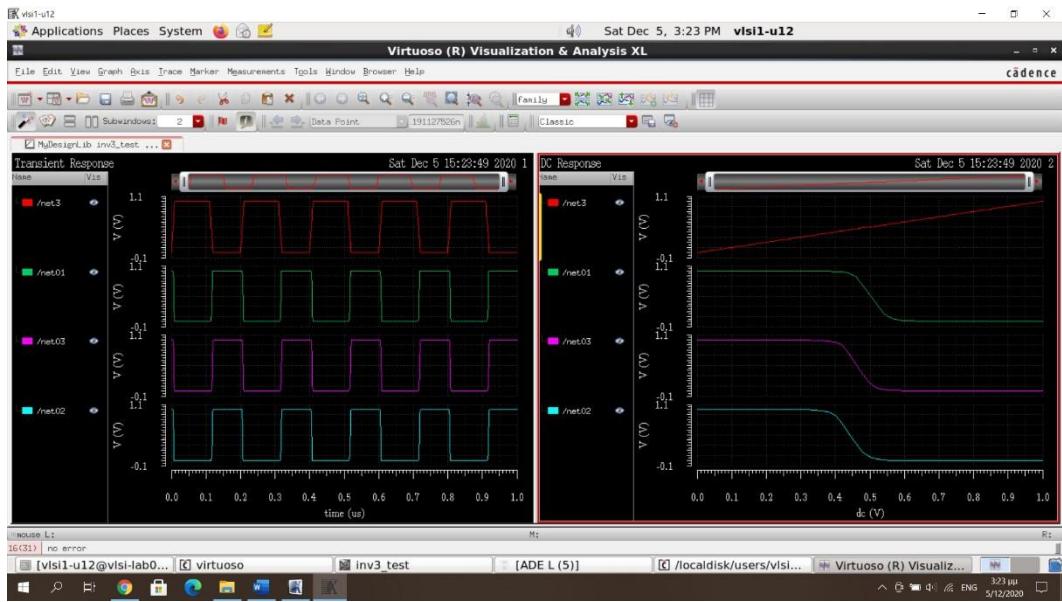
3rd inverter rise time: 1.69436ns



3rd inverter fall time: 1.45635ns

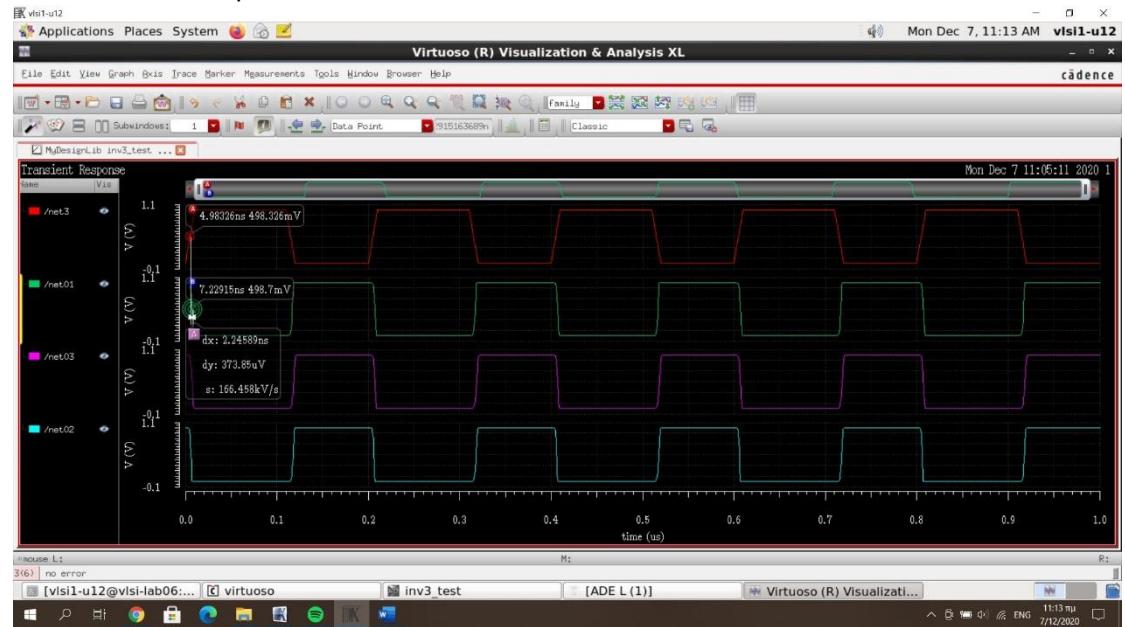


Transient-DC analysis(50f):



### Propagation delay (1rst inverter):

- 1->0 είναι 2.24589ps

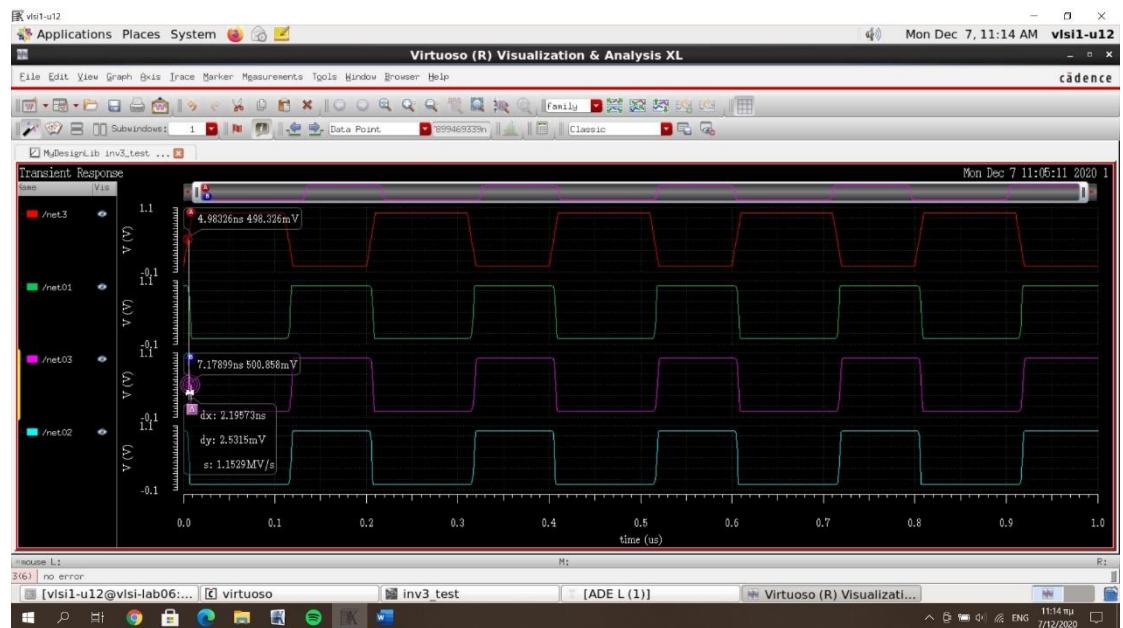


- 0->1 είναι 1.89978ns

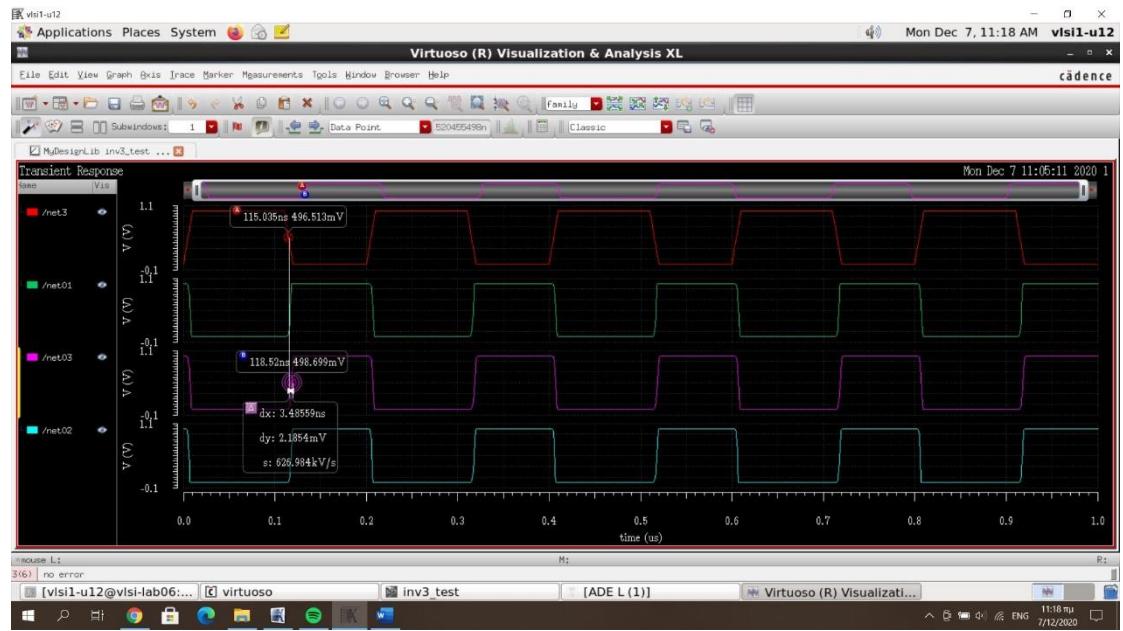


### Propagation delay (2nd inverter):

- 1->0 είναι 2.19573ns



- 0->1 είναι 3.48559ns



### Propagation delay (3rd inverter):

- 1->0 είναι 1.04229ns



- 0->1 είναι 2.87265ns



1rst inverter rise time: 2.35877ns



1rst inverter fall time: 2.8563ns



2nd inverter rise time: 3.50662ns



2nd inverter fall time: 2.86183ns



3rd inverter rise time: 2.89669ns

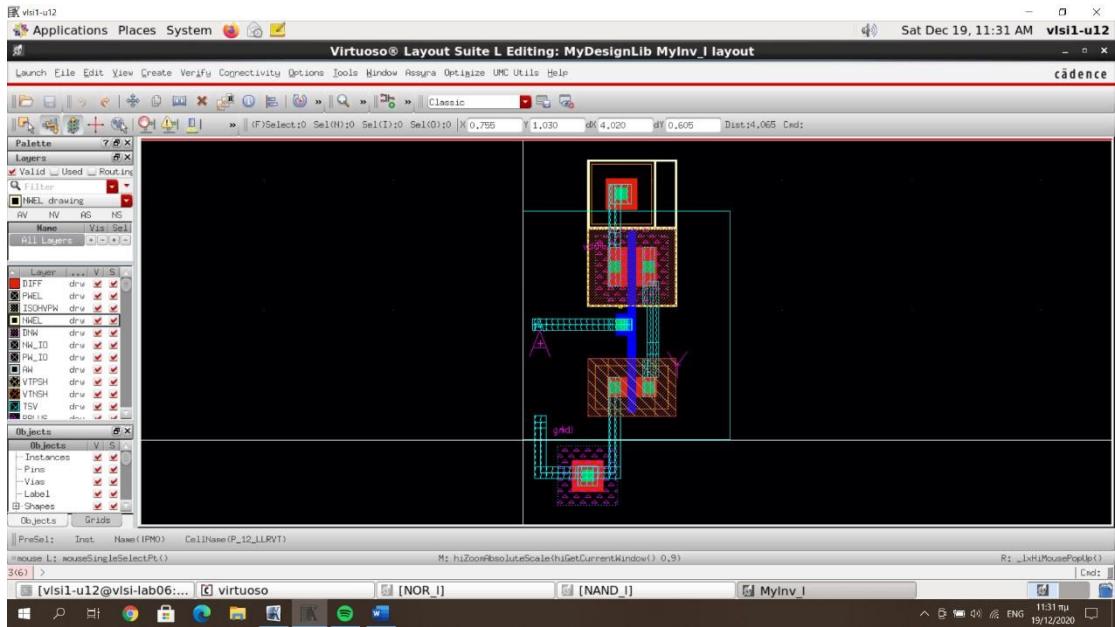


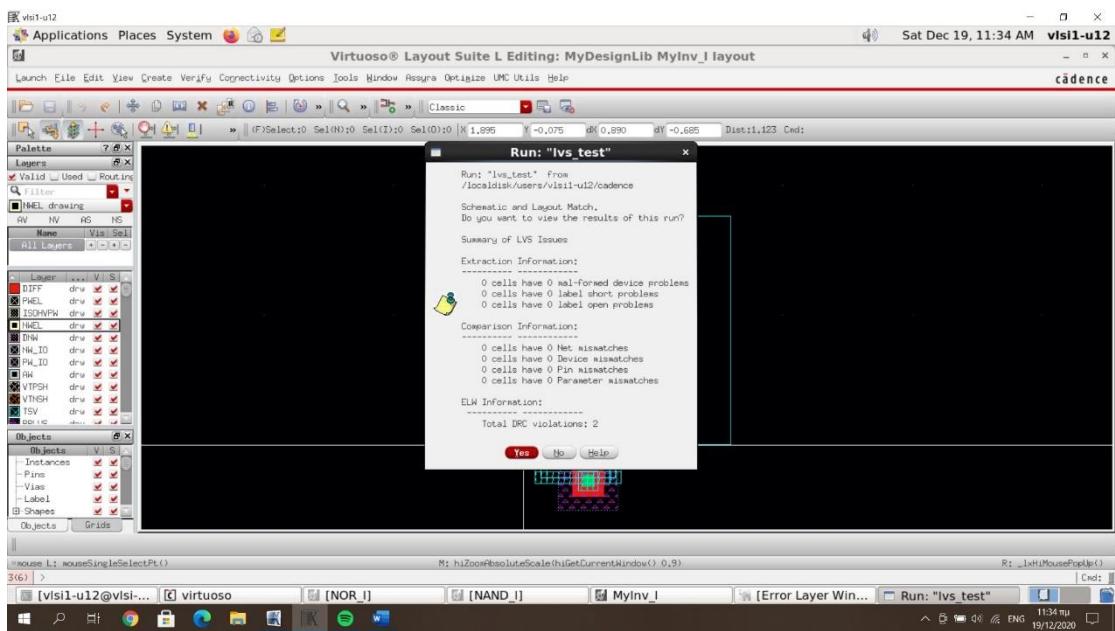
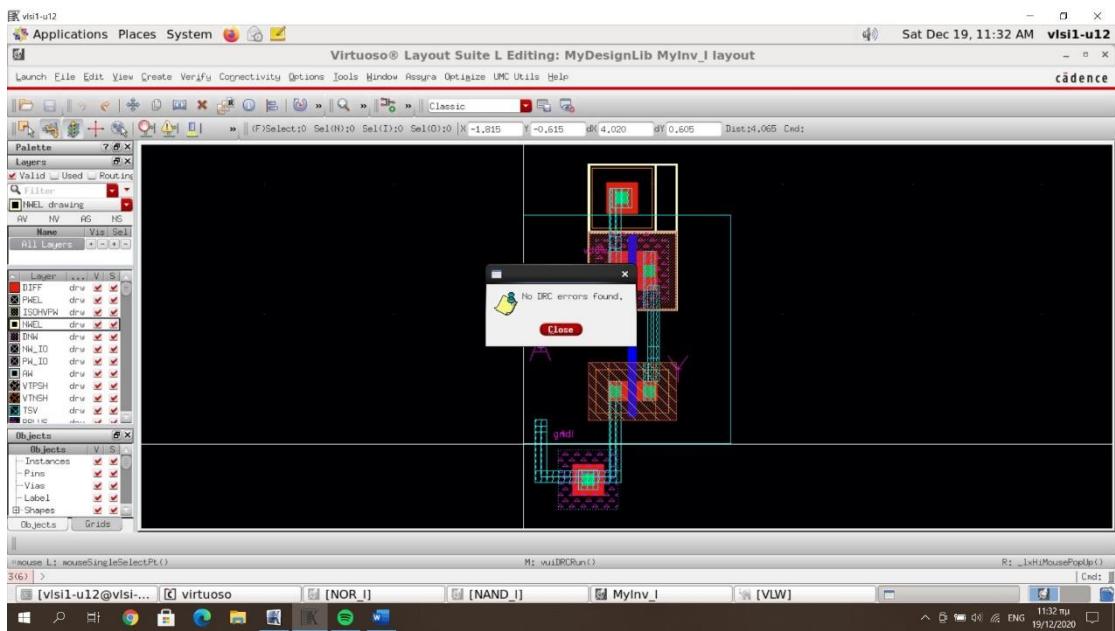
3rd inverter fall time: 2.01022ns



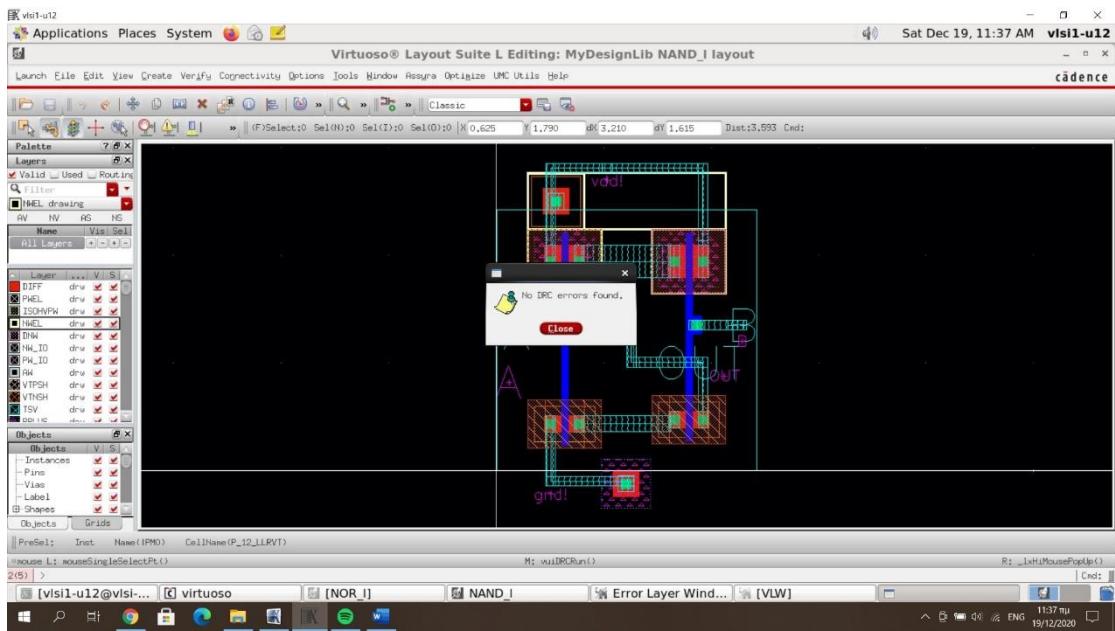
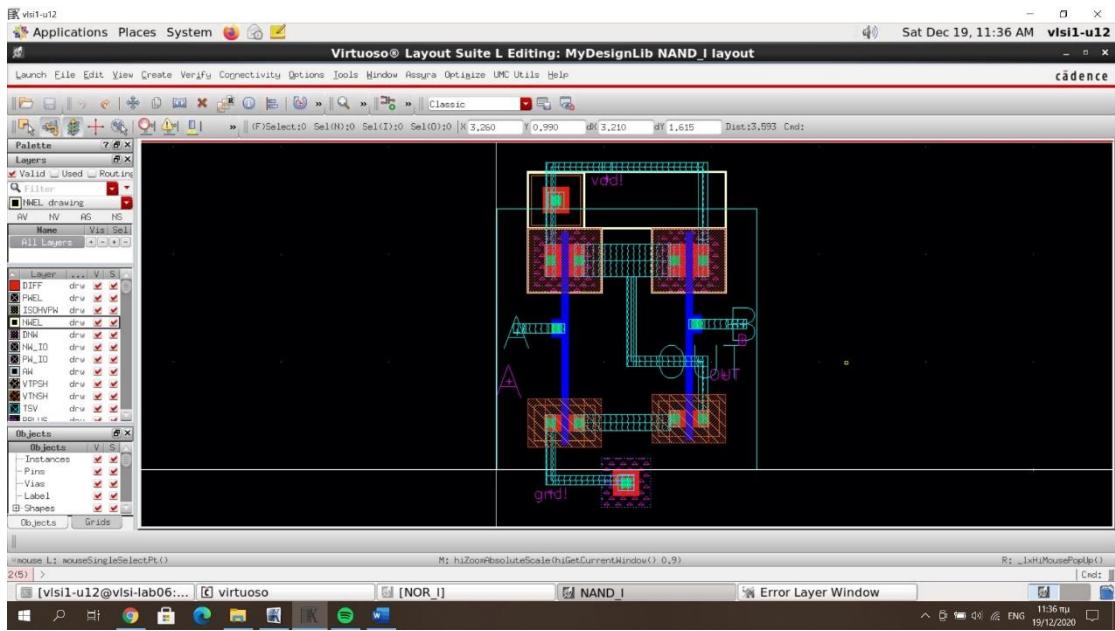
## Άσκηση 4

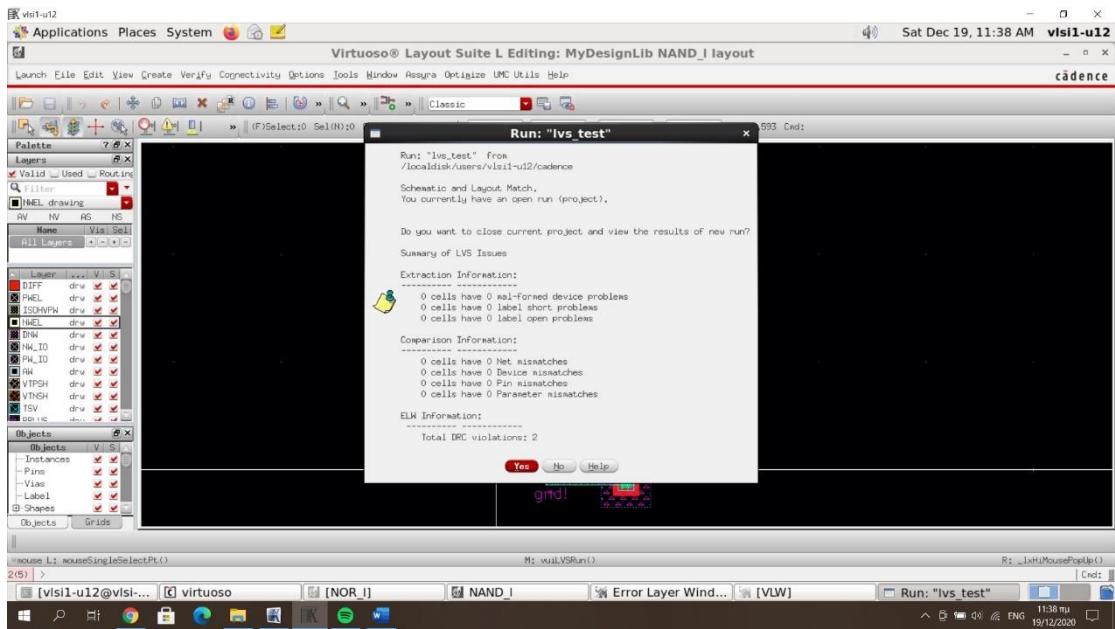
### Inverter 1 finger



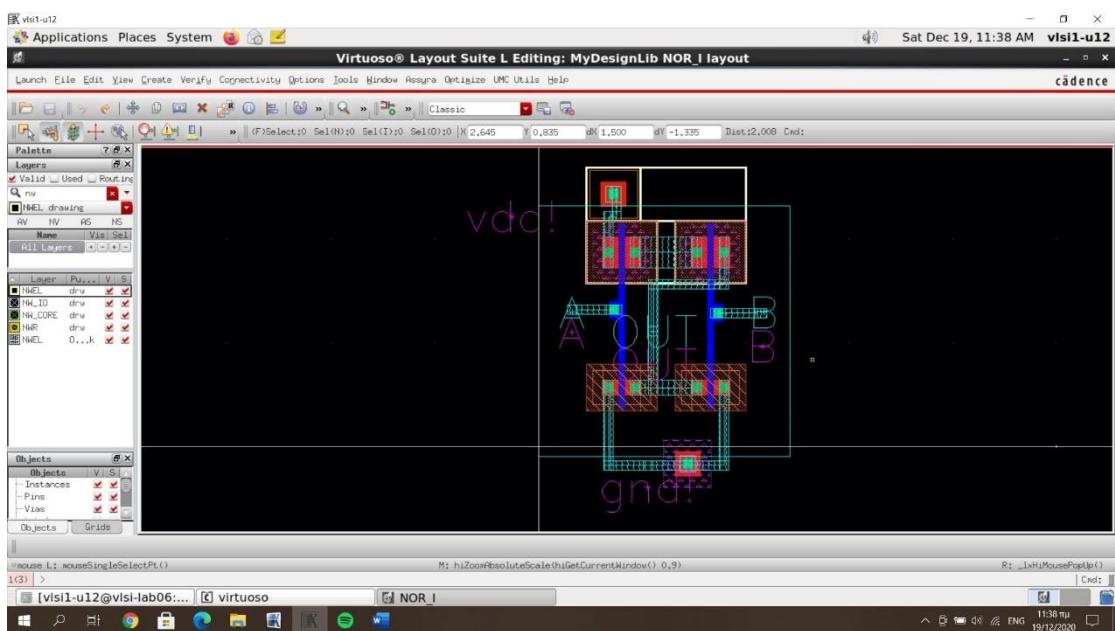


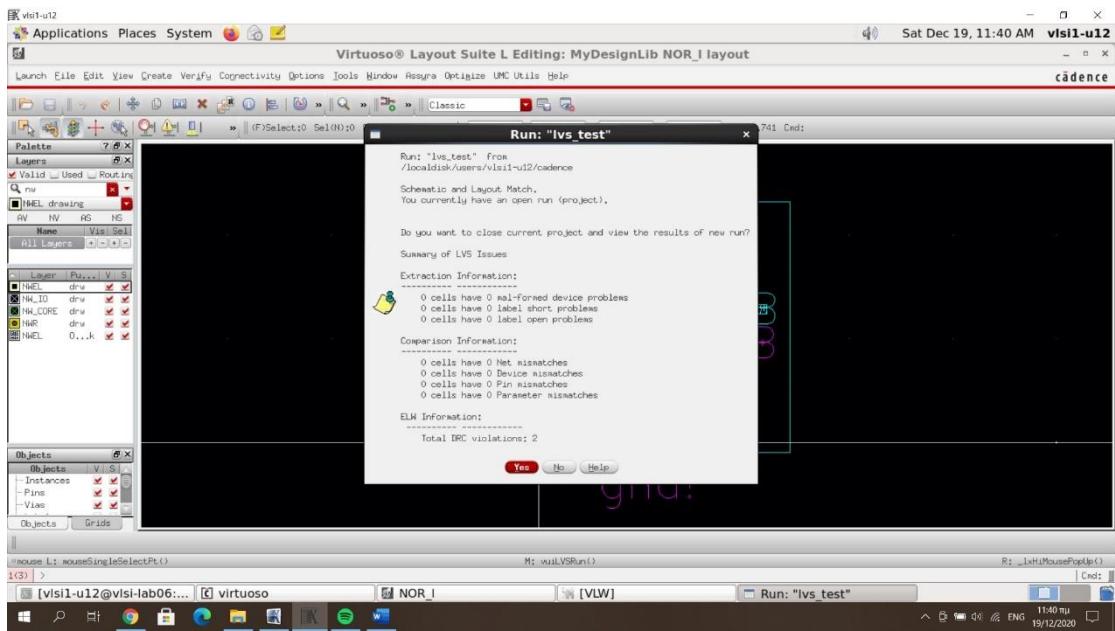
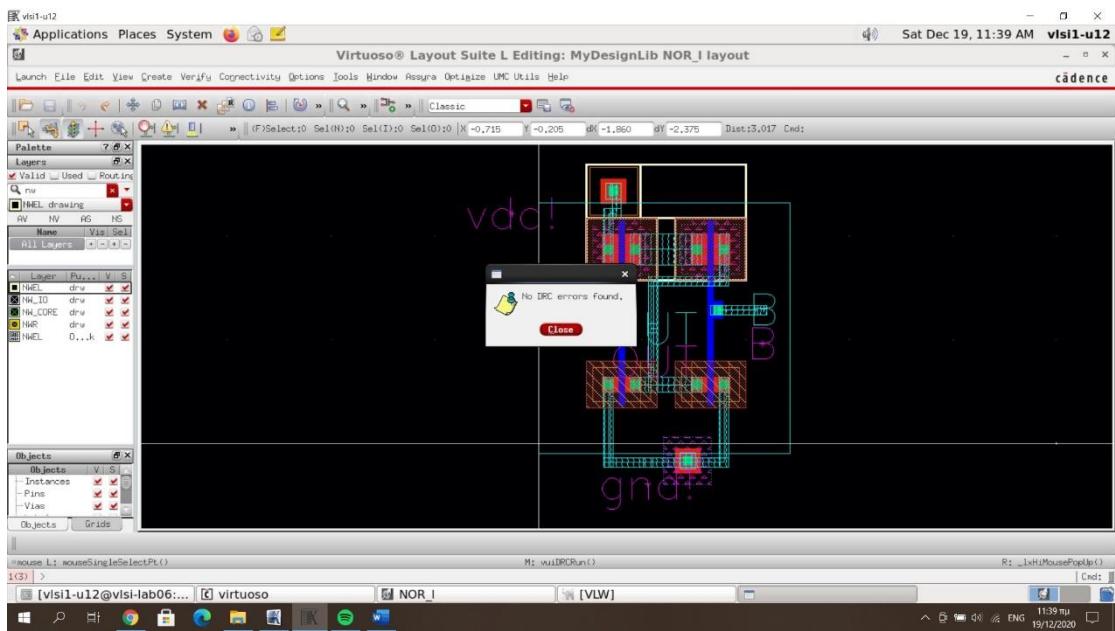
## NAND



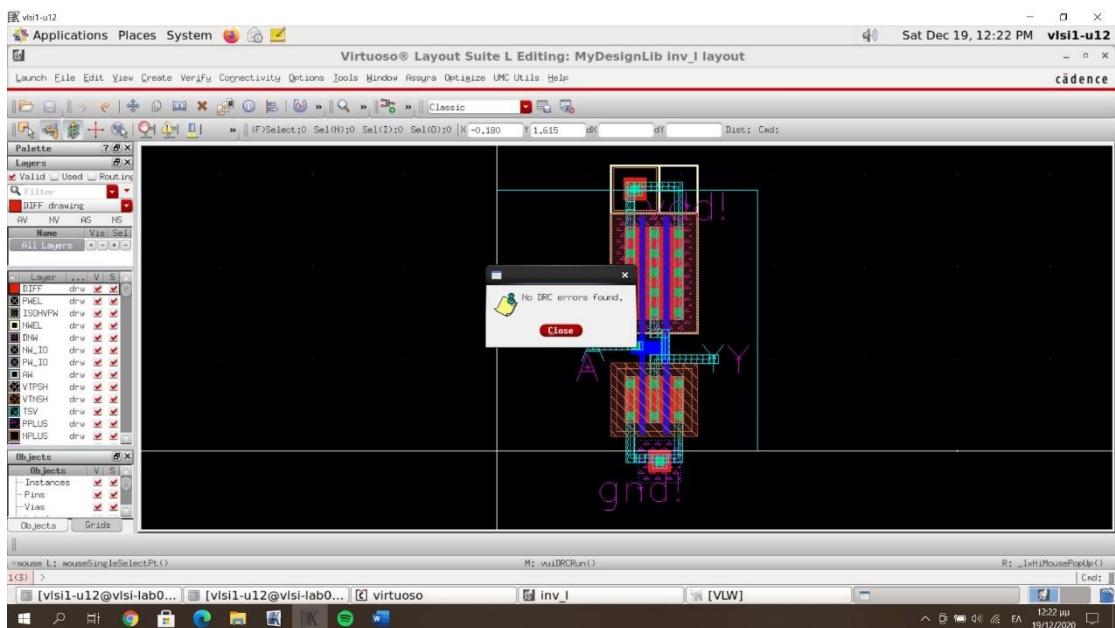
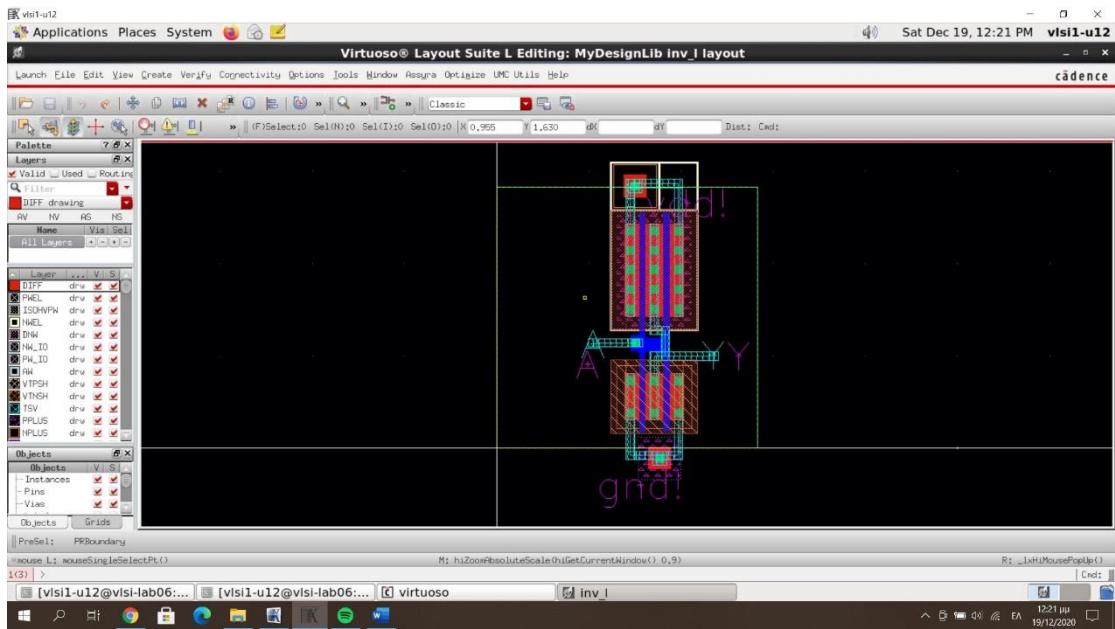


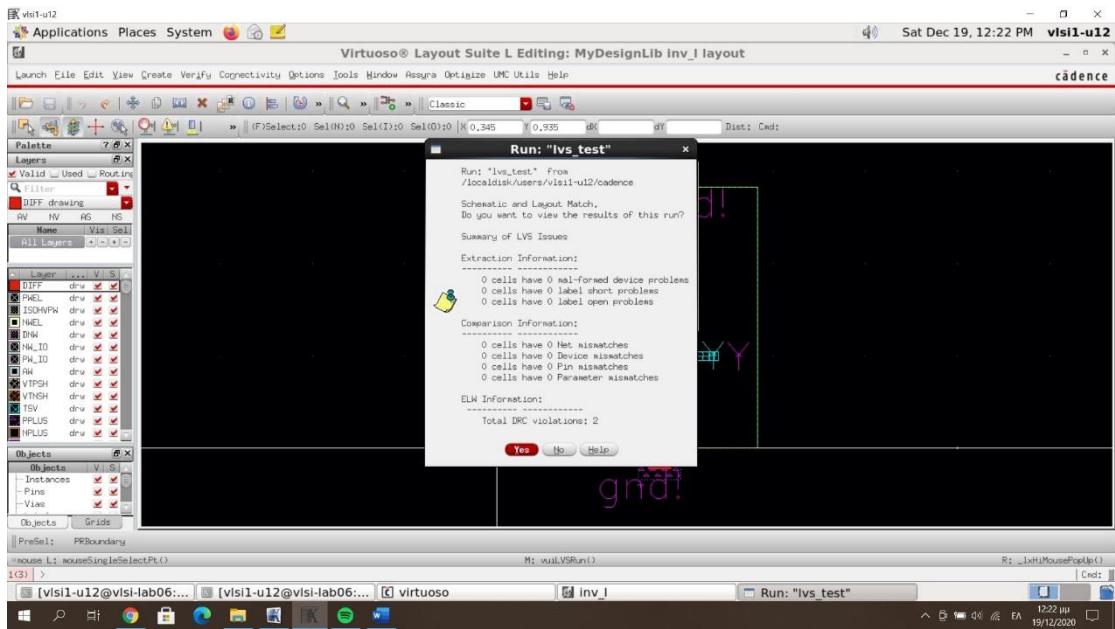
## NOR



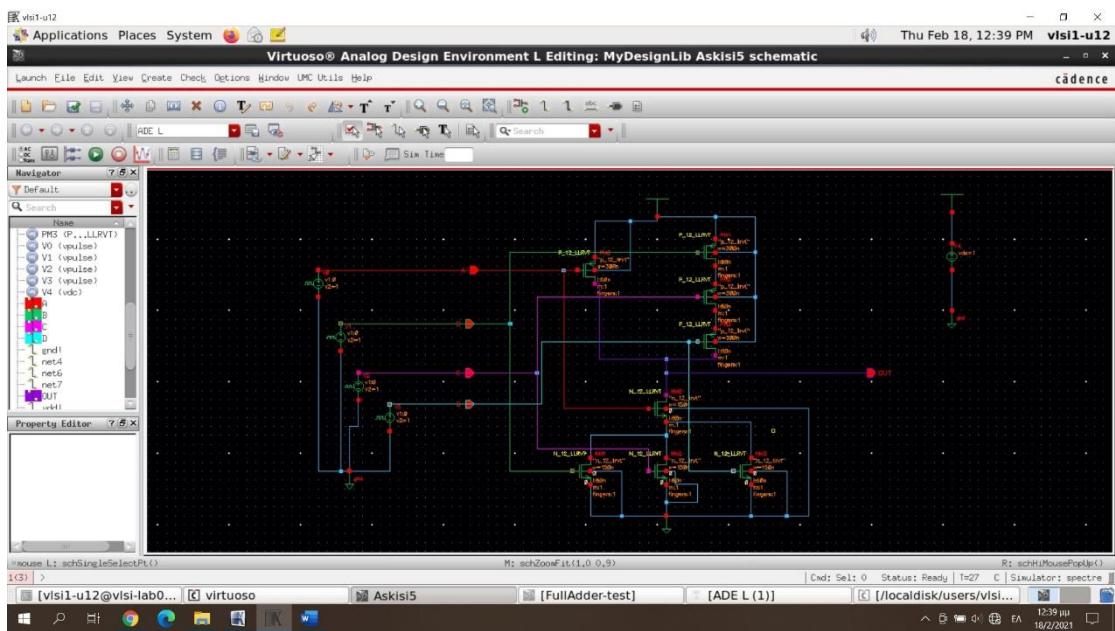


Inverter 2 fingers





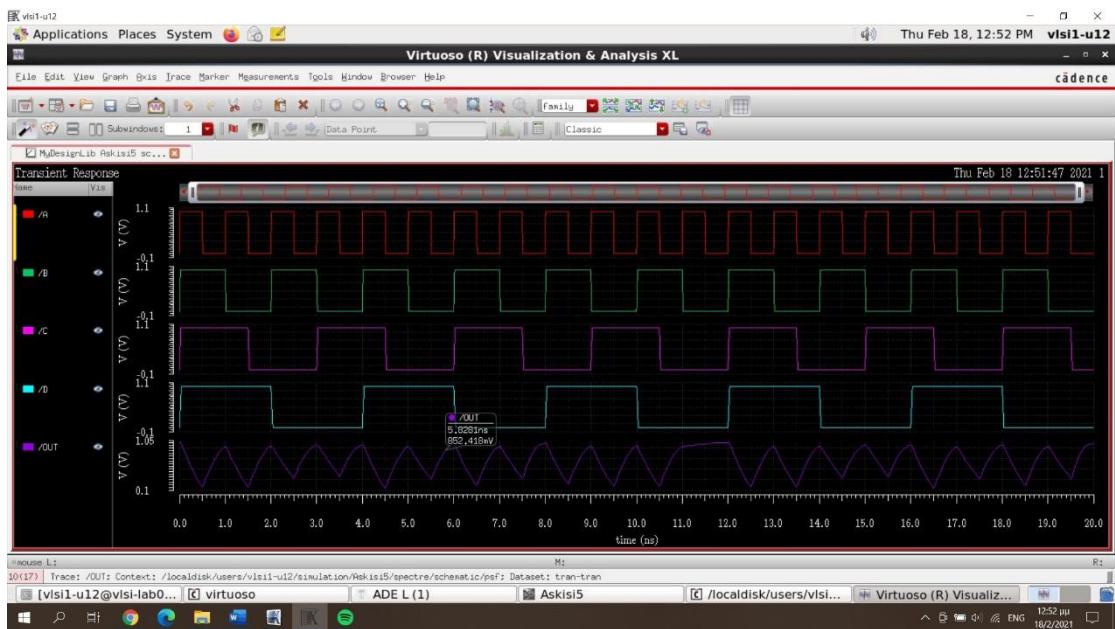
## Άσκηση 5



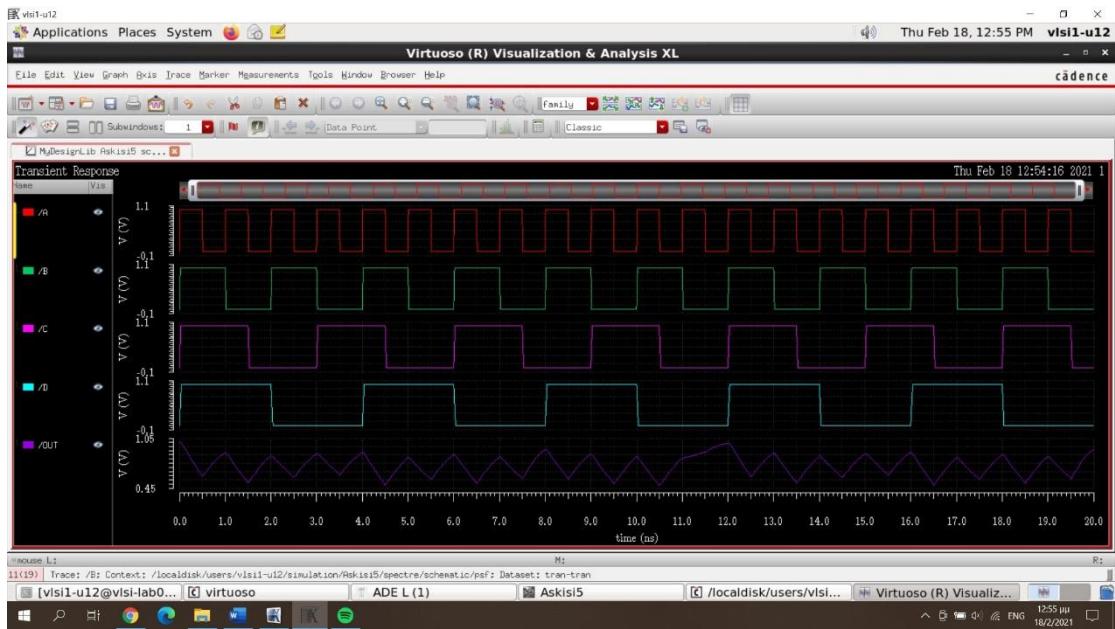
1)  $c=1 \text{ if } F$



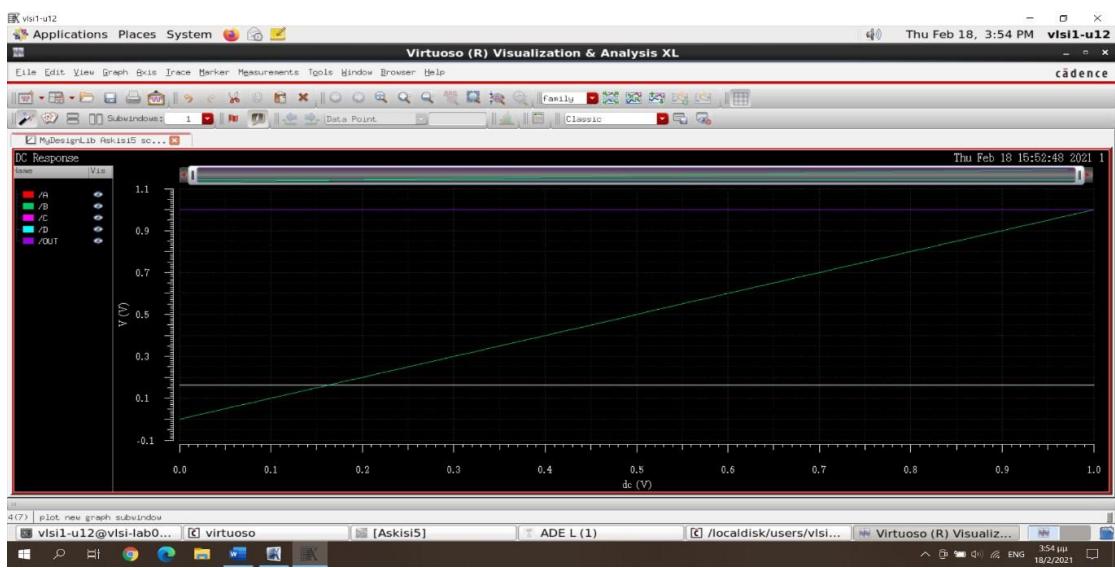
C=20f F



C=50f F



## 2) DC analysis(B)

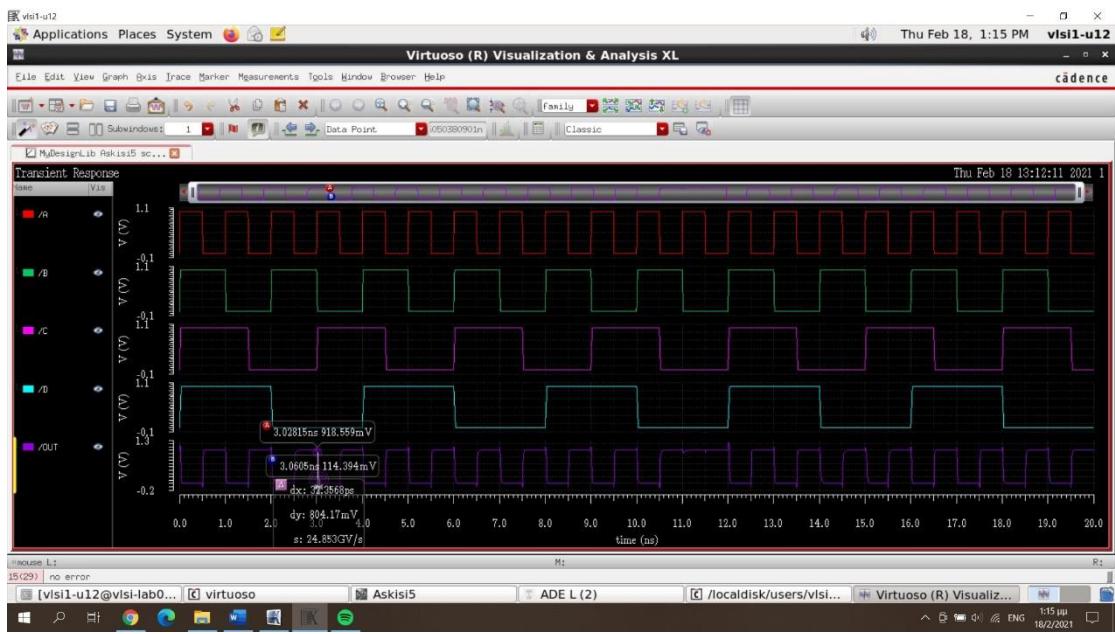


## Rise-Fall time των εξόδων

Rise Time: 12.819ps



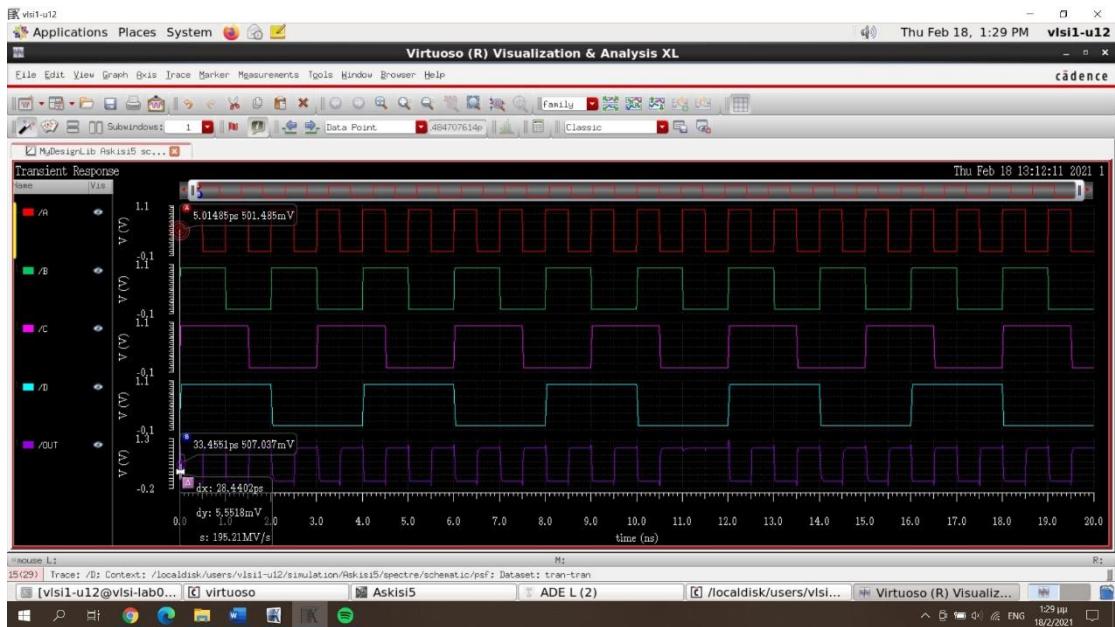
Fall Time: 32.3568ps



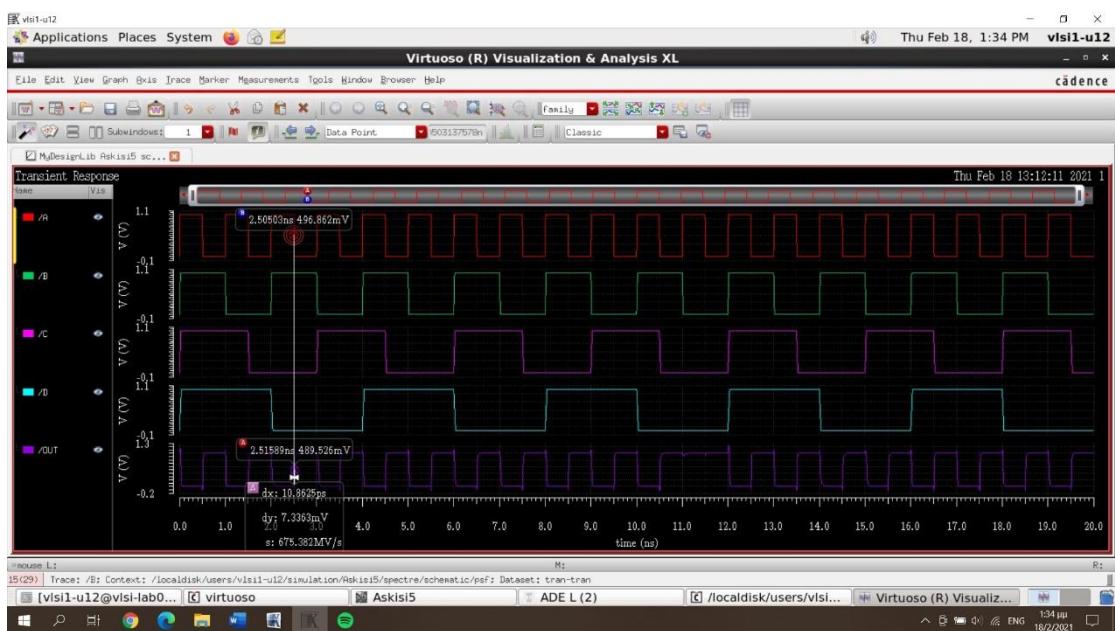
Propagation Delay:

A)

1->0: 28.4402ps



0->1: 10.8625ps

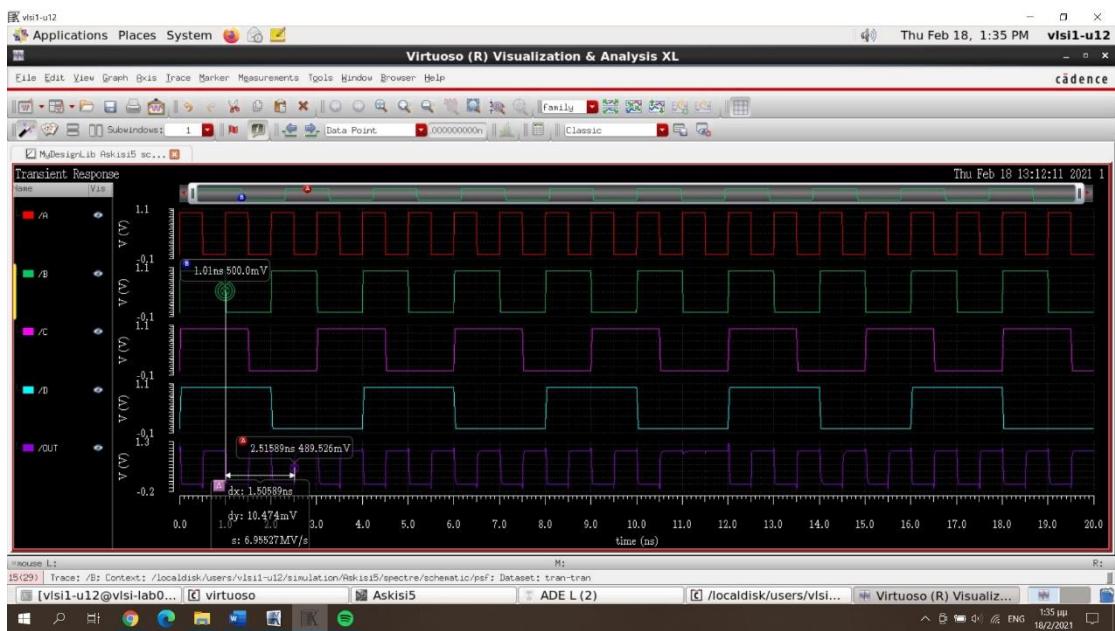


B)

1->0: 23.4551ps

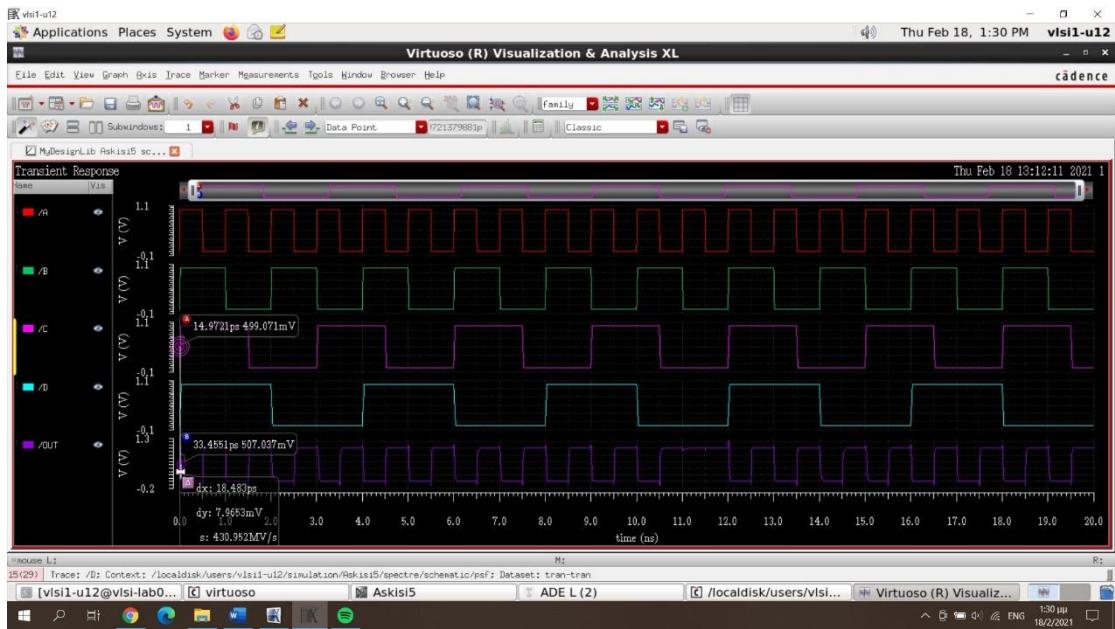


0->1: 1.50589ns

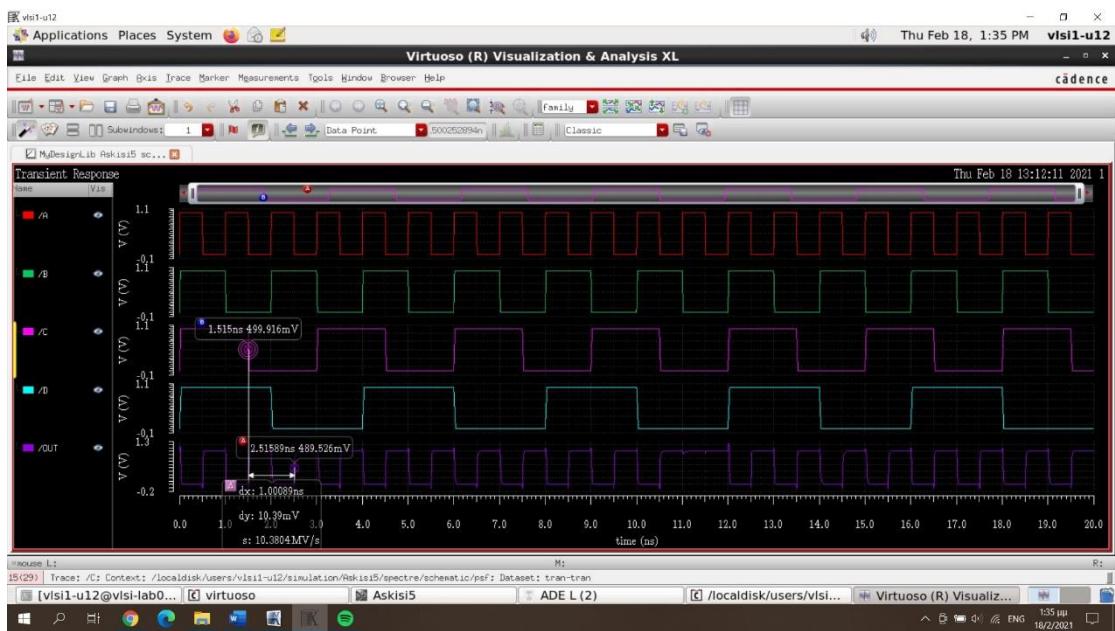


C)

1->0: 18.483ps



0->1: 1.00089ns



D)

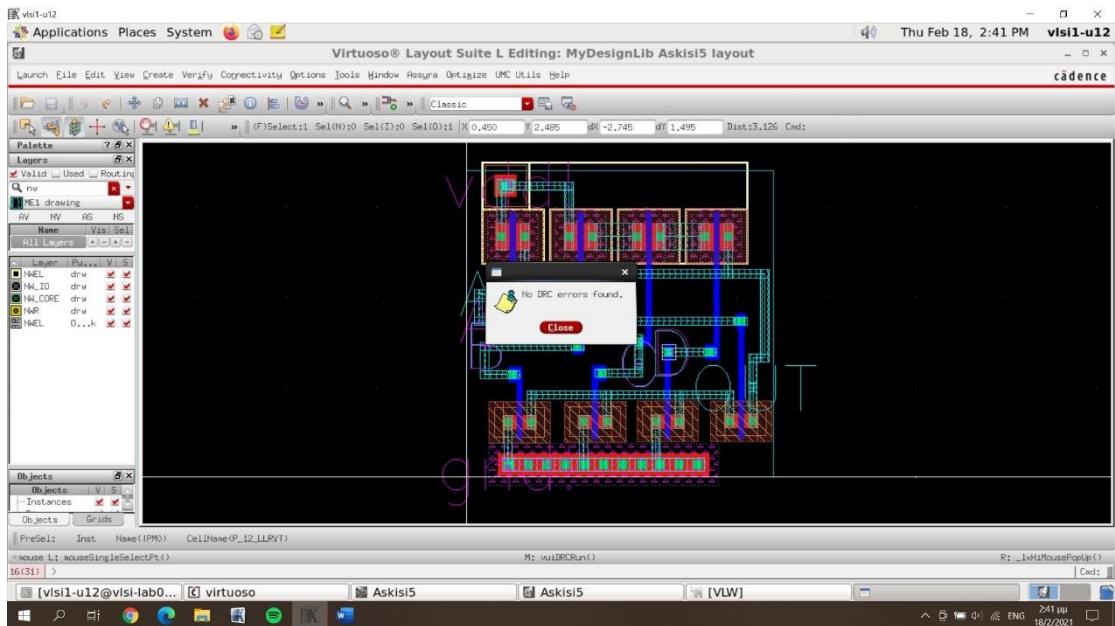
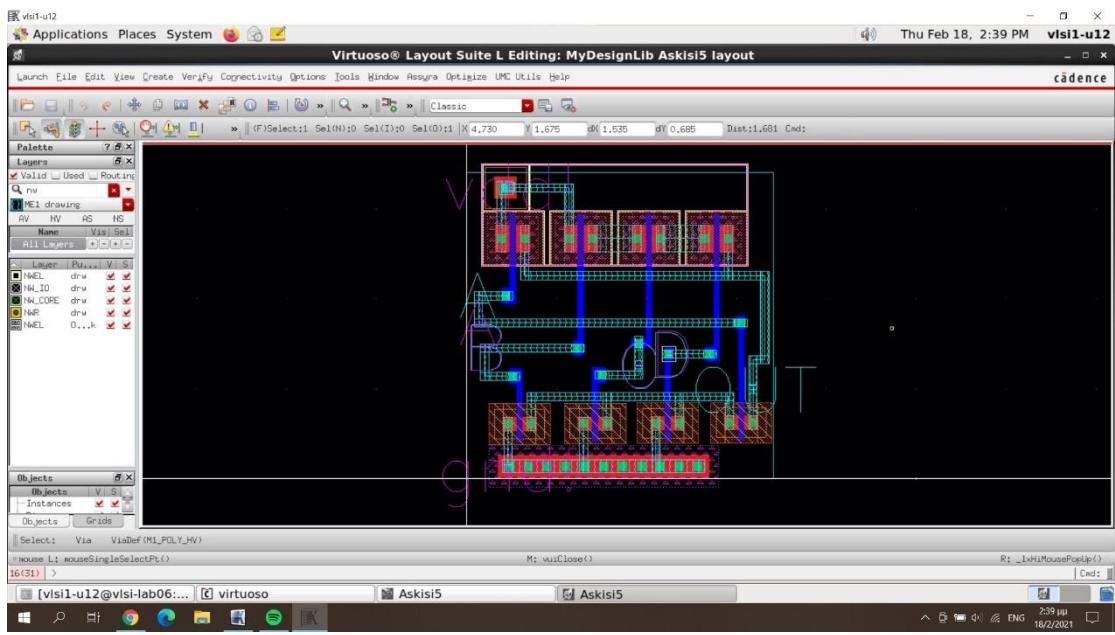
1->0: 13.4551ps

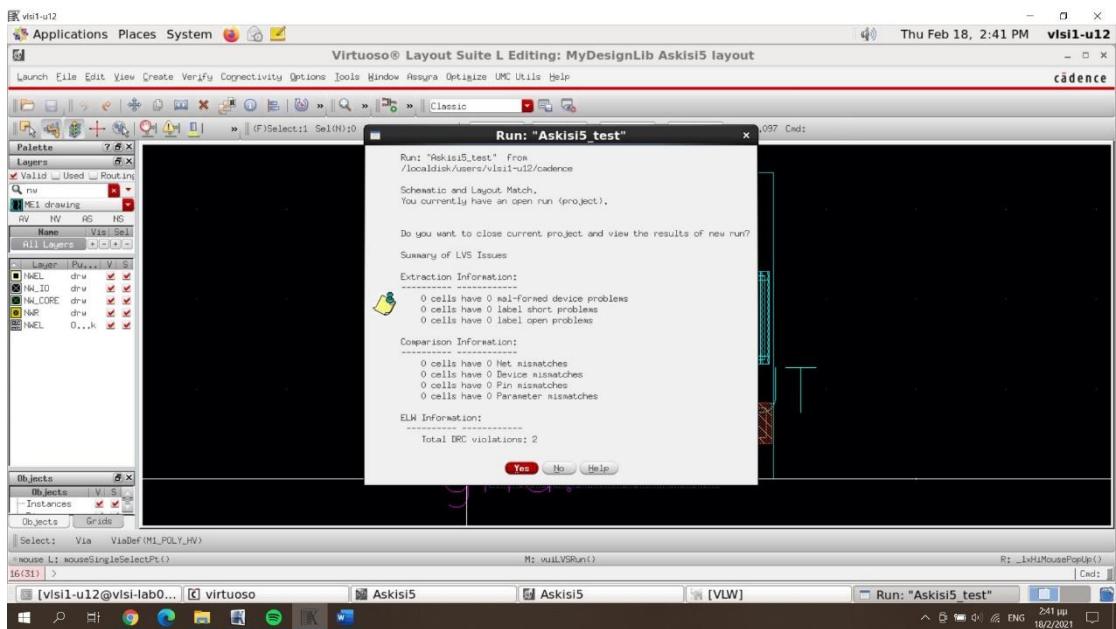


0->1: 495.894ps

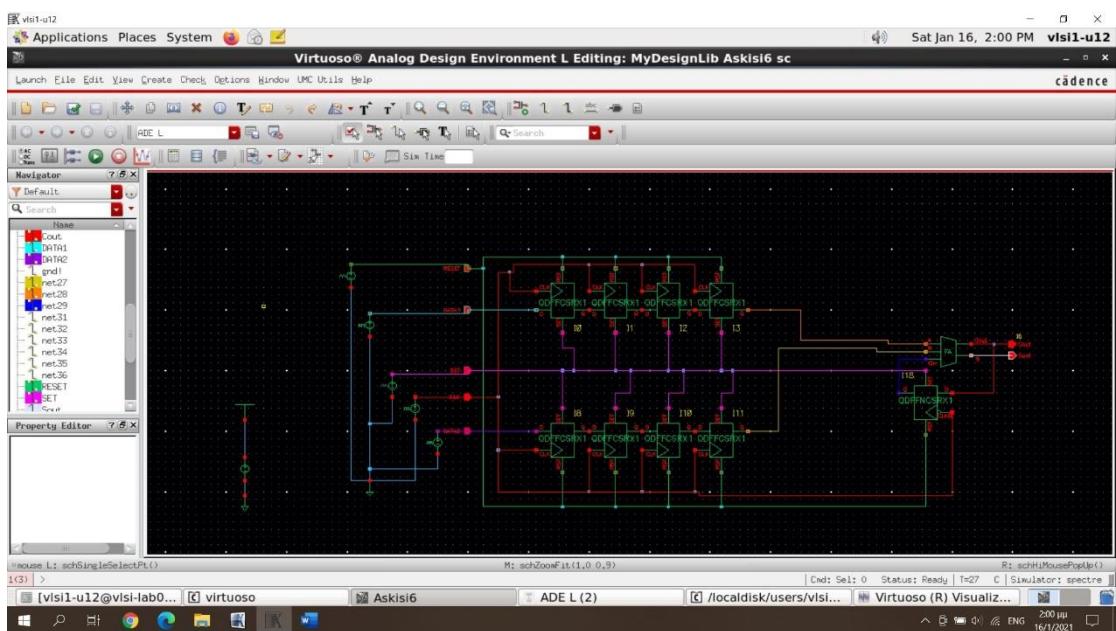


Layout:





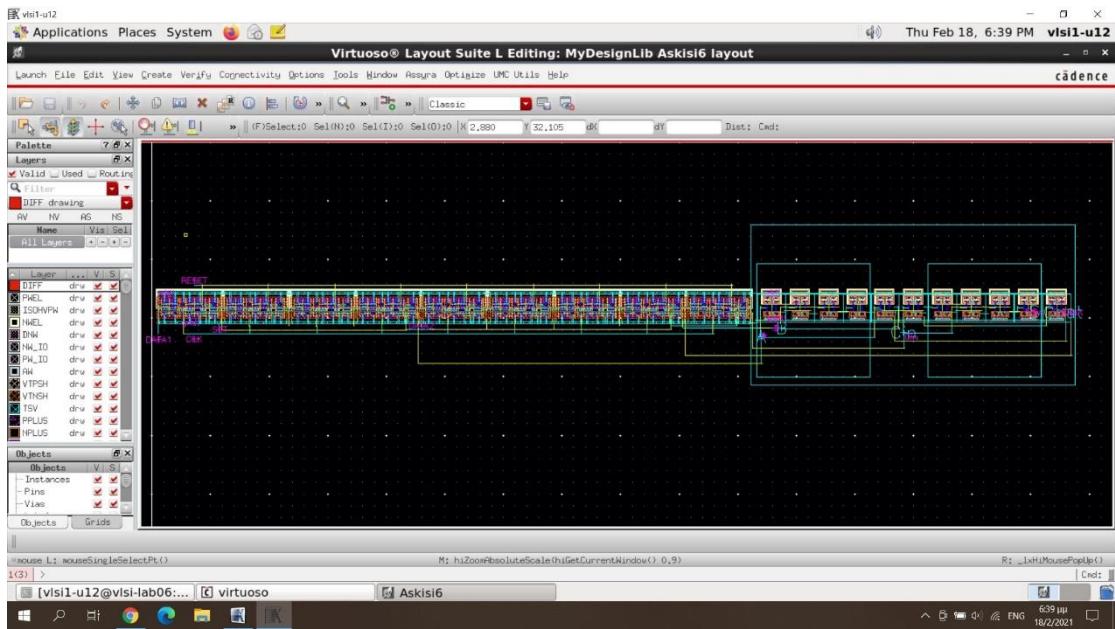
## Άσκηση 6





\*Ακόμα και με το αρνητικά ακμοπυροδότητο που μου σύστησαν οι συνάδελφοι στο τελευταίο μάθημα, πάλι έχω αυτή την πτώση στο Cin(μπλε) και στο Sout.

2)



Έχω φτιάξει το layout αλλά δεν με αφήνει να τρέξω το LVS. Μου βγάζει error ότι δεν μπορεί να χρησιμοποιήσει την άδεια για το σχηματικό και δεν μου ανοίγει επίσης κανένα σχηματικό.

vts1-u12

Applications Places System

Virtuoso® 6.1.6-64b - Log: /localdisk/users/vts1-u12/CDS.log

File Tools Options Help

```
Loading treeResistant.cxt
Loading soln.cxt
Load shared object file ./eda/cadence/2015-16/RHELx86/WSU90_04_14_124_ID51604/tools.lnx86/assura/lib/64bit/libavview.so
Version: 0(+)KIDS: libavview.so version av4.1Production:dF16,1,i=64b;ID6,1,i=64b,500,10 07/09/15 23:58 (g,jfn1944) *
Loading lo.cxt
Loading vb.cxt
Loading vba.cxt
Loading ol.cxt
Loading ast.cxt
Loading atv.cxt
Loading vca.cxt
Loading vca.cxt
+4444D0* LIB analogLib From File /localdisk/users/vts1-u12/cadence/cds.lib Line 2 redefines
LIB analogLib From File /localdisk/users/share/vts1/uuc_0511/Designkits/Cadence_6.1/cds.lib
Insert UNDEFINE analogLib
Delete DEFINE analogLib
in /localdisk/users/vts1-u12/cadence/cds.lib
Or remove or comment out DEFINE analogLib
in /localdisk/users/share/vts1/uuc_0511/Designkits/Cadence_6.1/cds.lib
+4444D0* LIB basic From File /localdisk/users/vts1-u12/cadence/cds.lib Line 4 redefines
LIB basic From File /localdisk/users/share/vts1/uuc_0511/Designkits/Cadence_6.1/cds.lib
Insert UNDEFINE basic
before
in /localdisk/users/vts1-u12/cadence/cds.lib
Or remove or comment out DEFINE basic
in /localdisk/users/share/vts1/uuc_0511/Designkits/Cadence_6.1/cds.lib
to suppress this warning message
+4444D0* The directory '/localdisk/users/vts1-u12/cadence/MuDesignLibrary' does not exist.
but was defined in libfile '/localdisk/users/vts1-u12/cadence/cds.lib' For Lib 'MuDesignLibrary'.
+4444D0* The directory '/localdisk/users/vts1-u12/cadence/MuDesignLib' does not exist.
but was defined in libfile '/localdisk/users/vts1-u12/cadence/cds.lib' For Lib 'MuDesignLib'.
+4444D0* (icLie-21) License Virtuoso_Schematic_Editor_JL ('95100') is not available to run Schematics L.
Trying to check out the license Virtuoso_Schematic_Editor_JL ('95115') instead.
+4444D0* (icLie-3) Could not get license Virtuoso_Schematic_Editor_JL
+4444D0* (icLie-22) License Virtuoso_Schematic_Editor_JL ('95115') is not available to run Schematics L.
(DEMGE-100019); (deLicense-5) Could not get the license for Schematics. Open aborted.
```

mouse L:

1 | > [vts1-u12@vts1-lab06: ~] [ virtuoso ]

Windows Taskbar: File Explorer, Edge, File Manager, Start, Task View, Taskbar settings, Date/Time (18/2/2021), Resolution (641 ppi)

