



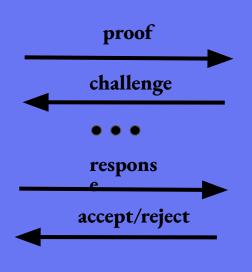
Circle STARK GPU Acceleration

An Analysis of Performance and Implementation



Proof Systems

Prover



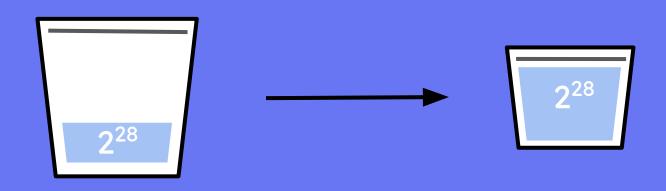
Verifier

ZK-STARK

- Zero-Knowledge
- Scalable
- Transparent
- Argument
- of Knowledge



A Matter of Effice en Etypf Unused Space!



2²⁵⁶ ?

A Matter of Efficiency

- > STARK field prime : p = 2²⁵¹ + 17 * 2¹⁹² + 1
- ▶ Goldilocks prime: p = 2⁶⁴ 2³² + 1
- Babybear prime: p = 15 * 2²⁷ + 1
- **Mersenne 31 Prime:** $p = 2^{31} 1$



Why the Circle?

- Map the field ontocoordinates of the circle
- Circle gives us the extra point for FFT



A Matter of Efficiency

- Mersenne 31 is very efficient on 32-bit architecture
- The Circle enables FFTs
- 3 1.4x performance increase over Babybear



GPU parallelization

GPUs can handle many simultaneous calculations.

- Data-intensive computations
- Algebraic operations
- Image or signal processing



GPU problems

The GPU and CPU use separate memory spaces

One cannot access the other's memory



Copying data from one to the other is expensive

GPU problems

Memory accessing is not trivial

- GPU threads are grouped in blocks
- Blocks cannot access each other's *shared* memory either



GPU benefits

When we launch threads to process our data

- Threads will run concurrently
- The GPU will handle as many threads in parallel as it can.

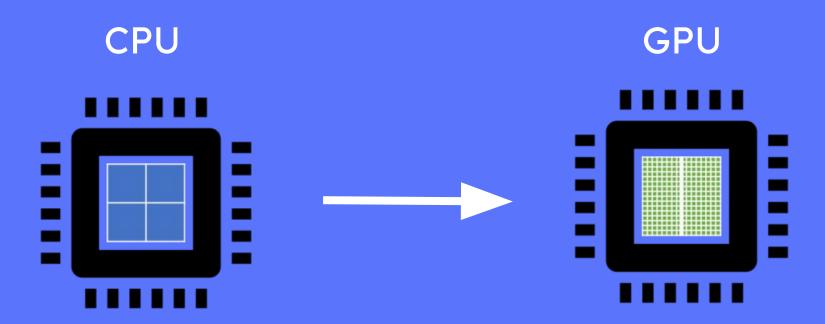


GPU benefits

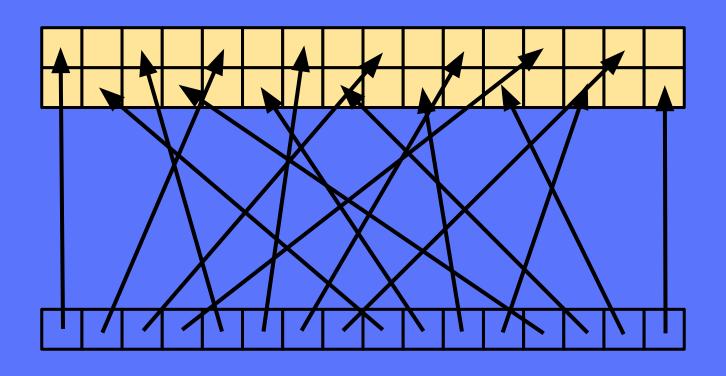
There are a lot of architecture-specific features.

- Blocks and warps
- Memory banks, global memory, shared memory
- Consecutive memory access operations
- 4 Shared registers

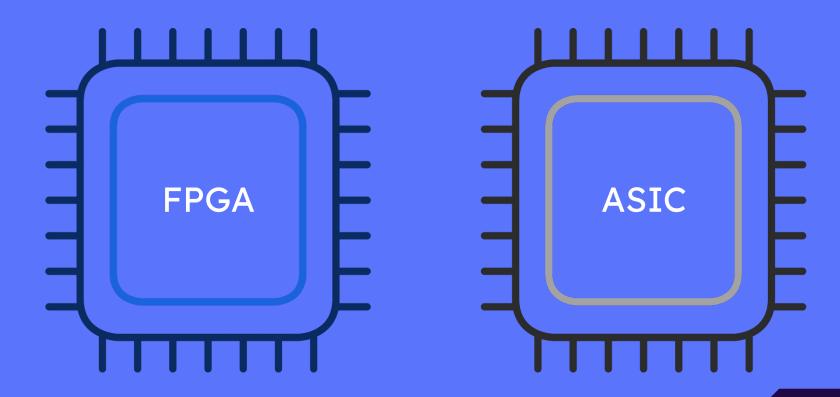
GPU Data Transfer



GPU Memory Access



Other Hardware





on Sequential algorithm

02. Parallel algorithm

os. Comparison

Batch inverse

It's a Stwo component we'll parallelize.

Its purpose is to calculate the multiplicative inverse in the field for a batch of numbers.



Sequential Well first review the sequential implementation.

Since field inversion is an expensive operation (extended euclidean algorithm), we use something called Montgomery's trick.

$$a_1,a_2,a_3,a_4\in F_p$$

$$eta_1 = a_1 \ eta_2 = a_1 imes a_2 \ eta_3 = a_1 imes a_2 imes a_3 \ eta_4 = a_1 imes a_2 imes a_3 imes a_4$$

$$eta_1=a_1 \ eta_2=eta_1 imes a_2 \ eta_3=eta_2 imes a_3 \ eta_4=eta_3 imes a_4$$

$$eta_4^{-1} \longleftarrow eea(eta_4)$$

*Intuitively

$$egin{aligned} a_4^{-1}&=eta_4^{-1} imeseta_3\ &=rac{1}{a_1 imes a_2 imes a_3 imes a_4} imes a_1 imes a_2 imes a_3\ &=rac{1}{a_4} \end{aligned}$$

*Intuitively

$$eta_3^{-1} = eta_4^{-1} imes a_4 \ = rac{1}{a_1 imes a_2 imes a_3 imes a_4} imes a_4 \ = rac{1}{a_1 imes a_2 imes a_3 imes a_4}$$

$$a_4^{-1} = eta_4^{-1} imes eta_3 \quad a_2^{-1} = eta_2^{-1} imes eta_1 \ eta_3^{-1} = eta_4^{-1} imes a_4 \quad eta_1^{-1} = eta_2^{-1} imes a_2 \ a_3^{-1} = eta_3^{-1} imes eta_2 \quad a_1^{-1} = eta_1^{-1} \ eta_2^{-1} = eta_3^{-1} imes a_3 \quad a_1^{-1} = eta_1^{-1} \ eta_2^{-1} = eta_3^{-1} imes a_3 \ eta_1^{-1} = eta_1^{-1}$$

For an array of size n it replaces n field inversions with 3n field multiplications + 1 field inversion.



- n multiplications for the acc. products
- 1 inversion of the accumulated product
- 2 multiplications to invert each element which warrants the change

It cannot be parallelized as is.

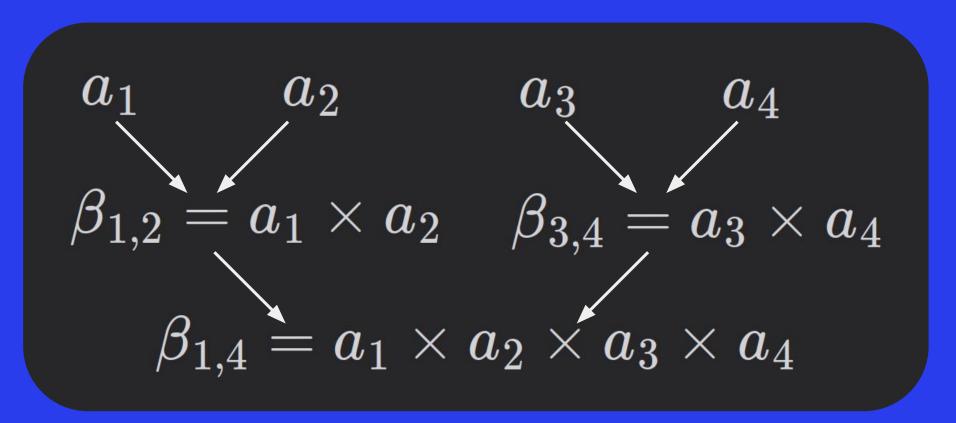
Calculating any of the accumulated products requires the previous value.

So we'll adapt the algorithm for its parallelization.



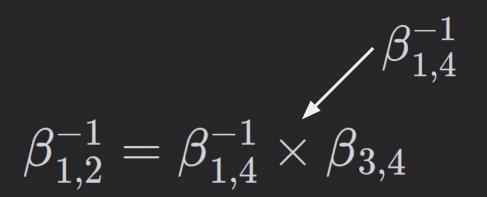


But suppose the amount is a power of two.



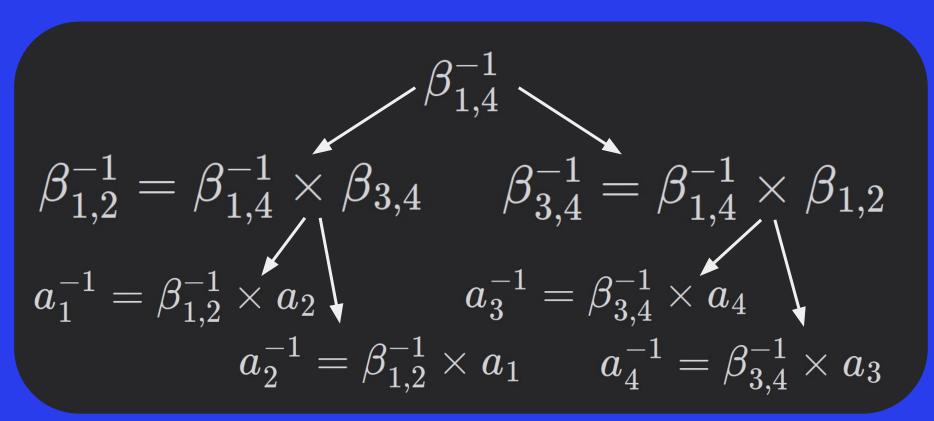
 In the same level of the tree, all multiplications are independent.
 They can be parallelized.

$$\beta_{1,4}^{-1} \longleftarrow eea(\beta_{1,4})$$



*Intuitively

$$eta_{1,2}^{-1} = eta_{1,4}^{-1} imes eta_{3,4}$$
 $= rac{1}{a_1 imes a_2 imes a_3 imes a_4} imes a_3 imes a_4$





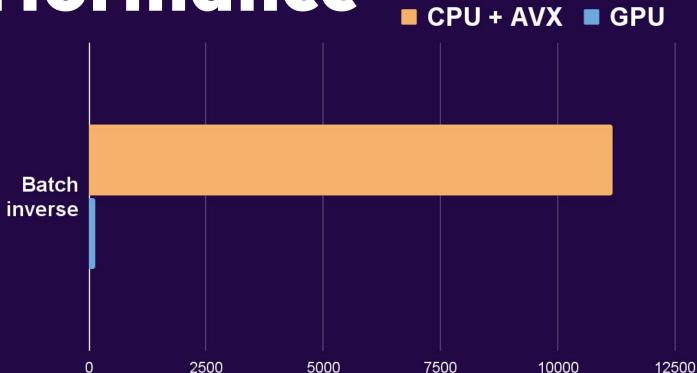
Once again, each level of this tree can be parallelized.

Even more CUDA-specific optimizations can be applied to it:



- Use of shared memory
- Use of warps to invert 32 elements at once
- Use of consecutive memory access

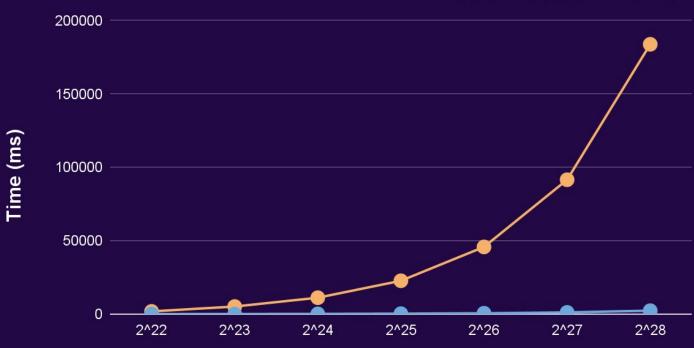
Performance



Time (ms) for 2^24 elements

Performance





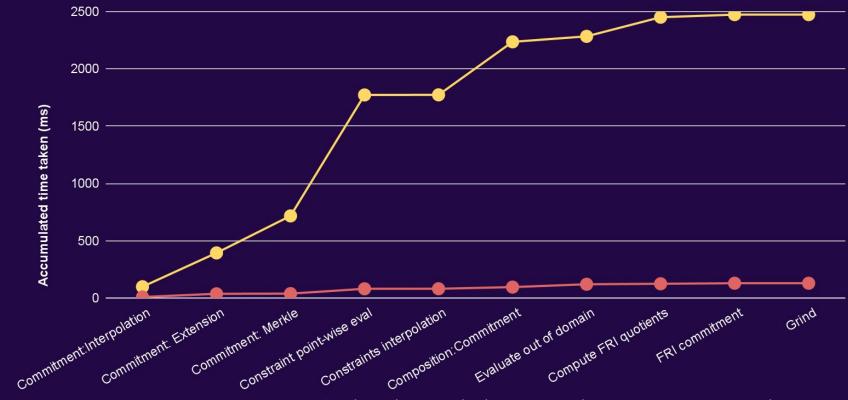
Number of elements

What we learned

- GPU parallelization is a very powerful tool to make our algorithms quicker and cheaper to run.
- A simple heuristic goes a long way in harnessing the power of both high-performance and commodity hardware GPUs.

More metrics

CPU + AVXGPU



* Wide Fibonacci with Blake, with 2^(10) columns of size 2^(16) each.

Summary

Circle STARKs utilize smaller fields to balance security and efficiency 2

Harnessing **GPU** power is nowadays vital for the computation of cryptography primitives.

3

We should keep an eye on future hardware acceleration trends.

Due thanks

Thank you!

Contact









@nethermindeth

@eryxcoop