



Hi3536DV100 H.265/H.264 Decoder Processor

Brief Data Sheet

Issue **02**

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Hi3536DV100 H.265/ H.264 Decoder Processor

Key Specifications

Processor Core

- ARM Cortex A7 @850 MHz
 - 32 KB L1 I-cache, 32 KB L1 D-cache
 - 128 KB L2 cache
 - NEON and FPU

Video Encoding/Decoding Protocols

- H.265 Main Profile, Level 4.1 decoding
- H.264 Baseline/Main/High Profile, Level 4.2 decoding
- JPEG Baseline encoding
- MJPEG/JPEG baseline decoding

Video Encoding/Decoding

- H.265/H.264/JPEG encoding and decoding of multiple streams
 - 4x1080p@25 fps H.265/H.264 decoding
 - 4x960p(1280*960)@30 fps H.265/H.264 decoding
 - 4x720p@30 fps JPEG decoding

Video and Graphics Processing

- Sharpen and contrast strengthening
- 1/15x to 16x video scaling
- 1/2x to 2x graphics scaling
- Cover regions
- OSD overlaying

Audio Encoding/Decoding

- Software audio encoding and decoding complying with multiple protocols

Security Engine

- AES, DES, and 3DES algorithms implemented by hardware

Video Interfaces

- VO interfaces
 - One HDMI 1.4b output interface
 - One VGA HD output interface
 - HDMI/VGA outputs from the same source, with the maximum output of 1080p@60 fps
 - One HD video layer and 16-picture output
 - One HD PIP layer
 - One ARGB1555 or ARGB8888 HD graphics layer
 - One hardware cursor layer in ARGB1555 or ARGB8888 format (configurable) with the maximum resolution of 256 x 256

Audio Interfaces

- Two unidirectional I²S/PCM interfaces
 - One input interface, supporting dual-channel input
 - One output interface, supporting dual-channel output
 - 16-bit audio inputs and outputs
- Integrated with Audio DAC
 - 48 kHz, 44.1 kHz, 32 kHz sampling rates
 - Dual-audio channel line-out output

Ethernet Ports

- One fast Ethernet (FE) interface

- Integrated with FE PHY
- PHY, RMII, and MII modes
- 10/100 Mbit/s half-duplex or full-duplex
- TSO for reducing the CPU usage

Peripheral Interfaces

- One SATA 2.0 interface
 - PM
 - eSATA
- Two USB 2.0 host ports, supporting the hub
- Three UART interfaces, one of which supporting four wires
- One IR interface
- One I²C interface
- Multiple GPIO interfaces

Memory Interfaces

- One 16-bit DDR3/DDR3L SDRAM interface
 - Maximum frequency of 800 MHz
 - ODT
 - Maximum capacity of 512 MB
 - Automatic power consumption control
- SPI NOR/NAND flash interface
 - 1-/2-/4-wire SPI NOR/NAND flash
 - Two CSs, connected to different types of flash memories
 - Maximum capacity of 64 MB for each CS (for the SPI NOR flash)
 - Maximum capacity of 512 MB for each CS (for the SPI NAND flash)
 - 2 KB/4 KB page size (for the SPI NAND flash)
 - 8-bit/1 KB, 16-bit/1 KB, 24-bit/1 KB, or 28-bit/1 KB ECC (for the SPI NAND flash)
- Embedded 4 KB BOOTROM

RTC with an Independent Power Supply

- Independent battery for supplying power to the RTC

Configurable Boot Modes

- Booting from the BOOTROM
- Booting from the SPI NOR flash
- Booting from the SPI NAND flash

SDK

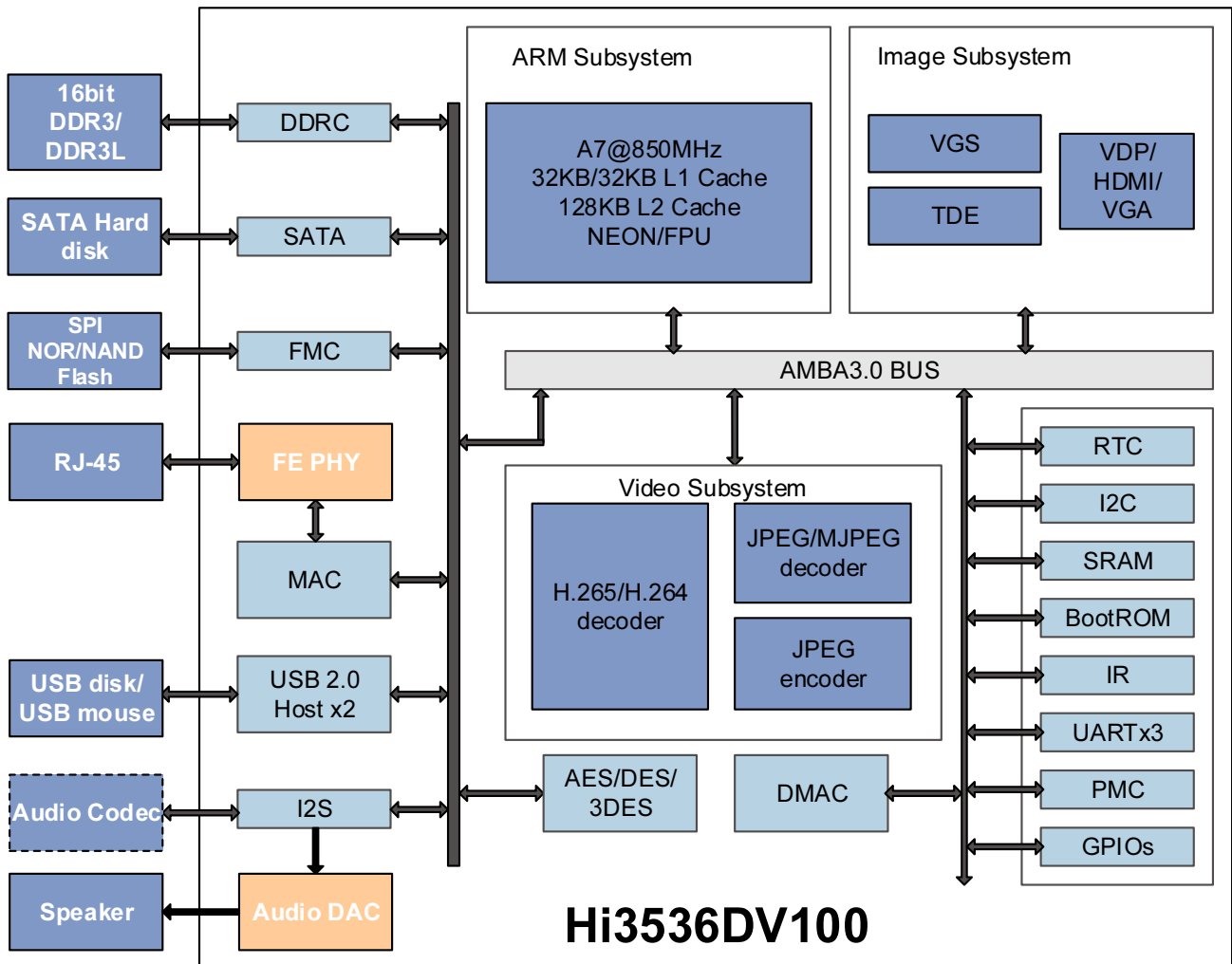
- Linux 4.9-based SDK
- Audio encoding and decoding libraries complying with various protocols
- High-performance H.265/H.264 PC decoding library

Physical Specifications

- Power consumption
 - Typical power consumption of 1.6 W
 - Multi-level power consumption control
- Operating voltages
 - 1.1 V core voltage
 - 1.26 V CPU voltage
 - 3.3 V I/O voltage
 - 1.5 V DDR3 SDRAM/1.35 V DDR3L SDRAM

**Hi3536DV100 H.265/ H.264 Decoder Processor**

- interface voltage
- Package
 - RoHS, TFBGA
 - Lead pitch of 0.65 mm (0.03 in.)
- Body size of 13 mm x 13 mm (0.51 in. x 0.51 in.)
- Operating temperature ranging from 0°C (32°F) to 70°C (158°F)

Functional Block Diagram

The Hi3536D V100 is a professional SoC designed for entry-level H.265 HD (4M/1080p/720p) NVRs. The Hi3536D V100 provides an embedded ARM Cortex-A7 processor, a high-performance H.265/H.264 video decoding engine, a high-performance video/graphics processing engine with various complicated graphics processing algorithms, HDMI/VGA HD outputs, and various peripheral interfaces. These features enable the Hi3536D V100 to provide high-performance, high-picture-quality, and low-cost NVR solutions for customers' products while reducing the eBOM cost.

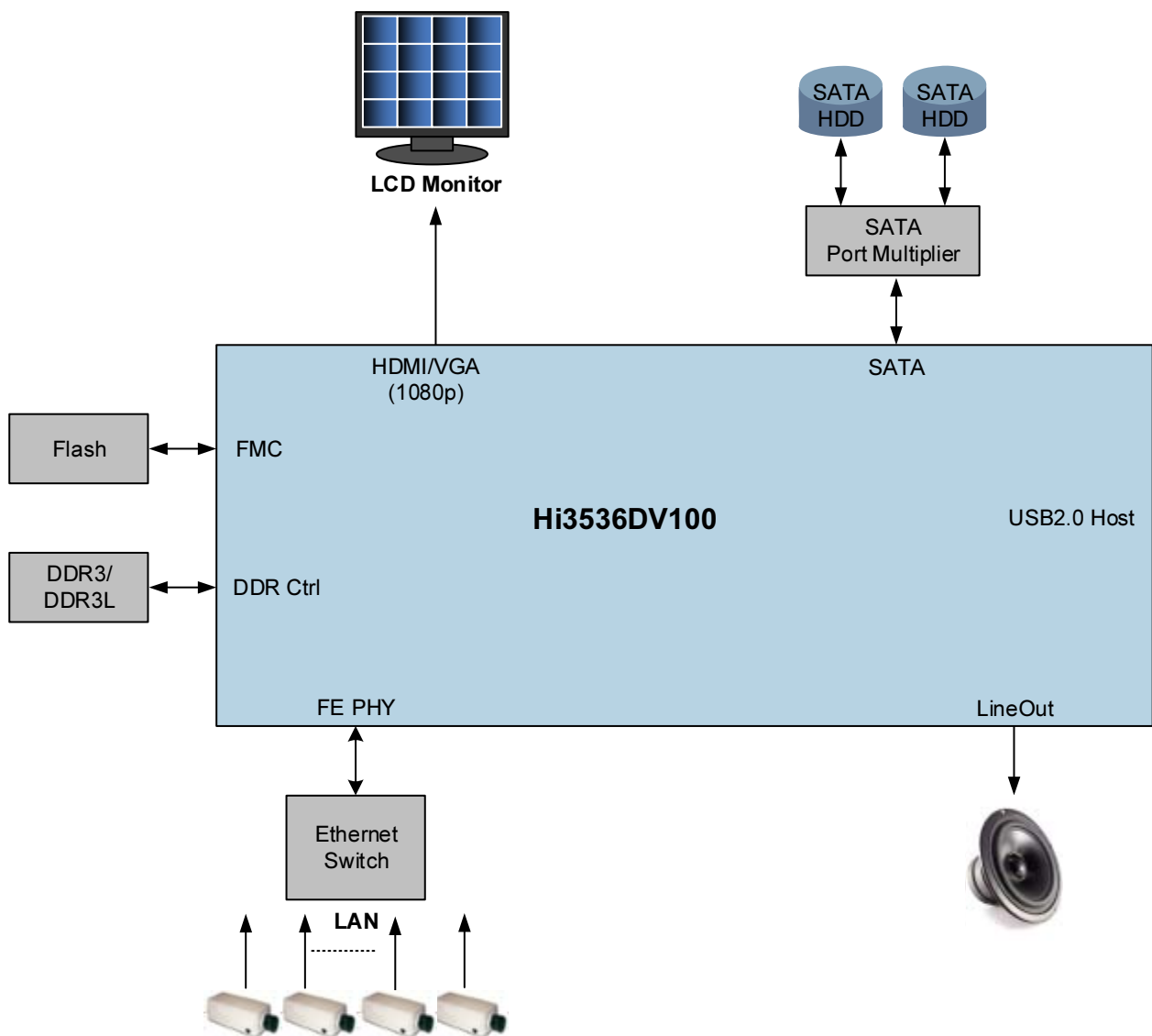


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NVRs (Each with a Hi3536D V100)

8 x 1080p NVR

- 8x IPC streams receiving (primary streams: 1080p@4 Mbit/s; secondary streams: D1@1 Mbit/s)
- 8x IPC main stream forwarding
- 2x 1080p@30 fps or 8x D1@30 fps H.265/H.264 decoding
- HDMI/VGA 1080p@60 fps outputs from the same source





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Acronyms and Abbreviations

3DES	triple data encryption standard
ADPCM	adaptive differential pulse code modulation
AES	advanced encryption standard
CBR	constant bit rate
CS	chip select
CVBS	composite video broadcast signal
DCI	dynamic contrast improvement
DDR	double data rate
DES	data encryption standard
NVR	network video recorder
eBOM	engineering bill of materials
ECC	error correcting code
eSATA	external serial advanced technology attachment
GPIO	general-purpose input/output
HD	high definition
HDMI	high definition multimedia interface
I ² C	inter-integrated circuit
I ² S	inter-IC sound
IR	infrared
MII	media independent interface
ODT	on-die termination
OSD	on-screen display
PCM	pulse code modulation
PM	port multiplexer
QP	quantization parameter
RMII	reduced media independent interface
RoHS	Restriction of Hazardous Substances
ROI	region of interest
RTC	real-time clock
SATA	serial advanced technology attachment
SD	standard definition
SDI	serial digital interface
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SoC	system-on-chip
SPI	serial peripheral interface
SRAM	static random access memory
TDM	time division multiplexing
TSO	TCP segmentation offload
UART	universal asynchronous receiver transmitter
VBR	variable bit rate
VGA	video graphics array
VO	video output