Hi3536D V100 Hardware Design

User Guide

Issue 00B04

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About This Document

Purpose

This document describes the recommendations for Hi3536D V100 schematic diagram design, printed circuit board (PCB) design, and board thermal design.

This document provides hardware design methods for the Hi3536D V100.

Related Version

The following table lists the product version related to this document:

Product Name	Related Version
Hi3536D	V100

Intended Audience

This document is intended for:

- Technical support engineers
- Board hardware development engineers

Change History

Changes between document issues are cumulative. The latest document issue contains all changes made in previous issues.

Issue 00B04 (2018-04-02)

This issue is the fourth draft release, which incorporates the following changes:

Section 1.1.5 is modified.

Issue 00B03 (2017-11-20)

This issue is the third draft release, which incorporates the following changes:

Chapter 1 Schematic Diagram Design

In section 1.1.1, Figure 1-1 and Figure 1-2 are updated.

Section 1.1.5 is updated.

Chapter 4 Recommendations on Chip Heat Dissipation Design

Chapter 4 is updated.

Issue 00B02 (2017-10-18)

This issue is the second draft release, which incorporates the following changes:

Sections 1.1.5, 1.2.5.2, 1.2.10.2, 1.2.10.3, 1.2.11.2, 1.2.12.2, 2.8, 2.9, 2.11, and 2.12 are updated.

Section 4.1 is added.

Issue 00B01 (2017-09-08)

This issue is the first draft release.

Contents

Figures

Tables

1 Schematic Diagram Design

1.1 External Circuits for the Small System

1.1.1 Clocking Circuit

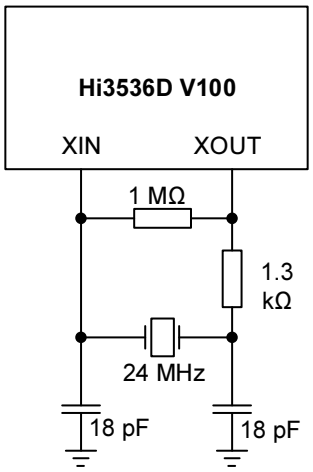
The system clock circuit can be generated by combining the internal feedback circuit of the Hi3536D V100 with a 24 MHz external crystal oscillator circuit.

Figure 1-1 shows the connection mode and component parameters of the crystal oscillator.

CAUTION

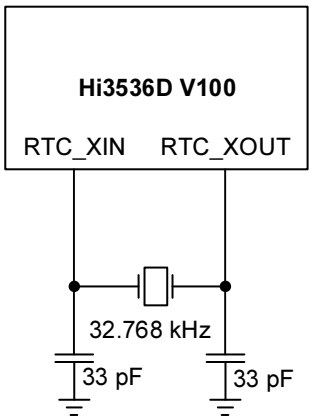
The selected capacitors must match the load capacitor of the crystal oscillator, and the NPO capacitors are recommended. You are advised to select the 4-pin surface mount device (SMD) crystal oscillator and connect its two GND pins to board GND completely to improve the anti-ESD interference capability for the system clock.

Figure 1-1 Connection mode and component parameters of the crystal oscillator



The Hi3536D V100 integrates a real-time clock (RTC). A clock circuit must be provided for the RTC on the board. Figure 1-2 shows the connection mode and component parameters of the RTC crystal oscillator.

Figure 1-2 Connection mode and component parameters of the RTC crystal oscillator



NOTE

The capacitance of the capacitors in Figure 1-2 must match the load capacitance of the actual crystal oscillator. The inherent load capacitance varies according to the brand and model of the crystal oscillator.

1.1.2 Reset and Watchdog Circuits

The Hi3536D V100 selects the internal reset mode or external reset mode by checking the status of the POR_ENABLE pin during power-on.

- When the level of POR_ENABLE is high, the internal reset mode is selected.

  After the master chip is powered on, the internal power-on reset (POR) circuit resets the chip, as shown in Table 1-1.

Table 1-1 Pins related to internal reset

Pin No.	Function	Description
V11	SYS_RSTN_OUT	This pin outputs high level in normal mode. It outputs low level when the chip reset is triggered, and is restored to high level after about 64 ms. It outputs reset signals to reset related peripherals.
V12	-	The RSTN pin is invalid and can be floated.

CAUTION

In internal reset mode, peripherals related to the small system (such as the boot flash memory) must release the reset signal before the Hi3536D V100 or they release the reset signals simultaneously to ensure that the system boots properly. Otherwise, exceptions such as system boot failure may occur.

- When the level of POR_ENABLE is low, the external reset mode is selected.

  After the main chip is powered on, the internal POR circuit does not take effect. In this case, the RSTN pin is a reset signal input pin. A dedicated reset chip can be used to generate the reset signal, as shown in Table 1-2.

Table 1-2 Pins related to external reset

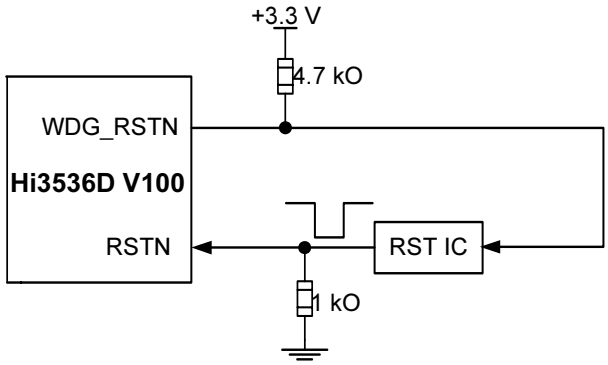
Pin No.	Function	Description
V11	WDG_RSTN	This pin is an open drain (OD) output pin and it must connect to an external pull-up resistor. When the watchdog takes effect, the WDG_RSTN pin outputs low level continuously and is restored to high level until the RSTN pin detects a low level reset signal.
V12	RSTN	The system is reset when Hi3536D V100 detects that the level of the RSTN pin is low. After connecting to the external reset signal, the signal from the WDG_RSTN pin is output to the RSTN pin. For details, see Figure 1-3.

CAUTION

The WDG_RSTN pin cannot be directly connected to the RSTN pin.

- Figure 1-3 shows the typical external reset and watchdog circuit.

Figure 1-3 Typical external reset and watchdog circuit



1.1.3 JTAG Debug Interface

Table 1-3 describes the signals over the JTAG debug interface.

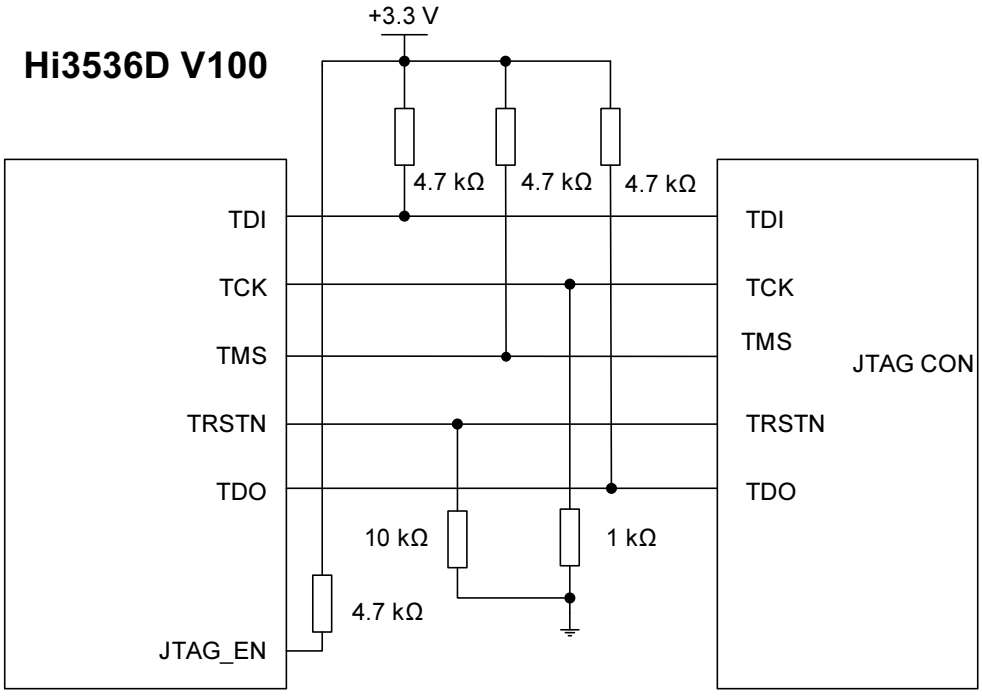
Table 1-3 Signals over the JTAG debug interface

Signal	Description
TCK	JTAG clock input. This signal must connect to a 1 kΩ pull-down resistor on the board.
TDI	JTAG data input. This signal must connect to a 4.7 kΩ pull-up resistor on the board.
TMS	JTAG mode select input. This signal must connect to a 4.7 kΩ pull-up resistor on the board.
TRSTN	JTAG reset input. To ensure that the Hi3536D V100 works properly, this signal must connect to a 10 kΩ pull-down resistor on the board.
TDO	JTAG data output. This signal must connect to a 4.7 kΩ pull-up resistor on the board.

NOTE

For details about the impedance of the external pull-up and pull-down resistors, see Figure 1-4.

Figure 1-4 JTAG connection mode and standard connector pins



The JTAG pins on the Hi3536D V100 can be multiplexed as GPIO pins by configuring the JTAG_EN pin.

When the Hi3536D V100 works properly, the TEST_MODE pin must be floated or connect to a pull-down resistor.

1.1.4 System Configuration Circuit for Hi3536D V100 Hardware Initialization

The Hi3536D V100 can boot from the BOOTROM, which is specified by configuring the BOOTROM_SEL pin.

When the Hi3536D V100 boots from the BOOTROM, the serial port communication mechanism is started, and the communication between the serial port and the related software running on the PC is set up, and the boot program is downloaded. If the serial port communication times out, the Hi3536D V100 will boot from an external SPI NAND/NOR flash memory.

CAUTION

If the hardware configuration pins of Hi3536D V100 connect to the signal pins of the peripherals, pull-up or pull-down resistors must be designed for the signals to determine the initial states of configuration pins. 4.7 kΩ pull-up or pull-down resistors are recommended.

The working mode of each module is determined based on the pull-up/pull-down status of the corresponding configuration pin during the power-on initialization of the Hi3536D V100. Table 1-4 describes hardware configuration signals.

Table 1-4 Hardware configuration signals

Signal	Direction	Description
JTAG_EN	I	JTAG enable 0: disabled 1: enabled
BOOTROM_SEL	I	Boot mode select 0: booting from the SPI flash 1: booting from the BOOTROM
SFC_DEVICE_MODE	I	SPI flash select 0: SPI NOR flash 1: SPI NAND flash
SFC_BOOT_MODE	I	Boot mode select for the SPI flash Boot address mode of the SPI NOR flash when SFC_DEVICE_MODE is 0 0: 3-byte address mode 1: 4-byte address mode Boot mode of the SPI NAND flash when SFC_DEVICE_MODE is 1 0: 1-wire boot mode 1: 4-wire boot mode

Signal	Direction	Description
POR_ENABLE	I	Internal POR enable 0: disabled 1: enabled

1.1.5 Power Supply Circuit

NOTE

For details about the power specifications of the Hi3536D V100, see section 2.5 "Electrical Specifications" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.

Note the following when designing the power supply circuit:

- The ripple and noise amplitude of both the Hi3536D V100 core power and CPU power must be within ±30 mV at the chip pins.
- Design the power supply circuit including the filter capacitance and number of capacitors by strictly following the schematic diagram of the Hi3536D V100 demo board.
- Connect the core power pin DVDD_CORE. The voltage is controlled by the selective voltage binging (SVB) dynamic voltage scaling circuit. The SVB dynamic voltage scaling circuit must be used; otherwise, exceptions such as system crash may occur. A DC-DC converter that supports at least 1 A current is required for DVDD_CORE.
- Connect the CPU power pin DVDD_CPU. The voltage is controlled by the SVB dynamic voltage scaling circuit. The SVB dynamic voltage scaling circuit must be used; otherwise, exceptions such as system crash may occur. A DC-DC converter that supports at least 1 A current is required for DVDD_CPU. The CPU load is light. Therefore, pay attention to the relationship between the load current and the operating mode of the DC-DC during model selection and prevent the DC-DC from entering the light-load high-efficiency mode because the power noise becomes larger in this mode.
- The core power and CPU power can share the same DC-DC power supply. The voltage is controlled by the SVB dynamic voltage regulation circuit (**PWM_SVB_CORE** by default). The SVB dynamic voltage regulation circuit must be used; otherwise, system crashes or other anomalies may result. In the design where DVDD_CORE and DVDD_CPU share the same power supply, a DC-DC converter that supports at least 2 A current is required.

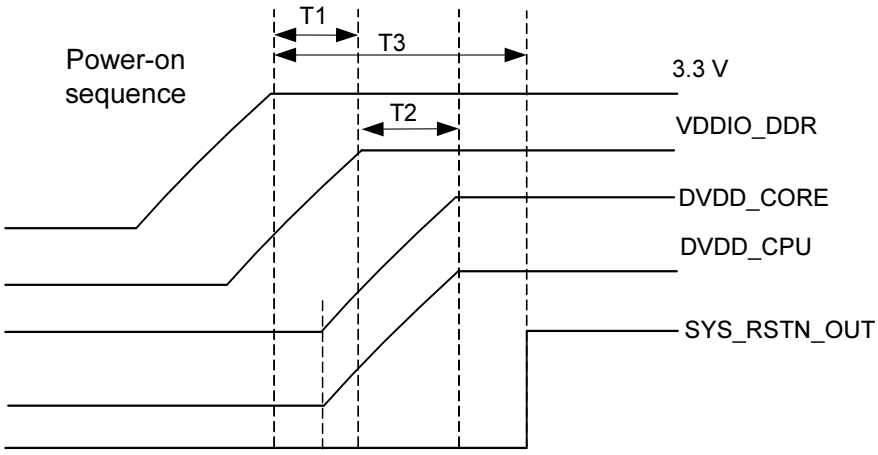
  For details about the design descriptions, see the *Hi3536D V100 Core and CPU Power Combination Solution*.
- Connect the I/O power pin DVDD33 to the 3.3 V power.
- Connect the DDR power pin VDDIO_DDR. This pin and the connected DDR SDRAM must use the power supply from the same power network. The DDR load is light. Therefore, pay attention to the relationship between the load current and the operating mode of the DC-DC during model selection and prevent the DC-DC from entering the light-load high-efficiency mode because the power noise becomes larger in this mode.
- The PLL power pins AVDD11_PLL and AVDD33_PLL are isolated from the DVDD_CORE and 3.3 V power supplies by using the 1 kΩ@100 MHz electromagnetic interface (EMI) bead. For details about the circuit design, see the schematic diagram of the Hi3536D V100 demo board.

  - The ripple and noise amplitude of the AVDD11_PLL power must be less than 20 mV at the chip pins. The ripple noise of the fixed frequency cannot be found on the power supply. Fixed-frequency ripple and noise are not allowed on the AVDD11_PLL power.
  - The ripple and noise amplitude of theAVDD33_PLL power must be less than 20 mV at the chip pins. The ripple noise of the fixed frequency cannot be found on the power supply. Fixed-frequency ripple and noise are not allowed on the AVDD33_PLL power.
- The DDR CLK power VDDIO_CK_DDR must be isolated from the DDR I/O power by using an EMI bead whose specification is 1 kΩ@100 MHz. For details about the circuit design, see the schematic diagram of the Hi3536D V100 demo board.
- The PLL power pins (AVDD33_DDRPLL1 or AVDD33_DDRPLL2) of the DDR must be isolated from the 3.3 V power by using an EMI bead whose specifications are 1 kΩ@100 MHz. For details about the circuit design, see the schematic diagram of the Hi3536D V100 demo board.

Power-on and Power-off Sequences

- Figure 1-5 shows the power-on sequence in internal reset mode.

Figure 1-5 Power-on sequence in internal reset mode

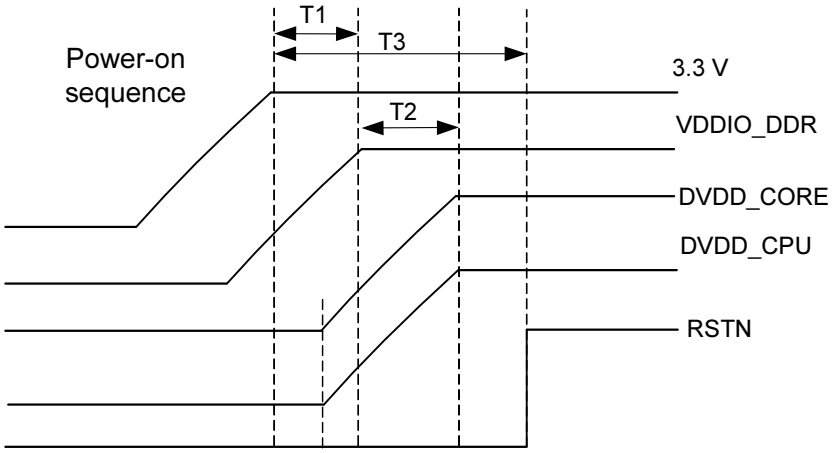


NOTE

T3 is about 64 ms; T1 + T2 ≤ 32 ms; T2 > 0; T1 > 0. DVDD_CORE and DVDD_CPU are turned on at the same time.

- Figure 1-6 shows the power-on sequence in external reset mode.

Figure 1-6 Power-on sequence in external reset mode

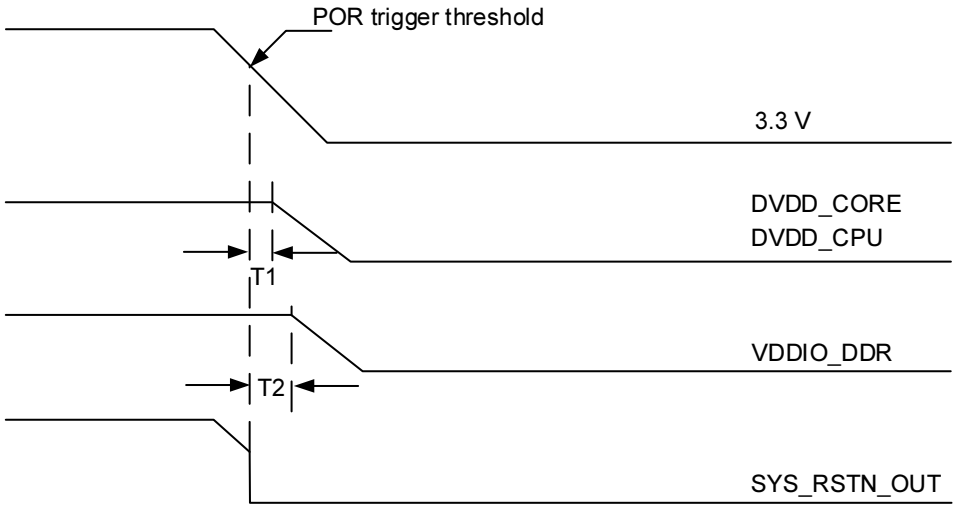


NOTE

T1 + T2 ≤ 100 ms; T2 > 0; T1 > 0, T3 > T1 + T2. DVDD_CORE and DVDD_CPU are turned on at the same time.

- Figure 1-7 shows the power-off sequence of the power supplies in internal reset mode.

Figure 1-7 Power-off sequence of the power supplies in internal reset mode



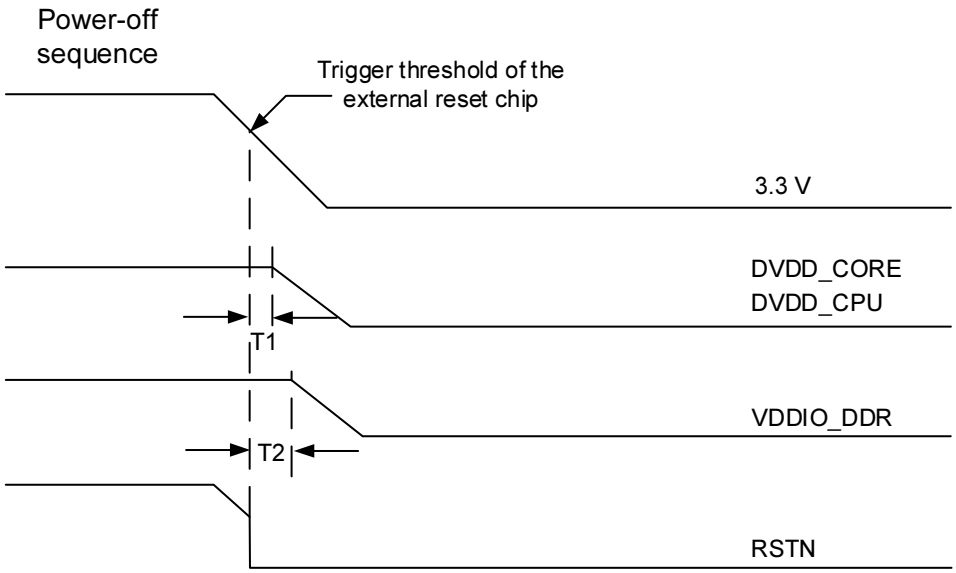
NOTE

T1 is greater than 0. T2 is greater than 0.

In internal reset mode, the 3.3 V power is turned off first, and then VDDIO_DDR is turned off. When the level of the 3.3 V power decreases to the POR trigger threshold, the POR is triggered and then the core power starts to be turned off.

- Figure 1-8 shows the power-off sequence of the power supplies in external reset mode.

Figure 1-8 Power-off sequence of the power supplies in external reset mode



NOTE

T1 is greater than 0. T2 is greater than 0.

- The 3.3 V power is powered off first. When the level of the 3.3 V power decreases to the threshold of the external reset chip, the reset of the external reset chip is triggered and the external reset chip generates the RSTN reset signal. At this time, the core and CPU power supplies can be powered off.

CAUTION

During the power-off process in internal reset mode, the Hi3536D V100 POR module may be in any of the following working states:

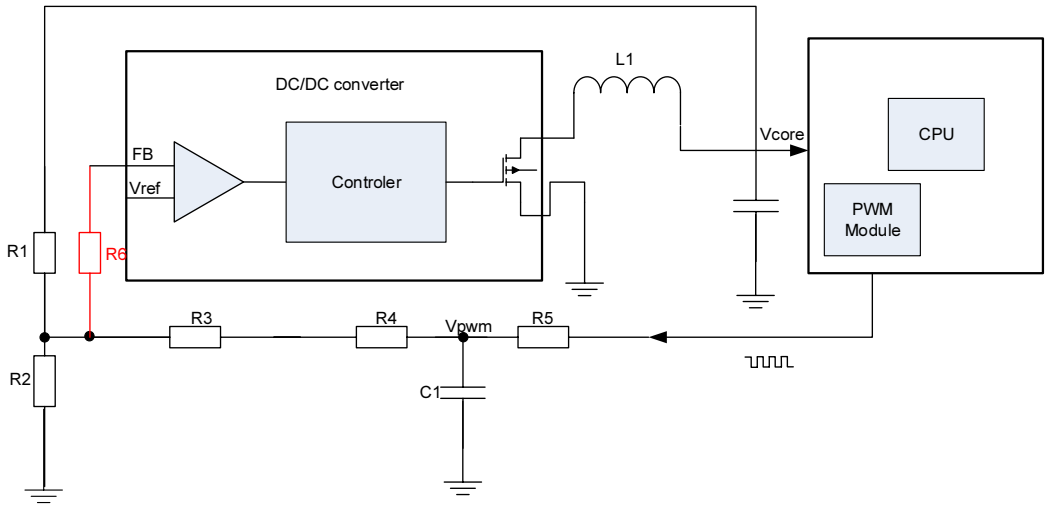
- When the voltage of DVDD33 decreases from 3.3 V to 2.6 V, the timing starts. If the voltage of DVDD33 is higher than 2.6 V at the 5 μs time point, the POR module considers that there is a power fluctuation and does not trigger reset, and the SYS_RSTN_OUT pin retains the high level.
- When the voltage of DVDD33 decreases from 3.3 V to 2.6 V, the timing starts. If the voltage of DVDD33 is greater than 2.1 V but less than or equal to 2.6 V at the 5 μs time point, the POR module triggers reset at this moment (5 μs time point during the timing) and the SYS_RSTN_OUT pin outputs low level.
- When the voltage of DVDD33 decreases from 3.3 V to 2.6 V, the timing starts. If the voltage of DVDD33 is less than or equal to 2.1 V within 5 μs after timing starts, the POR module triggers reset when the voltage of DVDD33 decreases to 2.1 V and the SYS_RSTN_OUT pin outputs low level.

1.1.6 SVB Dynamic Voltage Scaling

The DVDD_CPU and DVDD_CORE power supplies must support dynamic voltage scaling as follows, ensuring the stability of the Hi3536D V100 system:

Transmit the signal from the PWM waveform output pins (SVB_CORE/PWM_SVB_CPU). The pin outputs the direct current (DC) levels ranging from 0 V to 3.3 V after RC filtering. The DC levels are overlapped at the input end of the DC-DC feedback voltage to implement DC-DC output voltage scaling. Then adjust the PWM frequency and duty cycle by configuring related registers to implement dynamic scalding of the DC-DC output voltage. See Figure 1-9.

Figure 1-9 Schematic diagram of dynamic voltage scaling



During SVB circuit design, connect the PWM pin of the Hi3536D V100 to the SVB circuit and then to the FB pin of the DC-DC circuit for the core power supply and CPU power supply. Note the following during design:

- PWM_SVB_CORE is used to adjust the voltage of the core power supply, and PWM_SVB_CPU is used to adjust the voltage of the CPU power supply.
- The error range of the DC voltage of the 3.3 V power for the Hi3536D V100 must be within ±50 mV.
- A resistor (R6) must be reserved before the FB pin in the DC-DC circuit to ensure the loop stability of the DC-DC component.
- The impedance of R6 can be calculated by using the following equation (This calculation method applies only to some DC-DCs of MPS. You need to confirm with the vendors whether this equation applies to the DC-DC of other solutions):

  R6 x (Vout/Vref) + R1 = 200 kΩ

  where

  Vout is the nominal voltage of the DC-DC output, Vref is the reference voltage of the DC-DC, and R1 is the voltage-division resistor on the FB pin of the DC-DC.

  The value 200 kΩ in the right of the equation is an empirical value, and it can be changed to 100 kΩ if the capacitance of the DC-DC output capacitor is greater than the reference capacitance in the DC-DC manual.

  The obtained impedance of R6 is a reference value. The actual impedance fluctuates around the calculation result, and is close to the reference value.
- The reference voltage values of the selected DC-DC chip must be those contained in Table 1-5 and Table 1-6. The Vref precision deviation of the DC-DC should not exceed 2%.

CAUTION

The precision of all the resistors must be 1%, and the material of the capacitors must be X5R or X7R.

The stability of the SVB output voltage depends on two PWM output signals. The parameters of the SVB circuit must be consistent with those in Table 1-5 and Table 1-6.

Table 1-5 RC parameters for DVDD_CORE_SVB voltage scaling

Vref (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	R5 (kΩ)	C (μF)
0.45	18	11.3	69.8	90.9	1	2.2
0.6	13.3	14.7	1.54	120	1	2.2
0.608	19.6	22.1	56.2	120	1	2.2
0.765	12.7	27	15.4	100	1	2.2
0.8	14.7	36.5	59	75	1	2.2
0.807	14.3	36.5	59	69.8	1	2.2

Table 1-6 RC parameters for DVDD_CPU_SVB voltage scaling

Vref (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	R5 (kΩ)	C (μF)
0.45	18	10	40.2	100	1	2.2
0.6	14.3	13.3	30.1	80.6	1	2.2
0.608	13.3	12.7	22.1	80.6	1	2.2
0.765	18	30.1	40.2	100	1	2.2
0.8	12.7	24.3	18	80.6	1	2.2
0.807	13.3	26.1	33.2	69.8	1	2.2

1.2 Design of the Hi3536D V100 Interface Circuits

1.2.1 DDR3/DDR3L Interfaces

1.2.1.1 Features

For details about the features of the DDRC, see chapter 4 "Memory Interfaces" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.

1.2.1.2 Circuit Design

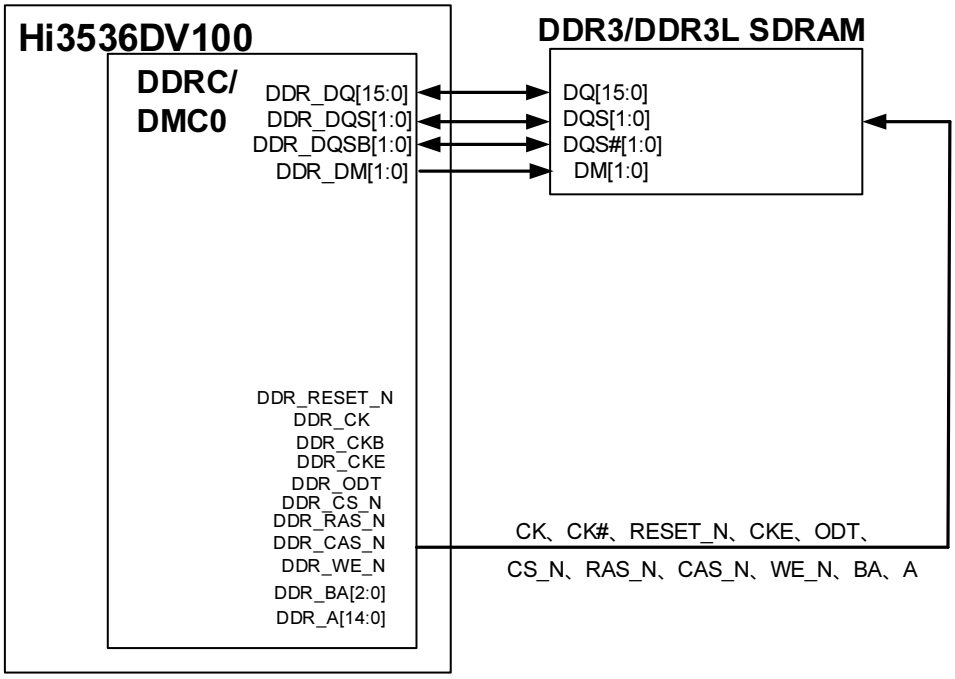
The schematic diagram and PCB design of the DDR must be the same as those of the demo board.

DDR Topology

Hi3536D V100 supports the DDR3/DDR3L topology.

The Hi3536D V100 can be connected to one 16-bit DDR3/DDR3L SDRAM. The DDRC channel connects to one 16-bit DDR3/DDR3L SDRAM. For details, see Figure 1-10.

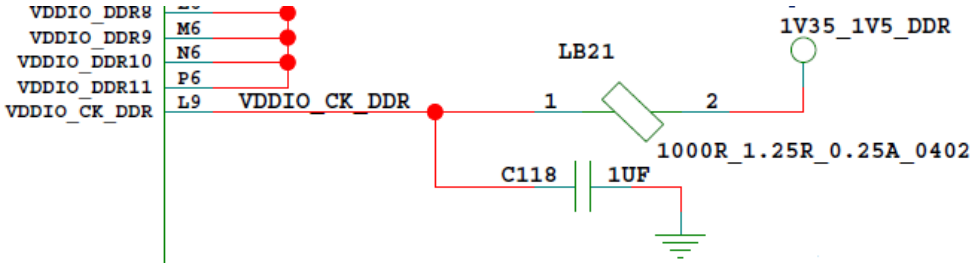
Figure 1-10 Topology for connecting the DDRC to one 16-bit DDR3/3L SDRAM



DDR Power Supply

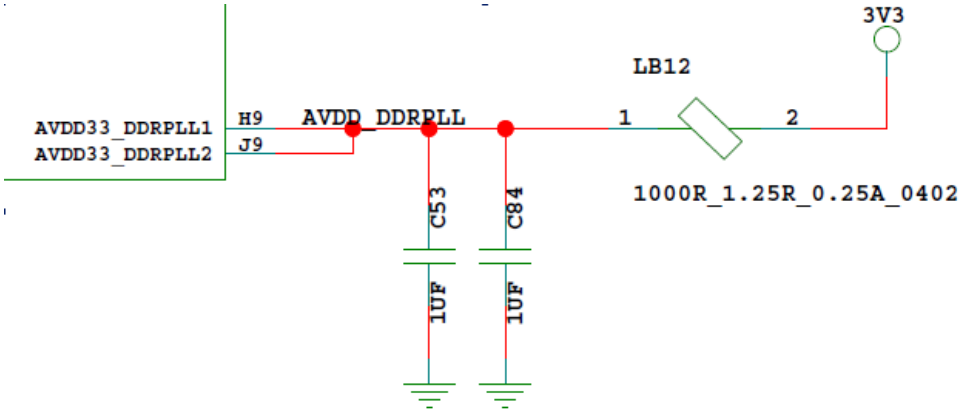
The DDRC of the Hi3536D V100 supports only the DDR3/DDR3L SDRAM. The voltage of the DDRIO power is 1.5 V/1.35 V, and the corresponding reference voltage (Vref) is 0.75 V/0.675 V. The DDRIO power of the Hi3536D V100 must be consistent with the I/O power of the DDR SDRAMs. A separate power chip must be provided on the board to supply power to the DDR3/DDR3L SDRAMs and the 1.5 V/1.35 V power pins (VDDIO_DDR) of the Hi3536D V100 DDRC. The VDDIO_CK_DDR must be isolated by using a bead. For details, see the diagram schematic of the Hi3536D V100 demo board. Figure 1-11 shows the VDDIO_CK_DDR circuit design.

Figure 1-11 VDDIO_CK_DDR circuit diagram



The AVDD33_DDRPLL1/2 pin must be isolated from the 3.3 V power by using a 1 kΩ@100 MHz EMI bead, and the filter capacitors must be placed close to the pin. For details, see the schematic diagram of the Hi3536D V100 demo board. Figure 1-12 shows the AVDD33_DDRPLL circuit design.

Figure 1-12 AVDD33_DDRPLL circuit diagram

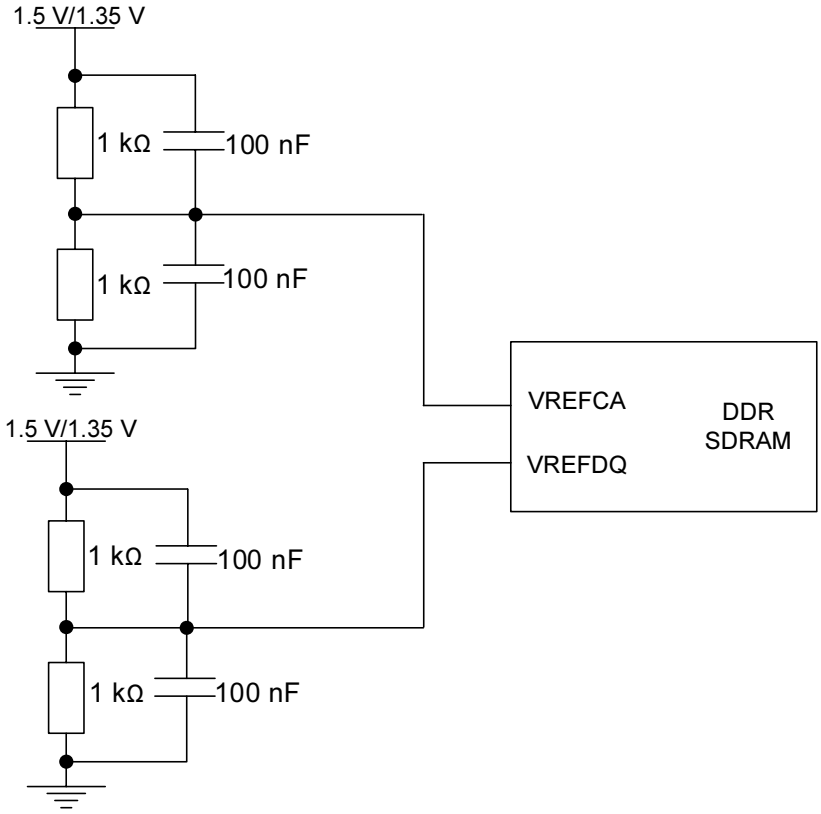


The 0.75 V/0.675 V Vref for the DDR3/DDR3L SDRAMs is obtained by using the1 kΩ±1% voltage division resistor. Figure 1-13 shows the reference design of the DDR3/DDR3L voltage-divider circuit.

CAUTION

VREFDQ and VREFCA must be separately supplied with power.

Figure 1-13 Reference design of the DDR3/DDR3L voltage-divider circuit



1.2.1.3 Matched Mode Design

Bidirectional DQ and DQS Signals

In the Hi3536D V100 DDR application, the point-to-point topology is used. The DQ, DQS_P, and DQS_N signals of the Hi3536D V100 connect directly to the DQ, DQS_P, and DQS_N signals of the DDR respectively.

Differential Clocks

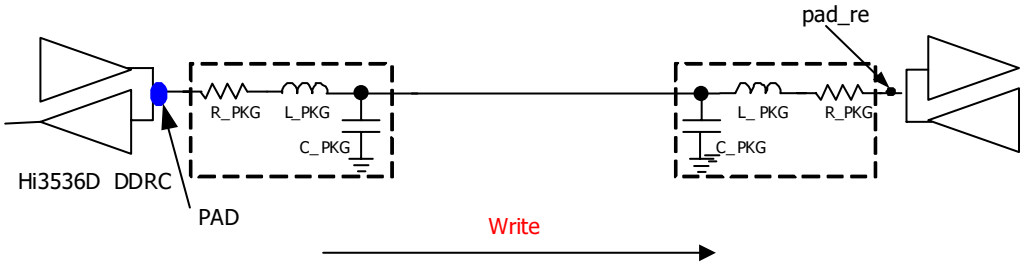
- Hi3536D V100 has one group of differential clock signals DDR_CLK_N/DDR_CLK_P.
- DDR_CLK_N/DDR_CLK_P connects to a 100 Ω resistor at the DDR SDRAM end. For details, see the schematic diagram of the Hi3536D V100 demo board.

1.2.1.4 Address and Command Signals

In the Hi3536D V100 DDR application:

- The Hi3536D V100 signals (DDR_A0 and DDR_A2, DDR_A3, DDR_A5, DDR_A7, DDR_A9, DDR_A10, DDR_A11, DDR_A12, DDR_A13, DDR_BA0, DDR_BA2, DDR_RAS, DDR_CAS, DDR_WE_N, and DDR_RESET_N) need to connect to a 33 Ω matched resistor in series at the Hi3536D V100 end.
- When Hi3536D V100 connects to one 16-bit DDR SDRAM, the address and command signals use the one-drive-one connection mode, as shown in Figure 1-14.

Figure 1-14 Address and command signals in one-drive-one mode



1.2.1.5 External Resistor for the DDR SDRAM

A 240 Ω±1% external resistor (ZQ) connects to the DDR3/DDR3L SDRAM.

1.2.2 RTC

CAUTION

In fixed frequency-division mode, the timing accuracy of the embedded RTC depends on the external crystal oscillator. Select an appropriate crystal oscillator based on its frequency deviation and temperature offset. If high timing accuracy is required, the external integrated RTC is recommended.

1.2.3 UART

1.2.3.1 Features

For details about the features of the UART, see section 11.2 "UART" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet.*

1.2.3.2 Circuit Design

The Hi3536D V100 has three UART units, and UART0 is used for debugging. In the schematic diagram of the Hi3536D V100 demo board, UART0 is used for debugging, and the fastboot boots only from UART0.

1.2.4 EFUSE

The AVDD25_EFUSE pin of Hi3536D V100 must be floated.

1.2.5 USB 2.0 Ports

1.2.5.1 Features

For details about the features of the USB 2.0 ports, see section 11.6 "USB 2.0" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet.*

1.2.5.2 Circuit Design

The design requirements are as follows:

- The analog power pin AVDD33_USB must be isolated from the 3.3 V digital power by using an EMI bead, and filter capacitors must be placed close to the AVDD33_USB pin.
- ESD protection measures must be taken for USB signals and ESD components must be placed close to USB ports. The junction capacitance of the ESD component must be less than 2 pF.
- For details, see the schematic diagram of the Hi3536D V100 demo board.

1.2.6 Ethernet MAC Interface

1.2.6.1 Features

For details about the features of the gigabit media access controller (GMAC) interface, see chapter 5 "Network Interfaces" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.

1.2.6.2 Circuit Design

The Hi3536D V100 provides an Ethernet media access controller (MAC) interface, which supports the media independent interface (MII) and RMII modes. The MII and RMII interface supports only 3.3 V power.

CAUTION

The Hi3536D V100 provides only one MAC interface. Therefore, the MII/RMII and Fast Ethernet PHY (FEPHY) functions cannot be used at the same time.

Figure 1-15 to Figure 1-16 show the signal connection in two modes.

Figure 1-15 Signal connection in MII mode

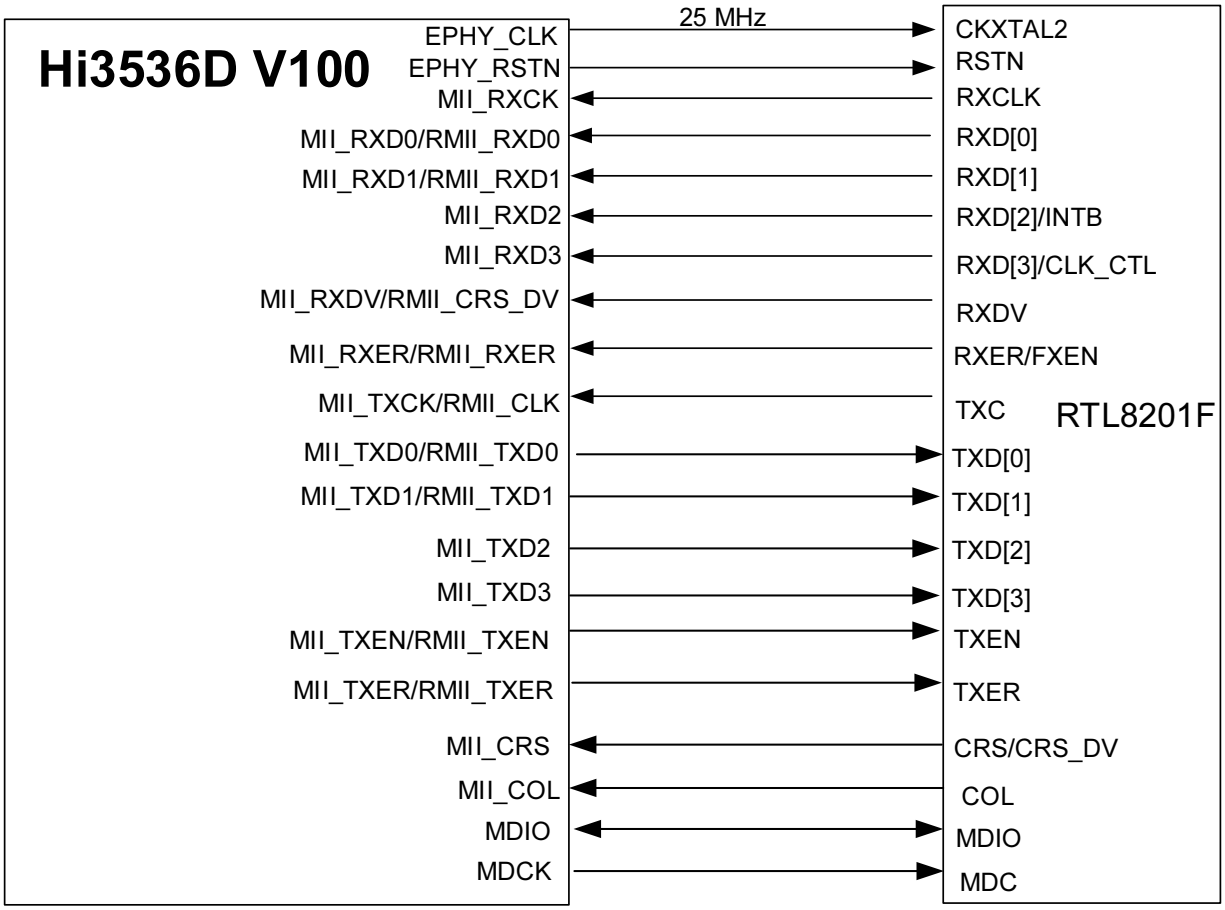
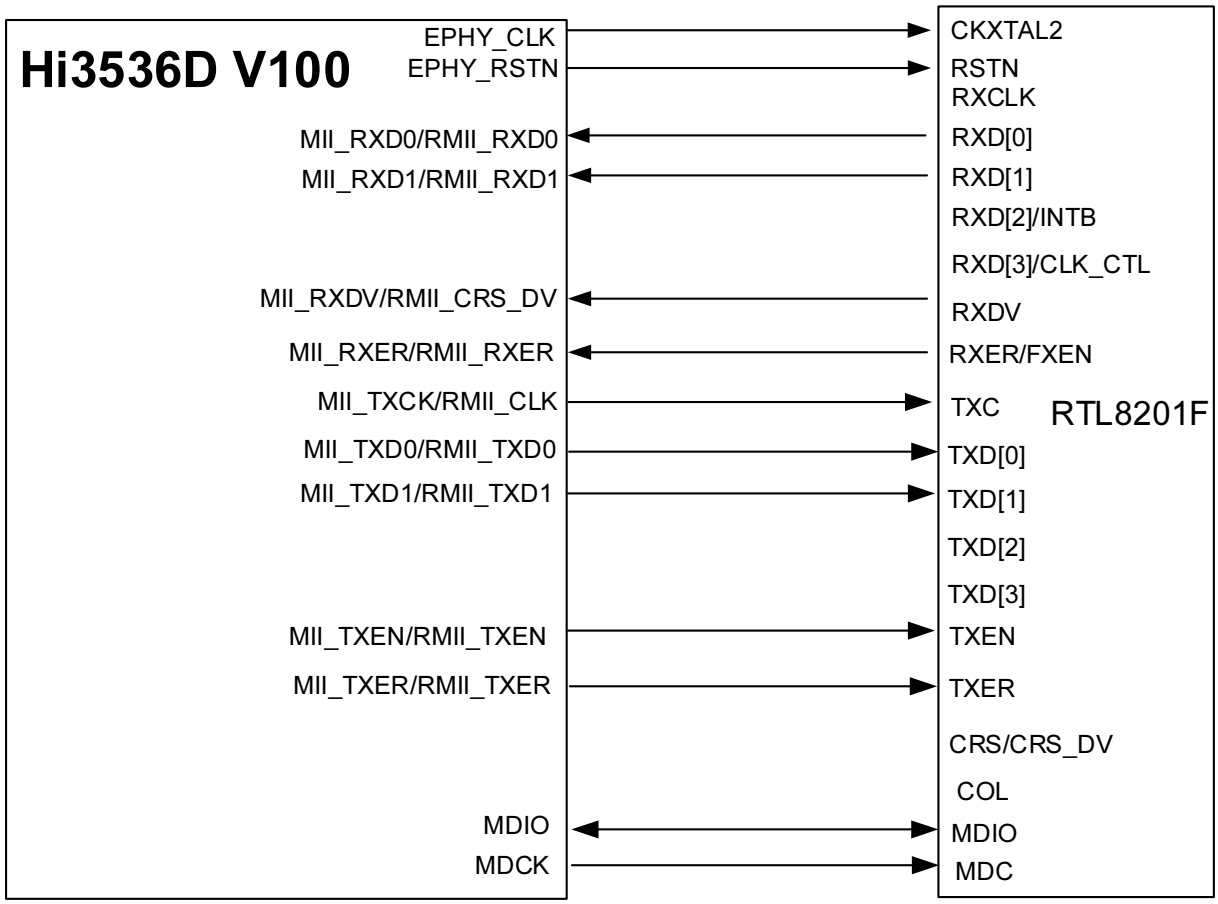


Figure 1-16 Signal connection in RMII mode



Some network port signals are connected in point-to-point topology. The following are recommendations for designing matched resistors:

- The Management Data Input/Output (MDIO) signal needs to connect to a pull-up resistor, whose resistance must meet the PHY connection requirement. The MDCK signal needs to connect to a 33 Ω resistor in series close to the source end.
- In consideration of the EMI risk of the actual product, it is recommended that the TXD0–TXD3, TXEN, and TXCK signals connect to a 33 Ω resistor in series at the Hi3536D V100 end.
- In RMII mode, the RMII_CLK signal needs to connect to a 33 Ω resistor in series at the Hi3536D V100 end.
- Connect a 33 Ω resistor to the EPHY_CLK signal in series close to the Hi3536D V100. It is recommended that the chip reserve an external clock oscillator or crystal on the Ethernet PHY.
- In consideration of the EMI risk of the actual product, it is recommended that the TXD0–TXD3 signals connect to a 33 Ω resistor in series close to the PHY chip.
- The GPIO2_1/EPHY_RSTN pin is used for resetting network PHY chips. Note that this pin must connect to a 1 kΩ–10 kΩ pull-down resistor to ensure that the PHY chips are reset during chip reset.

1.2.7 FEPHY Interfaces

1.2.7.1 Features

For details about the features of the FEPHY interfaces, see chapter 5 "Network Interfaces" in *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.

1.2.7.2 Circuit Design

Hi3536D V100 provides one embedded FEPHY. The medium dependent interface (MDI) in the FEPHY module directly connects to the twisted pair through a transformer and RJ45 interface. At the MAC end, the MII of this module connects to the MAC layer.

The Hi3536D V100 provides only one MAC interface. Therefore, MII/RMII and FEPHY functions cannot be enabled at the same time.

The Hi3535 provides only one MDI.

- The analog power (AVDD33_FE) pins of the FEPHY module must be isolated from digital power pins by using EMI beads, and filter capacitors must be placed close to the analog power pins.
- The MDI signal needs to connect to a 1 Ω resistor with the 0402 encapsulation in series. The resistor must be placed close to the network transformer.
- ETH_MDI_AN/P and ETH_MDI_BN/P can automatically detect the signal transmitting and receiving of the peer end, and appropriate transmit (TX) and receive (RX) channels are configured.

Figure 1-17 FEPHY application diagram

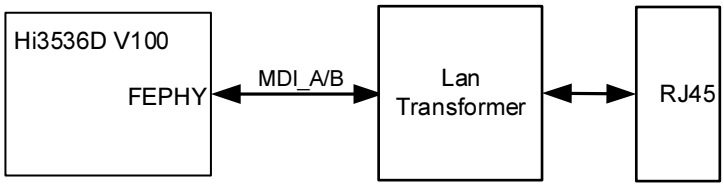


Table 1-7 MDI pin description

Pin Name	I/O	Attribute	Function Description
ETH_MDI_AN	IO	Analog	Differential RX and TX signals The mode can be forcibly or adaptively set to 10BASE-T or 100BASE-TX. The MDI and MDI-X interconnection modes are supported. The polarity of MDI_N and MDI_P can be corrected. In 10 or 100 Mbit/s mode, the automatic medium dependent interface crossover (MDIX) function detects the TX channel of the peer end, and TX and RX channels are configured.
ETH_MDI_AP	IO	Analog	
ETH_MDI_BN	IO	Analog	
ETH_MDI_BP	IO	Analog	

1.2.8 Flash Interfaces

1.2.8.1 Features

The Hi3536D V100 SPI flash controller (SFC) supports the SPI NOR flash and SPI NAND flash.

The SFC also supports two chip selects (CSs) that can connect to two SPI NOR flash memories, two SPI NAND flash memories, or one SPI NAND flash memory and one SPI NOR flash memory.

The read and write operations can be selected by using the CS signals SFC_CS0N and SFC_CS1N.

CAUTION

The master chip provides two CS signals SFC_CS0N and SFC_CS1N. The master chip can boot only from SFC_CS0N after its reset signal is released. During circuit design, connect the CS pin corresponding to the boot flash to the SFC_CS0N pin.

Matched Design for the SPI Flash

Table 1-8 describes the recommended design when an external SPI flash is connected.

Table 1-8 Recommended design when an SPI flash is connected

Signal	Recommended Design
SFC_CLK	A 33 Ω resistor is connected in series at the Hi3536D V100 source end.
SFC_MOSI_IO0 SFC_MISO_IO1 SFC_WP_IO2 SFC_HOLD_IO3 SFC_CS0N SFC_CS1N	The signals are connected directly. A 4.7 kΩ pull-down resistor is recommended to connect to SFC_WP_IO2, and 4.7 kΩ pull-up resistors are recommended to connect to SFC_HOLD_IO3 and SFC_CS0N/SFC_CS1N.

1.2.9 SATA Ports

1.2.9.1 Features

For details about the features of the serial advanced technology attachment (SATA) ports, see section 11.5 "SATA" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.

1.2.9.2 Circuit Design

Hi3536D V100 provides only one SATA 2.0 port.

- The analog power pins (AVDD_SATA and AVDD33_SATA) of SATA ports must be isolated from digital power pins by using EMI beads, and filter capacitors must be placed close to the analog power pins.
- The 10 nF X7R multilayer ceramic capacitor (using the 0402 package) connecting to the Rx and Tx differential signals in series must be placed close to the SATA connector.
- For details, see the schematic diagram of the Hi3536D V100 demo board.

1.2.10 Audio Interface

1.2.10.1 Features

For details about the features of the audio interfaces, see chapter 10 "Audio Interfaces" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.

1.2.10.2 Analog Audio Interface

Hi3536D V100 provides a group of dual-channel audio output interface (AC_OUTL/R).

- The analog power AVDD33_AC for the audio module must be isolated from the 3.3 V system power by using a 1 kΩ@100 MHz EMI bead.
- The filter capacitor connected to the AC_VREF pin must be greater than or equal to 10 μF. You are advised to add the 10 μF and 100 μF capacitors.
- You are advised to connect an audio amplifier and filtering circuit to the audio output pins AC_OUTL and AC_OUTR, which ensures excellent audio quality.
- ESD protection measures must be taken on the audio output signal lines to enhance the anti-interference capability of the interface.

1.2.10.3 I²S Interface

Hi3536D V100 supports an inter-IC sound (I^2S) interface, which can be multiplexed in two module pins (MII and JTAG). The I^2S signals multiplexed at the two positions have the same source and cannot be used at the same time. Note that the connection mode in master differs from that in slave modes, as shown in Figure 1-18 and Figure 1-19.

- It is recommended that Hi3536D V100 be set to the master mode when the I^2S interface is used.
- If Hi3536D V100 is set to the slave mode, the interconnected component must meet the I^2S interface specifications and the timing of the I^2S interface signals must meet the requirements of the setup/hold time. (For details, see chapter 10 "Audio Interfaces" in the latest-version *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.)

Figure 1-18 Connection mode when the Hi3536D V100 works in master mode

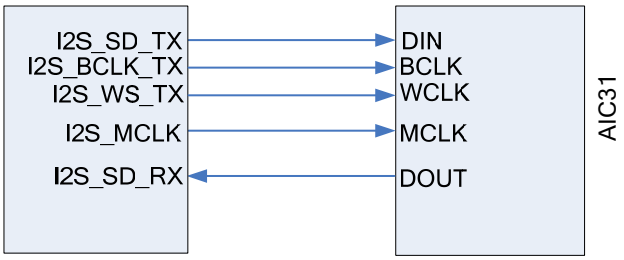
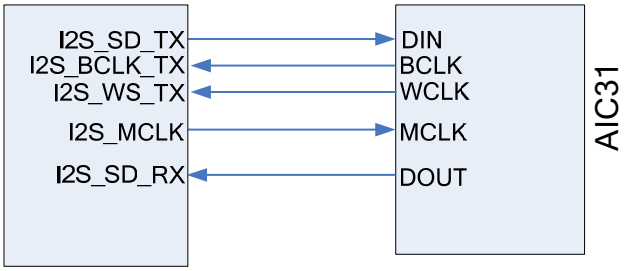


Figure 1-19 Connection mode when the Hi3536D V100 works in slave mode



Some I²S signals are connected in point-to-point topology. The design recommendations on matched resistors are as follows:

- A 33 Ω resistor needs to be connected in series to the MCLK signal close to the Hi3536D V100 end.
- A 33 Ω resistor needs to be connected in series to the BCLK_TX signal close to the signal source.

CAUTION

The I²S interface and analog audio CODEC share the same source.

1.2.11 HDMI Output Interface

1.2.11.1 Features

For details about the features of the HDMI interface, see chapter 9 "Video Interfaces" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.

1.2.11.2 Circuit Design

The Hi3536D V100 has an embedded HDMI PHY.

- The analog power AVDD_HDMITX of the HDMI must be isolated from the digital power DVDD_CORE by using an electromagnetic interference (EMI) bead, and the filter capacitor must be placed close to the pin. You are advised to use a 1 kΩ@100 MHz EMI bead. A 2.2 µF filter capacitor must be connected after the EMI bead.
- The analog power AVDD33_HDMITX of the HDMI must be isolated from the 3.3 V digital power by using a 1 kΩ@100 MHz EMI bead, and the 2.2 µF filter capacitor must be placed close to the pin.
- The HDMI signals must be protected by the electrostatic discharge (ESD) components that are placed close to the HDMI. The junction capacitance of the ESD component must be less than 0.8 pF.
- For the I²C circuit design of the HDMI output port, see the schematic diagram of the Hi3536D V100 demo board.
- For details, see the schematic diagram of the Hi3536D V100 demo board.

1.2.12 Analog DAC Interface

1.2.12.1 Features

For details about the features of the analog DAC interface, see chapter 9 "Video Interfaces" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.

1.2.12.2 Circuit Design

The Hi3536D V100 supports 1-channel video graphics array (VGA) output.

- The VGA signals VGA_R, VGA_G, and VGA_B must each connect to an external 75 Ω±1% pull-down resistor.
- The VGA signals VGA_HS and VGA_VS need to connect to 33-ohm serial resistors at the source end.
- The power supplies of the analog power AVDD33_VDAC and the digital power DVDD33_VDAC of the video digital-to-analog converter (VDAC) interface must be separated. The AVDD33_VDAC must be isolated from the 3.3 V digital power by using a 1 kΩ@100 MHz EMI bead, and a 2.2 μF filter capacitor must be placed close to the chip pin. The DVDD33_VDAC is supplied by the 3.3 V digital power supply, and a 1 μF filter capacitor is placed close to the chip pin.
- The VDAC_REXT pin must connect to a 12 kΩ±1% pull-down resistor, and then to the GND.
- For details about the VGA interface design, see the schematic diagram of the Hi3536D V100 demo board.
- ESD protection measures must be taken for VGA interfaces and ESD components must be placed close to VGA interfaces. The junction capacitance of the ESD component must be less than 1 pF.

1.3 Special Pins

1.3.1 Unused Pins During the Design

Table 1-9 describes how to process unused pins.

Table 1-9 Methods for processing unused pins

Module	Pin	Processing Method
JTAG	JTAG_EN	Connect this pin to a 4.7 kΩ pull-down resistor.
	JTAG_TCK JTAG_TMS JTAG_TRSTN JTAG_TDO JTAG_TDI	Set these pins as output GPIOs, which can be floated externally.

Module	Pin	Processing Method
SATA	AVDD_SATA	Connect this pin to the core power and ensure that this pin is always supplied with power.
	AVDD33_SATA	Connect this pin to the 3.3 V power and ensure that this pin is always supplied with power.
	SATA_TXxP/M	Float this pin.
	SATA_RXxP/M	Float this pin.
	SATA_LED_N	Set these pins as output GPIOs, which can be floated externally.
	AVSS_SATA	Connect this pin to the GND.
USB	AVDD33_USB	Connect this pin to the 3.3 V power and ensure that this pin is always supplied with power.
	USB2_DP0	Float these pins.
	USB2_DM0	
	USB2_DP1	
	USB2_DM1	
	USB2_PWRENX	Set these pins as output GPIOs, which can be floated externally.
	AVSS_USB	Connect this pin to the GND.
MII/RMII	MAC signals	Set these pins as output GPIOs, which can be floated externally.
RTC	AVDD_BAT	Float this pin.
	AVSS_RTC	Connect this pin to the GND.
	RTC_XIN, RTC_XOUT	Float these pins.
AVDD25_EFUSE	-	Must be floated.
TEST MODE	-	Float this pin.
VDAC	DVDD33_VDAC	Connect this pin to the 3.3 V power and ensure that this pin is always supplied with power.
	AVDD33_VDAC	Connect this pin to the 3.3 V power and ensure that this pin is always supplied with power.

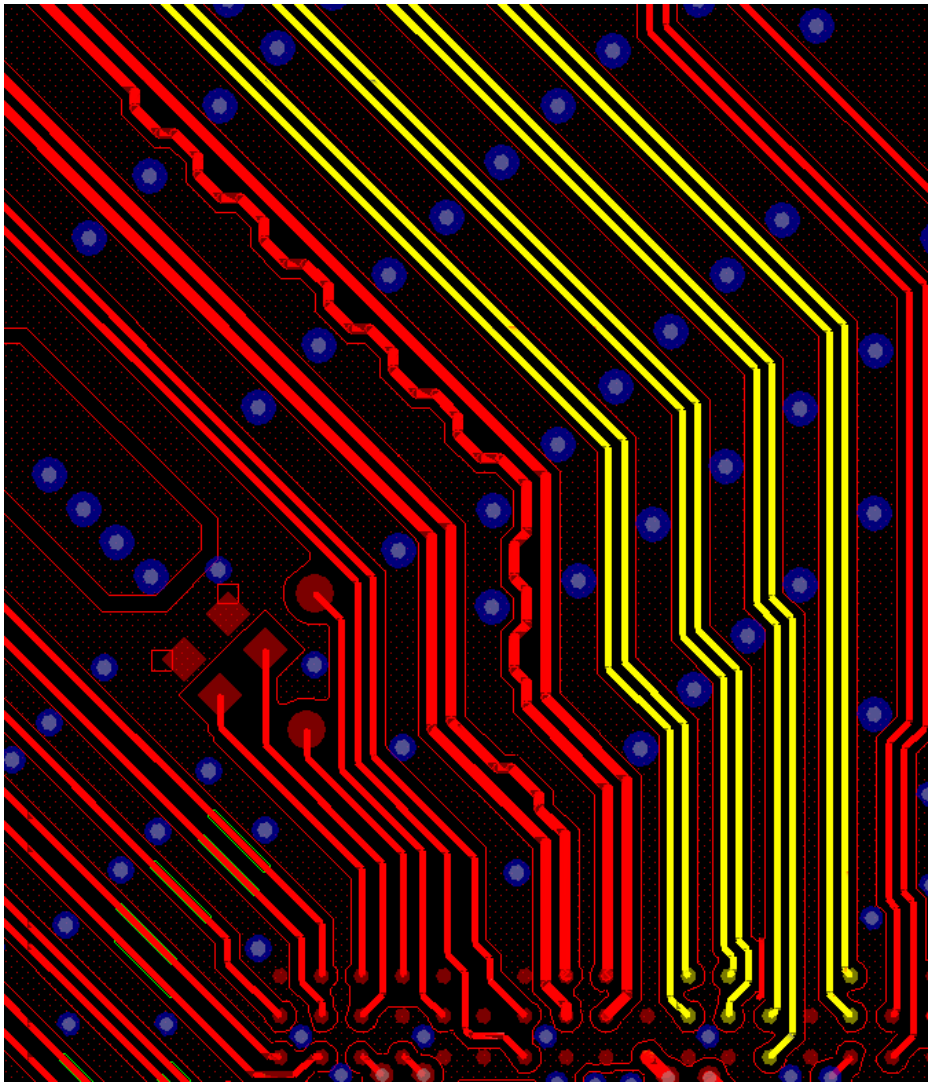
Module	Pin	Processing Method
	AVSS_VDAC	Connect this pin to the GND.
	DVSS_VDAC	Connect this pin to the GND.
	VGA_R	Float these pins.
	VGA_G	
	VGA_B	
	VGA_HS	Set these pins as output GPIOs, which can be floated externally.
	VGA_VS	
	VDAC_REXT	Connect this pin to a 12 kΩ±1% pull-down resistor.
HDMI	AVDD_HDMITX	Connect this pin to the core power and ensure that this pin is always supplied with power.
	AVDD33_HDMITX	Connect this pin to the 3.3 V power and ensure that this pin is always supplied with power.
	AVSS_HDMITX	Connect this pin to the GND.
	HDMI_TX0N/P	Float these pins.
	HDMI_TX1N/P	
	HDMI_TX2N/P	
	HDMI_TXCN/P	
	HDMI_HOTPLUG	Set these pins as output GPIOs, which can be floated externally.
	HDMI_SDA	
	HDMI_SCL	
FEPHY	AVDD33_FE	Connect this pin to the 3.3 V power and ensure that this pin is always supplied with power.
	ETH_MDI	Float these pins.
	ETH_LINK_LED	Set these pins as output GPIOs, which can be floated externally.
	ETH_SPD_LED	

2 PCB Design

2.1 Impedance Control

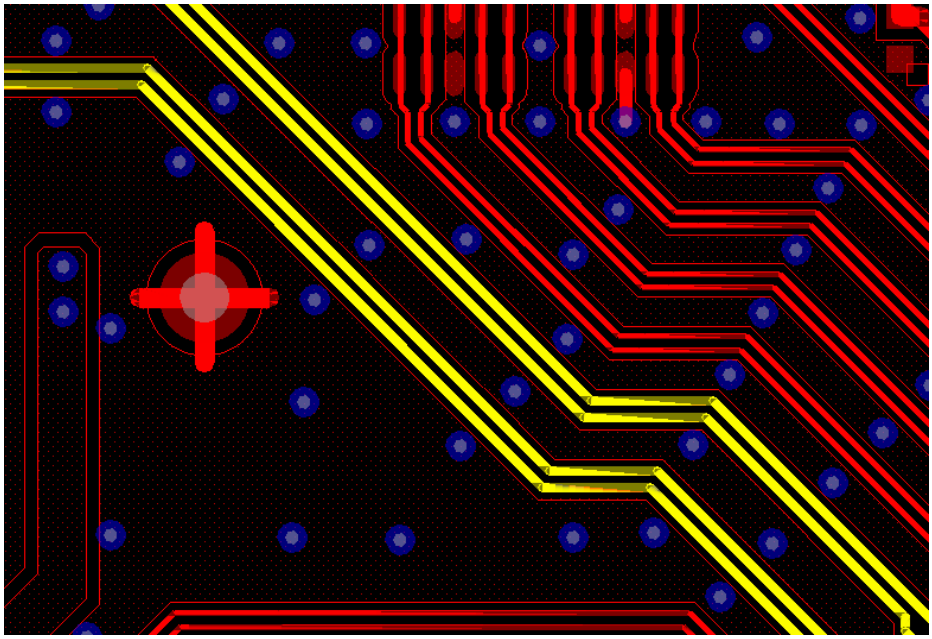
- The layout and routing of the small system must be the same as those of the Hi3536D V100 demo board.
- The impedance of the differential traces on a 2-layer PCB can be controlled by surrounding the differential traces with GND traces. The impedance of high-speed signal traces such as the SATA, HDMI, and network port differential traces must be 100 Ω. The width of the differential trace with 100 Ω impedance is 4.6 mils, the spacing between a pair of differential traces is 5 mils, and the space between a differential trace and GND copper is 5 mils. For a differential trace pair with 100 Ω impedance on a 2-layer PCB, the spacing between the GND copper sheet and one of the two differential traces is 5 mils, the width of this differential trace is 4.6 mils, the spacing between the two differential traces is 5 mils, the width of the other differential trace is 4.6 mils, and the spacing between the other differential trace and the GND copper sheet is 5 mils. Therefore, the trace width and spacing can be described as 5//4.6/5/4.6//5 in short. See Figure 2-1.

Figure 2-1 Impedance control for differential traces with 100 Ω impedance



- The impedance of USB differential traces must be 90 Ω. The width of the differential trace with 90 Ω impedance is 7.2 mils, the spacing between a pair of differential traces is 5 mils, and the space between a differential trace and GND copper is 5 mils. For a differential trace pair with 90 Ω impedance on a 2-layer PCB, the spacing between the GND copper sheet and one of the two differential traces is 5 mils, the width of this differential trace is 7.2 mils, the spacing between the two differential traces is 5 mils, the width of the other differential trace is 7.2 mils, and the spacing between the other differential trace and the GND copper sheet is 5 mils. Therefore, the trace width and spacing can be described as 5//4.6/5/4.6//5 in short. See Figure 2-2.

Figure 2-2 Impedance control for differential traces with 90 Ω impedance



2.2 Power Supplies and Filter Capacitors

The Hi3536D V100 uses the thin & fine-pitch ball grid array (TFBGA) package. It has 314 pins, its body size is 13 mm x 13 mm (0.51 in. x 0.51 in.), and its ball pitch is 0.65 mm (0.03 in.). For details about dimensions and the package, see chapter 2 "Hardware" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.

During the power channel design, you need to make sure that each power channel has sufficient width to ensure the current-carrying capability of the reflow channel in the GND layer and the power channel.

CAUTION

For the Hi3536D V100 power, ensure that the valid width of the power copper sheets for DVDD_CORE must be wide enough to support 2 A or higher current-carrying capability, and that for the DVDD_CPU must be wide enough to support 1 A or higher current-carrying capability.

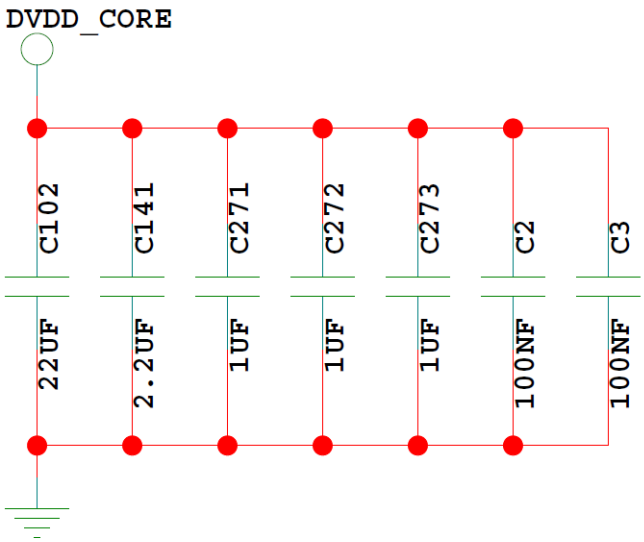
2.2.1 Core Power Supply

Type and Quantity of Filter Capacitors

The type, quantity, and layout of filter capacitors for the core power supply must be the same as those on the Hi3536D V100 demo board. For details, see the schematic diagram of the

Hi3536D V100 demo board. Figure 2-3 shows the type of filter capacitors for the core power supply.

Figure 2-3 Type of filter capacitors for the core power supply

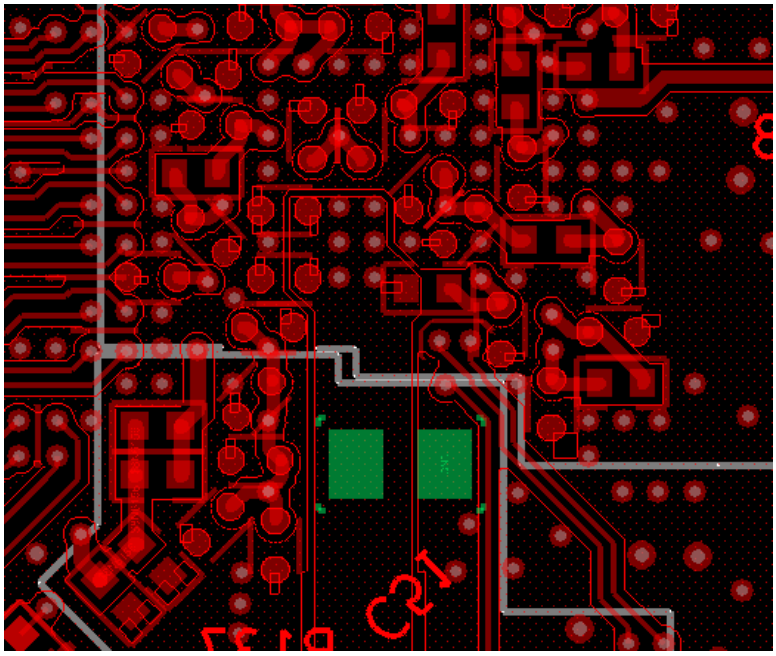


Routing Mode and Filter Capacitor Layout

The routing mode and filter capacitor layout for the core power supply must be the same as those on the Hi3536D V100 demo board.

The core power supply traces on copper sheets. A 22 μF filter capacitor must be placed at the chip entry of the core power, as shown in Figure 2-4

Figure 2-4 Filter capacitor places at the chip entry of the core power

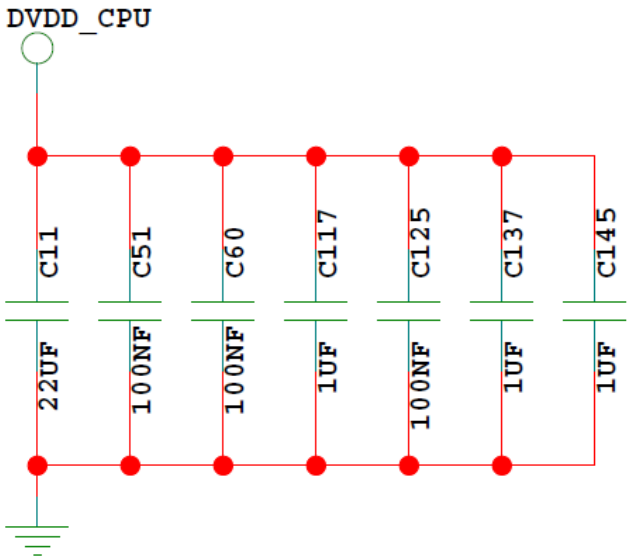


2.2.2 CPU Power Supply

Type and Quantity of Filter Capacitors

The type, quantity, and layout of filter capacitors for the core power supply must be the same as those on the Hi3536D V100 demo board. The recommended material of the filter capacitors is X7R. For details, see the schematic diagram of the Hi3536D V100 demo board. Figure 2-5 shows the type of filter capacitors for the CPU power supply.

Figure 2-5 Type of filter capacitors for the CPU power supply

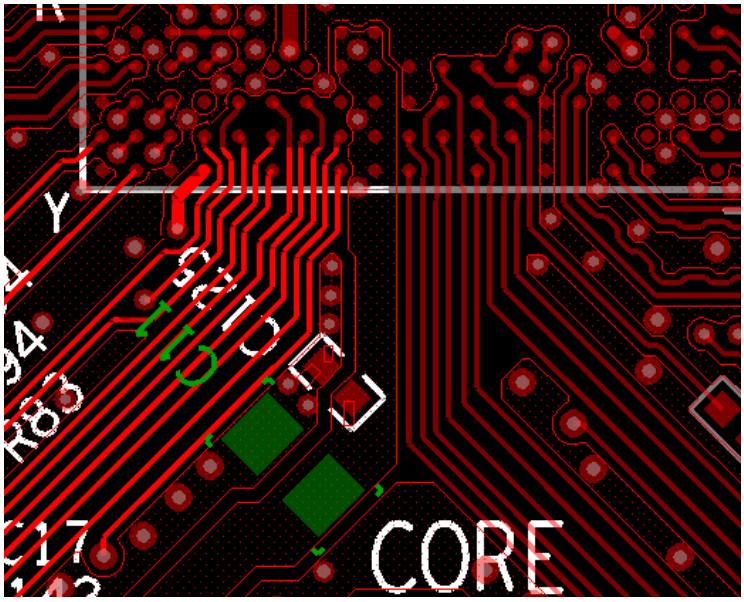


Routing Mode and Filter Capacitor Layout

The routing mode and filter capacitor layout for the CPU power supply must be the same as those on the Hi3536D V100 demo board.

The CPU power supply traces on copper sheets. A 22 μF filter capacitor must be placed at the chip entry of the CPU power, as shown in Figure 2-6.

Figure 2-6 Filter capacitor places at the chip entry of the CPU power

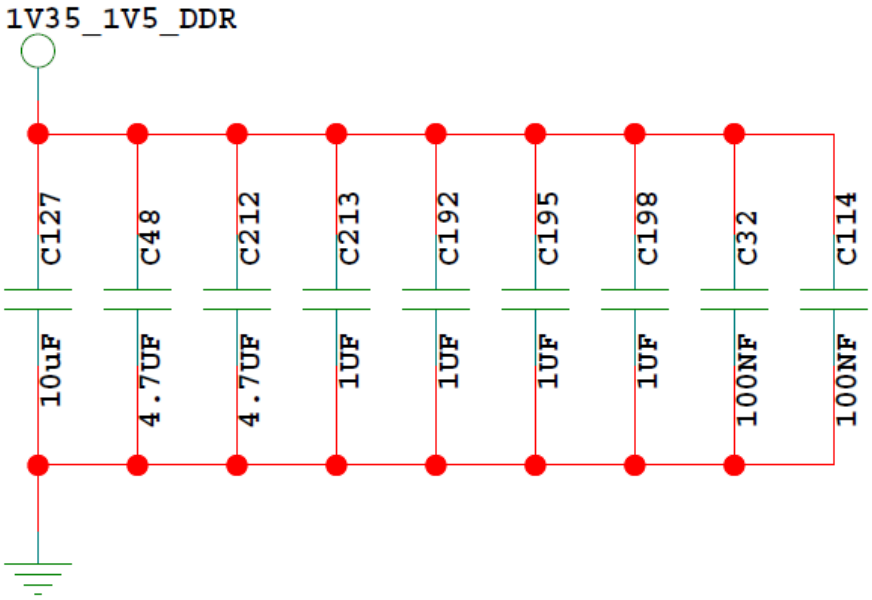


2.2.3 DDR Power Supply

Type and Quantity of Filter Capacitors

The type and quantity of filter capacitors for the DDR power supply must be the same as those on the Hi3536D V100 demo board. For details, see the schematic diagram of the Hi3536D V100 demo board. Figure 2-7 shows the type of filter capacitors for the DDR power supply.

Figure 2-7 Type of filter capacitors for the DDR power supply

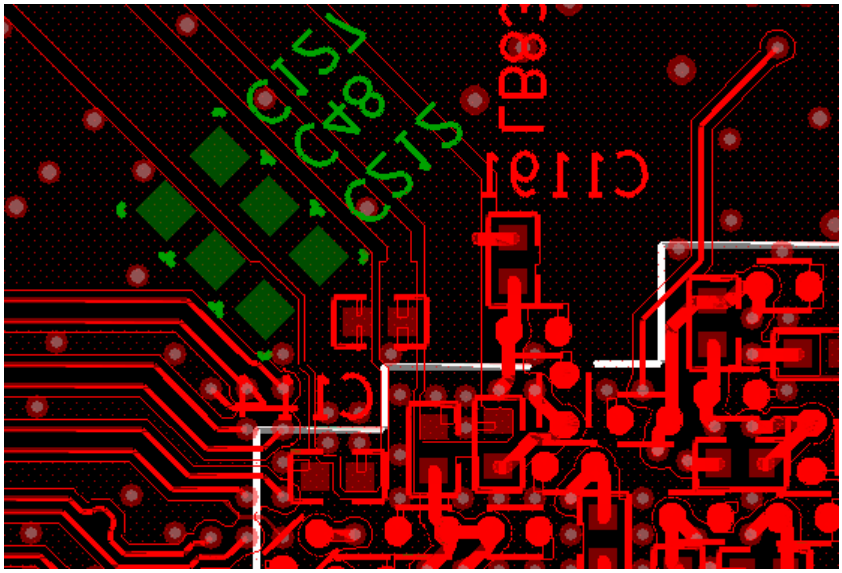


Routing Mode and Filter Capacitor Layout

The routing mode and filter capacitor layout for the DDR power supply must be the same as those on the Hi3536D V100 demo board.

The DDR power supply traces on copper sheets. A 10 µF and a 4.7 µF filter capacitors must be placed at the chip entry of the DDR power, as shown in Figure 2-8.

Figure 2-8 Filter capacitor places at the chip entry of the DDR power

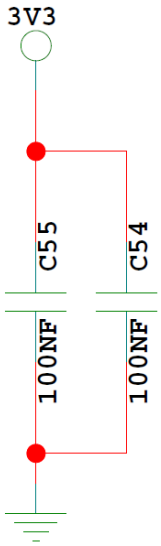


2.2.4 3.3 V Power Supply

Type and Quantity of Filter Capacitors

The type and quantity of filter capacitors for the 3.3 V power supply must be the same as those on the Hi3536D V100 demo board. For details, see the schematic diagram of the Hi3536D V100 demo board. Figure 2-9 shows the type of filter capacitors for the 3.3 V power supply.

Figure 2-9 Type of filter capacitors for the 3.3 V power supply



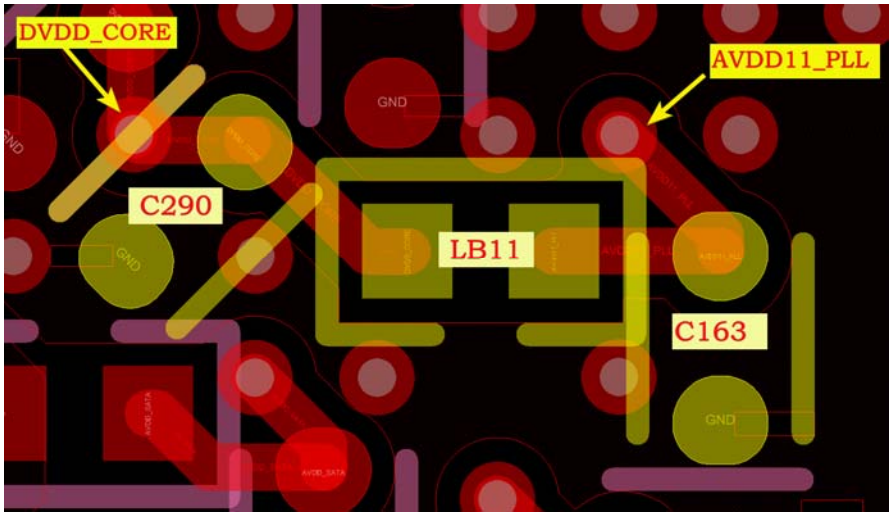
Routing Mode and Filter Capacitor Layout

The routing mode and filter capacitor layout for the 3.3 V power supply need to be designed by following the design on the Hi3536D V100 demo board.

2.3 PLL Circuit

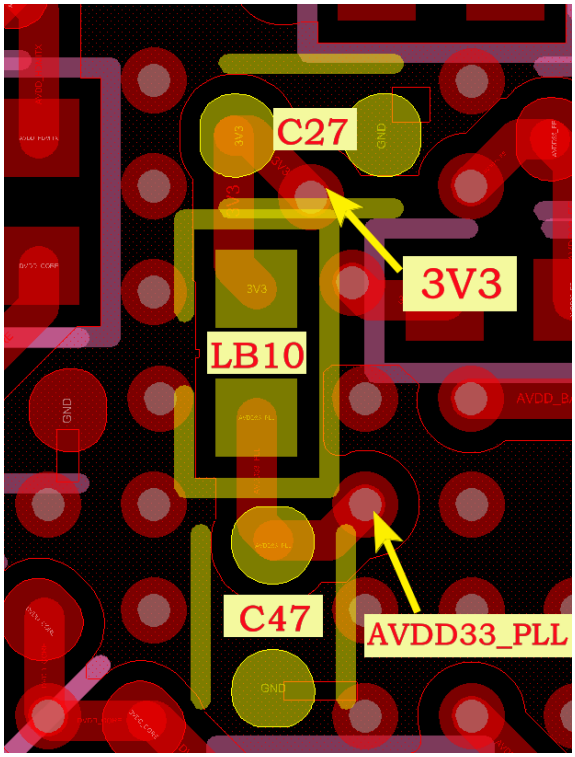
AVDD11_PLL is isolated from DVDD_CORE by using a 1 kΩ@100 MHz EMI bead. The power and surrounding capacitors form the π-shape filter circuit. The design must be the same as that of the Hi3536D V100 demo board. See Figure 2-10.

Figure 2-10 PCB layout of the π-type filter circuit for supplying power to AVDD11



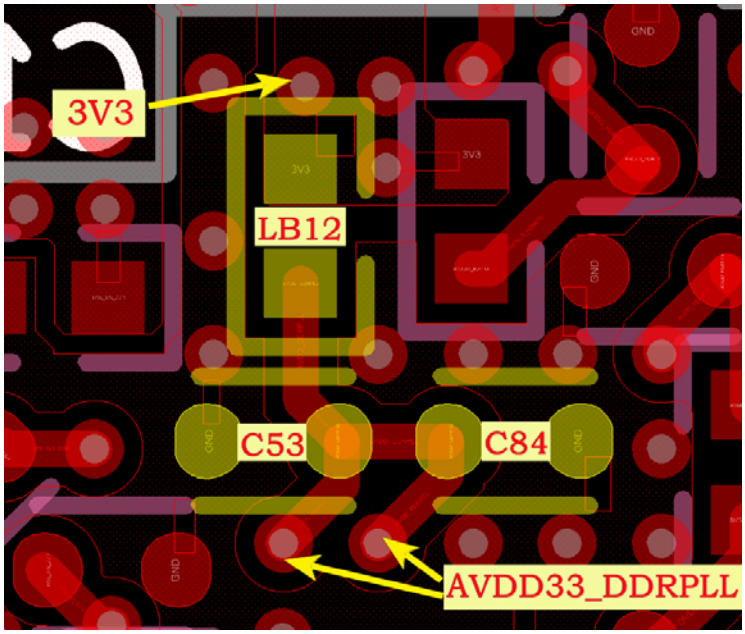
- AVDD33_PLL is isolated from the 3.3 V power by using a 1 kΩ@100 MHz EMI bead. The power and surrounding capacitors form the π-shape filter circuit. The design must be the same as that of the Hi3536D V100 demo board. See Figure 2-11.

Figure 2-11 The π-type filter circuit for supplying power to AVDD33_PLL



- AVDD33_DDRPLL is isolated from the 3.3 V power by using a 1 kΩ@100 MHz EMI bead. The filter capacitor of the AVDD33_DDRPLL must be placed close to the chip pin. The design must be the same as that of the Hi3536D V100 demo board. See Figure 2-12.

Figure 2-12 AVDD33_DDRPLL power supply filter circuit



2.4 Crystal Circuit

The traces of the crystal signals (Xin, Xout, RTC_XIN, and RTC_XOUT) must be surrounded with GND traces. Ensure that the reference plane of the signal traces is complete, and no high-speed signal is routed under the crystal circuit.

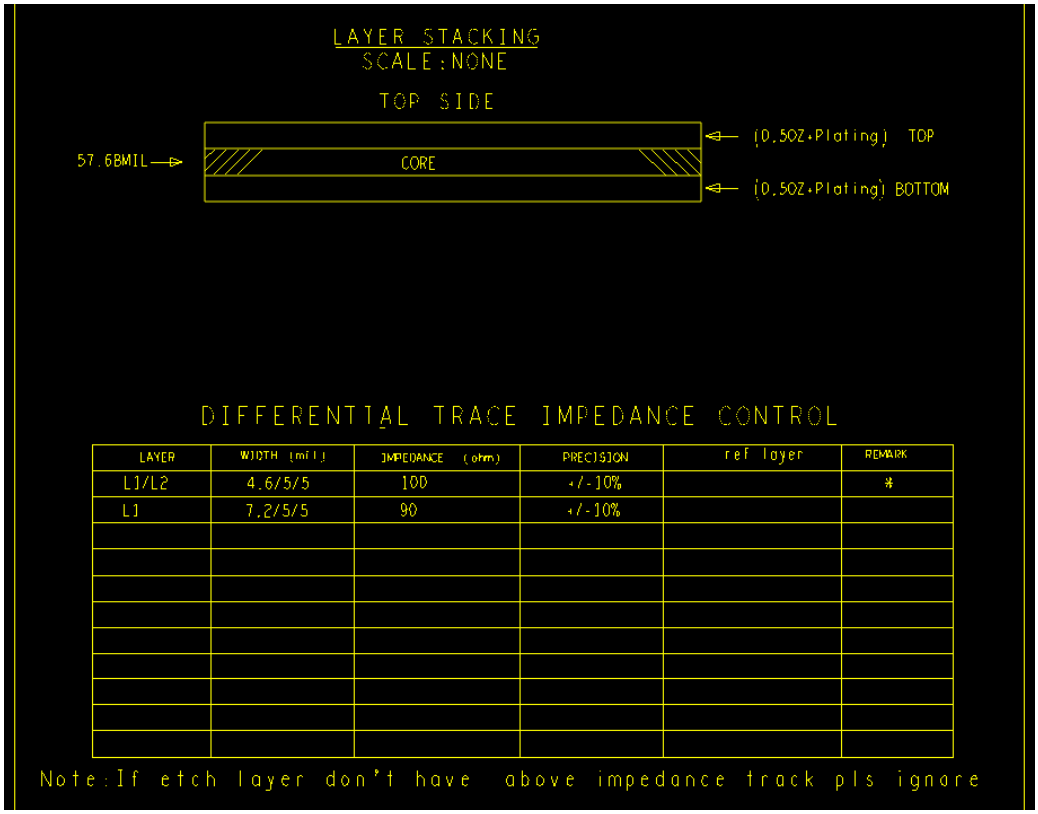
2.5 DDR3/DDR3L Interface

The design of the DDR SDRAM interface on the Hi3536D V100 must be the same as that on the Hi3536D V100 demo board. The design items include the trace width, trace spacing, trace length, method of surrounding signal traces with GND traces, layout of filter capacitors, and matching mode.

CAUTION

All DDR methods of surrounding signal traces with GND traces and matching modes must be completely the same as that on the Hi3536D V100 demo board.

Figure 2-13 Stack diagram of the 2-layer PCB (The thickness of the board is 1.6 mm.)



2.6 MAC Trace Routing

The design requirements on MAC signal traces are as follows:

- Avoid routing signal traces across power plane splits to maintain complete reference planes for signal traces.
- Ensure that the spacing between adjacent signal traces complies with the 3W rule.
- The differential signals from the Ethernet PHY chip to the transformer are MDI0+, MDI0-, MDI1+, and MDI1. The deviation of differential traces must fall within 5 mils and the differential impedance must be 100 Ω. For details about impedance control of the 2-layer PCB, see section 2.1 "Impedance Control."
- The maximum signal trace length of the MAC interface cannot exceed 8 inches.

2.7 FEPHY Trace Routing

The design requirements on FEPHY signal traces are as follows:

- Avoid routing signal traces across power plane splits to retain complete reference planes for signal traces.
- The ETH_MDI_AN or ETH_MDI_AP and ETH_MDI_BN or ETH_MDI_BP signals must connect to 1 Ω resistors in series. The resistor must be placed close to the network transformer.

- The traces in ETH_MDI_AN or ETH_MDI_AP and ETH_MDI_BN or ETH_MDI_BP differential signal traces must have the same length. The length deviation must fall within 5 mils. The total length of the differential traces must be less than 5 inches, and the differential impedance must be 100 Ω. For details about impedance control of the 2-layer PCB, see section 2.1 "Impedance Control."
- The MDI differential traces must be surrounded with GND traces.

2.8 USB 2.0 Circuit Design

Route the USB 2.0 signal traces on the PCB based on the following guidelines:

- The traces in each pair of differential signal traces must have the same length. The length deviation of each pair of differential signal traces must fall within ±5 mils. The total length of the differential traces of the USB 2.0 connecting to the USB connector must be less than 8 inches.
- The impedance of the USB 2.0 differential traces must be 90 Ω. For details about impedance control of the 2-layer PCB, see section 2.1 "Impedance Control."
- The USB differential traces must be surrounded with GND traces.
- Place the ESD component of the interface close to the USB socket.

2.9 SATA Trace Routing

The routing requirements on SATA traces are as follows:

- The differential impedance must fall within 100 Ω. For details about impedance control of the 2-layer PCB, see section 2.1 "Impedance Control."
- The SATA differential traces must be surrounded with GND traces.
- The 10 nF surface mounting technology (SMT) capacitor (using the 0402 package) connected to the differential signal line in series must be placed close to the SATA connector.
- The length deviation of each pair of differential signal traces must be less than or equal to 5 mils.
- Route traces at the top layer and never change the routing layer.
- It is recommended that the signal trace on the PCB be shorter than or equal to 5 inches.

2.10 HDMI Trace Routing

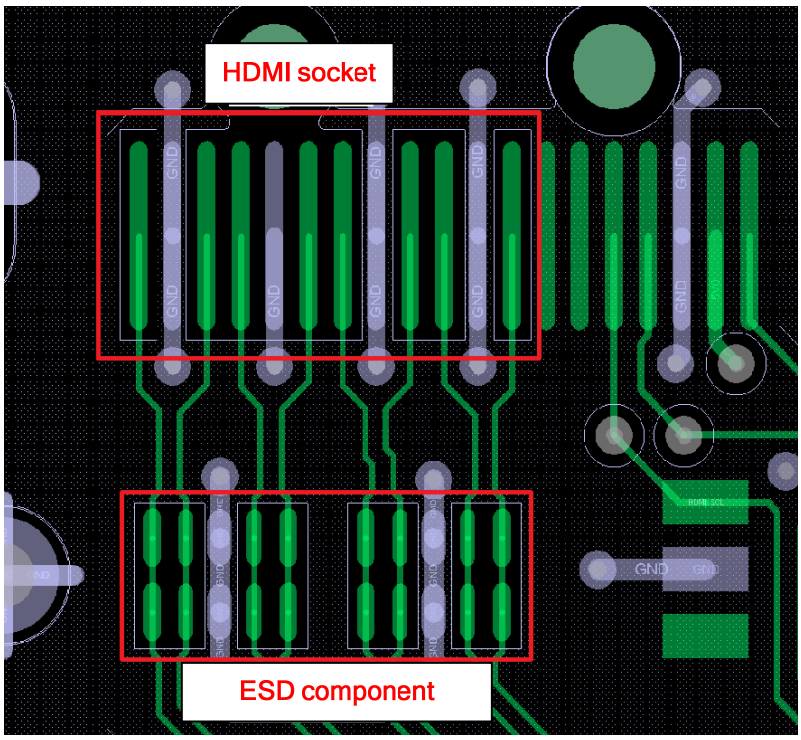
Route the HDMI traces based on the following guidelines:

- The differential impedance of the four pairs of HDMI differential signal traces must fall within 100 Ω. For details about impedance control of the 2-layer PCB, see section 2.1 "Impedance Control."
- The HDMI differential traces must be surrounded with GND traces.
- ESD components must be placed close to the HDMI connector.

- The length deviation of each pair of differential signal traces must be less than or equal to 40 mils. The zigzag trace cannot be used to make the trace length equal between the P and N signals. Instead, the impedance continuity has priority.
- The length of the four pairs of HDMI differential signal traces must be less than 5 inches.
- If a 4-layer or above PCB design is used, the reference GND at the second layer under the Hi3536D V100 pin position where the differential signals are fanned out, ESD components, and HDMI socket, must be voided. High-speed signals cannot be routed at the third layer under the position that is voided.

Figure 2-14 shows the diagram of the HDMI tracing 1 (the reference GND of the second layer of the HDMI socket and ESD component is void).

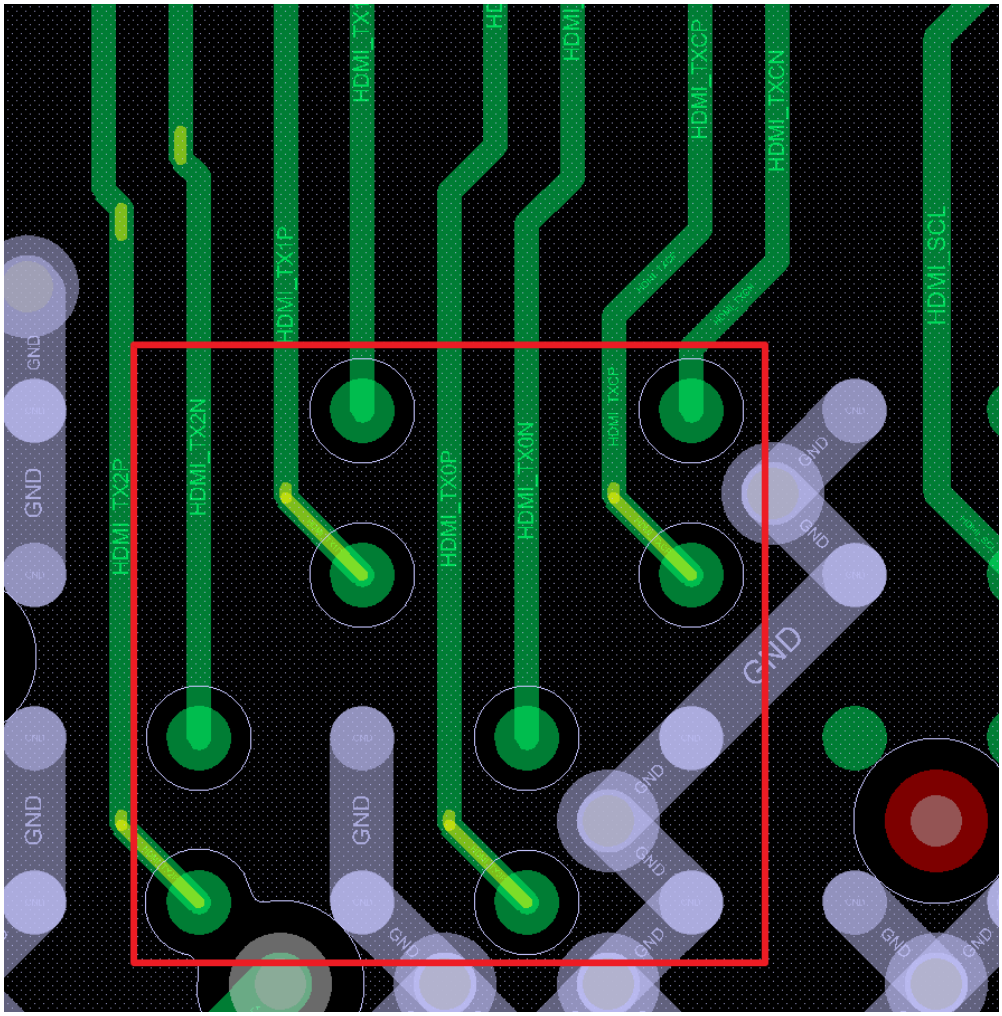
Figure 2-14 Diagram of the HDMI tracing 1



HDMI tracing diagram 2 (The reference GND of the second layer of the pin fanned out from the chip is void, as shown in Figure 2-15.)

The rule of hollowing the second GND layer of the pin fanned out from the HDMI chip is that the spacing between the pin and the edge of the hollowed area is 3–5 mils.

Figure 2-15 Diagram of the HDMI tracing 2



2.11 VDAC Trace Routing

The design requirements on the VDAC interface traces are as follows:

- The trace from the REXT configuration resistor to the master chip must be shorter than 300 mils.
- The analog output signal traces (such as VGA_R, VGA_G and VGA_B) must be surrounded with GND traces.
- The VDAC analog power supplies (AVDD33_VDAC) use an independent supply power, and the filter capacitor C1188 must be placed close to the power supply pin D17.
- Place the ESD component of the interface close to the VGA socket.

2.12 Analog Audio Circuit Design

- Place the capacitor connected to the AC_VREF pin close to the master chip, and ensure that the maximum spacing is less than or equal to 150 mils.
- Ensure that the signal traces of AC_OUTL and AC_OUTR are surrounded by GND traces and the GND vias between adjacent signal traces are evenly placed.
- The analog audio signal traces must refer to a clean GND.
- If the audio is outputted without passing through the power amplifier, place the ESD protection components of the audio output signal lines AC_OUTL and AC_OUTR close to the audio connector.

3 ESD Design

3.1 Background

As the chip performance and clock frequency become higher, the network video recorder (NVR) is more sensitive to external interference. Therefore, you need to pay special attention to the electrostatic discharge (ESD) design during the NVR design.

The ESD tests of the Hi3536D V100 are conducted complying with the JEDEC standard. The Hi3536D V100 has passed the ±2000 V test, which meets the industrial standards. However, you need to evaluate the board hardware design and NVR design based on your ESD test standards. This document provides the design recommendations and workarounds based on ESD design risks during the NVR design.

3.2 ESD Design

You need to emulate the following recommendations based on your standards and project experience:

- When designing the 24 MHz system clock, use the 4-pin surface mount device (SMD) crystal oscillator, and ensure that its two GND pins and the board GND are completely in contact to improve the anti-interference capability. Route other traces away from the crystal oscillator area, that is, never route traces under the crystal oscillator.
- It is recommended that the small system be kept away from the metal interfaces during the PCB component layout design. The farther the small system is away from the metal interfaces, the better the ESD performance of the entire system.
- Add ESD protective components for the peripheral interfaces (such as the audio/video input/output interfaces, USB port, Ethernet port, and alarm port) to improve their anti-interference capability.
- When the entire system is designed as a floating ground device, never use GND plane splits for the metal interfaces on the board.
- Use metal vias as the positioning holes of the board and connect them to the board GND, and ensure that the board GND is fully connected to the metal cover through the screw holes.
- When the NVR is designed as a grounding device, connect the metal cover to the earth, and connect the protective GND splits to the board digital GND in single-point mode. Ensure that the single point is far away from the circuits of the small system and close to the power connector of the NVR.

- It is recommended that the metal covers be used as the covers of the interface connectors (such as the HDMI and USB port with positioning screws or the RJ45 connector with a tab). Ensure that the connectors and the metal cover of the entire system are fully connected (using the conductive pillar or foam when necessary).

You need to evaluate the preceding recommendations based on your standards and project experience.

4 Recommendations on Chip Heat Dissipation Design

4.1 Operating Conditions

For details about the power consumption, temperature, and thermal resistance specifications, see section 2.5 "Electrical Specifications" in the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet*.

4.2 Reference Design for Heat Dissipation

Heat Sink Specifications

The thermal resistance of heat sink for the component or module must meet the following heat dissipation requirements:

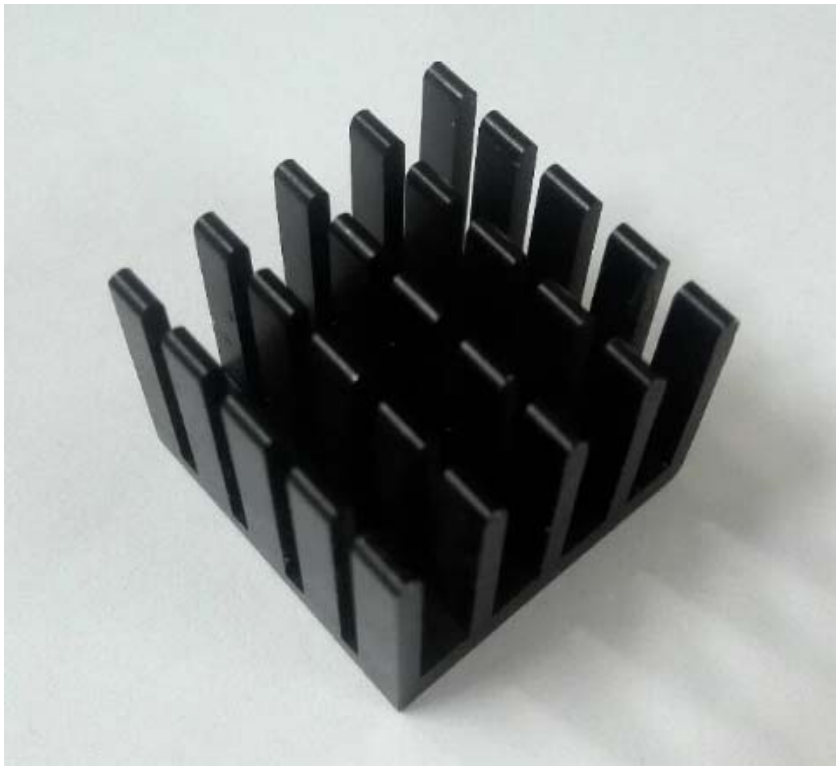
$\theta_{sa} < (T_{j\_max} - T_a)/P - \theta_{jc} - \theta_{cs}$

where

- $\mathbf{T_{j\_max}}$ indicates the upper limit for the junction temperature of a component.
- **P** indicates the dissipation power consumption.
- $\mathbf{T_a}$ indicates the maximum ambient temperature.
- $\boldsymbol{\theta_{jc}}$ indicates the junction-to-case thermal resistance of a component.
- $\boldsymbol{\theta_{cs}}$ indicates the interface thermal resistance between a component and a heat sink.

For the heat dissipation solution of the Hi3536D V100, users are advised to adopt the heat sink with the size no less than 20 mm x 20 mm x 15 mm (0.79 in. x 0.79 in. x 0.59 in.). The dimensions of the heat sink rack are 15 mm x 3 mm x 1 mm (0.59 in. x 0.12 in. x 0.04 in.). You are advised to paint the heat sink surface black, as shown in Figure 4-1. Ensure that the junction temperature of the chip is below 105°C by taking appropriate heat dissipation measures.

Figure 4-1 A group of heat sinks



NOTE

The preceding specifications are only for reference.

4.3 Reference Thermal Design for Circuits

4.3.1 Schematic Diagram

Power Supply

Ensure that the power conversion efficiency of the board is the highest as long as the power supplies are stable. That is, design the board power supplies optimally and use few LDO components with large voltage difference to reduce the heat produced during power conversion.

Low-Power Configurations for Idle Modules

If some modules such as USB and SATA are not used in actual applications of the Hi3536D V100, these modules should be set to the power-down mode or default state.

CAUTION

Enable clock gating for the Hi3536D V100 to reduce power consumption.

4.3.2 PCB

Component Layout

Lay out components based on the product architecture and heat dissipation design as follows:

- Place the components that consume much power and generate much heat evenly to avoid overheating of some parts and ensure the reliability and efficiency of components. You are advised to keep the Hi3536D V100 far away from power supplies.
- Design the product architecture optimally to ensure that the heat produced internally can be dissipated.
- If a chip has an exposed pad at the top layer of the PCB, the copper at the bottom layer should be exposed as well to facilitate heat dissipation.

Trace Routing

The heat dissipation design recommendations for routing traces are as follows:

- For the connection style of the vias under the Hi3536D V100, select the full connection style but not the thermal connection style to improve the board heat dissipation efficiency.
- The power and GND signals of the Hi3536D V100 are connected over copper sheets. When the signal current-carrying capability is ensured, more vias are recommended on copper sheets.

Increase the sizes of copper sheets under and around the components that produce much heat to ensure that PCB heat can be effectively dissipated. Place inductors and power chips in a distributed manner and increase the sizes of copper sheets around them.