Differences Between the SDKs of the Hi3536D V100 and Hi3536C V100

Issue 00B03

Date 2018-04-13

HiSilicon Technologies Co., Ltd.

Address: Huawei Industrial Base
Bantian, Longgang
Shenzhen 518129
People's Republic of China

Website: http://www.hisilicon.com

Email: support@hisilicon.com

About This Document

Purpose

Both the Hi3536D V100 and Hi3536C V100 are high-performance system-on-chips (SoCs) developed by HiSilicon. They apply to the multi-channel high-definition (HD) and D1 network video recorder (NVR). The software development kit (SDK) of the Hi3536D V100 is similar to that of the Hi3536C V100.

This document describes the differences between the Hi3536D V100 and Hi3536C V100 and the changes in SDK components and media processing application programming interfaces (APIs).

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3536D	V100

Intended Audience

This document is intended for:

- Technical support engineers
- Software development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B03 (2018-04-13)

This issue is the third draft release, which incorporates the following changes:

Chapter 1, Table 1-1 is modified.

Issue 00B02 (2017-11-20)

This issue is the second draft release, which incorporates the following changes:

The Hi3536D V100 CPU frequency is updated to 850 MHz.

Issue 00B01 (2017-09-08)

This issue is the first draft release.

Contents

Tables

1 Differences in the Specifications

As a high-performance NVR SoC, Hi3536D V100 has the similar specifications to Hi3536C V100.

Table 1-1 describes the specification differences between the Hi3536D V100 and the Hi3536C V100. For details of the specifications of the Hi3536D V100, see the *Hi3536D V100 H.265/H.264 Decoder Processor Data Sheet.*

Table 1-1 Differences in the specifications

Major Specifications	Hi3536D V100	Hi3536C V100
Processor	• ARM Cortex A7 @850 MHz - 32 KB L1 I-cache, 32 KB L1 D-cache - 128 KB L2 cache - NEON and FPU	• ARM Cortex A7 dual-core@1.3 GHz - 32 KB L1 I-cache, 32 KB L1 D-cache - 256 KB L2 cache - NEON and FPU
Video decoding	• H.265 Main Profile, Level 4.1 decoding • H.264 Baseline/Main/High Profile, Level 4.2 decoding • MJPEG/JPEG baseline decoding	• H.265 Main Profile, Level 5.0 decoding • H.264 Baseline/Main/High Profile, Level 5.1 decoding • MJPEG/JPEG baseline
Video encoding	JPEG Baseline encoding	• H.265 Main Profile, Level 4.0 encoding • H.264 Baseline/Main/High Profile, Level 4.1 encoding • MJPEG/JPEG baseline
Video encoding/decoding performance	• H.265/H.264/JPEG encoding and decoding of multiple streams - 4x1080p@25 fps H.265/H.264 decoding - 4x960p(1280*960)@30 fps H.265/H.264 decoding - 4x720p@30 fps JPEG decoding	• H.265/H.264/JPEG encoding and decoding of multiple streams - 4x 1080p@30 fps H.265/H.264 decoding - 8x 720p@30 fps H.265/H.264 decoding - 16x D1@30 fps H.265/H.264

Major Specifications	Hi3536D V100	Hi3536C V100
		decoding - 1x 1080p@ 30 fps H.265/H.264 encoding - 4x 1080p@30 fps JPEG decoding • Constant bit rate (CBR) mode, variable bit rate (VBR) mode, FIXQP mode, adaptive variable bit rate (AVBR) mode, and QpMap mode • Maximum 40 Mbit/s output bit rate • ROI encoding • Color-to-gray encoding
Intelligent video analysis	IVE not supported	IVE 2.0 integrated, supporting various intelligent analysis applications, including: - Motion detection - Video diagnosis - Perimeter defense
Video input (VI)	VI interface not supported	VI interface not supported
Video output (VO)	• VO interfaces - One HDMI 1.4b output interface - One VGA HD output interface - HDMI/VGA outputs from the same source, with the maximum output of 1080p@60 fps - One HD video layer and 16-picture output - One HD PIP layer - One ARGB1555 or ARGB8888 HD graphics layer - One hardware cursor layer in ARGB1555 or ARGB8888 format (configurable) with the maximum resolution of 256 x 256	• VO interfaces - One HDMI 1.4b output interface with the maximum output of 3840 x 2160@30 fps - One VGA HD output interface with the maximum output of 1080p@60 fps - Two independent HD output channels (DHD0 and DHD1), output over any HD interface (HDMI or VGA) - 36-picture output for DHD0, maximum output of 3840 x 2160@30 fps - 16-picture output for DHD1, maximum output of 1080p@60 fps - One CVBS SD output interface - Three full-screen GUI graphics layers in ARGB1555 or ARGB8888 format for two HD channels and one SD

Major Specifications	Hi3536D V100	Hi3536C V100
		channel - Two hardware cursor layers in ARGB1555 or ARGB8888 format (configurable) with the maximum resolution of 256 x 256
Video pre-processing (VPP)	No VPSS hardware module	Four physical channels with one supporting only scaling
VGS	• HSP supported • Video anti-flicker not supported	Video anti-flick processing
Audio interfaces	• Two unidirectional I²S/PCM interfaces - One input interface, supporting dual-channel input - One output interface, supporting dual-channel output - 16-bit audio inputs and outputs • Integrated with Audio DAC - 48 kHz, 44.1 kHz, 32 kHz sampling rates - Dual-audio channel line-out output	• Two unidirectional I²S/PCM interfaces - One input interface, supporting 16-channel multiplexed input - One output interface, supporting dual-channel output - 16-bit audio inputs and outputs
Memory interface	• One 16-bit DDR3/DDR3L SDRAM interface - Maximum frequency of 800 MHz - ODT - Maximum capacity of 512 MB - Automatic power consumption control • SPI NOR/NAND flash interface - 1-/2-/4-wire SPI NOR/NAND flash - Two CSs, connected to different types of flash memories - Maximum capacity of 64 MB for each CS (for the SPI NOR flash) - Maximum capacity of 512 MB for each CS (for the SPI NAND flash) - 2 KB/4 KB page size (for the SPI NAND flash) - 8-bit/1 KB, 16-bit/1 KB, 24-bit/1 KB, or 28-bit/1 KB ECC (for the SPI NAND flash) • Embedded 4 KB BOOTROM	• One 16-bit DDR3 SDRAM interface - Maximum frequency of 933 MHz - ODT - Maximum capacity of 1 GB - Automatic power consumption control • SPI NOR/NAND flash interface - 1-/2-/4-wire SPI NOR/NAND flash - Two CSs, connected to different types of flash memories - Maximum capacity of 64 MB for each CS (for the SPI NOR flash) - Maximum capacity of 512 MB for each CS (for the SPI NAND flash) - 2 KB/4 KB page size (for the SPI NAND flash) - 8-bit/1 KB or 24-bit/1 KB

Major Specifications	Hi3536D V100	Hi3536C V100
		ECC (for the SPI NAND flash) • Embedded 4 KB BOOTROM and 16 KB SRAM
Peripheral interface	• One SATA 2.0 interface - PM - eSATA • Two USB 2.0 host ports, supporting the hub • Three UART interfaces, one of which supporting four wires • One IR interface • One I^2C interface • Multiple GPIO interfaces	• Two SATA 3.0 interfaces - PM - eSATA • Two USB 2.0 host ports, supporting the hub • Three UART interfaces, one of which supporting four wires • One SPI, supporting two CSs • One IR interface • One I^2C interface • Multiple GPIO interfaces
Network interface	• One fast Ethernet (FE) interface - Integrated with FE PHY - PHY, RMII, and MII modes - 10/100 Mbit/s half-duplex or full-duplex - TSO for reducing the CPU usage	• Two gigabit Ethernet ports - RGMII, RMII, and MII modes - 10/100 Mbit/s half-duplex or full-duplex - 1000 Mbit/s full-duplex - TSO for reducing the CPU usage
Security engine	AES, DES, and 3DES algorithms implemented by hardware	AES, DES, and 3DES algorithms implemented by hardware
Various boot modes	• Booting from the BOOTROM • Booting from the SPI NOR flash • Booting from the SPI NAND flash	• Booting from the BOOTROM • Booting from the SPI NOR flash • Booting from the SPI NAND flash

2 Differences in the SDK Components

The SDK of the Hi3536D V100 is similar to that of the Hi3536C V100.

Table 2-1 describes the differences between the SDK components of the Hi3536D V100 and the Hi3536C V100.

Table 2-1 Differences in the SDK components

SDK Component	Hi3536D V100	Hi3536C V100
lib	uClibc-0.9. 33.2 glibc-2.24	uClibc-0.9. 33.2 glibc-2.20-2012.09
Tool chain	arm-hisiv510-linux- arm-hisiv610-linux- gcc 6.2	arm-hisiv500-linux- arm-hisiv600-linux- gcc 4.9
Linux kernel	Linux-4.9.y, single-core A7, NEON, and VFP supported	Linux-3.18.y, dual-core A7, NEON, and VFP supported
File system	busybox-1.26.2.tgz	busybox-1.20.2.tgz

3 Differences in the Media Processing APIs

The APIs of the Hi3536D V100 are similar to those of the Hi3536C V100. Table 3-1 describes the differences of the media processing APIs between the Hi3536D V100 and Hi3536C V100. For details, see the *HiMPP V3.0 Media Processing Software Development Reference*.

Table 3-1 Differences in the MPIs

Module	Change of the Hi3536D V100 Compared with the Hi3536C V100	Change Description
System control	Same as the Hi3536C V100	-
VI	-	-
VDEC	Same as the Hi3536C V100	-
VPSS	Functions modified	The Hi3536D V100 does not have the VPSS logic. The VGS is invoked to implement related functions in the software.
VENC	Functions modified	The VENC module does not support H.264, H.265, or MJPEG encoding.
VO	Same as the Hi3536C V100	-
Frame buffer	Same as the Hi3536C V100	-
Motion detection	Deleted	The Hi3536D V100 does not support this module.
TDE	Same as the Hi3536C V100	-
Region	Same as the Hi3536C V100	-

Module	Change of the Hi3536D V100 Compared with the Hi3536C V100	Change Description
VGS	Same as the Hi3536C V100	-
Audio	Functions added	The Hi3536D V100 supports the embedded DAC.
PCIV	-	-
IVE	Deleted	The Hi3536D V100 does not support this module.