TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

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2º Laboratory Report

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Contents

1 Introduction

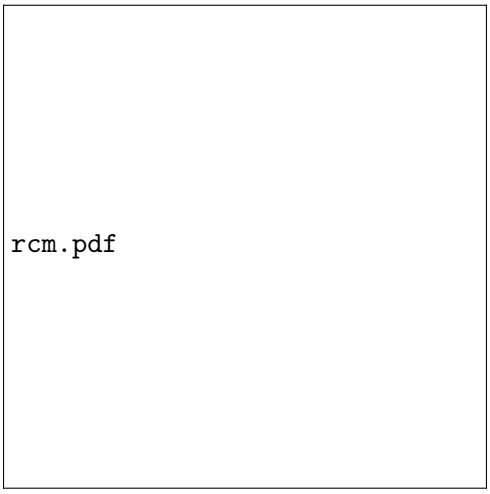

Figure 1: Nodal representation of the circuit.

Name	Value
§R(1)	1.015259 K
§R(2)	2.090689 K
§R(3)	3.108356 K
§R(4)	4.101243 K
§R(5)	3.033480 K
§R(6)	2.009605 K
§R(7)	1.005573 K
!!C	1.015319 u
Vs	5.026261
£Kb	7.161103 m
§Kd	8.185741 K

Table 1: Constants provided by Python. A variable preceded by !! is of type *capacitance* and expressed in Farad ;a variable preceded by § is of type *resistence* and expressed in Ohm;a variable preceded by £ is of type *conductance* and expressed in Siemens; other variables are of type *voltage* and expressed in Volt.

The objective of this laboratory assignment is to chose the architecture of the envelope detector and voltage regulator. By doing this we will design a AC/DC converter and bear in mind that cost is a very important factor and we should make the circuit as budget friendly as possible while keeping a good or great efficiency. The circuit can be seen in Figure **??**.

In section 2, a theoretical analysis of the circuit is presented. In section 5, the circuit's simulation analysis results are expressed in graphics and commented. Finally, in section 6, we will compare the simulation and theoretical values and in this way conclude our study.

2 Theoretical Analysis

In this section, the circuit shown in Figure **??** is analysed theoretically. The key equations for all the theoretical analysis ar shown below: To compute 't_on

$$V_s/n(t) * C * w * sin(w * t_off) = (1/R1) * (V_s/n) * cos(w * t_off) + I_x * (e^{12/eta*Vt*k} - 1) \quad (1)$$

In which $i_D = i_R + i_C$
To compute t_on we use the equation

$$(V_s/n) * cos(w * t_off) = -(V_s/n) * cos(w * t_off) * (e^{(-1/R_eq*C)*(t_on - T_off)} \quad (2)$$

2.1 envelope detector

In this section we will start by analyzing the envelope detector, where t varies from 0 to 20 ms, by using the main equations above.

$$V_6n(t) = V_x e^{-(t)/CR_eq} \quad (3)$$

Using octave we obtain the following table:

Name	Value [mA]

Table 2

We can now plot the graph of the solution for t raging from 0 to 20 ms:

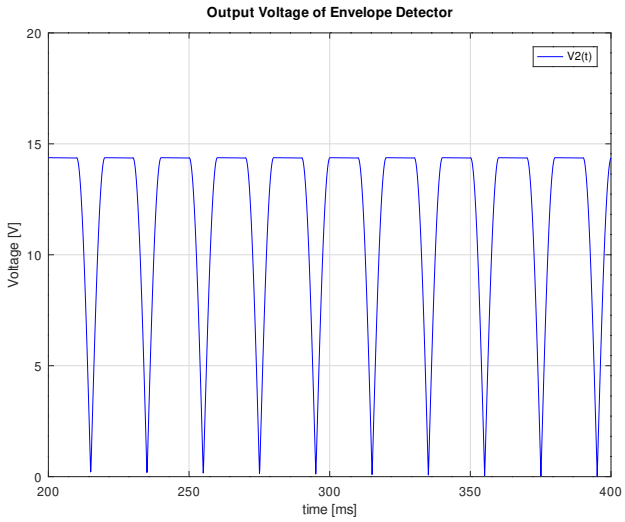

Figure 2: envelop detector output

2.2 voltage regulator

The voltage regulator theoretical analysis of this circuit, like with the envelope detector is done with the help of a key equation above.

$$V_6 n(t) = V_x e^{-(t)/CR_e q} \tag{4}$$

After this, we can plot the following graphic:

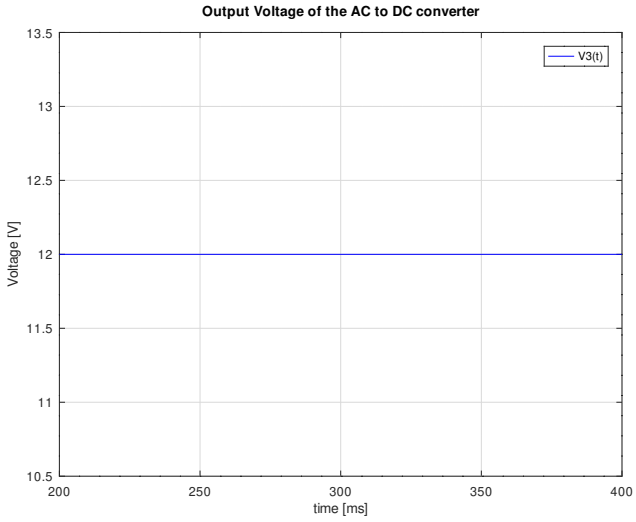

Figure 3: Voltage regulator output

2.3 Voltage regulator deviation

Lastly, we will analyze the voltage regulator deviation plot, which like in the error subsection of the simulation analysis will give us the deviation in our results.

Considering:

$$V_c(t) = V_6(t) - V_8(t) \tag{5}$$

The graphics of the voltage deviation is:

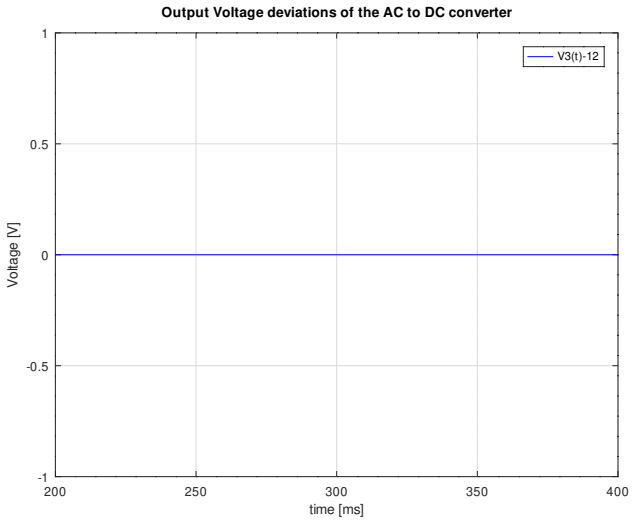

Figure 4: Voltage deviation plot

3 Simulation Analysis

the simulated values we obtained are represented in the graphics present in subsections below. We will add some comments to the results and in the conclusion we will compare them to the theoretical analysis.

3.1 Envelope detector and voltage regulator

First, in order to compute the envelope detector and voltage regulator response . The graphic in figure ?? was obtained by executing a transient analysis, with t ranging from 100 to 300 ms.

By analyzing the graphics below, which corresponds to the envelope detector and voltage regulator respectively, we can see that the graphics can be summarized in a sinusoidal equation like the ones below:

Figure 5: envelope detector output

Figure 6: voltage regulator output

3.2 error

On this last graphic, we can see the standard deviation of the value of 12V from the average voltage and the errors between the simulation and theoretical values.

Figure 7: error plot

4 Conclusion

4.1 V_s is constant an non-null

In conclusion, the values we obtained in the simulation agree with the theoretical values obtained for the dc voltage source V_s, showing negligible errors. These are excellent results which show that the methods we used are legitimate, as expected, and can be used by the simulation program to simulate the circuit.

Nevertheless, the simulator and methods used might produce solutions, which may not occur in a real circuit due to various factors including the Joule effect in the cables that connect the components in the circuit, and other random and systematic errors, which compromise the precision and accuracy of the results. However, the results might still be a good approximation of the real values, which can be verified by analyzing a real representation of the circuit. It-s also safe to say that while some relative errors were very close to zero, or in some cases even zero, this is due to approximations made by the simulator (ngspice) and octave.

Name	Value [mA]
V(1)	5.026261
V(2)	4.779742
V(3)	4.248215
V(4)	0.000000
V(5)	4.815244
V(6)	5.586461
V(7)	-1.871505
V(8)	-2.807975

Table 3: Theoretical voltage results obtained with octave

Name	Value [mA]
@c[i]	0.000000e+00
@g1[i]	-2.54235e-04
@r1[i]	2.428134e-04
@r2[i]	-2.54235e-04
@r3[i]	-1.14215e-05
@r4[i]	1.174094e-03
@r5[i]	-2.54235e-04
@r6[i]	9.312805e-04
@r7[i]	9.312805e-04
v(1)	5.026261e+00
v(2)	4.779742e+00
v(3)	4.248216e+00
v(4)	4.815245e+00
v(5)	5.586461e+00
v(6)	-1.87151e+00
v(7)	-2.80798e+00
v(8)	-1.87151e+00

Table 4: Simulation results obtained with Ngspice

4.2 $V_s = 0$ and capacitor are replaced by the voltage source

By analysing the tables below, we can see a pattern of repeated voltages, whose order of magnitude is around $10^(- 15)$:

Name	Value [mA]
V(1)	0.000000
V(2)	0.000000
V(3)	0.000000
V(4)	0.000000
V(5)	0.000000
V(6)	8.394437
V(7)	-0.000000
V(8)	-0.000000

Table 5: Theoretical voltage results obtained with octave

Name	Value [mA]
@g1[i]	2.140176e-18
@r1[i]	-2.04403e-18
@r2[i]	2.140176e-18
@r3[i]	9.614768e-20
@r4[i]	4.331265e-19
@r5[i]	-2.76726e-03
@r6[i]	4.336809e-19
@r7[i]	8.998149e-19
v(1)	0.000000e+00
v(2)	2.075218e-15
v(3)	6.549660e-15
v(4)	1.776357e-15
v(5)	8.394437e+00
v(6)	-8.71527e-16
v(7)	-1.77636e-15
v(8)	-8.71527e-16

Table 6: Simulation results obtained with Ngspice