# Quiz - 2

**Due** Feb 25 at 11:59pm **Points** 100 **Questions** 25 **Time Limit** None
**Allowed Attempts** Unlimited

Take the Quiz Again

## Attempt History

| | Attempt | Time | Score |
|---|---|---|---|
| **KEPT** | Attempt 6 | 3 minutes | 100 out of 100 |
| **LATEST** | Attempt 6 | 3 minutes | 100 out of 100 |
| | Attempt 5 | 2 minutes | 96 out of 100 |
| | Attempt 4 | 6 minutes | 92 out of 100 |
| | Attempt 3 | 22 minutes | 88 out of 100 |
| | Attempt 2 | 23 minutes | 64 out of 100 |
| | Attempt 1 | 72 minutes | 52 out of 100 |

Correct answers are hidden.

Score for this attempt: **100** out of 100
Submitted Feb 24 at 11:10pm
This attempt took 3 minutes.

### Question 1 — 4 / 4 pts

When a voltage of 0V (Low) is applied to the Gate of a PMOS transistor, the transistor is:

- OFF
- Not enough information
- ON

### Question 2 — 4 / 4 pts

Tri-state inverter gate has:

- 2 NMOS transistors in the Pull Up Network

- 2 PMOS transistors in the Pull-Down Network
- 2 NMOS transistors in series and 2 PMOS transistors in series
- 2 NMOS transistors in series and 2 PMOS transistors in parallel

## Question 3

**4 / 4 pts**

The amount of drain current ($I_{DS}$) depends on:

1) Gate to Source voltage (Vgs)
2) Drain to Source voltage (Vds)
3) Bulk to Source voltage (Vsb)
4) Threshold voltage (Vth)
5) Dimensions of MOSFET (W/L)

- Only 1st, 2nd and 3rd options
- All of the mentioned
- Only 1st option
- Only 5th option

## Question 4

**4 / 4 pts**

When a voltage of 0V (Low) is applied to the Gate of an NMOS transistor, the transistor is:

- Not enough information
- OFF
- ON

## Question 5

**4 / 4 pts**

**W**hich of the following will reduce the power dissipated by a CMOS inverter?

- Decrease the supply voltage

- Increase how often it switches
- Increase the MOSFET's "off current"
- None of these
- Increase the load capacitance

## Question 6

**4 / 4 pts**

The drain current $I_{DS}$

- Depends inversely on (Vgs - Vth) in the triode region
- None of the mentioned
- Depends linearly on (Vgs - Vth ) in the saturation region
- (•) Depends on the square of (Vgs - Vth) in the saturation region

## Question 7

**4 / 4 pts**

When $V_{gs}$ reaches to threshold voltage drain current is:

- min
- 10 milli Amps
- max
- (•) close to 0

## Question 8

**4 / 4 pts**

In the Cadence assignments, what tool is used in the DRC and LVS steps of Layout Design.

- Quantus

- Diva
- Spectre
- Assura

## Question 9

**4 / 4 pts**

When the threshold voltage is more, the (sub threshold) leakage current will be

- more
- less

Increasing the threshold voltage, leads to small leakage current when turned off and reduces current flow when turned on.

- not enough information to determine
- none of the mentioned

## Question 10

**4 / 4 pts**

CMOS inverter transfer curve has _____ regions of operation

- three
- four
- two
- five

## Question 11

**4 / 4 pts**

A MOSFET biased in saturation, can act as a good:

- inverter
- buffer
- current source
- voltage source

## Question 12

**4 / 4 pts**

A 2:1 MUX is implemented using transmission gates. How many PMOS transistors does it use? _____.

- 1
- 4
- 3
- 5

## Question 13

**4 / 4 pts**

Because of short channel effect, the _____ of a MOSFET increases with increasing values of L. (Hint: Ids decreases).

- L
- mobility
- W
- Vth

## Question 14

**4 / 4 pts**

When a voltage of 2V is applied between the G and S of an NMOS, the transistor is: (assume Vt = 1 V)

- Not enough information

- OFF
- ON

## Question 15

**4 / 4 pts**

When a voltage of -2V is applied to between the G and S of a PMOS transistor, the transistor is (Assume |Vtp| = 1V):

- Not enough information
- ON
- OFF

## Question 16

**4 / 4 pts**

Pick the most appropriate statement from below. A 3-input NOR gate has:

- (d) 3 NMOS transistors in series and 3 PMOS transistors in parallel
- (b) 3 PMOS transistors in the Pull-Down Network
- (e) Both (a) and (c) are true
- (c) 3 NMOS transistors in parallel and 3 PMOS transistors in series
- (a) 3 NMOS transistors in the Pull-Down Network
- (f) Both (b) and (d) are true

## Question 17

**4 / 4 pts**

Which of the following is true about PMOS transistor?

- It provides a good ‘1’
- It uses p-well

- It provides a good '0'
- It has positive threshold voltage Vtp

## Question 18

**4 / 4 pts**

Input dependent phase shift is brought about by which of the following transistor non–idealities?

- (•) Non–zero ON–resistance
- Channel–charge injection
- Negative–bias Temperature Instability (NBTI)
- Clock–feed through

## Question 19

**4 / 4 pts**

Which of the following Capacitances is fundamental to the operation of a MOS transistor?

- (•) Oxide Capacitance between Gate and Channel
- Depletion capacitance between Drain and Bulk
- Overlap Capacitance between Gate and Source/Drain
- Depletion capacitance between Source and Bulk

## Question 20

**4 / 4 pts**

In Figure – 1 shown below, which capacitance shorts the input to the output at high frequencies?

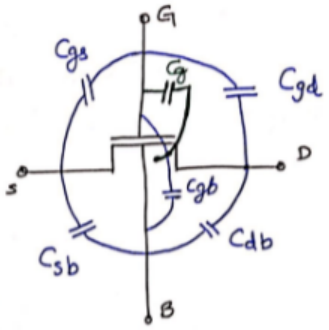


**Figure – 1. MOSFET Capacitances**

- Csb
- Cdb
- Cgs
- Cgd

## Question 21

**4 / 4 pts**

Shown below are transistor higher-order effects. Identify a lateral field effect from below.

- c. Body effect
- b. Mobility degradation
- d. Velocity saturation
- a. Subthreshold conduction

## Question 22

**4 / 4 pts**

Shown below are transistor higher-order effects. Identify a vertical field effect from below.

- b. Mobility degradation
- d. Velocity saturation
- c. Body effect
- a. Subthreshold conduction

## Question 23

**4 / 4 pts**

"Pinch-off" occurs in which region of operation?

- [x] Saturation
- [ ] Subthreshold
- [ ] Linear
- [ ] All the regions

## Question 24

**4 / 4 pts**

By definition, the time from input to rising output crossing VDD/2 is:

- [ ] Rising Contamination delay (tcdr)
- [ ] Setup – time
- [ ] Rise Time - (tr)
- [x] Rising Propagation Delay (tpdr)

## Question 25

**4 / 4 pts**

Which of the following effects will cause current through a MOSFET to be higher than expected?

- [ ] None of these
- [ ] Velocity saturation
- [x] Drain induced barrier lowering
- [ ] Body effect
- [ ] Mobility degradation

Quiz Score: **100** out of 100