This attempt took 2 minutes.

Question 1

5 / 5 pts

Modern FPGAs often use flash and/or SRAM memory to allow the chip to be reconfigured multiple times.

- (●) True
- ( ) False

Question 2

5 / 5 pts

Which of the following phenomenon can be useful in programming FLASH memories?

- (●) Hot - Carrier Injection
- ( ) Channel-charge Injection
- ( ) Clock-feed through
- ( ) Channel Length Modulation

Question 3

5 / 5 pts

Which cell is non-volatile?

- ( ) two-transistor dynamic cell

- NV RAM cell
- one transistor dynamic cell
- four transistor dynamic cell

Question 4

5 / 5 pts

Static RAM uses ____ transistors

- 6
- 5
- 8
- 4

Question 5

35 / 35 pts

Arrange the following in the **decreasing order of their ease of programmability**. Ideal Memory, FLASH, MASK-Programmed ROM, SRAM/DRAM, OTP, EPROM, EEPROM.

(easiest to write first and most difficult to write last)

i Ideal Memory

ii SRAM/DRAM

iii	FLASH
iv	EEPROM
v	EPROM
vi	OTP
vii	Mask programmed

Question 6

5 / 5 pts

For a memory of size 256 x 32, the word size is _____ .

- (●) 32
- ( ) 16
- ( ) 512
- ( ) 64

Question 7

5 / 5 pts

The number of input signals needed to access 256 address signals is k_____

- 256
- 16
- 8
- 9

Question 8

5 / 5 pts

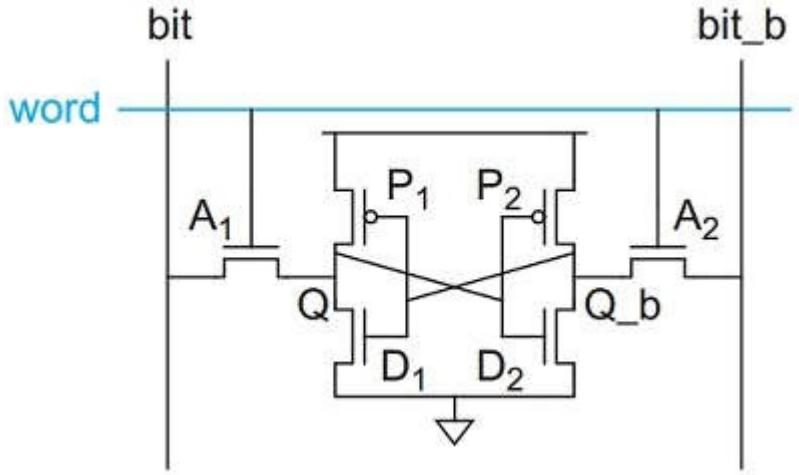
RAM is a _____ memory

- non-volatile
- content addressable
- volatile
- sequential

Question 9

5 / 5 pts

The Read operation in SRAM involves which of the following? Refer to Figure below.

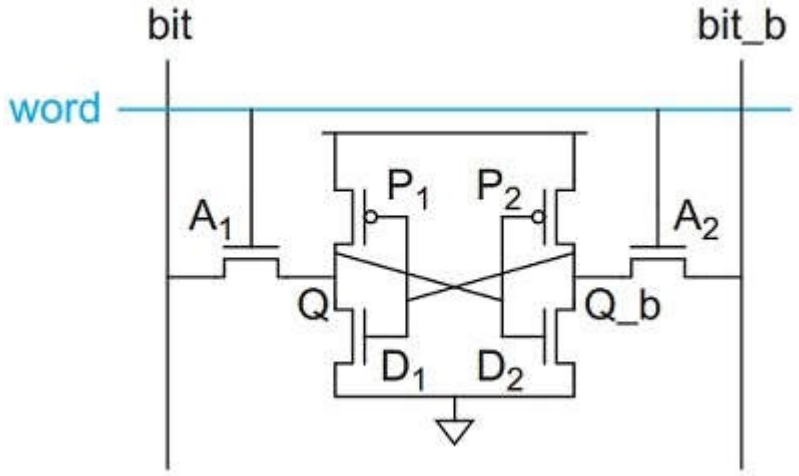


- bit_b is precharged High and left floating
- bit is precharged High and left floating
- Bit lines are initially floated High
- Bit lines are initially floated Low

Question 10

5 / 5 pts

The Write operation in SRAM involves which of the following when trying to write a '1' into the cell? Refer to Figure



- bit is precharged High and left floating

- Bit lines are initially floated Low
- bit_b is precharged High and left floating
- Bit lines are initially floated High

Question 11

5 / 5 pts

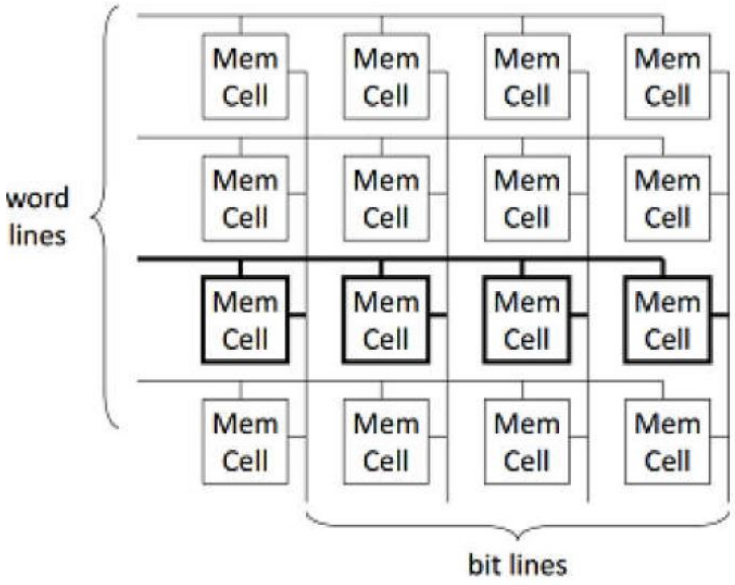
Which of the following components occupies the most amount of silicon area per each bit of memory?

- SRAM
- Flip Flop
- DRAM
- Latch

Question 12

5 / 5 pts

Figure below shows a 4 x 4 memory array (ROM). ROMs can be used to implement any combinational circuit. If each column in the array below is used to implement a combinational logic SOP, how many variables does the SOP have

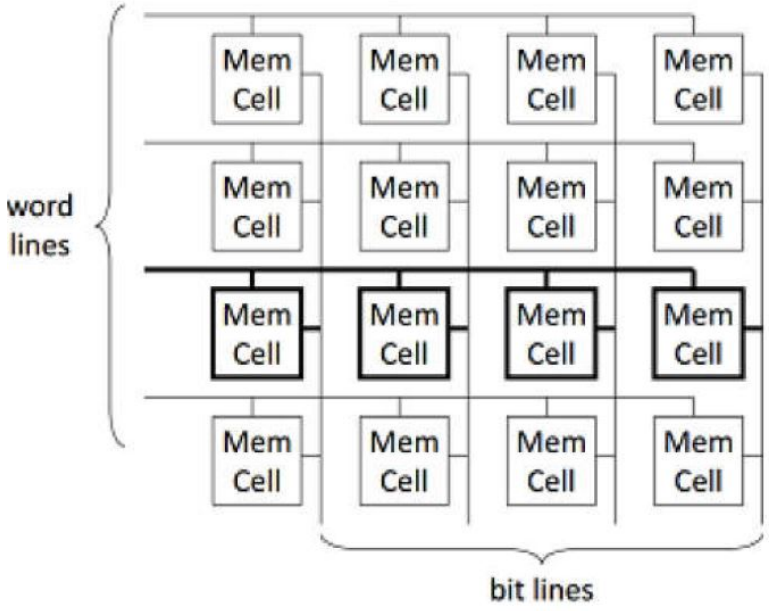


- 2
- 18
- 8
- 4

Question 13

10 / 10 pts

How many different combinational functions of 2 variables can be implemented using the memory in figure as a look up table?



- 16
- 4
- 8
- 2

Quiz Score: **100** out of 100