Quiz-4

Due Apr 15 at 11:59pm **Points** 100 **Questions** 16 **Time Limit** None **Allowed Attempts** Unlimited

Instructions

Submit before the deadline for your section.

Total Number of questions: 16. (For 4 of these questions, you might need calculator.)

Take the Quiz Again

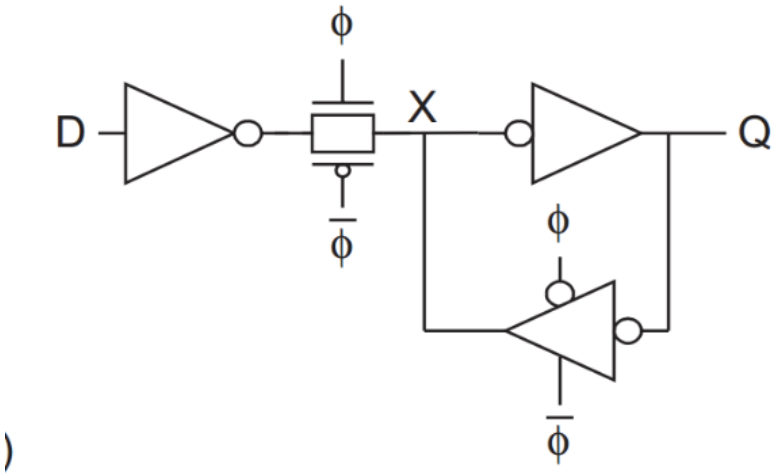
Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	21 minutes	100 out of 100

ⓘ Correct answers are hidden.

Score for this attempt: **100** out of 100
Submitted Apr 15 at 7:45pm
This attempt took 21 minutes.

Question 1 — 5 / 5 pts



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1. The latch shown in the figure above is _____ (Static/Dynamic).

Static

Question 2

5 / 5 pts

The figure below shows two implementations of a conventional CMOS latch. Annotate the maximum output voltage at the Q of figure (a). Assume the input is driven by V_{DD}

- Vtn
- Vdd -vtn
- Vdd-2Vtn
- Vdd

Question 3

5 / 5 pts

The figure below shows two implementations of a conventional CMOS latch. Annotate the maximum output voltage at the Q of figure(b). Assume the input is driven by V_{DD}

- Vdd-2Vtn
- Vdd
- Vdd-Vtn
- Vtn

Question 4

5 / 5 pts

Sequential circuit includes

- feedback
- delays and (feedback from output to input)

- delays and (feedback from the input to output)
- delays

Question 5

5 / 5 pts

For a Moore machine, Outputs are functions of

- previous state
- present state
- present state and current inputs
- current inputs

Question 6

5 / 5 pts

Which is the delay/sequencing element for a clocked system?

- OR gates
- Multiplexers
- AND gates
- Flip-flops

Question 7

5 / 5 pts

A latch is a device with:

- Two stable states
- Three stable states
- None of the mentioned
- One stable states

Question 8

5 / 5 pts

Two stable states of latches are

- (•) High output & low output
- ( ) Astable & Monostable
- ( ) Low output & high input
- ( ) Low input & high output

Question 9

5 / 5 pts

Latches consist of

- (•) inverters
- ( ) frequency generators
- ( ) inductors
- ( ) timing generators

Question 10

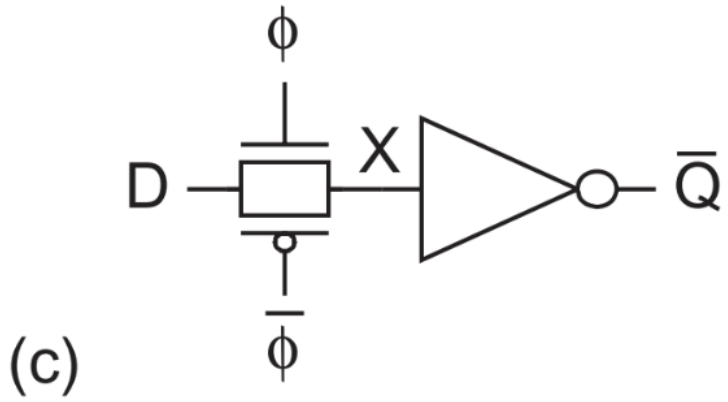
5 / 5 pts

Two inverters are cross-coupled to generate

- (•) latch
- ( ) timing generator
- ( ) gate
- ( ) inductor

Question 11

5 / 5 pts



(c)

Identify the Identify a drawback of using the latch below from figure (c)

- The signal 'D' drives the diffusion input of the transistor. As a result, noise issues
- State node is exposed. As a result, noise on the output can corrupt the state
- The output does not swing from rail-to-rail
- None of the above

Question 12

5 / 5 pts

From the figure (d) below, identify the drawback:

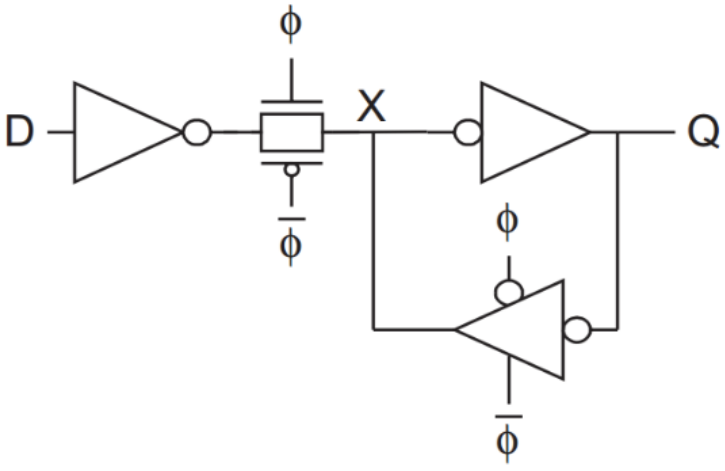


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Figure (d)

- None of the above
- State node is exposed. As a result, noise on the output can corrupt the state

- The output does not swing from rail-to-rail
- The signal 'D' drives the diffusion input of the transistor. As a result, noise issues

Question 13

10 / 10 pts

For a Flip-flop, determine the maximum logic propagation
delay available within a 500 ps clock cycle. Assume there is zero clock skew.

Use the timing parameters needed from Table 10.5

TABLE 10.5 Sequencing element parameters

	Setup Time	*clk*-to-*Q* Delay	*D*-to-*Q* Delay	Contamination Delay	Hold Time
Flip-Flops	65 ps	50 ps	n/a	35 ps	30 ps
Latches	25 ps	50 ps	40 ps	35 ps	30 ps

- 385 ps
- 535 ps
- 400 ps
- 485 ps

Question 14

10 / 10 pts

For a Flip-flop, determine the maximum logic propagation delay available within a 500 ps clock cycle. Assume clock skew between any two elements can be up to 50 ps.

Use the timing parameters needed from Table 10.5

TABLE 10.5 Sequencing element parameters

	Setup Time	*clk*-to-*Q* Delay	*D*-to-*Q* Delay	Contamination Delay	Hold Time
Flip-Flops	65 ps	50 ps	n/a	35 ps	30 ps
Latches	25 ps	50 ps	40 ps	35 ps	30 ps

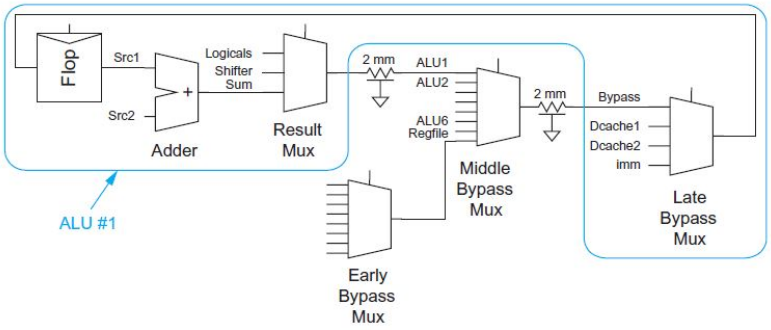
- 485 ps
- 435 ps
- 385 ps
- 335 ps

Question 15

10 / 10 pts

The figure below shows a typical self-bypass path circuit used in ALUs. Table – 1 shows the combinational logic delays (both Propagation and Contamination). As shown in the figure below (**ignore the blue box**), the self – bypass path consists of a FF, followed by combinational logic. The combinational logic path (**critical path**) includes the Adder, Result Mux, 2 mm wire, Middle Bypass Mux, another 2 mm wire, and the Late Bypass Mux.

What is the value of t_{pd} along the critical path in figure?



Element	Propagation Delay	Contamination Delay
Adder	590 ps	100 ps
Result Mux	60 ps	35 ps
Early Bypass Mux	110 ps	95 ps
Middle Bypass Mux	80 ps	55 ps
Late Bypass Mux	70 ps	45 ps
2-mm Wire	100 ps	65 ps

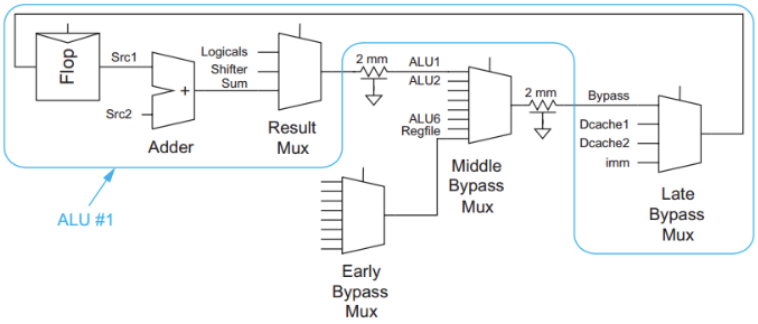
- 1000 ps
- 590 ps
- 1240 ps
- 385 ps

Question 16

10 / 10 pts

The figure below shows a typical self-bypass path circuit used in ALUs. Table – 1 shows the combinational logic delays (both Propagation and Contamination). As shown in the figure (ignore the blue box), the self – bypass path consists of a FF, followed by combinational logic. The combinational logic path (**critical path**) includes the Adder, Result Mux, 2 mm wire, Middle Bypass Mux, another 2 mm wire, and the Late Bypass Mux.

Element	Propagation Delay	Contamination Delay
Adder	590 ps	100 ps
Result Mux	60 ps	35 ps
Early Bypass Mux	110 ps	95 ps
Middle Bypass Mux	80 ps	55 ps
Late Bypass Mux	70 ps	45 ps
2-mm Wire	100 ps	65 ps



What is the minimum value of T_C, if the setup time for the FF is 62 ps and its t_{pcq} = 90 ps?

- 1152 ps
- 1125 ps
- 1512 ps
- 1250 ps

Quiz Score: **100** out of 100