Mario Palacios
CpE 142 – Section 01
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1. Describe the difference between computer architecture and computer organization. (10 Points)

Computer architecture involves the interface between hardware and software. While also implementing eight great ideas; Moore's Law, Abstraction, Common Case Fast, Parallelism, Pipelining, Prediction, Hierarchy, and Dependability.

Computer organization deals with the structure and behavior of the computer system as a whole. This can be broken down into five parts; Input, Outputs, Memory, Datapath, and Control.

2. Define CPU execution time and explain how it can be calculated. (10 points)

CPU execution time (or just CPU time) is the amount of time spent processing a given task, but discounts I/O time or the time spent running other programs. The overall CPU time includes user CPU time [programming itself] and system CPU time [OS performing tasks behalf of program]. To calculate CPU execution time:

$$CPU\ Time = CPU\ Clock\ Cycles\ for\ a\ program \times\ Clock\ Cycle\ Time$$

or
[because clock rate and clock cycle time are inverses]

$$CPU\ Time = \frac{CPU\ Clock\ Cycles\ for\ a\ program}{Clock\ Rate}$$

3. Define response time. (10 points)

Also known as execution time, takes into account the total time required for a computer to complete a task. This includes disk access, memory access, I/O activities, operating system overhead, and CPU execution time.

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4. Problem 1.5 from the text. (20 points)

1.5 [4] <§1.6> Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second?

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

a) Processor 2 has the highest performance expressed in instructions per second.

$$CPU\ Time = Instruction\ Count \times CPI \times Clock\ Cycle\ Time$$

$$\frac{CPU\ Time}{Instruction\ Count} = Instruction\ per\ second = \frac{Clock\ Rate}{CPI}$$

P1: Clock Rate / CPI = (3.0GHz) / (1.5) = 2*10^9 instructions per second
P2: Clock Rate / CPI = (2.5GHz) / (1.0) = 2.5*10^9 instructions per second
P3: Clock Rate / CPI = (4.0GHz) / (2.2) = 1.81*10^9 instructions per second

b) $\#\ of\ Instructions = Time\ per\ instruction \times 10\ Seconds, \quad \#\ of\ cycles = \#\ of\ instructions \times CPI$

P1: # of instructions = 2*10^10, # of cycles = 3.0 * 10^10
P2: # of instructions = 2.5*10^10, # of cycles = 2.5 * 10^10
P3: # of instructions = 1.81*10^10, # of cycles = 3.98 * 10^10

c) $Old\ CPU\ Time \times 0.7 = \frac{\#\ of\ intructions \times CPI \times 1.2}{New\ Clock\ Rate} \Rightarrow New\ Clock\ Rate = \frac{Old\ Clock\ Rate \times 1.2}{0.7}$

P1: New Clock Rate = 5.14 GHz
P2: New Clock Rate = 4.28 GHz
P3: New Clock Rate = 6.85 GHz

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5. Problem 1.6 from the text. (20 points)

> **1.6** [20] <§1.6> Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.
>
> Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?
>
> **a.** What is the global CPI for each implementation?
>
> **b.** Find the clock cycles required in both cases.

Processor	Clock Rate	A	B	C	D
P1	2.5 GHz	1	2	3	3
P2	3.0 GHz	2	2	2	2

Processor 2 has a much faster implementation than processor 1.

$$CPU\ Time = \frac{\sum(CPI\ \times\ Instructions)}{Clock\ Rate}$$

P1: [(10^6) * ((0.1*1) + (0.2*2) + (0.5*5) + (0.2*3)) / (2.5 * 10^9)] = 1.04ms
P2: [(10^6) * ((0.1*2) + (0.2*2) + (0.5*2) + (0.2*2)) / (3.0 * 10^9)] = 0.667ms

a) $Global\ CPI = \frac{CPU\ Time \times Clock\ Rate}{Number\ of\ Instructions}$

P1: Global CPI = 2.6
P2: Global CPI = 2.0

b) $Number\ of\ Cycles = Global\ CPI\ \times\ Number\ of\ Instructions$

P1: Number of Cycles = (2.6) * (10^6) = 2.6 * 10^6
P2: Number of Cycles = (2.0) * (10^6) = 2.0 * 10^6

6. List four features of a RISC architecture. (10 points)

Four features of a RISC architecture include; limited loading/storing instruction, large number of registers, fewer addressing modes, and instruction pipelining.

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7. System M1 requires 640ms to execute a program. Thirty percentc(30%) of the elapsed time is devoted to CPU computations while the rest to memory and I/O. M1 is enhanced by doubling the performance of its CPU. Calculate the speedup for the enhancement. (20 point)

$$Speed\ Up = \frac{T_{original}}{T_{improved}}$$

M1 Current CPU Time = 0.3 * 640ms = 192ms

New M1 CPU Time = 192ms / 2 = 96ms

New Elapsed Time = 640 – 192 + 96 = 544ms

Speed Up = 640ms / 544ms = 1.176 or 117.6%