SACRAMENTO STATE

MARIO PALACIOS

LAB COURSE (CpE 64) SECTION #20

WEDNESDAY

INSTRUCTOR: EMMANUEL DUPART

## Part 1. Breadboard Continuity

### Description:

The objective of this part of the lab is to get familiarization with the lines of continuity on the breadboard.

### Problem Definition:

Examine the breadboard, and figure out where the lines of continuity are (what lines of holes are connected to other lines of holes). A Digital Multimeter (DMM) set to a low resistance setting can be used to test where the lines of continuity are located. Knowing where the lines of continuity are crucial to testing circuit designs.

### Engineering Data:

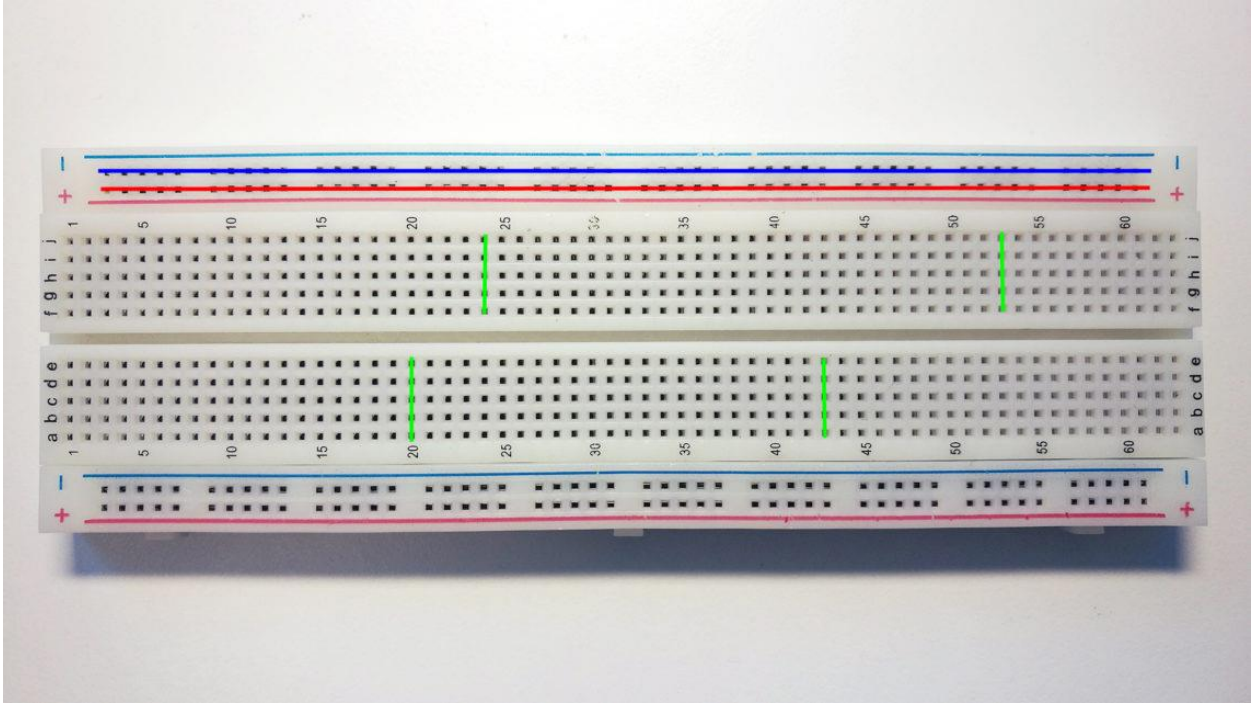


**Figure 1. Breadboard with Lines of Continuity Drawn**

After testing the breadboard's continuity, I found out that the bus strip (red and blue lines) have continuity and are best to supply power to the breadboard. The bus strips on my breadboard are separated into a total of eight groups of five nodes, and after four groups there is a gap. The gap signifies that there is a break and the continuity stops. The middle group of nodes is called the terminal strips and there is two rows that consist of 60 nodes. The line of continuity is vertical (green lines), and does not contain any breaks.

**Conclusion:**

After completing this part of the lab, I am able to say that I understand how to build circuits on my breadboard. It did not take me long to understand how it works but served as a good review. In total this part of the lab took me about five minutes.

## Part 2. Identifying the 7400 Series TTL Gates

**Description:**

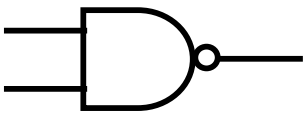
The objective of this part is to identify the 7400 series TTL gates and look up their; logic symbol, function in an equation, and the Truth Table.

**Problem Definition:**

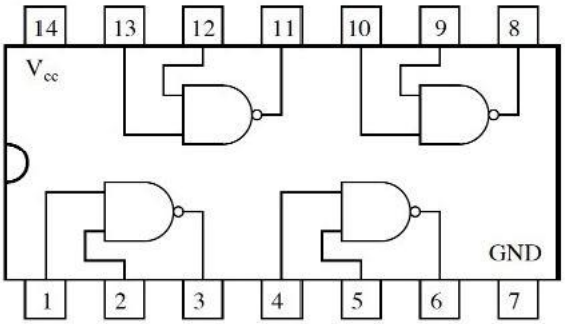
Record all the information on the 7400 series TTL gates; 7400, 7404, 7408, and 7432. Show their logic symbol, function in an equation, and the truth table for each one.

**Engineering Data:**

*7400: quad NAND gate*

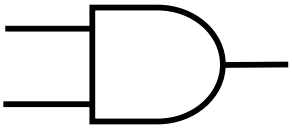


$\overline{A \cdot B}$ *or* $A \uparrow B$

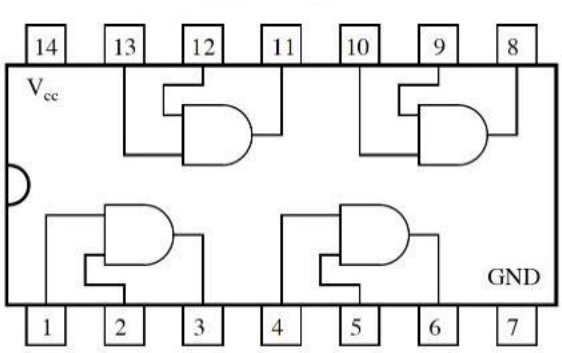



| Input | | Output |
|---|---|---|
| **A** | **B** | **A NAND B** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

*7408: quad AND gate*

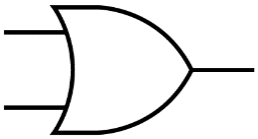


$A \cdot B \; or \; A \cap B$

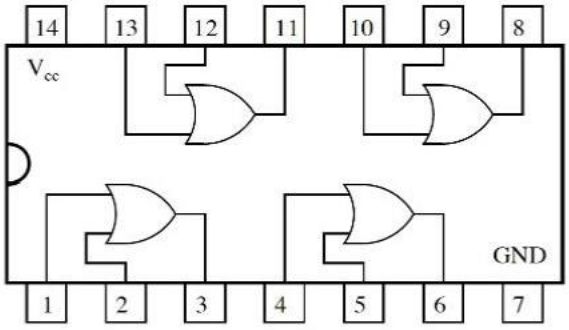



| **Input** | | **Output** |
|---|---|---|
| **A** | **B** | **A AND B** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

*7432: quad OR gate*

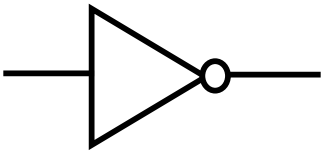


$A + B \; or \; A \cup B$

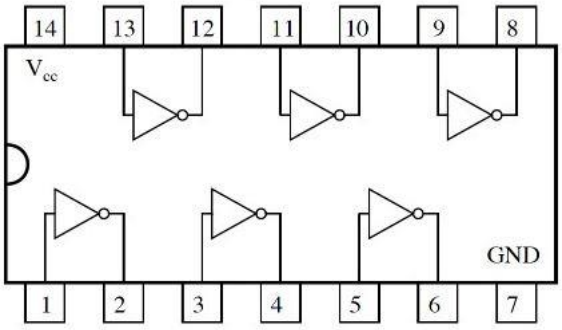



| **Input** | | **Output** |
|---|---|---|
| **A** | **B** | **A OR B** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

*7404: hex NOT gate*



$\bar{A}$ *or* $\neg A$




| Input | Output |
|---|---|
| A | NOT A |
| 0 | 1 |
| 1 | 0 |

**Conclusion:**

Once I completed this part I got a better understanding of what logic gates are, by seeing their symbol, truth table, pin out diagram, and Boolean operator. Overall the pin outs for all four chips have the same voltage input (pint 14) and ground (pin 7). For logic gates 7400, 7408, and 7432, have two inputs and one output. While the 7404 logic gate only has one input and one output. In total this part of the lab took me about 15 minutes because of all the research needed to be done.

**Part 3. Gate Testing**

**Description:**

The goal of this part of the lab is to verify the truth tables of each logic gate.

**Problem Definition:**

We will test each gate in MultiSim first, and create a truth table gathered in part 2. The information collected will have a c column for inputs, one for output based on gate specification, another for simulation results, and lastly an output column for breadboard results. Once the MultiSim data is verified, build up each gate on a breadboard and compare the output data with the truth table from part 2 and MultiSim. You will need only one LED for the one output of each gate.

**Engineering Data:**

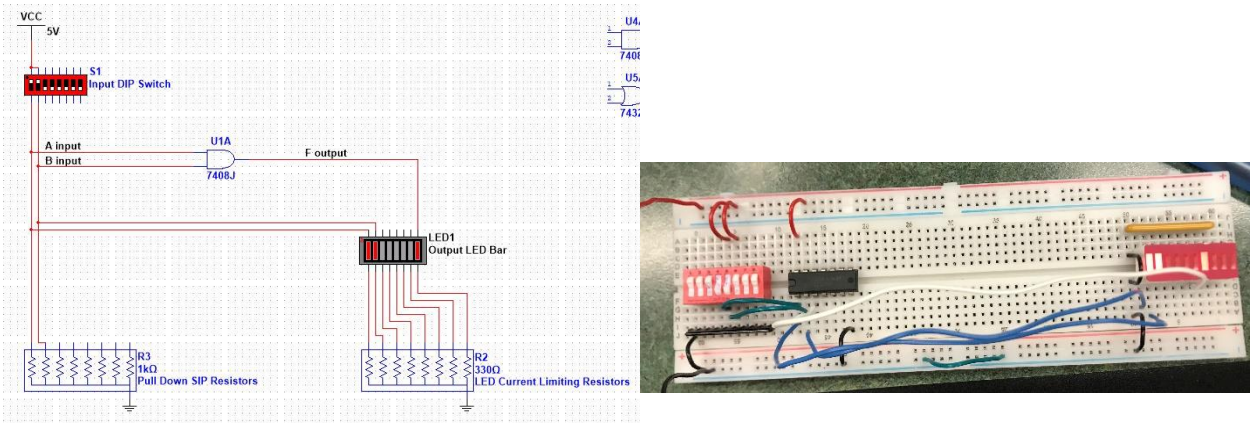



**Figure 2. MultiSim Diagram and Circuit with Output Results**

| Input | | Expected Output | MultiSim Output | BB Output |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Table 1. Output Results from Truth Table, MultiSim, and Breadboard for AND Gate**

| Input | | Expected Output | MultiSim Output | BB Output |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |

**Table 2. Output Results from Truth Table, MultiSim, and Breadboard for NAND Gate**

| Input | | Expected Output | MultiSim Output | BB Output |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Table 3. Output Results from Truth Table, MultiSim, and Breadboard for OR Gate**

| Input | | Expected Output | MultiSim Output | BB Output |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |

**Table 4. Output Results from Truth Table, MultiSim, and Breadboard for NOT Gate**

**Conclusion:**

In the end the truth table matches with the results from MultiSim and the breadboard for each of the logic gates. This verifies the outputs are valid and will be useful for future circuit designs. In total the circuit design done on MultiSim and on the breadboard as seen on Figure 1, took me 30 minutes. The same design was used for each of the remaining logic gates.

## Part 4. Four Chips on One Breadboard

**Description:**

The objective of this part is to test all four chips together on MultiSim and on the breadboard.

**Problem Description:**

Before building the circuit on the breadboard test the circuit in MultiSim and record all the outputs. There should be two inputs and four outputs. Wire on LED to each of the gate's output, there should be 4 LEDs used. For inputs there should be two switches that will connect each gate. Test and record the functions by observing the four outputs, when you do the four possible input patterns (00, 01, 10, and 11).

**Engineering Data:**

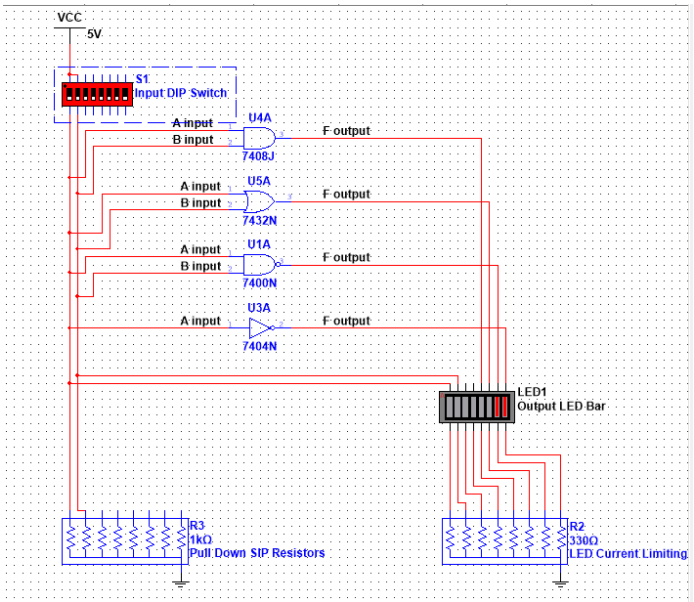



**Figure 3. MultiSim Circuit Diagram for Input (00)**

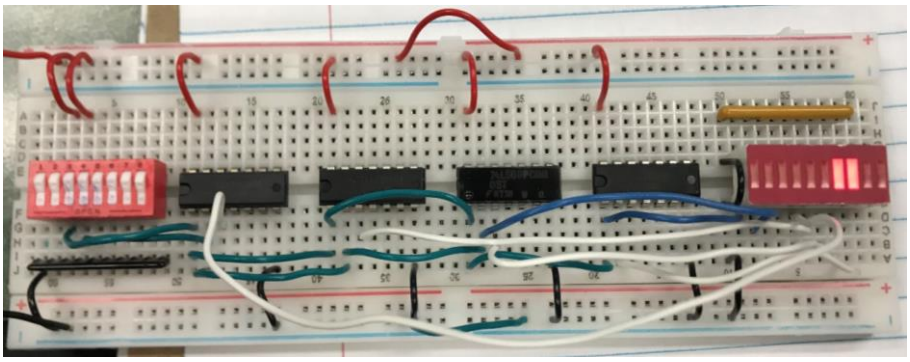


**Figure 4. Breadboard Circuit Diagram for Input (00)**

| INPUTS | | EXPECTED OUTPUTS | | | | SIMULATED OUTPUTS | | | | BB ACTUAL OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IN1 | IN2 | AND | OR | NAND | NOT | AND | OR | NAND | NOT | AND | OR | NAND | NOT |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

**Table 5. Output Data from Truth Tables, MultiSim, and Breadboard**

When building this circuit it was fairly easy once part 3 and part 1 was completed. Without knowing where the lines of continuity are and the break on the bus strip, the breadboard design would not be working properly. The red and black wires going from one group of nodes to another on the terminal strip is used to pass the current because of the gap breaking continuity.

**Conclusion:**

In conclusion the MultiSim and breadboard LED order was the same as the truth table. In order to have this result one must know how logic gates work and their breadboard. There was a problem that I occurred which is that I forgot about the gap in my bus strip. However with some testing with a Digital Multimeter, I was able to figure out again that the gap meant a break in continuity. Overall this part of the lab took me the longest because of that, but wiring the logic gates and LED was not difficult when I had MultiSim as a guide.