Mario Palacios and Andrew Peterson

California State University, Sacramento

Lab 05: PSPICE

EEE 117 Lab – Section 04: Tuesday, 4:30pm – 7:10pm

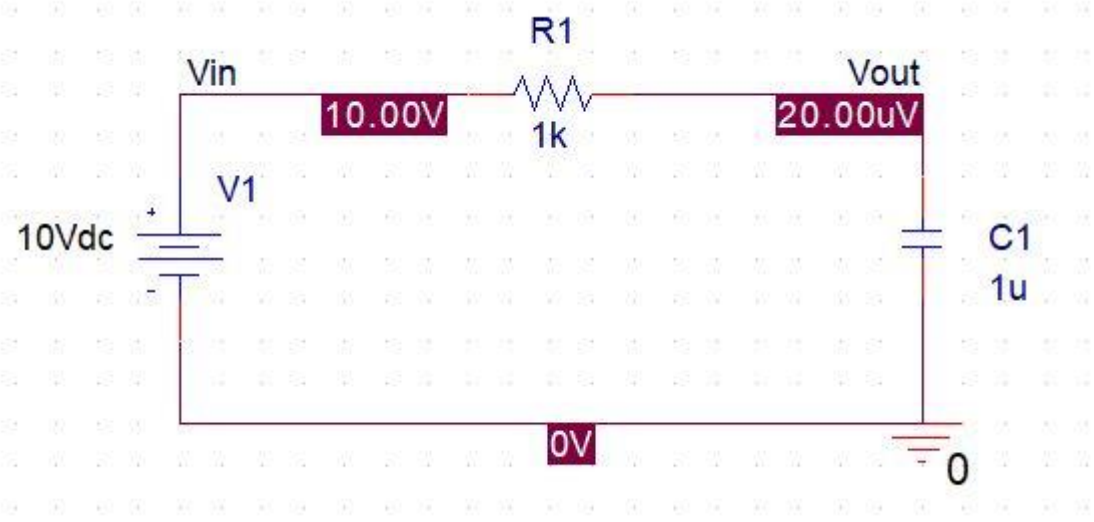

Figure 1. Transient Analysis, Resistor-Capacitor Circuit

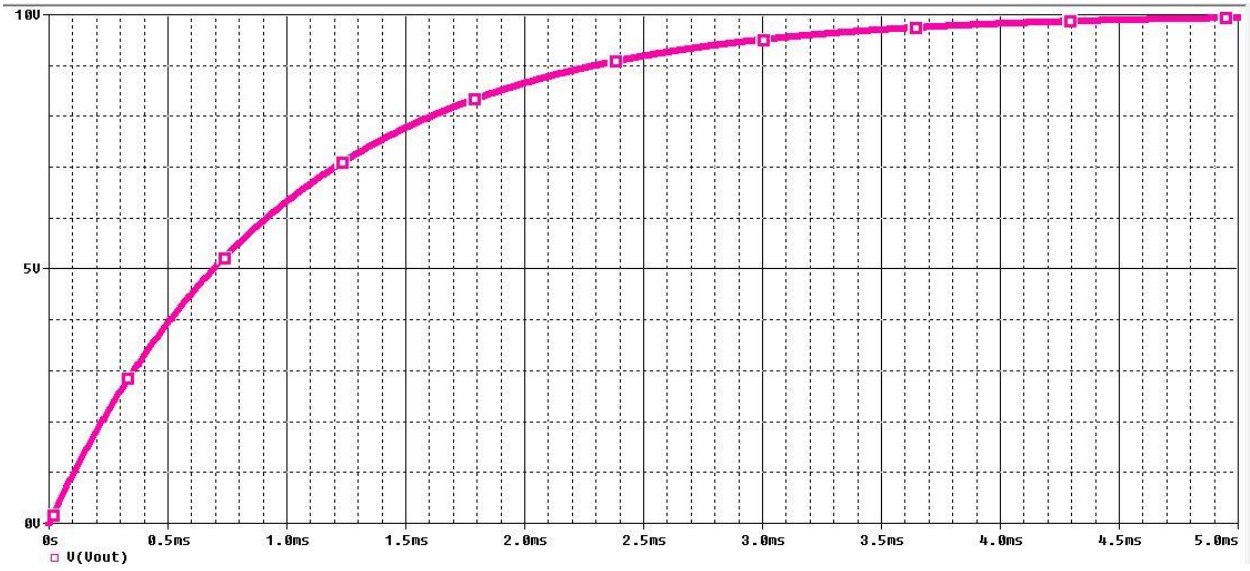

Figure 2. Transient Analysis, Resistor-Capacitor Graph (V_{out}[V] vs Time [ms])

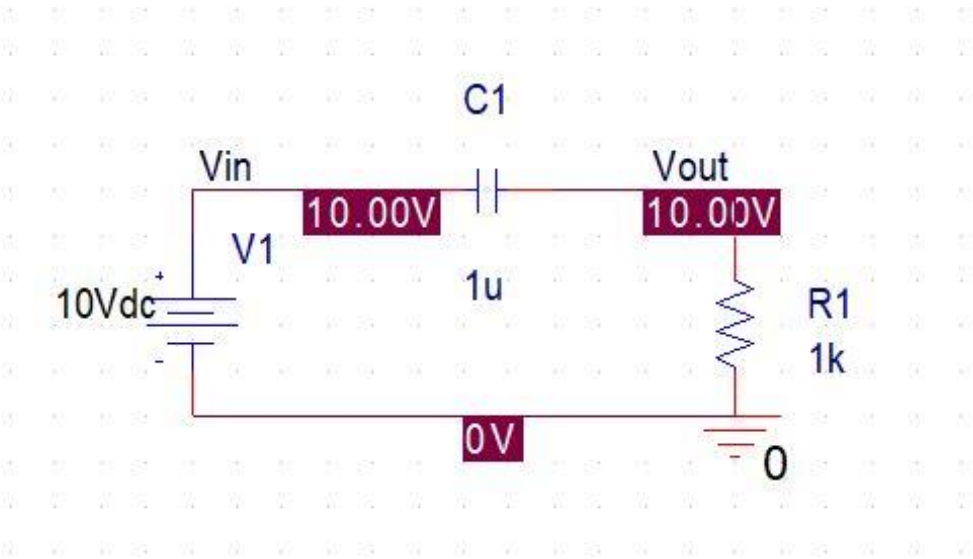

Figure 3. Transient Analysis, Capacitor-Resistor Circuit

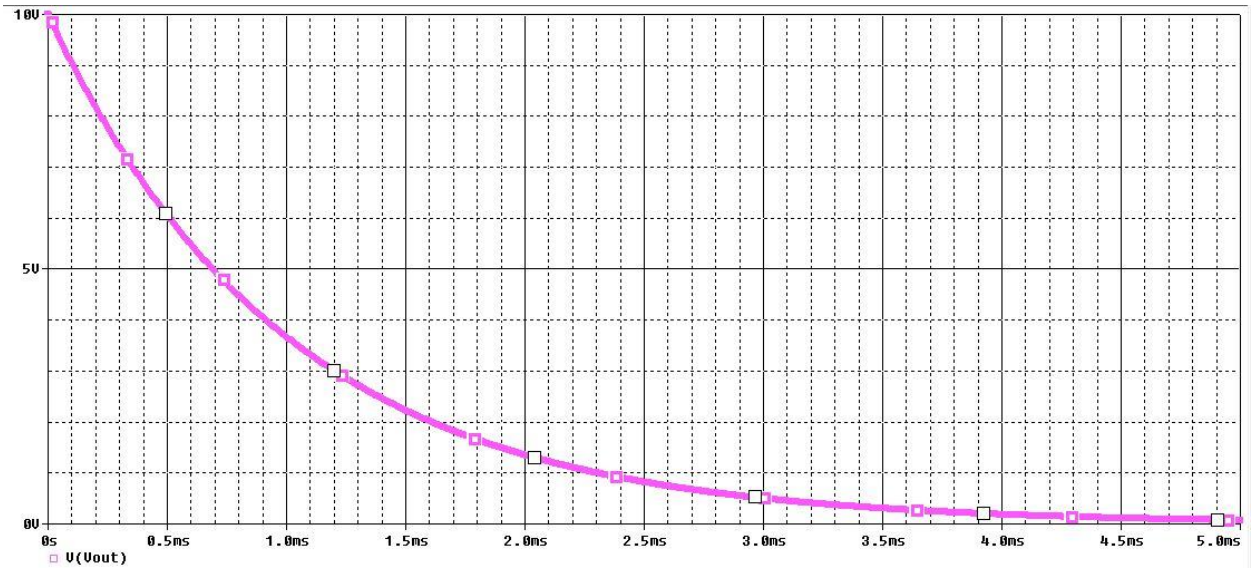

Figure 4. Transient Analysis, Capacitor-Resistor Graph (V_{out}[V] vs Time [ms])

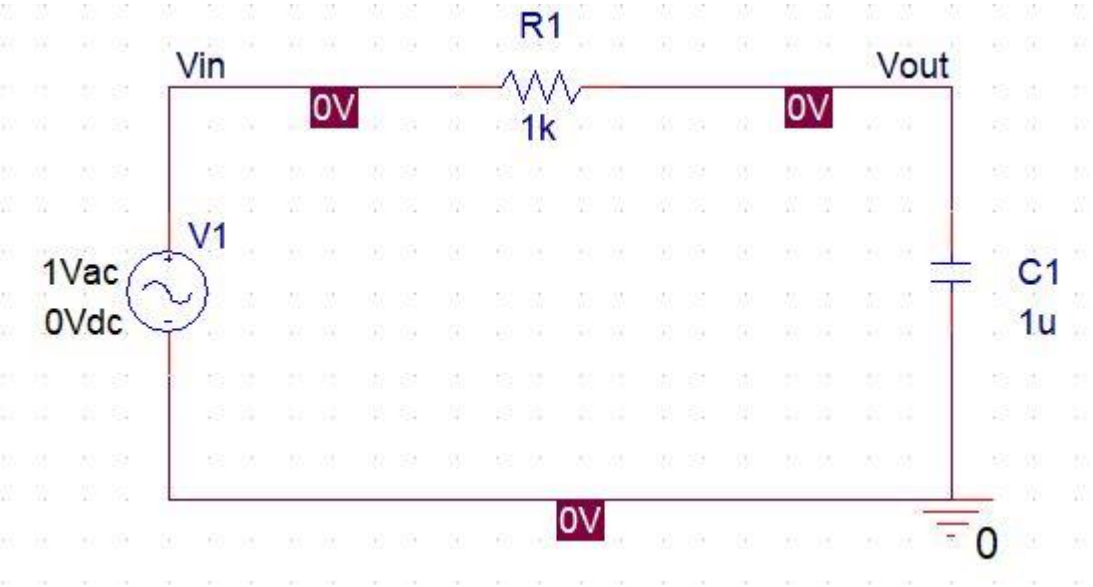

Figure 5. AC Analysis, Resistor-Capacitor Circuit

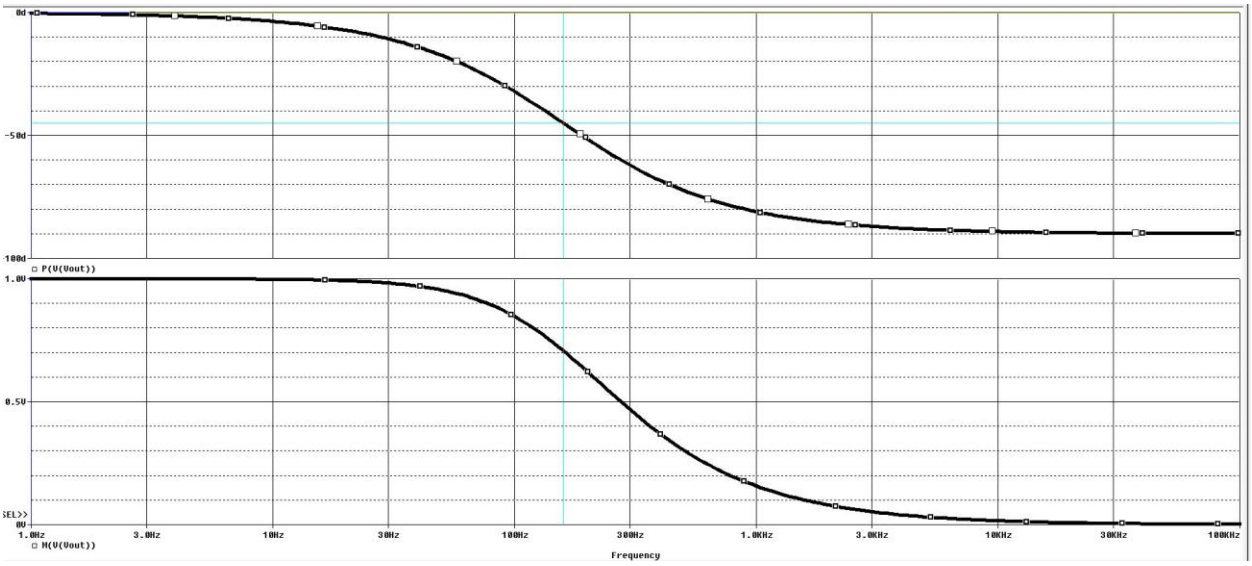

Figure 6. AC Analysis, Resistor-Capacitor (Top Graph: Phase[V_{out}] vs Log[Frequency], Bottom graph: Magnitude[V_{out}] vs Log[Frequency])

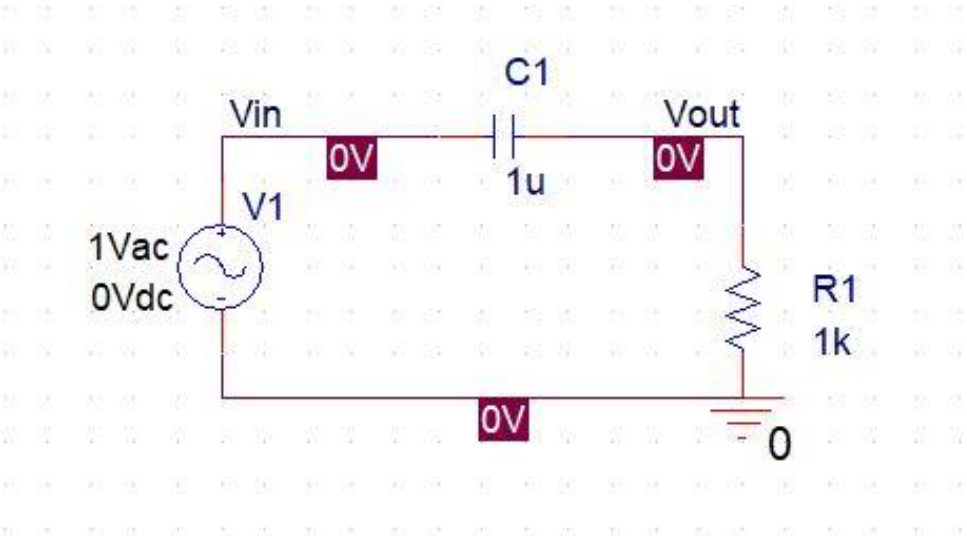

Figure 7. AC Analysis, Capacitor-Resistor Circuit

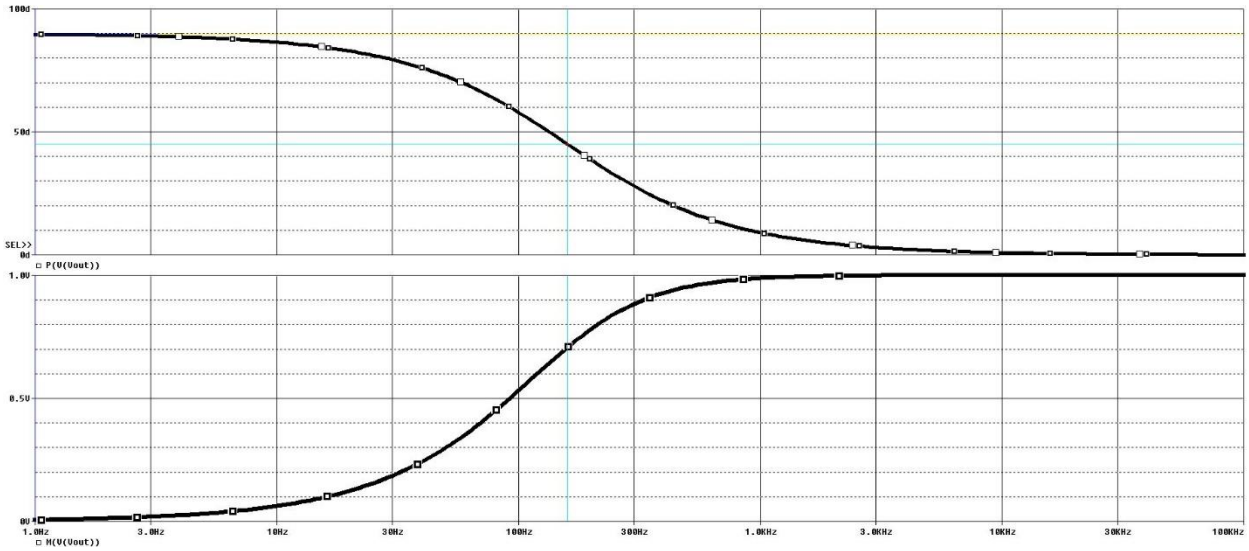

Figure 8. AC Analysis, Capacitor-Resistor (Top Graph: Phase[V_{out}] vs Log[Frequency], Bottom graph: Magnitude[V_{out}] vs Log[Frequency])