Quiz - 3

Due Mar 16 at 11:59pm **Points** 100 **Questions** 10 **Time Limit** None
Allowed Attempts Unlimited

Take the Quiz Again

Attempt History

	Attempt	Time	Score
KEPT	Attempt 2	2 minutes	100 out of 100
LATEST	Attempt 2	2 minutes	100 out of 100
	Attempt 1	35 minutes	40 out of 100

Correct answers are hidden.

Score for this attempt: **100** out of 100
Submitted Mar 15 at 9:43pm
This attempt took 2 minutes.

Question 1 — 10 / 10 pts

1. By definition, **the minimum time from input to rising output crossing $V_{DD}/2$** is:

- Rise Time - (tr)
- Setup – time
- Rising Contamination delay (tcdr)
- Rising Propagation Delay (tpdr)

Question 2 — 10 / 10 pts

In RC Delay Model, which of the following substitutions is valid?

- NMOS transistor with a width of k times the unit transistor has a resistance of 2R/k
- PMOS transistor with a width of k times the unit transistor has a resistance of R/k
- NMOS transistor with a width of k times the unit transistor has a cap of 2kC on the gate
- PMOS transistor with a width of k times the unit transistor has a cap of kC on the gate

Question 3

10 / 10 pts

The falling delay is affected by the resistance in the _____ network?

- (•) PDN
- ( ) PUN

Question 4

10 / 10 pts

The rising delay is affected by the resistance in the _____ network?

- (•) PUN
- ( ) PDN

Question 5

10 / 10 pts

A 2-input NAND gate is designed to achieve the effective Resistance of a unit inverter for PUN and PDN. It has a fan-out of 1.

What is the Kp value for the NAND gate above?

- ( ) Kp = 1
- ( ) Kp = 8
- (•) Kp = 2
- ( ) Kp = 4

Question 6

10 / 10 pts

A 2-input NAND gate is designed to achieve the effective Resistance of a unit inverter for PUN and PDN. It has a fan-out of 1.

What is the Kn value for the NAND gate above?

- Kn = 2
- Kn = 8
- Kn = 4
- Kn = 1

Question 7

10 / 10 pts

A 2-input NAND gate is designed to achieve the effective Resistance of a unit inverter for PUN and PDN. It has a fan-out of 1.

For the NAND gate above, what is the value of the parasitic delay, tpdr, worst case (load-free component)?

- 6RC
- 12RC
- 5RC
- 8RC

Question 8

10 / 10 pts

A 2-input NAND gate is designed to achieve the effective Resistance of a unit inverter for PUN and PDN. It has a fan-out of 1.

For the NAND gate above, what is the value of the delay from the load (parasitic-free component)?

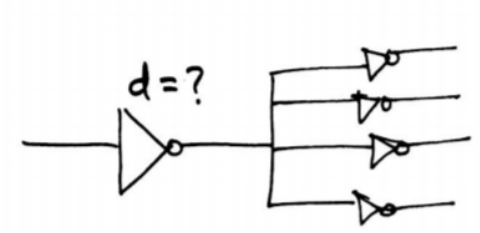
- 5RC
- 12RC
- 6RC
- 4RC

Question 9

10 / 10 pts

For the figure shown below, what is the parasitic delay in terms of T?

(T is defined as the delay of a parasitic–free fanout-of-1 inverter)



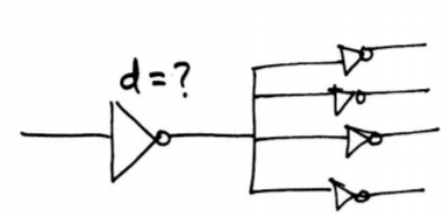
- 2T
- 4T
- 1T
- 3T

Question 10

10 / 10 pts

For the figure shown below, what is the load (fanout) delay in terms of T?

(T is defined as the delay of a parasitic–free fanout-of-1 inverter)



- 1T
- 4T
- 3T
- 2T

Quiz Score: **100** out of 100