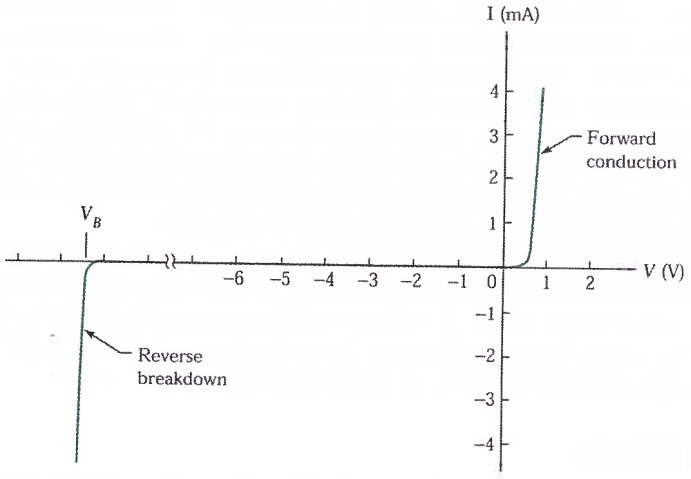

Fig. 1 **Current-voltage characteristics of a typical silicon *p–n* junction.**

▶ 3.1 THERMAL EQUILIBRIUM CONDITION

Today, planar technology is used extensively for *p–n* junction and integrated circuit (IC) fabrication. The planar processes include oxidation, lithography, ion implantation, and metallization; they will be discussed in Chapters 13–15. The most important characteristic of *p–n* junctions is that they rectify: that is, they allow current to flow easily in only one direction. Figure 1 shows the current-voltage characteristics of a typical silicon *p–n* junction. When we apply "forward bias" to the junction (i.e., positive voltage on the *p*-side), the current increases rapidly as the voltage increases. However, when we apply a "reverse bias," virtually no current flows initially. As the reverse bias is increased the current remains very small until a critical voltage is reached, at which point the current suddenly increases. This sudden increase in current is referred to as the junction breakdown. The applied forward voltage is usually less than 1V, but the reverse critical voltage, or breakdown voltage, can vary from just a few volts to many thousands of volts, depending on the doping concentration and other device parameters.

3.1.1 Band Diagram

In Fig. 2*a*, we see two regions of *p*- and *n*-type semiconductor materials that are uniformly doped and physically separated before the junction is formed. Note that the Fermi level E_F is near the valence band edge in the *p*-type material and near the conduction band edge in the *n*-type material. While *p*-type material contains a large concentration of holes with few electrons, the opposite is true for *n*-type material.

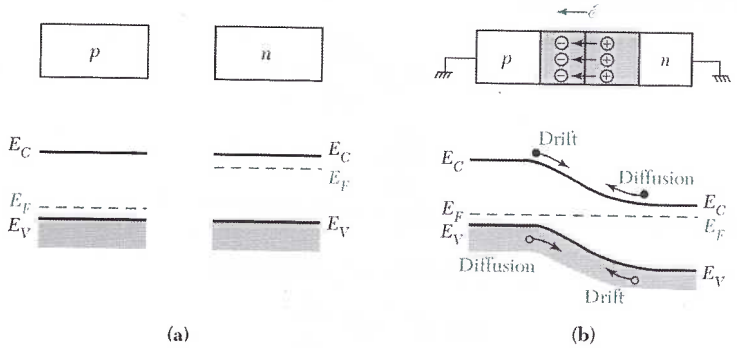

Fig. 2 **(*a*) Uniformly doped *p*-type and *n*-type semiconductors before the junction is formed. (*b*) The electric field in the depletion region and the energy band diagram of a *p–n* junction in thermal equilibrium.**