AIC HW1

111511076 陳彥宇

Code for Problem 1 & 2

```
***-----------------------***
***        setting        ***
***-----------------------***
.lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" ff
.TEMP 25
.op
***-----------------------***
***       simulation      ***
***-----------------------***
.option post
.tran 0.1n 60n

.DC V1 0V 1.8V 1mV
.probe id_mos = I(MN)
***-----------------------***
***      parameters       ***
***-----------------------***
.param wn = 5.4u
.param ln = 1.8u
.global VDD GND
***-----------------------***
***      power/input      ***
***-----------------------***
Vsupply VDD GND 1.8v
V1 Vds GND 1.8V
V2 Vgs GND 1.8V
***-----------------------***
***        circuit        ***
***-----------------------***
MN  Vds VDD GND GND n_18_mm w=wn l=ln
```

```
31.
32. ***------------------------***
33. ***         alter         ***
34. ***------------------------***
35. .alter
36. .param wn = 0.54u
37. .param ln = 0.18u
38. .end
```

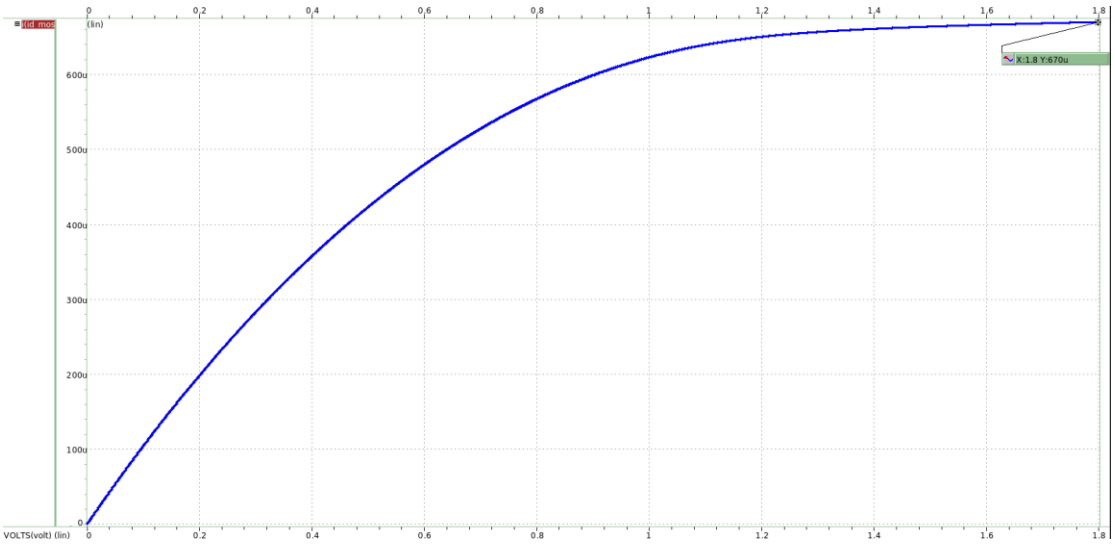
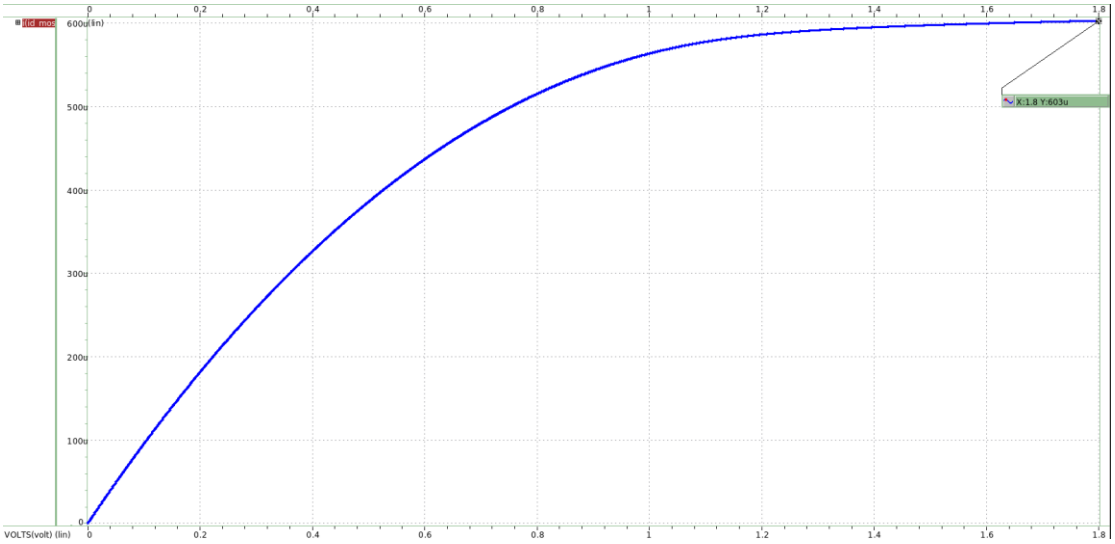
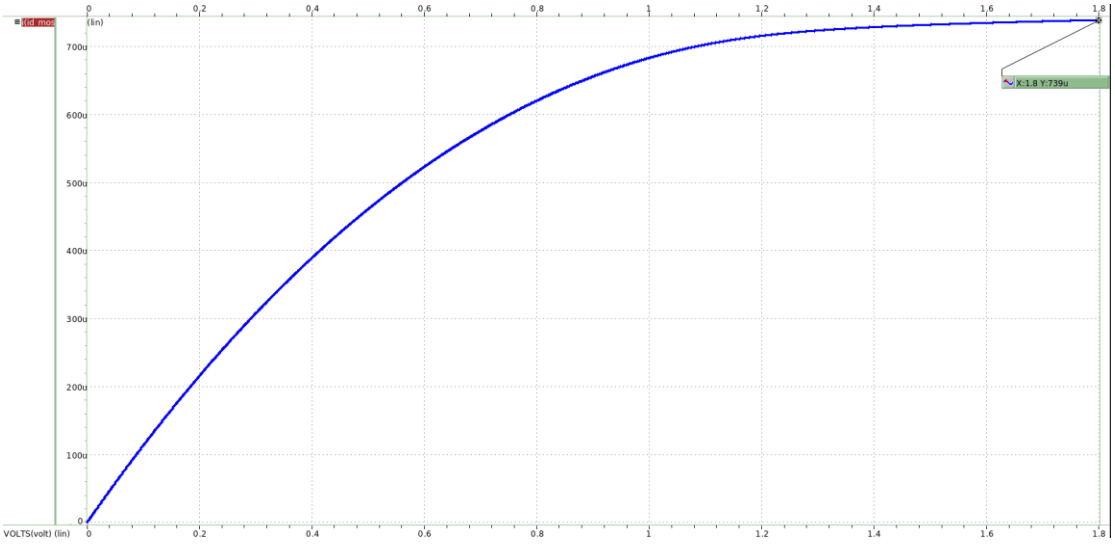
Problem 1

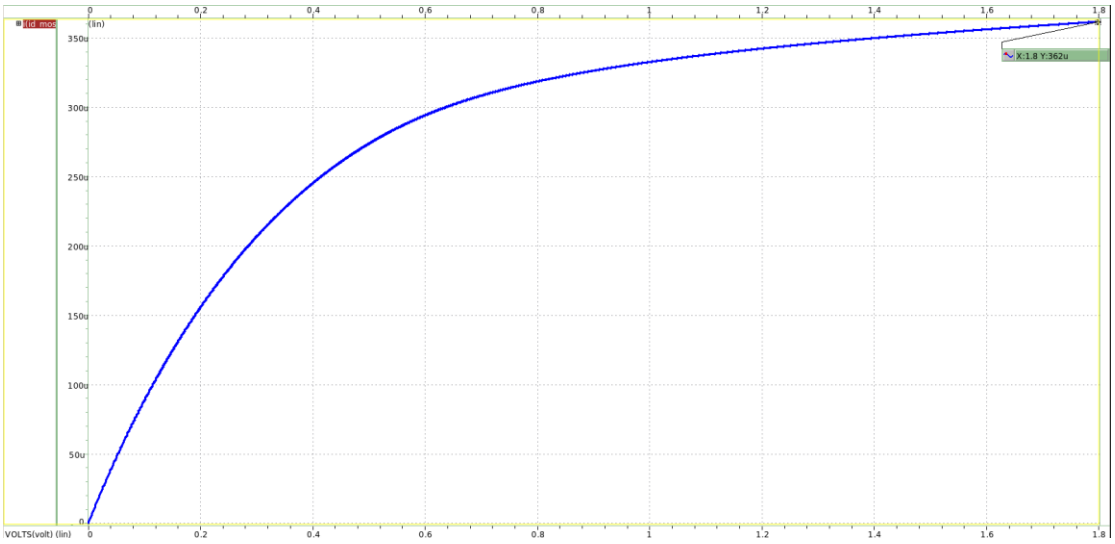
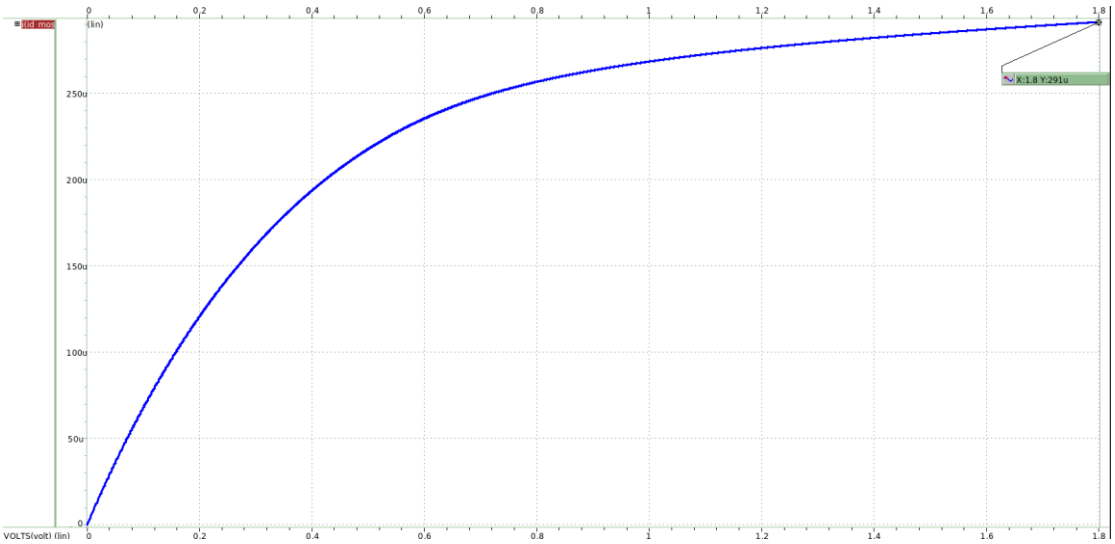
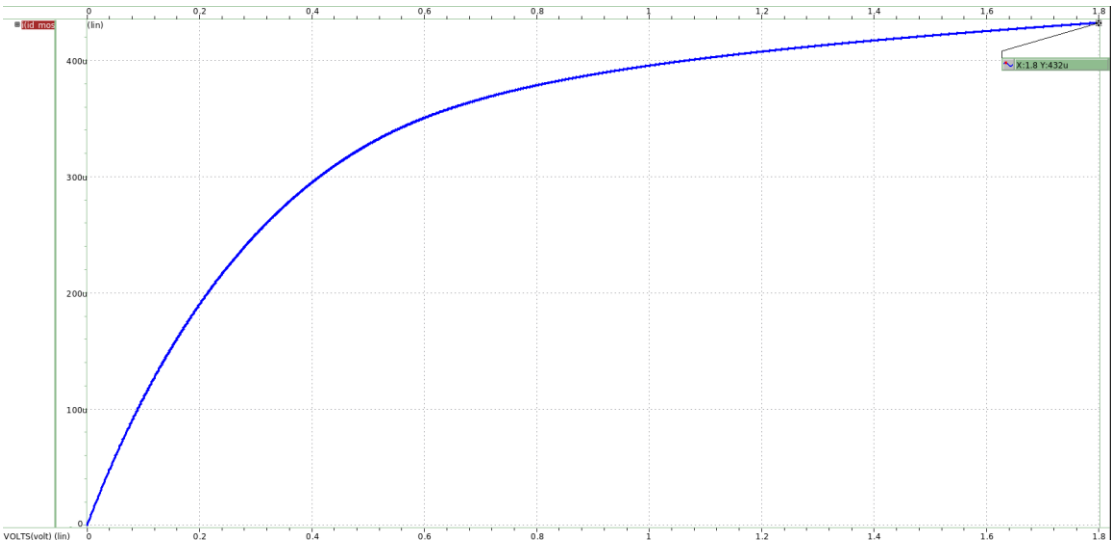
According to the waveforms and simulated values, I_D is smaller in the SS corner, and larger in the FF corner when compared to TT. The following is the meaning of each corner:

SS (Slow-Slow) Corner: Both NMOS and PMOS transistors are slow. The MOSFETs have higher threshold voltages. The circuit operates slower in this corner. It represents a worst-case scenario in terms of performance.

TT (Typical-Typical) Corner: Both NMOS and PMOS transistors exhibit typical behavior. The process variation is minimal, and the transistor characteristics match the nominal or average conditions. It is the reference point when comparing performance under other corners like SS (slow) or FF (fast).

FF (Fast-Fast) Corner: Both NMOS and PMOS transistors are fast. This results in lower threshold voltages and faster switching, causing the circuit to operate more quickly. It represents a best-case scenario in terms of performance.

Corner	I_D @ V_{gs} = V_{ds} = 1.8V W/L=5.4um/1.8um
TT	
SS	
FF	

Corner	I_D @ V_{gs} = V_{ds} = 1.8V W/L=0.54um/0.18um
TT	
SS	
FF	

Problem 2

The simulated values are smaller than calculated values potentially due to second-order effects like mobility degradation and narrow-width effect:

Mobility Degradation:

The effective mobility of charge carriers degrades with higher electric fields (especially in short-channel devices). In my hand calculations, I assume that μ_n is constant, whereas HSPICE uses more realistic models that account for mobility degradation under strong inversion conditions.

Narrow-Width Effect:

When the width of the transistor becomes very small (narrow-width devices), the fringing fields from the gate extend into the sidewalls, causing more of the substrate to be depleted. This makes it harder for the gate to invert the channel, effectively increasing V_{th}. Notice that even though W/L=5.4um/1.8um & W/L=0.54um/0.18um have the same $\frac{W}{L}$ ratio, I_D is smaller when W/L=0.54um/0.18um.

Param.	Sim.	Cal.
$V_{gs} = 1.8V,\ V_{ds} = 1.8V$ W/L=5.4um/1.8um	$I_D = 670uA$	$I_D = 862.47uA$
$V_{gs} = 0.8V,\ V_{ds} = 1.8V$ W/L=5.4um/1.8um	$I_D = 76.9uA$	$I_D = 93.91uA$

$V_{gs} = 1.8V$, $V_{ds} = 1.8V$ W/L=0.54um/0.18um	$I_D = 362uA$	$I_D = 862.47uA$
$V_{gs} = 0.8V$, $V_{ds} = 1.8V$ W/L=0.54um/0.18um	$I_D = 64.6uA$	$I_D = 93.91uA$

$V_{th} = 0.3075$

$\mu_0 = 314.1\ cm^2/(V \cdot s)$

$k_{ox} = 3.9$

$\varepsilon_0 = 8.854187 \times 10^{-14} F/cm$

$t_{ox} = 4.2 \times 10^{-7} cm$

$$C_{ox}WL = C_g = k_{ox}\frac{\varepsilon_o}{t_{ox}}WL$$

$$= 3.9 \times \frac{8.854187 \times 10^{-14}}{4.2 \times 10^{-7}} \times WL\ (F/cm^2)$$

$$I_D = \frac{1}{2}kV_{ov}^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{ov}^2$$

$$= \frac{1}{2}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}V_{ov}^2$$

$$= \frac{1}{2} \times 314.1 \times 3.9 \times \frac{8.854187 \times 10^{-14}}{4.2 \times 10^{-7}} \times \frac{W}{L} \times V_{ov}^2$$

Code for Problem 3

```
***-----------------------***
***        setting        ***
***-----------------------***
.lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" tt
.TEMP 25
.op
***-----------------------***
***       simulation      ***
***-----------------------***
.option post
.DC V1  0V 1.8V 1mV sweep V2  0V 1.8V 0.2V
.probe id_mos = I(MN)

***-----------------------***
***      parameters       ***
***-----------------------***
.param wn = 5.4u
.param ln = 1.8u
.param ls = 0.48u
.global VDD GND

***-----------------------***
***      power/input      ***
***-----------------------***
Vsupply VDD GND 1.8v
V1 Vds GND 1.8V
V2 Vgs GND 1.8V
***-----------------------***
***        circuit        ***
***-----------------------***
MN  Vds Vgs GND GND n_18_mm w=wn l=ln AD = 'ls * wn' AS = 'ls * wn' PD = '2*ls + wn' PS = '2*ls + wn'

***-----------------------***
***         alter         ***
***-----------------------***
.alter
.param wn = 0.54u
.param ln = 0.18u
```

```
39.
40. .end
```

Problem 3

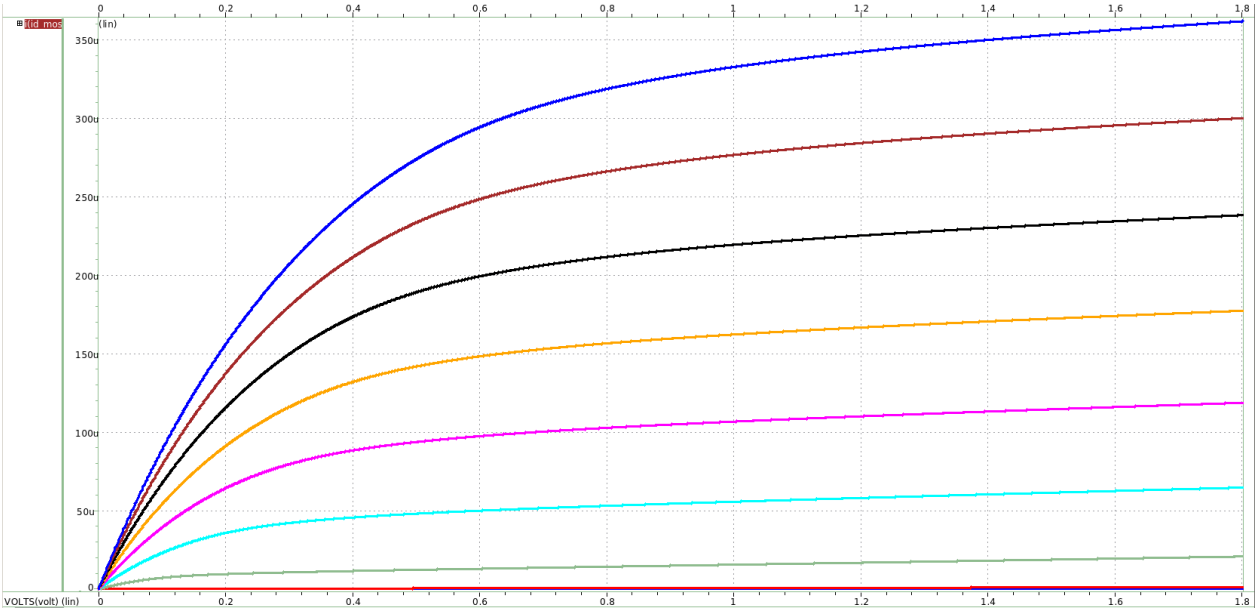


Fig 1. W/L=0.54/0.18um IV Curve (with perimeter)

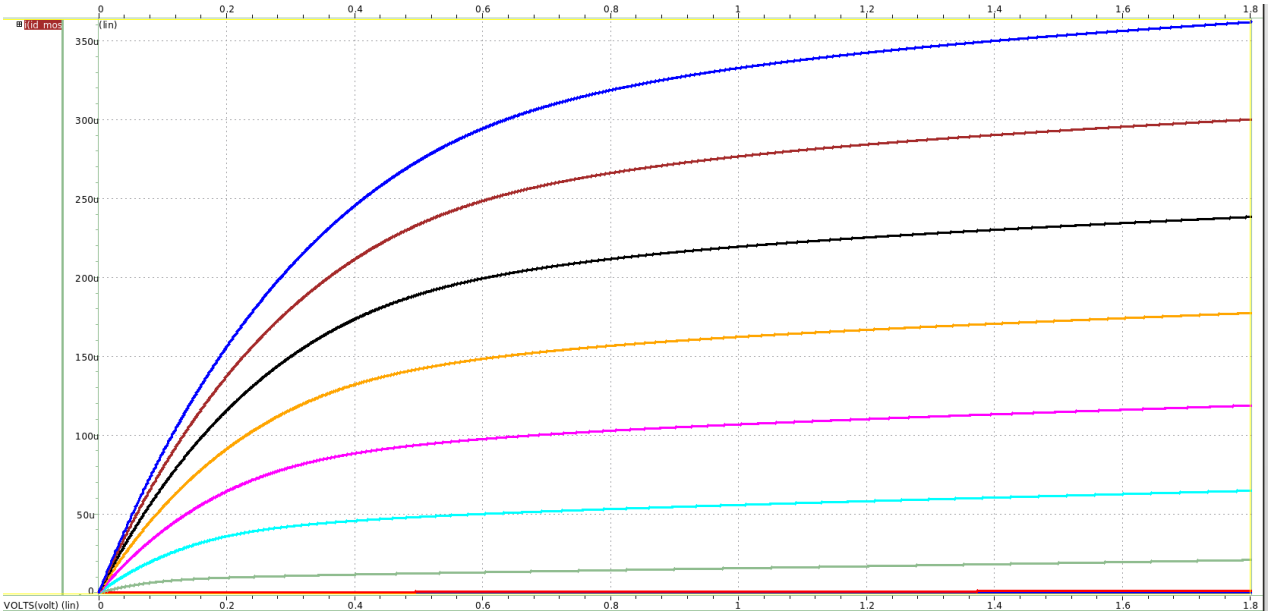
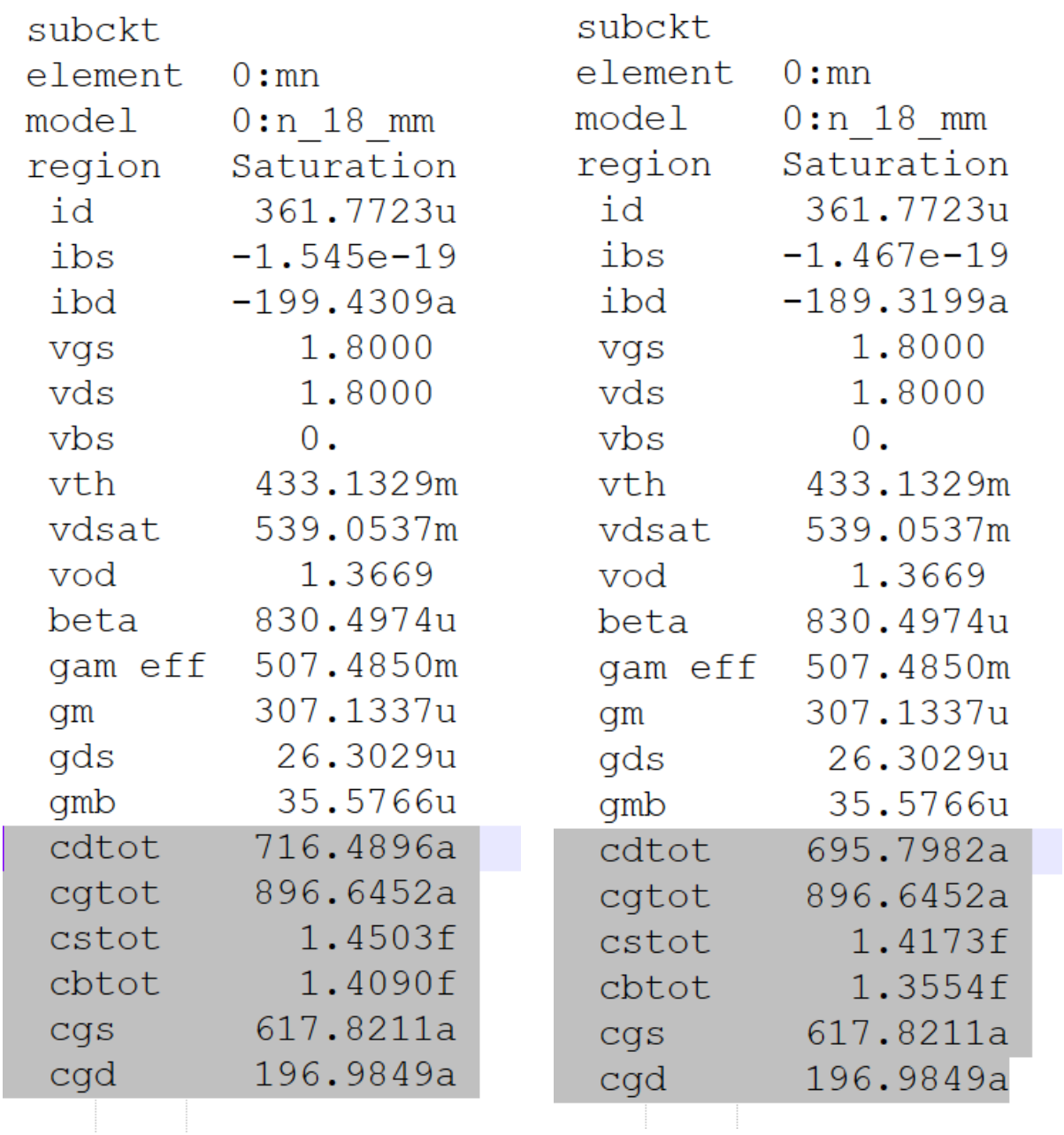


Fig 2. W/L=0.54/0.18um IV Curve (without perimeter)



subckt		subckt	
element	0:mn	element	0:mn
model	0:n_18_mm	model	0:n_18_mm
region	Saturation	region	Saturation
id	361.7723u	id	361.7723u
ibs	-1.545e-19	ibs	-1.467e-19
ibd	-199.4309a	ibd	-189.3199a
vgs	1.8000	vgs	1.8000
vds	1.8000	vds	1.8000
vbs	0.	vbs	0.
vth	433.1329m	vth	433.1329m
vdsat	539.0537m	vdsat	539.0537m
vod	1.3669	vod	1.3669
beta	830.4974u	beta	830.4974u
gam eff	507.4850m	gam eff	507.4850m
gm	307.1337u	gm	307.1337u
gds	26.3029u	gds	26.3029u
gmb	35.5766u	gmb	35.5766u
cdtot	716.4896a	cdtot	695.7982a
cgtot	896.6452a	cgtot	896.6452a
cstot	1.4503f	cstot	1.4173f
cbtot	1.4090f	cbtot	1.3554f
cgs	617.8211a	cgs	617.8211a
cgd	196.9849a	cgd	196.9849a

Fig 3. MOSFET Characteristics (left: without perimeter / right: with perimeter)

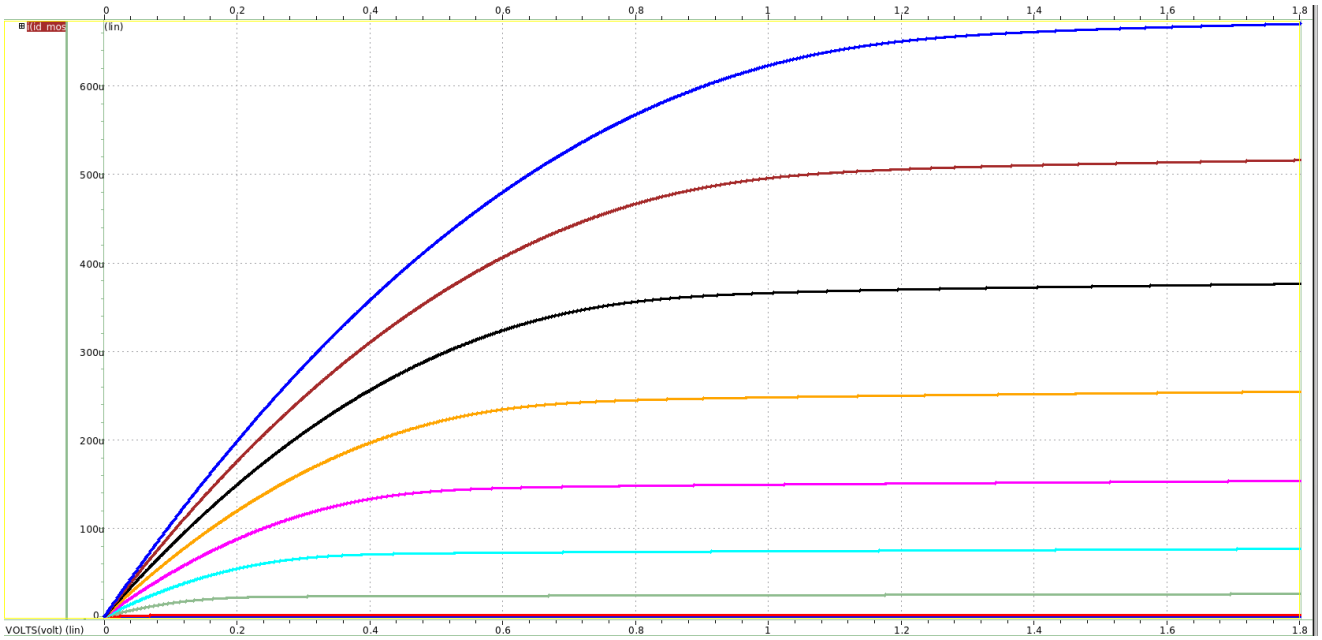


Fig 4. W/L=5.4/1.8um IV Curve (without perimeter)

Channel length modulation:

At high V_{ds}, the depletion region near the drain widens, causing the channel to "pinch off" near the drain. If we increase V_{ds} even further, the pinch off point moves closer to the source. This shortens the channel length, allowing more current to go through. In this case, I_D becomes dependent on V_{ds}, so we modify the original equation by introducing a *(1+* λV_{ds}*)* term.

$$I_D = \frac{1}{2} k V_{ov}^2 (1 + \lambda V_{ds})$$

(λ is the channel length modulation parameter)

This should make the simulated current higher than my hand calculation, which ignored channel length modulation. However, as observed in problem 2, this is not the case. I think it might be that there are other second-order effects present, further complicating things.

Velocity saturation:

When the drift velocity of charge carriers (electrons or holes) in the transistor channel reaches a maximum limit, despite further increases in the applied electric field. This occurs because at high electric fields, the carrier velocity no longer increases linearly with the field but instead saturates due to scattering effects. In short-channel MOSFETs, velocity saturation becomes significant. The current in the transistor becomes less sensitive to the gate voltage because increasing the field further does not increase the carrier velocity significantly. Notice that even though W/L=5.4um/1.8um & W/L=0.54um/0.18um have the same $\frac{W}{L}$ ratio, $\mathrm{I_D}$ increases more with $\mathrm{V_{gs}}$ when L = 1.8um.

What difference with specifying the area & perimeter make?

The current values in fig 1 & 2 look identical. It doesn't seem like adding area & perimeter to the simulation affected current. However, the parasitic capacitance was reduced after specifying the perimeter. This shows that parameters (area and perimeter) are essential for accurately modeling the parasitic capacitances and resistances in MOSFETs.