AIC HW2

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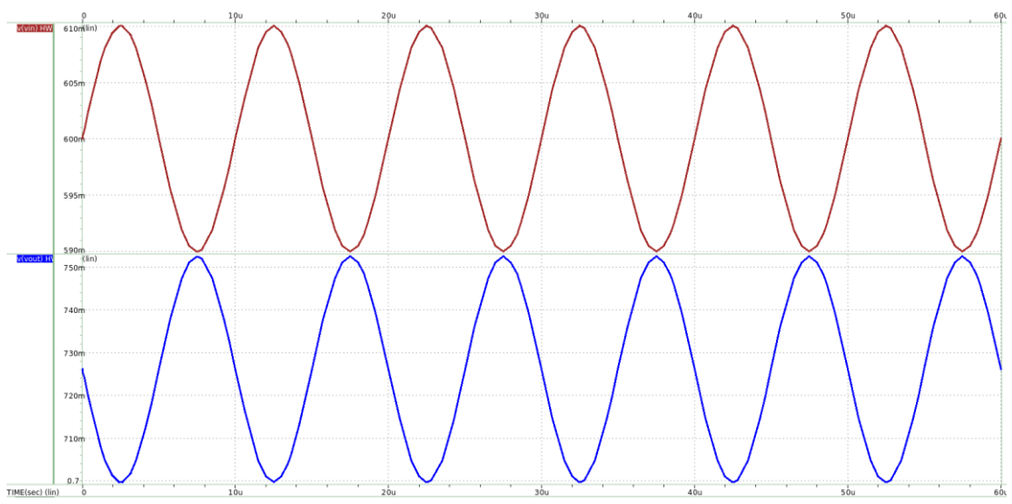
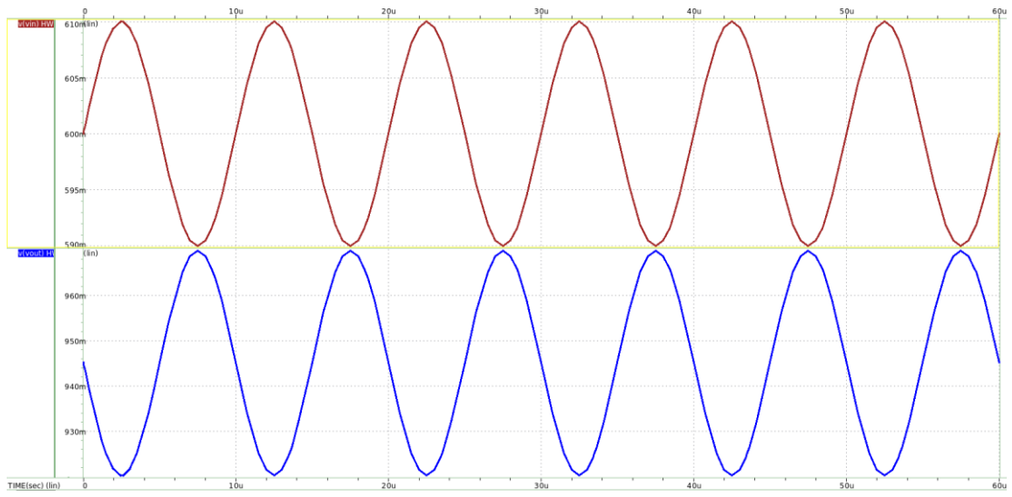
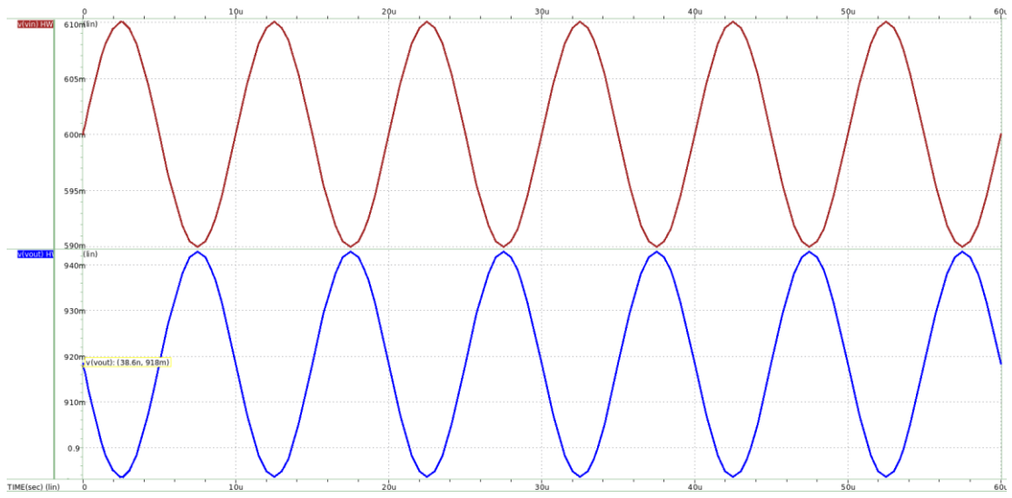
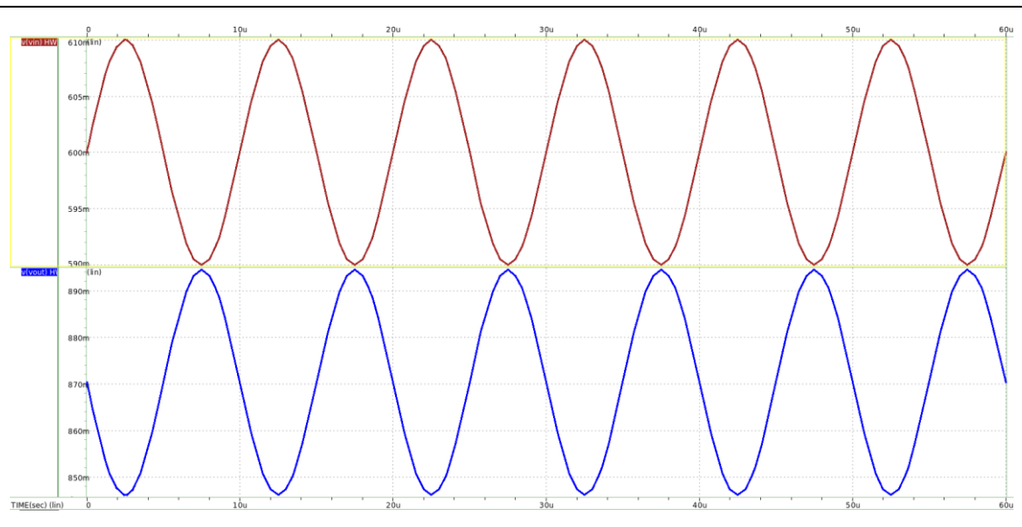
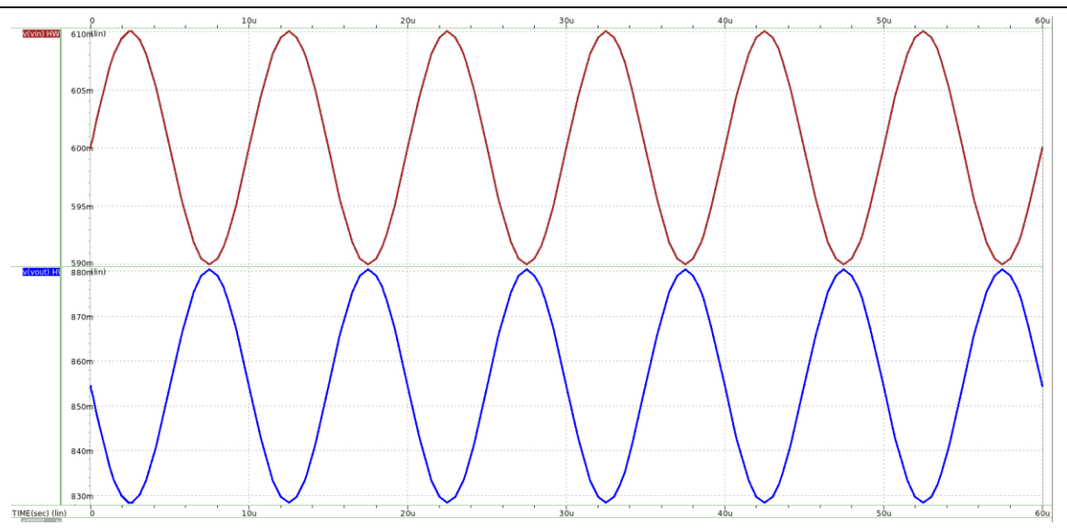
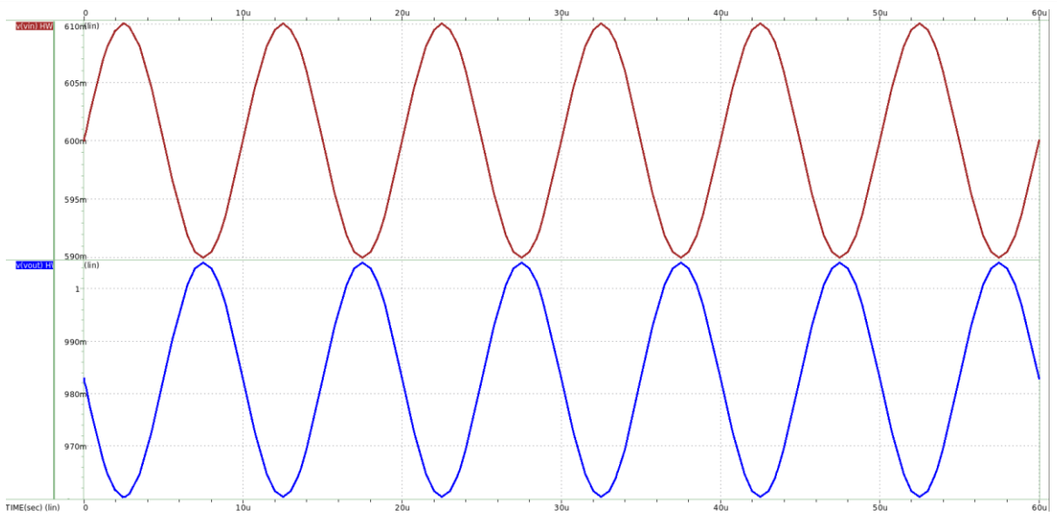
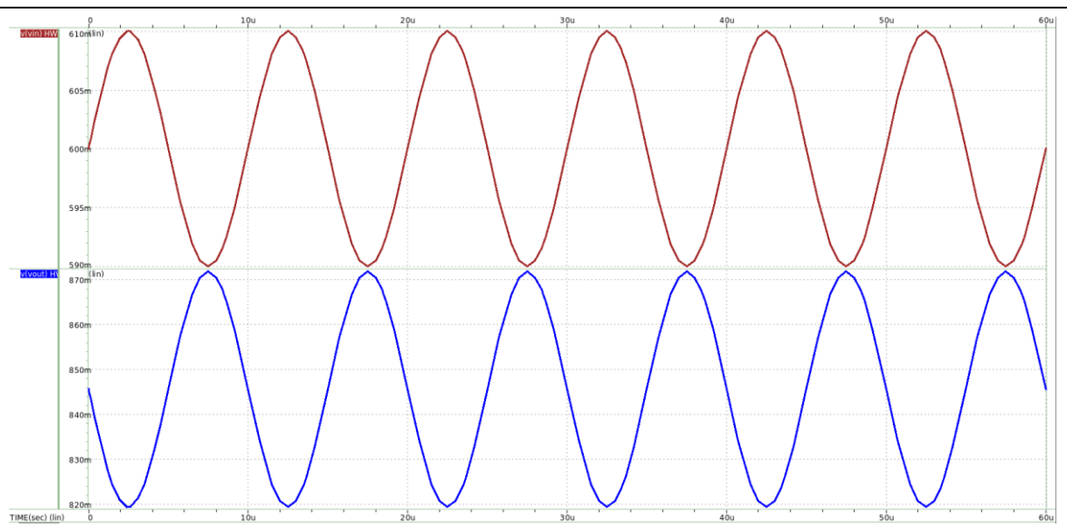
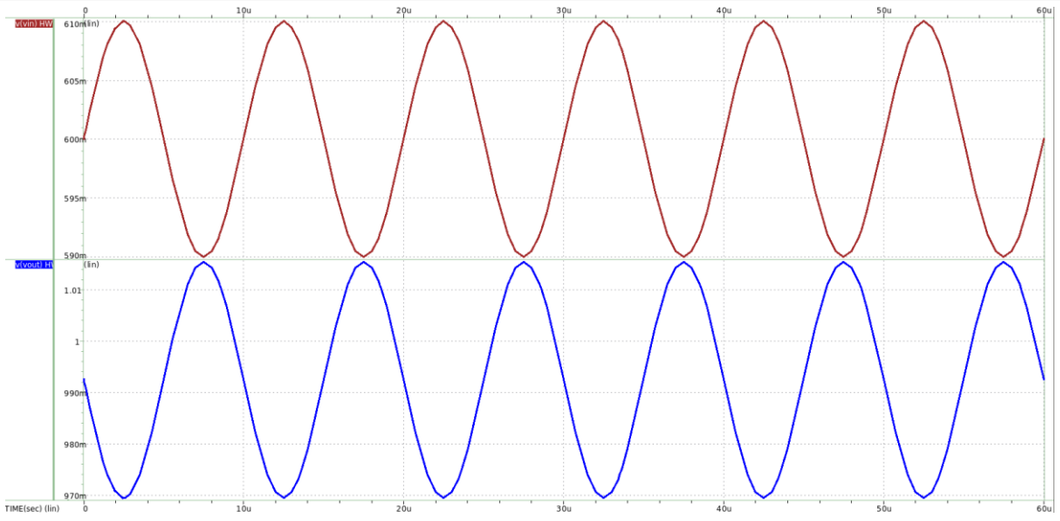
Problem 1

Corner	Temp (°C)	Circuit	Waveform	Vout (mV)	Ids (A)	DC gain (V/V)	Rout (Ω)	Cin (F)	Cout (F)
TT	25	(b)		726.117	42.4507u	-2.6400	7.3868k	37.8985f	47.3303f
TT	0	(a)		945.275	17.5753u	-2.4806	10.2106k	4.7420f	42.1002f
TT	25	(a)		918.353	20.6289u	-2.4679	9.8549k	4.7640f	42.1827f
TT	75	(a)		870.359	26.1780u	-2.4174	9.4633k	4.7856f	42.3225f

FF	25	(a)		854.429	33.0366u	-2.6042	7.6539k	4.8411f	42.4229f
SS	25	(a)		982.866	11.5971u	-2.2322	13.4338k	4.7264f	41.9959f
FnSp	25	(a)		845.718	25.5978u	-2.6229	9.0640k	4.6852f	42.4630f
SnFp	25	(a)		992.596	16.0392u	-2.2991	10.9135k	4.8468f	41.9022f

Code for Problem 1

```
***-----------------------***
***       setting       ***
***-----------------------***
.lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" tt
.TEMP 25
.op
***-----------------------***
***      simulation     ***
***-----------------------***
.option post
.option captab
.tf V(Vout) Vinput
.tran 0.01u 60u
.probe id_mos = I(MN)

***-----------------------***
***      parameters      ***
***-----------------------***
.param wn = 6u
.param ln = 0.9u
.param wp = 5u
.param lp = 1u
.global VDD GND

***-----------------------***
***      power/input     ***
***-----------------------***
Vsupply VDD GND 1.8v
*             SIN(Offset   Amplitude   Freq.   Delay )
Vinput Vin GND SIN(0.6V     0.01V      100k    0)
***-----------------------***
***       circuit       ***
***-----------------------***
MP  Vout    Vout    VDD     VDD    p_18_mm w=wp l=lp
MN  Vout    Vin     GND     GND    n_18_mm w=wn l=ln

***-----------------------***
***        alter        ***
***-----------------------***
.alter
.TEMP 0
.param wn = 2u
.param ln = 0.3u

.alter
.TEMP 25
.param wn = 2u
.param ln = 0.3u

.alter
.TEMP 75
.param wn = 2u
.param ln = 0.3u

```

```
55. .end
```

Problem 2

Corner	Temp (°C)	Circuit	Rout (Ω)	Av (V/V)
TT	25	(a)	9.8549k	-2.4679
TT	25	(b)	7.3868k	-2.6400
TT	75	(a)	9.4633k	-2.4174
TT	75	(b)	7.6529k	-2.5072

Relationship Between MOSFET Dimensions & Resistance:

- The resistance difference between circuit (a) & (b) might be caused by short channel effects like velocity saturation. Velocity saturation occurs when the electric field in the channel becomes so strong that the carrier velocity (electrons or holes) reaches a maximum value and cannot increase further, despite increases in the electric field. This effectively increases the resistance of the channel. The effect is more pronounced in smaller MOSFETs. Therefore, even though 6μm/0.9μm & 2μm/0.3μm are of the same ratio, circuit (a) has higher R_{out}.

Temperature's impact on MOSFETs:

- As temperature rises, more charge carriers are thermally generated, which reduces the voltage needed to form the conductive channel. This can lead to increased conduction (more current flow) at lower gate voltages. According to Sedra Smith's Microelectronic Circuits, the magnitude of V_{th} decreases by about 2mV per 1 °C rise in temperature. Reduced threshold voltage can shift the operating point of the MOSFET.
- As for the gain, $A_v. = -g_m r_o.$

  Both g_m and r_o typically decrease with temperature, this often results in a net decrease in voltage gain as

temperature rises.

Code for Problem 2

```
***-----------------------***
***       setting       ***
***-----------------------***
.lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" tt
.TEMP 25
.op
***-----------------------***
***      simulation     ***
***-----------------------***
.option post
.option captab
.tf V(Vout) Vinput
.tran 0.01u 60u
.probe id_mos = I(MN)

***-----------------------***
***      parameters      ***
***-----------------------***
.param wn = 2u
.param ln = 0.3u
.param wp = 5u
.param lp = 1u
.global VDD GND

***-----------------------***
***      power/input     ***
***-----------------------***
Vsupply VDD GND 1.8v
*             SIN(Offset   Amplitude   Freq.   Delay )
Vinput Vin GND SIN(0.6V     0.01V      100k    0)
***-----------------------***
***       circuit        ***
***-----------------------***
MP  Vout    Vout    VDD     VDD    p_18_mm w=wp l=lp
MN  Vout    Vin     GND     GND    n_18_mm w=wn l=ln

***-----------------------***
***        alter         ***
***-----------------------***
.alter
.param wn = 6u
.param ln = 0.9u

.alter
.TEMP 75
.param wn = 2u
.param ln = 0.3u
```

```
48.
49. .alter
50. .TEMP 75
51. .param wn = 6u
52. .param ln = 0.9u
53.
54. .end
```

Problem 3

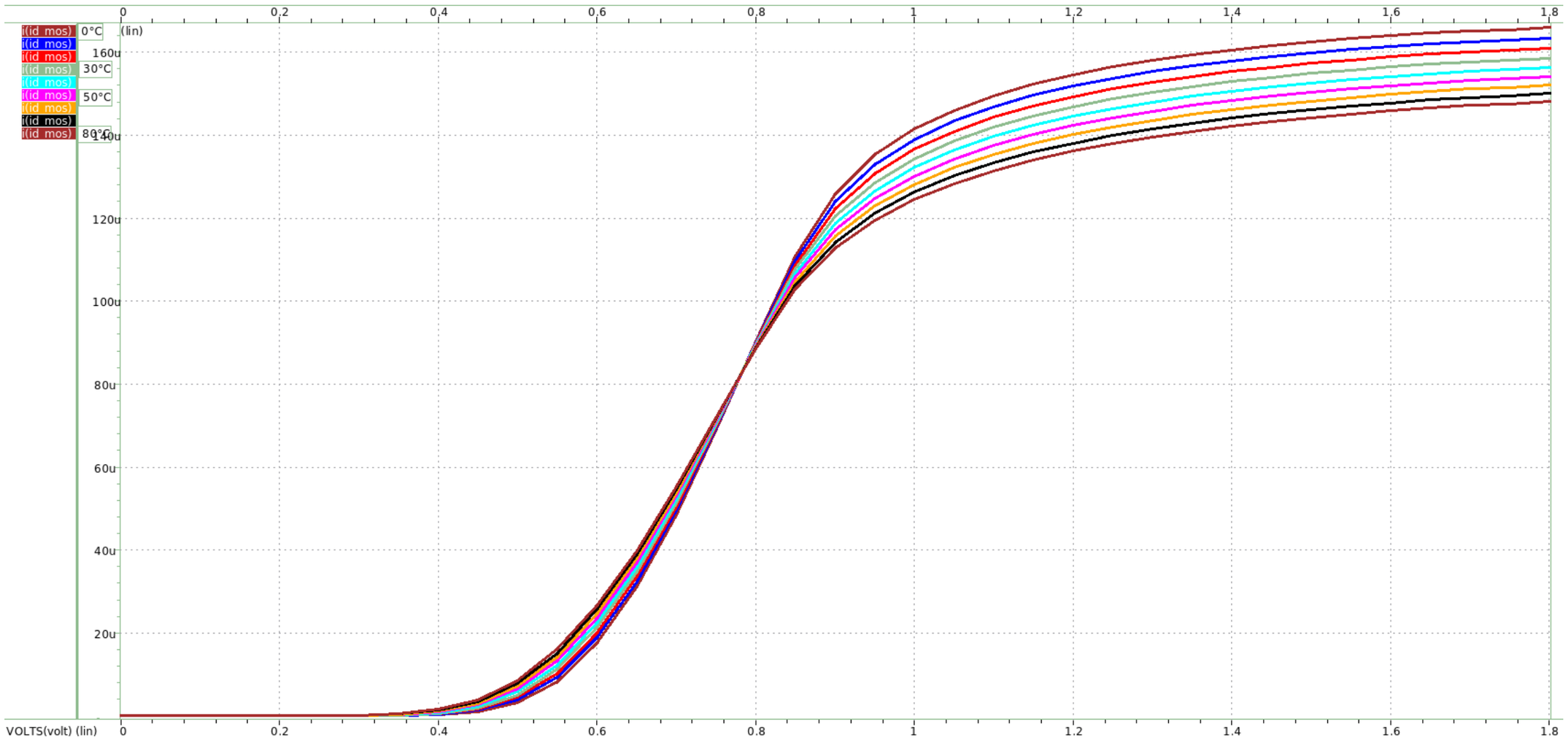


Fig 1. Circuit(a) I_D-V_{GS} Curve at Temperatures 0 ~ 80 °C

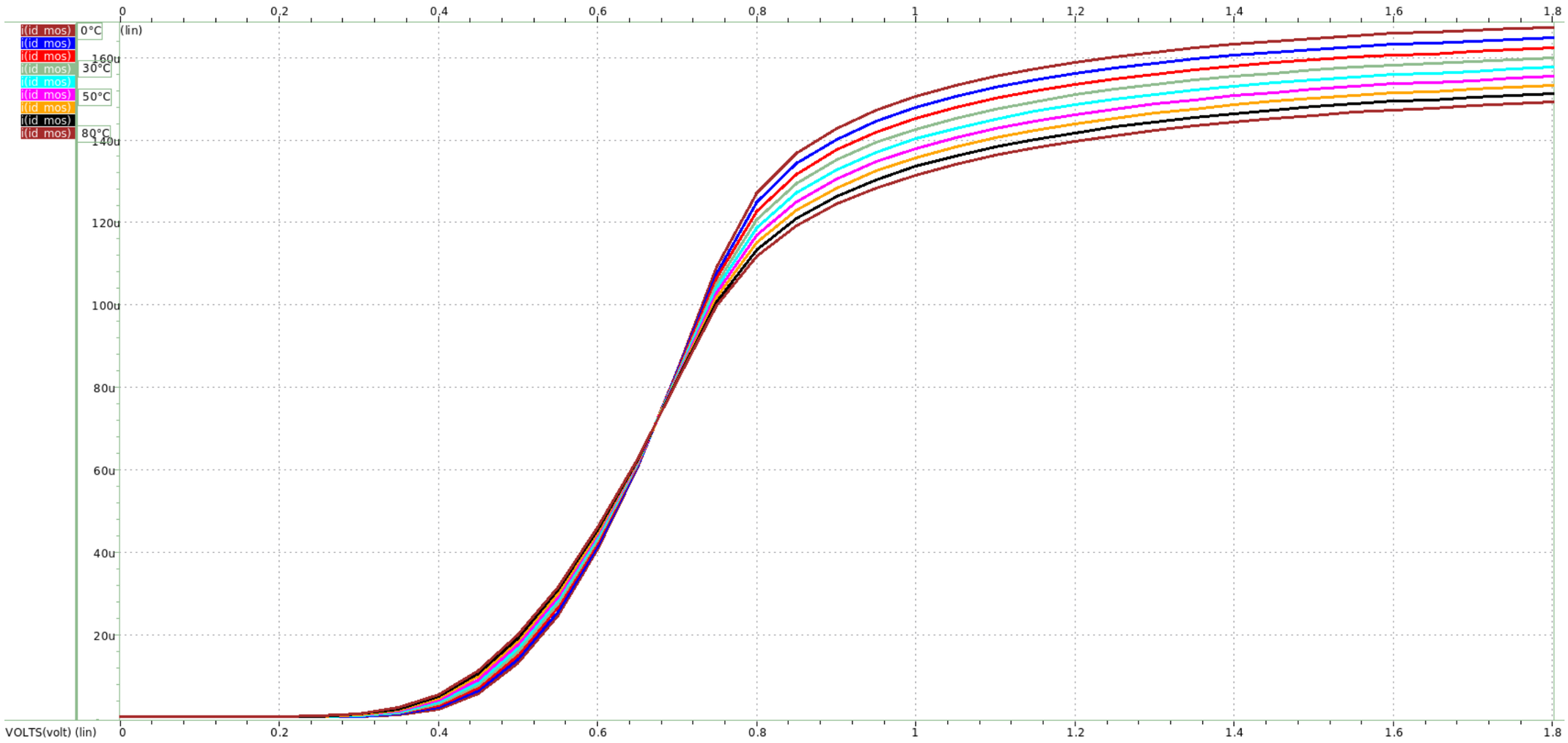


Fig 2. Circuit(b) I_D-V_{GS} Curve at Temperatures 0 ~ 80 °C

- I_D increases very slightly with temperature at lower V_{GS} but decreases with temperature at higher V_{GS}. Let first examine how temperature affects electrons/holes. Temperature has 2 effects on carriers:
  1. Higher temperatures can increase the number of carriers through thermal generation. This is likely what leads to the decrease in V_{th} as mentioned in problem 2.
  2. Carrier mobility typically decreases with temperature due to increased lattice vibrations (phonon scattering).
- I believe that at lower V_{GS}. the effect of increasing carrier concentration takes dominance, and higher temperatures allow more current to flow through. However, at higher V_{GS}, the slowing effect is more dominant. Increased lattice vibrations lead to more frequent collisions between carriers and the crystal lattice, so the higher the temperature, the less the current.

Code for Problem 3

```
1. ***-----------------------***
2. ***        setting        ***
3. ***-----------------------***
4. .lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" tt
5. .TEMP T
6. .op
```

```
***-----------------------***
***       simulation      ***
***-----------------------***
.option post
.DC Vgs  0V 1.8V 0.05V sweep T 0 80 10
.probe id_mos = I(MN)

***-----------------------***
***      parameters       ***
***-----------------------***
.param wn = 6u
.param ln = 0.9u
.param wp = 5u
.param lp = 1u
.global VDD GND

***-----------------------***
***      power/input      ***
***-----------------------***
Vsupply VDD GND 1.8v
*             SIN(Offset   Amplitude   Freq.   Delay )
Vgs     Vin GND 1.8v
***-----------------------***
***        circuit        ***
***-----------------------***
MP  Vout    Vout    VDD     VDD    p_18_mm w=wp l=lp
MN  Vout    Vin     GND     GND    n_18_mm w=wn l=ln

.end
```