Homework #4 of「類比積體電路導論」

作業繳交截止日期: Oct. 29, 2024 12:00 (上傳 E3 數位平台繳交)

本次作業共三大題, 4.1~4.3

請將作業轉成一個 PDF 檔案(file size 小於 10MB)，檔名請使用「AIC_HW4_自己的學號」(例如: AIC_HW4_109700018)，於作業繳交截止日期/時間前，上傳到指定的 E3 數位平台繳交。

Unless otherwise stated, in the following problems, use the device data shown in Table 1 and assume that $V_{DD} = 3V$. The Dielectric constant of gate oxide is 3.9 and $\varepsilon_o = 8.854 \times 10^{-12} F/m$.

Table 1. Level 1 SPICE models for NMOS and PMOS devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body-effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate-oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

- Hint: The calculation of capacitance of MOS.
  - $C_{ov} = C_{ox}L_D$
  - $C_{gd} = C_{gd0}W$
  - $C_{gs} = \frac{2}{3}W(L - 2L_D)C_{ox} + WC_{ov}$
  - $C_{db} = C_{bo}WL_j + C_{sw}(2W + 2L_j)$
  - $L_j = 1.5\ \mu m\ (length\ of\ junction)$
  - $C_{bo} = \frac{C_j}{(1+\frac{V_R}{PB})^{MJ}}$, $C_{sw} = \frac{C_{jsw}}{(1+\frac{V_R}{PB})^{MJSW}}$

4.1 A source follower is shown in Fig. 4.1.

(a) Derive the output impedance $Z_{out}(S)$ in terms of g_m, R_s, and C_{gs}. (20 pts)

(b) If the source follower employ a NMOS M1 with $(W/L)_1$ = 50µm/0.5µm and a bias current of 1 mA. Assume that $\lambda = \gamma = 0$. M1 is driven by a source impedance R_s of 20 kΩ. Source/ drain side diffusion is needed to take into consideration. Explain why the output impedance is inductive (10 pts) and calculate the equivalent inductance seen at the output (10 pts).

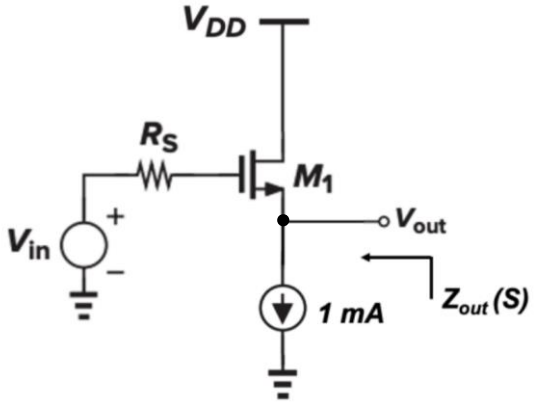

Fig. 4.1

4.2 The common-gate stage of Fig. 4.2 is designed with $(W/L)_1 = 50/0.5$, $I_{D1} = 1$ mA, $R_D = 2$ kΩ, $R_S = 1$ kΩ, $C_S = 1.012 \times 10^{-13} F$, and $C_D = 27.14 fF$. Assuming $\lambda=0$, $\gamma\neq0$, and $V_b=1.45$V, determine the input and output poles ($\omega_{p,in}$ and $\omega_{p,out}$) and the low-frequency gain. (30 pts)

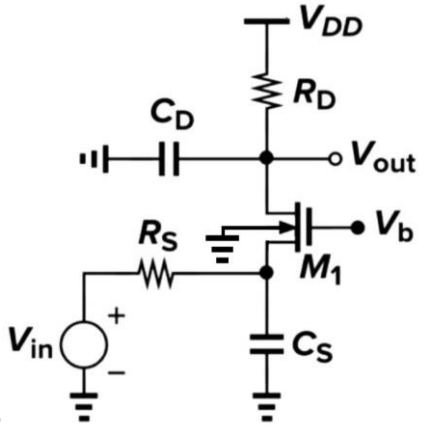

Fig. 4.2

4.3 The CS stage of Fig. 4.3 is designed with $(W/L)_1 = 50/0.5$, $R_S = 2$kΩ, and $R_D = 2$kΩ. If $I_{D1} = 1$ mA, determine the poles and the zero of the circuit. Need to consider C_{gs}, C_{gd} and C_{db}. Assume $\lambda=0$, $\gamma=0$. (30 pts)

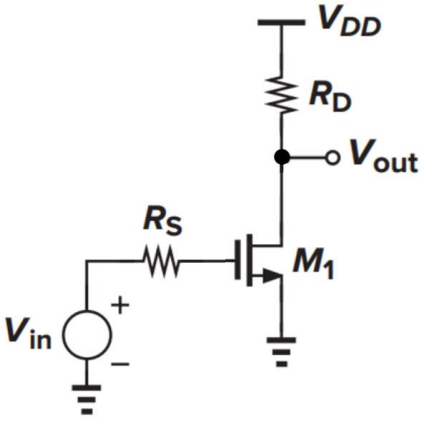

Fig. 4.3