Homework #6 of「類比積體電路導論」

作業繳交截止日期: Nov. 28, 2024 12:00 (上傳 E3 數位平台繳交)

本次作業共三大題, 6.1~6.3

請將作業轉成一個 PDF 檔案(file size 小於 10MB)，檔名請使用「AIC_HW6_自己的學號」(例如: AIC_HW6_109700018)，於作業繳交截止日期/時間前，上傳到指定的 E3 數位平台繳交。

Unless otherwise stated, in the following problems, use the device data shown in Table 1 and assume that $V_{DD} = 3V$. The Dielectric constant of gate oxide is 3.9 and $\varepsilon_o = 8.854 \times 10^{-12} F/m$.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body-effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate-oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

6.1 Using feedback techniques, calculate the input and output impedances of each circuit at relatively low frequencies in Fig 1. Neglecting channel length modulation.

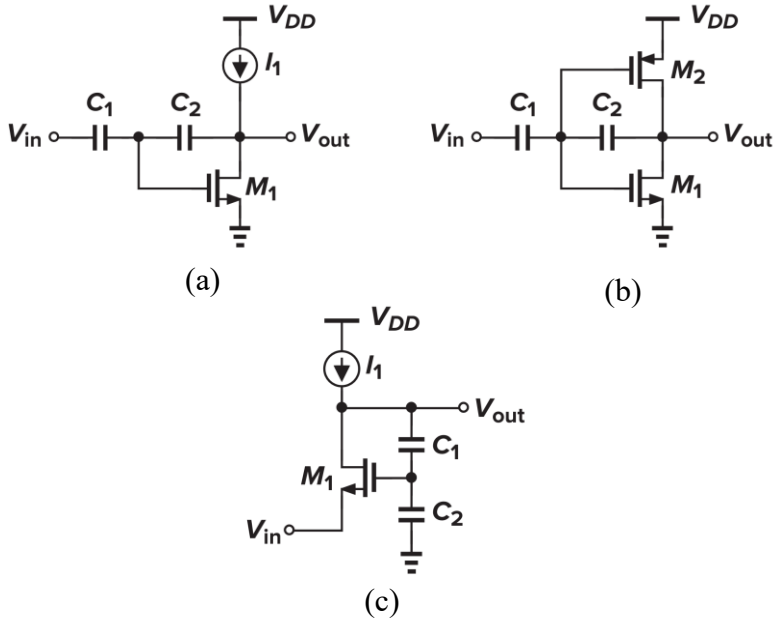

Fig. 1

6.2 In the circuit of Fig. 2, $(W/L)_{1\text{-}3}$ = 50/0.5, $I_{D1} = |I_{D2}| = |I_{D3}|$ = 0.5 mA, and $R_{S1} = R_F = R_{D2}$ = 2 kΩ. Neglecting channel length modulation of M1 and if γ = 0.

(a) Determine the input bias voltage required to establish the above currents.

(b) Calculate the closed-loop voltage gain and output resistance.

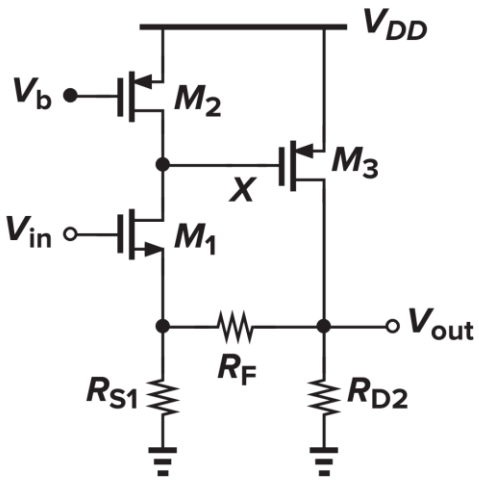

Fig. 2

6.3 In the circuit of Fig. 3, assume that $\lambda = 0$, $g_{m1,2} = 10$ mS, $R_{1\text{-}3} = 3$ kΩ, and $C_1 = 100$ pF. Neglecting channel length modulation and other capacitances, estimate the closed-loop voltage gain at very low and very high frequencies.

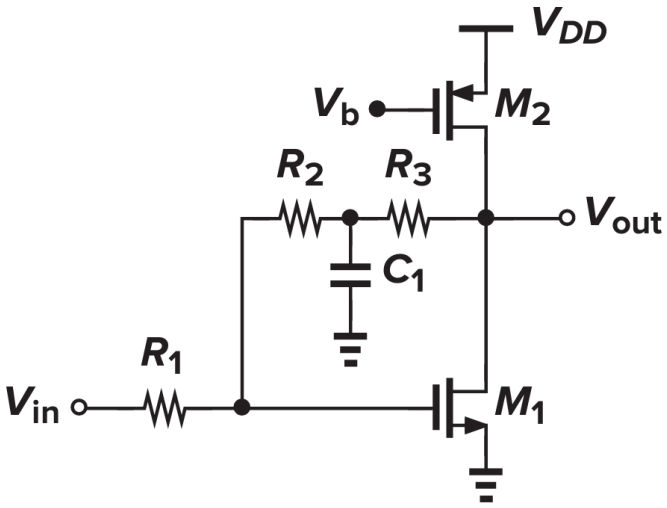

Fig. 3