AIC HW3

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Problem 1:

	Acm (V/V)	Adm (V/V)	CMRR (V/V)
(a)	165.6810m	-13.4153	79.7635
(b)	37.1281m	-4.0028	107.8105

Problem 1 code:

```
***-----------------------***
***         setting        ***
***-----------------------***
.lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" tt
.TEMP 25
.op
***-----------------------***
***        simulation      ***
***-----------------------***
.option post
.tran 0.1n 30u
.probe I(M1_n)
.probe I(M2_n)
.probe Vout=V(x,y)
*.DC Vgs  0V 1.8V 0.05V sweep T 0 80 10

***-----------------------***
***       parameters       ***
***-----------------------***
.global VDD GND Vbs Vb

***-----------------------***
***        measure         ***
***-----------------------***
```

```
.meas tran Vx_max  max  v(x)   from=0.1ns to=30us
.meas tran Vx_min  min  v(x)   from=0.1ns to=30us
.meas tran Vx_Vpp  param ='Vx_max - Vx_min'

.meas tran Vy_max  max  v(y)   from=0.1ns to=30us
.meas tran Vy_min  min  v(y)   from=0.1ns to=30us
.meas tran Vy_Vpp  param ='Vy_max - Vy_min'

.meas tran Vin_max  max  v(V_diff+)   from=0.1ns to=30us
.meas tran Vin_min  min  v(V_diff+)   from=0.1ns to=30us
.meas tran Vin_Vpp  param ='Vin_max-Vin_min'

.meas tran Vout_max  param ='Vx_max - Vy_min'
.meas tran Vout_min  param ='Vx_min - Vy_min'
.meas tran Vout_Vpp  param ='Vout_max - Vout_min'

.meas tran Vdiff_max  max  v(Vdiff)   from=0.1ns to=30us
.meas tran Vdiff_min  min  v(Vdiff)   from=0.1ns to=30us
.meas tran Vdiff_Vpp  param ='Vdiff_max - Vdiff_min'

.meas tran Adm  param ='-Vout_Vpp / Vdiff_Vpp'
*.meas tran Acm  param ='-Vx_Vpp / Vin_Vpp'
*.meas tran CMRR  param ='Adm / Acm'

*MAX tells Hspice to take the max value of V/I of variable during t1 ~ t2
***-----------------------***
***       power/input      ***
***-----------------------***
Vsupply VDD GND 3v
*              SIN(Offset   Amplitude   Freq.   Delay )
V1      Vbs GND 0.6v
V2      Vb  GND 2v
Vcm     N0  GND 1v
V4      Vdiff  GND SIN(0   1m   100k  0)
EV+     V_diff+ N0 Vdiff GND +0.5
EV-     V_diff- N0 Vdiff GND -0.5
***-----------------------***
***        circuit       ***
```

```
***----------------------***
R1  VDD  X   5k
R2  VDD  Y   5k
M1_n  X  V_diff+    Virtual      GND    n_18_mm w=45u l=0.3u
M2_n  Y  V_diff-    Virtual      GND    n_18_mm w=45u l=0.3u
M5_n  Virtual  Vbs        GND     GND    n_18_mm w=75u l=1u

.subckt CKT_A   Vin_pos Vin_neg  X   Y
R1  VDD  X   5k
R2  VDD  Y   5k
M1_n  X  Vin_pos    V       GND    n_18_mm w=45u l=0.3u
M2_n  Y  Vin_neg    V       GND    n_18_mm w=45u l=0.3u
M5_n  V  Vbs        GND     GND    n_18_mm w=75u l=1u
.ends

.subckt CKT_B   Vin_pos Vin_neg  X   Y
M3_p  X  X          VDD     VDD    p_18_mm w=10u l=0.3u
M4_p  Y  Y          VDD     VDD    p_18_mm w=10u l=0.3u
M1_n  X  Vin_pos    V       GND    n_18_mm w=45u l=0.3u
M2_n  Y  Vin_neg    V       GND    n_18_mm w=45u l=0.3u
M5_n  V  Vbs        GND     GND    n_18_mm w=75u l=1u
.ends

.subckt CKT_C   Vin_pos Vin_neg  X   Y
M3_p  X  Vb         VDD     VDD    p_18_mm w=10u l=0.3u
M4_p  Y  Vb         VDD     VDD    p_18_mm w=10u l=0.3u
M1_n  X  Vin_pos    V       GND    n_18_mm w=45u l=0.3u
M2_n  Y  Vin_neg    V       GND    n_18_mm w=45u l=0.3u
M5_n  V  Vbs        GND     GND    n_18_mm w=75u l=1u
.ends

.end
```

Problem 2:

Derivation of Max Input Amplitude & Output Swing:

$\beta = k = \mu C_{ox} \frac{W}{L}$

$M1, 2: \quad \beta = k = 49.4970m$

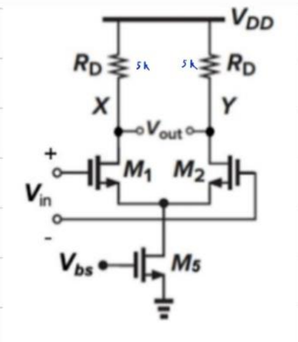
$V_{th} = 524.9338m$

$M3, 4: \quad \beta = k = 2.2610m$

$V_{th} = -518.0554m$

$M5: \quad \beta = k = 22.6916m \qquad I_d = 501.3930\mu A = I_{ss}$

$V_{th} = 385.0746m$



(a)

$V_{out,max} = 3V$

$V_{out,min} = 1 - 0.5249338$

$= 0.4750662V$

$0.4751V \le V_{out} \le 3V$

$V_{out,bias} = V_{ds5} + V_{ds1}$

$= 0.40582 + 1.3417$

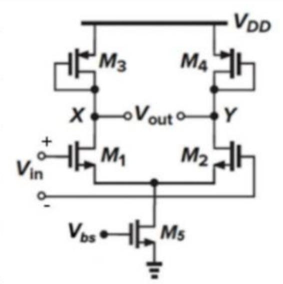
$= 1.74752$

Output Swing $= 2 \min(V_{out,bias} - V_{out,min}, V_{out,max} - V_{out,bias})$

$= 2(3 - 1.74752)$

$= 2.50496$ #

$$\frac{\min(V_{out,bias} - V_{out,min}, V_{out,max} - V_{out,bias})}{|A_{dm}|} = \frac{3 - 1.74752}{-13.4153} = 0.09336V \ \#$$



(b)

$V_{out,max} = V_{DD} - |V_{th_p}|$

$= 3 - 0.5180554$

$= 2.4819$

$I_d = 501.3930\mu A$

$= \frac{1}{2} \cdot 2.2610m \cdot (V_{sg_3} - 518.0554m)^2$

$V_{sg_3} = 1.18402$

$V_{out,min} = 3 - 1.18402$

$= 1.81598$

$1.81598 \le V_{out} \le 2.4819$

$V_{out,bias} = V_{ds5} + V_{ds1}$

$= 0.4109556 + 1.5972$

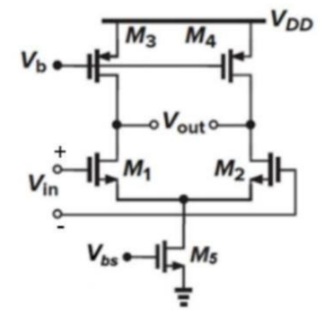
$= 2.0081556V$

Output Swing $= 2 \min(V_{out,bias} - V_{out,min}, V_{out,max} - V_{out,bias})$

$= 2(2.0081556 - 1.81598)$

$= 384.351mV$ #

$$\frac{\min(V_{out,bias} - V_{out,min},\ V_{out,max} - V_{out,bias})}{|A_{dm}|} = \frac{2.0081556 - 1.81598}{4.0028} = 0.04801\,V \quad \#$$



(c)

$$V_{ds,max} = 3 - 1.18402 + 0.5180554$$
$$= 2.33403$$
$$V_{out,min} = 1 - 0.5249338$$
$$= 0.47507$$

$$0.47507 \leq V_{out} \leq 2.33403$$

$$V_{out,bias} = V_{ds5} + V_{ds1}$$
$$= 0.4148495 + 1.7928$$
$$= 2.2076495$$

$$\frac{\min(V_{out,bias} - V_{out,min},\ V_{out,max} - V_{out,bias})}{|A_{dm}|} = \frac{2.33403 - 2.2076495}{30.736} = 0.004112 \quad \#$$

$$\text{Output Swing} = 2\min(V_{out,bias} - V_{out,min},\ V_{out,max} - V_{out,bias})$$
$$= 2(2.33403 - 2.2076495)$$
$$= 252.761\,mV \quad \#$$

	DC Gain (V/V)	Vout, bias (V)	Vout, min (V)	Vout, max (V)	Output Swing (V)	Max Input Signal Amplitude (V)
(a)	-13.4151	1.748	0.475	3	2.505	93.36m
(b)	-4.0028	2.008	1.816	2.482	384.351m	48.01m
(c)	-30.7332	2.208	0.475	2.334	252.761m	4.112m

The circuits (a), (b), (c) are identical to 2.2 of handwrite handwork 2. We can use the same calculation methods employed in the handwrite homework to acquire the Vout, max & Vout, min.

The maximum output swing is defined as the difference between the maximum and minimum output voltages. This is limited by the bias voltage Vout, bias caused by setting Vicm to 1V. The output swing is given by the following equation:

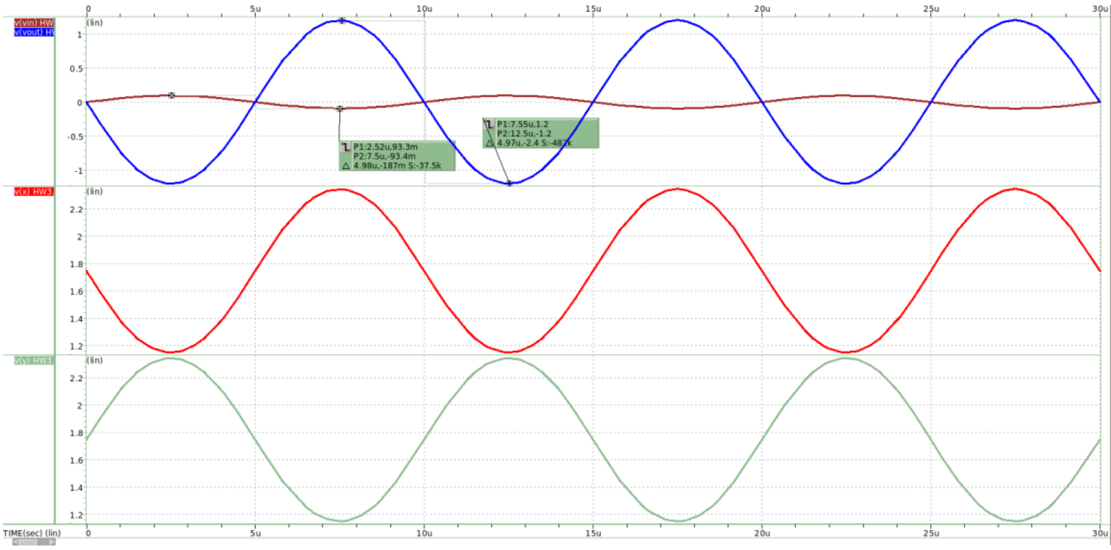
$$Output\ Swing = 2\min(V_{out,max}\text{-}V_{out,bias}, V_{out,bias}\text{-}V_{out,min})$$

Next, to determine the max amplitude of the input signal, I use the following equation:

$$\frac{\min(V_{out,max}\text{-}V_{out,bias}, V_{out,bias}\text{-}V_{out,min})}{|A_{dm}|} = Max\ Input\ Amplitude$$

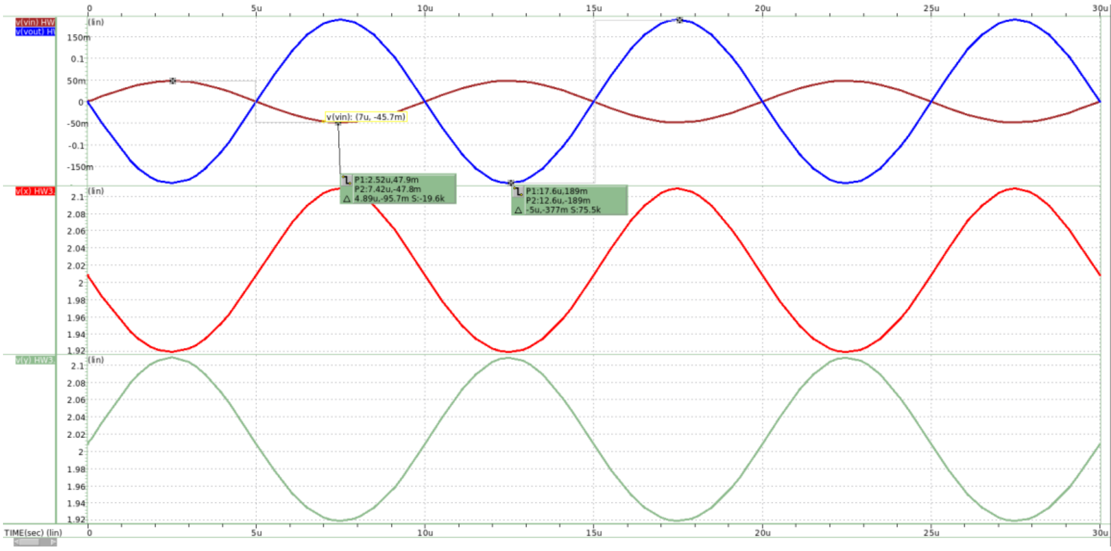
This helps us find a suitable input that satisfies the requirement of the problem and keeps all transistors in saturation.

Circuit (a) Waveform & MOSFET Operating Region:



subckt			
element	0:m1_n	0:m2_n	0:m5_n
model	0:n_18_mm	0:n_18_mm	0:n_18_mm
region	Saturation	Saturation	Saturation
id	250.5004u	250.5004u	501.0008u
ibs	-1.3174f	-1.3174f	-7.450e-20
ibd	-5.6727f	-5.6727f	-2.1759f
vgs	594.1752m	594.1752m	600.0000m
vds	1.3417	1.3417	405.8248m
vbs	-405.8248m	-405.8248m	0.
vth	529.9849m	529.9849m	385.1133m
vdsat	114.5085m	114.5085m	200.5304m
vod	64.1902m	64.1902m	214.8867m
beta	49.4812m	49.4812m	22.6916m
gam eff	517.7531m	517.7531m	507.4463m
gm	3.8757m	3.8757m	4.0909m

Circuit (b) Waveform & MOSFET Operating Region:

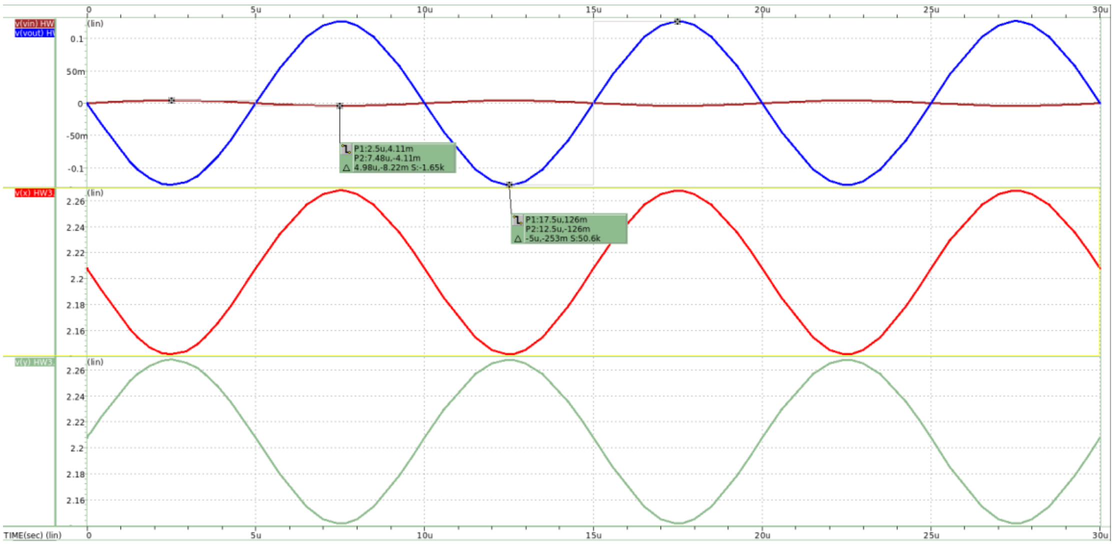


**** mosfets

subckt

element	0:m3_p	0:m4_p	0:m1_n	0:m2_n	0:m5_n
model	0:p_18_mm	0:p_18_mm	0:n_18_mm	0:n_18_mm	0:n_18_mm
region	Saturation	Saturation	Saturation	Saturation	Saturation
id	-250.6965u	-250.6965u	250.6965u	250.6965u	501.3930u
ibs	2.453e-20	2.453e-20	-1.3341f	-1.3341f	-7.456e-20
ibd	466.5857a	466.5857a	-6.5188f	-6.5188f	-2.2034f
vgs	-991.8423m	-991.8423m	589.0444m	589.0444m	600.0000m
vds	-991.8423m	-991.8423m	1.5972	1.5972	410.9556m
vbs	0.	0.	-410.9556m	-410.9556m	0.
vth	-518.0554m	-518.0554m	524.9338m	524.9338m	385.0746m
vdsat	-444.3561m	-444.3561m	114.4061m	114.4061m	200.5587m
vod	-473.7869m	-473.7869m	64.1106m	64.1106m	214.9254m
beta	2.2610m	2.2610m	49.4970m	49.4970m	22.6916m
gam eff	557.0903m	557.0903m	517.8721m	517.8721m	507.4463m
gm	854.6328u	854.6328u	3.8902m	3.8902m	4.0941m

Circuit (c) Waveform & MOSFET Operating Region:



subckt					
element	0:m3_p	0:m4_p	0:m1_n	0:m2_n	0:m5_n
model	0:p_18_mm	0:p_18_mm	0:n_18_mm	0:n_18_mm	0:n_18_mm
region	Saturation	Saturation	Saturation	Saturation	Saturation
id	-250.8435u	-250.8435u	250.8435u	250.8435u	501.6869u
ibs	2.455e-20	2.455e-20	-1.3467f	-1.3467f	-7.460e-20
ibd	372.7140a	372.7140a	-7.1666f	-7.1666f	-2.2243f
vgs	-1.0000	-1.0000	585.1505m	585.1505m	600.0000m
vds	-792.3054m	-792.3054m	1.7928	1.7928	414.8495m
vbs	0.	0.	-414.8495m	-414.8495m	0.
vth	-518.0583m	-518.0583m	521.0531m	521.0531m	385.0451m
vdsat	-450.7120m	-450.7120m	114.3540m	114.3540m	200.5802m
vod	-481.9417m	-481.9417m	64.0974m	64.0974m	214.9549m
beta	2.2567m	2.2567m	49.5082m	49.5082m	22.6916m
gam eff	557.0903m	557.0903m	517.9622m	517.9622m	507.4463m
gm	834.7725u	834.7725u	3.9006m	3.9006m	4.0966m

Code for Problem 2 & 3:

```
***-----------------------***
***        setting        ***
***-----------------------***
.lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" tt
.TEMP 25
.op
```

```
***-----------------------***
***       simulation      ***
***-----------------------***
.option post
.tran 0.1n 30u
.probe I(M1_n)
.probe I(M2_n)
.probe Vout=V(x,y)
*.DC Vgs  0V 1.8V 0.05V sweep T 0 80 10

***-----------------------***
***      parameters       ***
***-----------------------***
.global VDD GND Vbs Vb
***-----------------------***
***      power/input      ***
***-----------------------***
Vsupply VDD GND 3v
*              SIN(Offset   Amplitude   Freq.   Delay )
V1      Vbs GND 0.6v
V2      Vb  GND 2v
Vcm     N0  GND 1v
V4      Vdiff  GND SIN(0   1m   100k  0)
EV+     V_diff+ N0 Vdiff GND +0.5
EV-     V_diff- N0 Vdiff GND -0.5
***-----------------------***
***        circuit        ***
***-----------------------***
R1  VDD  X   5k
R2  VDD  Y   5k
M1_n  X  V_diff+    Virtual      GND    n_18_mm w=45u l=0.3u
M2_n  Y  V_diff-    Virtual      GND    n_18_mm w=45u l=0.3u
M5_n  Virtual  Vbs        GND     GND    n_18_mm w=75u l=1u

.subckt CKT_A   Vin_pos Vin_neg  X   Y
R1  VDD  X   5k
R2  VDD  Y   5k
M1_n  X  Vin_pos    V      GND    n_18_mm w=45u l=0.3u
```

```
M2_n  Y  Vin_neg    V       GND    n_18_mm w=45u l=0.3u
M5_n  V  Vbs        GND     GND    n_18_mm w=75u l=1u
.ends

.subckt CKT_B   Vin_pos Vin_neg  X   Y
M3_p  X  X          VDD     VDD    p_18_mm w=10u l=0.3u
M4_p  Y  Y          VDD     VDD    p_18_mm w=10u l=0.3u
M1_n  X  Vin_pos    V       GND    n_18_mm w=45u l=0.3u
M2_n  Y  Vin_neg    V       GND    n_18_mm w=45u l=0.3u
M5_n  V  Vbs        GND     GND    n_18_mm w=75u l=1u
.ends

.subckt CKT_C   Vin_pos Vin_neg  X   Y
M3_p  X  Vb         VDD     VDD    p_18_mm w=10u l=0.3u
M4_p  Y  Vb         VDD     VDD    p_18_mm w=10u l=0.3u
M1_n  X  Vin_pos    V       GND    n_18_mm w=45u l=0.3u
M2_n  Y  Vin_neg    V       GND    n_18_mm w=45u l=0.3u
M5_n  V  Vbs        GND     GND    n_18_mm w=75u l=1u
.ends

.end
```

Problem 3:

	DC Gain (V/V)	Rout (Ω)	Output Swing(V)
(b)	-4.0028	2.0583k	1.33184
(c)	-30.7332	15.7615k	3.71792

(b) is a differential amplifier biased using diode-connected transistors M3 & M4, while (c) is biased using PMOS current sources. The diode-connected transistors provide a **fixed voltage drop** and are easier to implement, but they don't provide optimal performance in terms of output swing or gain. he diode connection reduces the voltage swing at the output because part of the supply voltage is consumed by the voltage drop across M3 and M4. The current-source biasing provides **higher output swing** and **better gain** compared to diode-connected biasing. It also allows more flexibility in controlling the current flowing through the differential pair by adjusting Vb.

	Diode-Connected	Current Source
Pros	Simple to Implement	Higher Gain, Larger Output Swing
Cons	Sacrifices Gain, Output Swing & Input CM Range	More Complex to Implement