AIC Final Project

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I chose to design a two-stage op amp. The slew rate spec allows us to pick a bias current for the 1st stage. Using the equation:

$$\frac{I_{ss}}{C_c} = Slew\ Rate$$

Since the slew rate must be larger than 4V/us. I picked a slew rate of 5V/us. Additionally, I placed a 8pF compensation capacitor alongside the 2pF at the output port. Substituting this into the equation and solving it gives:

$$I_{ss} = 50uA$$

According to our textbook, *Design of Analog CMOS Integrated Circuit*, the 1st stage of the two-stage amplifier should provide high gain and the second stage should provide high output swing. Therefore, the output MOS M8 & M5 should have larger widths. I chose to give M8 11 times the width of M6. This ensures that the amplifier provides a high swing. M1 & M2 must also have large W to provide a large enough gain.

As for the phase margin, the 4.5k compensation resistor is placed to introduce a pole at around 4.42MHz that will drop the gain to unity even faster.

$$\frac{1}{4.5k \times 8p \times 2\pi} = 4.42MHz$$

Sweeping Vin,cm from 0V to 1.8V, reveals that Vin,cm,min = 0V, Vin,cm,max = 1.12V. However, further testing at Vin,cm = 1.12V reveals that the common-mode gain and gain from VDD will cause CMRR & PSRR to fall below the spec.

After more simulation, 1V turns out to be the maximum input DC voltage. The following are measurement results and simulation waveforms at Vin,cm min, mid, and max.

Supply Voltage (VDD) (V)	1.8		
Vin,cm (V)	0 (min)	0.2	1.0 (max)
DC Gain (dB)	66.186	68.030	68.759
Unity-gain Frequency (Hz)	158.453M	159.261M	149.552M
Slew Rate (V/us)	7.45	6.27	5.7
Input Common Mode Range(V)	1 - 0 = 1		
Output Max Range (V)	1.15	1.15	1.15
CMRR (dB)	79.471	80.385	67.420
PSRR(VDD) (dB)	89.741	93.763	70.640
Phase Margin (°)	65.9604	65.5138	69.8056

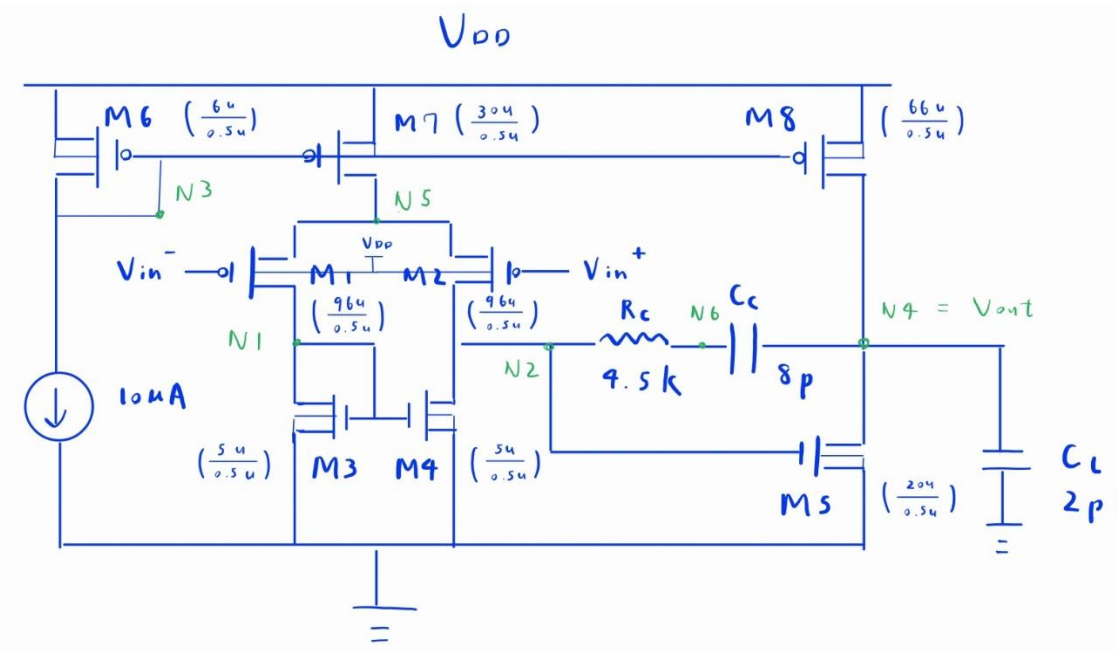

Fig 1. Circuit Schematic

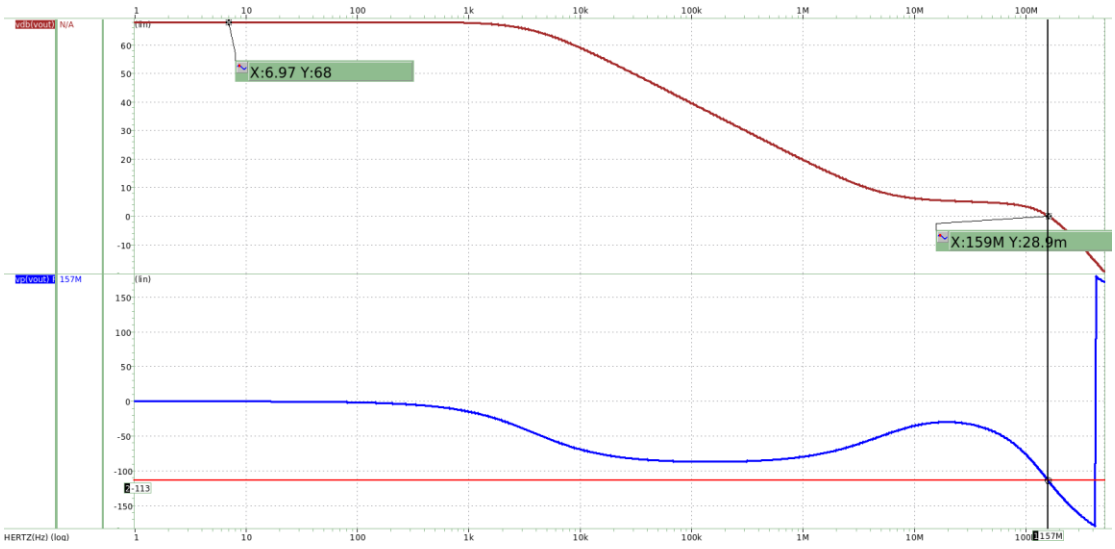

Fig 2. Bode Plot (Vin,cm = 0.2V) (measures DC gain, PM, Unity-gain Freq.)

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgaindb=  68.0295     at=   1.0000
           from=   1.0000     to= 501.1872x
dcgainv/v=   2.5204k    at=   1.0000
           from=   1.0000     to= 501.1872x
f3db=   3.7765k
funity= 159.2608x
wgc_phase=-114.4862
pm=  65.5138
******
```

Fig 3. .ac result (Vin,cm = 0.2V) (measures DC gain, PM, Unity-gain Freq.)

```
****     small-signal transfer characteristics

    v(vout)/vsupply                          =   51.6769m
    input resistance at            vsupply   =   82.0811k
    output resistance at v(vout)             =   32.3566k
```

Fig 4. Gain from VDD (Vin,cm = 0.2V)

```
****     small-signal transfer characteristics

    v(vout)/v_common                          =  241.1015m
    input resistance at              v_common =  1.000e+20
    output resistance at v(vout)               =   32.3566k
```

Fig 5. Common-mode Gain (Vin,cm = 0.2V)

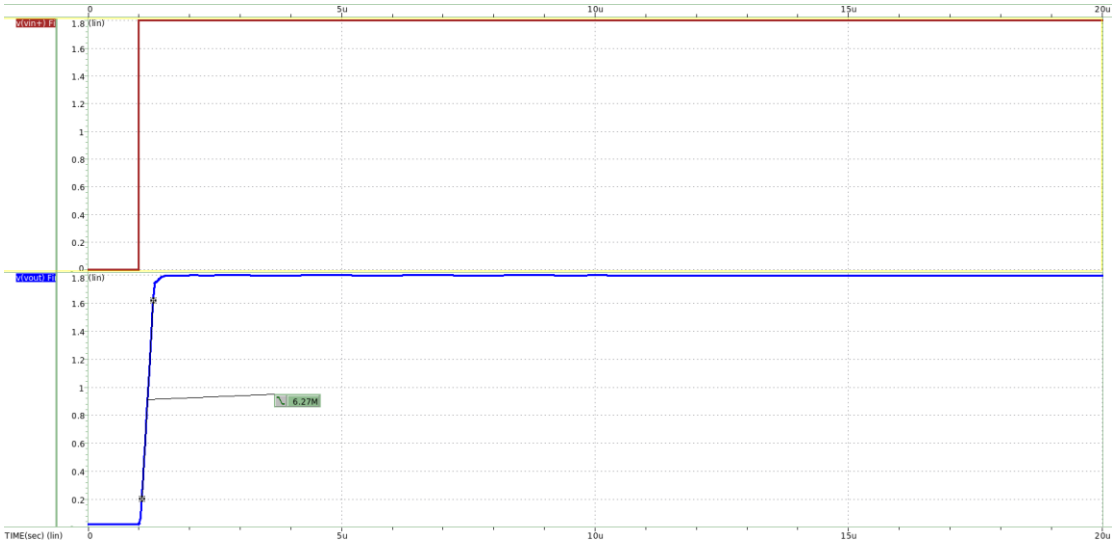

Fig 6. Slew Rate (Vin,cm = 0.2V)

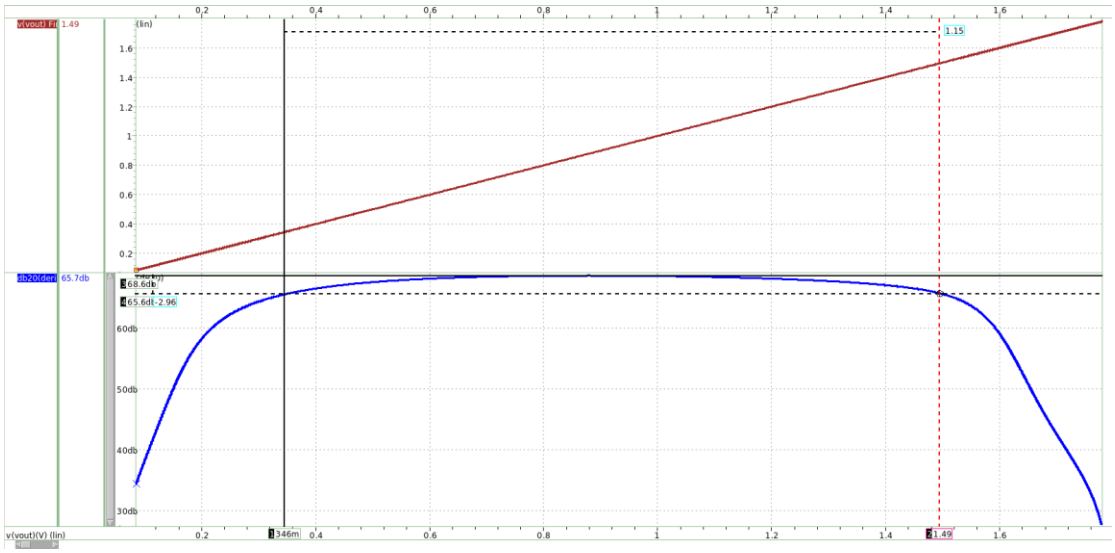

Fig 7. Output Range (Vin,cm = 0.2V)

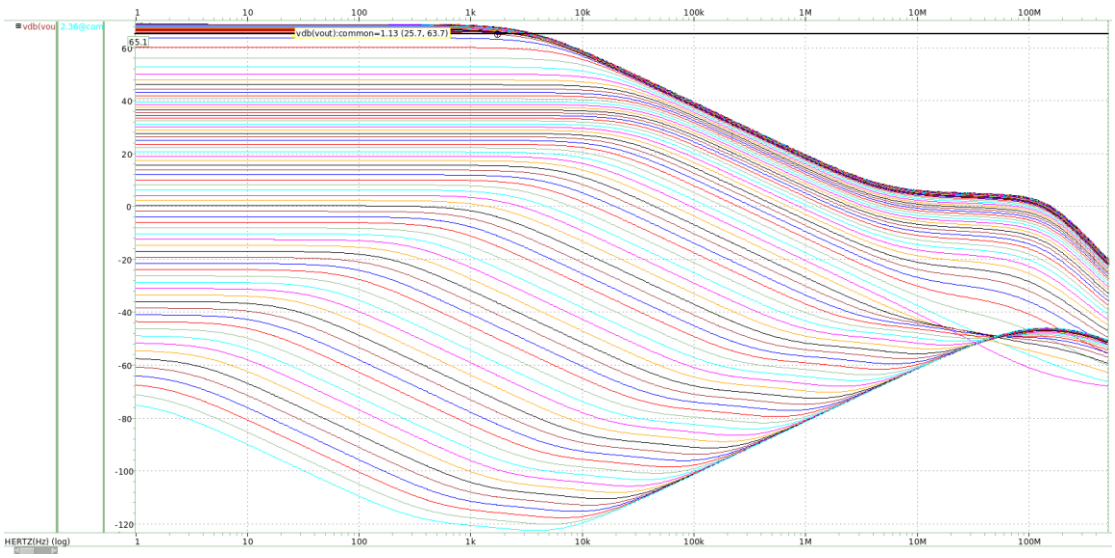

Fig 8. Gain at Different Vin,cm

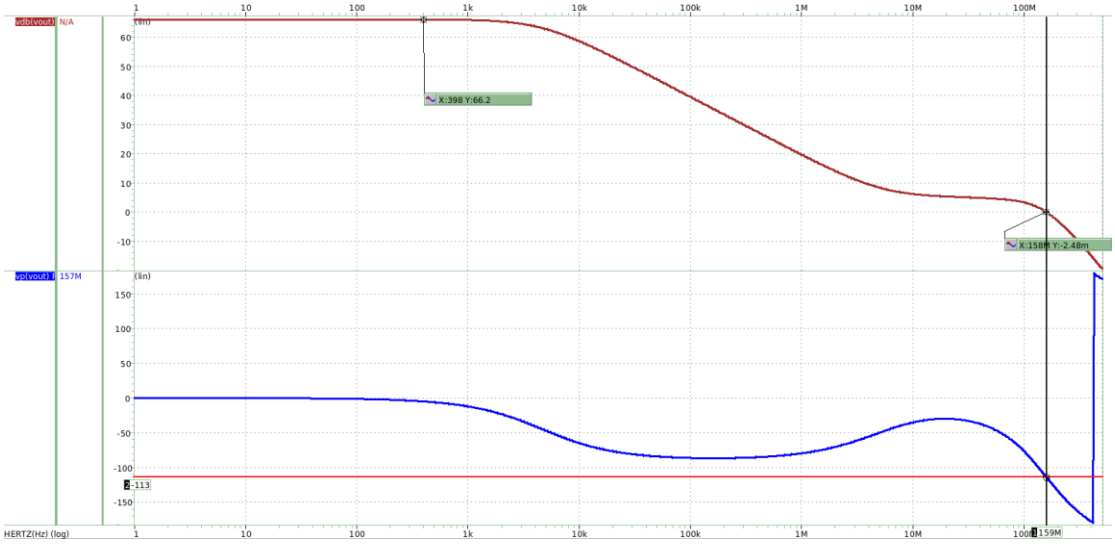

Fig 9. Bode Plot (Min Vin,cm = 0V) (measures DC gain, PM, Unity-gain Freq.)

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgaindb=  66.1859     at=   1.0000
           from=   1.0000     to= 501.1872x
dcgainv/v=   2.0384k    at=   1.0000
           from=   1.0000     to= 501.1872x
f3db=   4.6520k
funity= 158.4531x
wgc_phase=-114.0396
pm=  65.9604
******
```

Fig 10. .ac result (Min Vin,cm = 0V) (measures DC gain, PM, Unity-gain Freq.)

```
****     small-signal transfer characteristics

    v(vout)/vsupply                          =   66.4105m
    input resistance at            vsupply   =   86.8931k
    output resistance at v(vout)             =   32.2265k
```

Fig 11. Gain from VDD (Min Vin,cm = 0V)

```
****     small-signal transfer characteristics

    v(vout)/v_common                         =  216.6296m
    input resistance at            v_common  =  1.000e+20
    output resistance at v(vout)             =   32.2265k
```

Fig 12. Common-mode Gain (Min Vin,cm = 0V)

Fig 13. Slew Rate (Min Vin,cm = 0V)

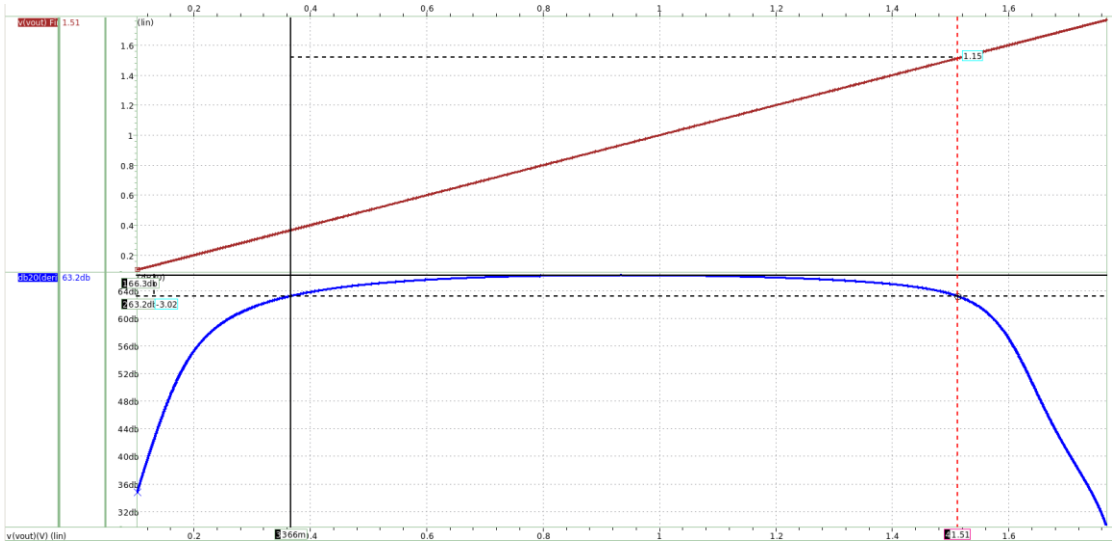

Fig 14. Output Range (Max Vin,cm = 1V)

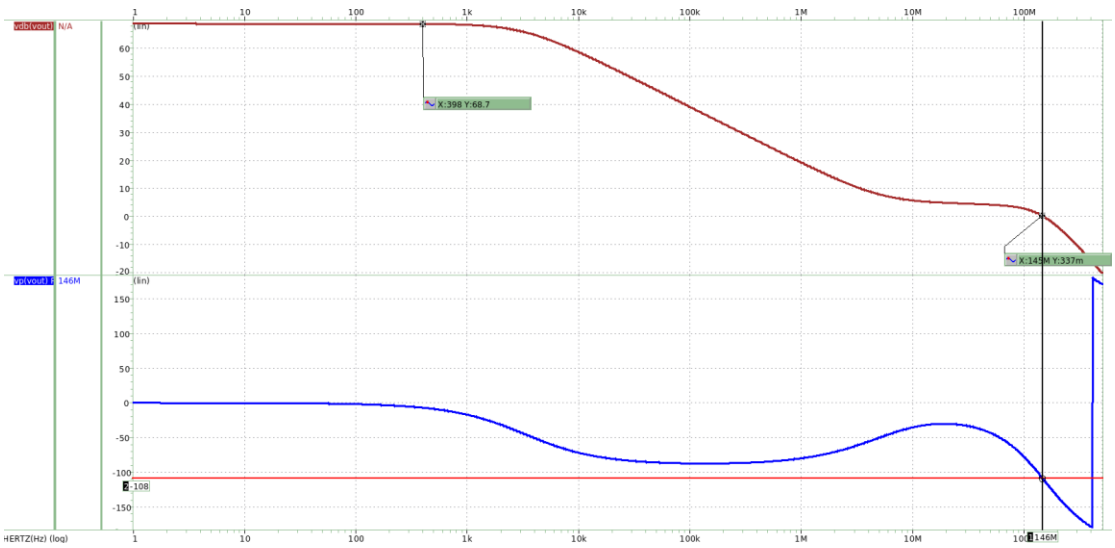

Fig 15. Bode Plot (Min Vin,cm = 0V) (measures DC gain, PM, Unity-gain Freq.)

```
***-----------------------***

****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgaindb=  68.7592     at=   1.0000
           from=   1.0000     to= 501.1872x
dcgainv/v=   2.7413k    at=   1.0000
           from=   1.0000     to= 501.1872x
f3db=   3.2753k
funity= 149.5517x
wgc_phase=-110.1944
pm=  69.8056
******
```

Fig 15. .ac result (Max Vin,cm = 1V) (measures DC gain, PM, Unity-gain Freq.)

```
****     small-signal transfer characteristics

    v(vout)/vsupply                          = -805.3288m
    input resistance at            vsupply   =   26.2472k
    output resistance at v(vout)             =   31.3777k
```

Fig 16. Gain from VDD (Max Vin,cm = 1V)

```
****     small-signal transfer characteristics

    v(vout)/v_common                          =    1.1667
    input resistance at              v_common =  1.000e+20
    output resistance at v(vout)              =   31.3777k
```

Fig 17. Common-mode Gain (Max Vin,cm = 1V)

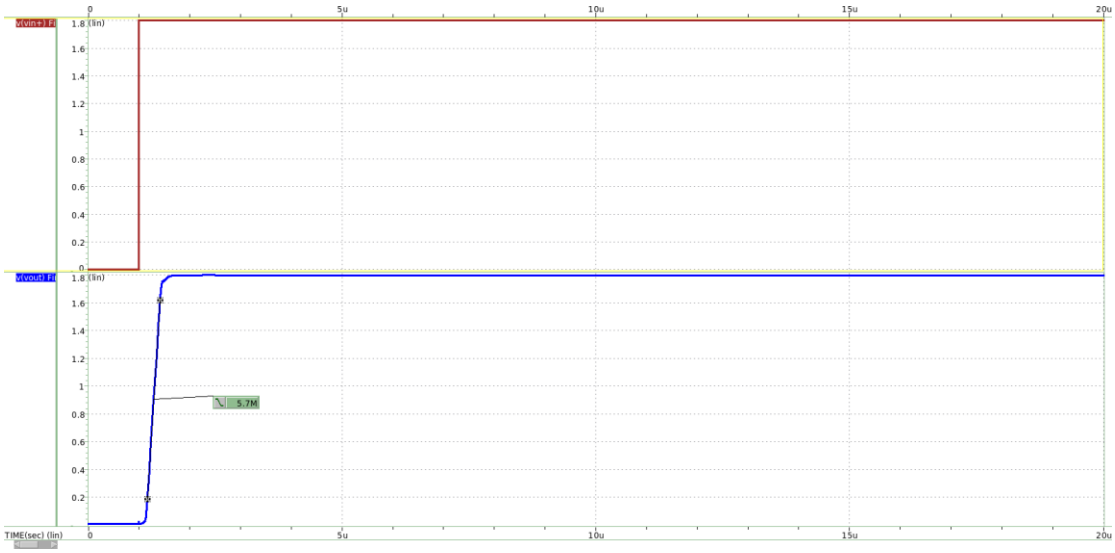

Fig 18. Slew Rate (Max Vin,cm = 1V)

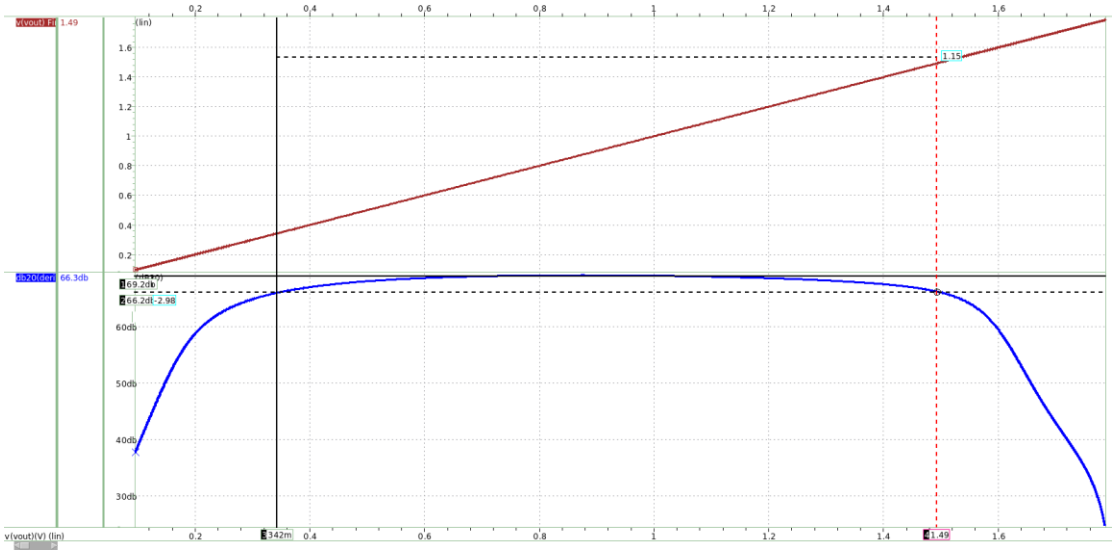

Fig 19. Output Range (Max Vin,cm = 1V)

Code:

```
***-----------------------***
***        setting        ***
***-----------------------***
.lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" tt
.TEMP 25
.op 10u
***-----------------------***
***       simulation      ***
***-----------------------***

.option post
.option accurate=1
.ac    DEC  100 1 500Meg
.probe AC P(Vout)
.probe AC Vdb(Vout)
.probe AC VP(Vout)
.tran 0.1n 20u
.probe tran V(Vout)
.tf   V(Vout)   Vin1

***-----------------------***
***       measure         ***
***-----------------------***
.meas AC DCgainDB max Vdb(Vout)
.meas AC DCgainV/V max V(Vout)
.meas AC f3db when Vdb(Vout)='DCgainDB-3.0'
.meas AC funity when Vdb(Vout)='0'
.meas AC wgc_phase find VP(Vout) when Vdb(Vout)='0'
.meas AC PM param = 'wgc_phase + 180'
.meas tran avg_power avg power

.meas tran vout_max param = '1.25'
.meas tran delta_t trig V(Vout) val='1.25*0.1' rise = 1
+targ V(Vout) val='1.25*0.9' rise = 1
.meas tran slew_rate param = "(1.25*0.9 - 1.25*0.1) / delta_t"

```

```
***-----------------------***
***      power/input      ***
***-----------------------***
Vsupply     VDD     GND       1.8V

Vin1        Vin+    GND       DC      1V      AC  0.5V   0
Vin2        Vin-    GND       DC      1V      AC  0.5V   180

Iss         N3      GND      10u
***-----------------------***
***        circuit        ***
***-----------------------***
M1        N1    Vin-    N5     VDD    p_18_mm   w=96u       l=0.5u
M2        N2    Vin+    N5     VDD    p_18_mm   w=96u       l=0.5u

M3        N1    N1      GND    GND    n_18_mm   w=5u        l=0.5u
M4        N2    N1      GND    GND    n_18_mm   w=5u        l=0.5u

M5        Vout  N2      GND    GND    n_18_mm   w=20u       l=0.5u

M6        N3    N3      VDD    VDD    p_18_mm   w=6u        l=0.5u

M7        N5    N3      VDD    VDD    p_18_mm   w=30u       l=0.5u

M8        Vout  N3      VDD    VDD    p_18_mm   w=66u       l=0.5u

CL        Vout  GND     2p
Rc        N2    N6      1
Cc        N6    Vout    8p

*Original circuit measures DC gain, 3-dB bandwidth, power, unity gain freq., Phase
Margin
.alter
*output_swing
VDM vid  GND offset
VCM VCMI GND 0.2V
EIN+ Vin+ VCMI vid GND 0.5
EIN- Vin- VCMI vid GND -0.5
```

```
74.
75. .alter
76. .alter
77. *measures gain from VDD
78. .tf   V(Vout)   Vsupply
79. Vsupply     VDD   GND    DC      1.8V   AC 1
80.
81. .alter
82. *measures Acm
83. .tf   V(Vout)   V_common
84. Vin1        Vin+    Common       DC      0V
85. Vin2        Vin-    Common       DC      0V
86. V_common    Common  GND          DC      0.2V     AC  0.5
87.
88. .alter
89. *measures Slew Rate, Settling Time
90. .tran 0.1n 20u
91. *                          PULSE(V1    V2  Tdelay  Trise   Tfall   Pwidth  Period)
92. Vin1       Vin+     GND     PULSE(0V  1.8V  1us     0ns     0ns     30us    50us)
93. Vin2       Vin-     GND     DC      0.2V
94.
95. .end
96.
97.
```