HSPICE Homework #2 of「類比積體電路導論」

作業繳交截止日期: **Oct. 03, 2024,18:00**

(上傳E3 數位平台繳交)

Fig. 1 is an NMOS common-source amplifier circuits with the W/L ratios of (a) 2um/0.3um and (b) 6um/0.9um. Perform the HSPICE simulations using device parameters of 0.18um CMOS technology. Please use n_18_mm and p_18_mm. From the simulation results,

(1) Find the gain Av=Vout/Vin, output DC voltage, Drain DC current, Vin and Vout capacitance, and the output resistance looking into the Vout node. You should use Hspice to simulate five corners and fill up the **table1**.

Problem (2)~(3) under TT Corner.

(2) Calculate with the simulation parameters and compare both output resistances and gains of the circuits with different W/L between (a) and (b). Explain the reason of differences.

Table2: Calculation Results

Temp.(˚C)	Circuit	Rout (Ω)	Av (V/V)
25	(a)		
25	(b)		
75	(a)		
75	(b)		

(3) Plot the I_D-V_{GS} curve and observe the variation of V_{th} and I_D by sweeping the temperatures from 0° to 80°(step=10°). Explain the reason of differences. Consider the drain current I_D under the saturation region and subthreshold region.

Table1: Simulation Results of NMOS common-source amplifier

Corner	Temp (°C)	Circuit	Vout (V)	Ids (mA)	*DC Gain Av (V/V)	Rout (Ω)	Cin (F)	Cout (F)
TT	25	(b)						
TT	0	(a)						
TT	25	(a)						
TT	75	(a)						
FF	25	(a)						
SS	25	(a)						
FnSp	25	(a)						
SnFp	25	(a)						

*The DC gain is the low-frequency gain.

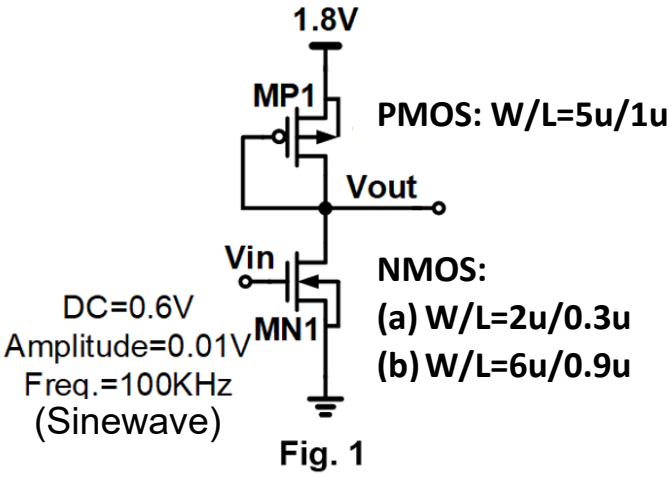

Fig. 1

HSPICE_HW2：作業需要有以下幾點：

1. HSPICE Code (截圖)
2. Simulation Result (波形繳交背景請用白色，並且波形標示和呈現要清楚)
3. 每個小題的單獨說明

   問題(1) 填表格

   問題(2) 計算、表格、說明

   問題(3) 說明、波型圖
4. 以.pdf 的格式上傳
5. 檔案名稱用「Hspice_HW2_自己的學號」(例如：Hspice_HW2_0811541)，於作業繳交截止日期(發布後隔週禮拜四晚上 6 點)前，上傳到指定的 E3 數位平台繳交，遲交一周內打八折，一周後不計分。