Homework #7 of「類比積體電路導論」

作業繳交截止日期:Dec. 5, 2024 12:00 (上傳E3數位平台繳交)

本次作業共兩大題，7.1~7.2

請將作業轉成一個PDF檔案(file size小於10MB)，檔名請使用

「AIC_HW7_自己的學號」(例如: AIC_HW7_109700018)，於作業繳

交截止日期/時間前，上傳到指定的E3數位平台繳交。

Unless otherwise stated, in the following problems, use the device data shown in Table 1 and assume that VDD=3V. The Dielectric constant of gate oxide is 3.9 and εo=$8.854\times10^{-12}F/m$.

Table 1. Level 1 SPICE models for NMOS and PMOS devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body-effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate-oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

7.1 In this problem, we design a two-stage op amp based on topology shown in Fig 7.1. Assume a power budget of 6mW, a required output swing of 2.4V, and L_{eff} = 0.5µm for all devices. Assume λ=γ=0 for bias purpose and γ=0, λ≠0 for small signal analysis.

(a) Allocating a current of 1 mA to the output stage and roughly equal overdrive voltages to M_5 and M_6, determine $(W/L)_5$ and $(W/L)_6$.
Note that the gate-source capacitance of M_5 is in the signal path, whereas that of M_6 is not. Thus, M_6 can be quite a lot larger than M_5.

(b) Calculate the small-signal gain of the output stage. (calculate the 2nd stage gain only).

(c) With the remaining 1 mA flowing through M_7, determine the aspect ratio of M_3 (and M_4) such that $VGS_3 = VGS_5$.
This is to guarantee that if Vin = 0 and hence $V_X = V_Y$, then M_5 carries the expected current.

(d) Calculate the aspect ratios of M_1 and M_2 such that the overall voltage gain of the op amp is equal to 400.

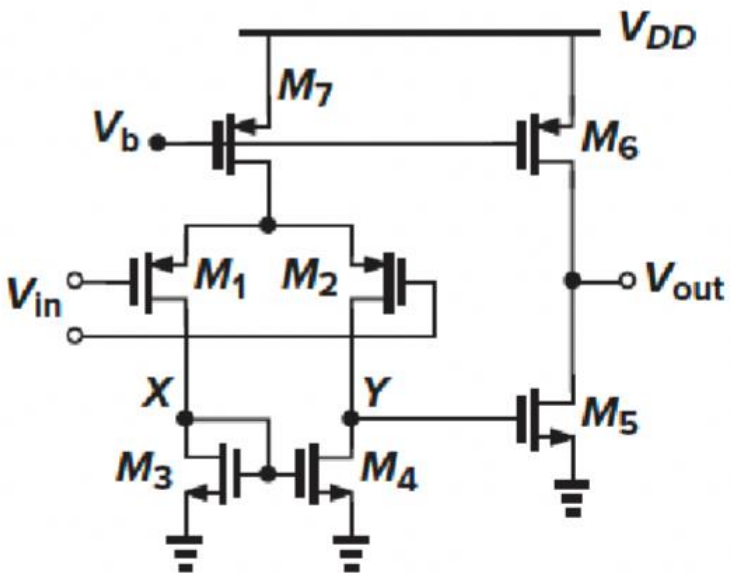

Fig.7.1

7.2 In the op amp of Fig. 7.2, $(W/L)_{1\text{-}8}$ = 120 µm/0.5 µm, I_{SS} = 1 mA, and V_{b1} = 1.7 V. Assume that $\lambda = \gamma = 0$.

(a) What is the maximum allowable input CM level?

(b) What is V_X?

(c) What is the maximum allowable output swing if the gate of M_2 is connected to the output?

(d) What is the acceptable range of V_{b2}?

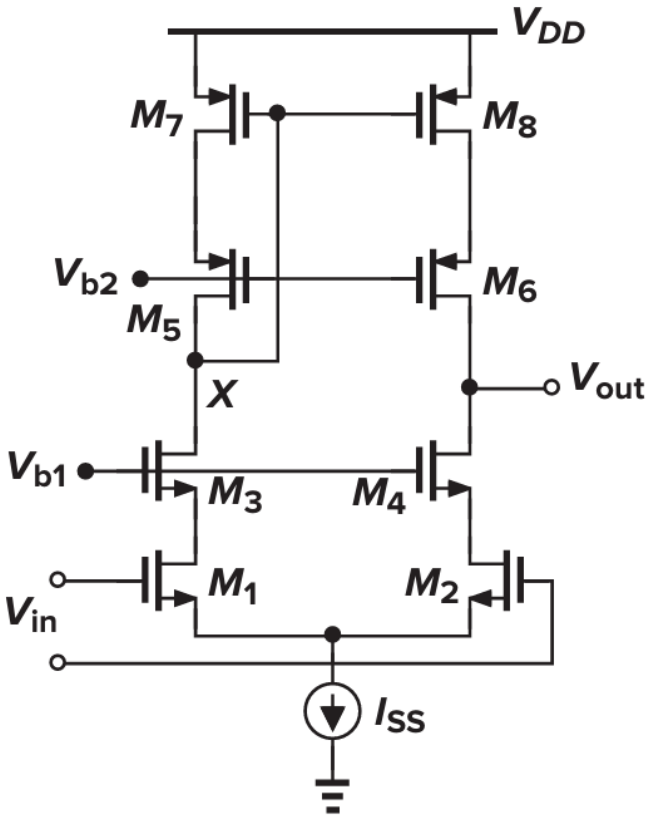

Fig.7.2