AIC HW5

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Problem 1:

NO.	Performance Parameters	TT	FF	SS	FnSp	SnFp
1	DC Gain(dB)	71.9366	68.9745	72.8455	70.8103	72.7023
2	3-dB Bandwidth(Hz)	4.2395k	6.0042k	3.7281k	4.8376k	3.8657k
3	Slew Rate(V/us)	17.8	17.9	16.9	17.4	18
4	Settling Time(us)	0.68	0.78	0.62	0.69	0.53
5	CMRR(dB)	210.7917	202.7448	214.8733	206.5053	206.3872
6	PSRR(VDD)(dB)	209.5586	226.8923	209.6000	222.4707	204.4728
7	PSRR(GND)(dB)	221.7783	225.2085	216.3918	219.7673	235.7218
8	Unity-gain Frequency(Hz)	16.2195M	16.3384M	15.8460M	16.2718M	16.1411M
9	Phase Margin (°)	74.2417	73.9909	74.5330	74.3321	74.1580
10	Power(uW)	467.9814	468.3307	467.4536	467.7367	468.1831

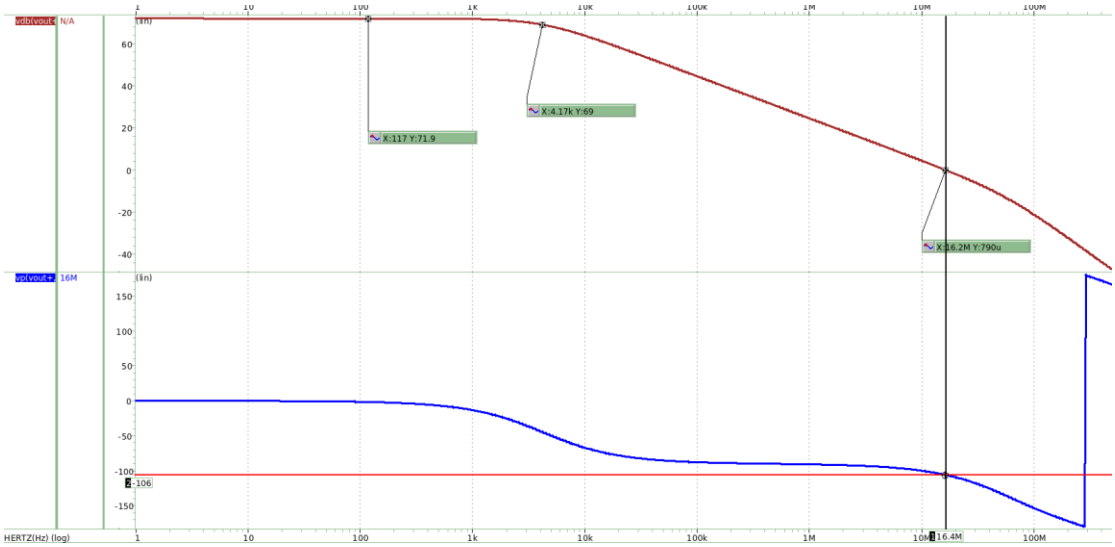

Fig 1. TT Bode Plot (DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

Fig 2. TT Slew Rate & Settling Time

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgaindb=  71.9366     at=   1.0000
           from=   1.0000     to= 501.1872x
dcgainv/v=   3.9521k    at=   1.0000
           from=   1.0000     to= 501.1872x
f3db=   4.2395k
funity=  16.2195x
wgc_phase=-105.7583
pm=  74.2417
******
```

Fig 3. TT .measure(DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/v_common                  = -114.0888n
    input resistance at              v_common =  1.000e+20
    output resistance at v(vout+,vout-)      =   14.4535x
```

Fig 4. TT .measure(Common-mode Gain)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/vsupply                    =  131.4910n
    input resistance at              vsupply  =  320.2773k
    output resistance at v(vout+,vout-)       =   14.4535x
```

Fig 5. TT .measure(Gain from VDD)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/vss                        =   32.2041n
    input resistance at               vss     = -2.545e+13
    output resistance at v(vout+,vout-)       =   14.4535x
```

Fig 6. TT .measure(Gain from GND)

```
**** voltage sources

subckt
element  0:v1       0:v2       0:v3       0:v_common 0:vss      0:vsupply
 volts    800.0000m  800.0000m  900.0000m    0.         0.         1.8000
 current    0.         0.         0.         0.        58.7860f -259.9897u
 power      0.         0.         0.         0.         0.       467.9814u

   total voltage source power dissipation=  467.9814u       watts
```

Fig 7. TT Power

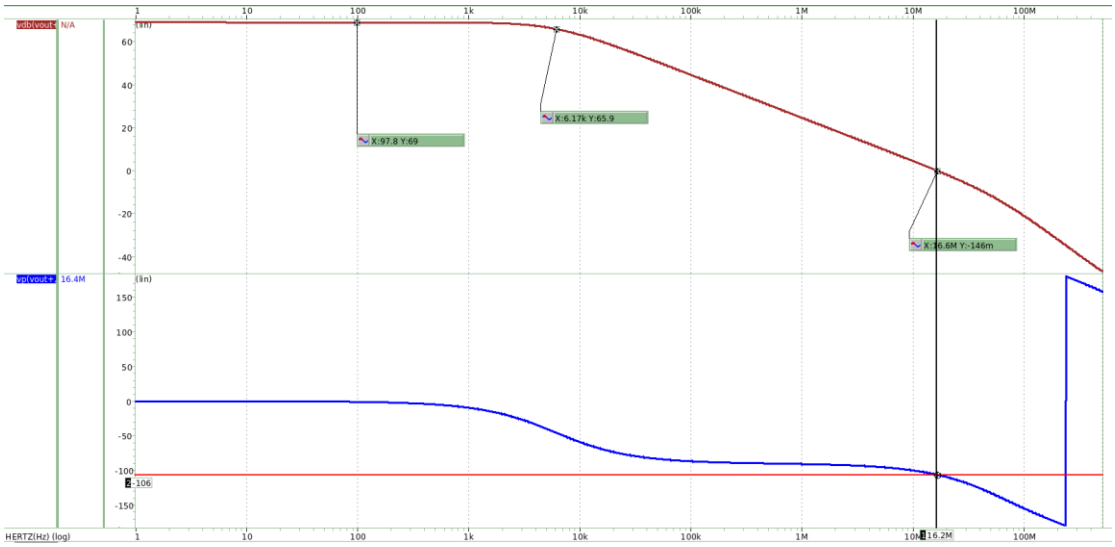

Fig 8. FF Bode Plot (DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

Fig 9. FF Slew Rate & Settling Time

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgaindb=  68.9745     at=   1.0000
           from=   1.0000     to= 501.1872x
dcgainv/v=   2.8101k    at=   1.0000
           from=   1.0000     to= 501.1872x
f3db=   6.0042k
funity=  16.3384x
wgc_phase=-106.0091
pm=  73.9909
******
```

Fig 10. FF .measure(DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/v_common                 =  204.8710n
    input resistance at             v_common =  1.000e+20
    output resistance at v(vout+,vout-)      =   10.2242x
```

Fig 11. FF .measure(Common-mode Gain)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/vsupply                  =   12.7088n
    input resistance at             vsupply  =  673.1213k
    output resistance at v(vout+,vout-)      =   10.2242x
```

Fig 12. FF .measure(Gain from VDD)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/vss                      =   15.4276n
    input resistance at             vss      = -1.272e+13
    output resistance at v(vout+,vout-)      =   10.2242x
```

Fig 13. FF .measure(Gain from GND)

```
**** voltage sources

subckt
element  0:v1       0:v2       0:v3       0:v_common 0:vss      0:vsupply
 volts    800.0000m  800.0000m  900.0000m    0.         0.         1.8000
 current    0.         0.         0.         0.        29.7816f -260.1837u
 power      0.         0.         0.         0.         0.       468.3307u

    total voltage source power dissipation=  468.3307u       watts
```

Fig 14. FF Power

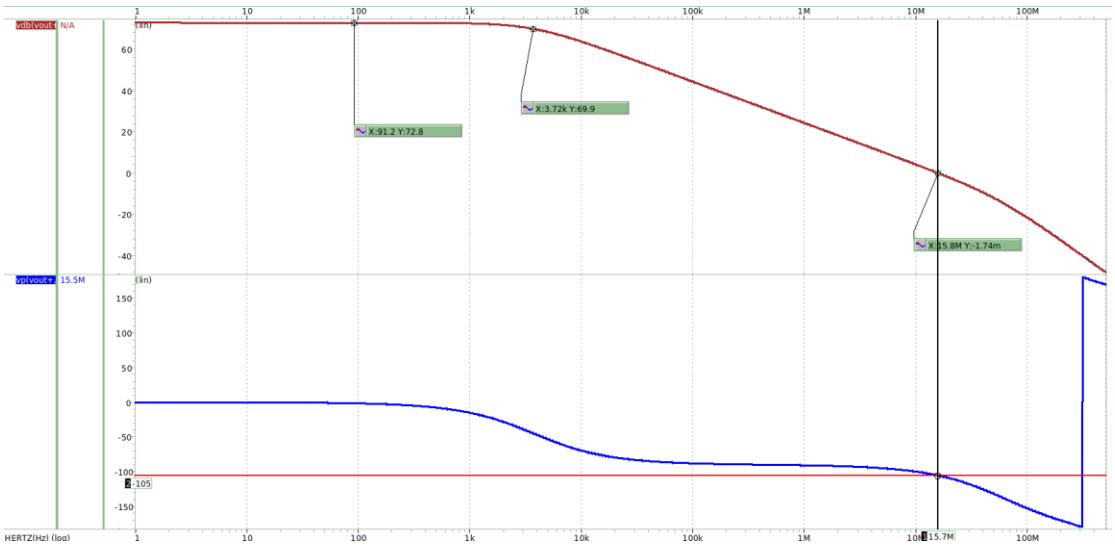

Fig 15. SS Bode Plot (DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

Fig 16. SS Slew Rate & Settling Time

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgaindb=  72.8455     at=   1.0000
           from=   1.0000     to= 501.1872x
dcgainv/v=   4.3881k    at=   1.0000
           from=   1.0000     to= 501.1872x
f3db=   3.7281k
funity=  15.8460x
wgc_phase=-105.4670
pm=  74.5330
******
```

Fig 17. SS .measure(DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/v_common                 =  -79.1793n
    input resistance at             v_common =  1.000e+20
    output resistance at v(vout+,vout-)      =   16.4022x
```

Fig 18. SS .measure(Common-mode Gain)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/vsupply                  =  145.3043n
    input resistance at             vsupply  =  146.3439k
    output resistance at v(vout+,vout-)      =   16.4022x
```

Fig 19. SS .measure(Gain from VDD)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/vss                      =  -66.4796n
    input resistance at             vss      = -1.043e+13
    output resistance at v(vout+,vout-)      =   16.4022x
```

Fig 20. SS .measure(Gain from GND)

```
**** voltage sources

subckt
element  0:v1        0:v2        0:v3        0:v_common 0:vss       0:vsupply
 volts     800.0000m   800.0000m   900.0000m     0.          0.          1.8000
 current     0.          0.          0.          0.        93.9871f -259.6965u
 power       0.          0.          0.          0.          0.        467.4536u

    total voltage source power dissipation=   467.4536u       watts
```

Fig 21. SS Power

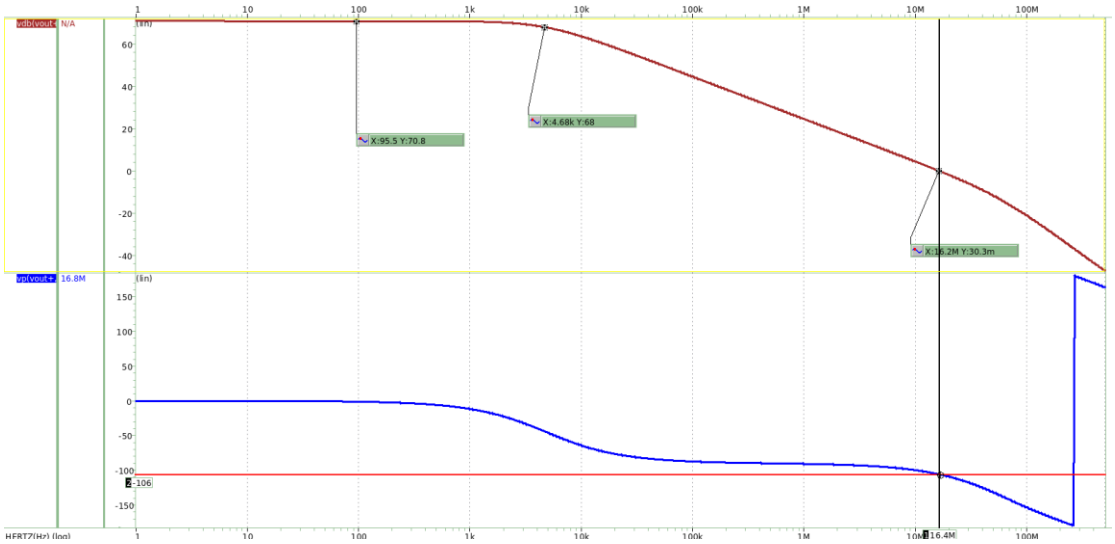

Fig 22. FnSp Bode Plot (DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

Fig 23. FnSp Slew Rate & Settling Time

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgaindb=  70.8103     at=   1.0000
           from=   1.0000     to= 501.1872x
dcgainv/v=   3.4715k    at=   1.0000
           from=   1.0000     to= 501.1872x
f3db=   4.8376k
funity=  16.2718x
wgc_phase=-105.6679
pm=  74.3321
******
```

Fig 24. FnSp .measure(DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/v_common                 = -164.1548n
    input resistance at             v_common =  1.000e+20
    output resistance at v(vout+,vout-)      =   12.6682x
```

Fig 25. FnSp TT .measure(Common-mode Gain)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/vsupply                  =  -26.1205n
    input resistance at             vsupply  =  216.5334k
    output resistance at v(vout+,vout-)      =   12.6682x
```

Fig 26. FnSp TT .measure(Gain from VDD)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/vss                      =  -35.6574n
    input resistance at             vss      = -5.647e+13
    output resistance at v(vout+,vout-)      =   12.6682x
```

Fig 27. FnSp TT .measure(Gain from GND)

```
**** voltage sources

subckt
element  0:v1        0:v2        0:v3        0:v_common 0:vss       0:vsupply
 volts     800.0000m   800.0000m   900.0000m     0.         0.          1.8000
 current     0.          0.          0.          0.        -5.6399f -259.8537u
 power       0.          0.          0.          0.         0.        467.7367u

    total voltage source power dissipation=  467.7367u       watts
```

Fig 28. FnSp Power

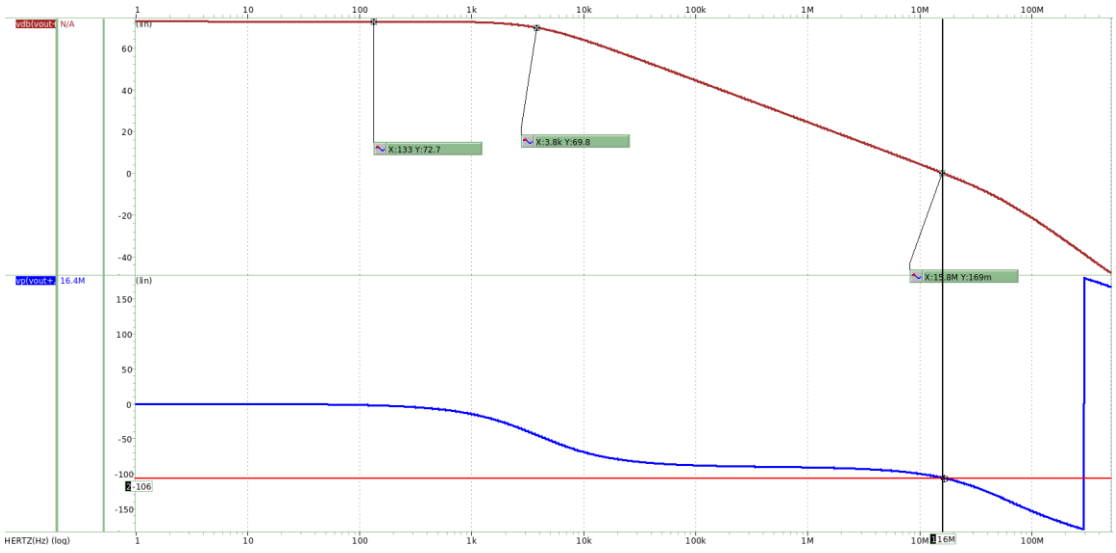

Fig 29. SnFp Bode Plot (DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

Fig 30. SnFp Slew Rate & Settling Time

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgaindb=  72.7023     at=   1.0000
           from=   1.0000     to= 501.1872x
dcgainv/v=   4.3163k    at=   1.0000
           from=   1.0000     to= 501.1872x
f3db=   3.8657k
funity=  16.1411x
wgc_phase=-105.8420
pm=  74.1580
******
```

Fig 31. SnFp .measure(DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/v_common                 = -206.8962n
    input resistance at             v_common =  1.000e+20
    output resistance at v(vout+,vout-)      =   15.8476x
```

Fig 32. SnFp .measure(Common-mode Gain)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/vsupply                  = -257.9120n
    input resistance at             vsupply  =  485.3339k
    output resistance at v(vout+,vout-)      =   15.8476x
```

Fig 33. SnFp .measure(Gain from VDD)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/vss                      =    7.0635n
    input resistance at             vss      = -1.100e+14
    output resistance at v(vout+,vout-)      =   15.8476x
```

Fig 34. SnFp .measure(Gain from GND)

```
**** voltage sources

subckt
element  0:v1       0:v2       0:v3       0:v_common 0:vss      0:vsupply
 volts    800.0000m  800.0000m  900.0000m    0.         0.         1.8000
 current    0.         0.         0.         0.        93.9871f -259.6965u
 power      0.         0.         0.         0.         0.       467.4536u

    total voltage source power dissipation=  467.4536u       watts
```

Fig 35. SnFp Power

Problem 2:

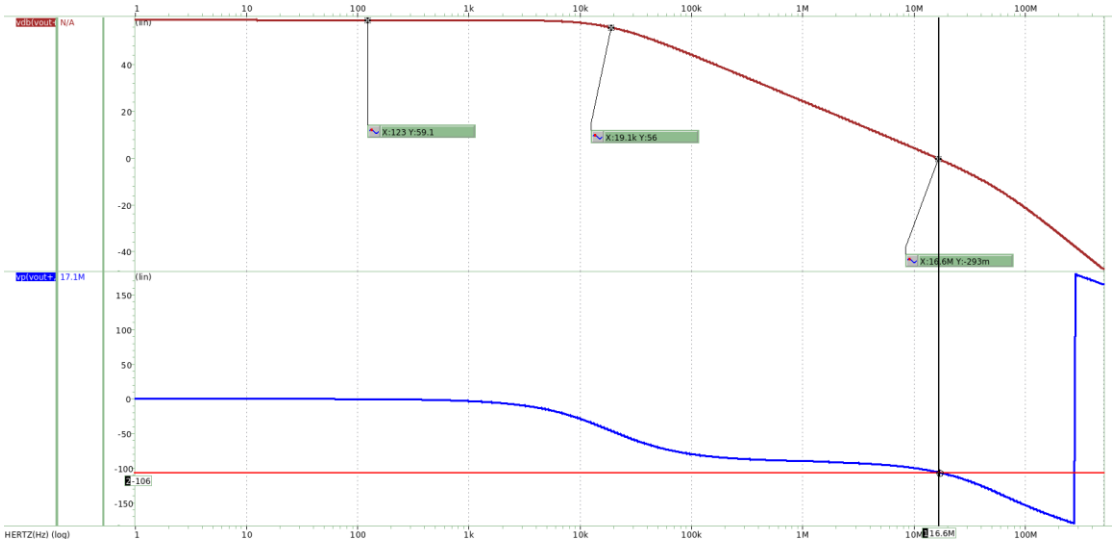

Fig 36. M2 W/L = 60.1u/4u TT Bode Plot (DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

Fig 37. M2 W/L = 60.1u/4u TT Slew Rate & Settling Time

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgaindb=  59.1438     at=   1.0000
           from=   1.0000     to= 501.1872x
dcgainv/v= 906.1296     at=   1.0000
           from=   1.0000     to= 501.1872x
f3db=  18.2747k
funity=  16.0809x
wgc_phase=-105.5453
pm=  74.4547
******
```

Fig 38. M2 W/L = 60.1u/4u TT .measure(DC Gain, Bandwidth, Unity-gain Freq., Phase Margin)

```
****     small-signal transfer characteristics

    v(vout+,vout-)/v_common                  =  404.2798m
    input resistance at              v_common =  1.000e+20
    output resistance at v(vout+,vout-)      =    3.3135x
```

Fig 39. M2 W/L = 60.1u/4u TT .measure(Common-mode Gain)

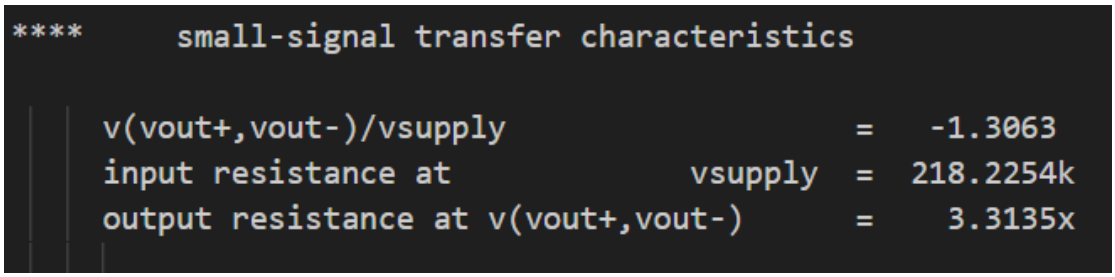

Fig 40. M2 W/L = 60.1u/4u TT .measure(Gain from VDD)

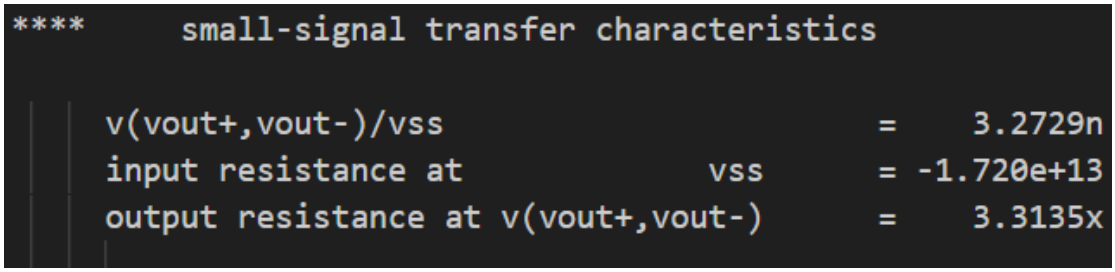

Fig 41. M2 W/L = 60.1u/4u TT .measure(Gain from GND)

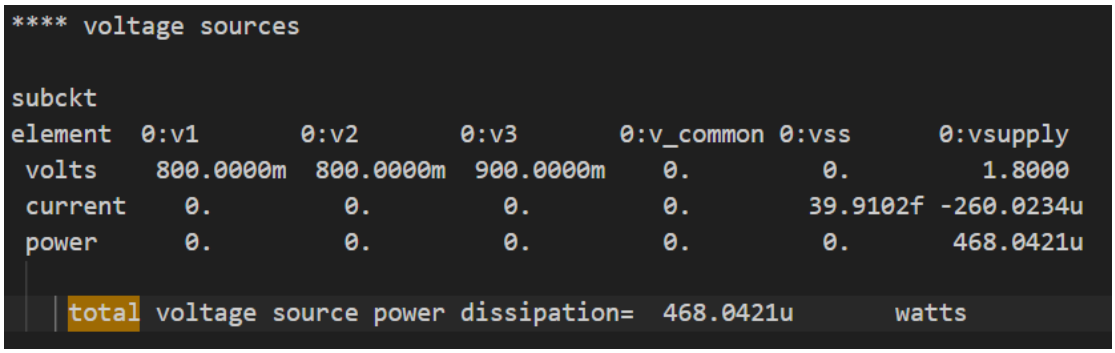

Fig 42. M2 W/L = 60.1u/4u TT .measure(Power)

NO.	Performance Parameters	TT M2 W/L = 60.1u/4u	TT M2 W/L = 60u/4u
1	DC Gain(dB)	59.1438	71.9366
2	3-dB Bandwidth(Hz)	18.2747k	4.2395k
3	Slew Rate(V/us)	17.8	17.8
4	Settling Time(us)	0.68	0.68
5	CMRR(dB)	67.0102	210.7917
6	PSRR(VDD)(dB)	56.8229	209.5586
7	PSRR(GND)(dB)	228.8452	221.7783
8	Unity-gain	16.0809M	16.2195M

	Frequency(Hz)		
9	Phase Margin (°)	74.4547	74.2417
10	Power(uW)	468.0421	467.9814

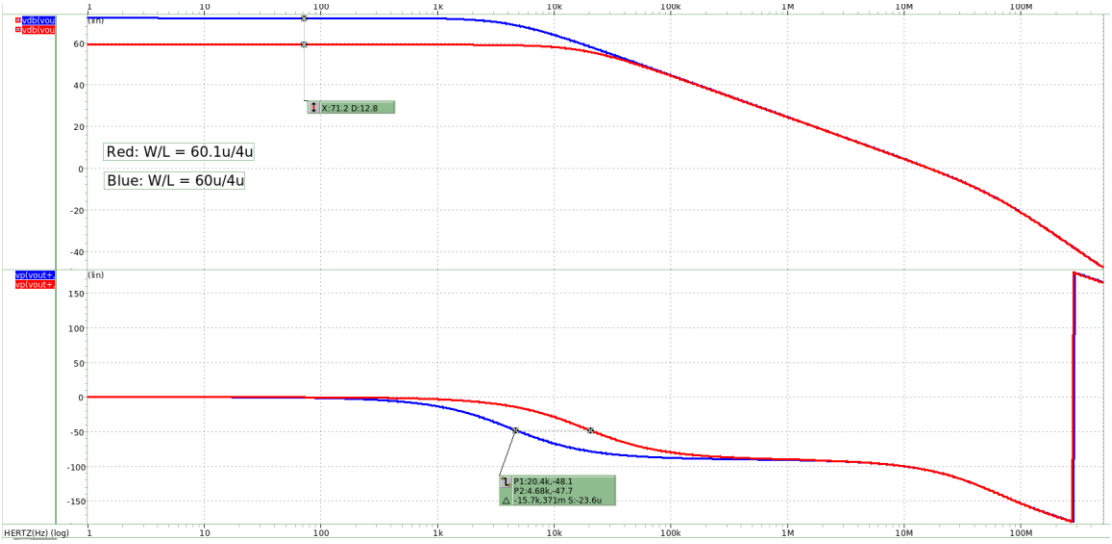

Fig 43. M2 W/L = 60.1u/4u & M2 W/L = 60u/4u TT Bode Plot Comparison

Comparison & Discussion:

Because the widths of the MOSFETs in the differential amplifier are mismatched, it causes imbalance in the differential pair, leading to several undesirable effects:

1. Mismatch in Transconductance (gm)

The transconductance gm of a MOSFET depends on its width (W). Because the width are mismatched, the gm values of the two sides are different. This results in an unequal current flow in the differential branches, even when the input voltages are balanced. This imbalance reduces the symmetry of the circuit and affects the differential amplifier's performance.

2. Reduced Common-Mode Rejection Ratio (CMRR)

The differential amplifier is designed to amplify differential signals and reject common-mode signals. As we can see from the .tf results above, the mismatched widths degrade the common-mode rejection ratio (CMRR) because

the differential pair no longer perfectly cancels common-mode signals.

3. Reduced Power Supply Rejection Ration (PSRR)

The same reasons CMRR is reduced can be applied here. Unequal gm makes the amplifier more sensitive to variations in the power supply.

4. Reduced Gain and Linearity

The differential gain of the amplifier depends on the matching of the transistors. Width mismatch has reduced the gain and affected the linearity of the amplifier. Its gain reduced by approximately 12.8dB compared to the perfectly matched amplifier.

5. Phase Response

The width of a MOSFET directly influences its parasitic capacitances. Therefore, the first pole of the mismatched amplifier is shifted to the right by approximately 15.7Hz.

6. Slew Rate & Settling Time

The slew rate and settling time seem to be unaffected by the mismatch.

Code for Problems 1 & 2:

```
***------------------------***
***        setting        ***
***------------------------***
.lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" tt
.TEMP 25
.op 0.5m
***------------------------***
***       simulation      ***
***------------------------***

.option post
.option accurate=1
.ac    DEC  100 1 500Meg
.probe AC P(Vout+,Vout-)
.probe AC Vdb(Vout+,Vout-)
```

```
.probe AC VP(Vout+,Vout-)
.tran 0.1n 20u
.probe tran V(Vout+, Vout-)
.tf   V(Vout+, Vout-)   V1

***-----------------------***
***       measure         ***
***-----------------------***
.meas AC DCgainDB max Vdb(Vout+,Vout-)
.meas AC DCgainV/V max V(Vout+,Vout-)
.meas AC f3db when Vdb(Vout+,Vout-)='DCgainDB-3.0'
.meas AC funity when Vdb(Vout+,Vout-)='0'
.meas AC wgc_phase find VP(Vout+,Vout-) when Vdb(Vout+,Vout-)='0'
.meas AC PM param = 'wgc_phase + 180'
.meas tran avg_power avg power

.meas tran vout_max param = '1.25'
.meas tran delta_t trig V(Vout+,Vout-) val='1.25*0.1' rise = 1
+targ V(Vout+,Vout-) val='1.25*0.9' rise = 1
.meas tran slew_rate param = "(1.25*0.9 - 1.25*0.1) / delta_t"

***-----------------------***
***      power/input      ***
***-----------------------***
Vsupply     VDD     vss       1.8V
V1          Vin+    Common    DC      0.8V      AC  0.5V   0
V2          Vin-    Common    DC      0.8V      AC  0.5V   180
V_common    Common    vss     DC      0V
Vgnd    GND 0   0V
VSS     vss GND 0V

V3  Vcmo     vss    0.9V
I1  VDD      Vb2    50uA
I2  Vb3      vss    50uA
I3  Vb4      vss    50uA

***-----------------------***
***        circuit        ***
```

```
***-----------------------***
Mb1     Vb2     Vb2     vss     vss     n_18_mm w=3u   l=4u     ad=0.48u*3u
as=0.48u*3u pd=0.96u+3u ps=0.96u+3u
Mb2     Vb3     Vb3     VDD     VDD     p_18_mm w=15u  l=4u     ad=0.48u*15u
as=0.48u*15u pd=0.96u+15u ps=0.96u+15u
Mb3     N1      Vb4     VDD     VDD     p_18_mm w=90u  l=4u     ad=0.48u*90u
as=0.48u*90u pd=0.96u+90u ps=0.96u+90u
Mb4     Vb4     Vb3     N1      VDD     p_18_mm w=50u  l=4u     ad=0.48u*50u
as=0.48u*50u pd=0.96u+50u ps=0.96u+50u

MSS     N2      Vb1     vss     vss     n_18_mm w=150u l=8u     ad=0.48u*150u
as=0.48u*150u pd=0.96u+150u ps=0.96u+150u
M1      N3      Vin+    N2      vss     n_18_mm w=60u  l=4u     ad=0.48u*60u
as=0.48u*60u pd=0.96u+60u ps=0.96u+60u
M2      N4      Vin-    N2      vss     n_18_mm w=60u  l=4u     ad=0.48u*60u
as=0.48u*60u pd=0.96u+60u ps=0.96u+60u
M3      Vout-   Vb2     N3      vss     n_18_mm w=65u  l=4u     ad=0.48u*65u
as=0.48u*65u pd=0.96u+65u ps=0.96u+65u
M4      Vout+   Vb2     N4      vss     n_18_mm w=65u  l=4u     ad=0.48u*65u
as=0.48u*65u pd=0.96u+65u ps=0.96u+65u

CL1     Vout-   vss     5p
CL2     Vout+   vss     5p

M5      Vout-   Vb3     N5      VDD     p_18_mm w=50u  l=4u     ad=0.48u*50u
as=0.48u*50u pd=0.96u+50u ps=0.96u+50u
M6      Vout+   Vb3     N6      VDD     p_18_mm w=50u  l=4u     ad=0.48u*50u
as=0.48u*50u pd=0.96u+50u ps=0.96u+50u
M7      N5      Vb4     VDD     VDD     p_18_mm w=90u  l=4u     ad=0.48u*90u
as=0.48u*90u pd=0.96u+90u ps=0.96u+90u
M8      N6      Vb4     VDD     VDD     p_18_mm w=90u  l=4u     ad=0.48u*90u
as=0.48u*90u pd=0.96u+90u ps=0.96u+90u

M9      Vb1     Vb1     vss     vss     n_18_mm w=8u   l=8u     ad=0.48u*8u
as=0.48u*8u pd=0.96u+8u ps=0.96u+8u
M10     N7      N7      vss     vss     n_18_mm w=8u   l=8u     ad=0.48u*8u
as=0.48u*8u pd=0.96u+8u ps=0.96u+8u
```

```
M11     N7      Vout-   N8      N8      p_18_mm w=5u   l=1u     ad=0.48u*5u
as=0.48u*5u pd=0.96u+5u ps=0.96u+5u
M12     Vb1     Vcmo    N8      N8      p_18_mm w=5u   l=1u     ad=0.48u*5u
as=0.48u*5u pd=0.96u+5u ps=0.96u+5u
M13     Vb1     Vcmo    N9      N9      p_18_mm w=5u   l=1u     ad=0.48u*5u
as=0.48u*5u pd=0.96u+5u ps=0.96u+5u
M14     N7      Vout+   N9      N9      p_18_mm w=5u   l=1u     ad=0.48u*5u
as=0.48u*5u pd=0.96u+5u ps=0.96u+5u
M15     N8      Vb4     VDD     VDD     p_18_mm w=9u   l=4u     ad=0.48u*9u
as=0.48u*9u pd=0.96u+9u ps=0.96u+9u
M16     N9      Vb4     VDD     VDD     p_18_mm w=9u   l=4u     ad=0.48u*9u
as=0.48u*9u pd=0.96u+9u ps=0.96u+9u

*Original circuit measures DC gain, 3-dB bandwidth, power, unity gain freq., Phase
Margin

.alter
*measures Acm
.tf   V(Vout+, Vout-)   V_common
V1          Vin+    Common   DC      0.8V
V2          Vin-    Common   DC      0.8V
V_common    Common    vss    DC      0V     AC  0.5

.alter
*measures Slew Rate, Settling Time
*                          PULSE(V1    V2  Tdelay  Trise   Tfall   Pwidth  Period)
V1          Vin+      vss   PULSE(0V  1.8V  1us     0ns     0ns 30us 50us)
V2          Vin-      vss    DC      0.8V
V_common    Common    vss    DC      0V

.alter
*measures gain from GND
.tf   V(Vout+, Vout-)   VSS
V_common    Common    vss    DC      0V
VSS         vss       GND    DC      0V     AC 1

.alter
*measures gain from VDD
```

```
.tf   V(Vout+, Vout-)   Vsupply
V_common    Common    vss    DC      0V
VSS         vss       GND    DC      0V
Vsupply     VDD       vss    DC      1.8V   AC 1

.end
```