HSPICE Homework #5 of「類比積體電路導論」

作業繳交截止日期: **Dec. 10, 2024 (上傳E3 數位平台繳交)**

For the fully differential operational amplifier with differential outputs shown below, perform the HSPICE simulations to obtain the following performance parameters using device parameters of UMC 0.18μm CMOS technology.

In the HSPICE simulation, the source/drain area dimensions of each MOSFET should be given.

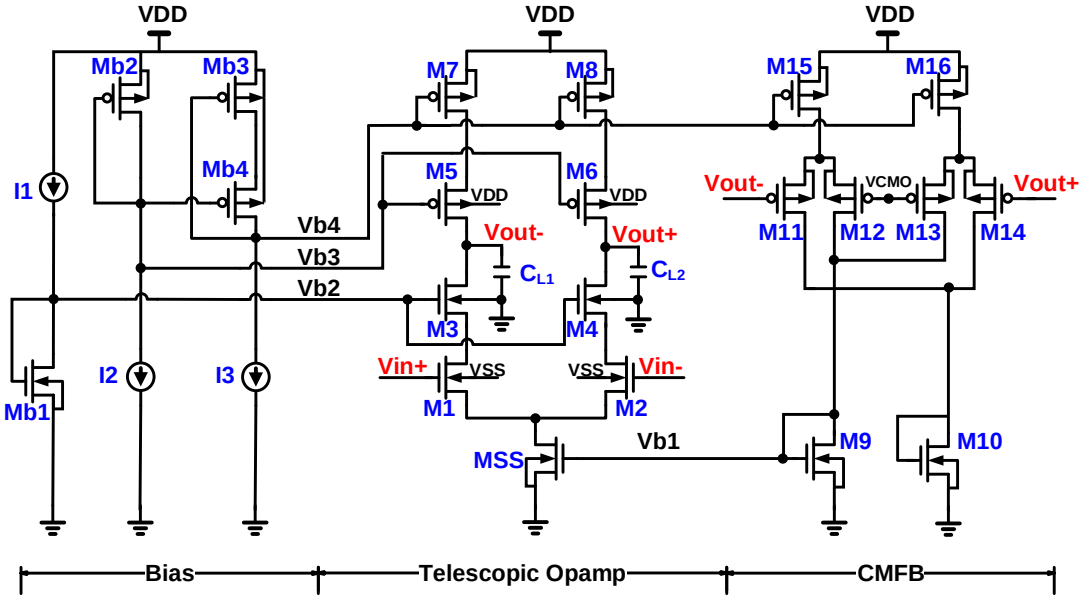
Part 1

You should simulate five corners at 25°C and fill up the following table.

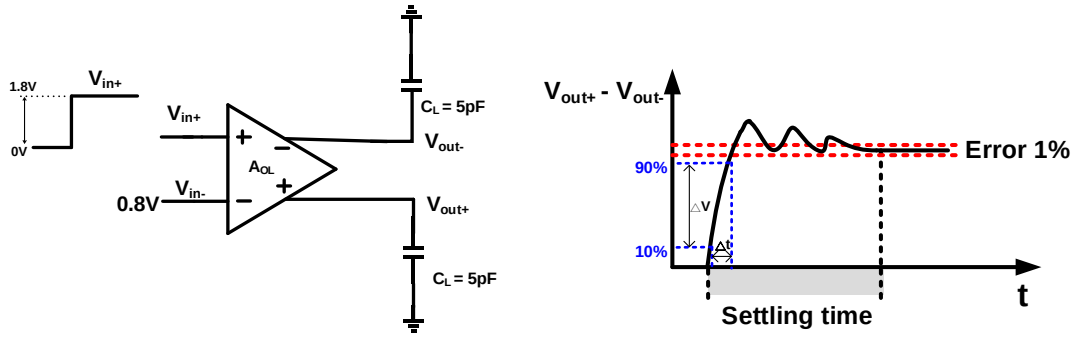
NO.	Performance Parameters	TT	FF	SS	FnSp	SnFp
1	DC Gain (dB)					
2	3-dB bandwidth(Hz)					
3	Slew rate (V/us)					
4	Settling time (us)					
5	CMRR (dB)					
6	PSRR(VDD) (dB)					
7	PSRR(GND) (dB)					
8	Unity-gain frequency (Hz)					
9	Phase margin (∘)					
10	Power (uW)					

MOSFET	W/L (um/um)	MOSFET	W/L (um/um)	MOSFET	W/L (um/um)
Mb1	3/4	M1~M2	60/4	M9~M10	8/8
Mb2	15/4	M3~M4	65/4	M11~M14	5/1
Mb3	90/4	M5~M6	50/4	M15~M16	9/4
Mb4	50/4	M7~M8	90/4		
		MSS	150/8		

SOURCE	Value
V_{IN+} & V_{IN-}	0.8 V
V_{DD}	1.8 V
V_{CMO}	0.9 V
I_1 , I_2, I_3	50 uA
C_{L1}, C_{L2}	5 pF



Definition of slew rate and settling time:



SR= $\frac{\triangle V}{\triangle t}$(10%和 90%兩點間的斜率)

Part 2

Change the device dimension of M2 to W/L=60.1u/4u and keep all the others the same. Performing part 1 on TT corner again, comparing and discussing the result.

HSPICE_HW#5: 作業需要有以下幾點：

1. HSPICE Code
2. Simulation result
3. 請列出表格
4. 以.pdf 的格式上傳，檔案名稱請使用「Hspice_HW5_ 自己的學號」（例如 ：Hspice_HW5_0811541)，於作業繳交截止日期前，上傳到指定的 E3 數位平台繳交）