Homework #2 of「類比積體電路導論」

作業繳交截止日期: Oct. 17, 2024 12:00 (上傳 E3 數位平台繳交)

本次作業共三大題, 2.1~2.3

請將作業轉成一個 PDF 檔案(file size 小於 10MB)，檔名請使用「AIC_HW2_自己的學號」(例如: AIC_HW2_109700018)，於作業繳交截止日期/時間前，上傳到指定的 E3 數位平台繳交。

Unless otherwise stated, in the following problems, use the device data shown in Table 1 and assume that $V_{DD} = 3V$. The Dielectric constant of gate oxide is 3.9 and $\varepsilon_o = 8.854 \times 10^{-12} F/m$.

Table 1. Level 1 SPICE models for NMOS and PMOS devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body-effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate-oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

2.1 Assuming all MOSFETs are in saturation, calculate the small signal voltage gain of each circuit in Fig. 1 ($\gamma = 0, \lambda \neq 0$).

本題限定使用 gm_x, r_{0x}電晶體參數符號進行推導 (30 pts)

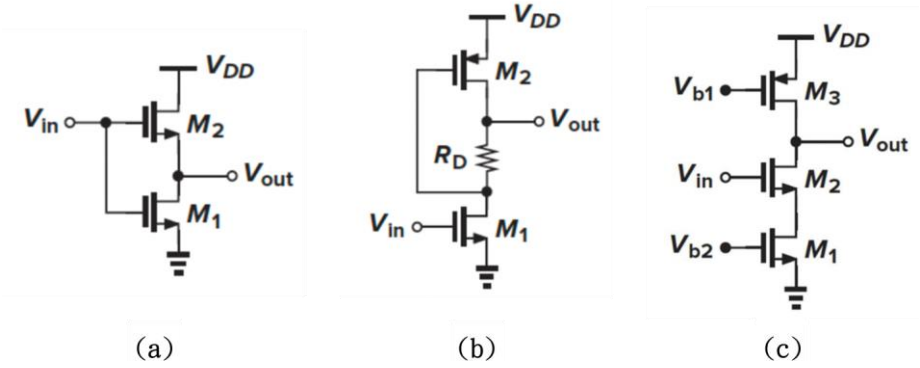

Figure 1

2.2 Assuming that all the transistors in the circuits of Fig. 2 are saturated and designed with $(W/L)_{1,2} = 45/0.3$ (μm/μm), $(W/L)_{3,4} = 10/0.3$ (μm/μm), $R_D = 5$ kΩ, and $(W/L)_5 = 75/1$ (μm/μm) with $I_{DS,M5} = 0.5$ mA.

Use $\lambda = \gamma = 0$ for bias purpose and $\gamma = 0, \lambda \neq 0$ for small signal analysis. Answer the following questions for each circuit. (45 pts)

(i) What are the minimum and maximum allowable input common mode voltage levels if the differential swings at the input and output are small?

(ii) What are the maximum allowable output voltage swing if $V_{in,CM} = 1.2$ V?

(iii) What's the differential mode voltage gain if $V_{in,CM} = 1.2$ V?

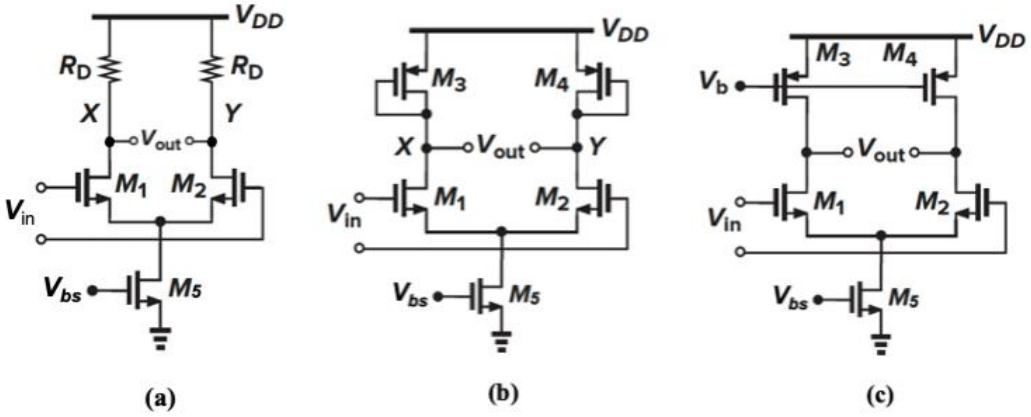

Figure 2

2.3 In the circuit of Fig. 3, assume that I_{ss}=1 mA, V_{DD}=3 V and W/L=60/0.5 for all the transistors. Also we have $I_{SD,M5} = I_{SD,M6} = 0.4 \times I_{SS}$. Use $\lambda=\gamma=0$ for bias purpose and $\lambda \neq 0$, $\gamma=0$ for small signal analysis. (25 pts)

(a) Determine the differential mode voltage gain (V_{out}/V_{in}).

(b) Calculate V_b such that $I_{SD,M5} = I_{SD,M6} = 0.4 \times I_{SS}$.

(c) If I_{SS} requires a minimum voltage of 0.4 V, what is the maximum differential output swing?

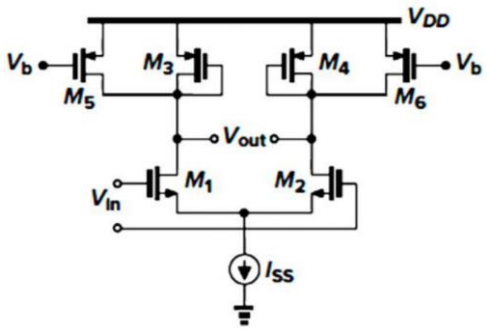

Figure 3