Homework #1 of「類比積體電路導論」

作業繳交截止日期: Oct. 3, 2024 12:00 (上傳 E3 數位平台繳交)

本次作業共三大題, 1.1~1.3

請將作業轉成一個 PDF 檔案(file size 小於 10MB)，檔名請使用「AIC_HW1_自己的學號」(例如: AIC_HW1_109700018)，於作業繳交截止日期/時間前，上傳到指定的 E3 數位平台繳交。

Unless otherwise stated, in the following problems, use the device data shown in Table 1 and assume that $V_{DD} = 3V$. The Dielectric constant of gate oxide is 3.9 and $\varepsilon_o = 8.854 \times 10^{-12} F/m$.

Table 1. Level 1 SPICE models for NMOS and PMOS devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body-effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate-oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

1.1 Assuming all MOSFETs are in saturation with $\lambda \neq 0$ and $\gamma=0$, calculate the small-signal voltage gain of each circuit in Fig. 1. 本題限定使用 R_x, gm_x, r_{ox} 電晶體參數符號進行推導 (40 pts)

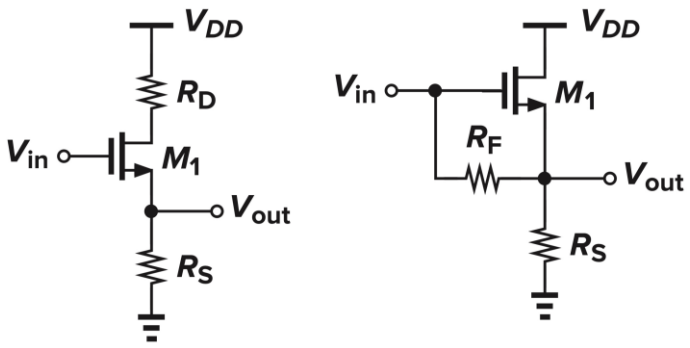

Figure 1. (a) (b)

1.2 A source follower can operate as a level shifter. Suppose the circuit of Fig. 2 is designed to shift the voltage level by 1 V, i.e., $V_{in} - V_{out} = 1V$. The body of M_1 and M_2 is connected to GND. (30 pts)

(a) Calculate the dimensions of M_1 and M_2 if $I_{D1} = I_{D2} = 0.5$ mA, $V_{GS2} - V_{GS1} = 0.5$ V, and $\lambda = \gamma = 0$.

(b) Repeat part (a) if $\lambda = 0$, $\gamma = 0.45\ V^{-1}$ and $V_{in} = 2.5$ V.

(c) If $I_{D1} = I_{D2} = 0.5$ mA, $V_{GS2} - V_{GS1} = 0.5$ V and $\lambda = 0$, $\gamma = 0.45\ V^{-1}$, what is the minimum input voltage for which M_2 remains saturated? Assume dimensions of M1 and M2 remain part(b).

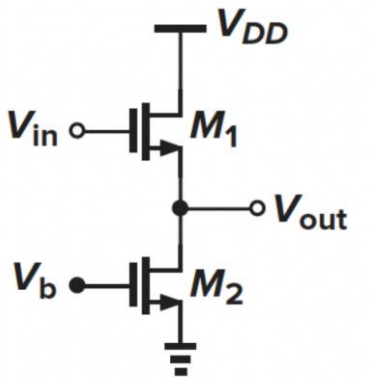

Figure 2

1.3 Suppose the common-source stage of Fig. 3 is to provide an output swing from 1 V to 2 V. Assume that W/L = 60/0.5, R_D = 2 kΩ. Also, use λ = γ = 0 for bias purpose and λ ≠ 0, γ = 0 for small signal analysis. (30 pts)

(a) Calculate the input voltages that yield V_{out} = 1 V and V_{out} = 2 V.

(b) Calculate the drain current and the transconductance of M_1 for both cases.

(c) How much does the small-signal gain for the output voltage equal 1 V and 2 V? (Variation of small-signal gain can be viewed as nonlinearity.)

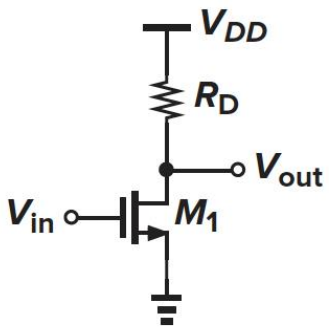

Figure 3