Homework #8 of「類比積體電路導論」

作業繳交截止日期:Dec. 12, 2024 12:00 (上傳E3數位平台繳交)

本次作業共兩大題, 8.1~8.3

請將作業轉成一個 PDF 檔案(file size 小於 10MB)，檔名請使用「AIC_HW8_自己的學號」(例如: AIC_HW8_109700018)，於作業繳交截止日期/時間前，上傳到指定的E3 數位平台繳交。

Unless otherwise stated, in the following problems, use the device data shown in Table 1 and assume that VDD=3V. The Dielectric constant of gate oxide is 3.9 and εo=$8.854\times10^{-12}F/m$.

Table 1. Level 1 SPICE models for NMOS and PMOS devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body-effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate-oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

8.1 A feedback amplifier has a loop gain of 100 and two poles at ω_{p1} and ω_{p2}. For ω_{p1}=1 MHz. (Hint: can use Bode plot)

(a) Calculate the unit gain frequency if $\omega_{p2} = 2\omega_{p1}$.

(b) Calculate the phase margin if $\omega_{p2} = 3\omega_{p1}$.

8.2 Consider the amplifier of Fig. 1, where (W/L)1-4 = 50/0.5 and $I_{SS} = I_1 = 0.5$ mA. Assume that $C_X = C_Y = 1$ pF and all the transistor capacitances can be neglected.

(a) Estimate the poles at nodes X and Y by multiplying the small-signal resistance and capacitance to ground.

(b) What is the phase margin for unity-gain feedback?

(c) Depict the Bode plot. Specify the low-frequency gain, the frequency of pole X, the frequency of Pole Y and the unit-gain frequency.

(d) What is the maximum tolerable value of C_Y that yields a phase margin of 60° for unity-gain feedback?

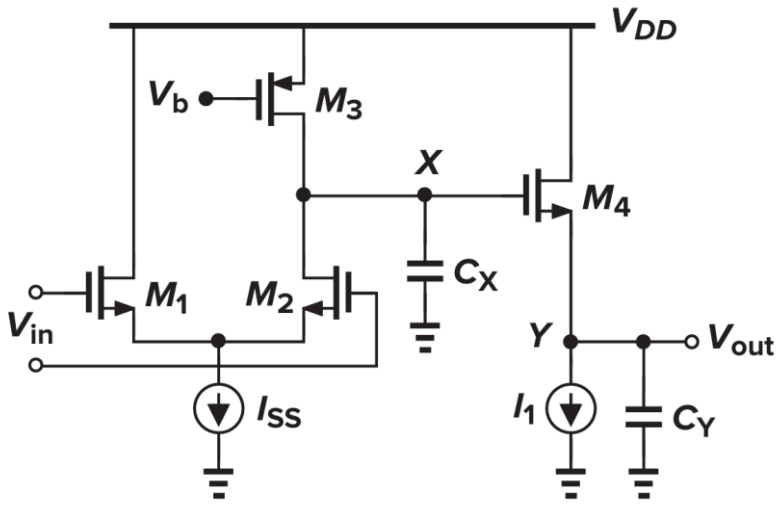

Fig. 1

8.3 For the circuit shown in Fig.2.

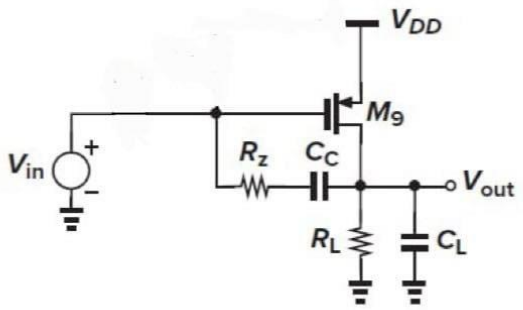

Fig. 2

(a) Find the zero of the circuit and express it in terms of a function.
(b) How will this zero affect the phase margin if Rz=0? Explain it.
(c) What value can we choose for Rz to eliminate the zero?