AIC HW4

Name: 陳彥宇 ID: 111511076

Problem 1

	Fig.(a)	Fig.(b)	Fig.(c)
Av(dB)	17.9287	0.06003	18.0703
3-dB bandwidth (Hz)	90.622M	229.905M	117.372M

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
gain_a=   7.8784
gain_b=   1.0069
gain_c=   8.0079

         ***** job concluded
```

Fig. 1: Low-Frequency Gain .measure Result

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
a_gainmax=  17.9287     at=   2.4547
            from=    1.0000     to=1000.0000x
a_f3db=  90.6221x
b_gainmax=  60.0300m    at=   6.3096
            from=    1.0000     to=1000.0000x
b_f3db= 229.9052x
c_gainmax=  18.0703     at=   3.1623
            from=    1.0000     to=1000.0000x
c_f3db= 117.3718x

         ***** job concluded
```

Fig. 2: -3dB Gain

Fig. 3: Circuit (a) -3dB Freq.

Fig. 4: Circuit (b) -3dB Freq.

Fig. 5: Circuit (c) -3dB Freq.

Problem 1 Code

```
***-----------------------***
***         setting        ***
***-----------------------***
.lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" tt
.TEMP 25
.op
***-----------------------***
***        simulation      ***
***-----------------------***

.option post
.AC DEC 100 1n 100G

***-----------------------***
***       parameters       ***
***-----------------------***
.global VDD GND
***-----------------------***
***        measure         ***
```

```
***-----------------------***
.measure ac Gain_a      FIND V(VOUT_a) at=10000Hz
.measure ac Gain_b      FIND V(VOUT_b) at=10000Hz
.measure ac Gain_c      FIND V(VOUT_c) at=10000Hz

***-----------------------***
***      power/input      ***
***-----------------------***
Vsupply VDD GND 1.8V

***-----------------------***
***        circuit        ***
***-----------------------***

Xa  VIN_a   VOUT_a  CKT_A
Xb  VIN_b   VOUT_b  CKT_B
Xc  VIN_c   VOUT_c  CKT_C

.subckt CKT_A   VIN     VOUT
RD  VDD     VOUT   15k
RS  VIN     Gate   10k
MN  VOUT    Gate   GND     GND      n_18_mm w=13u l=1.3u
C1  VOUT    GND    0.02p
V1  VIN     GND    DC      0.6V     AC  1
.ends

.subckt CKT_B   VIN     VOUT
RD  VDD     VOUT   15k
RS  VIN     Source 10k
MN  VOUT    Vb     Source  GND      n_18_mm w=13u l=1.3u
C1  VOUT    GND    0.02p
V1  VIN     GND    DC      0.3V     AC  1
V2  Vb      GND    DC      0.9V
.ends

.subckt CKT_C   VIN     VOUT
RD  VDD     VOUT   15k
RS  VIN     G1     10k
```

```
MN2 VOUT    Vb      VX      VX      n_18_mm w=13u l=1.3u
MN1 VX      G1      GND     GND     n_18_mm w=13u l=1.3u
C1  VOUT    GND     0.02p
V1  VIN     GND     DC      0.6V     AC  1
V3  Vb      GND     0.9V
.ends
.end
```

Problem 2:

Compare both low-frequency voltage gain Av and 3-dB bandwidth between these two amplifiers in Figs. (a) and (b). Please explain the reasons why they are larger or smaller.

Circuit (a) is a CS amplifier. Because the gate oxide is SiO2(basically glass), its input resistance looking into the gate is very high. On the other hand, circuit (b) is a CG amplifier, the input resistance looking into the source is given by 1/gm. 1/gm is typically only 1~2kΩ. After voltage division with Rs (10kΩ), the input voltage is significantly reduced to less than 20% its original value. This is why even though circuit (a) & (b) have identical output resistance, but (b) has a lower gain. This low input resistance problem can be resolved by using a cascode amplifier, as shown in circuit (c).

While CS amplifiers have the advantage of high input resistance, they have the problem of small bandwidth due to Miller effect. Due to this, the input capacitance is greatly increased, as shown by the following equation:

$$C_{in} \approx C_{gd} \times (1 + |A_v|)$$

CG amplifiers do not experience Miller effect, so they have a larger gain bandwidth. As shown in problem 1, the CS amplifier of circuit (a) only has a bandwidth of 90.1MHz, while the CG amplifier of circuit (b) has a bandwidth of 231MHz. We can combine the best of both worlds: high input resistance & large bandwidth by using a cascode amplifier, like the one in circuit (c).

Problem 3:

Compare both output noise voltage and input-referred noise between these two amplifiers in Figs. (a) and (c). Please describe the results you observed and explain whether you think MN2 in Fig. (c) has a significant impact on the total output noise. If not, please explain the reason for your assessment.

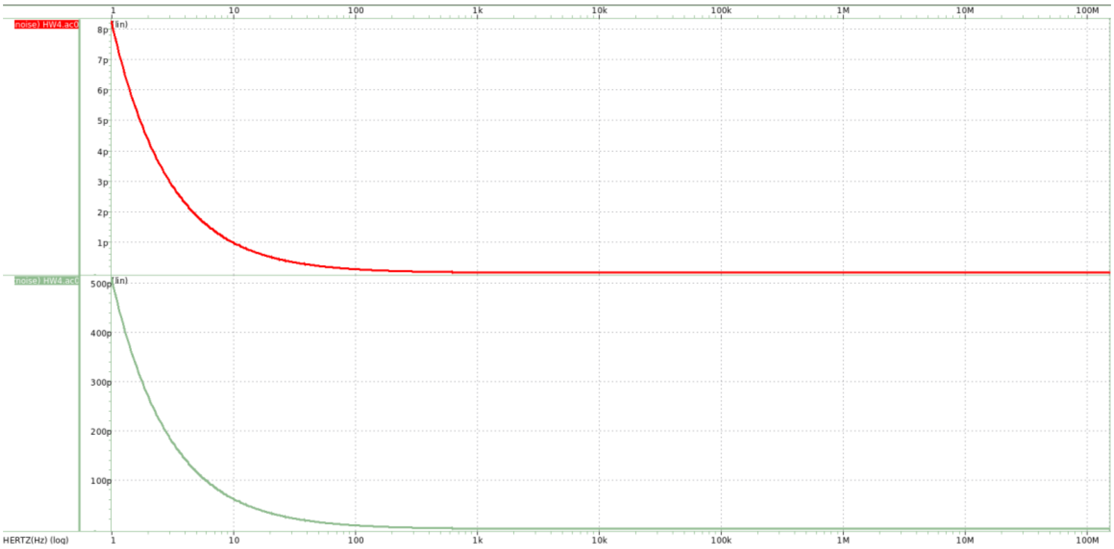

Fig. 6: Circuit (a) innoise & outnoise 1 ~ 150MHz

```
**** the results of the sqrt of integral (V^2 / freq)
     from fstart upto 151.3561x      Hz. using more freq points
     results in more accurate total noise values.

**** total output noise voltage   =    1.0794m      V

 **** total equivalent input noise =  175.3984u      V
```

Fig. 7: Circuit (a) Input-referred Noise

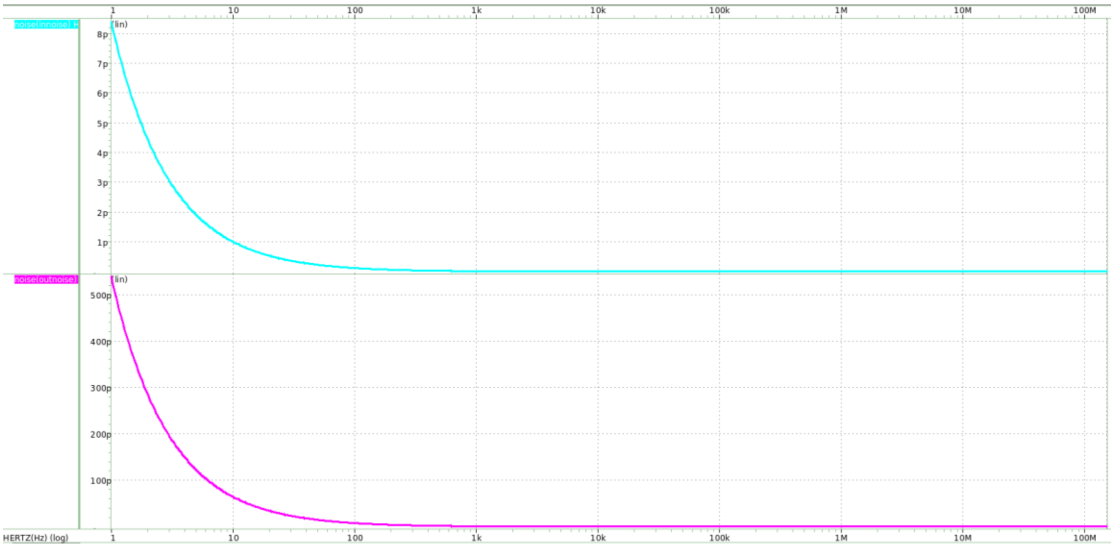

Fig. 8: Circuit (c) innoise & outnoise 1 ~ 150MHz

```
**** the results of the sqrt of integral (V^2 / freq)
     from fstart upto  151.3561x       Hz. using more freq points
     results in more accurate total noise values.

**** total output noise voltage   =    1.1921m      V

 **** total equivalent input noise =  177.6834u      V
```

Fig. 9: Circuit (c) Input-referred Noise

MN2 of circuit(c) has very small impact on the total output noise at low frequencies. We can use the following equivalent circuit to analyze this:

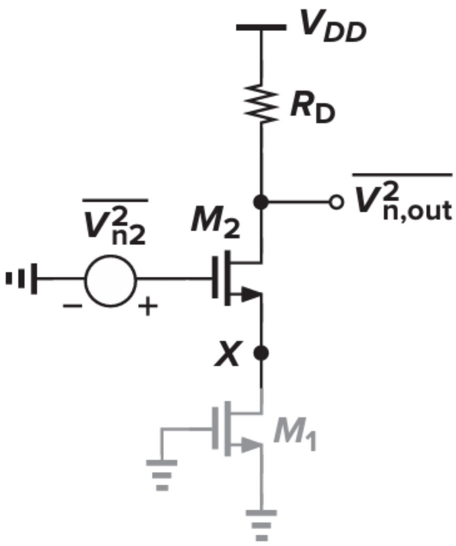

Fig. 10: Equivalent Circuit for M2 Input-referred Noise

In this circuit, the input-referred noise of M2 passes through a source-degenerated CS configuration, whose Gm is given by:

$$G_{m2} = \frac{g_{m2}}{1 + g_{m2}R_x}$$

The equation indicates that the gain seen from the M2's gate to M2's drain is small if Rx is large. In order to prove this through simulation, I modified my code to run an AC analysis from M2's gate to M2's drain. Notice that the gain at low frequency is quite small. However, the gain begins to increase past 10MHz. This is due to the capacitance at node X. At high frequencies, the gain from M2's gate to M2's drain is given by:

$$\frac{V_{n,out}}{V_{n2}} \approx \frac{-R_D}{\frac{1}{g_{m2}} + \frac{1}{C_x s}}$$

Therefore, M2 starts contributing more to the total output noise as the frequency increases.

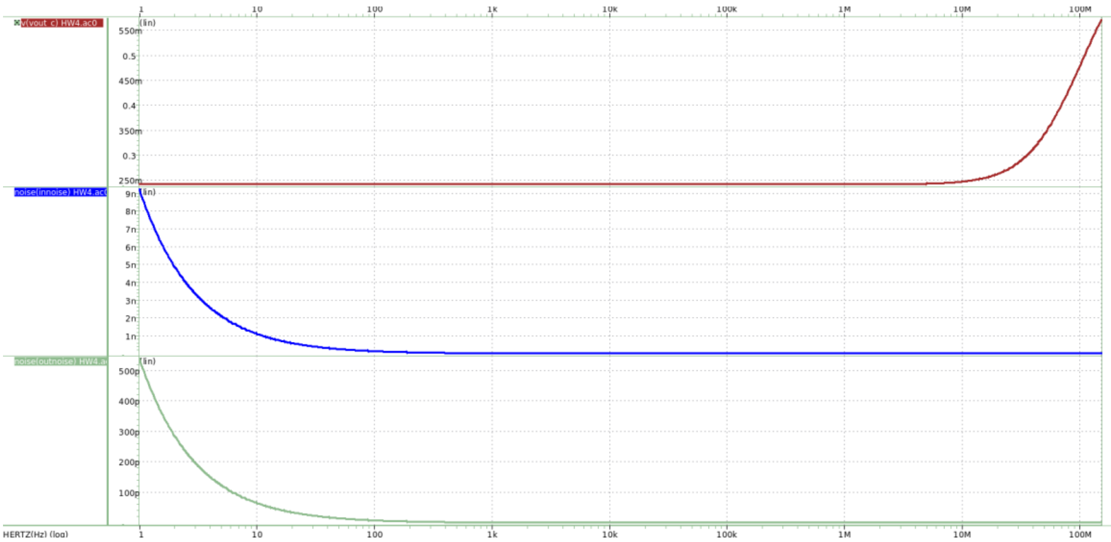

Fig. 11: Circuit (c) innoise & outnoise 1 ~ 150MHz from M2's gate to M2's drain

Problem 3 Code:

```
***-----------------------***
***        setting        ***
***-----------------------***
.lib "~/U18_HSPICE_Model/mm180_reg18_v124.lib" tt
.TEMP 25
.op
***-----------------------***
***       simulation      ***
***-----------------------***

.option post
.ac    DEC  100 1 150Meg
.noise V(VOUT_a)   VA  1

***-----------------------***
***      parameters       ***
***-----------------------***
.global VDD GND
***-----------------------***
```

```
***       measure        ***
***-----------------------***

***-----------------------***
***      power/input      ***
***-----------------------***
Vsupply VDD GND 1.8V
VA  VIN_a     GND    DC      0.6V     AC  1
VC  VIN_c     GND    DC      0.6V     AC  1

***-----------------------***
***        circuit        ***
***-----------------------***
Xa  VIN_a   VOUT_a  CKT_A
Xc  VIN_c   VOUT_c  CKT_C

.subckt CKT_A   VIN     VOUT
RD  VDD     VOUT   15k
RS  VIN     Gate   10k
MN  VOUT    Gate   GND     GND      n_18_mm w=13u l=1.3u
C1  VOUT    GND    0.02p
*V1  VIN     GND    DC      0.6V     AC  1
.ends

.subckt CKT_B   VIN     VOUT
RD  VDD     VOUT   15k
RS  VIN     Source 10k
MN  VOUT    Vb     Source  GND      n_18_mm w=13u l=1.3u
C1  VOUT    GND    0.02p
V1  VIN     GND    DC      0.3V     AC  1
V2  Vb      GND    DC      0.9V
.ends

.subckt CKT_C   VIN     VOUT
RD  VDD     VOUT   15k
RS  VIN     G1     10k
MN2 VOUT    Vb     VX      VX      n_18_mm w=13u l=1.3u
MN1 VX      G1     GND     GND     n_18_mm w=13u l=1.3u
```

```
C1  VOUT    GND    0.02p
V3  Vb      GND    0.9V
.ends

.alter
.noise V(VOUT_c)   VC  1

.end
```