國立陽明交通大學 期中 學期 考試答案紙

National Yang Ming Chiao Tung University Midterm/Final Examination Answer Sheet

記 分 Score
94

36.

112 學年度第 1 學期

Semester of Year

科目 VLSI 系所 電機 年級 3

Course title Department Year

考試日期 112 年 11 月 13 日 學號 110511118 姓名 陳宏頡

Date Y M D Student ID no. Name

從此處開始寫起 Please write from here

A. 1. F 2. F 3. T 4. F 5. F

6. F 7. F 8. T 9. T 10. T

explain: 1. For more transistors

2. MOS are voltage-controlled devices

4. Noise will change behavior in dynamic circuit.

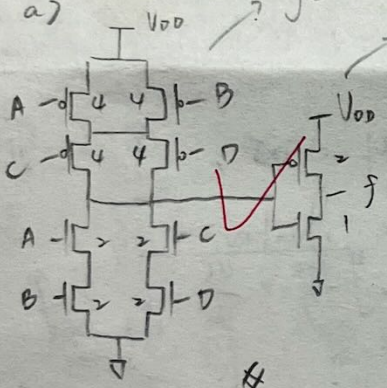
5. Pseudo-NMOS doesn't have better performance in power consumption

6. Area is bigger

7. g can be less than 1

B.

1. a)



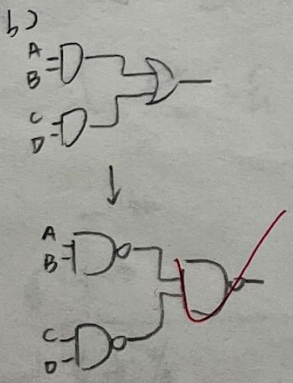
g=2 g=1

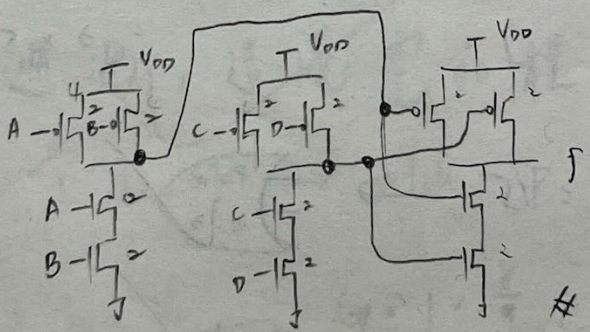
G = 2 B = 1 P = 4+1 = 5

$\hat{f} = \sqrt[3]{GBH} = \sqrt{2H}$

$D = 2 \cdot \sqrt{2H} + 5$ #

b)





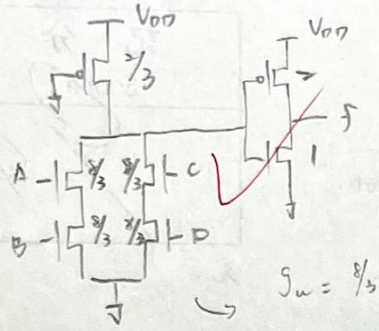
#

$G = \frac{4}{3} \times \frac{4}{3} = \frac{16}{9}$ B = 1 P = 2+2 = 4

$\hat{f} = \sqrt{\frac{16}{9}H} = \frac{4}{3}\sqrt{H}$

$D = 2 \cdot \frac{4}{3}\sqrt{H} + 4 = \frac{8}{3}\sqrt{H} + 4$ #

c)



Requirement : ① connect the remaining pMOS to GND

② make pMOS about 1/4 effective strength of pull down network. ✳

$S_u = 8/3$, $g_d = 8/9$, $S_{avg} = 16/9$

$P_u = 6$, $P_d = 2$, $P_{avg} = 4$

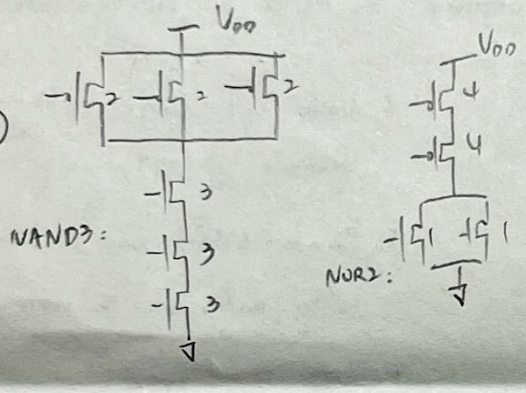
$\Rightarrow D = 2 \cdot \sqrt{\frac{16}{9} H} + 4$

$= \frac{8}{3}\sqrt{H} + 4$

→ speed is better than (a) ✳

2.

a)



	NAND3	NOR2
g	5/3	5/3
p	3	2

✳

b) $G = \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3} = \frac{100}{27}$

$H = \frac{45}{8}$

$B = 2 \times 3 = 6$

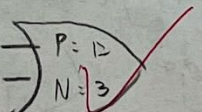
$P = 2 + 3 + 2 = 7$

$\Rightarrow F = GBH = 125$, $\hat{f} = \sqrt[3]{125} = 5$

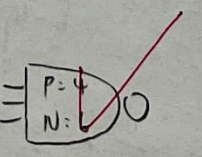
$\Rightarrow D = 3 \cdot \sqrt[3]{\frac{100}{27} \times \frac{45}{8} \times 6} + 7$

$= 3 \times 5 + 7 = 22$ ✳

c) $y = \frac{45}{5} \times \frac{5}{3} = 15$ →



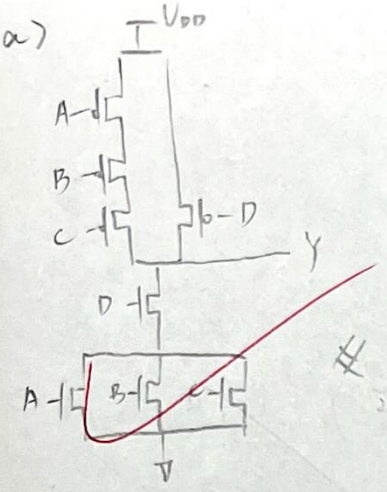
$x = \frac{15 \times 2}{5} \times \frac{5}{3} = 10$ →



✳

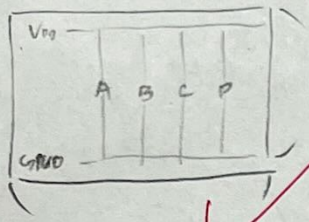
d) No, if we only down-size the top 2 3-inputs, some path are faster than the others, and we still have to wait for the latest path.

3. a)



$\Rightarrow Y = \overline{(A+B+C)\cdot D}$ ※

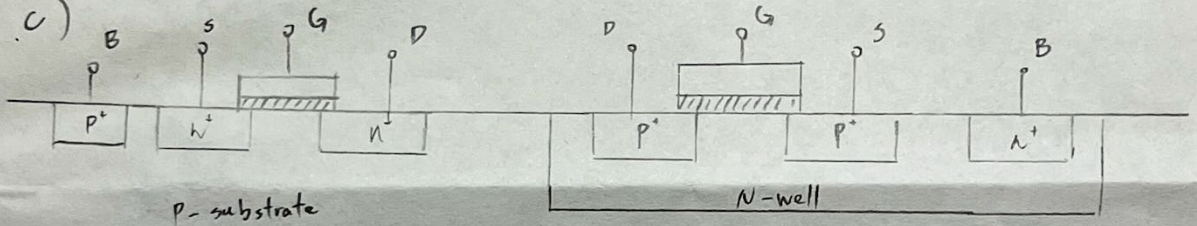
b)



$6 \times 8\lambda = 48\lambda$

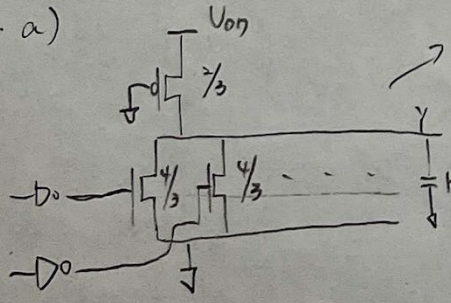
$5 \times 8\lambda = 40\lambda$ ※

c)



⇒ 若 well contacts 沒有做好，會導致電晶體內到偏壓跑掉，會在各材料交界處形成順向偏壓，使大電流通過，造成電晶體甚至電路燒掉或無法正常工作 → latch-up ※

4. a)



$g_u = 4/3$

$g_d = 4/9$

$g_{avg} = 8/9$

$P_u = \frac{2}{3} + \frac{4}{3}k$

$P_d = \frac{2}{9} + \frac{4}{9}k$

$P_{avg} = \frac{4}{9} + \frac{8}{9}k$

$G = 1 \times \frac{8}{9} = \frac{8}{9}$

$B = 1$

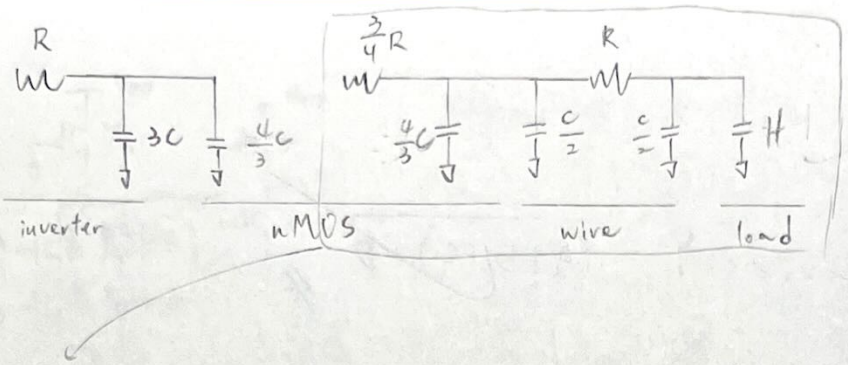
$H = \frac{H}{1}$

$P = 1 + \frac{4}{9} + \frac{8}{9}k = \frac{13}{9} + \frac{8}{9}k$

$\Rightarrow F = \frac{8}{9}H$, $\hat{f} = \frac{2}{3}\sqrt{2H}$

$D = 2 \cdot \frac{2}{3}\sqrt{2H} + \frac{13}{9} + \frac{8}{9}k$ ※

b)



calculate delay of the stage $= \frac{3}{4}R\left(\frac{4}{3}C + \frac{C}{2}\right) + \left(\frac{3}{4}R + R\right)\left(\frac{C}{2} + H\right)$

$= \frac{11}{8}RC + \frac{7}{8}RC + \frac{7}{4}RH$

$= \frac{18}{8}RC + \frac{7}{4}RH$

$= \frac{9}{4}RC + \frac{7}{4}RH$ //