Introduction to VLSI Design: Final-Term Exam

2019/1/8, Tue. 15:30-17:30@ED220

Note: this is a closed-book exam allowing one-page A4 summary for reference. You may make assumption whenever necessary in answering the following questions.

A. [20%] True (T) or False (F) for the following 10 statements.

1. Current sequential designs often exploit HDL-based design with edge-triggered elements, where soft-edge is allowed to overcome clock skew and jitter issues.
2. Speed of Carry Propagation Adder (CPA) can be improved by adding extra circuits dealing with carry propagation, leading to extra more power consumption as well.
3. Storage elements can be classified into two types, namely fore-ground and back-ground memory types, where the latter may demand several clock cycles during data accesses.
4. Design for testability (DFT) is very important in current chip designs for system-level integration, where built-in-self-test (BIST) is one solutions to reduce test time and cost.
5. Bonding wires from packages to silicon dices will lead to supply voltage drop due to parasitic inductance effect and hence the current variation should be limited in on-chip designs.
6. Power consumption from both dynamic power and static power should be minimized to achieve less packaging cost, where both parallelism and pipelining schemes are often exploited to reduce the dynamic power.
7. Static power dissipation can be further reduced by exploiting both stacked transistors and body biasing at circuit level without degrading overall circuit performance.
8. Switching activity factor (α) is highly dependent on both input (0,1) probability and logic gate function.
9. On-chip clock generation is very important for current chip designs to achieve both high performance and low-power indices.
10. In modern system-on-chip (SoC) designs for data-driven applications, on-chip memory is often the dominated part of the chip and is realized by SRAM with high-performance CMOS process technology.

B. [80%] Answer the following 4 questions:

1. [20%] High-speed multiplier-and-accumulators (MAC) are often requested for many communication and signal processing systems.

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Booth Encoding converts radix 2 multiplication to radix 4 or 8 by representing numbers with negative terms.

(a) For high-speed parallel multiplier design, Booth encoding is considered to reduce the number of partial products. Explain how this Booth encoding scheme works to reduce the number of partial products by half. [8%]

(b) Explain how Carry-Save-Adder (CSA) is realized and can be exploited to speed up the summation of partial products. [6%]

(c) If a 16X16 parallel multiplier with an accumulator (MAC) is to be designed by the schemes mentioned in (a) and (b), draw a block diagram of the MAC and then indicate how many levels of CSA's are needed before carry-propagation adder (CPA)? [6%]

2. [20%] Static Random Access Memory (RAM) is a key storage module in current system designs, especially for data-driven applications.

(a) Draw a 6-T SRAM cell and specify the driving capability of these transistors so that read/write operations can be completed accurately. [8%]

(b) Explain why sense amplifiers are needed in SRAM. Draw a circuit diagram and explain how it works to speed up access time. [6%]

(c) Modify the 6-T SRAM cell so that it can be used for content addressable memory (CAM) for parallel data match. [6%]

3. [20%] A 1-bit Full-Adder (FA) with inputs (A,B,C) and outputs (S,Co) can be realized by different approaches.

(a) Exploit programmable logic array (PLA) to realize the 1-bit FA with NOR-NOR structure, where dot represents there is a transistor. [6%]

(b) Realize the 1-bit FA in read-only-memory (ROM) with NOR-NOR structure. [6%]

(c) Find the corresponding input patterns to identify SA0/SA1 faults at outputs (S,Co). [8%]

4. [20%] I/O PADs need to be designed carefully to ensure circuit and system performance in CMOS fabrication.

(a) Explain why guard-ring is needed in I/O pads to avoid latch-up. Using Inverter as example to explain how latch-up occurs in CMOS fabrication. [8%]

(b) Draw an ESD protection circuit and explain how it works in INPUT PADS. [6%]

(c) Include a tri-state output driver in (b) so that a bi-directional I/O pad can be achieved, what is the major design issue for this output driver circuit? [6%]

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