Final-Term Exam on Introduction to VLSI Design

Date: Jan. 5, 2018, 10:10-12:10@ED220

Note: This is a closed book exam with one A4-page summary for reference. Make any assumption whenever necessary to answer your question.

A. [20%] True (T) or False (F) for the following 10 questions

F 1. Timing violation in sequential designs can ~~always~~ be solved by increasing cycle time.

F 2. Given a sequential design, ~~single~~ multi → harder to design, but allows pipelining and phase clocking can achieve better computational performance than that from multi-phase clocking. time borrowing

F 3. Given an edge-triggered design, higher clocking rate can be achieved by positive skew ~~without degrading design stability~~. skew adds sequencing overhead

T 4. Built-in-self-test (BIST) is very important in current chip designs to reduce chip testing time and identify manufacturing faults.

T 5. Chip I/O data pins have to be slew-rate controlled to minimize voltage drop over power supply lines.

T 6. Dynamic power consumption can be reduced by exploring parallelism and pipelining of data operations to lower down supply voltage.

F 7. Stacked transistors can reduce leakage current because ~~threshold voltage~~ (V_T) is reduced. Stacking doesn't change V_{TH}

T 8. On-chip clock generator using phase-locked-loop (PLL) is very important to generate high-speed clocks with minimized jitter in current chip designs.

T 9. Soft-edge designs can be achieved by exploiting overlapped multi-phase clocking for domino logic gates to overcome clock skew. 不去

F 10. SRAM and DRAM can be realized by standard CMOS technology, where the former achieves better speed and storage capacity than the latter.

SRAM Faster, DRAM stores more for the same number of transistors

B. [20%] High-speed parallel multipliers are often demanded in current complex chip designs for communication and data analysis.

1. Explain why Booth Encoding scheme can be exploited to reduce the number of partial products without increasing the complexity of partial product generation. Note that you may use Radix 2^2 as example to explain why the number of partial products can be reduced by half. [8%] Falle

2. Draw the circuit diagram of each bit in partial product generation. [6%]

3. If these partial products are summed to generate the final product by

carry-save-adder (CSA) array and carry propagation adder (CPA) in the last stage, how many levels of CSA are demanded before arriving at the input of CPA for a 16X16 multiplier? [6%]

C. [20%] Static Random Access Memory (SRAM) is often exploited in chip design to buffer input and temporary data to improve overall computational performance.

1. Draw a 6-T SRAM Cell and identify the strength of each transistor so that data access (read and write) can be done correctly. [8%]
2. Explain why sense amplifier is needed to speed up the data read-out time. [4%]
3. Modify the 6-T SRAM cell so that it can be used for data matching and then explain why it is very power consumptive as content addressable memory (CAM) for matching large volumes of datasets. [8%]

D. [20%] Read-Only Memory (ROM) and Programmable Logic Array (PLA) can be used to realize many logic functions needed in a complex system.

1. Explain why both ROM and PLA can be realized by NOR-NOR plane. [4%]
2. If 1-bit full-adder (input: A, B, C; output: S, Co) is to be realized by ROM and PLA respectively, you're asked to draw each NOR-NOR plane with black dots to label where those transistors are located. [12%]
3. Since Pseudo-NMOS designs are very power consumptive, how do you modify the circuit so that no power is lost when ROM and PLA are not activated? [4%]

E. [20%] Bi-directional PAD's are often included in chip I/O to reduce pin-count.

1. Draw the circuit diagram for ESD protection and explain how it works. [6%]
2. Draw the circuit diagram for tri-state output buffer and explain how it works. [6%]
3. Find the test patterns for the last stage of the tri-state buffer to ensure there are no SA1 and SA0 faults. [4%]
4. If both inputs (EN and D) of the tri-state output buffer have equal probability of "1" and "0", what is the probability to make the last stage charge or discharge? [4%]

A.

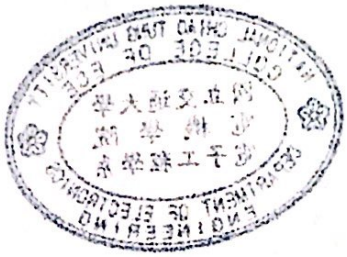
1. F
2. F
3. F
4. T
5. T
6. T
7. F
8. T
9. T
10. F

sum = $AB'C' + A'BC' + A'B'C + ABC$

cout = $AB + AC + BC$

$[(A'+B+C)' + (A+B'+C)' + (A+B+C')' + (A'+B'+C')']'$

$= AB'C' +$

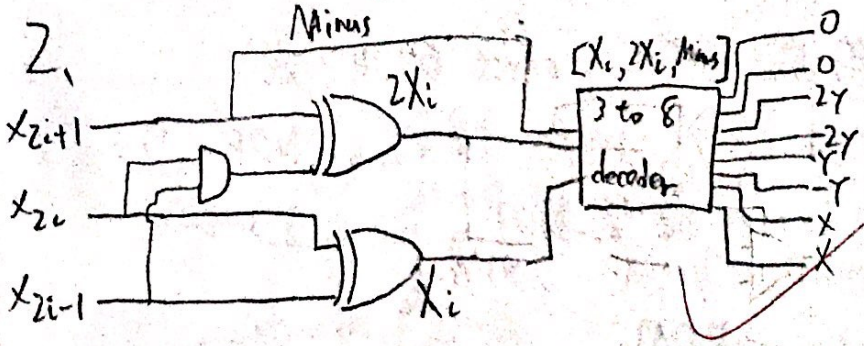


B. 1. booth encoding 可以一次看多個(乘數的) bit，故可 reduce partial product 數而他又不會新增一些計算較複雜的 partial product 故不會提升 complexity. 以下是 radix-4 的 booth-encoding table，X 為乘數，Y 為被乘

X_{2i+1}	X_{2i}	X_{2i-1}	PP_i	Y_i	$2Y_i$	Minus
0	0	0	0	0	0	0
0	0	1	Y	1	0	0
0	1	0	Y	1	0	0
0	1	1	2Y	0	1	0
1	0	0	-2Y	0	1	1
1	0	1	-Y	1	0	1
1	1	0	-Y	1	0	1
1	1	1	0	0	0	1

radix-4 是一次跳兩個 bit，並看該 bit 的前後各 1 bit，並從隔壁表中根據 X_{2i+1} X_{2i} X_{2i-1} 的值去得到一個 partial product，故相較於原本每個 X_i 都去得到 partial product，用 radix-4 次 X_{2i} 去得到的 partial product 明顯更為 X_i 的一半 #

2、



$X_i = X_{2i-1} \oplus X_{2i}$

$2X_i = X_{2i+1} \oplus (X_{2i} \cdot X_{2i-1})$.

3、16 bit

$16 \cdot \frac{2}{3} = 11$ $6 \cdot \frac{2}{3} = 4$

$11 \cdot \frac{2}{3} = 8$ $4 \cdot \frac{2}{3} = 3$

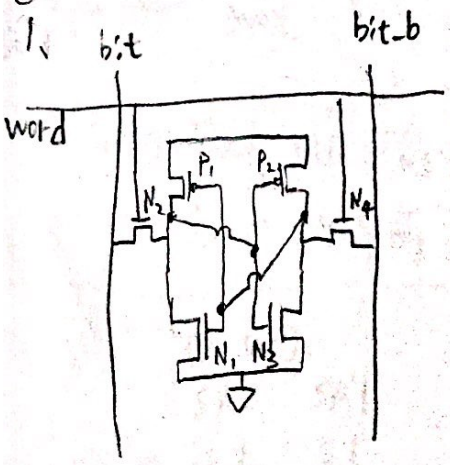
$8 \cdot \frac{2}{3} = 6$ $3 \cdot \frac{2}{3} = 2$

6 level

4 #

C.

1、



for read $N_1 >> N_2$

for write $N_2 >> P_1$

N_1, N_3 strong

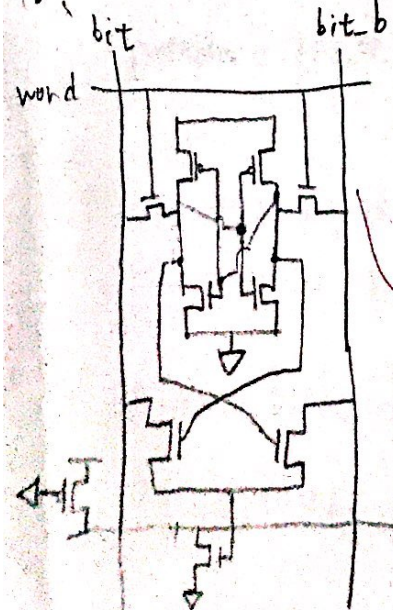
N_2, N_4 medium

P_1, P_2 weak

-6

有時 bit and bit_b 的差距不大，要靠 sense Amp 放大.

3、



when matched Matchline = high

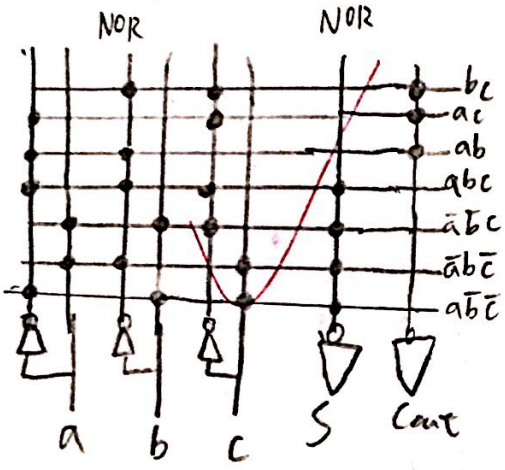
not matched Matchline = low

why cosume a lot power

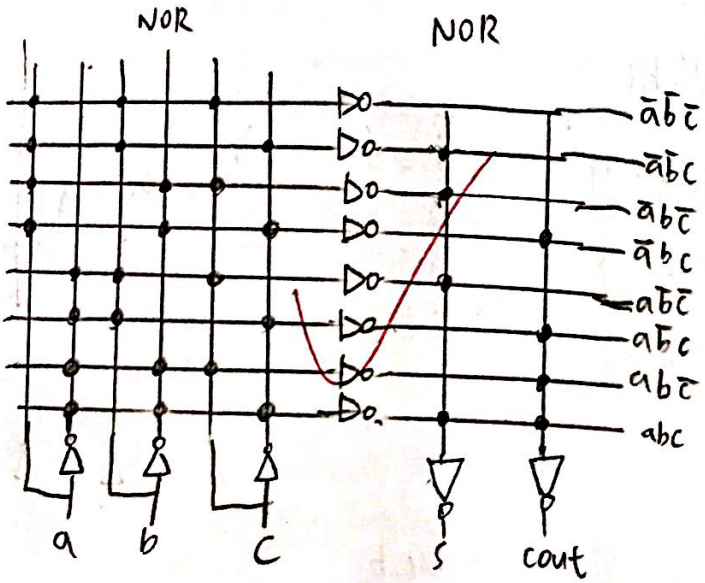
A: Because when match struct is based on Pseudo-NMOS, the transistor in match block will fight with the V_{DD} and consume power. #

D、1、ROM and PLA 都可用成 sum of product 的形式.
而 AND 本身只要將 input, output 都加 inverter 就能變 NOR D=D
OR 本身在 ouput 加 inverter 就變 NOR, D = D 好麼?

2、PLA



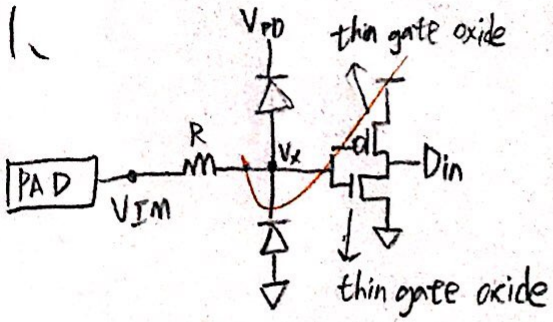
ROM



3、在後面加上 latch 或 flip-flop 在值。

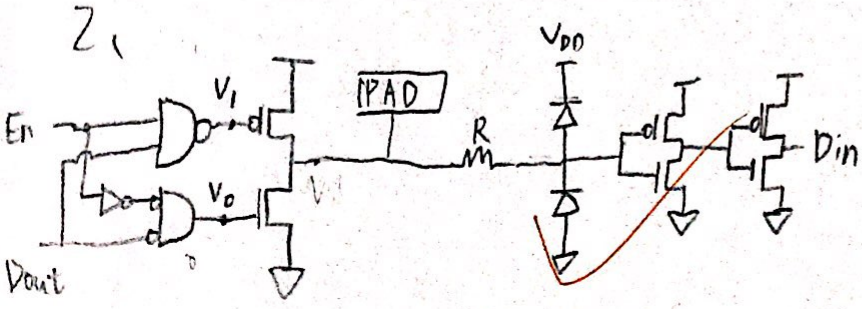
E.

1、



Input pad first put a resistor and protect it by diode clamped to lock the direction and at last thin gate oxide inverters are implemented.

2、



when En=1, PAD 輸出 Dout

En=0, PAD 輸入至 Din

3、

[En, Dout]

	SA0	SA1
En	1	0
Dout	1	0

(V1)

[En, Dout]

	SA0	SA1
En	1	0
Dout	1	0

(V0)

V0、V1 標在上面

前為 En，後為 Dout

pattern = {00, 01, 10, 11}

4、 En=1, D=1, charge

En=1, D=0, discharge

$P(En=1, D=1) = \frac{1}{2} \cdot \frac{1}{2} = \frac{1}{4}$ #

$P(En=1, D=0) = \frac{1}{2} \cdot \frac{1}{2} = \frac{1}{4}$ #