Introduction to VLSI Design: Final-Term Exam

2020/1/7, Tue. 15:30-17:30@ED220

Note: this is a closed-book exam allowing one-page A4 summary for reference. You may make assumption whenever necessary in answering the following questions.

A. [20%] True (T) or False (F) for the following 10 statements.

T 1. Current sequential designs often exploit HDL-based design with edge-triggered elements, where soft-edge is allowed to ~~overcome clock skew~~ and jitter issues.

T 2. Speed of Carry Propagation Adder (CPA) can be improved by adding extra circuits dealing with carry propagation, leading to extra more power consumption as well.

F 3. H-tree clock distribution can be exploited to minimize clock skew, and in the meantime, to save power consumption as well.

T 4. Design for testability (DFT) is very important in current chip designs, where built-in-self-test (BIST) is one solution to reduce test time and cost.

T 5. Bonding wires from packages to silicon dices will lead to supply voltage drop due to parasitic inductance effect and hence multiple power pads are demanded to ensure target computation performance.

T 6. Power consumption from both dynamic power and static power should be minimized to achieve less packaging cost, where both parallelism and pipelining schemes are often exploited to reduce dynamic power consumption with limited area overhead.

F 7. Static power dissipation in CMOS fabrication can be further reduced by exploiting both stacked transistors and body biasing at circuit level without degrading overall circuit performance. Too much body bias degrades performance

F 8. ~~Dynamic~~ Static power can be further reduced by exploiting low-V_t and high-V_t transistors, where low-Vt transistors are used in critical path designs.

T 9. PLL-based on-chip clock generator is a very important for current system-on-chip (SoC) designs to achieve both high performance and low-power indices.

T 10. Input PAD needs to have ESD protection circuits, which are often realized by diodes and current-limit resistors.

B. [80%] Answer the following 4 questions:

1. [20%] High-speed multiplier-and-accumulators (MAC) are often requested in many communication and data-driven systems.

(a) For high-speed parallel multiplier design, Booth encoding is considered to reduce the number of partial products. Explain how this Booth encoding scheme works to reduce

the number of partial products by half. [6%]

(b) Draw a one-bit circuit to generate the partial product based on Booth Encoding scheme. Note that you may use dot to illustrate a complete partial product for 2's complement and sign extension. [8%]

(c) Assume a 16X16 parallel multiplier with an accumulator (MAC) is to be designed by the above-mentioned schemes, draw a block diagram of the MAC and then indicate how many levels of CSA's are needed before carry-propagation adder (CPA)? [6%]

2. [20%] Static Random Access Memory (SRAM) is a key storage module in current system designs, especially for data-driven applications.

(a) Draw a 6-T SRAM cell and specify the driving capability of these transistors so that read/write operations can be operated accurately. [6%]

(b) Explain why both row and column address decoders are needed in SRAM designs. [6%]

(c) Add 3 transistors to the 6-T SRAM cell so that it can be used for content addressable memory (CAM) and then explain how it can be exploited for parallel data search. [8%]

3. [20%] A 1-bit Full-Adder (FA) with inputs (A,B,C) and outputs (S,Co) can be realized by different approaches.

(a) Exploit programmable logic array (PLA) to realize the 1-bit FA. Note that NOR-NOR structure with pseudo-NMOS is the target structure, where dot represents there is a transistor. [8%]

(b) Exploit read-only-memory (ROM) to realize the 1-bit FA with NOR-NOR structure, where dot represents there is a transistor. [8%]

(c) Identify which one, i.e. (a) or (b) has lower power consumption and then modify the pseudo-NMOS structure to reduce static power when it is not used. [4%]

4. [20%] A 1-bit half-adder (S=A'B+AB', C=AB) is to be realized by 2-input NAND gates only. You're asked to answer the following:

(a) Realize the 1-bit half adder using 5 2-input NAND gates. [4%]

(b) Assume 2 inputs (A,B) have the same probability of {0,1}, estimate the activity factor (α) at S and C respectively. [8%]

(c) Find the minimum test patterns to observe faults (SA0,SA1) in this NAND-based half adder. [8%]

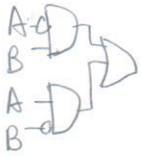
$\overline{A'+B'}$ = AB

$\overline{A'B'} = A+B$

A B	S C
0 0	0 0
0 1	1 0
1 0	1 0
1 1	0 1

$(A+B)(A'+B')$

$C' = A'B' +$



$\overline{(A+B')} = A'B$

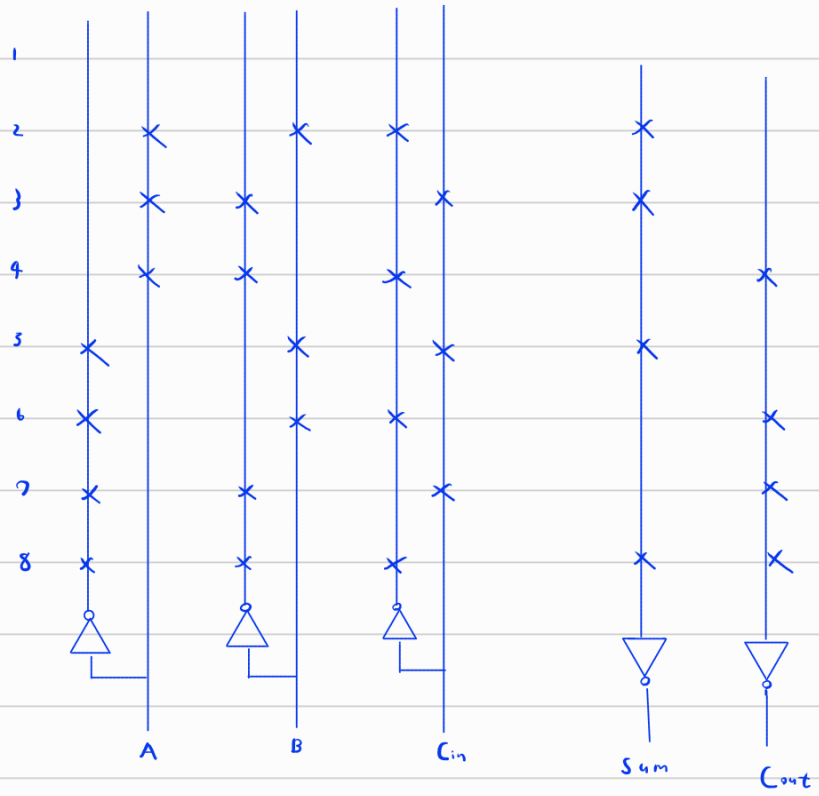
$C' = A'+B' = \overline{(AB)}$

$S' = \overline{A'B+AB'}$

$= (A'B)'(AB')'$

$S' = (A+B')(A'+B)$

$\overline{(\overline{A'B})(\overline{AB'})} = S = \overline{(A+B')(A'+B)}$

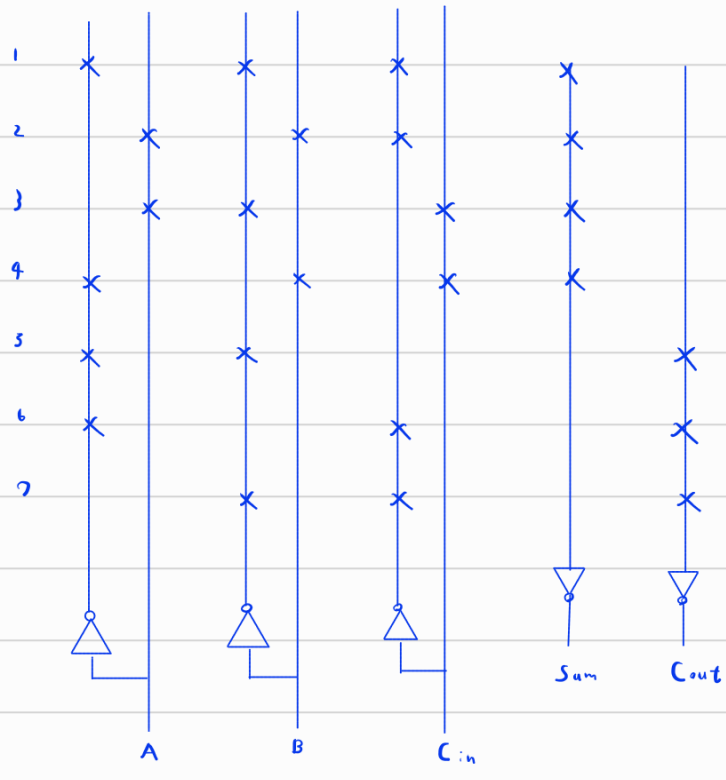


ROM

$S = ABC + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$

$Cout = AB + BC + AC$

$= AB\bar{C} + ABC + \bar{A}BC + A\bar{B}C$



PLA