Introduction to VLSI Design: Mid-Term Exam

Nov. 13, 2023, 15:30-18:00@ED220

Note: this is a closed-book exam allowing one-page A4 summary for reference. You may make assumption whenever necessary in answering the following questions.

A. [20%] True (T) or False (F) for the following 10 statements.

T 1. Advanced technology nodes, such as 3nm and 2ns, FinFET and GAAFET transistors are preferred because of less leakage current for very large scale (e.g. >10B) integration.

T 2. In current CMOS technology, transistors are current-controlled devices and can be easily integrated to achieve analog and digital chips for various applications.

T 3. Voltage Transfer Curve (VTC) of any complementary logic gates can be tuned to cope with noise margins and enhance speed in combinational logic by changing driving capability in P and N networks respectively.

F 4. Noise through coupling capacitors does have some impacts on speed but not change logic behaviors of both static and dynamic logic/circuit operations.

F 5. Pseudo-NMOS logic family achieves better speed and power performance than other static logic families and hence is preferred for higher integration in digital systems.

F 6. Complementary logic family becomes the mainstream in standard cell library because of better area, speed, and power efficiency, compared to other logic/circuit families.

F 7. Logic effort (g) is an important parameter to estimate path delay of logic functions and is always equal to or greater than 1.

T 8. Delay of any digital circuit can be modeled as a formulation of parasitic and output capacitive loads from both logic gates and interconnects.

T 9. In standard CMOS processes, top metal layers are reserved for large-area routing such as power lines and clocking because of better conductivity than those of bottom metal layers.

T 10. For digital circuit designs with complementary structure, if later input is connected to logic gate input which is close to gate output, better speed can be achieved.

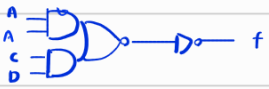
B. [80%] Answer the following 4 questions:

1. [20%] Realize the following logic f=AB+CD by taking into account the following requirements: (assume f is the output with H times of unit-size INV)

(a) Realize this logic function by one compound gate and one inverter, where you need to derive logic effort first and then estimate the delay model (D). [6%]

(b) Realize this logic function by 3 2-input NAND gates, where you need to derive logic effort

(a)



$\bar{A} + \bar{B}C$

(b)

1/2 4/2

4/1 2

4/1 2

$g = \frac{4}{3} = \frac{4}{3}$ $\quad g = \frac{4}{3}$

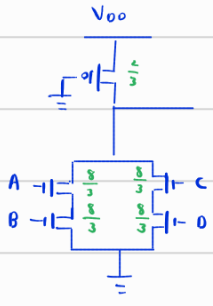
$h = \frac{4}{4} = 1$ $\quad h = \frac{f}{4}$

$f = \frac{4}{3}$ $\quad f = \frac{f}{3}$

$p = \frac{6}{3} = 2$ $\quad p = 2$

$D = \frac{4}{3} \times \frac{f}{3} + 2$

(c)



$g_u = \frac{8}{3}$

$g_d = \frac{8}{9}$

$g_{avg} = \frac{16}{9}$

VS

4 4

4 4 $\quad g = \frac{6}{3} = 2$

2 2

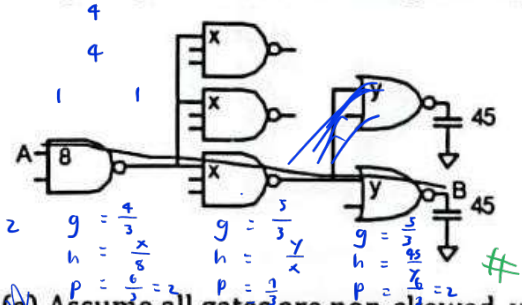
2 2

Yes, speed is improved #

first and then estimate the delay model (D). [6%]

(c) If the compound gate in (a) is replaced by Pseudo N-MOS structure, what's the requirement for correct logic operation? Will speed be improved in terms of logic effort (g)? [8%]

2. [20%] Given the following circuit, you're asked to complete the design:



(a) Assume all gates are non-skewed, you're asked to find the logic efforts (g) and parasitic (P) of these 2 complementary gates, i.e. NAND3, and NOR2. [4%]

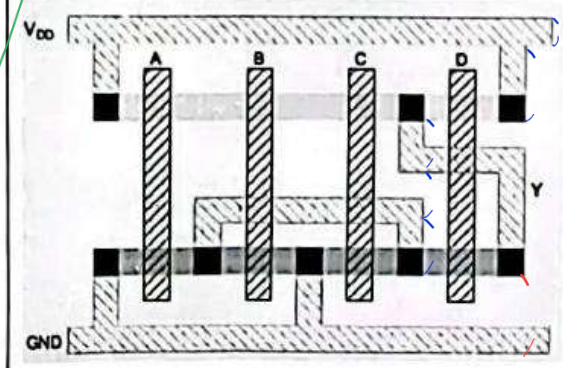
(b) Find the delay model from A to B of this design using path delay (G, B, H, P). [6%]

(c) Identify the P/N transistor widths of both X and Y input nodes. [6%]

(d) Will speed of A->B be improved if top 2 3-inputs are down-sized? [4%]

Yes, cause they will have less C.

3. [20%] A stick diagram for a logic gate is given below.



(a) Draw the circuit diagram and identify the logic function of this cell layout? [8%]

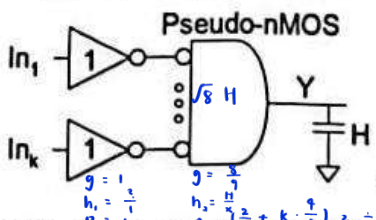
(b) Estimate the size of this layout in metal tracks (X and Y). [4%]

Let the track pitch be λ, then

(c) Explain why latch-up will happen in this layout if well contacts are not placed appropriately. Note you may draw a side view for illustration. [8%]

Without proper contacts there are no low-R path from well to GND/VDD. Voltage fluctuations can turn on the parasitic BJTs.

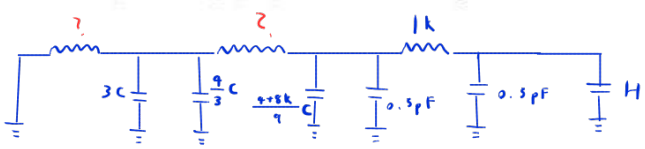
4. [20%] Design a k-input AND gate using Pseudo NMOS as below.



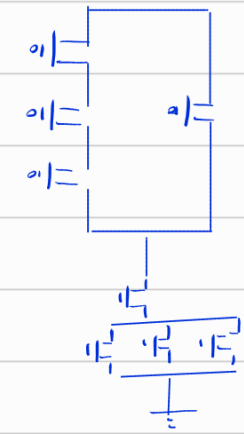
*Equivalent Resistance of NMOS Transistor: 2.5K*um

(a) Estimate the delay driving a fan-out of H. Note that you should find parameters (G,B,H,P) first and then derive the delay model. [12%]

(b) If Y has wire delay of R(1Kohm) and C(1pF) before reaching fan-out of H, re-estimate the delay from (a) by Elmore Delay Model with single-stage π-model. [8%]



3. (a)



P 串 = + 並 = AND

N 串 = AND 並 = +

$(A+B+C)\cdot D$