Introduction to VLSI Design: Final-Term Exam

2021/12/28, Tuesday 15:30-17:30@ED220

Note: this is a closed-book exam allowing one-page A4 summary for reference. You may make assumption whenever necessary in answering the following questions.

A. [20%] True (T) or False (F) for the following 10 statements.

1. Current sequential designs often exploit HDL-based design with edge-triggered elements, where different clock domains are allowed to reduce dynamic power consumption while maintaining acceptable computational performance.
2. Speed of Carry Propagation Adder (CPA) can be improved by adding carry-look-ahead (CLA) circuits to reduce carry propagation delay time, where there is no limit for group bits in current CMOS process.
3. On-chip clock generators based on ring-oscillators are often found in complex chip designs to achieve higher working frequency and less clock jitter.
4. Dynamic power consumption can be reduced by parallelism/pipelining to reduce supply voltage under given computational requirements.
5. Static power consumption can be reduced by transistor-stacking and body-bias to change threshold voltage of transistors in current CMOS process.
6. Guard Rings are often included in high-driving current circuits to avoid latch-up without increasing layout area.
7. Design for testability (DFT) is very important in current chip designs, where built-in-self-test (BIST) is one of the solutions to reduce test time and test cost.
8. Bonding wires from packages to silicon dices will lead to supply voltage drop due to parasitic inductance effect and hence high signal slew rates are often demanded to lower down current variations.
9. Input PAD needs to have ESD protection circuits, which are often realized by diodes and current-limit resistors to limit both input voltage and current ranges.
10. Semi-conductor fabrication technology provided by foundry often offers multi-threshold transistors to reduce leaking current, where low-V_{th} transistors are exploited to realize timing-critical designs.

B. [80%] Answer the following 4 questions:

1. [20%] High-speed multiplier-and-accumulators (MAC) are often requested in many communication and data-driven applications.

(a) For high-speed parallel multiplier design, Booth encoding is considered to reduce the

number of partial products. Explain how this Booth encoding scheme works to reduce the number of partial products by half. [6%]

(b) Explain why carry-save-adder (CSA) can be exploited to enhance parallel multiplier speed. [6%]

(c) Assume a 12X12 parallel multiplier with an accumulator (MAC) is to be designed by the above-mentioned schemes, draw a block diagram of the MAC and then indicate how many levels of CSA's are needed before carry-propagation adder (CPA)? [8%]

2. [20%] Static Random Access Memory (SRAM) is a key storage module in current system-on-chip designs, especially for those related to data-driven applications.

(a) Draw a 6-T SRAM cell and specify the driving capability of these transistors so that read/write operations can be operated accurately. [6%]

(b) Explain why read-operation consumes more power than write-operation in SRAM data access. (Note: you need to consider the peripheral circuits of SRAM) [6%]

(c) Add 3 transistors to the 6-T SRAM cell so that match signal can be generated and used for content addressable memory (CAM). Draw the block diagram of this CAM cell and explain how it works. [8%]

3. [20%] A 1-bit Full-Adder (FA) with inputs (A,B,C) and outputs (S,Co) can be realized by different approaches.

(a) Exploit programmable logic array (PLA) to realize the 1-bit FA. Note that NOR-NOR structure with pseudo-NMOS is the target structure, where dot represents there is a transistor. [8%]

(b) Exploit read-only-memory (ROM) to realize the 1-bit FA with NOR-NOR structure, where dot represents there is a transistor. [8%]

(c) Modify the pseudo-NMOS structure to reduce static power when it is not used or activated. [4%]

4. [20%] Given a logic function, F=AB+CD, you're asked to answer the following:

(a) Apply De Morgan Law to realize the function F with 2-input NAND gates only. [4%]

(b) Find the test vectors to observe SA0 and SA1 at F from (a). [8%]

(c) Find the activity factor α from (a), where the inputs (A,B,C,D) are with the same probability of "0" and "1". [8%]

the number of partial products by half. [6%]

(b) Explain why carry-save-adder (CSA) can be exploited to enhance parallel multiplier speed. [6%]

...with an accumulator (MAC) is to be designed by the

Instead of performing a slow ripple carry addition at every step, CSAs handle the addition of 3 numbers without propagating the carry immediately

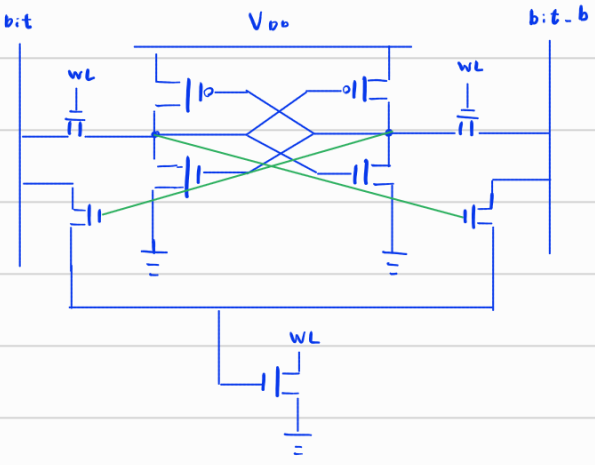
read/write operations can be operated accurately. [6%]

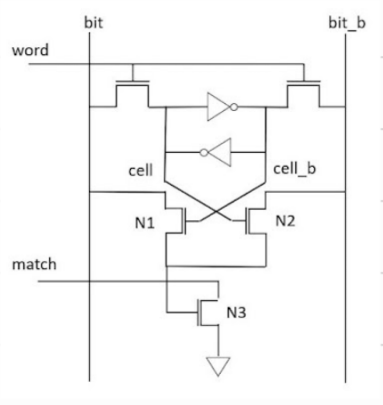
(b) Explain why read-operation consumes more power than write-operation in SRAM data access. (Note: you need to consider the peripheral circuits of SRAM) [6%]

(c) Add 3 transistors to the 6-T SRAM cell so that match signal can be generated and used for content addressable memory (CAM). Draw the block diagram of this CAM cell and explain how it works. [8%]

(b) Before a read operation, the bitlines are precharged to VDD. During the read, one bitline discharges through the SRAM cell based on stored data. Write operations don't require precharging, so they use less power.

(c)





4. [20%] Given a logic function, F=AB+CD, you're asked to answer the following:

(a) Apply De Morgan Law to realize the function F with 2-input NAND gates only. [4%]

(b) Find the test vectors to observe SA0 and SA1 at F from (a). [8%]

(c) Find the activity factor α from (a), where the inputs (A,B,C,D) are with the same probability of "0" and "1". [8%]

0 : 0 0 0 0 | 1 0 0 0
0 0 0 1 | 1 0 0 1
0 0 1 0 | 1 0 1 0
0 1 0 0
0 1 0 1
0 1 1 0

1 : 0 0 | 1 1
0 1 | 1 1
1 0 | 1 1
1 1 | 1 1
1 1 | 0 0
1 1 | 0 1
1 1 | 1 0