

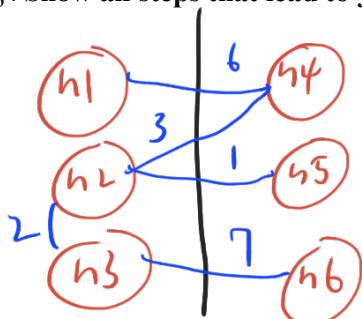
### Practice (Physical Design)

#### 1. (Partitioning)

Let the three tuple  $(u, v, w)$  denote an edge  $(u, v)$  with weight  $w$ . Given a circuit  $C$  of 6 vertices,  $n_1, n_2, \dots, n_6$ , and 5 edges,  $C = \{(n_1, n_4, 6), (n_4, n_2, 3), (n_2, n_3, 2), (n_2, n_5, 1), (n_3, n_6, 7)\}$ , apply the Kernighan-Lin heuristic to find the balanced min-cut for  $C$  with the initial partitions  $\{n_1, n_2, n_3\}$  and  $\{n_4, n_5, n_6\}$ . Show all steps that lead to your answer.

<Initial>

cut=17



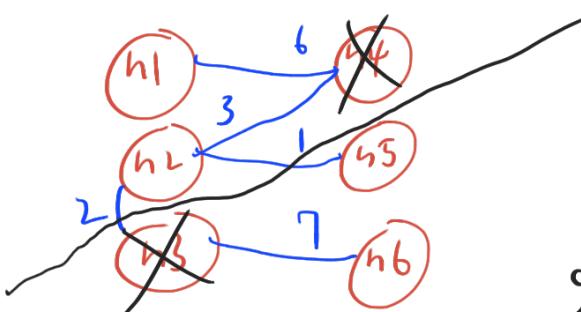
$$\begin{aligned}g_{14} &= 3 \\ g_{15} &= 7 \\ g_{16} &= 13 \\ g_{24} &= 5 \\ g_{25} &= 1\end{aligned}$$

$$\begin{aligned}g_{26} &= 9 \\ g_{34} &= 14 \\ g_{35} &= 6 \\ g_{36} &= -2\end{aligned}$$

$g_{34}$  has max gain

<Step 1>

cut=3

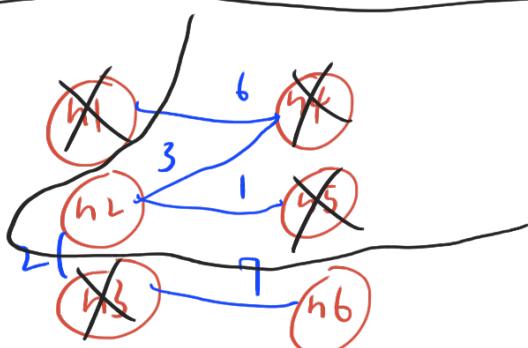


$$\begin{aligned}g_{15} &= -5 \\ g_{16} &= -13 \\ g_{25} &= -5 \\ g_{26} &= -11\end{aligned}$$

$g_{15}$  has maximum gain

<Step 2>

cut=8



$$g_{26} = -9$$

$g_{26}$  has maximum gain

<Step 3> = <Initial>

Ahs.<sup>1</sup>

<Step 1> has min cut : 3  
 $\{1, 2, 4\} \{3, 5, 6\}$

## 2. (Floorplanning)

Given the following Polish expression,  $E = 12H3H45HVV67V$ , where  $H(V)$  represents a horizontal(vertical) cut.

*for every subexpression  $E_i = e_1 \dots e_n$ ,  
 $1 \leq i \leq n-1, \# \text{operands} > \# \text{operators}$*

2:1 3:2 5:3 5:4  
 ↓ ↓ ↓ ↗  
 5:5

(a) Does the above expression have the balloting property? Justify your answer. **No**

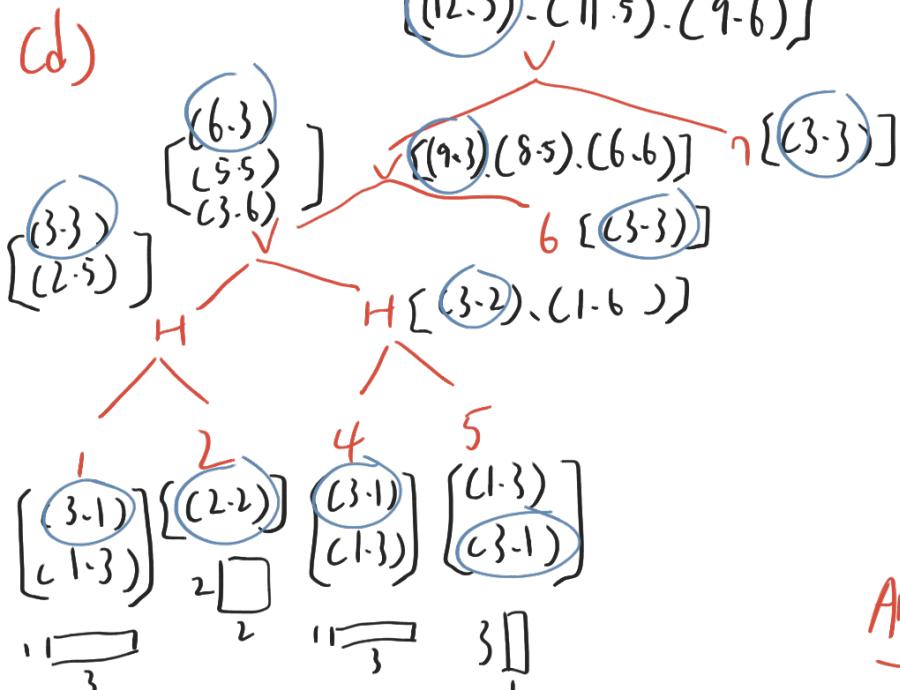
(b) Is  $E$  a normalized Polish expression? If not, exchange an operator and its adjacent operand to transform  $E$  into a normalized Polish expressions  $E'$ . **(b) No,  $E' \Rightarrow 12H3H45HV6V7V$**

(c) Give the slicing tree corresponding to the expression  $E$ , or explain why no such a slicing tree exists. Also, give the slicing tree corresponding to the “resulting” normalized Polish expression  $E'$ , if  $E$  is not a normalized Polish expression.

(d) Assume the modules 1, 2, ..., 7 have the widths and heights indicated in Figure 2. If all modules are rigid and have free orientations, what will be the size of the smallest bounding rectangle corresponding to  $E$  if it is a normalized Polish expression or  $E'$  otherwise? **Show all steps that lead to your answer.**

(c) • No slicing tree of  $E$  exist. We construct a slicing tree by traversing a normalized polish expression in post order, but  $E$  is not a normalized polish expression.

• Slicing tree of  $E'$  exist.



Module No.	Width	Height
1	3	1
2	2	2
3	4	3
4	3	1
5	1	3
6	3	3
7	3	3

Ans: Smallest Area is 36

### 3. (Polish Expression)

Let  $N_k$  be the number of operators in the Polish expression  $E = e_1e_2\dots e_k$ ,  $1 \leq k \leq 2n-1$ . Assume that the  $M_3$  move swaps the operand  $e_i$  with the operator  $e_{i+1}$ ,  $1 \leq i \leq k-1$ . Show that the swap will not violate the balloting property if and only if  $2N_{i+1} < i$ .

$E = e_1e_2\dots e_i$ ,  $E$  is a polish expression whose length is  $i$

Because every character of  $E$  is either operator or operand,  
 we know operand's number is  $i - N_i$

According to Balloting property "# operands > # operators for every subexpression"

We could get  $i - N_i > N_i \Rightarrow i > 2N_i$  ~~X~~

### 4. (Placement)

Consider the AND gate connected to other cells by wires as shown in Figure 3. The weights are specified beside the wires. The locations are indicated in the grid graph, e.g., Vdd is located at (0, 3), and Gnd is located at (3, 0). Please apply the force-directed method to find the zero-force location of the AND gate.

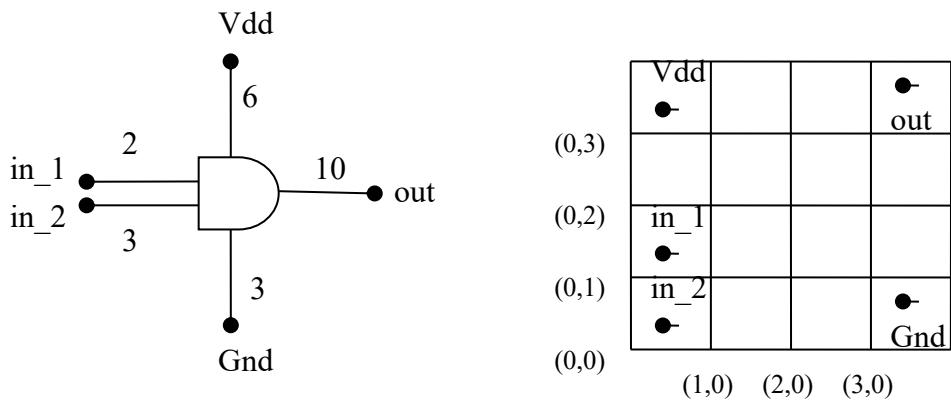


Figure 3. Placement of a AND gate.

$$\hat{x}_i = \frac{\sum_j w_{ij} x_j}{\sum_j w_{ij}} = \frac{6x_0 + 10x_3 + 3x_2 + 3x_0 + 2x_0}{6 + 10 + 3 + 3 + 2} = \frac{39}{24} \Rightarrow 2$$

$$\hat{y}_i = \frac{\sum_j w_{ij} y_j}{\sum_j w_{ij}} = \frac{6x_3 + 10x_3 + 3x_0 + 3x_0 + 2x_1}{6 + 10 + 3 + 3 + 2} = \frac{50}{24} \Rightarrow 3$$

Ans: AND gate's position  $\Rightarrow (2, 3)$

5. (Wire length estimation) For the four pins as shown below, give the wire length estimation for the following methods:

- (a) Semi-perimeter approximation.
- (b) Minimum rectilinear Steiner tree.
- (c) Minimum rectilinear spanning tree.

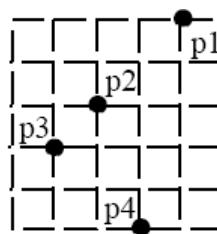
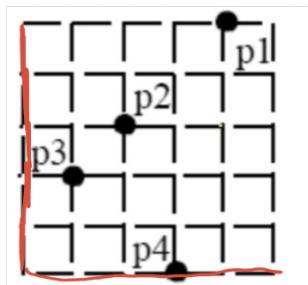


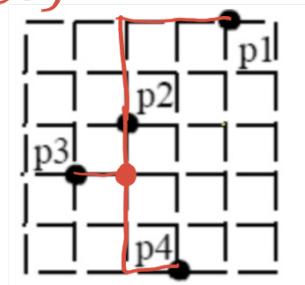
Figure 4. Wirelength estimation

(a)



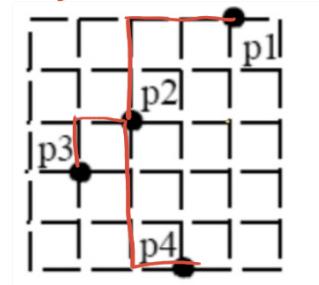
WL: 10

(b)



WL: 9

(c)



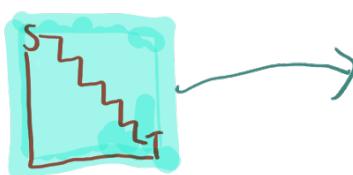
WL: 10

6. (Maze routing) Extend maze routing algorithm shown in class such that it generates a shortest path from source to target (sink) with the minimum number of bends.

Take Lee algorithm for example (此題沒標準答案，論述有道理即可)

<1> Calculating bend's number of every grid when doing wave propagation.  
 ⇒ when doing BFS, we should record minimum bend's number for every grid,  
 if the direction of 2 consecutive propagation is different,  
 bend's number of the grid should be increasing

ex:



5	0	1	2	3	4
0	1	2	3	4	5
0	1	2	3	4	5
0	1	2	3	4	5
0	1	2	3	4	5

bend's number of every grid

<2> At back tracking stage, we not only select the correct order but also select the grid whose bends as few as possible.

7. (Channel routing) Given the instance of the channel routing problem as shown below.

- What is the channel density? Find the set of nets that contribute the channel density.
- Draw the HCG and VCG.
- Can the basic left-edge algorithm apply to this channel routing instance? Route the instance if there exists a feasible routing solution; explain why the algorithm does not apply to this instance, otherwise.
- Can the constrained left-edge algorithm apply to this channel routing instance? Route the instance if there exists a feasible routing solution; explain why the algorithm does not apply to this instance, otherwise.

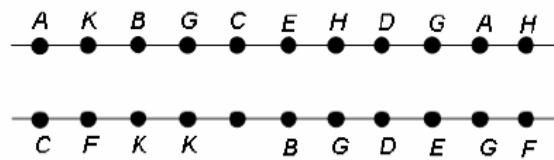
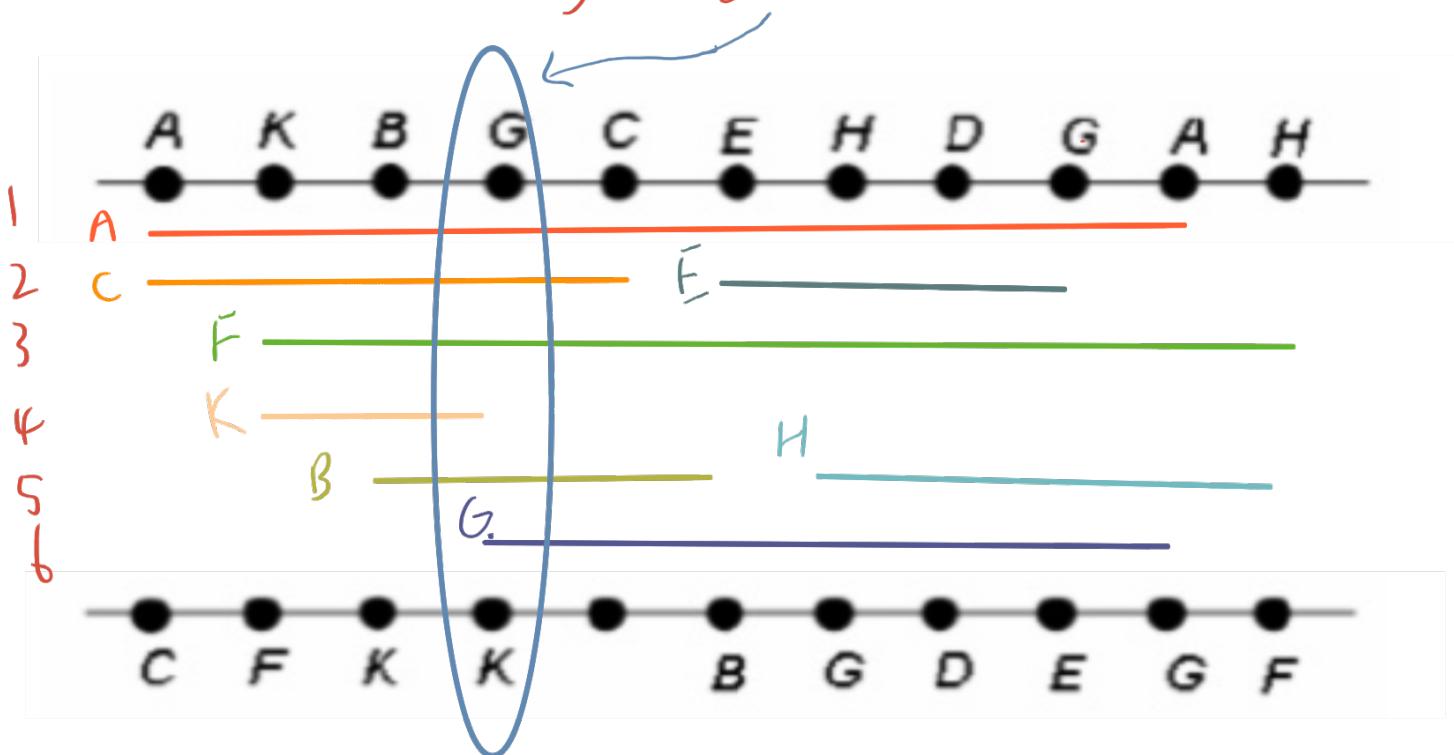
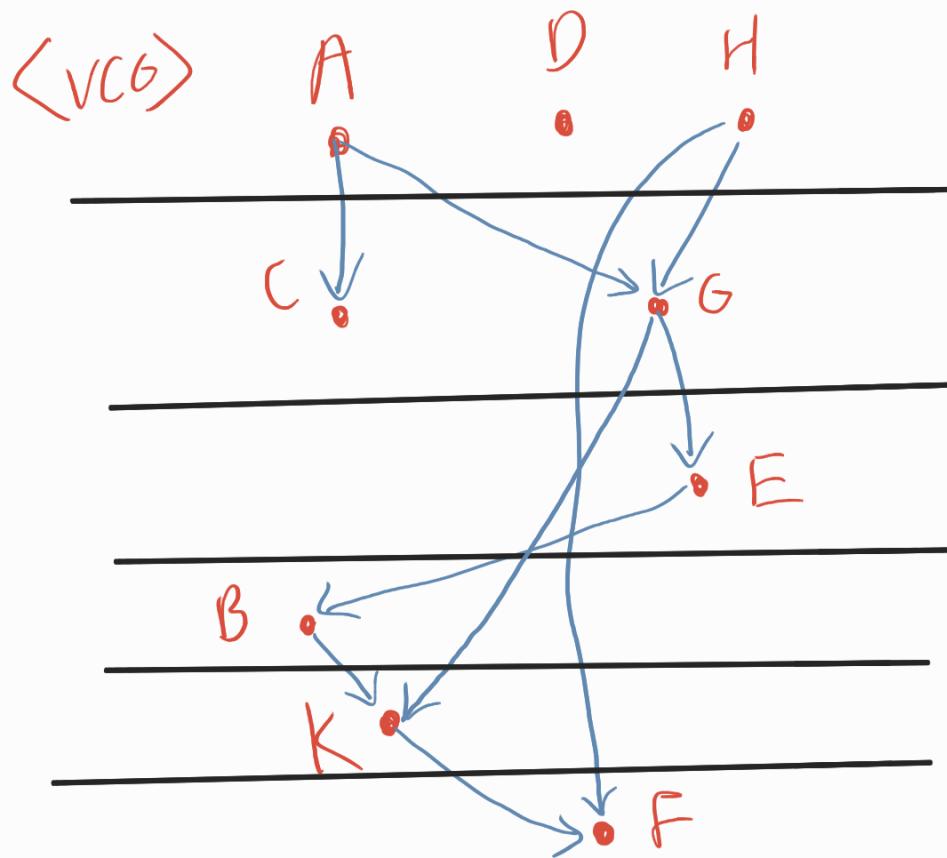
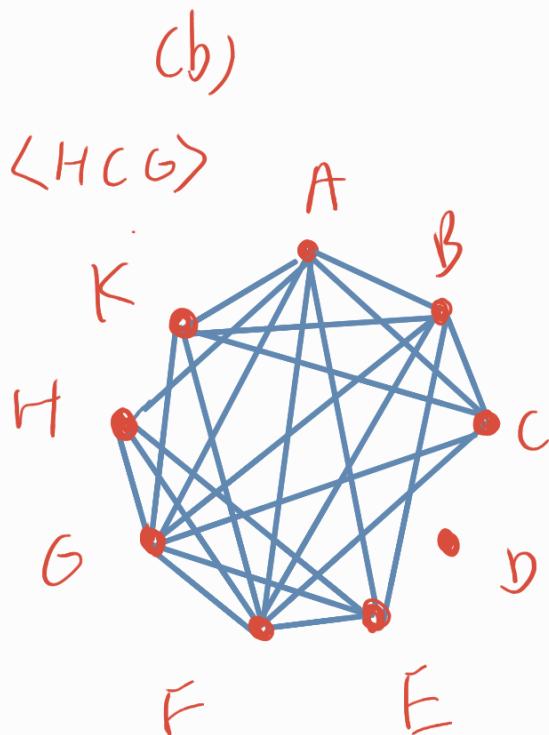


Figure 5. Routing Channel

(a) (channel density is maximum local density, and it is)  
 (also the low bound of horizontal tracks required.)  
 \* channel density: 6  
 channel density set: {A, C, K, B, G, F}





(c) No, basic left-edge only works for the graph which has no VCG.

ex: According to basic left-edge algorithm, first track would be filled with  $\bar{K}$  &  $\bar{E}$ . However, we could find that  $G \rightarrow E$  in the VCG. There is no chance for  $G$  to connect the pin which is above the  $E$ , and this algorithm would fail!

(d) Yes, constrained left-edge could work on this, because there is not cycle in the VCG.



1 A

2 C

3 G

4 E

5 B

6 K

7 F

