Unit 3: Logic Synthesis

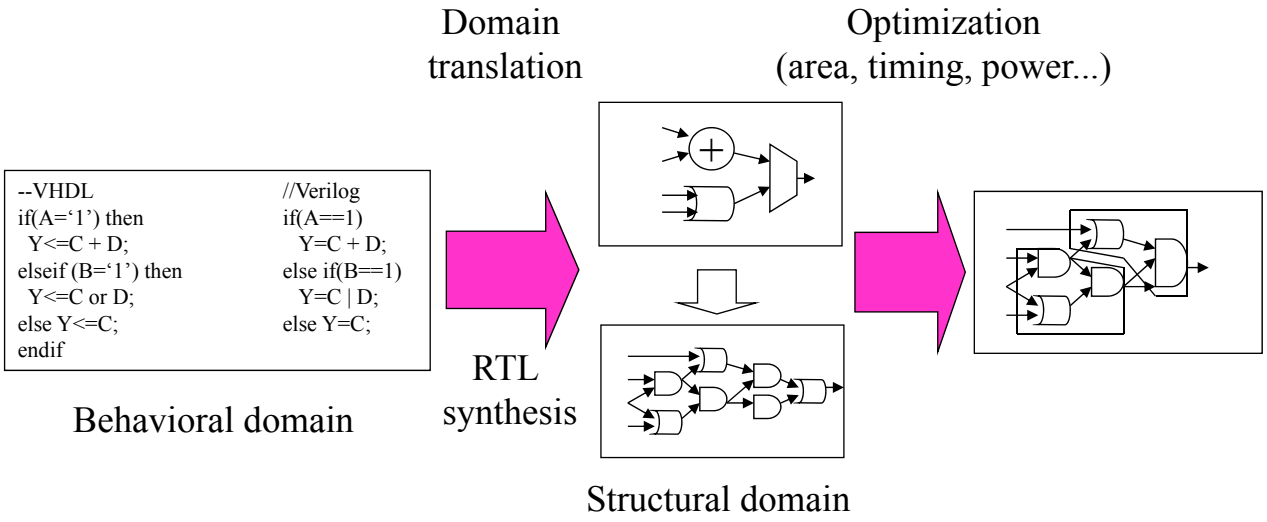
- Course contents
  - Synthesis overview
  - RTL synthesis
  - Logic optimization
  - Technology mapping
  - Timing optimization
  - Synthesis for low power
- Readings
  - Chapter 11
  - Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw-Hill, Inc., 1994.
  - Related papers

HDL Synthesis

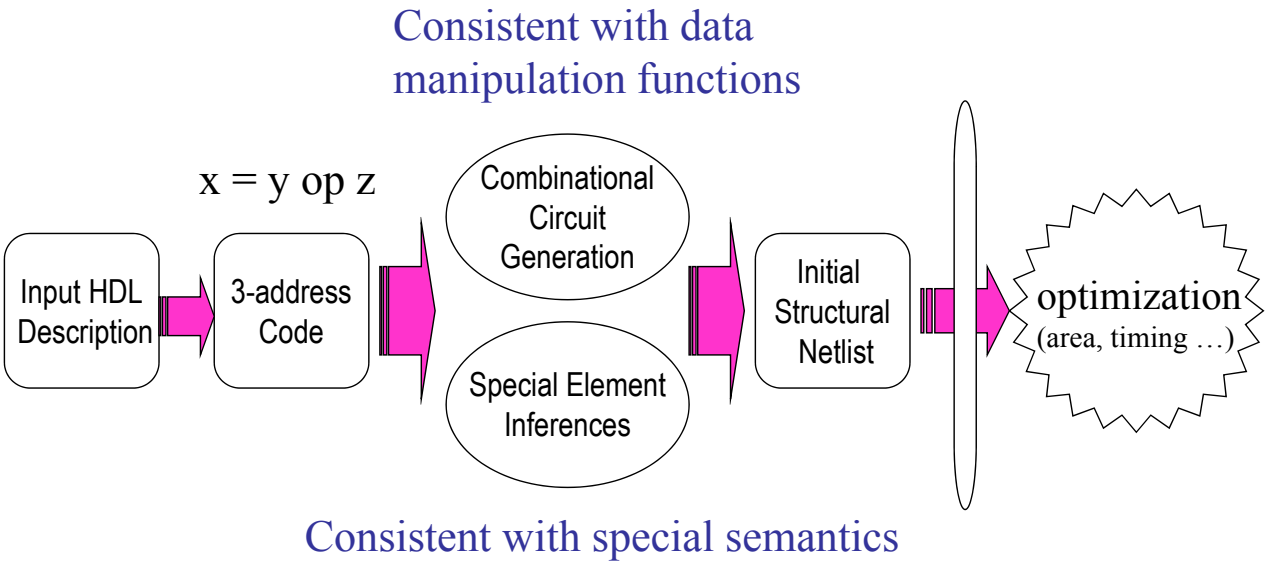
- **Logic synthesis** programs transform Boolean expressions or register-transfer level (RTL) description (in Verilog/VHDL/C) into logic gate networks (netlist) in a particular library.
- Advantages
  - Reduce time to generate netlists
  - Easier to retarget designs from one technology to another
  - Reduce debugging effort
- Requirement
  - **Robust** HDL synthesizers

Synthesis Procedure

Synthesis = Domain Translation + Optimization

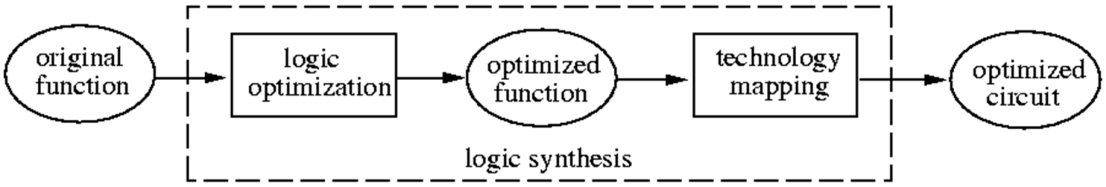


Domain Translation



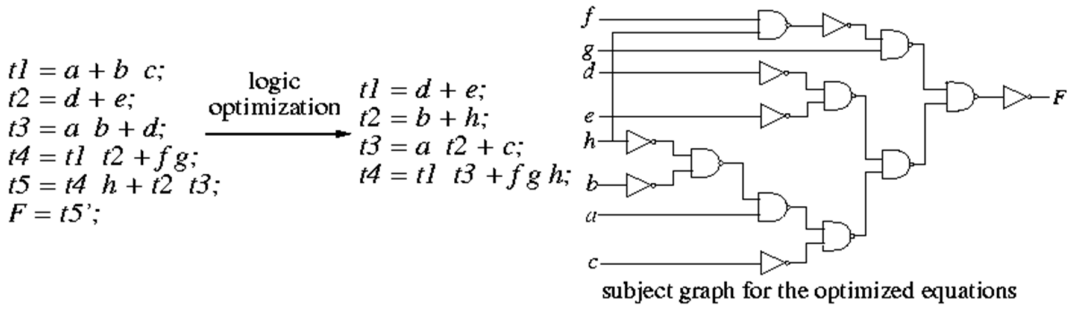
Optimization

- **Technology-independent** optimization: **logic optimization**
  - Work on Boolean expression equivalent
  - Estimate size based on # of literals
  - Use simple delay models
- **Technology-dependent** optimization: **technology mapping/library binding**
  - Map Boolean expressions into a particular cell library
  - May perform some optimizations in addition to simple mapping
  - Use more accurate delay models based on cell structures



Technology-Independent Logic Optimization

- **Two-level:** minimize the # of product terms.
  - $F = \bar{x_1}\bar{x_2}\bar{x_3} + \bar{x_1}\bar{x_2}x_3 + x_1\bar{x_2}\bar{x_3} + x_1\bar{x_2}x_3 + x_1x_2\bar{x_3} \Rightarrow F = \bar{x_2} + x_1\bar{x_3}$.
- **Multi-level:** minimize the #'s of literals, variables.
  - E.g., equations are optimized using a smaller number of literals.

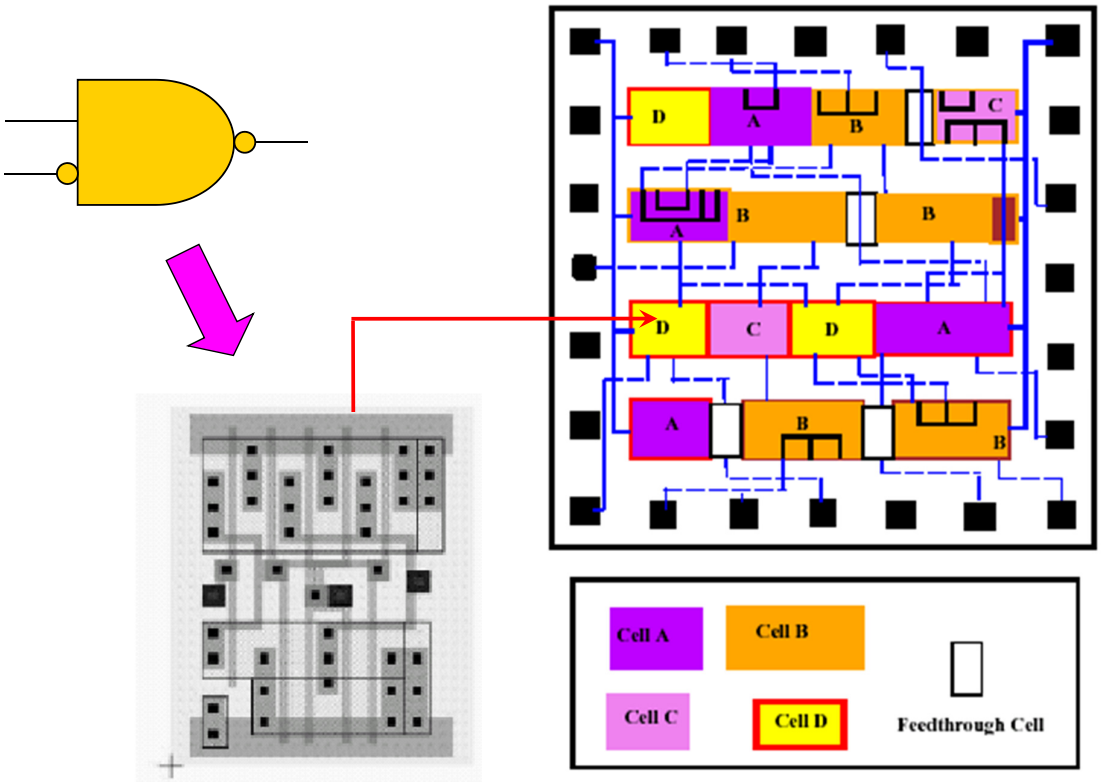


- Methods/CAD tools: The Quine-McCluskey method (exponential-time exact algorithm), Espresso (heuristics for two-level logic), MIS (heuristics for multi-level logic), Synopsys, etc.

Technology Mapping

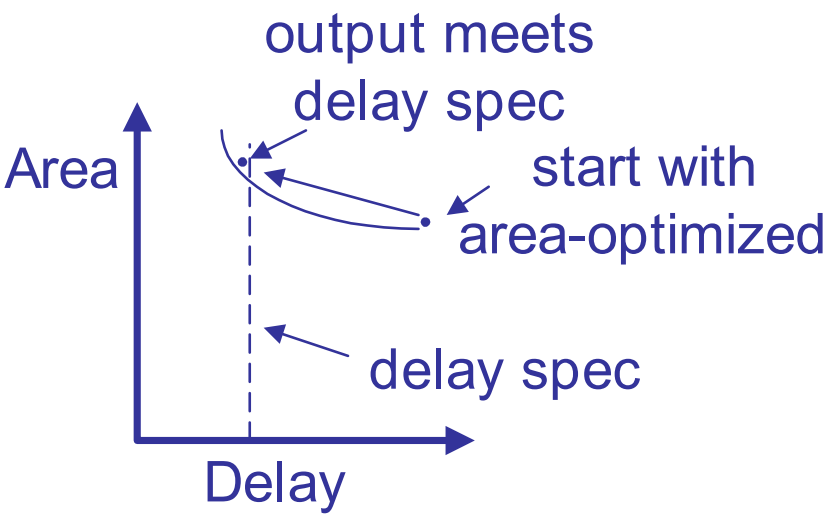
- Goal: translation of a technology independent representation (e.g. Boolean networks) of a circuit into a circuit in a given technology (e.g. standard cells) with optimal cost
- Optimization criteria:
  - Minimum area
  - Minimum delay
  - Meeting specified timing constraints
  - Meeting specified timing constraints with minimum area
- Usage:
  - Technology mapping after technology independent logic optimization
  - Technology translation

Standard Cells for Design Implementation



Timing Optimization

- There is always a trade-off between area and delay
- Optimize timing to meet delay spec. with minimum area



Outline

- Synthesis overview
- RTL synthesis
  - Combinational circuit generation
  - Special element inferences
- Logic optimization
  - Two-level logic optimization
  - Multi-level logic optimization
- Technology mapping
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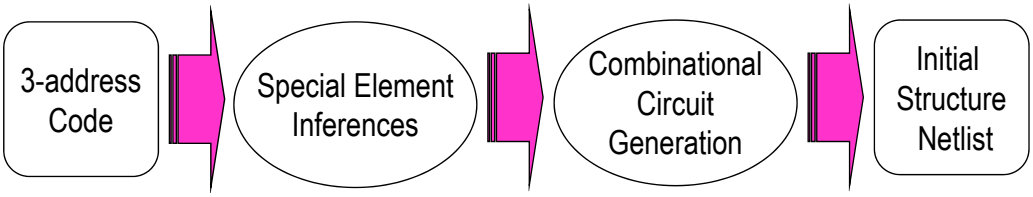
Typical Domain Translation Flow

- Translate original HDL code into 3-address format
- Conduct special element inferences before combinational circuit generation
- Conduct special element inferences process by process (local view)

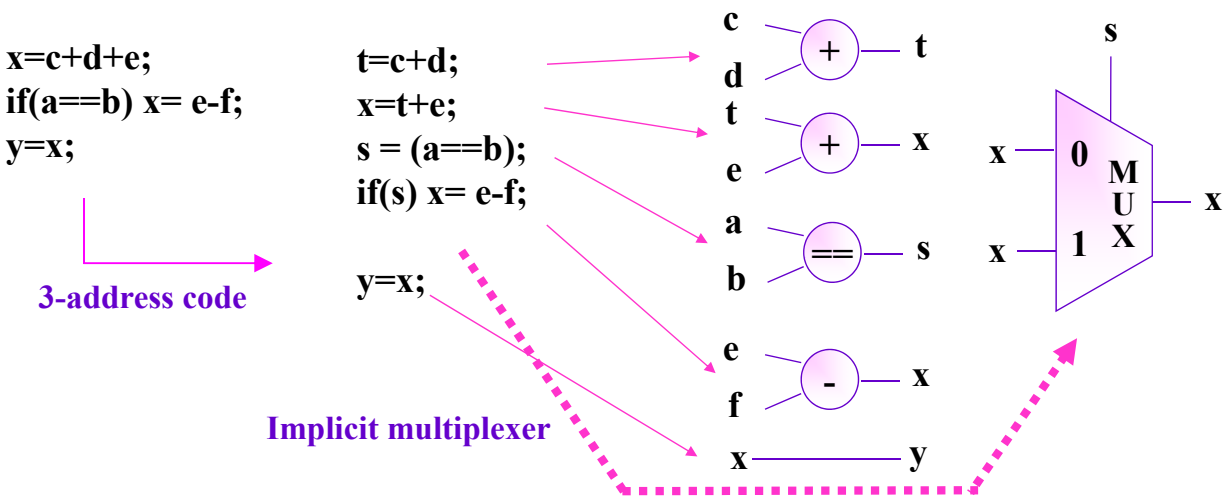


Combinational Circuit Generation

- Functional unit allocation
  - Straightforward mapping with 3-address code
- Interconnection binding
  - Using control/data flow analysis

Functional Unit Allocation

- 3-address code
  - x = y op z in general form
  - Function unit op with inputs y and z and output x



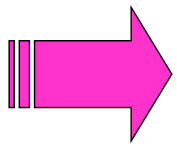
Interconnection Binding

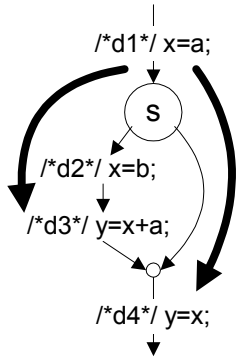
- Need the dependency information among functional units
  - Using **control/data flow analysis**
  - A traditional technique used in compiler design for a variety of code optimizations
  - Statically analyze and compute the set of assignments reaching a particular point in a program

Control/Data Flow Analysis

- Terminology
  - A **definition** of a variable x
    - An assignment assigns a value to the variable x
  - d1 can reach d4 but cannot reach d3
    - d1 is killed by d2 before reaching d3
- A definition can only be affected by those definitions being able to reach it
- Use a set of data flow equations to compute which assignments can reach a target assignment

```
/*d1*/  x = a;
        if(s) begin
/*d2*/      x = b;
/*d3*/      y = x + a;
        end
/*d4*/  y = x;
```





Combinational Circuit Generation: An Example

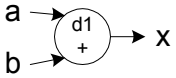
```
always @ (x or a or b or c or d or s)
begin
/*d1*/   x = a + b;
/*d2*/   if ( s ) x = c – d;
/*d3*/   else x = x;
/*d4*/   y = x;
end
```

Input HDL

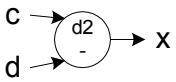
```
always @ (x or a or b or c or d or s)
begin
/*d1*/   x = a + b;
/*d2*/   if ( s ) x = c – d;
/*d3*/   else x = x;
/*d4*/   x = s mux x;
/*d5*/   y = x;
end
```

Modified 3-address code

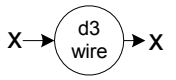
In[d1]={d4, d5} → **computed by control/ data flow analysis**



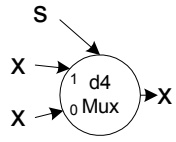
In[d2]={d1, d5}



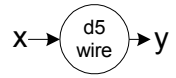
In[d3]={*d1, d5}



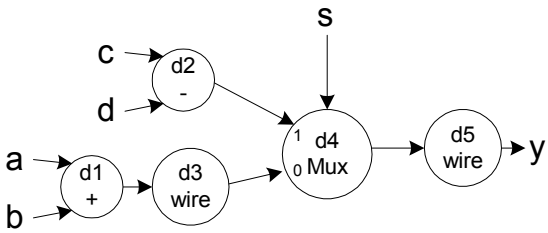
In[d4]={*d2, *d3, d5}



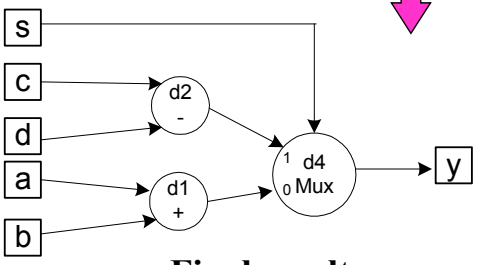
In[d5]={*d4, d5}



Functional unit allocation



Interconnection binding



Final result

Outline

- Synthesis overview
- RTL synthesis
  - Combinational circuit generation
  - Special element inferences
- Logic optimization
  - Two-level logic optimization
  - Multi-level logic optimization
- Technology mapping
- Timing optimization
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Special Element Inferences

- Given a HDL code at RTL, three special elements need to be inferred to keep the special semantics
  - Latch (D-type) inference
  - Flip-Flop (D-type) inference
  - Tri-state buffer inference
- Some simple rules are used in typical approaches

```
reg Q;
always@(D or en)
  if(en) Q = D;
```

Latch inferred!!

```
reg Q;
always@(posedge clk)
   Q = D;
```

Flip-flop inferred!!

```
reg Q;
always@(D or en)
  if(en) Q = D;
  else    Q = 1'bz;
```

Tri-state buffer inferred!!

Preliminaries

- Sequential section
  - Edge triggered always statement
- Combinational section
  - All signals whose values are used in the always statement are included in the sensitivity list

```
reg Q;
always@(posedge clk)
   Q = D;
```

Sequential section
Conduct flip-flop inference

```
reg Q;
always@(in or en)
  if(en) Q=in;
```

Combinational section
Conduct latch inference

Typical Latch Inference

- Conditional assignments are not completely specified
  - Check if the *else-clause* exists
  - Check if all case items exist
- Outputs conditionally assigned in an if-statement are not assigned before entering or after leaving the if-statement

```
always@(D or S)
if(S) Q = D;
```

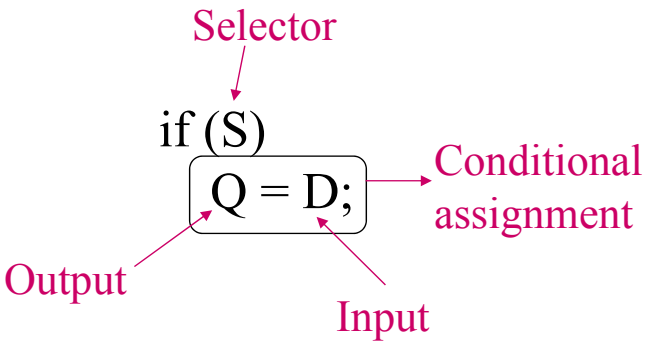
→ Infer latch for Q

```
always@(S or A or B)
begin
Q = A;
if(S) Q = B;
end
```

→ Do not infer latch for Q

Terminology (1/2)

- Conditional assignment
- Selector: S
- Input: D
- Output: Q

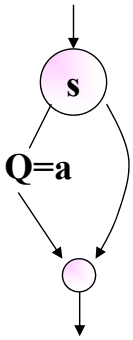


Terminology (2/2)

- A variable Q has a *branch* for a value of selector ***s***
  - The variable Q is assigned a value in a path going through the branch

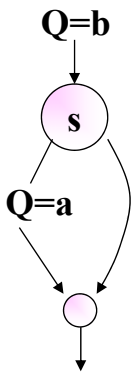
if(s) Q=a;

Q has no branch for the false value of the selector s



Q=b;
if(s) Q=a;

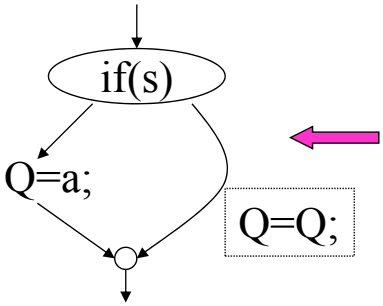
Q has a branch for the false value of the selector s



Rules of Latch Inference (1/2)

- Condition 1: There is no branch associated with the output of a conditional assignment for a value of the selector
  - Output depends on its previous value implicitly

```
always@(s or a)
if(s) Q=a;
```

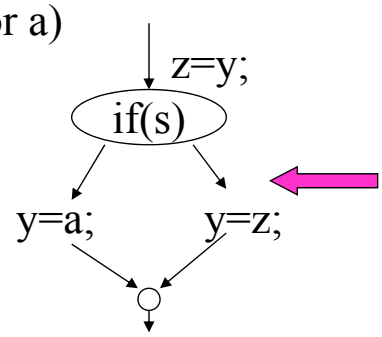


Q depends on its previous value at this branch

Rules of Latch Inference (2/2)

- Condition 2: The output value of a conditional assignment depends on its previous value explicitly

```
always@(s or z or y or a)
begin
  z = y;
  if(s) y=a;
  else y=z;
end
```



y depends on its previous value at this branch via the assignment z=y;

Terminology

- Clocked statement: edge-triggered always statement
  - Simple clocked statement

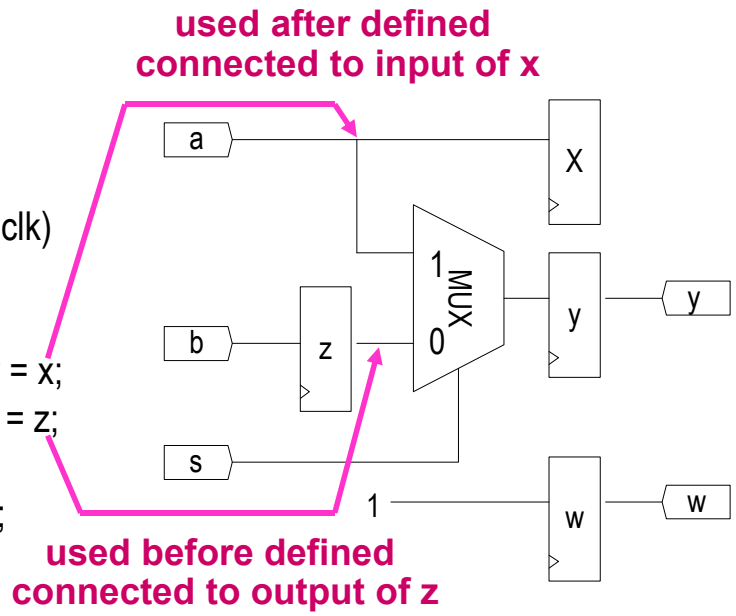
    e.g., always @ (posedge clock)
  - Complex clocked statement

    e.g., always @ (posedge clock or **posedge** reset)
- Flip-flop inference must be conducted only when synthesizing the **clocked statements**

Infer FF for Simple Clocked Statements (1/2)

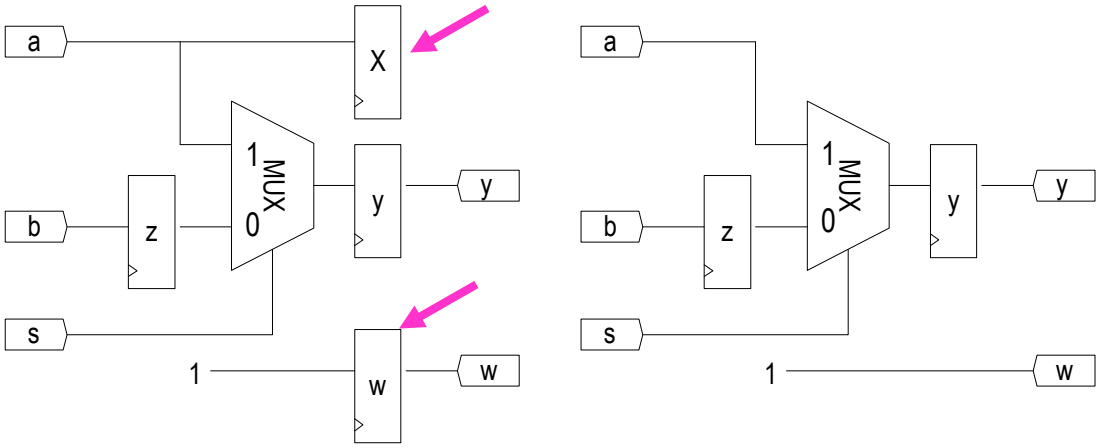
- Infer a flip-flop for **each variable** being assigned in the simple clocked statement

```
input a, b, s, clk;
output y, w;
reg x, w, y, z;
always @ (posedge clk)
begin
/* d1 */      x = a;
/* d2 */      if ( s )   y = x;
/* d3 */      else     y = z;
/* d4 */      z = b;
/* d5 */      w = 1'b1;
end
```



Infer FF for Simple Clocked Statements (2/2)

- Two post-processes
  - Propagating constants
  - Removing the flip-flops without fanouts



Infer FF for Complex Clocked Statements

- The edge-triggered signal not used in the following operations is chosen as the clock signal
- The usage of asynchronous control pins requires the following syntactic template
  - An if-statement immediately follows the always statement
  - Each variable in the event list except the *clock signal* must be a selective signal of the if-statements
  - Assignments in the blocks B1 and B2 must be constant assignments (e.g., x=1, etc.)

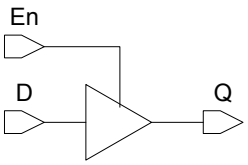
always @ (**posedge** clock or **posedge** reset or **negedge** set)

if(reset) begin **B1** end
else if (!set) begin **B2** end
else begin **B3** end

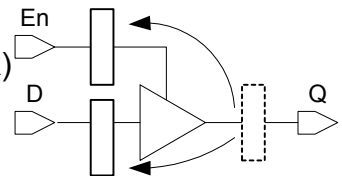
Typical Tri-State Buffer Inference (1/2)

- If a data object Q is assigned a high impedance value 'Z' in a multi-way branch statement (if, case, ?:)
  - Associated Q with a tri-state buffer
- If Q associated with a tri-state buffer has also a memory attribute (latch, flip-flop)
  - Have the **Hi-Z propagation problem**
    - Real hardware cannot propagate Hi-Z value
  - Require two memory elements for the control and the data inputs of tri-state buffer

```
reg Q;
always @ (En or D)
if(En) Q = D;
else Q = 1'bz;
```




```
reg Q;
always @ (posedge clk)
if(En) Q = D;
else Q = 1'bz;
```

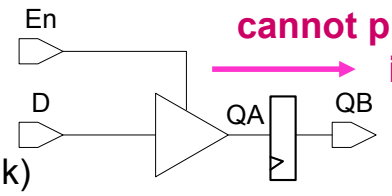


Typical Tri-State Buffer Inference (2/2)

- It may suffer from mismatches between synthesis and simulation
  - Process by process
  - May incur the Hi-Z propagation problem

```
reg QA, QB;
always @ (En or D)
if(En) QA = D;
else QA = 1'bz;

always @ (posedge clk)
QB = QA;
```



cannot propagate Hi-Z in real hardware

assignment can pass Hi-Z to QB in simulation

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Two-Level Logic Optimization

- Two-level logic optimization
  - Key technique in logic optimization
  - Many efficient algorithms to find a near minimal representation in a practical amount of time
  - In commercial use for several years
  - Minimization criteria: **number of product terms**
- Example: $F = XYZ + X\bar{Y}\bar{Z} + X\bar{Y}Z + \bar{X}YZ + XY\bar{Y}Z$

$$\Downarrow$$

$$F = X\bar{Y} + YZ$$

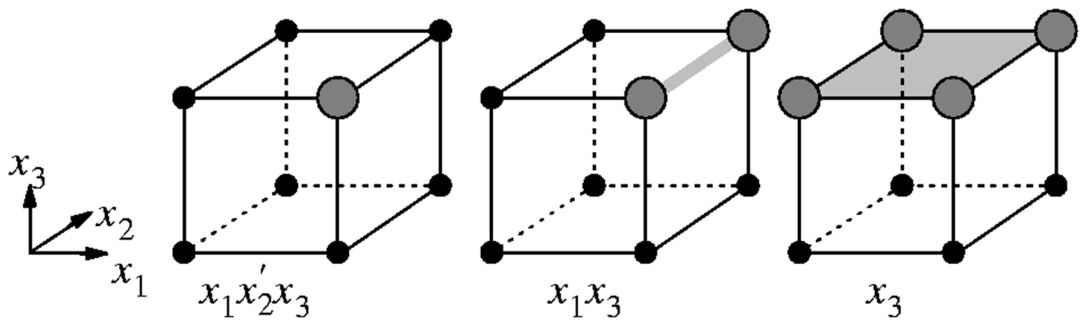
- Approaches to simplify logic functions:
  - Karnaugh maps [Kar53]
  - Quine-McCluskey [McC56]

Boolean Functions

- $B = \{0,1\}$, $Y = \{0,1,D\}$
- A Boolean function f: $B^m \rightarrow Y^n$
  - $f = \bar{x}_1 \bar{x}_2 + \bar{x}_1 \bar{x}_3 + \bar{x}_2 x_3 + x_1 x_2 + x_2 \bar{x}_3 + x_1 x_3$
- Input variables: x_1, x_2, …
- The value of the output partitions B^m into three sets
  - the on-set
  - the off-set
  - the dc-set (don't-care set)

Minterms and Cubes

- A minterm is a product of all input variables or their negations.
  - A minterm corresponds to a single point in B^n.
- A cube is a product of the input variables or their negations.
  - The fewer the number of variables in the product, the bigger the space covered by the cube.

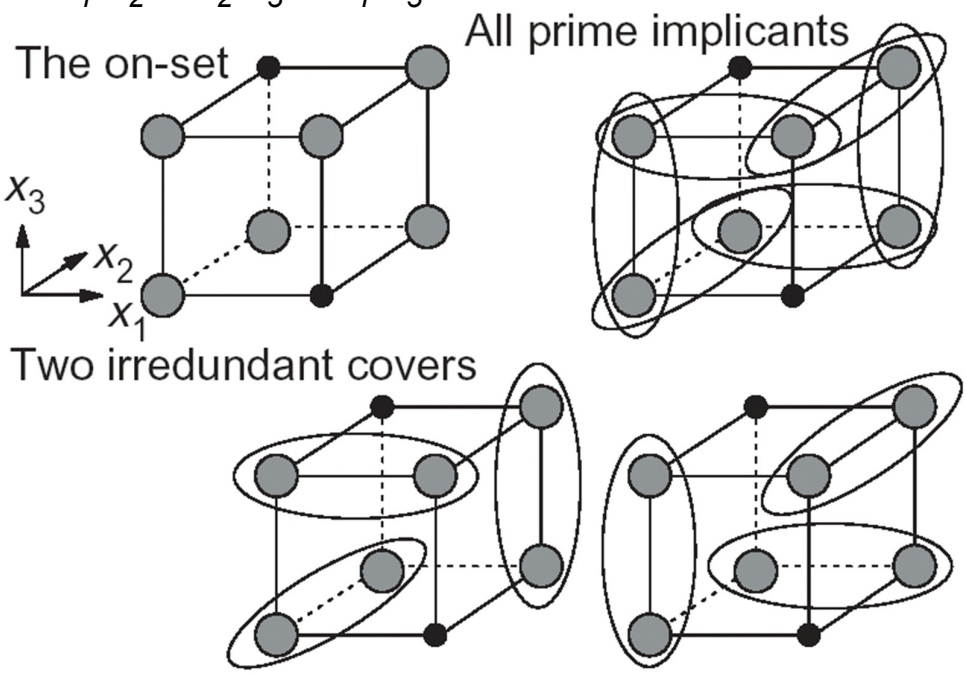


Implicant and Cover

- An **implicant** is a cube whose points are either in the on-set or the dc-set.
- A **prime implicant** is an implicant that is not included in any other implicant.
- A set of prime implicants that together cover all points in the on-set (and some or all points of the dc-set) is called a prime cover.
- A prime cover is irredundant when none of its prime implicants can be removed from the cover.
- An irredundant prime cover is minimal when the cover has the minimal number of prime implicants.

Cover Examples

- $f = \overline{x_1}\,\overline{x_3} + \overline{x_2}\,x_3 + x_1\,x_2$
- $f = \overline{x_1}\,\overline{x_2} + x_2\,\overline{x_3} + x_1\,x_3$



The Quine-McCluskey Algorithm

- Theorem:[Quine,McCluskey] There exists a minimum cover for F that is prime
  - Need to look just at primes (reduces the search space)
- Classical methods: two-step process
  1. Generation of all prime implicants (of the union of the on-set and dc-set)
  2. Extraction of a minimum cover (covering problem)
- Exponential-time exact algorithm, huge amounts of memory!
- Other methods do not first enumerate all prime implicants; they use an implicit representation by means of ROBDDs.

Primary Implicant Generation (1/5)

cd \ ab	00	01	11	10
00	X	1	0	1
01	0	1	1	1
11	0	X	X	0
10	0	1	0	1

a, b, c, d

Primary Implicant Generation (2/5)

	Implication Table	
	Column I	
zero "1"	0000	
one "1"	0100 1000	
two "1"	0101 0110 1001 1010	
three "1"	0111 1101	
four "1"	1111	

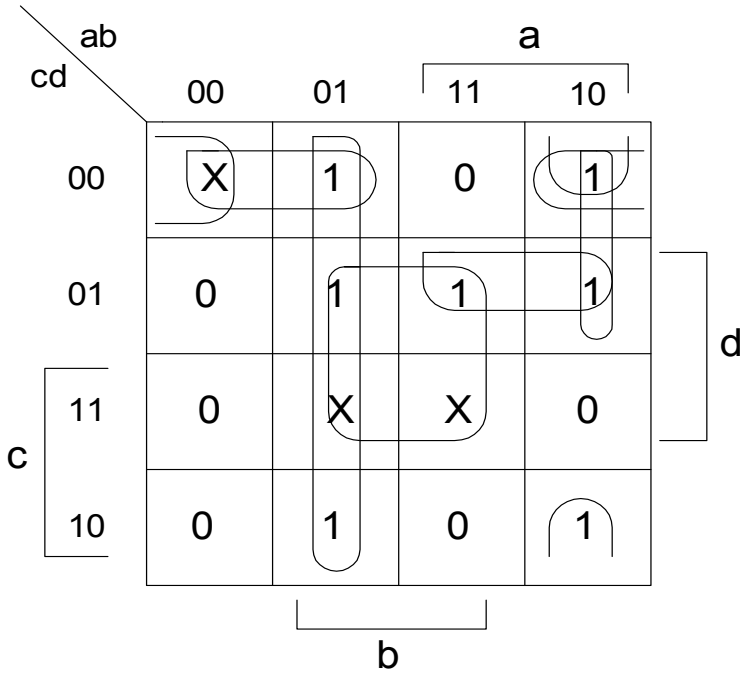
Primary Implicant Generation (3/5)

Implication Table		
Column I	Column II	
0000 |	0-00 -000	
0100 |		
1000 |	010- 01-0	
0101 |	100-	
0110 |	10-0	
1001 |		
1010 |	01-1 -101	
0111 |	011-	
1101 |	1-01	
1111 |	-111 11-1	

Primary Implicant Generation (4/5)

Implication Table		
Column I	Column II	Column III
0000 |	0-00 *	01-- *
	-000 *	
0100 |		-1-1 *
1000 |	010- |	
	01-0 |	
0101 |	100- *	
0110 |	10-0 *	
1001 |		
1010 |	01-1 |	
	-101 |	
0111 |	011- |	
1101 |	1-01 *	
1111 |	-111 |	
	11-1 |	

Primary Implicant Generation (5/5)



Prime Implicants:

0-00 = a'c'd'
100- = ab'c'
1-01 = ac'd
-1-1 = bd
-000 = b'c'd'
10-0 = ab'd'
01-- = a'b

Column Covering (1/4)

	4	5	6	8	9	10	13
0,4 (0-00)	X						
0,8 (-000)				X			
8,9 (100-)				X	X		
8,10 (10-0)				X		X	
9,13 (1-01)					X		X
4,5,6,7 (01- -)	X	X	X				
5,7,13,15 (-1-1)		X					X

rows = prime implicants
columns = ON-set elements
place an "X" if ON-set element
is covered by the prime implicant

Column Covering (2/4)

	4	5	6	8	9	10	13
0,4 (0-00)	X						
0,8 (-000)				X			
8,9 (100-)				X	X		
8,10 (10-0)				X		X	
9,13 (1-01)					X		X
4,5,6,7 (01- -)	X	X	X				
5,7,13,15 (-1-1)		X					X

If column has a single X, then the implicant associated with the row is essential. It must appear in minimum cover

Column Covering (3/4)

	4	5	6	8	9	10	13
0,4 (0-00)	X						
0,8 (-000)				X			
8,9 (100-)				X	X		
8,10 (10-0)				X		X	
9,13 (1-01)					X		X
4,5,6,7 (01- -)	X	X	X				
5,7,13,15 (-1-1)		X					X

Eliminate all columns covered by essential primes

Column Covering (4/4)

	4	5	6	8	9	10	13
0,4 (0-00)	X						
0,8 (-000)				X			
8,9 (100-)				X	X		
8,10 (10-0)				X		X	
9,13 (1-01)					X		X
4,5,6,7 (01- -)	X	X	X				
5,7,13,15 (-1-1)		X					X

Find minimum set of rows that cover the remaining columns

f = ab'd' + ac'd + a'b

Petrick's Method

- Solve the **satisfiability** problem of the following function

P = (P1+P6)(P6+P7)P6(P2+P3+P4)(P3+P5)P4(P5+P7)=1

		4	5	6	8	9	10	13
P1	0,4 (0-00)	×						
P2	0,8 (-000)				×			
P3	8,9 (100-)				×	×		
P4	8,10 (10-0)				×		×	
P5	9,13 (1-01)					×		×
P6	4,5,6,7 (01- -)	×	×	×				
P7	5,7,13,15 (-1-1)		×					×

- Each term represents a corresponding column
- Each column must be chosen at least once
- All columns must be covered

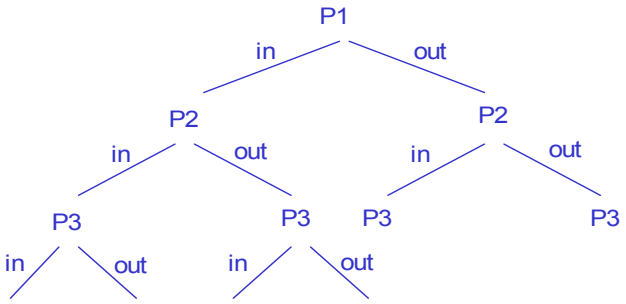
ROBDDs and Satisfiability

- A Boolean function is **satisfiable** if an assignment to its variables exists for which the function becomes '1'
- Any Boolean function whose ROBDD is unequal to '0' is satisfiable.
- Suppose that choosing a Boolean variable x_i to be '1' costs c_i. Then, the **minimum-cost satisfiability** problem asks to minimize: $\sum_{i=1}^{n} c_i \mu(x_i)$

  where $\mu(x_i)$ = 1 when x_i = '1' and $\mu(x_i)$ = 0 when x_i = '0'.
- Solving minimum-cost satisfiability amounts to computing the shortest path in an ROBDD, which can be solved in linear time.
  - Weights: $w(v, \eta(v)) = c_i$, $w(v, \lambda(v)) = 0$, variable $x_i = \phi(v)$.

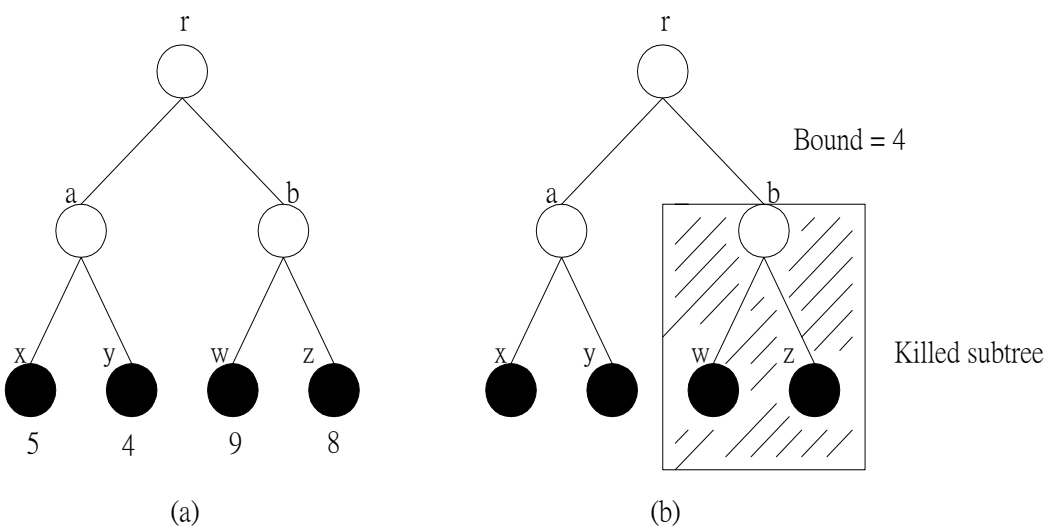
Brute Force Technique

- Brute force technique: Consider all possible elements



- Complete branching tree has $2^{|P|}$ leaves!!
  - Need to prune it
- Complexity reduction
  - Essential primes can be included right away
    - If there is a row with a singleton "1" for the column
  - Keep track of best solution seen so far
    - Classic ***branch and bound***

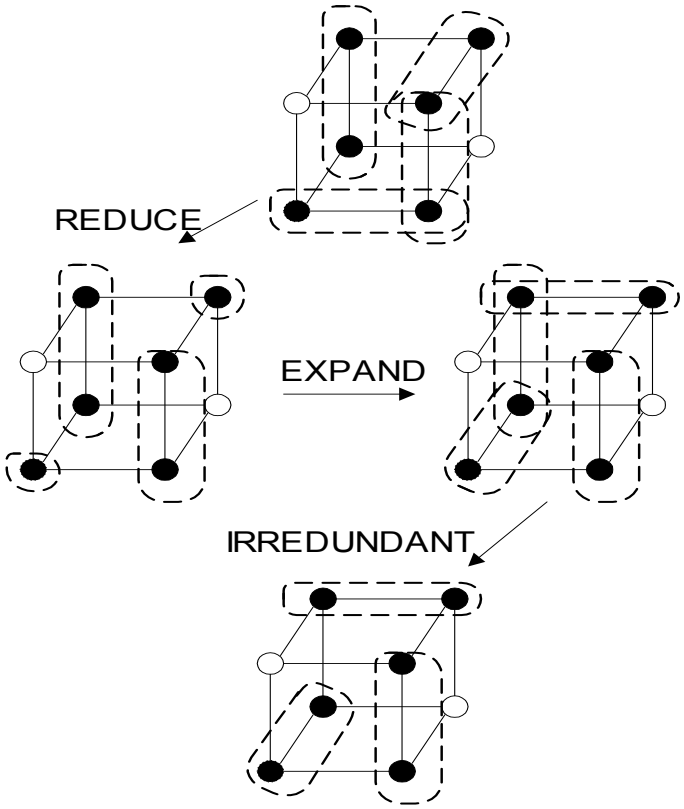
Branch and Bound Algorithm



Heuristic Optimization

- Generation of ***all*** prime implicants is impractical
  - The number of prime implicants for functions with *n* variables is in the order of $3^n/n$
- Finding an *exact* minimum cover is NP-hard
  - Cannot be finished in polynomial time
- Heuristic method: avoid generation of all prime implicants
- Procedure
  - A minterm of ON(f) is selected, and expanded until it becomes a prime implicant
  - The prime implicant is put in the final cover, and all minterms covered by this prime implicant are removed
  - Iterated until all minterms of the ON(f) are covered
- "ESPRESSO" developed by UC Berkeley
  - The kernel of synthesis tools

ESPRESSO - Illustrated



Outline

- Synthesis overview
- RTL synthesis
  - Combinational circuit generation
  - Special element inferences
- Logic optimization
  - Two-level logic optimization
  - Multi-level logic optimization
- Technology mapping
- Timing optimization
- Synthesis for low power

Multi-Level Logic Optimization

- Translate a combinational circuit to meet performance or area constraints
  - Two-level minimization
  - Common factors or kernel extraction
  - Common expression resubsitution
- In commercial use for several years
- Example:

$$f1 = abcd + abce + \bar{a}\bar{b}c\bar{d} + \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}c + cdf + a\bar{b}\bar{c}\bar{d}\bar{e} + a\bar{b}\bar{c}d\bar{f}$$

$$f2 = bdg + \bar{b}dfg + \bar{b}\bar{d}g + b\bar{d}eg$$

$$\Rightarrow$$

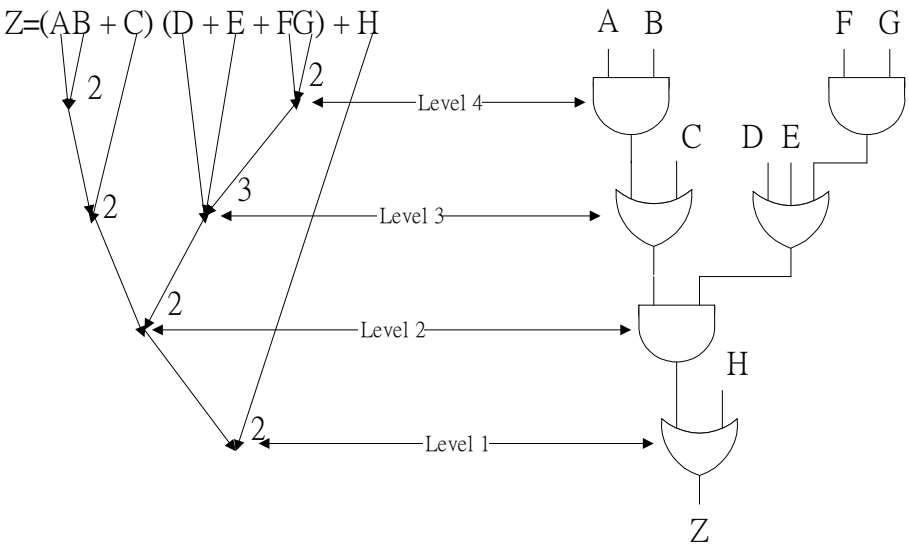
$$f1 = c(\bar{a} + x) + a\bar{c}\bar{x}$$

$$f2 = gx$$

$$x = d(b + f) + \bar{d}(\bar{b} + e)$$

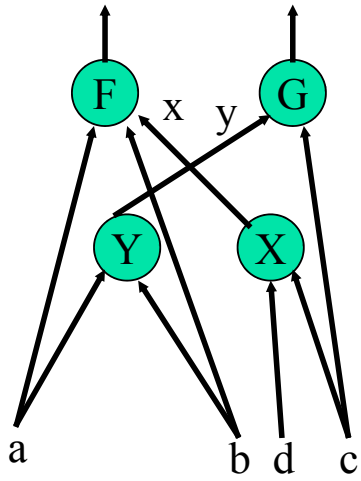
Multi-Level Logic

- Multi-level logic:
  - A set of logic equations with no cyclic dependencies
- Example: Z = (AB + C)(D + E + FG) + H
  - 4-level, 6 gates, 13 gate inputs



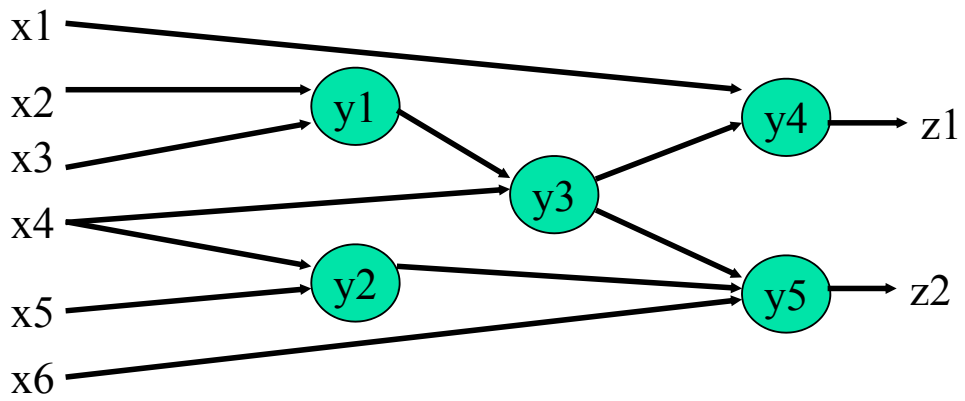
Boolean Network

- Directed acyclic graph (DAG)
- Each source node is a primary input
- Each sink node is a primary output
- Each internal node represents an equation
- Arcs represent variable dependencies



fanin of y : a, b
fanout of x : F

Boolean Network : An Example



$y1 = f_1(x2, x3) = x2' + x3'$

$y2 = f_2(x4, x5) = x4' + x5'$

$y3 = f_3(x4, y1) = x4'y1'$

$y4 = f_4(x1, y3) = x1 + y3'$

$y5 = f_5(x6, y2, y3) = x6y2 + x6'y3'$

Multi-Level v.s. Two-Level

- Two-level:
  - Often used in control logic design

    $f_1 = x_1x_2 + x_1x_3 + x_1x_4$

    $f_2 = x_1'x_2 + x_1'x_3 + x_1x_4$
  - Only x_1x_4 shared
  - Sharing restricted to common cube
- Multi-level:
  - Datapath or control logic design
  - Can share $x_2 + x_3$ between the two expressions
  - Can use complex gates

    $g_1 = x_2 + x_3$

    $g_2 = x_2x_4$

    $f_1 = x_1y_1 + y_2$

    $f_2 = x_1'y_1 + y_2$

    (y_i is the output of gate g_i)

Multi-Level Logic Optimization

- Technology independent
- Decomposition/Restructuring
  - Algebraic
  - Functional
- Node optimization
  - Two-level logic optimization techniques are used

Decomposition / Restructuring

- Goal : given initial network, find best network
- Two problems:
  - Find good **common subfunctions**
  - How to perform **division**
- Example:

  $f_1 = abcd + abce + ab'cd' + ab'c'd' + a'c + cdf + abc'd'e' + ab'c'df'$

  $f_2 = bdg + b'dfg + b'd'g + bd'eg$

  minimize (in sum-of-products form):

  $f_1 = bcd + bce + b'd' + b'f + a'c + abc'd'e' + ab'c'df'$

  $f_2 = bdg + dfg + b'd'g + d'eg$

  decompose:

  $f_1 = c(a' + x) + ac'x'$ $x = d(b + d) + d'(b' + e)$

  $f_2 = gx$

Basic Operations (1/2)

1. decomposition
(single function)

$f = abc + abd + (ac)'d' + b'c'd'$

$f = xy + (xy)'$
$x = ab$
$y = c + d$

2. extraction
(multiple functions)

$f = (az + bz')cd + e$
$g = (az + bz')e'$
$h = cde$

$f = xy + e$
$g = xe'$
$h = ye$
$x = az + bz'$
$y = cd$

Basic Operations (2/2)

3. factoring
(series-parallel decomposition)

$f = ac + ad + bc + bd + e$

$f = (a + b)(c + d) + e$

4. substitution
(with complement)

$g = a + b$
$f = a + bc + b'c'$

$f = g(a + c) + g'c'$

5. elimination

$f = ga + g'b$
$g = c + d$

$f = ac + ad + bc'd'$
$g = c + d$

"Division" plays a key role !!

Division

- Division: p is a Boolean divisor of f if $q \neq \phi$ and r exist such that $f = pq + r$
  - p is said to be a factor of f if in addition $r = \phi$:

    $$f = pq$$
  - q is called the **quotient**
  - r is called the **remainder**
  - q and r are **not unique**
- ***Weak division***: the unique algebraic division such that r has as few cubes as possible
  - The quotient q resulting from weak division is denoted by f / p (it is ***unique***)

Weak Division Algorithm (1/2)

Weak_div(f, p):

U = Set $\{u_j\}$ of cubes in f with literals not in p deleted

V = Set $\{v_j\}$ of cubes in f with literals in p deleted

/* note that $u_j v_j$ is the j-th cube of f */

$V^i = \{v_j \in V : u_j = p_i\}$

$q = \cap V^i$

$r = f - pq$

return(q, r)

Weak Division Algorithm (2/2)

- Example

common expressions

$f = acg + adg + ae + bc + bd + be + a'b$

$p = ag + b$

$U = ag + ag + a + b + b + b + b$

$V = c + d + e + c + d + e + a'$

$V^{ag} = c + d$

$V^{b} = c + d + e + a'$

$q = c + d = f/p$

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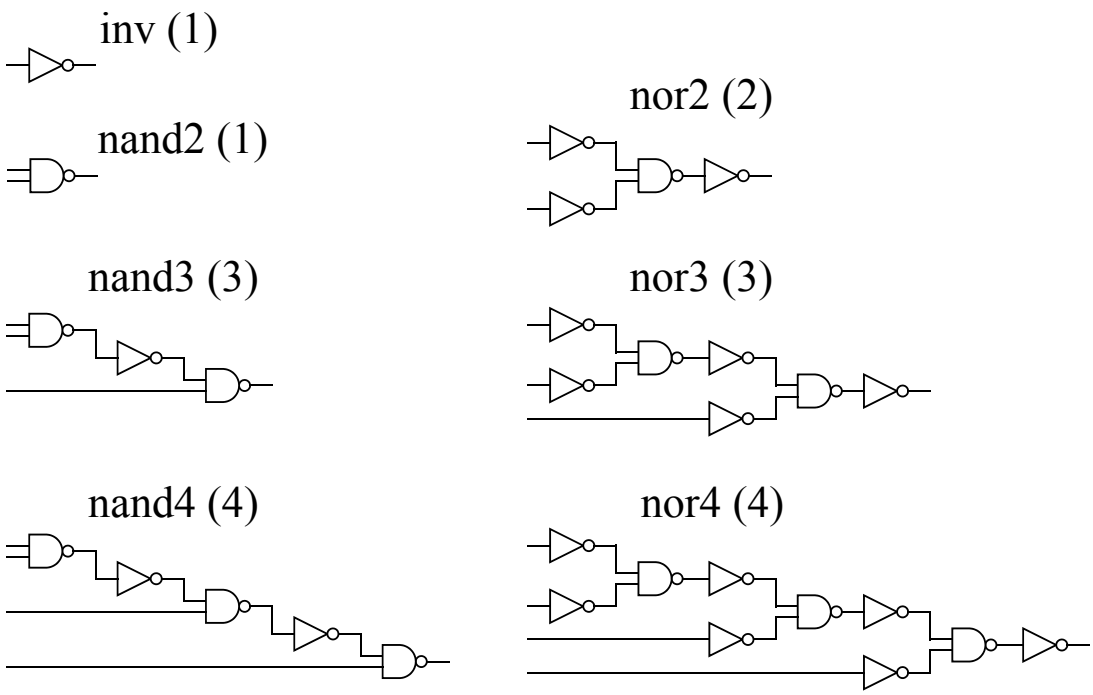
Technology Mapping

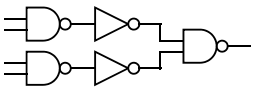
- General approach:
  - Choose base function set for canonical representation
    - Ex: 2-input NAND and Inverter
  - Represent optimized network using base functions
    - Subject graph
  - Represent library cells using base functions
    - Pattern graph
  - Each pattern associated with a cost which is dependent on the optimization criteria
- Goal:
  - Finding a minimal cost covering of a subject graph using pattern graphs

Example Pattern Graph (1/3)

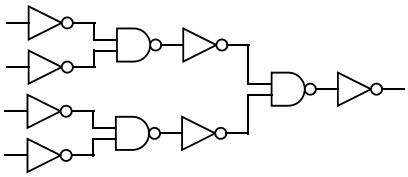


Example Pattern Graph (2/3)

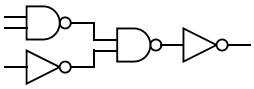
nand4 (4)



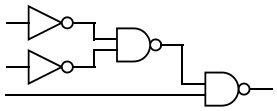
nor4 (4)



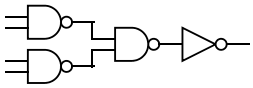
aoi21 (3)



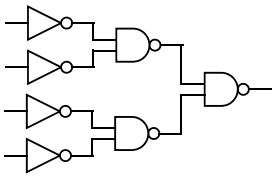
oai21 (3)



aoi22 (4)

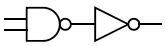


oai22 (4)

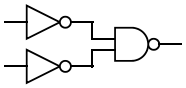


Example Pattern Graph (3/3)

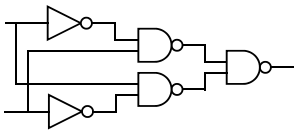
and2 (3)



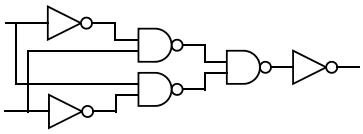
or2 (3)



xor (5)

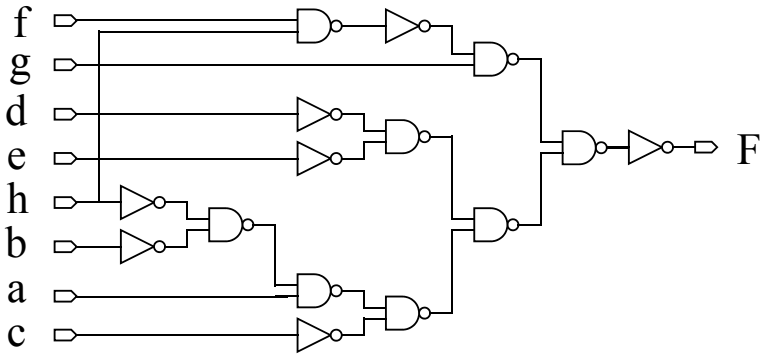


xnor (5)

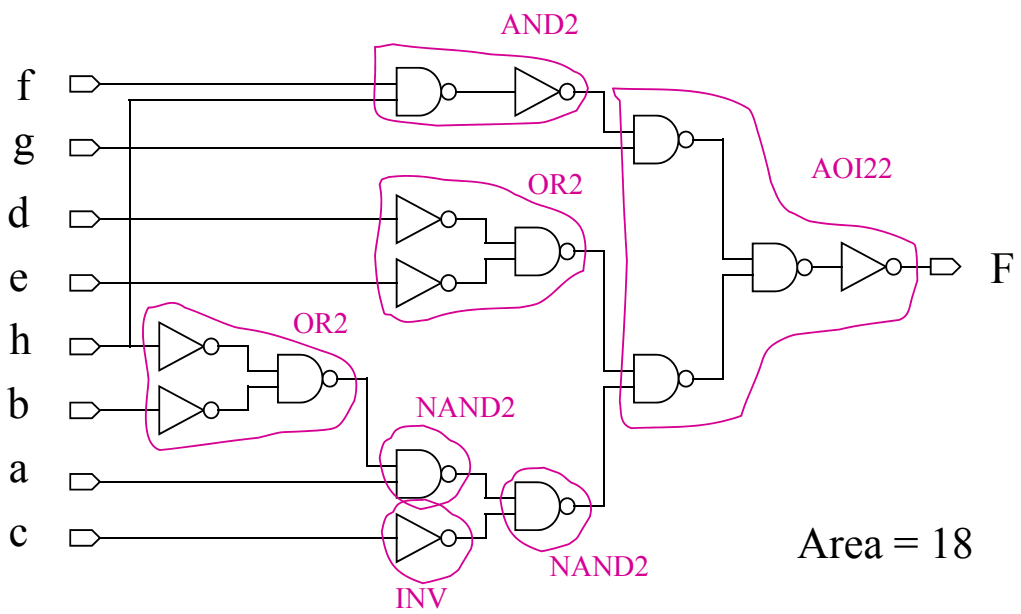


Example Subject Graph

t1 = d + e;
t2 = b + h;
t3 = a t2 + c;
t4 = t1 t3 + f g h;
F = t4';

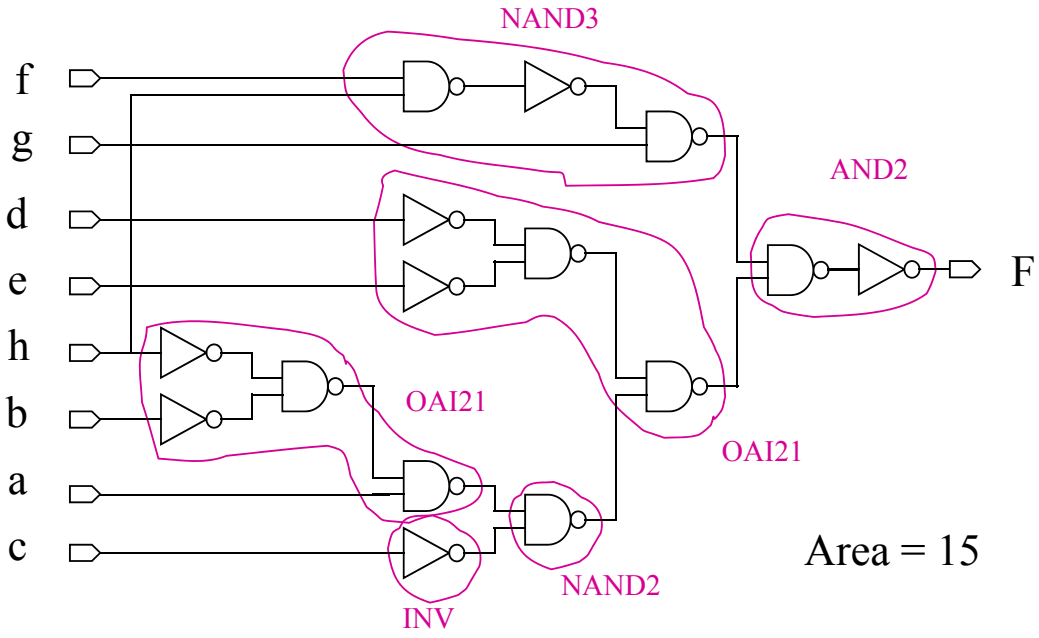


Sample Covers (1/2)



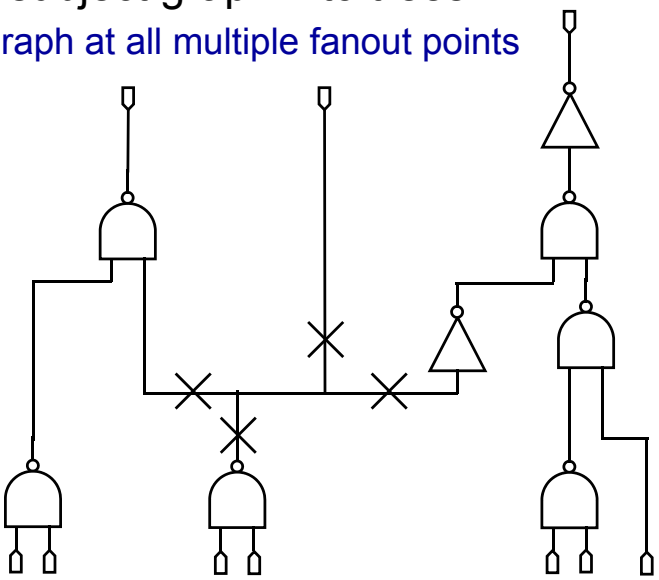
Area = 18

Sample Covers (2/2)



DAGON Approach

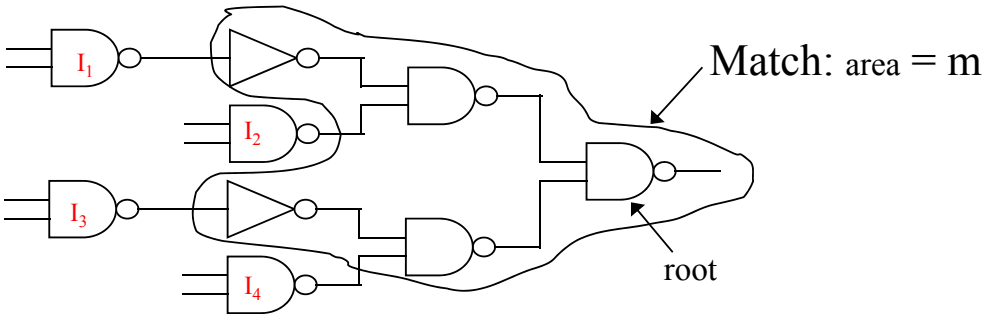
- Partition a subject graph into trees
  - Cut the graph at all multiple fanout points



- Optimally cover each tree using dynamic programming approach
- Piece the tree-covers into a cover for the subject graph

Dynamic Programming for Minimum Area

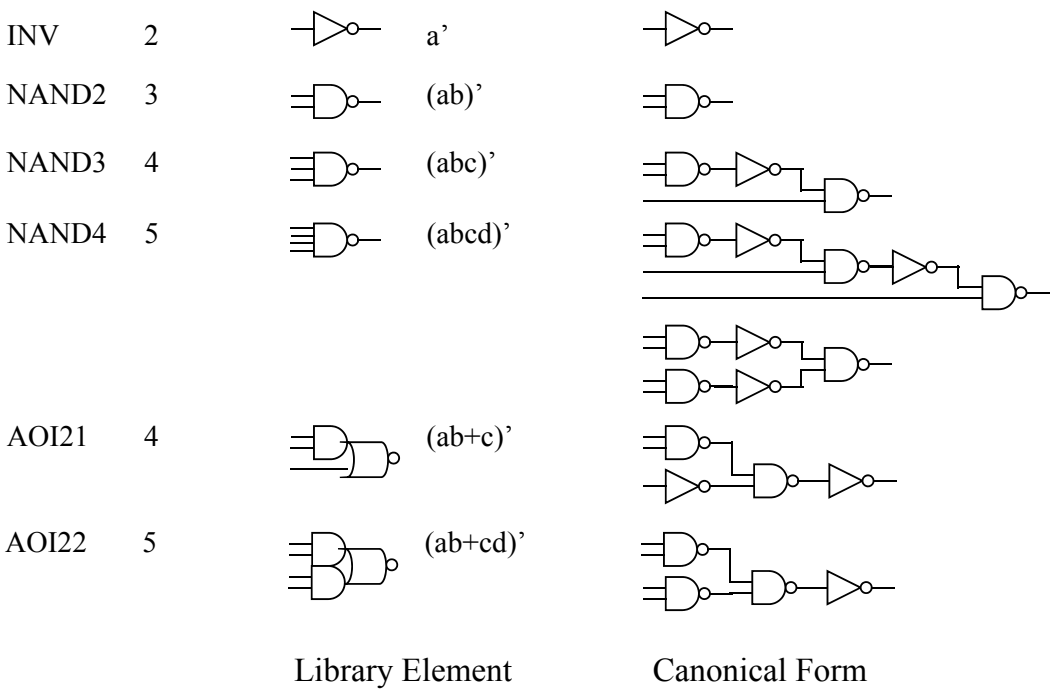
- Principle of optimality: optimal cover for the tree consists of a match at the root plus the optimal cover for the sub-tree starting at each input of the match



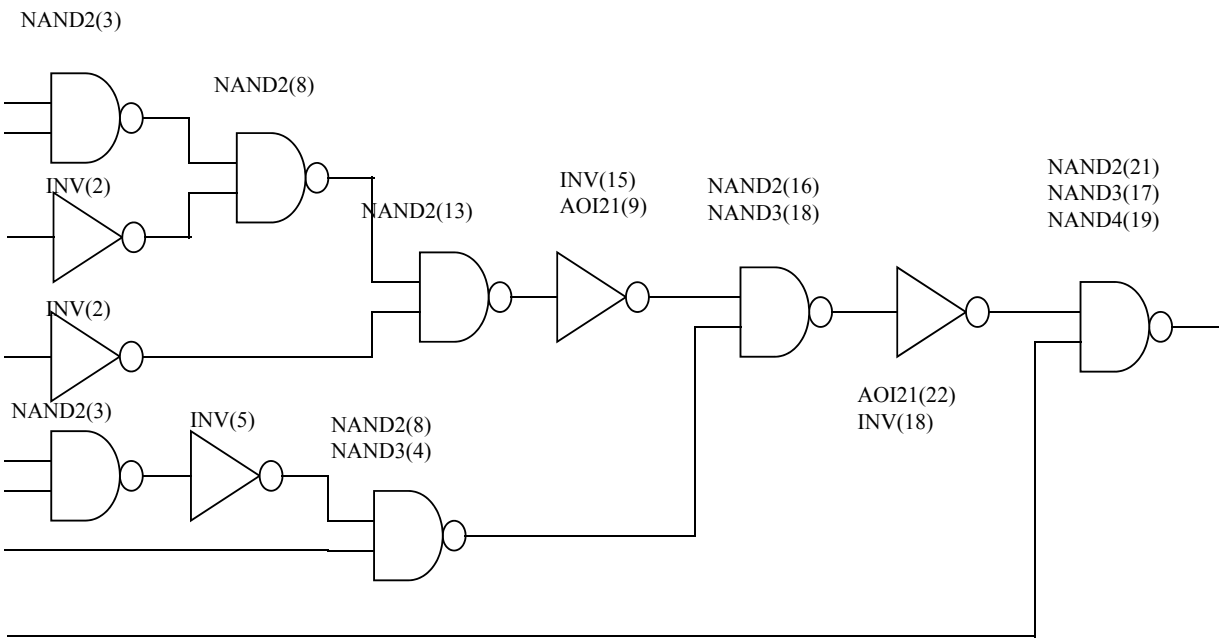
$$A(root) = m + A(I_1) + A(I_2) + A(I_3) + A(I_4)$$

cost of a leaf = 0

A Library Example



DAGON in Action

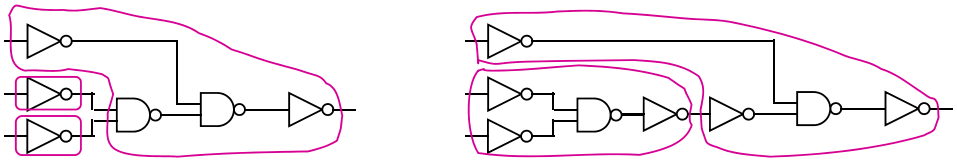


Features of DAGON

- Pros. of DAGON:
  - Strong algorithmic foundation
  - Linear time complexity
    - Efficient approximation to graph-covering problem
  - Given locally optimal matches in terms of both area and delay cost functions
  - Easily "portable" to new technologies
- Cons. Of DAGON:
  - With only a local (to the tree) notion of timing
    - Taking load values into account can improve the results
  - Can destroy structures of optimized networks
    - Not desirable for well-structured circuits
  - Inability to handle non-tree library elements (XOR/XNOR)
  - Poor inverter allocation

Inverter Allocation

- Add a pair of inverters for each wire in the subject graph
- Add a pattern of a wire that matches two inverters with zero cost
- Effect: may further improve the solution



2 INV
1 AIO21

2 NOR2

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Delay Model at Logic Level

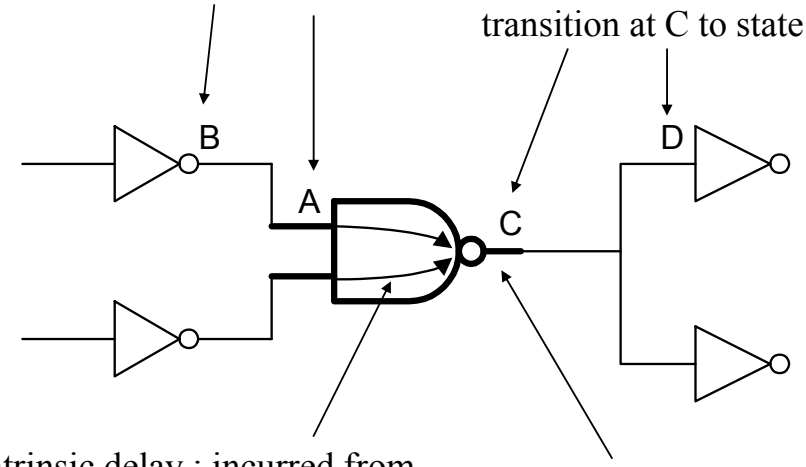
1. unit delay model
   - Assign a delay of 1 to ***each gate***
2. unit fanout delay model
   - Incorporate an ***additional*** delay for ***each fanout***
3. library delay model
   - Use delay data in the library to provide more accurate delay value
   - May use linear or non-linear (tabular) models

Linear Delay Model

Delay = Dslope + Dintrinsic + Dtransition + Dwire

Ds : Slope delay : delay at input A caused by the transition delay at B

Dw : Wire delay : time from state transition at C to state transition at D

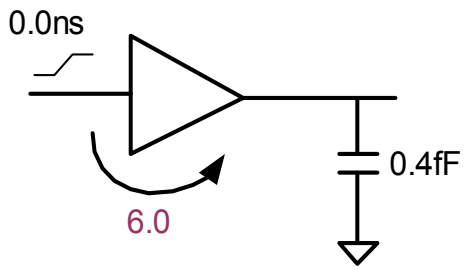


D_I : Intrinsic delay : incurred from cell input to cell output

D_T : Transition delay : output pin loading, output pin drive

Tabular Delay Model

- Delay values are obtained by a look-up table
  - Two-dimensional table of delays (m by n)
    - with respect to input slope (m) and total output capacitance (n)
  - One dimensional table model for output slope (n)
    - with respect to total output capacitance (n)
  - Each value in the table is obtained by real measurement



Total Output Load (fF)

Input Transition (ns)	0.2	0.3	0.4	0.5
0	3	4.5	6	7
0.1	5	8	10.7	13

Cell Delay (ps)

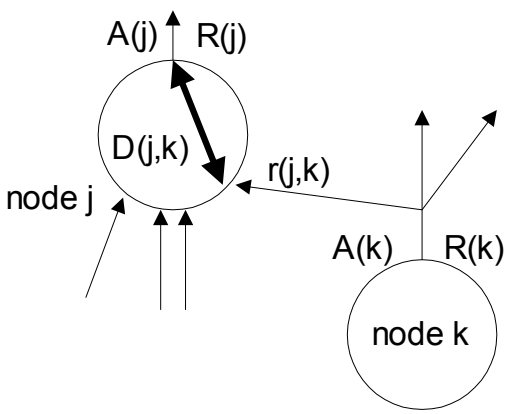
- Can be more precise than linear delay model
  - table size↑ ➔ accuracy ↑
- Require more space to store the table

Arrival Time and Required Time

- arrival time : calculated from input to output
- required time : calculated from output to input
- slack = required time - arrival time

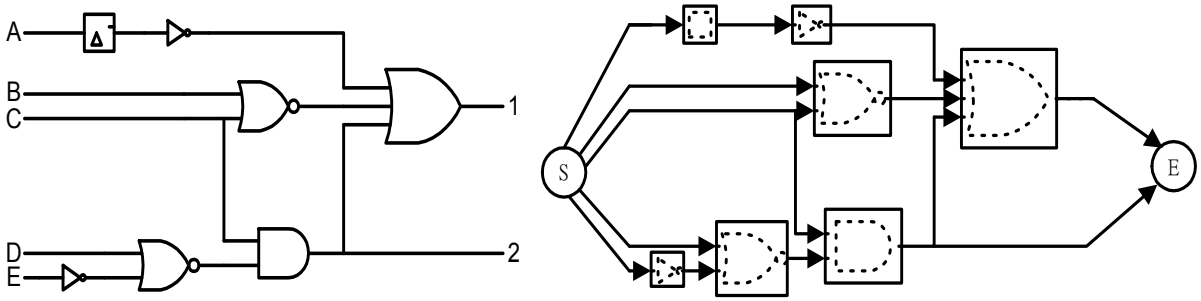
A(j): arrival time of signal j
R(k): required time or for signal k
S(k): slack of signal k
D(j,k): delay of node j from input k

$A(j) = \max_{k \in FI(j)} [A(k) + D(j,k)]$
$r(j,k) = R(j) - D(j,k)$
$R(k) = \min_{j \in FO(k)} [r(j,k)]$
$S(k) = R(k) - A(k)$



Delay Graph

- Replace logic gates with delay blocks
- Add start (S) and end (E) blocks
- Indicate signal flow with directed arcs

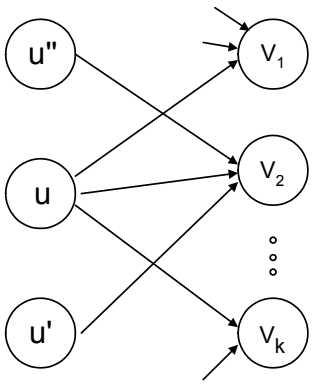


Longest and Shortest Path

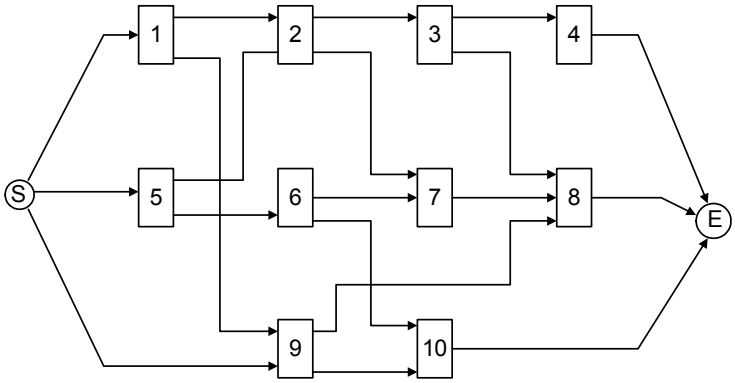
- If we visit vertices in precedence order, the following code will need executing only once for each *u*

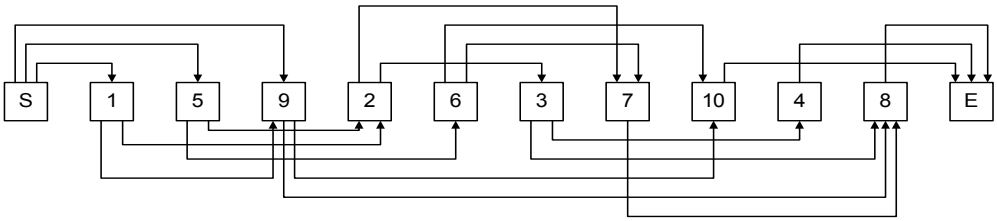
Update Successors[u]

```
for each vertex v ∈ Adj[u] do
    if A[v] < A[u] + Δ[u]   // longest
        then A[v] ← A[u] + Δ [u]
        LP[v] ← u  fi
    if a[v] >a[u] + δ[u]   // shortest
        then a[v] ← a[u] + δ[u]
        SP[v] ← u  fi
```

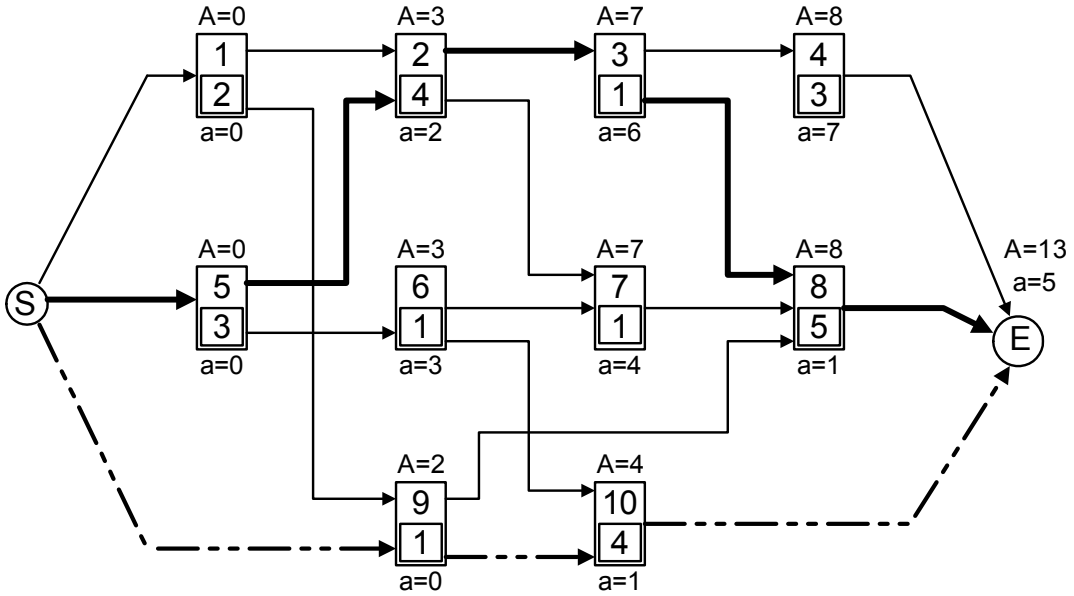


Delay Graph and Topological Sort





Delay Calculation



A=3 → longest path delay

2 → node number

4 → gate delay

a=2 → shortest path delay

P.S: The longest delay and shortest delay of each gate are assumed to be the same.

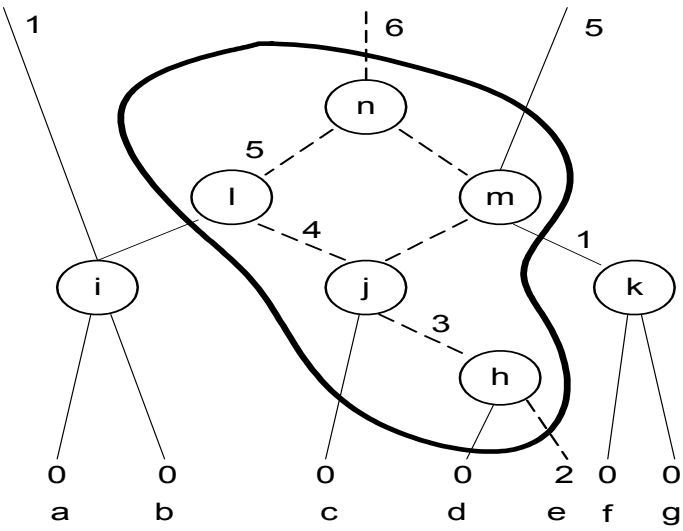
Restructuring Algorithm

While (circuit timing improves) do
    select regions to transform
    collapse the selected region
    resynthesize for better timing
done

- Which regions to restructure ?
- How to resynthesize to minimize delay ?

Restructuring Regions

- All nodes with slack within ε of the most critical signal belong to the ε-*network*
- To improve circuit delay, necessary and sufficient to improve delay at nodes on cut-set of ε-*network*



Find the Cutset

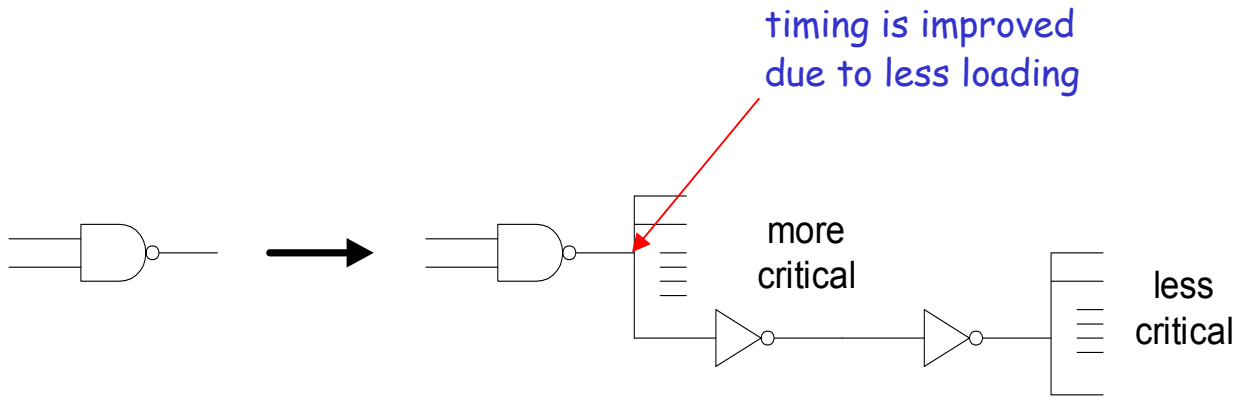
- The weight of each node is $W = Wxt + \alpha * Wxa$
  - Wxt is potential for speedup
  - Wxa is area penalty for duplication of logic
  - α is decided by various area/delay tradeoff
- Apply the maxflow-mincut algorithm to generate the cutset of the ε-*network*
- ε: Specify the size of the ε-*network*
  - Large ε might waste area without much reduction in critical delay
  - Small ε might slow down the algorithm
- α: Control the tradeoff between area and speed
  - Large α avoids the duplication of logic
  - $\alpha = 0$ implies a speedup irrespective of the increase in area

Timing Optimization Techniques (1/8)

- Fanout optimization
  - Buffer insertion
  - Split
- Timing-driven restructuring
  - Critical path collapsing
  - Timing decomposition
- Misc
  - De Morgan
  - Repower
  - Down power
- Most of them will increase area to improve timing
  - Have to make a good trade-off between them

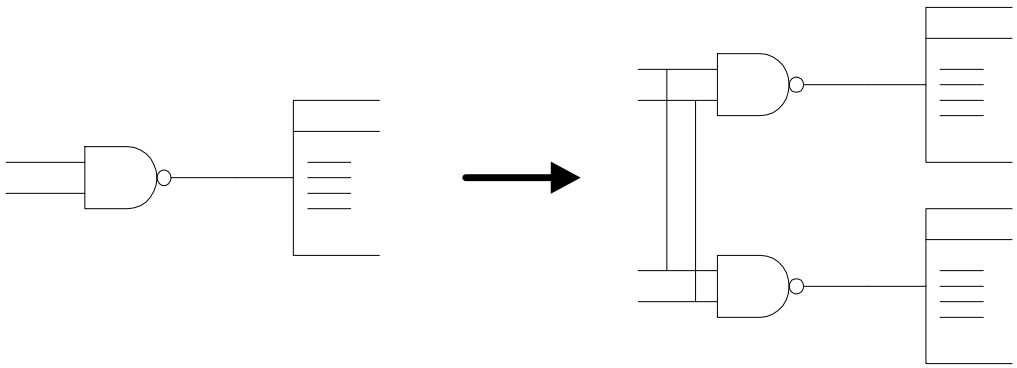
Timing Optimization Techniques (2/8)

- **Buffer insertion**: divide the fanouts of a gate into critical and non-critical parts and drive the non-critical fanouts with a buffer



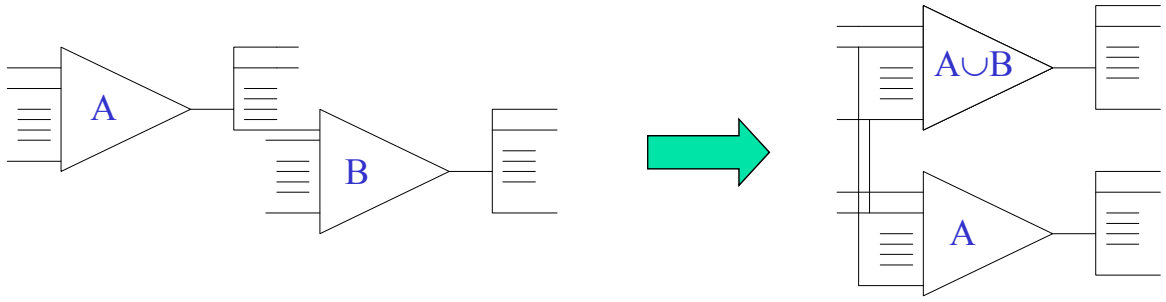
Timing Optimization Techniques (3/8)

- **Split**: split the fanouts of a gate into several parts. Each part is driven with a copy of the original gate.



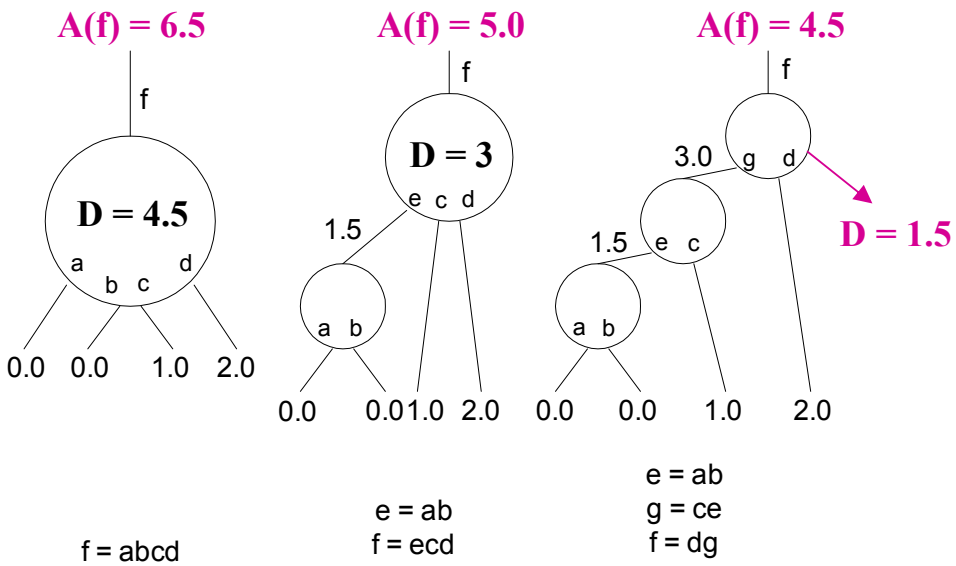
Timing Optimization Techniques (4/8)

- **Critical path collapsing**: reduce the depth of logic networks



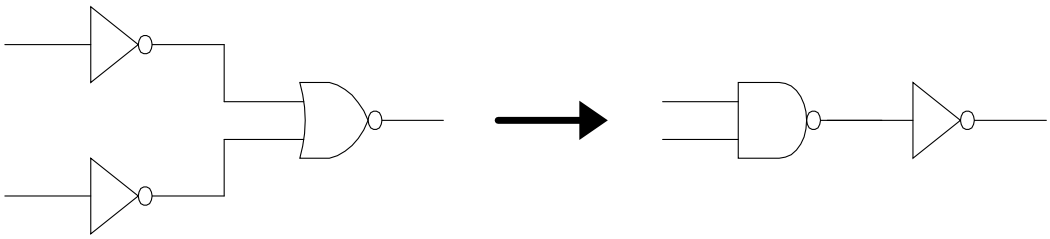
Timing Optimization Techniques (5/8)

- **Timing decomposition**: restructuring the logic networks to minimize the arrival time



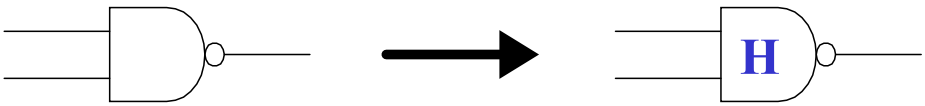
Timing Optimization Techniques (6/8)

- **De Morgan**: replace a gate with its dual, and reverse the polarity of inputs and output
  - NAND gate is typically faster than NOR gate



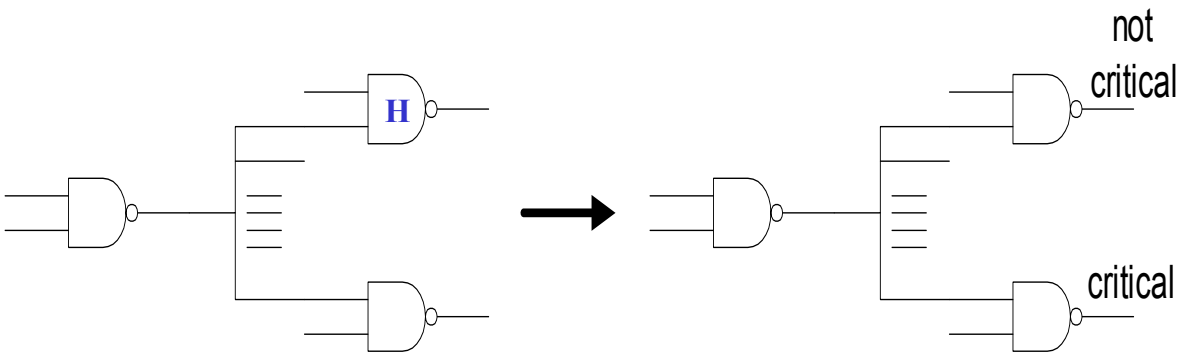
Timing Optimization Techniques (7/8)

- **Repower**: replace a gate with one of the other gate in its logic class with higher driving capability



Timing Optimization Techniques (8/8)

- **Down power**: reducing gate size of a non-critical fanout in the critical path

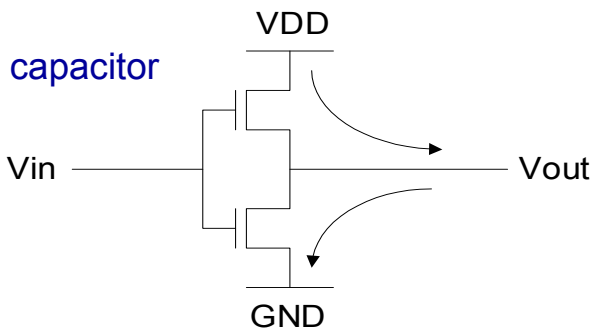


Outline

- Synthesis overview
- RTL synthesis
  - Combinational circuit generation
  - Special element inferences
- Logic optimization
  - Two-level logic optimization
  - Multi-level logic optimization
- Technology mapping
- Timing optimization
- Synthesis for low power

Power Dissipation

- Leakage power
  - Static dissipation due to leakage current
  - Typically a smaller value compared to other power dissipation
  - Getting larger and larger in deep-submicron process
- Short-circuit power
  - Due to the short-circuit current when both PMOS and NMOS are open during transition
  - Typically a smaller value compared to dynamic power
- Dynamic power
  - Charge and discharge of a load capacitor
  - Usually the major part of total power consumption



Power Dissipation Model

$$P = \frac{1}{2} \bullet C \bullet V_{dd}^2 \bullet D$$

- Typically, ***dynamic power*** is used to represent total power dissipation

  P: the power dissipation for a gate

  C: the load capacitance

  V_{dd}: the supply voltage

  D: the transition density
- To obtain the power dissipation of the circuit, we need
  - The **node capacitance** of each node (obtained from layout)
  - The **transition density** of each node (obtained by computation)

The Signal Probability

- Definition: The signal probability of a signal x(t), denoted by P_x^1 is defined as :

$$P_x^1 \equiv \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} x(t)\, dt$$

where T is a variable about time.

- P_x^0 is defined as the probability of a logic signal X(t) being equal to 0.
- $P_x^0 = 1 - P_x^1$

Transition Density

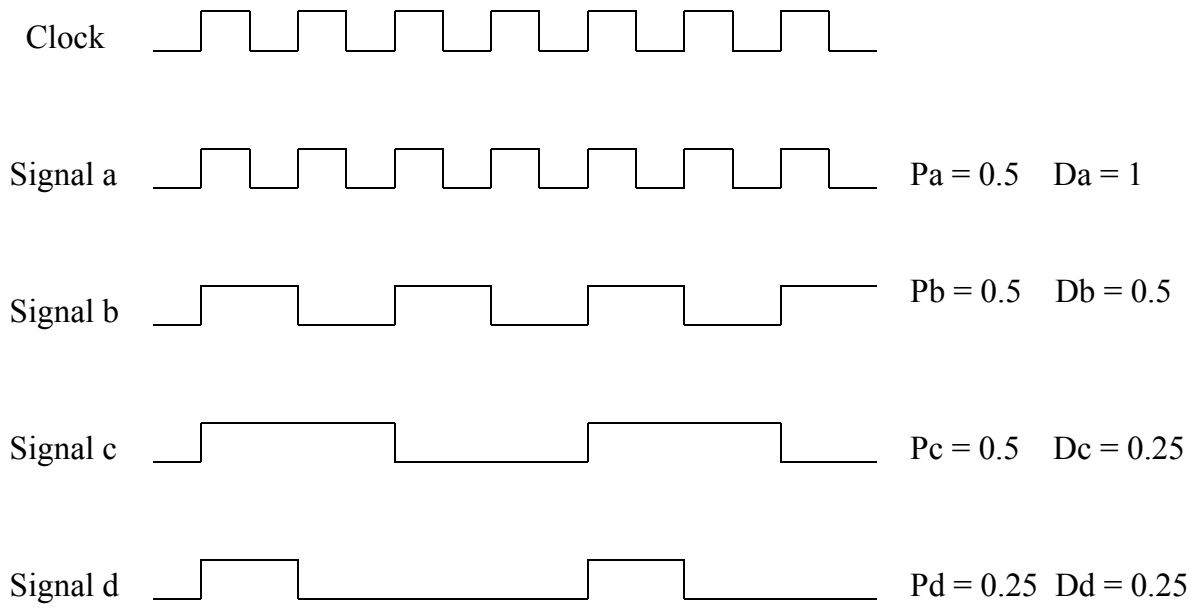
- Definition: The transition density Dx of a logic signal x(t), $t \in (-\infty, \infty)$, is defined as

$$D_x \equiv \lim_{T \to \infty} \frac{n_x(T)}{T \cdot f_c}$$

where f_c is the clock rate or frequency of operation.

- Dx is the expected number of transitions happened in a clock period.
- A circuit with clock rate 20MHz and 5 MHz transitions per second in a node, transition density of this node is 5M / 20M = 0.4

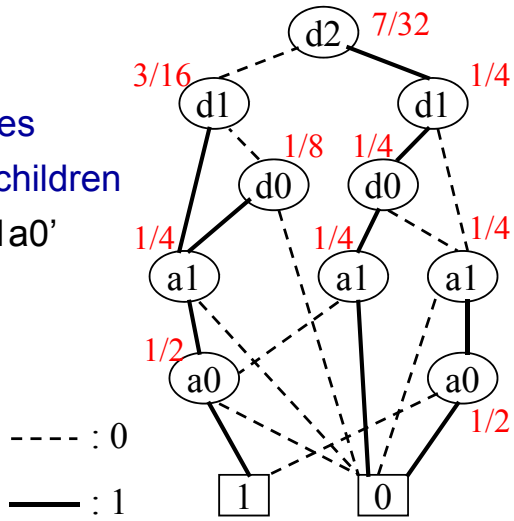
Signal Probability and Transition Density



The Calculation of Signal Probability

- BDD-based approach is one of the popular way
- Definition
  - p(F) : fraction of variable assignments for which F = 1
- Recursive Formulation
  - p(F) = [p(F[x=1]) + p(F[x=0])] / 2
- Computation
  - Compute bottom-up, starting at leaves
  - At each node, average the value of children
- Ex: F = d2'(d1+d0)a1a0 + d2(d1'+d0')a1a0'
  + d2d1d0a1'a0

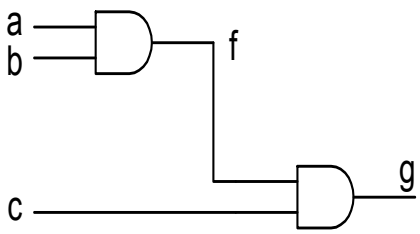
  p(F) = 7/32 = 0.21875



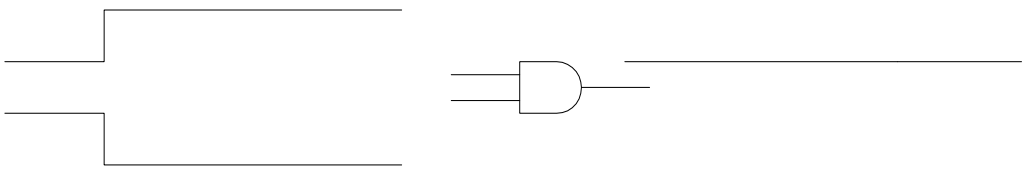
The Calculation of Transition Density

- Transition density of cube
  - f = ab
  - $D_f = D_a P_b + D_b P_a - 1/2\, D_a D_b$
  - $D_a P_b$ means that output will change when b=1 and a has changes
  - $1/2\, D_a D_b$ is the duplicate part when both a and b changes
- n-input AND :
  - a network of 2 -input AND gate in zero delay model
  - 3-input AND gate

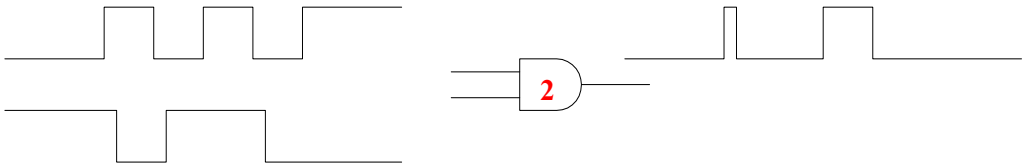
    $D_g = D_f P_c + D_c P_f - 1/2\, D_f D_c$
- Inaccuracy of this simple model :
  - Temporal relations
  - Spatial relations



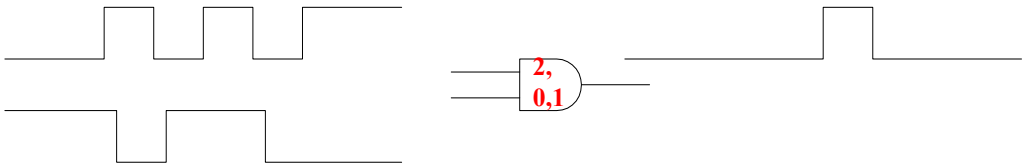
The Problem of Temporal Relations



(1) Without considering the Gate Delay and Inertial Delay

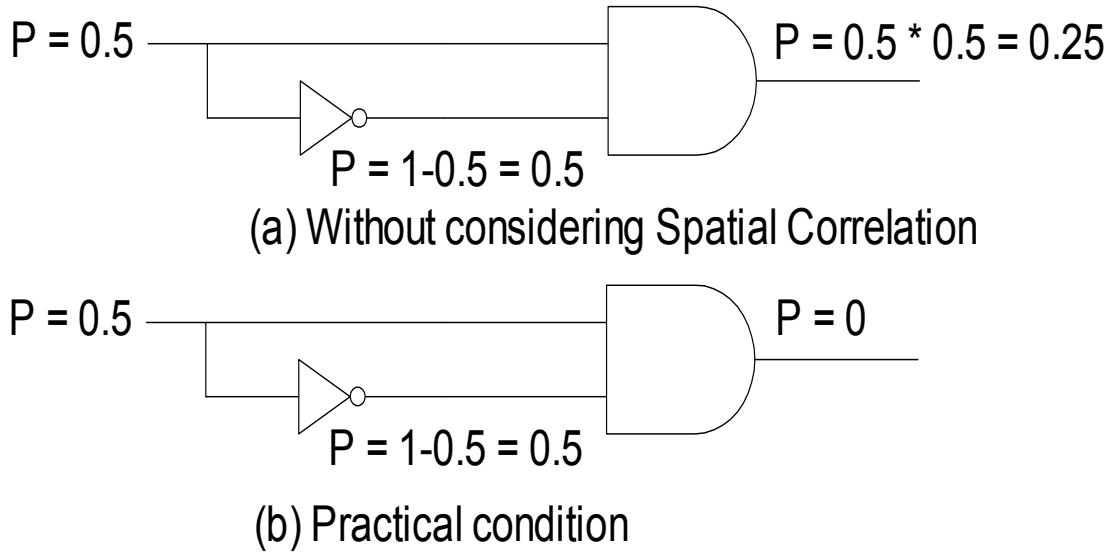


(2) Without considering Inertial Delay



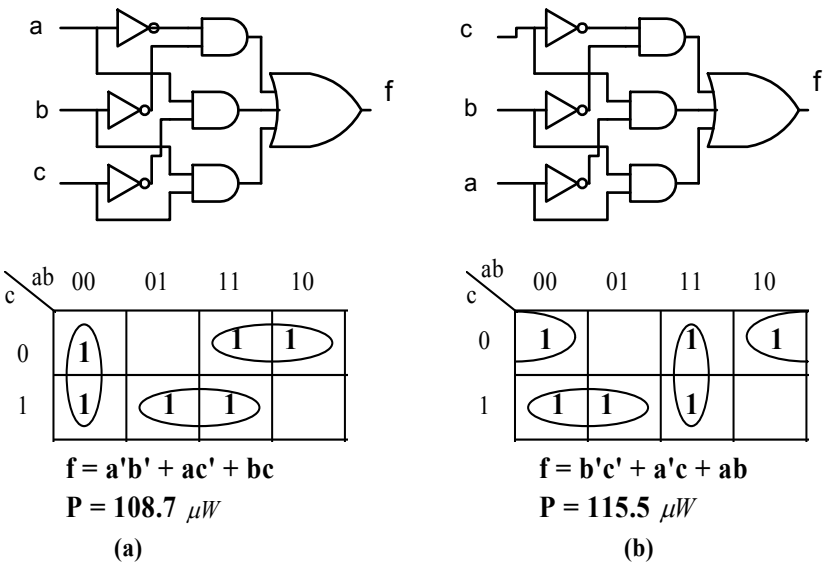
(3) Practical condition

The Problem of Spatial Correlation



Logic Minimization for Low Power (1/2)

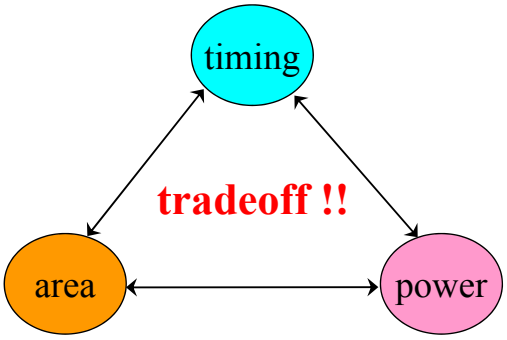
- Consider an example:



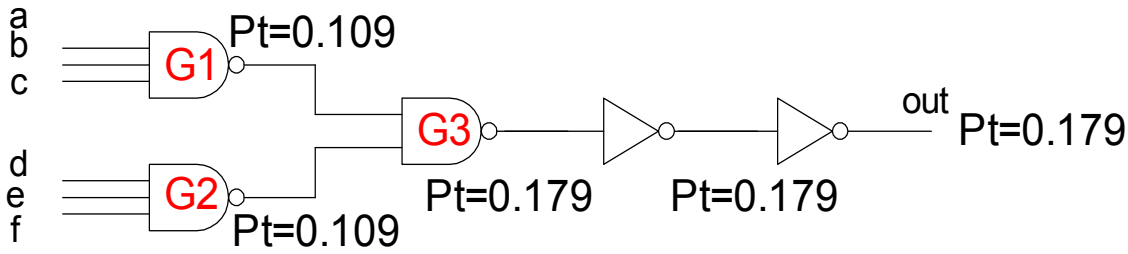
- Different choices of the covers may result in different power consumption

Logic Minimization for Low Power (2/2)

- Typically, the objective of logic minimization is to minimize
  - NPT : the number of product terms of the cover
  - NLI : the number of literals in the input parts of the cover
  - NLO : the number of literals in the output parts of the cover
- For low power synthesis, the power dissipation has to be added into the cost function for best covers



Technology Mapping for Low Power (1/3)

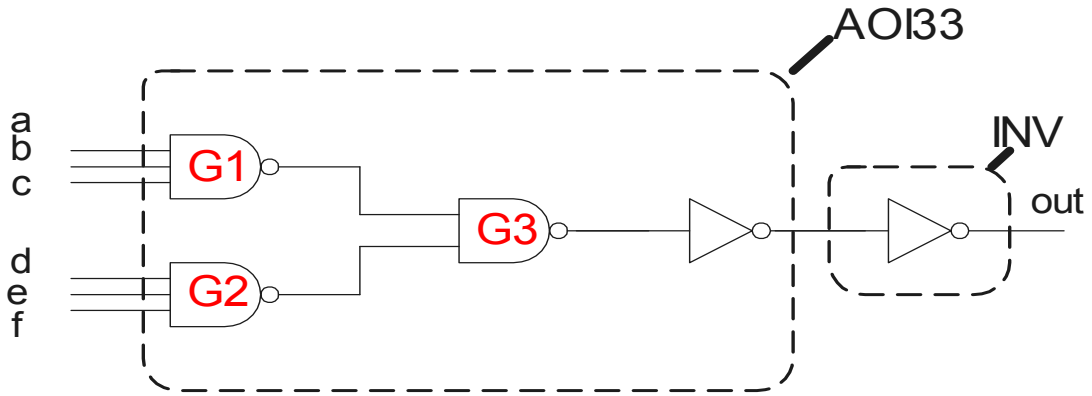


(a) Circuit to be mapped

Gate Type	Area	Intrinsic Cap.	Input Load
INV	928	0.1029	0.0514
NAND2	1392	0.1421	0.0747
NAND3	1856	0.1768	0.0868
AOI33	3248	0.3526	0.1063

(b) Characteristics of Library

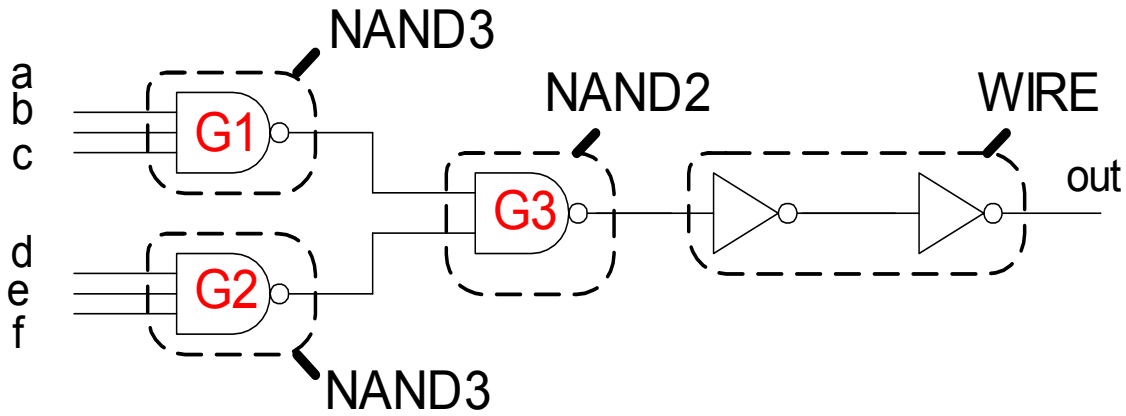
Technology Mapping for Low Power (2/3)



Area Cost: 4176
Power Cost: 0.0907

(a) Minimun-Area Mapping

Technology Mapping for Low Power (3/3)



Area Cost: 5104
Power Cost: 0.0803

(b) Minimun-Power Mapping