NYCU – 2022 DCS 數位電路與系統 期末考

1. Pipeline:

(a) C, 解釋(2%)

平均每一個 Stage 的計算量，可以使 cycle time 降低。

在 A 加入: Max(3, 10) = 10 ns,

在 B 加入: Max(5, 8) = 8 ns,

在 C 加入: Max(7, 6) = 7 ns

在 C 加入可以得到最小的 cycle time

(b) 6 ns 解釋(2%)

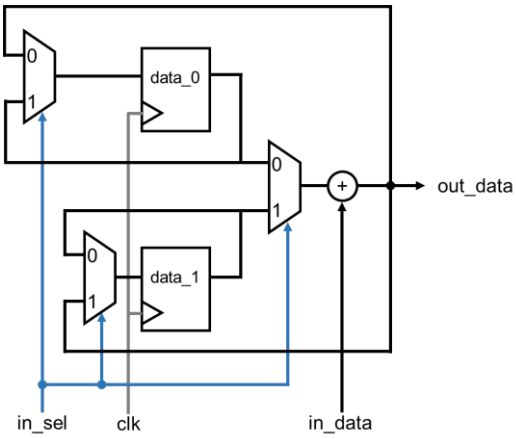
Max (3, 4, 6) = 6 ns

(c) Throughput = 總計算量/Cycle time = (45+40+50+60)/6ns = 32.5 GOPS (2%)

(d) 兩組 pipeline register，解釋(2%)可以讓 cycle time 降低，提高 throughput

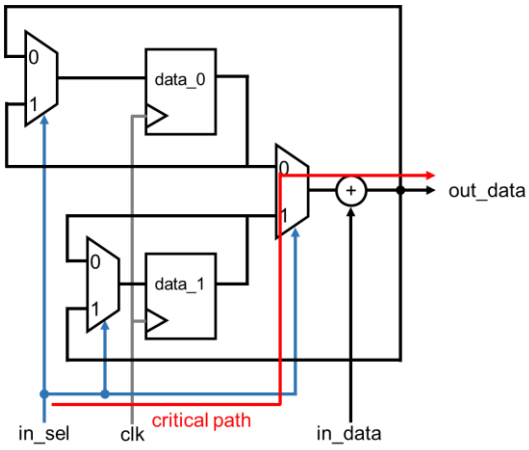
2. Block diagram & timing report

(a) (10%)



一個 MUX 標錯順序-2，沒畫 clk-2

(b) (3%)



起點: in_sel、終點: out_data (各 1%)

(c)

發生 timing violation，原因是有 input-to-output 的 timing path (2%)，

input external delay 和 output external delay 把一整個 cycle time 耗完了，

所以不管怎麼減少中間 combination 運算都沒用，

解決方法(3%)，

只能在 in_sel 與 in_data 輸入前擋一層 DFF，或是在 out_data 輸出前擋一層 DFF，

只擋 in_sel 或 in_data 不給分，只寫擋 DFF 但沒說哪裡不給分，

只提到其他方式(優化組合電路、提高 cycle time)不給分，

擋對 DFF 但提到其他方式給 2 分

3. Waveform

因為 Pattern 的第 10 行是整數除以整數，所以 cycle time 是 4 ns，

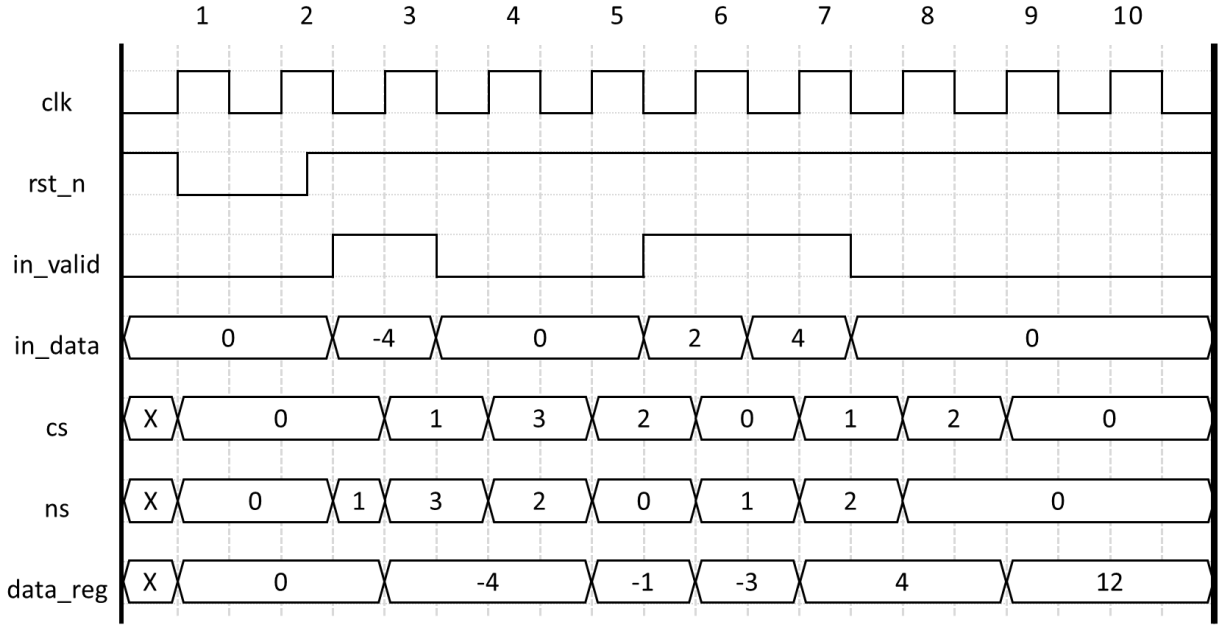
rst_n 拉起的位置會在第二 cycle 3/4 處，而不是 clk 上緣處。

1 bit / multi-bit 格式錯: 每錯一個訊號-2

rst_n: 下緣錯-1，上緣錯-2

其他訊號: 錯一個 cycle -1

cs, ns, data_reg 前面沒 unknown -1



4-10 請參考講義

10. memory data

Need to add DFF for next state and output

	State	carew	address	data
gns	00	0	000	00100001
	00	1	001	01100001
yns	01	0	010	11010001
	01	1	011	11010001
gew	11	0	110	10001100
	11	1	111	10001100
yew	10	0	100	00001010
	10	1	101	00001010

11. (Pipelining)

You have been given the task of designing a new media chip for HD applications. Specifications call for the rendering of a 2000x1000 pixel image at 100Hz, With a single module, it takes 10us to process one pixel, and t_{reg} is 0ps.

(a) What is the throughput needed, in pixels per second, for this task?

(b) Your coworker suggests making one long pipeline. Can you do this and still meet your throughput goal? If so, how many stages does it require? If not, why not?

(c) Why could (a) be a bad idea?

(d) Another coworker suggest just replicating the processing module; how many do you need?

(e) Why this be a bad idea?

(f) After talking to the logic designers, you decide to use replicated ten-stage pipelined. How many do you need?

(a) 2000x1000*100Hz/sec =200x10^6 =2* 10^8pixels/sec

(b) 2*10^8/ (10^6) = 2000, Need to speedup by x2000

2000 stages is required

(c) This could be a very long pipeline stage, thus have long latency, and could significant performance penalty when stall

(d) duplicate 2000

(e) Large area

(f) Duplicate 200

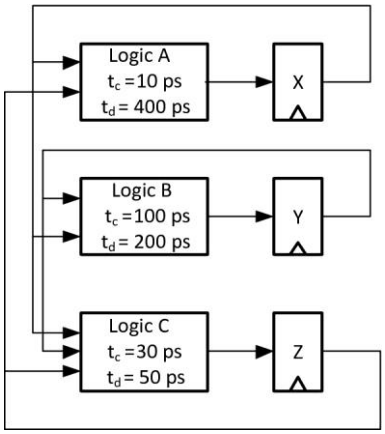
12. (setup time and hold time violation check)

For Flip-Flop A in Table 1, and a 2GHz clock, check the following figure for timing violations. If there is a hold time violation, indicate

(a) where delay must be added, and

(b) the necessary delay

(c) recheck for setup time violation. Is it possible to run faster than 2GHz clock? Derive the cycle time for this maximum clock frequency?



Parameter (ps)	DFF A
Setup time: t_s	20
Hold time: t_h	30
Contamination delay, clock to q, T_{ccq}	10
Propagation delay, clock to q, t_{dcq}	20

(Hint: setup time check, tcy ≥ tdCQ + tdMax + ts

Hold time check, th ≤ tcCQ + tcMin)

(a) A 2GHz cycle time gives tcy = 500ps.

tcy ≥ tdCQ + tdMax + ts

500 ≥ 20 + 400 + 20, no setup time violation.

500 ≥ 440, Cycle time can be reduced to 440ps, faster than 2GHz clock

th ≤ tcCQ + tcMin

30 ≤ 10 + 10

30 ≤ 20 (violated), hold time violation, add 10ps delay to logic A to solve this.

(b) add 10ps delay

(c) with extra 10ps delay, tcy ≥ 20 + 400 + 20 + 10 = 450