REPORT

DCS HW1
Student: 111511076 陳彥宇

Submodule Explanation

The homework's module can be separated into 3 sections.

1. Fetch values with given address
   - There are 6 input addresses in total, so 6 of the TA's register module must be instantiated
2. Rearrange the sequence
   - Some operations require the numbers sorted in non-decreasing or non-increasing order, so I used a modified version of Lab02's module(It could take 5 inputs, I made it take 6 inputs by adding 5 more comparators) to achieve this
   - The "Rearrange_Input_Sequence" module takes the values in their original order, the sorted values, and opcode[2:0] and sends the chosen sequence to the next stage.
3. Compute output
   - The "Compute_out_n" module computes the final output based on the operation given by opcode[2:0]

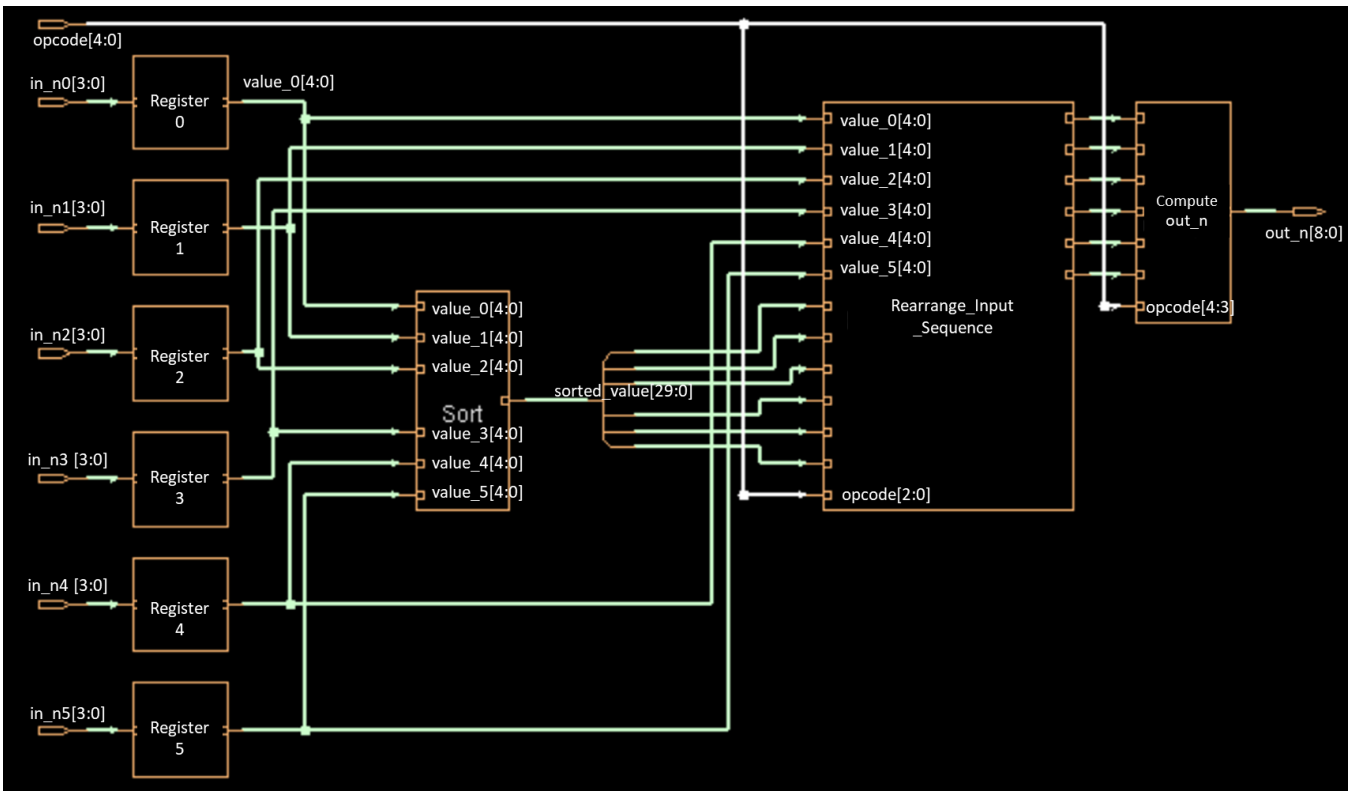

Fig. 1 Design Block Diagram

Area & Timing Optimization:

According to p61 of Lecture 2-4, related logic should be put in the same always block so that resources can be shared. By combining the modules "Rearrange_Input_Sequence" and "Compute_out_n" into one. I reduced the area from 21383.099 to 20034.907. This may sacrifice a bit of readability, but it's essentially just moving two case statements into the same always block. This highlights the importance of properly explaining the code using comments when working as a group. Circuit design is all about making compromises, so such sacrifices are inevitable. Properly explaining things will save everybody's time and

make the group project more efficient.

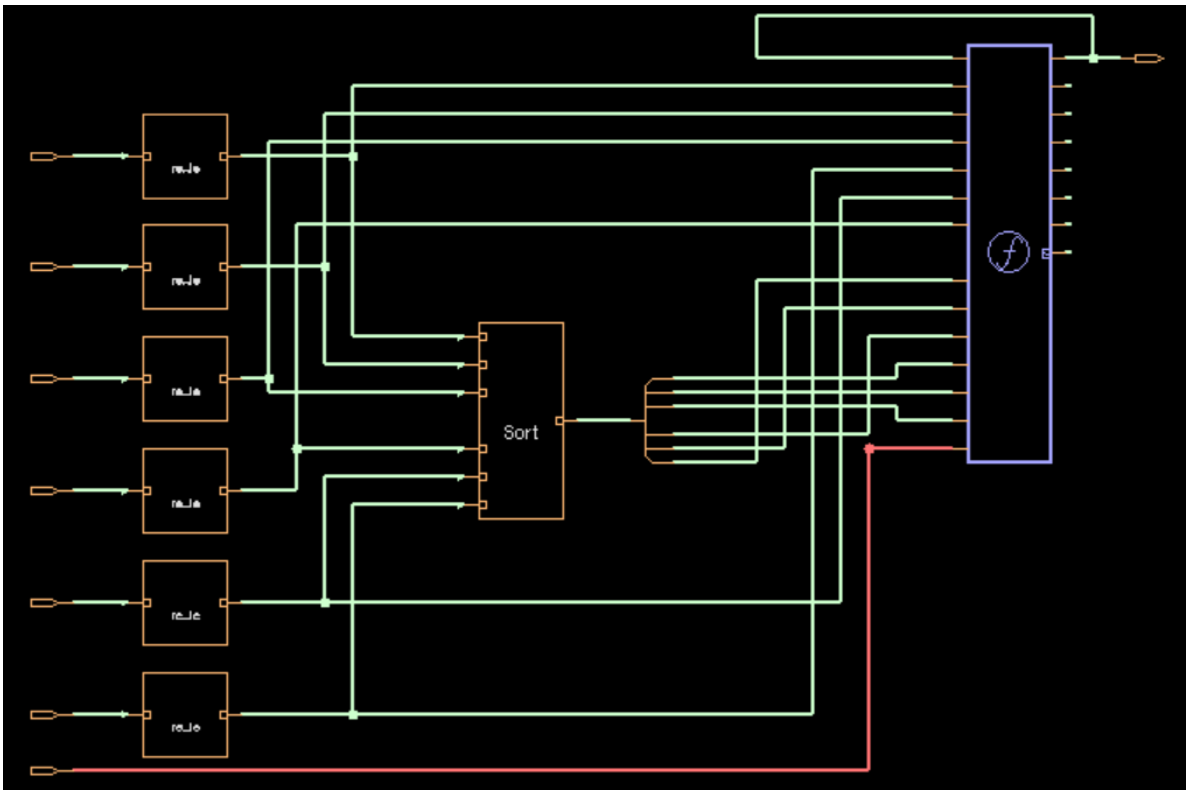

Fig. 2 Schematic of 2 Modules Combined

15 Comparators **12 Comparators**

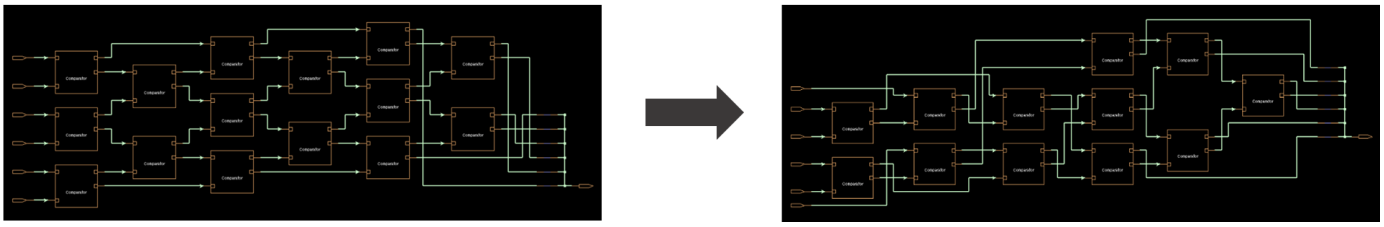

Fig. 3 Sorting Modification

Initially, I thought that sorting 6 elements required 15 comparisons minimum. However, that didn't turn out to be the case. The correct minimum is actually 12 comparisons. Implementing this led to an area decrease of approximately 2000.

n	1	2	3	4	5	6	7
Depth[10]	0	1	3	3	5	5	6
Size, upper bound[11]	0	1	3	5	9	12	16
Size, lower bound (if different)[12]							

Fig. 4 n Element Minimum Comparisons Required

Code	V1(Best Readability)	V2(Module Combined)	V3	V4	V5	V6(Sorting Improved)
Area	21382.099435	20034.907432	19479.39648	17440.31544	16415.78425	15181.68989

Code: https://github.com/Mark-Chen0220/DCS/tree/main