1.

(a)Please briefly describe the advantage and the disadvantage for the synchronous and asynchronous reset, r espectively.

Synchronous :

(1)pros : glitch filtering(1/1)

(2)cons : larger area, larger critical path, it can’ t be reset without clock signal(1/1)

Asynchronous :

(1)pros : smaller area, smaller critical path, reset signal is immediate, reset is independent of clock signal(1/1)

(2)cons : noisy reset could cause unwanted reset, metastability issue(1/1)

(b)(4/4)

如果有人兩個答案寫同一個，全錯!!!!!!!!!!!!!!!!!!!!!!!!沒有部份給分!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

```
always_ff @ (posedge clk or negedge rst_n) begin
    if(!rst_n)
        c <= 'd0;
    else
        c <= a + 'd1;
end
```

Ans : Asynchronous reset

```
always_ff @ (posedge clk) begin
    if(!rst_n)
        c <= 'd0;
    else
        c <= a + 'd1;
end
```

Ans : Synchronous

(c)(4/4)

Please identify the following figure as synchronous reset or asynchronous reset.

如果有人兩個答案寫同一個，全錯!!!!!!!!!!!!!!!!!!!!!!!!沒有部份給分!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

Left : Synchronous

Right : Asynchronous

(d)(4/4)

Synchronous reset

2.

(a) Please determine if the following code is synthesizable. (Answer yes or no) (8%)

```
always_comb begin
    a = in;
    a = a + 1;
    b = a + 1;
end
```

Ans: Yes

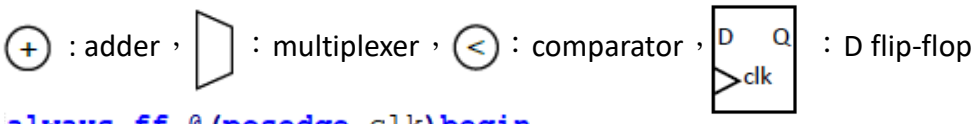
```
always_comb begin
    a <= in;
    a <= a +
    b <= a + 1;
end
```

Ans: No

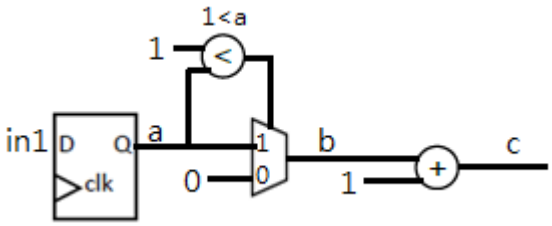
(b) Please draw the block diagrams of the following two circuits using the symbols of adders, multiplexers, comparators, and D flip-flops. (18%)

※ comparator, multiplexer 之訊號順序請標示清楚。

※所有訊號不論 multi-bit bus 或 1-bit signal 都用一條線表示即可。




```
always_ff @(posedge clk)begin
    a = in1;
    b = (a>1 ? a:0);
    c = b + 1;
end
```

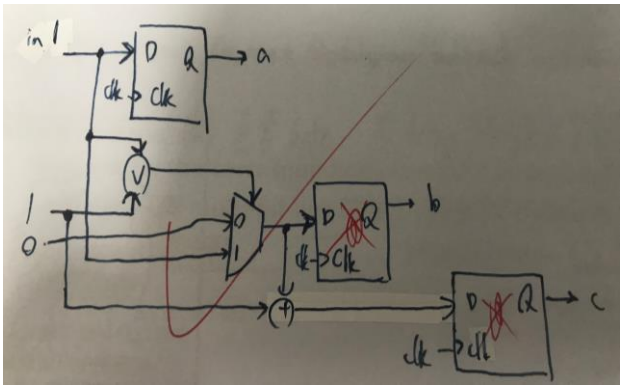


comparator, multiplexer 訊號順序沒畫不扣分

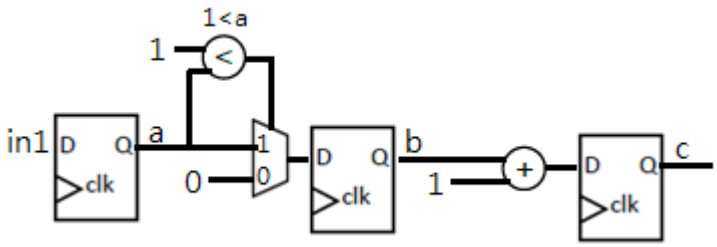
FF 數量位置全對得 4 分，一個 FF 但位置錯誤得 3 分

combination circuit b=(a>1 : a:0)畫對 3 分，c=b+1 畫對且電路順序邏輯正確得 2 分

下圖為第二種解，寫這種解的同學被改錯麻煩找助教補正



```
always_ff @(posedge clk)begin
    a <= in1;
    b <= (a>1 ? a:0);
    c <= b + 1;
end
```



FF 數量位置全對得 4 分

combination circuit b=(a>1 : a:0)畫對 3 分，c=b+1 畫對且電路順序邏輯正確得 2 分

3. Please find out 5 errors in the design below (i.e. the errors cause 01_RTL and 02_SYN failed), write down the line number of each error, and briefly describe the type of error. (There are 6 errors exist, find out 5 of them and you can get all points) (25%)

Ans:

25 or 30 multiple drivers

31 combinational loop

33~44 no default

36 latch

40 in1 is integer, can not synthesis

46 assign in always block

每找出一個 bug 得 5 分，bug 描述大致正確但有瑕疵依情況得 2~4 分

4.

(a) RTL 只驗證 function 的正確性，並沒有時間的考量，所以不會出錯。
SYN 會考慮時間來選擇要使用哪一些 cell，若 critical path 超出 cycle time，這樣 slack 就會 violated

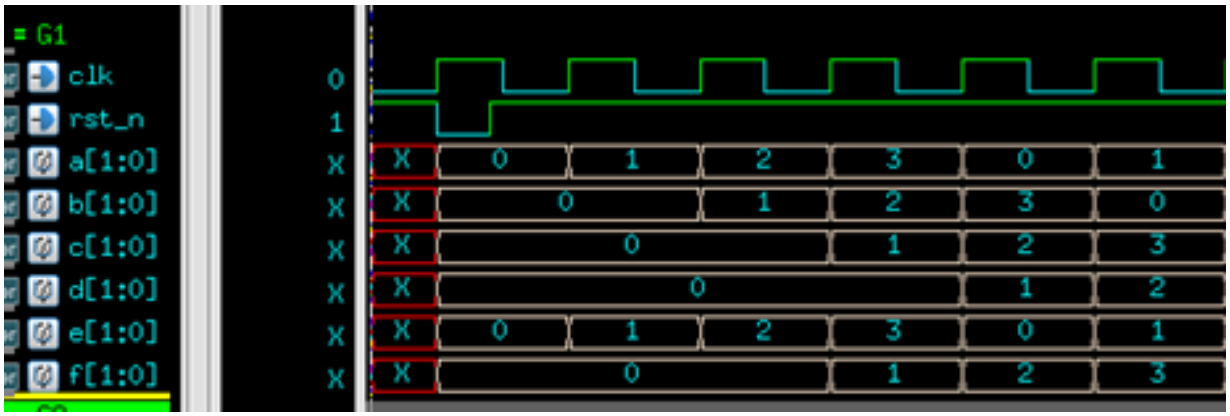
註：你們可以試著改改看 02_SYN 裡面的 syn.tcl　Set CYCLE 的時間變小，你會發現到除了 slack 有可能錯以外，你會發現面積也會變大喔！

評分標準：RTL 會不會發生錯誤(1%)，原因(2%)
SYN 會不會發生錯誤(1%)，原因(2%)

(b)
01_RTL　電路模擬，檢查電路功能性與 Pattern 是否相符，不考慮時間的資訊。
02_SYN　電路合成，實際合成電路，會考慮時間資訊，且會產生面積等結果。
03_GATE 用 02 合成的電路來模擬，跟 01 相比多了 timing 的資訊。

評分標準: 01 02 03 各三分，有寫到 timing 的資訊(一分)且描述沒錯誤(兩分)就給對。
Timing 錯誤扣一分，描述沒寫扣兩分

5.



評分標準: 一根訊號錯就扣一分，總共六分