REPORT5

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| DCS HW5 |
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Design Diagram:

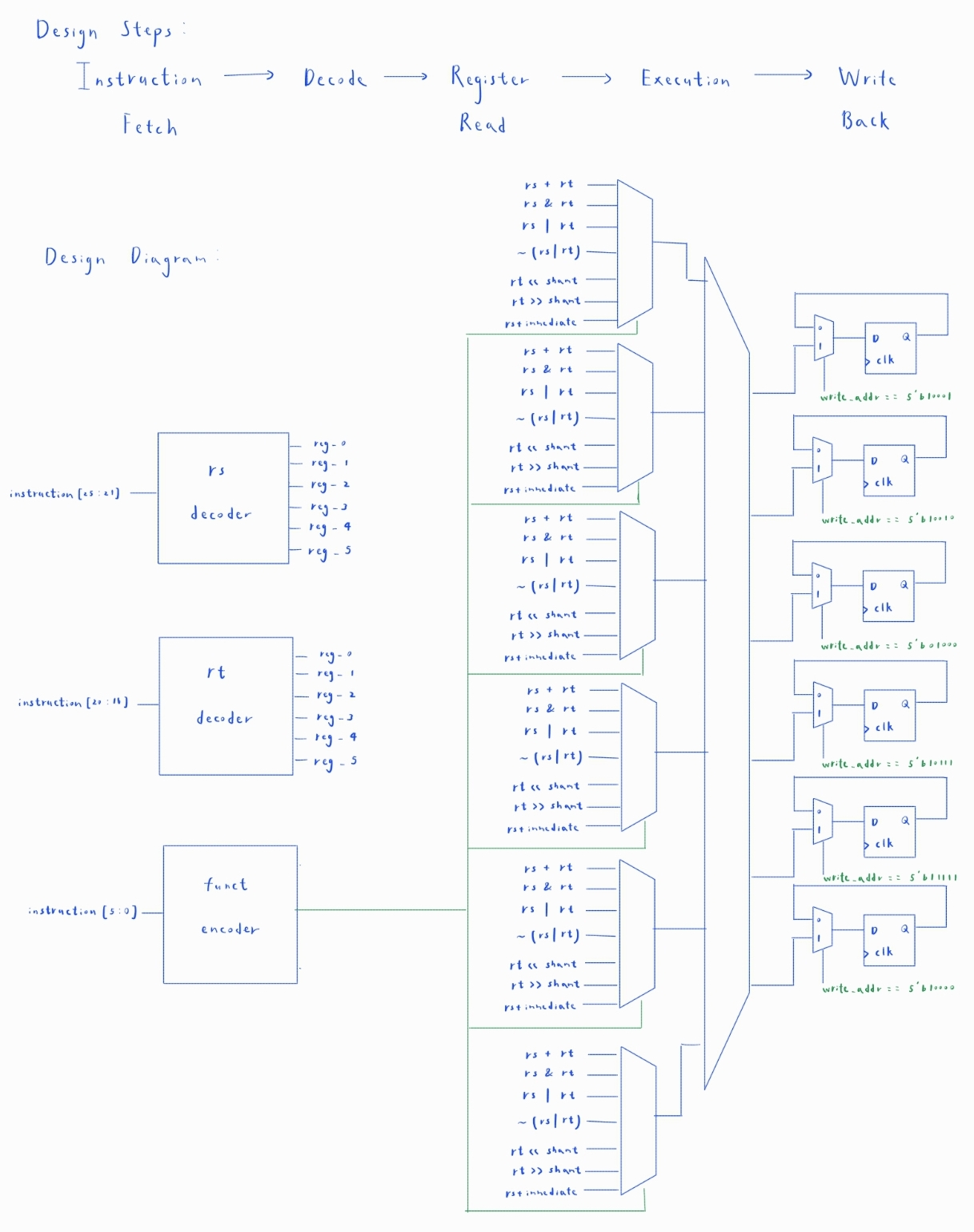


Fig1: Design Diagram

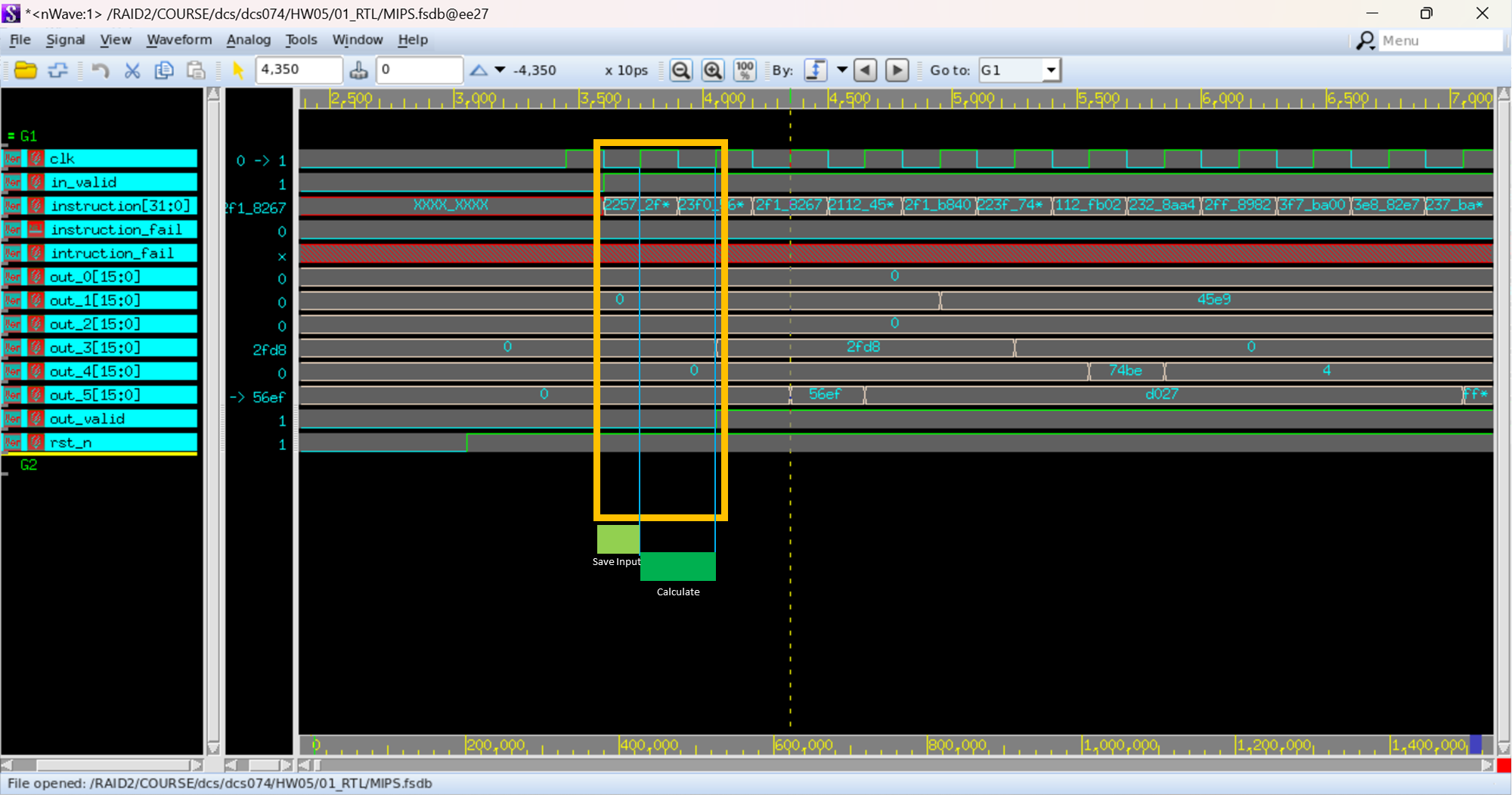
# Design Steps

This problem can be separated into several segments:

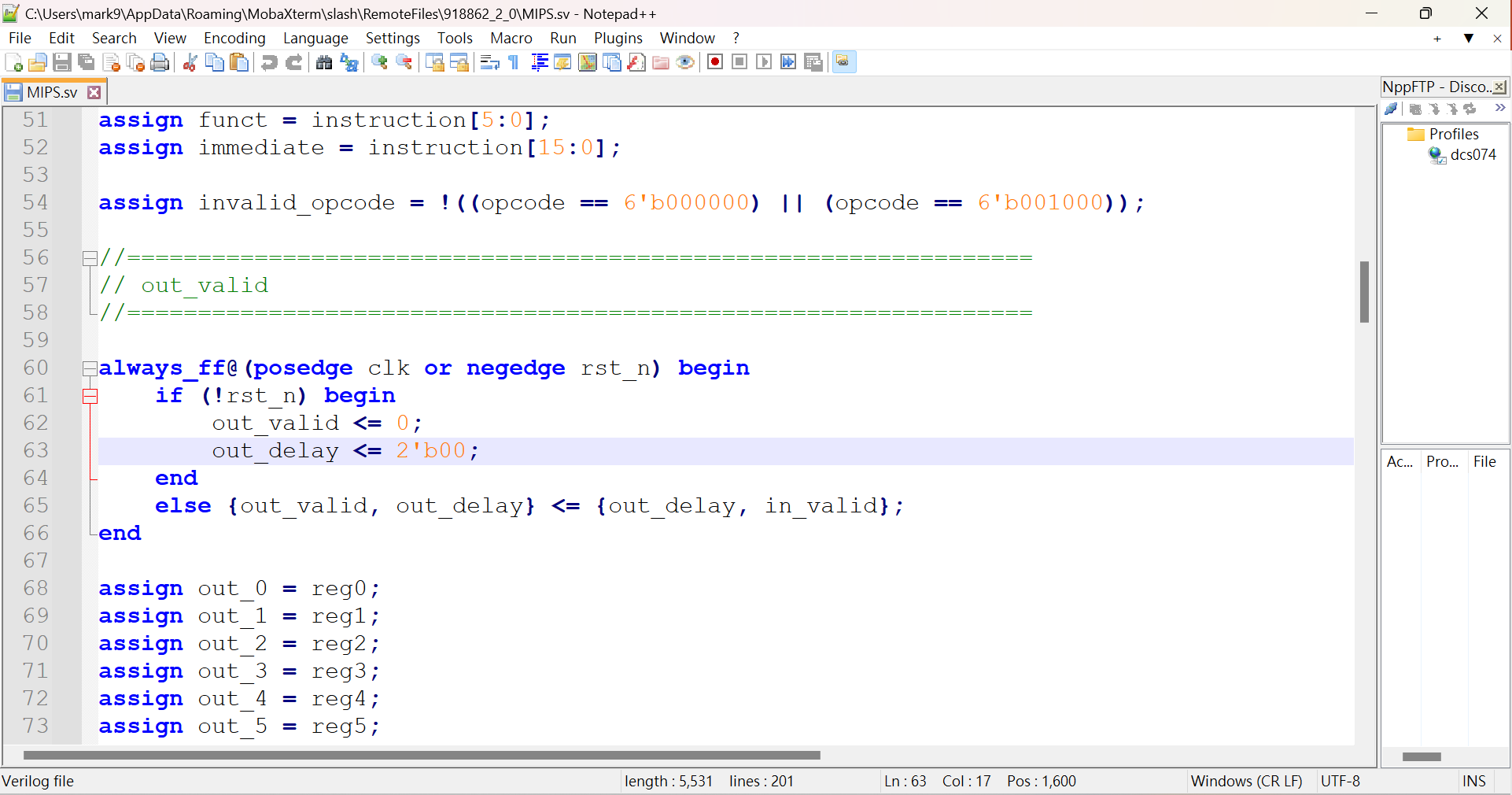
1. Instruction Fetch: Save the input
2. Register Read: Acquire the register values using their addresses
3. Execution: Execute the operation designated by “funct”.
4. Write Back: Write the computed value back to the register designated by “rd”

# Area & Timing Optimization:

This homework is an advanced version of HW1. “out\_valid” must be pulled high in 1.5 cycles after the arrival of the 1st input. Otherwise, “reg\_0” to “reg\_5” will lag behind and the following input addresses will fetch the wrong value. An earlier version of my code took 2.5 cycles to update the registers’ values. That would pass the 10 provided test data. However, when provided with the additional test data I created, it failed.



To control the delay of the output I used a 1-bit reg, “out\_delay” in the following way:



I realized that the problem was that I had a redundant DFF stage. After removing it, the new code now outputs within 1.5 cycles and can pass all test data.