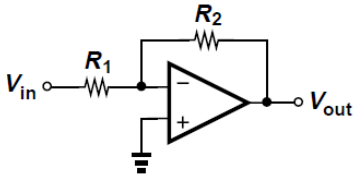
Chapter 13: Introduction to Switched-Capacitor Circuits

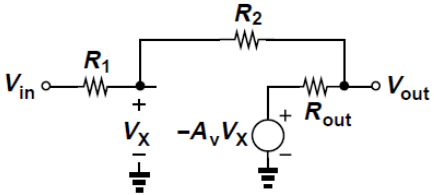
General Considerations



(a)

- For continuous-time amplifier [Fig. (a)], *Vout/Vin = -R2/R1* ideally
- Difficult to implement in CMOS technology
- Typically, open-loop output resistance of CMOS op-amps is maximized to maximize *Av*
- *R2* heavily drops open-loop gain, affecting precision

General Considerations



(b)

- **In equivalent circuit of Fig. (b), we can write**

$$-A_v\left(\frac{V_{out}-V_{in}}{R_1+R_2}R_1+V_{in}\right)-R_{out}\frac{V_{out}-V_{in}}{R_1+R_2}=V_{out}$$

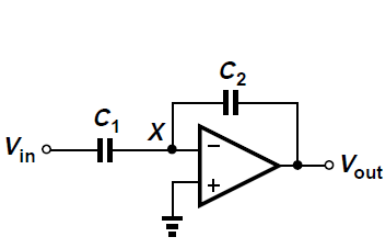
- **Hence,**

$$\frac{V_{out}}{V_{in}}=-\frac{R_2}{R_1}\cdot\frac{A_v-\dfrac{R_{out}}{R_2}}{1+\dfrac{R_{out}}{R_1}+A_v+\dfrac{R_2}{R_1}}$$

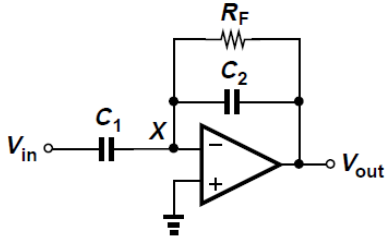
- **Closed-loop ga... is inaccurate compared to when *Rout = 0***

General Considerations

- To reduce open-loop gain, resistors can be replaced by capacitors [Fig. (a)]
- Gain of this circuit is ideally $-C1/C2$
- To set bias voltage at node X, large feedback resistor can be added [Fig. (b)]



(a)



(b)

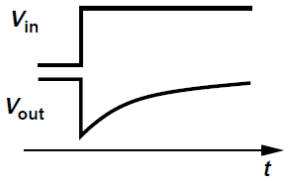
General Considerations

- **Feedback resistor is not suited to amplify wideband signals**
- **Charge on *C2* is lost through *RF* resulting in "tail"**
- **Circuit exhibits high-pass transfer function given by**

$$\frac{V_{out}}{V_{in}}(s) \approx -\frac{R_F \dfrac{1}{C_2 s}}{R_F + \dfrac{1}{C_2 s}} \div \frac{1}{C_1 s}$$

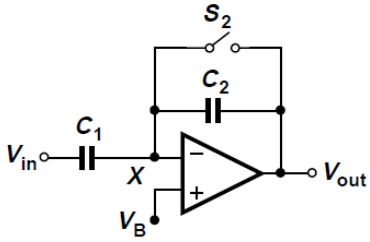
$$= -\frac{R_F C_1 s}{R_F C_2 s + 1},$$

- **Ddd** **only if** $V_{out}/V_{in} \approx -C_1/C_2$ $\omega \gg (R_F C_2)^{-1}$.

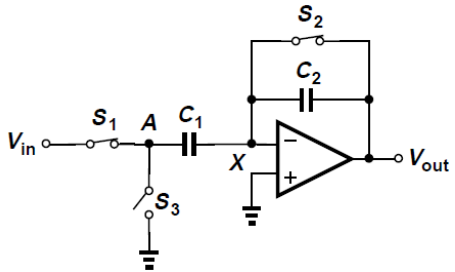


General Considerations

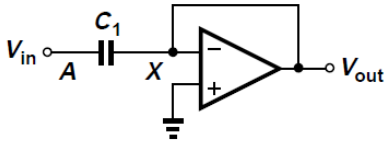
- *RF* can be replaced by a switch
- *S2* is turned on to place op amp in unity gain feedback to force *VX* equal to *VB*, a suitable common-mode value
- When *S2* turns off, node *X* retains the voltage allowing amplification
- When *S2* is on, circuit does not amplify *Vin*



General Considerations

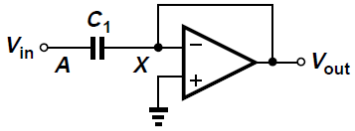


- In above circuit, *S1* and *S3* connect left plate of *C1* to Vin and ground, *S2* for unity-gain feedback
- Assume large open-loop gain of op amp
- First phase: *S1* and *S2* on, *S3* off [Fig. (a)]

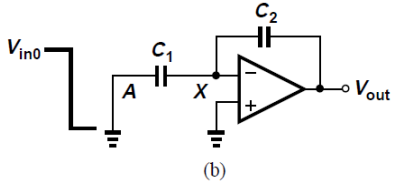


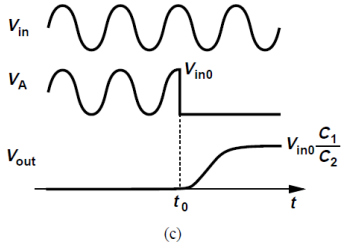
(a)

General Considerations



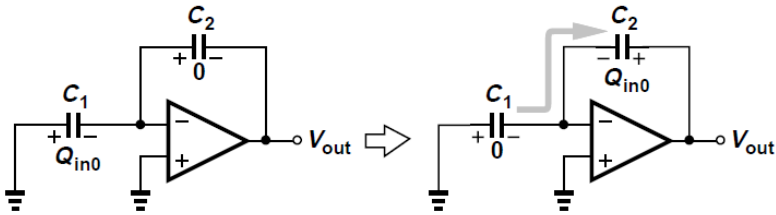
- Here, $V_B = V_{out} \approx 0$ and *C1* samples the input *Vin*
- Second phase: At *t = t0*, *S1* and *S2* turn off and *S3* turns on, pulling node *A* to ground [Fig. (b)]
- *VA* changes from *Vin* to *0*, therefore *Vout* must change from zero to *Vin0C1/C2* [Fig. (c)]





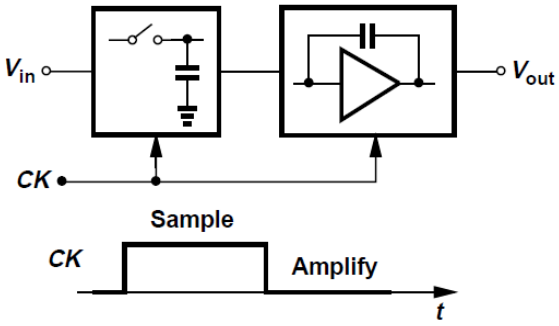
General Considerations

- Circuit devotes some time to sample input, setting output to zero and providing no amplification
- After sampling, for $t > t0$, circuit ignores input voltage, amplifies sampled voltage



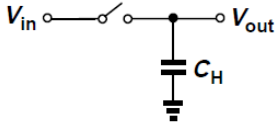
General Considerations

- **Switched-capacitor amplifiers operate in two phases: Sampling and Amplification**
- **Clock needed in addition to analog input *Vin***

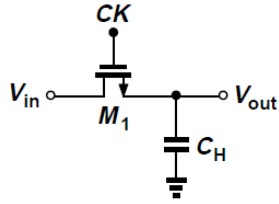


MOSFETS as Switches

- Sampling circuit consists of a switch and a capacitor [Fig. (a)]
- MOS transistor can function as switch [Fig. (b)] since it can be on while carrying zero current

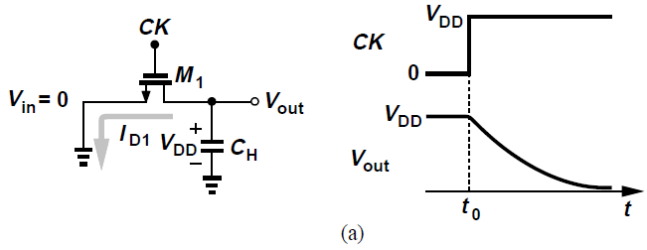


(a)



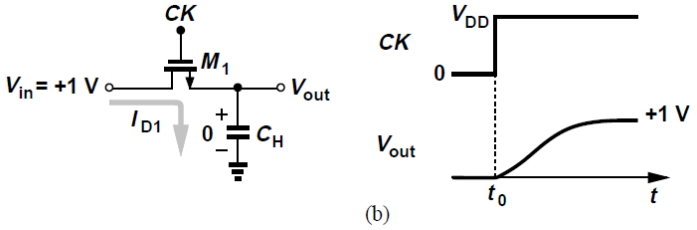
(b)

MOSFETS as Switches



- *CK* goes high at *t = t0*
- Assume *Vin = 0* and capacitor has initial voltage *VDD*
- At *t = t0*, *M1* is in saturation and draws current
- As *Vout* falls, at some point *M1* goes into triode region
- *CH* is discharged until *Vout* reaches zero
- For *Vout << 2(VDD - VTH)*, transistor is an equivalent resistor

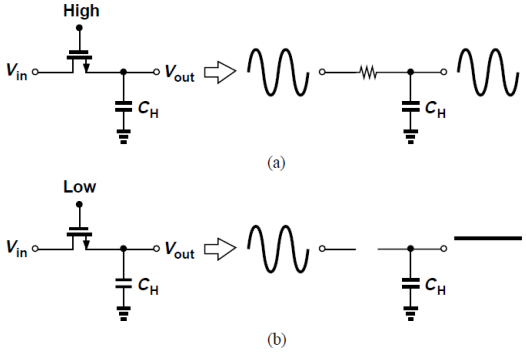
MOSFETS as Switches



- If *Vin = +1 V, Vout(t = t0) = +0 V* and *VDD = +3 V*
- Terminal of *M1* connected to *CH* acts as source, and the transistor turns on with *VGS = +3 V* but *VDS = +1 V*
- *M1* operates in triode region and charges *CH* until Vout approaches *+1 V*
- For *Vout* ≈ *+1 V*, *M1* exhibits an on-resistance of

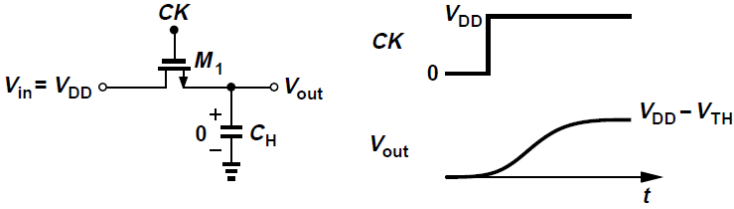
$$R_{on} = [\mu_n C_{ox}(W/L)(V_{DD} - V_{in} - V_{TH})]^{-1}$$

MOSFETS as Switches



- **When switch is on [Fig. (a)], *Vout* follows *Vin***
- **When switch is off [Fig. (b)], *Vout* remains constant**
- **Circuit "tracks" signal when *CK* is high and "freezes" instantaneous value of *Vin* across *CH* when *CK* goes low**

MOSFETS as Switches



- **Suppose *Vin = V0* instead of *+1 V***
- ***M1* is saturated and we have:**

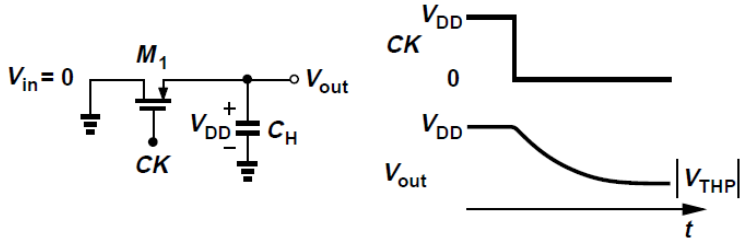
$$C_H \frac{dV_{out}}{dt} = I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_{out} - V_{TH})^2$$

- **Solving,**

$$V_{out} = V_{DD} - V_{TH} - \frac{1}{\frac{1}{2}\mu_n \frac{C_{ox}}{C_H}\frac{W}{L}t + \frac{1}{V_{DD} - V_{TH}}}$$

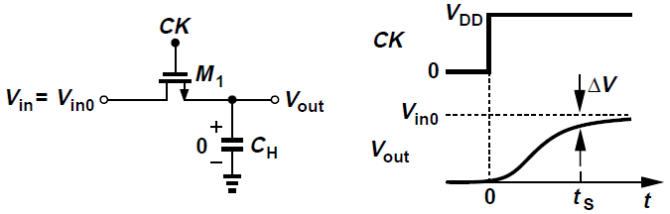
- **As t □ □, *Vout* □ *VDD - VTH* so NMOS cannot pull up to *VDD***

MOSFETS as Switches



- **Similarly, PMOS transistor fails to operate as a switch if gate is grounded and drain senses an input voltage of |*VTHP*| or less**
- **On resistance rises rapidly as input and output levels fall to |*VTHP*| above ground**

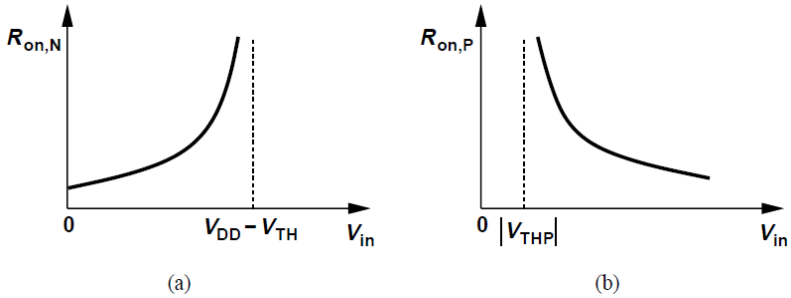
MOSFETS as Switches: Speed Considerations



- **Measure of speed is the time required for output to go from zero to the maximum input level after switch turns on**
- **Consider output settled within a certain "error band" *ΔV* around final value**
- **If output settles to *0.1%* accuracy after *tS* seconds, then *ΔV/Vin0 = 0.1%***
- **After *t = tS*, consider source and drain voltages to be approximately equal**

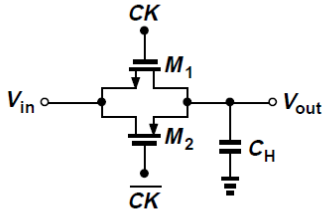
MOSFETS as Switches: Speed Considerations

- Sampling speed is given by two factors: switch on-resistance and sampling capacitance
- For higher speed, large aspect ratio and small capacitance are needed
- On-resistance also depends on input level for both NMOS and PMOS

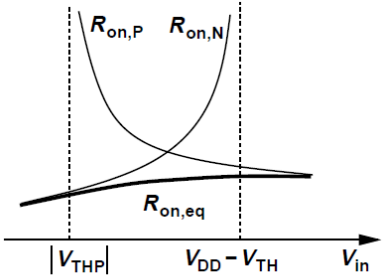


MOSFETS as Switches: Speed Considerations

- To allow greater input swings, we can use "complementary" switches, requiring complementary clocks [Fig. (a)]
- Equivalent on-resistance shows following behavior [Fig. (b)], revealing much less variation



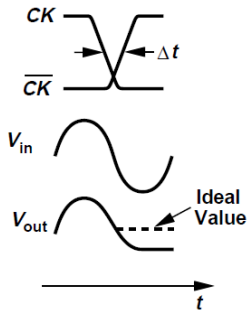
(a)

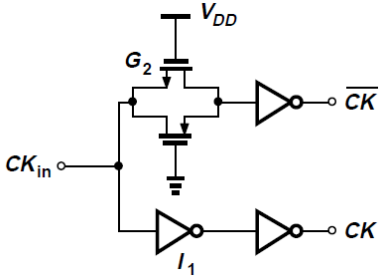


(b)

MOSFETS as Switches: Speed Considerations

- For high speed signals, NMOS and PMOS switches must turn off simultaneously to avoid ambiguity in sampled value
- If NMOS turns off Δt seconds before PMOS, output tends to track input for the remaining Δt seconds, causing distortion
- For moderate precision, circuit below is used to provide complementary clocks

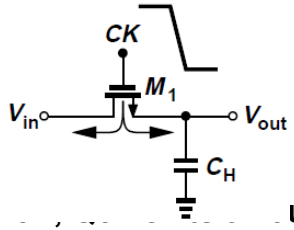




MOSFETS as Switches: Precision Considerations

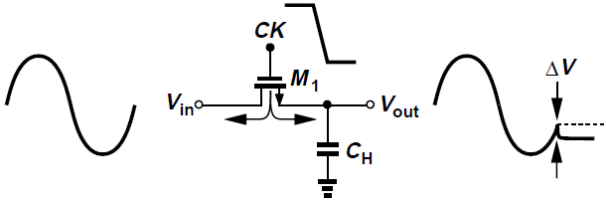
- Speed trades with precision
- Channel Charge Injection:
- For MOSFET to be on, a channel must exist at the oxide-silicon interface
- Assuming *Vin ≈ Vout*, total charge in the inversion layer is

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$



- When switch turn[illegible]ugh the source and drain terminals ("channel charge injection")

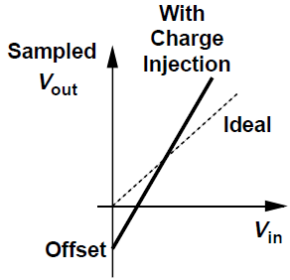
MOSFETS as Switches: Precision Considerations



- **Charge injected to the left is absorbed by input source, creating no error**
- **Charge injected to the right deposited on *CH*, introducing error in voltage stored on capacitor**
- **For half of *Qch* injected onto *CH*, error (negative pedestal) equals**

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H}$$

MOSFETS as Switches: Precision Considerations



- **If all of the charge is deposited on *CH*,**

$$V_{out} \approx V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H}$$

$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) - \frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH})$$

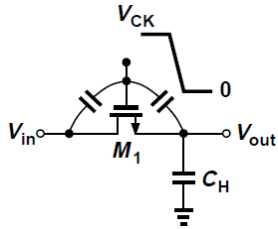
- **Since we assume *Qch* is a linear function of *Vin*, circuit exhibits only gain error and dc offset**

MOSFETS as Switches: Precision Considerations

- **Clock Feedthrough:**
- **MOS switch couples clock transitions through *CGD* or *CGS***
- **Sampled output voltage has error due to this give by**

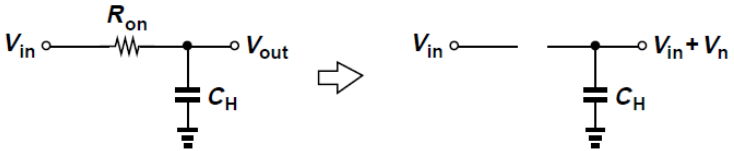
$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov} + C_H}$$

- ***Cov* is the overlap capacitance per unit width**
- **Error *∆V* is independent of input level, manifests as constant offset in the input/output characteristic**

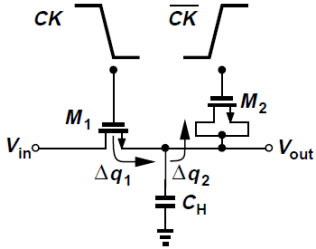


MOSFETS as Switches: Precision Considerations

- **kT/C Noise:**
- **Resistor charging a capacitor gives a total RMS noise voltage of** $\sqrt{kT/C}$
- **On resistance of switch introduces thermal noise at output which is stored on the capacitor when switch turns off**
- **RMS voltage of sampled noise is still approximately equal to** $\sqrt{kT/C}$



Charge Injection Cancellation

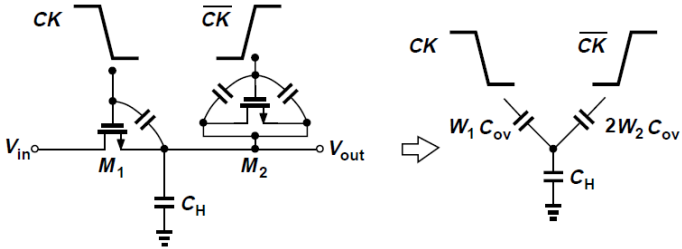


- Charge injected by main transistor removed by a dummy transistor *M2*
- *M2* is driven by $\overline{CK}$ so that after *M1* turns off and *M2* turns on, channel charge deposited by *M1* on *CH* is absorbed by *M2* to create a channel
- If *W2 = 0.5W1*, then charge injected by *M1*, *q1* is equal to that absorbed by *M2*

$$\Delta q_1 = \frac{W_1 L_1 C_{ox}}{2}(V_{CK} - V_{in} - V_{TH1})$$

$$\Delta q_2 = W_2 L_2 C_{ox}(V_{CK} - V_{in} - V_{TH2})$$

Charge Injection Cancellation

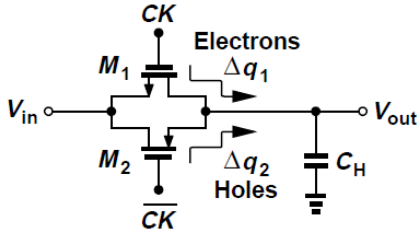


- If *W2 = 0.5W1* and *L2 = L1*, effect of clock feedthrough is suppressed
- Total change in *Vout* is zero because

$$-V_{CK}\frac{W_1C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}}+V_{CK}\frac{2W_2C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}}=0$$

Charge Injection Cancellation

- Incorporate both PMOS and NMOS devices so that opposite charge packets injected cancel each other



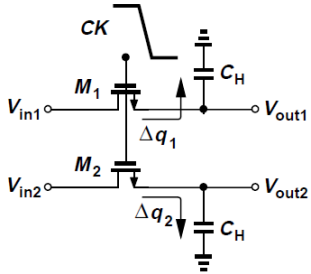
- For *Δq1* to cancel *Δq2*, we must have

$$W_1 L_1 C_{ox}(V_{CK} - V_{in} - V_{THN}) = W_2 L_2 C_{ox}(V_{in} - |V_{THP}|)$$

- Cancellation occurs for only one input level
- Clock feedthrough is not completely suppressed since *CGD* of NFETs is not equal to that PFETs

Charge Injection Cancellation

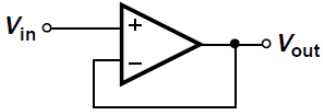
- Charge injection appears as a common-mode disturbance, may be countered by differential operation



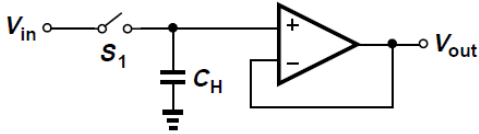
- *Δq1 = Δq2* only if $V_{in1} = V_{in2}$, thus overall error is not suppressed for differential signals
- Removes constant offset and nonlinear component

$$\begin{aligned}\Delta q_1 - \Delta q_2 &= WLC_{ox}[(V_{in2} - V_{in1}) + (V_{TH2} - V_{TH1})] \\ &= WLC_{ox}\left[V_{in2} - V_{in1} + \gamma\left(\sqrt{2\phi_F + V_{in2}} - \sqrt{2\phi_F + V_{in1}}\right)\right]\end{aligned}$$

Unity-Gain Sampler/ Buffer



(a)

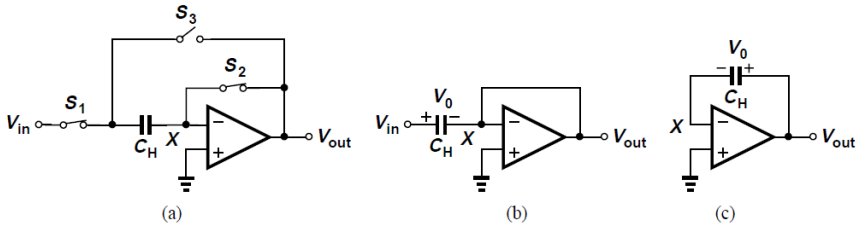


(b)

- For discrete-time applications, unity-gain amplifier [Fig. (a)] requires a sampling circuit [Fig. (b)]
- Accuracy limited by input-dependent charge injected by *S1* onto *CH*

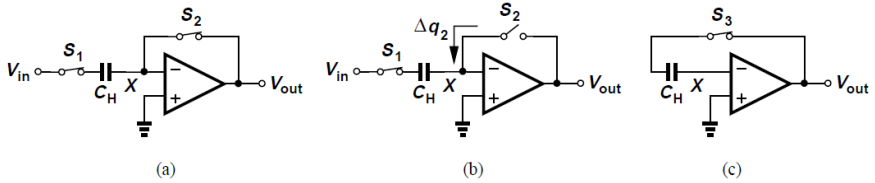
Unity-Gain Sampler/ Buffer

- Consider the topology shown in Fig. (a)

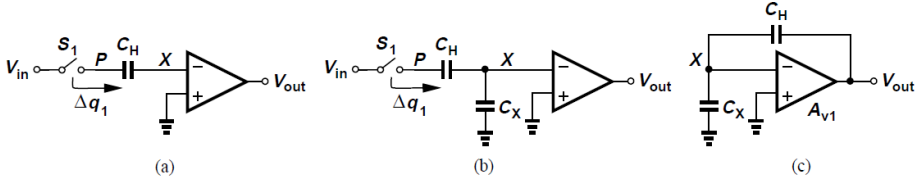


- In sampling mode, S1 and S2 are on, S3 is off yielding circuit in Fig. (b)
- Thus, *Vout = VX ≈ 0*, and the voltage across *CH* tracks *Vin*
- At *t = t0*, when *Vin = V0*, *S1* and *S2* turn off and *S3* turns on, yielding circuit of Fig. (c) [amplification mode]
- Op amp requires node *X* is still a virtual ground, *Vout* rises to approximately *V0* – "frozen" for processing by subsequent stages

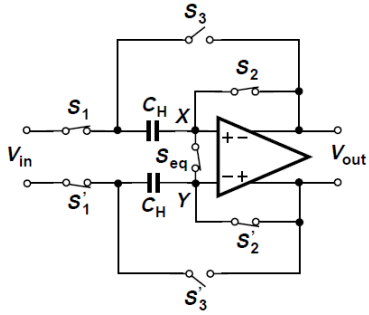
Unity-Gain Sampler/ Buffer



- ***S2* turns off slightly before *S1* during transition from sampling mode to amplification mode**
- **Charge injected by *S2*, *□q2* is input-independent and constant, producing only an offset**
- **After *S2* turns off, total charge at node *X* stays constant and charge injected by *S1* does not affect output voltage**



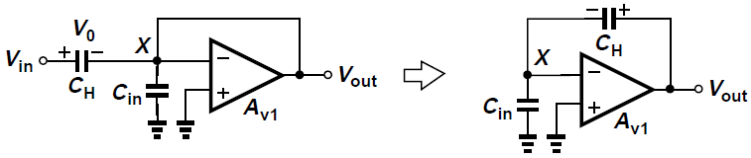
Unity-Gain Sampler/ Buffer



- Input-independent charge injected by *S2* can be cancelled by differential operation as shown
- Charge injected by *S2* and *S2'* appears as common-mode disturbance at nodes *X* and *Y*
- Charge injection mismatch between *S2* and *S2'* resolved by adding another switch *Seq* that turns off slightly after *S2* and *S2'*, equalizing the charge at nodes *X* and *Y*

Unity-Gain Sampler/ Buffer

- **Precision Considerations:**
- **Assume op-amp has a finite input capacitance *Cin* and calculate output voltage when circuit goes from sampling to amplification mode**



- **It can be shown from the above fig. that**

$$V_{out} = \frac{V_0}{1+\frac{1}{A_{v1}}\left(\frac{C_{in}}{C_H}+1\right)}$$

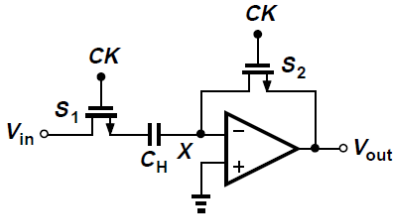
$$\approx V_0\left[1-\frac{1}{A_{v1}}\left(\frac{C_{in}}{C_H}+1\right)\right]$$

- **Circuit suffer kimately**

$$-(C_{in}/C_H+1)/A_{v1}$$

Unity-Gain Sampler/ Buffer

- **Speed Considerations:**
- **In sampling mode, circuit appears as in Fig. (a)**



- **Use equivalent circuit of Fig. (b) to find time constant in sampling mode**
- **Total resistance in series with *CH* is *Ron1* and the resistance between *X* and ground, *RX***

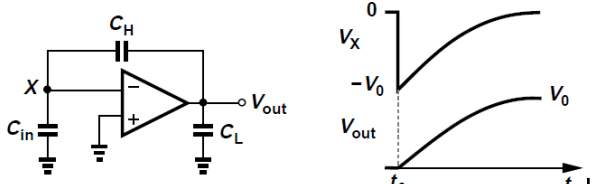
$$R_X = \frac{R_0 + R_{on2}}{1 + G_m R_0}$$

Unity-Gain Sampler/ Buffer

- **Since typically** $R_{on2} \ll R_0$ **and** $G_m R_0 \gg 1$, $R_X \approx 1/G_m$
- **Time constant in sampling mode is thus**

$$\tau_{sam} = \left(R_{on1} + \frac{1}{G_m} \right) C_H$$

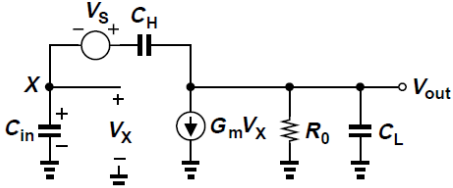
- **Consider circuit as it enters amplification mode**



- **Circuit must begin with Vout = 0 and eventually produce *Vout* ≈ *V0***
- **For relatively small *Cin*, voltages across *CL* and *CH* do not change instantaneously so that *VX* = *-V0* at the beginning of amplification**

Unity-Gain Sampler/ Buffer

- Represent charge on *CH* by a voltage source *VS* that goes from zero to *V0* at *t = t0*, while *CH* carries no charge itself



- The transfer function $V_{out}(s)/V_{in}(s)$ can be obtained as

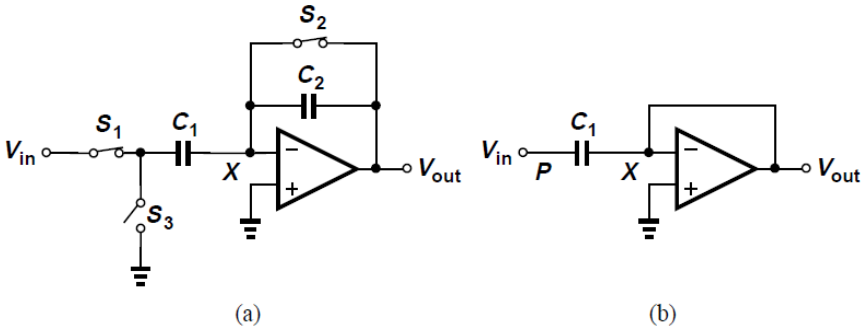
$$\frac{V_{out}}{V_S}(s) = \frac{(G_m + C_{in}s)C_H}{(C_L C_{in} + C_{in}C_H + C_H C_L)s + G_m C_H}$$

- This response is characterized by a time constant independent of op-amp output resistance

$$\begin{aligned} \tau_{amp} &= \frac{C_L C_{in} + C_{in}C_H + C_H C_L}{G_m C_H} \\ &= \frac{1}{G_m}\left[C_{in} + \left(1 + \frac{C_{in}}{C_H}\right) C_L\right] \end{aligned}$$

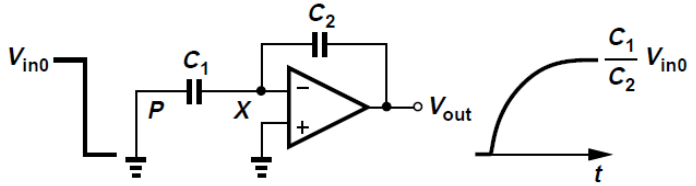
Noninverting Amplifier

- **In non-inverting amplifier of Fig. (a), in sampling mode, *S1* and *S2* are on while *S3* is off, creating a virtual ground at *X* and allowing voltage across *C1* to track *Vin* [Fig. (b)]**



Noninverting Amplifier

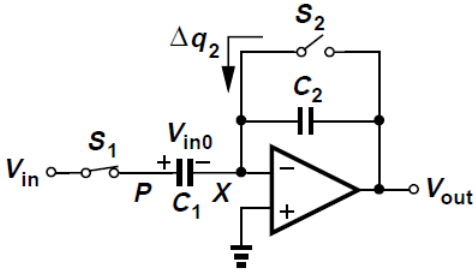
- At the end of sampling mode, *S2* turns off first, injecting a constant charge *−q2* onto node *X*, after which *S1* turns off and *S3* turns on [Fig. (c)]
- Since *VP* goes from *Vin0* to *0*, output voltage changes from 0 to approximately *Vin0(C1/C2)*, providing a gain of *C1/C2*
- Called a "noninverting amplifier" since output polarity is the same as *Vin0* and the gain can be greater than unity



(c)

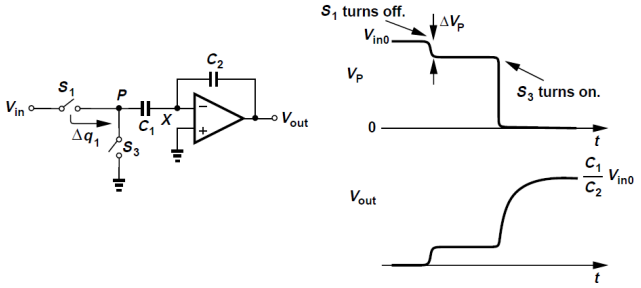
Noninverting Amplifier

- **Noninverting amplifier avoids input-depending charge injection by turning off *S2* before *S1***
- **After *S2* is off, total charge at node *X* remains constant, making the circuit insensitive to charge injection of *S1* or charge "absorption" of *S3***



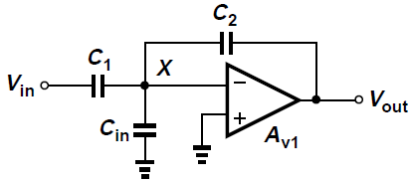
Noninverting Amplifier

- Charge injected by *S1*, *□q1* changes voltage at node *P* by *□VP = □q1/C1* and output voltage by *-□q1C1/C2*
- After *S3* turns on, *VP* becomes zero so overall change in *VP* is *0 – Vin0 = -Vin0*, producing overall change in output of *–Vin0(-C1/C2) = Vin0C1/C2*
- *VP* goes from *V0* to *0* with a perturbation due to *S1*
- Since output is measure after node *P* is connected to ground, charge injected by *S1* does not affect final output



Noninverting Amplifier

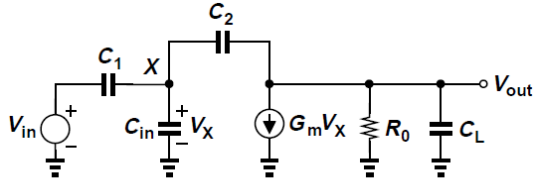
- **Precision Considerations:**
- **Calculate actual gain if op amp has finite open-loop gain of *Av1* and input capacitance *Cin***



- **It can be sh** $\left|\frac{V_{out}}{V_{in}}\right| \approx \frac{C_1}{C_2}\left(1 - \frac{C_2 + C_1 + C_{in}}{C_2} \cdot \frac{1}{A_{v1}}\right)$
- $(C_2 + C_1 + C_{in})/(C_2 A_{v1})$ **a gain error of**
- **Gain error increases with the nominal gain *C1/C2***

Noninverting Amplifier

- **Speed Considerations:**
- **Consider equivalent circuit in amplification mode [Fig. (a)]**



(a)

- **It can be shown for a large $G_m R_0$ that**

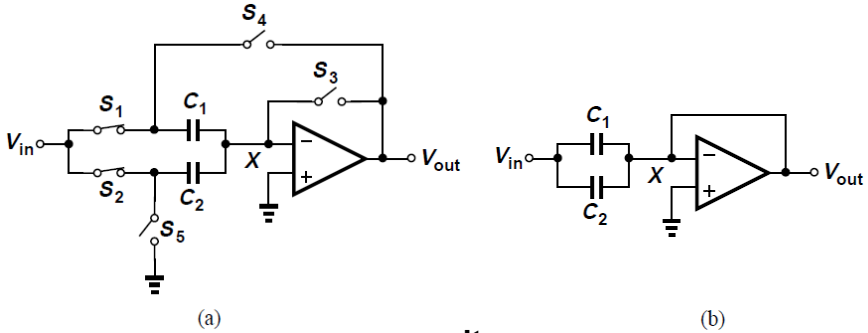
$$\frac{V_{out}}{V_{in}}(s) \approx \frac{-C_{eq}\dfrac{C_1}{C_1 + C_{in}}(G_m - C_2 s)R_0}{R_0(C_L C_{eq} + C_L C_2 + C_{eq} C_2)s + G_m R_0 C_2}$$

- **This give**

$$\tau_{amp} = \frac{C_L C_{eq} + C_L C_2 + C_{eq} C_2}{G_m C_2}$$

Precision Multiply-by-Two Circuit

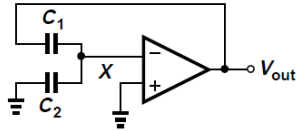
- Topology shown in Fig. (a) provides a nominal gain of two while achieving higher speed and lower gain error



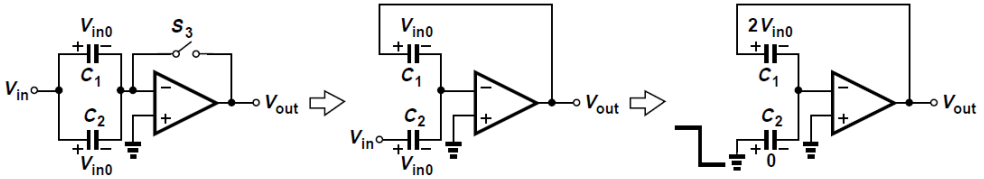
- Incorporates two equal capacitors ***C1 = C2 = C***
- In sampling mode [Fig. (b)], node ***X*** is a virtual ground, allowing voltage across ***C1*** and ***C2*** to track ***Vin***

Precision Multiply-by-Two Circuit

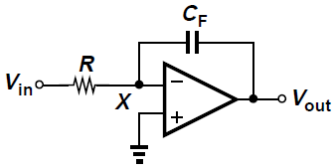
- During transition to amplification mode [Fig. (c)], *S3* turns off first, placing *C1* around op-amp and left plate of *C2* is grounded
- At the moment *S3* turns off, total charge on *C1* and *C2* equals *2Vin0C* and since voltage across *C2* approaches zero in amplification mode, final voltage across *C1* and hence output are approximately *2Vin0*



(c)

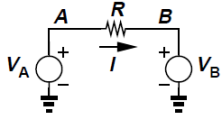


Switched-Capacitor Integrator

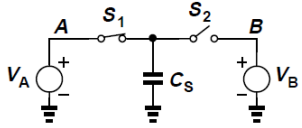


- **Output of a continuous-time integrator can be expressed as**

$$V_{out} = -\frac{1}{RC_F}\int V_{in}dt$$



(a)

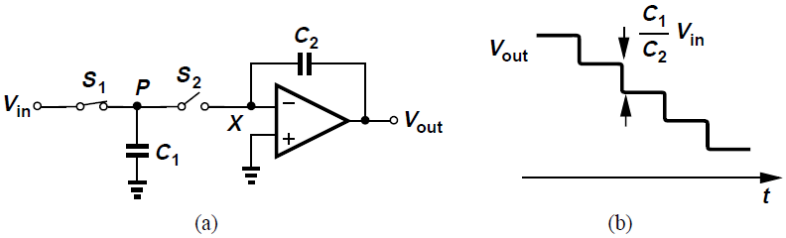


(b)

- **In Fig. (a), resistor *R* carries a current of *(VA – VB)/R***
- **In circuit of Fig. (b), *CS* is alternately connected to nodes *A* and *B* at a clock rate *fCK***
- **Average current flowing from *A* to *B* is the charge moved in one clock period**
- **Can be viewed as a resistor of value** $(C_S f_{CK})^{-1}$

$$\begin{aligned}\overline{I_{AB}} &= \frac{C_S(V_A - V_B)}{f_{CK}^{-1}} \\ &= C_S f_{CK}(V_A - V_B)\end{aligned}$$

Switched-Capacitor Integrator

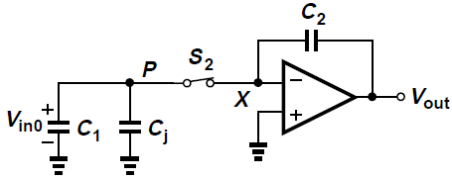


- **Fig. (a) shows discrete-time integrator**
- **In every clock cycle, *C1* absorbs a charge equal to *C1Vin* when *S1* is on and deposits it on *C2* when *S2* is on**
- **If *Vin* is constant, output changes by *VinC1/C2* every clock cycle [Fig. (b)]**
- **Final value of *Vout* after clock cycle can be written as**

$$V_{out}(kT_{CK}) = V_{out}[(k-1)T_{CK}] - V_{in}[(k-1)T_{CK}] \cdot \frac{C_1}{C_2}$$

Switched-Capacitor Integrator

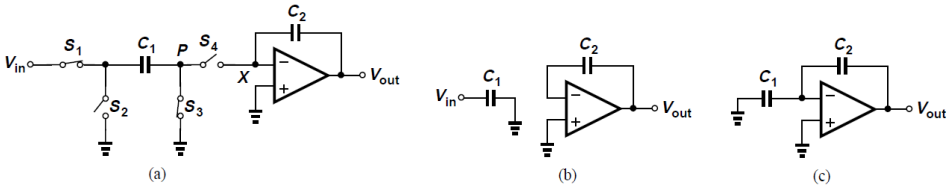
- Input-dependent charge injection of *S1* introduces nonlinearity in output voltage
- Nonlinear capacitance at node *P* resulting from source/drain junctions of *S1* and *S2* leads to a nonlinear charge-to-voltage conversion when *C1* is switched to *X*



- Charge stored on the total junction capacitance, *Cj* is not equal to *Vin0Cj*, but rather equal to

$$q_{cj} = \int_0^{Vin0} C_j dV.$$

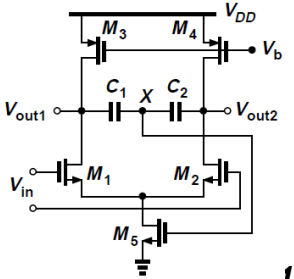
Switched-Capacitor Integrator



- **Circuit of Fig. (a) resolves the issues in the simple integrator**
- **In sampling mode [Fig. (b)], *S1* and *S3* are on, *S2* and *S4* are off, allowing voltage across *C1* to track *Vin* while op amp and *C2* hold previous value**
- **In the transition to integration mode, *S3* turns off first, injecting a constant charge onto *C1*, *S1* turns off next, and subsequently *S2* and *S4* turn on**
- **Charge stored on *C1* is transferred to *C2* through the virtual ground node**

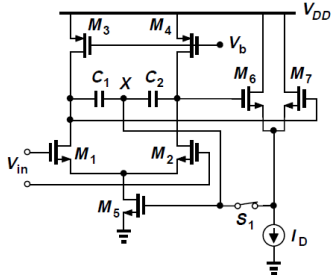
Switched-Capacitor Common-Mode Feedback

- In switched-capacitor common-mode feedback, outputs are sensed by capacitors rather than resistors



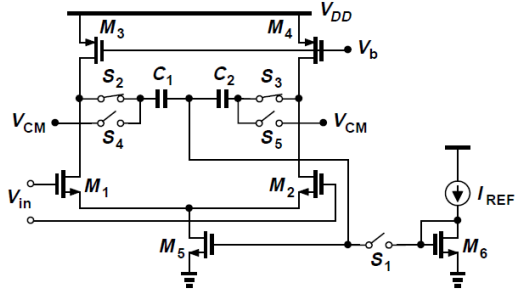
- In circuit above, equal capacitors *C1* and *C2* reproduce at node *X* the average of the changes in each output voltage
- If *Vout1* and *Vout2* experience a positive CM change, then *VX* and *ID5* increase, pulling *Vout1* and *Vout2* down
- Output CM is *VGS2* plus voltage across *C1* and *C2*

Switched-Capacitor Common-Mode Feedback



- Voltage across *C1* and *C2* defined as shown above
- During CM level definition, amplifier differential input is zero and *S1* is on
- *M6* and *M7* act as a linear sense circuit since their gate voltages are nominally equal
- Circuit settles such that output CM level is equal to *VGS6,7 + VGS5*
- At the end of this mode, *S1* turns off, leaving a voltage equal to *VGS6,7* across *C1* and *C2*

Switched-Capacitor Common-Mode Feedback



- For more accuracy in CM level definition, above circuit may be used
- In the reset mode, one plate of *C1* and *C2* is switched to *VCM* while the other is connected to the gate of *M6*
- Each capacitor sustains a voltage of *VCM – VGS6*
- In the amplification mode, *S2* and *S3* are on and the other switches are off, yielding an output CM level of *VCM – VGS6 + VGS5*, which is equal to *VCM* if *ID3* and *ID4* are copied properly from *IREF* so that *VGS5 = VGS6*