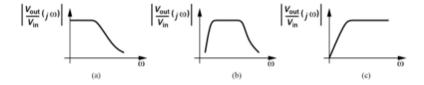
Chapter 6: Frequency Response of Amplifiers

- 6.1 Basic Current Mirrors
- 6.2 Common-Source Stage
- 6.3 Source Followers
- 6.4 Common-Gate Stage
- 6.5 Cascode Stage
- 6.6 Differential Pair
- 6.7 Gain-Bandwidth Trade-Offs

General Considerations



- In this chapter, we are primarily interested in the magnitude of the transfer function.
- The magnitude of a complex number a + jb is given by $\sqrt{a^2+b^2}$
- Zeros and poles are respectively defined as the roots of the numerator and denominator of the transfer function.

Miller effect

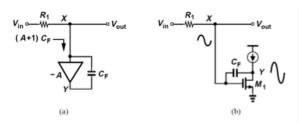


 If the circuit of Fig (a) can be converted to that of Fig (b), then

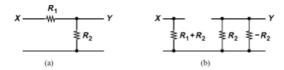
$$Z_1 = Z/(1 - A_v)$$

$$Z_2 = Z/(1 - A_v^{-1})$$

$$A_v = V_Y/V_X$$



- A student needs a large Capacitor and decides to utilize the Miller multiplication
- · What is the issues in this approach?

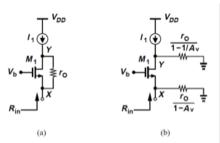


Improper application of Miller's theorem



Typical case for valid application of Miller's theorem.

- Miller's theorem does not stipulate the conditions under which this conversion is valid.
- If the impedance Z forms the only signal path between X and Y, then the conversion is often invalid.



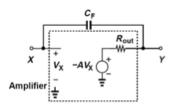
- Calculate the input resistance of the circuit shown.
- Since Av is usually greater than unity, $r_O/(1-A_v)$ is a negative resistance.

• Av =
$$1 + (g_m + g_{mb})r_O$$

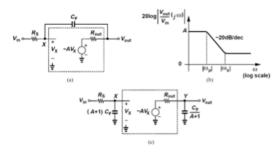
$$R_{in} = \frac{r_O}{1 - [1 + (g_m + g_{mb})r_O]} \Big\| \frac{1}{g_m + g_{mb}}$$

$$= \frac{-1}{g_m + g_{mb}} \Big\| \frac{1}{g_m + g_{mb}}$$

$$= \infty.$$



- The value of Av = VY / VX must be calculated at the frequency of interest.
- In the figure, the equivalent circuit_{VY} ≠ -AV_Xthat at high frequencies.
- In many cases we use the low-frequency value of VY / VX to gain insight.
- · We call this approach "Miller's approximation."



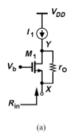
Direct Calculation:

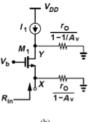
$$\frac{V_{out}}{V_{in}}(s) = \frac{R_{out}C_F s - A}{[(A+1)R_S + R_{out}]C_F s + 1}$$

Miller Aproximation:

$$\frac{V_{out}}{V_{in}}(s) = \frac{-A}{[(1+A)R_SC_Fs+1](\frac{1}{1+A^{-1}}C_FR_{out}s+1)}$$

 Miller's approximation has eliminated the zero and predicted two poles for the circuit!





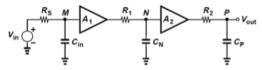
$$R_{out} = \frac{r_O}{1 - 1/A_v}$$

$$= \frac{r_O}{1 - [1 + (g_m + g_{mb})r_O]^{-1}}$$

$$= \frac{1}{1 - [1 + (g_m + g_{mb})r_O]^{-1}}$$

- Actual Rout =r0
- Miller's approximation:
- (1) it may eliminate zeros
- (2) it may predict additional poles
- (3) it does not correctly compute the "output" impedance.

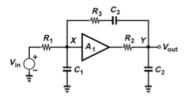
Association of Poles with Nodes

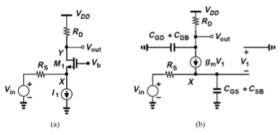


The overall transfer function can be written as

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_1}{1 + R_S C_{in} s} \cdot \frac{A_2}{1 + R_1 C_{NS}} \cdot \frac{1}{1 + R_2 C_{PS}}$$

- Each node in the circuit contributes one pole to the transfer function.
- Not valid in general. Example:





At node X:

$$\omega_{in} = \left[\left(C_{GS} + C_{SB} \right) \left(R_S \left\| \frac{1}{g_m + g_{mb}} \right) \right]^{-1}$$

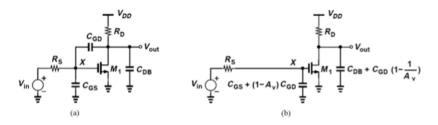
At node Y:

$$\omega_{out} = [(C_{DG} + C_{DB})R_D]^{-1}$$

• The overall trancilling....

$$\frac{V_{out}}{V_{in}}(s) = \frac{(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S} \cdot \frac{1}{\left(1 + \frac{s}{\omega_{in}}\right)\left(1 + \frac{s}{\omega_{out}}\right)}$$

Common-Source Stage



The magnitude of the "input" pole

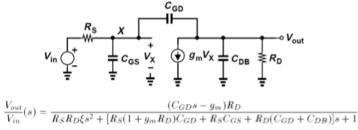
$$\omega_{in} = \frac{1}{R_S[C_{GS} + (1+g_mR_D)C_{GD}]}$$

At the output node

$$\omega_{out} = \frac{1}{R_D(C_{DB} + C_{GD})}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{-g_m R_D}{\left(1 + \frac{s}{\omega_{in}}\right) \left(1 + \frac{s}{\omega_{out}}\right)}$$

Direct Analysis

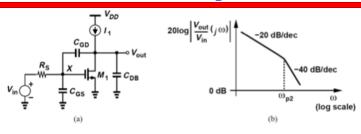


$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{R_S R_D \xi s^2 + [R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})]s + 1}$$

- While the denominator appears rather complicated, it can yield intuitive expressions for the two poles. $|\omega_{v1}| \ll |\omega_{v2}|$
- "Dominant pole" approximation.

$$\omega_{p1} = \frac{1}{R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})}$$

The intuitive approach provides a rough estimate with much less effort.



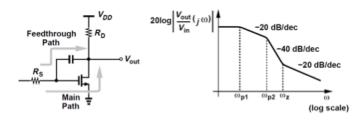
$$\begin{split} \frac{V_{out}}{V_{in}}(s) &= \frac{C_{GD}s - g_m}{R_S\xi s^2 + [g_mR_SC_{GD} + (C_{GD} + C_{DB})]s} \\ &= \frac{C_{GD}s - g_m}{s[R_S(C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB})s + (g_mR_S + 1)C_{GD} + C_{DB}]} \end{split}$$

- One pole is at the origin because the dc gain is infinity.
- For a large CDB or load capacitance

$$\omega_{p2} \approx \frac{1}{R_S(C_{GS} + C_{GD})}$$

No miller multiplication. Why?

Zero in Transfer Function



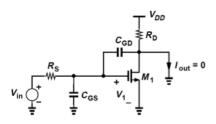
$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{R_SR_D\xi s^2 + [R_S(1 + g_mR_D)C_{GD} + R_SC_{GS} + R_D(C_{GD} + C_{DB})]s + 1}$$

The transfer function of exhibits a zero given by

$$\omega_z = +g_m/C_{GD}$$

 CGD provides a feedthrough path that conducts the input signal to the output at very high frequencies.

Calculating zero in a CS stage

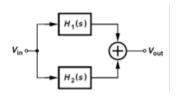


- The transfer function Vout(s)=Vin(s) must drop to zero for s = sz.
- Therefore, the currents through C_{GD} and M1 are equal and opposite:

$$V_1C_{GD}s_z = g_mV_1$$

That is

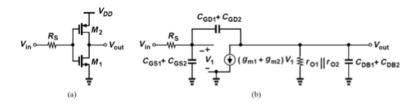
$$s_z = +g_m/C_{GD}$$



- Can this (the zero) occur if H1(s) and H2(s) are first-order low-pass circuits?
- H1= $A_1/(1+s/\omega_{p1})$ and H2= $A_2/(1+s/\omega_{p2})$

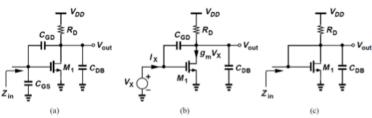
$$\frac{V_{out}}{V_{in}}(s) = \frac{(\frac{A_1}{\omega_{p2}} + \frac{A_2}{\omega_{p1}})s + A_1 + A_2}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$

· The overall transfer function contains a zero.



- Since the corresponding terminals ofM1 and M2 are shorted to one another in the small-signal model, we merge the two transistors.
- The circuit thus has the same transfer function as the simple CS stage.

Miller's Approximation



With the aid of Miller's approximation,

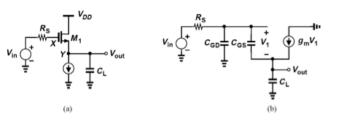
$$Z_{in} = \frac{1}{[C_{GS} + (1 + g_m R_D)C_{GD}]s}$$

- But at high frequencies, the effect of the output node capacitance must be taken into account.
- Ignore Cgs

$$\frac{V_X}{I_X} = \frac{1 + R_D(C_{GD} + C_{DB})s}{C_{GD}s(1 + q_m R_D + R_D C_{DB}s)}$$

 if CgD is large, it provides a low impedance path between the gate and drain of M1.

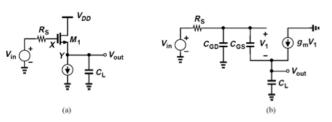
Source Followers



 The strong interaction between nodesX and Y through Cos in makes it difficult to associate a pole with each node.

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m + C_{GS}s}{R_S(C_{GS}C_L + C_{GS}C_{GD} + C_{GD}C_L)s^2 + (g_mR_SC_{GD} + C_L + C_{GS})s + g_m}$$

· Contains a zero in the left half plane. Why?

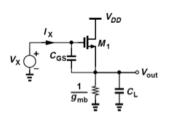


Transfer function if CL = 0?

$$\begin{split} \frac{V_{out}}{V_{in}} &= \frac{g_m + C_{GS}s}{R_S C_{GS} C_{GD} s^2 + (g_m R_S C_{GD} + C_{GS})s + g_m} \\ &= \frac{g_m + C_{GS}s}{(1 + R_S C_{GD}s)(g_m + C_{GS}s)} \\ &= \frac{1}{1 + R_S C_{GD}s}. \end{split}$$

- C_{GS} disappear
- In the absence of channel-length modulation and body effect, the voltage gain from the gate to the source is equal to unity.

Input impedance



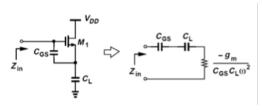
C_{GD} simply shunts the input and can be ignored initially.

 $Z_{in} = \frac{1}{C_{GS}s} + \left(1 + \frac{g_m}{C_{GS}s}\right) \frac{1}{g_{mb} + C_L s}$

- If gmb = 0 and CL = 0, then Zin = ∞
- Cgs is entirely bootstrapped by the source follower and draws no current from the input.
- At Low frequency the overall input capacitance is equal to CgD plus a fraction of Cgs.

$$Z_{in} \approx \frac{1}{C_{GS}s} \left(1 + \frac{g_m}{g_{mb}} \right) + \frac{1}{g_{mb}}$$

Input Impedance

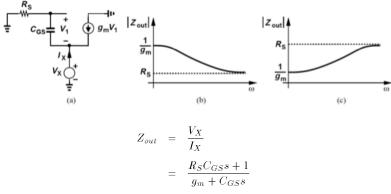


• At high frequencies, $g_{mb} \ll |C_L s|$

$$Z_{in} \approx \frac{1}{C_{GS}s} + \frac{1}{C_{L}s} + \frac{g_m}{C_{GS}C_{L}s^2}$$

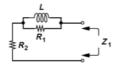
 A source follower driving a load capacitance exhibits a negative input resistance, possibly causing instability.

Output Impedance



- At low frequency: $Z_{out} \approx 1/g_m$
- At very high frequencies, $Z_{out} \approx R_S$
- Because Cgs shorts the gate and the source.
- Which one of these variations is more realistic?

Output Impedance

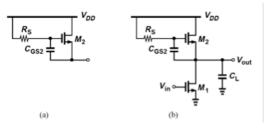


- Equivalent output impedance of a source follower
- Since the output impedance increases with frequency, we postulate that it contains an inductive component.

$$Z_{out} - \frac{1}{g_m} = \frac{C_{GS}s\left(R_S - \frac{1}{g_m}\right)}{g_m + C_{GS}s}$$

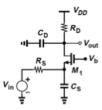
$$\frac{1}{Z_{out} - \frac{1}{g_m}} = \frac{1}{R_S - \frac{1}{g_m}} + \frac{1}{\frac{C_{GS}s}{g_m}\left(R_S - \frac{1}{g_m}\right)}$$

$$L = \frac{C_{GS}}{g_m}\left(R_S - \frac{1}{g_m}\right)$$



- Can we construct a (two-terminal) inductor from a source follower?
- Yes, but non-ideal.
- It also incurs a parallel resistance and a series resistance.
- The inductance can partially cancel the load capacitance, CL, at high frequencies, thus extending the bandwidth.

Common-Gate Stage

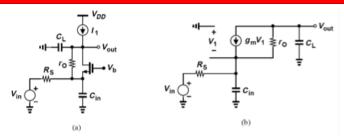


Common-gate stage at high frequencies

A transfer function

$$\frac{V_{out}}{V_{in}}(s) = \frac{(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S} \frac{1}{\left(1 + \frac{C_S}{q_m + q_{mb} + R_{\overline{\phi}}^{-1}} s\right)(1 + R_D C_D s)}$$

- No Miller multiplication of capacitances.
- RD is typically maximized, so the dc level of the input signal must be quite low.
- As an amplifier in cases where a low input impedance is required
- In cascode stages.

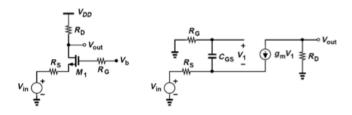


 Why Zin becomes independent of C_L as this capacitance increases?

$$Z_{in} = \frac{1}{g_m + g_{mb}} + \frac{1}{C_L s} \cdot \frac{1}{(g_m + g_{mb})r_O}. \label{eq:Zin}$$

- As C_L or s increases, Zin approaches 1/(gm + gmb)
- CL lowers the voltage gain of the circuit, thereby suppressing the effect of the negative resistance introduced by Miller effect through rO.

CG Stage

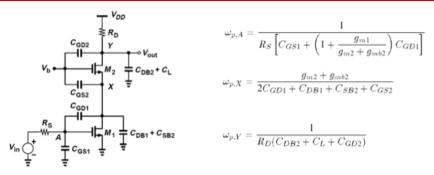


- The bias network providing the gate voltage exhibits a finite impedance.
- · Consider only Cgs here.

$$\begin{split} \frac{V_{out}}{V_{in}} &= \frac{g_m R_D}{(R_G + R_S) C_{GS} s + 1 + g_m R_S}, \\ \omega_p &= \frac{1 + g_m R_S}{(R_G + R_S) C_{GS}}. \end{split}$$

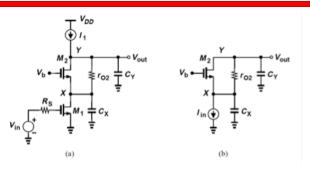
- Lowering the pole magnitude.
- Output impedance of the circuit drops at high frequencies.

Cascode Stage



High-frequency model of a cascode stage.

- Miller effect is less significant in cascode amplifiers than in common-source stages.
- But $\omega_{p,X}$ is typically quite higher than the other two.
- What if RD is replaced by a current source?
- Pole at node X may be quite lower, but transfer function will not affect much by this. See example.



Compute the transfer function.

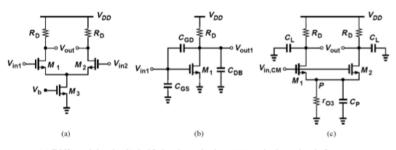
$$\frac{V_{out}}{I_{in}} = -\frac{g_{m2}r_{O2} + 1}{C_X s} \cdot \frac{1}{1 + (1 + g_{m2}r_{O2})\frac{C_Y}{C_X} + C_Y r_{O2} s}$$

For $g_{m2}r_{O2}\gg 1$

$$\frac{V_{out}}{g_{out}} = -\frac{g_{m1}g_{m2}}{g_{m2}}$$

• The magnitu $\frac{V_{out}}{V_{in}} = -\frac{g_{m1}g_{m2}}{C_YC_Xs} \frac{1}{g_{m2}/C_X + s}$ node X is still given by gm2/Cx. Why?

Differential Pair

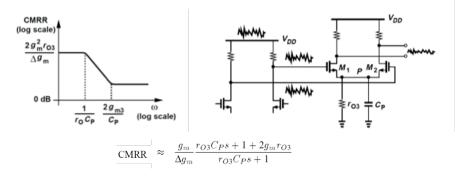


- (a) Differential pair, (b) half-circuit equivalent, (c) equivalent circuit for common-mode inputs.
- For differential signals, the response is identical to that of a common-source stage.
- the common-mode rejection of the circuit degrades considerably at high frequencies.

$$A_{v,CM} = -rac{\Delta g_m \left[R_D \middle\| \left(rac{1}{C_L s}
ight)
ight]}{\left(g_{m1} + g_{m2}
ight) \left\lceil r_{O3} \middle\| \left(rac{1}{C_P s}
ight)
ight
ceil + 1}$$

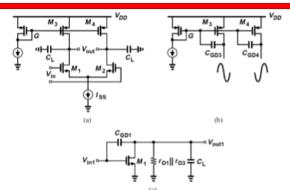
• Channel of the capacitances are neglected.

Differential Pair



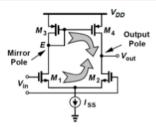
- This transfer function contains a zero and a pole.
- The magnitude of the zero is much greater than the pole.
- Common-mode disturbance at node P translates to a differential noise component at the output, if the supply voltage contains high-frequency noise and the circuit exhibits mismatches.
- Trade-off between voltage headroom and CMRR.

Diff Pair



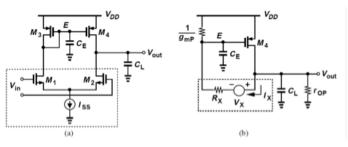
- Frequency response of differential pairs with high-impedance loads.
- Fig (b) CGD3 and CGD4 conduct equal and opposite currents to node G, making this node an ac ground.
- The differential half circuit is depicted in Fig. (c).
- More on chapter 10

Differential Pair with Active Load



- How many poles does this circuit have?
- The severe trade-off between gm and CGS of PMOS devices results in a pole that impacts the performance of the circuit.
- The pole associated with node E is called a "mirror pole."

Active Load



 Replacing Vin, M1, and M2 by a Thevenin equivalent.

$$V_X = g_{mN} r_{ON} V_{in}$$

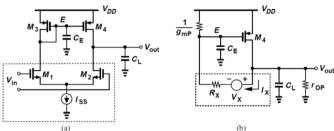
$$R_X = 2r_{ON}$$

$$\frac{V_{out}}{V_{in}}$$

$$=\frac{g_{mN}r_{ON}(2g_{mP}+C_{E}s)r_{OP}}{2r_{OP}r_{ON}C_{E}C_{L}s^{2}+[(2r_{ON}+r_{OP})C_{E}+r_{OP}(1+2g_{mP}r_{ON})C_{L}]s+2g_{mP}(r_{ON}+r_{OP})}.$$

$$\omega_{p1} \approx \frac{1}{(r_{ON} || r_{OP}) C_L} \qquad \qquad \omega_{p2} \approx \frac{g_{mP}}{C_E}$$

Active Load

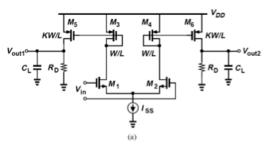


- A zero with a magnitude of $2g_{mP}/C_E$ in the left half plane.
- The appearance of such a zero can be understood by noting that the circuit consists of a "slow path" (M1,M3 and M4) in parallel with a "fast path" (M1 and M2) by $A_0/[(1+s/\omega_{n1})(1+s/\omega_{n2})]$

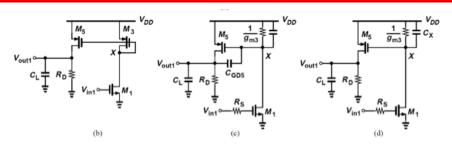
$$A_0/(1 + s/\omega_{p1})$$

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + s/\omega_{p1}} \left(\frac{1}{1 + s/\omega_{p2}} + 1\right)$$

$$= \frac{A_0(2 + s/\omega_{p2})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})}.$$



- Not all fully differential circuits are free from mirror poles.
- Estimate the low-frequency gain and the transfer function of this circuit.

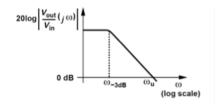


- M5 multiplies the drain current of M3 by K.
- Assume RDCL is relatively small so that the Miller multiplication of CgD5 can be approximated as

$$C_{GD5}(1 + g_{m5}R_D)$$

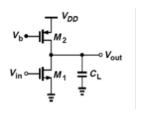
• The overall tran $\frac{V_{out1}}{V_X}(s) = -g_m s R_D \frac{1}{1 + R_D C_L s}$ n equal to Vx/Vin1 multiplied by Vout1/Vx.

Gain-Bandwidth Trade-Offs



- We wish to maximize both the gain and the bandwidth of amplifiers.
- we are interested in both the 3-dB bandwidth, ω_{-3dB} and the "unity-gain" bandwidth, ω_u .

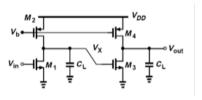
One pole circuit



$$\begin{array}{rcl} GBW & = & A_0 \omega_p \\ & = & g_{m1}(r_{O1}||r_{O2}) \frac{1}{2\pi(r_{O1}||r_{O2})C_L} \\ & = & \frac{g_{m1}}{2\pi C_L}. \end{array}$$

$$\begin{array}{rcl} \omega_u & = & \sqrt{A_0^2 - 1} \omega_p \\ \\ \approx & A_0 \omega_p \end{array}$$

Multi-Pole Circuits



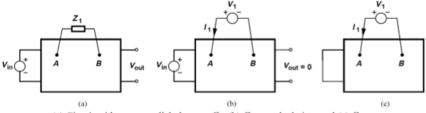
- It is possible to increase the GBW product by cascading two or more gain stages.
- Assume the two stages are identical and neglect other capacitances.

$$\begin{split} \frac{V_{out}}{V_{in}} &= \frac{A_0^2}{(1+\frac{s}{\omega_p})^2} \\ \omega_{-3-dB} &= \sqrt{\sqrt{2}-1}\omega_p \\ &\approx 0.64\omega_m \end{split}$$

$$GBW = \sqrt{\sqrt{2}-1}A_0^2\omega_p$$

 While raising the GBW product, cascading reduces the bandwidth.

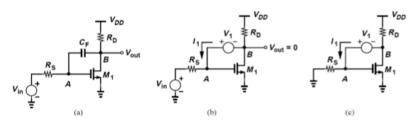
Appendix A: Extra Element Theorem



- (a) Circuit with extra parallel element, Z₁, (b) Z_{out,0} calculation, and (c) Z_{in,0} calculation.
- Suppose the transfer function of a circuit is known and denoted by H(s). Add an extra impedance Z1 between two nodes of the circuit.
- New transfer function:

$$G(s) = H(s) \frac{1 + \frac{Z_{out,0}}{Z_1}}{1 + \frac{Z_{in,0}}{Z_1}}$$

Particularly useful for frequency response analysis.



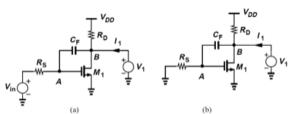
Find the transfer function.

$$H(s) = -g_m(R_D||r_O)$$

 $Z_{out,0} = -1/g_m$

• The negative sign of Zout,0 does not imply a negative impedance between A and B, since $_{V_{in} \neq 0}$

$$\begin{split} Z_{in,0} &= (1+g_m R_S) R_D + R_S = (1+g_m R_D) R_S + R_D \\ G(s) &= -g_m (R_D||r_O) \frac{1 - \frac{1}{g_m} C_F s}{1 + [(1+g_m R_D) R_S + R_D] C_F s} \end{split}$$



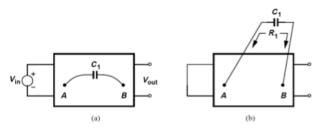
Include CB, from node B to ground.

$$Z_{out,0} = 0$$

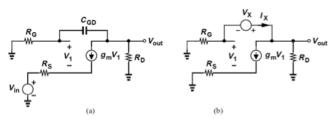
$$Z_{in,0} = \frac{R_D(R_SC_Fs + 1)}{R_S(1 + g_mR_D) + R_D]C_Fs + 1}$$

$$G(s) \ = \ -g_m(R_D||r_O) \frac{1 - \frac{C_F}{g_m} s}{1 + [(1 + g_m R_D)R_S + R_D]C_F s} \frac{1}{1 + \frac{R_D(R_S C_F s + 1)C_B s}{[R_S (1 + g_m R_D) + R_D]C_F s + 1}}$$

Appendix B: Zero-Value Time Constant



- Suppose a circuit contains one capacitor and no other storage elements.
- Wish to determine the pole of the system.
- Set the input to zero, compute the resistance, R1, seen by C1, and express the pole as 1/(R1C1).

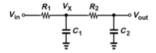


If only CGD is considered, determine the pole frequency.

$$\begin{split} g_m V_1 R_S + V_1 &= -I_X R_G \\ \frac{V_X}{I_X} &= R_D + \left(\frac{g_m R_D}{1 + g_m R_S} + 1\right) R_G = R_{eq} \end{split}$$

The pole is given by $_{1/(R_{eq}C_{GD})}$

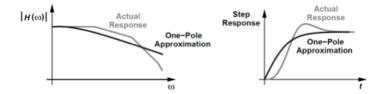
$$1/(R_{eq}C_{GD}$$



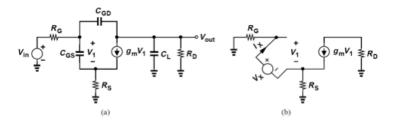
Writing a KVL around Vin, R1, R2, and Vout gives

$$\frac{V_{out}}{V_{in}}(s) = \frac{1}{R_1R_2C_1C_2s^2 + [R_1C_1 + (R_1 + R_2)C_2]s + 1}$$

- The dominant pole is indeed equal to the inverse of the sum of the zero-value time constants. (need to prove)
- The Latitude provided Hardward Provided Hardward Hardward Provided Hardward Hardw



 Approximation of the frequency and time responses by one-pole counterparts.

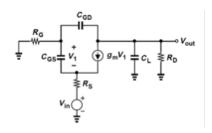


- Estimate the 3-dB bandwidth.
- Begin with the time constant associated with Cgs and set Cgp and CL to zero.

$$\begin{split} R_{CGS} &= \frac{R_G + R_S}{1 + g_m R_S} \\ R_{CGD} &= R_D + \left(\frac{g_m R_D}{1 + g_m R_S} + 1\right) R_G \end{split}$$

The resistance seen by C_L is simply equal to R_D.

$$\omega_{-3dB}^{-1} = \frac{R_G + R_S}{1 + g_m R_S} C_{GS} + \left[R_D + \left(\frac{g_m R_D}{1 + g_m R_S} + 1 \right) R_G \right] C_{GD} + R_D C_L$$



- Find 3-dB band width of a common-gate stage containing a gate resistance of RG and a source resistance of RS.
- The resulting equivalent circuits are identical for CS and CG stages, yielding the same time constants and hence the same bandwidth.
- Does this result contradict our earlier assertion that the CG stage is free from the Miller effect?
- · No. Why?