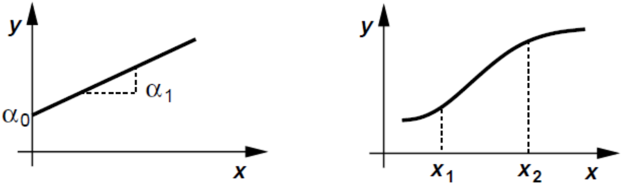
Chapter 3: Single-stage Amplifiers

Ideal vs Non-ideal Amplifier



(a) (b)

- **Ideal amplifier (Fig. a)**

$$y(t) = \alpha_0 + \alpha_1 x(t)$$

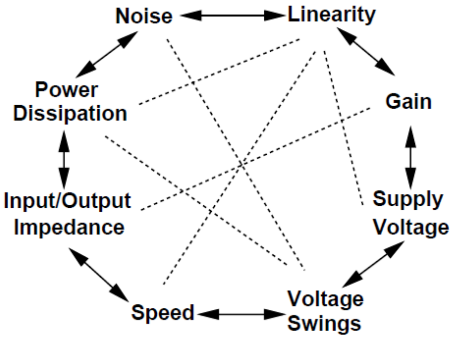
  – **Large-signal characteristic is a straight line**
  – ***α1* is the "gain", *α0* is the "dc bias"**

- **Nonlinear amplifier (Fig. b)**

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \cdots + \alpha_n x^n(t)$$

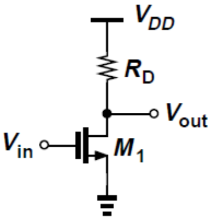
  – **Large-signal excursions around bias point**
  – **Varying "gain", approximated by polynomial**
  – **Causes distortion of signal of interest**

Analog Design Tradeoff



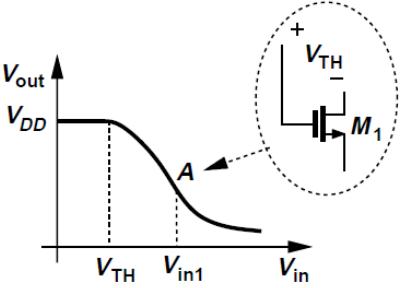
- Along with gain and speed, other parameters also important for amplifiers
- Input and output impedances decide interaction with preceding and subsequent stages
- Performance parameters trade with each other
  - Multi-dimensional optimization problem

Common-Source stage with Resistive load



- Very high input impedance at low frequencies
- For *Vin* < *VTH*, *M1* is off and *Vout* = *VDD*

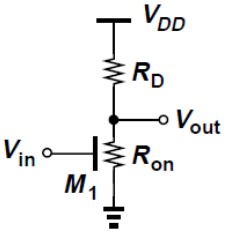
$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$



- When *Vin* > *VTH*, *M1* turns on in saturation region, *Vout* falls
- When *Vin* > *Vin1*, *M1* enters triode region
- At point A, *Vout* = *Vin1-VTH*

$$V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{TH})^2$$

Common-Source stage with Resistive load



- For *Vin* > *Vin1*,

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{in} - V_{TH})V_{out} - V_{out}^2\right]$$

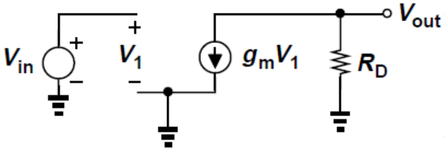
- If *Vin* is high enough to drive *M1* into deep triode region so that *Vout* << 2(*Vin* - *VTH*),

$$\begin{aligned} V_{out} &= V_{DD}\frac{R_{on}}{R_{on} + R_D} \\ &= \frac{V_{DD}}{1 + \mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})} \end{aligned}$$

Common-Source stage with Resistive load

$$A_v = \frac{\partial V_{out}}{\partial V_{in}}$$
$$= -R_D \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})$$
$$= -g_m R_D.$$

- **Taking derivative of *ID* equation in saturation region, small-signal gain is obtained**



- **Same result is obtained from small-signal equivalent circuit**

$$V_{out} = -g_m V_1 R_D = -g_m V_{in} R_D$$

- ***gm and Av* vary for large input signal swings according to**

$$g_m = \mu_n C_{ox}(W/L)(V_{GS} - V_{TH}).$$

- **This causes non-linearity**

Common-Source stage with Resistive load

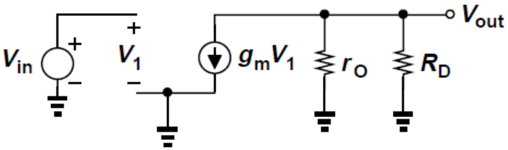
- **For large values of *RD*, channel-length modulation of *M1* becomes significant, *Vout* equation becomes**

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2(1 + \lambda V_{out})$$

- **Voltage gain is**

$$A_v = -g_m \frac{r_O R_D}{r_O + R_D}$$

- **Above result is also obtained from small-signal equivalent circuit**



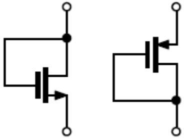
$$V_1 = V_{in}$$

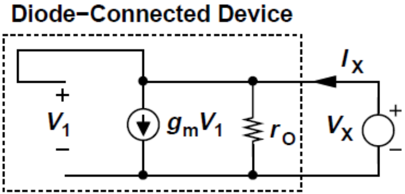
$$g_m V_1 (r_O \| R_D) = -V_{out}$$

$$V_{out}/V_{in} = -g_m (r_O \| R_D)$$

Diode-Connected MOSFET

- A MOSFET can operate as a small-signal resistor if its gate and drain are shorted, called a "diode-connected" device
- Transistor always operates in saturation



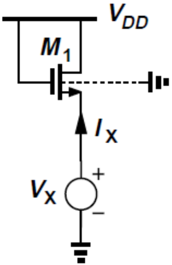


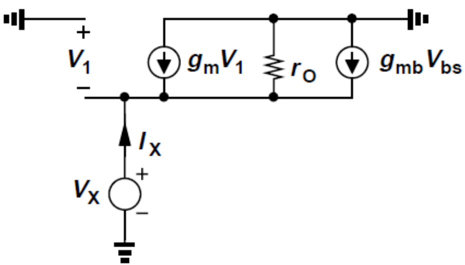
- Impedance of the device can be found from small-signal equivalent model

$$V_1 = V_X \qquad\qquad I_X = V_X / r_O + g_m V_X$$

$$V_X / I_X = (1/g_m) || r_O \approx 1/g_m$$

Diode-Connected MOSFET





- **Including body-effect, impedance "looking into" the source terminal of diode-connected device is found as**

$$V_1 = -V_X \qquad V_{bs} = -V_X$$

$$(g_m + g_{mb})V_X + \frac{V_X}{r_O} = I_X$$

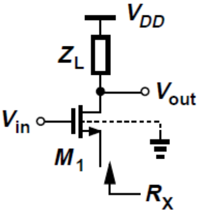
$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb} + r_O^{-1}}$$

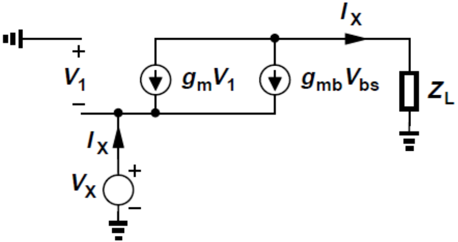
$$= \frac{1}{g_m + g_{mb}} \| r_O$$

$$\approx \frac{1}{g_m + g_{mb}}.$$

Diode-Connected MOSFET: Example

- Find *RX* if *λ* = 0





- Set independent sources to zero, apply *VX* and find resulting *IX*

$$V_1 = V_X$$

$$V_{bs} = -V_X$$

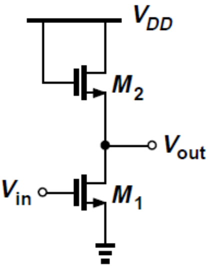
$$(g_m + g_{mb})V_X = I_X$$

$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb}}.$$

- Result is same compared to when drain of *M1* is at ac ground, but only when *λ* = 0

- Loosely said that looking into source of MOSFET, we see 1/*gm* when *λ* = *γ* = 0

CS Stage with Diode-Connected Load



- **Neglecting channel-length modulation, using impedance result for diode-connected device,**

$$A_v = -g_{m1}\frac{1}{g_{m2}+g_{mb2}}$$
$$= -\frac{g_{m1}}{g_{m2}}\frac{1}{1+\eta},$$

where,

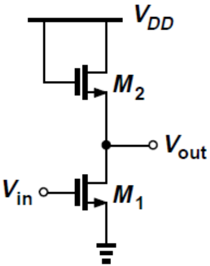
$$\eta = g_{mb2}/g_{m2}.$$

- **Expressing *gm1* and *gm2* in terms of device dimensions,**

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}\frac{1}{1+\eta}$$

- **This shows that gain is a weak function of bias currents and voltages, i.e., relatively linear input-output characteristic**

CS Stage with Diode-Connected Load



- **From large-signal analysis,**

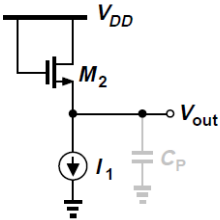
$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{DD} - V_{out} - V_{TH2})^2$$

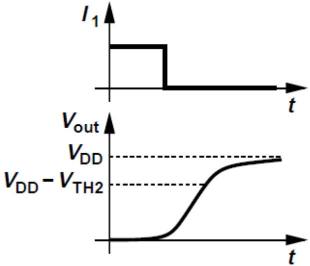
$$\sqrt{\left(\frac{W}{L}\right)_1}(V_{in} - V_{TH1}) = \sqrt{\left(\frac{W}{L}\right)_2}(V_{DD} - V_{out} - V_{TH2})$$

- **If *VTH2* does not vary much with *Vout*, input-output characteristic is relatively linear.**
- **Squaring function of *M1* (from its input voltage to its drain current) and square root function of *M2* (from its drain current to its overdrive) act as inverse functions**

$$f^{-1}(f(x)) = x.$$

CS Stage with Diode-Connected Load



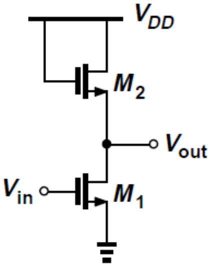


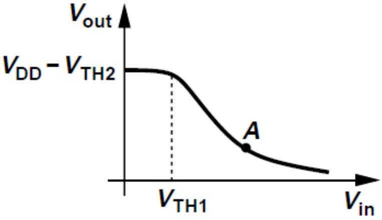
- As *I1* falls, so does overdrive of *M2* so that

$$V_{GS2} \approx V_{TH2} \qquad V_{out} \approx V_{DD} - V_{TH2}$$

- Subthreshold conduction of *M2* eventually brings *Vout* to *VDD*, but at very low current levels, finite capacitance at output node *CP* slows down the change in *Vout* from *VDD-VTH2* to *VDD.*
- In high-frequency circuits, *Vout* remains around *VDD-VTH2* when *I1* falls to small values.

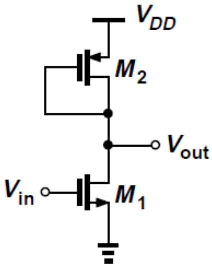
CS Stage with Diode-Connected Load





- **For *Vin* < *VTH1*, *Vout* = *VDD* – *VTH2***
- **When *Vin* > *VTH1*, previous large-signal analysis predicts that *Vout* approximately follows a single line**
- **As *Vin* exceeds *Vout* + *VTH1* (to the right of point A), *M1* enters the triode region and the characteristic becomes nonlinear.**

CS Stage with Diode-Connected PMOS device



- **Diode-connected load can be implemented as a PMOS device, free of body-effect**
- **Small-signal voltage gain neglecting channel-length modulation**

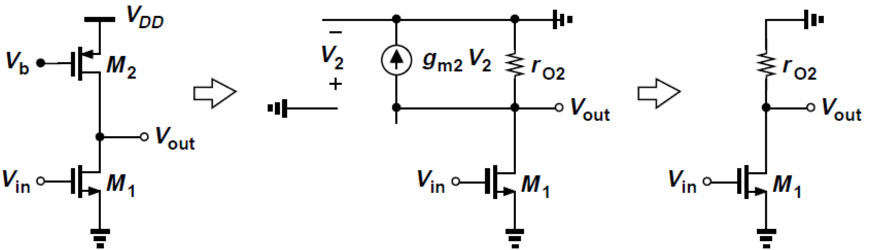
$$A_v = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

- **Gain is a relatively weak function of device dimensions**
- **Since *μn* ≈ 2*μp,* high gain requires "strong" input device (narrow) and "weak" load device (wide)**
- **This limits voltage swings since for *λ* = 0, we get**

$$\frac{|V_{GS2} - V_{TH2}|}{V_{GS1} - V_{TH1}} = A_v$$

- **For diode-connected loads, swing is constrained by both required overdrive voltage and threshold voltage, i.e., for small overdrive, output cannot exceed *VDD* - |*VTH*|.**

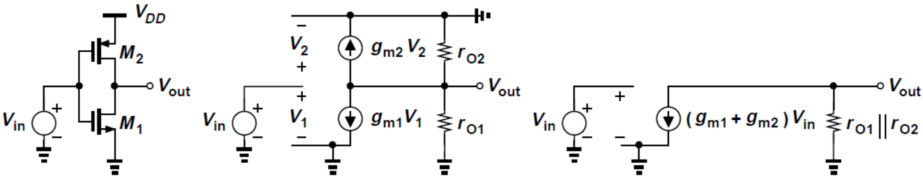
CS Stage with Current-Source Load



- **Current-source load allows a high load resistance without limiting output swing**
- **Voltage gain is** $A_v = -g_{m1}(r_{O1} || r_{O2})$
- **Overdrive of *M2* can be reduced by increasing its width, *ro2* can be increased by increasing its length**
- **Output bias voltage is not well-defined**
- **Intrinsic gain of *M1* increases with *L* and decreases with *ID***

$$g_{m1} r_{O1} = \sqrt{2\left(\frac{W}{L}\right)_1 \mu_n C_{ox} I_D}\,\frac{1}{\lambda I_D}$$

CS Stage with Active Load

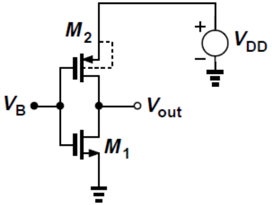


- Input signal is also applied to gate of load device, making it an "active" load
- *M1* and *M2* operate in parallel and enhance the voltage gain
- From small-signal equivalent circuit,

$$-(g_{m1}+g_{m2})V_{in}(r_{O1}||r_{O2}) = V_{out}$$
$$A_v = -(g_{m1}+g_{m2})(r_{O1}||r_{O2})$$

- Same output resistance as CS stage with current-source load, but higher transconductance
- Bias current of *M1* and *M2* is a strong function of PVT

CS Stage with Active Load: Supply sensitivity

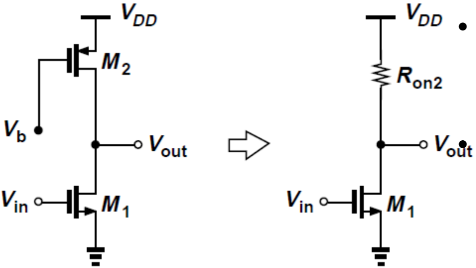


$$V_{GS1} + |V_{GS2}| = V_{DD}$$

- Variations in *VDD* or the threshold voltages directly translate to changes in the drain currents
- Supply voltage variations "supply noise" are amplified too
- Voltage gain from *VDD* to *Vout* can be found to be

$$\frac{V_{out}}{V_{DD}} = \frac{g_{m2}r_{O2} + 1}{r_{O2} + r_{O1}} r_{O1} = \left(g_{m2} + \frac{1}{r_{O2}}\right)(r_{O1}||r_{O2})$$

CS Stage with Triode Load



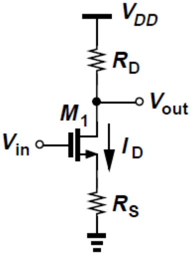
- A MOS device biased in the deep triode region acts as a resistive load in a CS stage
- *Vb* is sufficiently low to ensure *M2* is in deep triode region for all output voltage swings

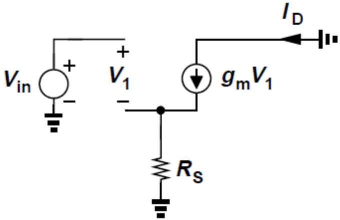
- Voltage gain is *Av* = *-gm1Ron2*, where *Ron2* is the MOS ON resistance given by

$$R_{on2} = \frac{1}{\mu_p C_{ox}(W/L)_2(V_{DD} - V_b - |V_{THP}|)}$$

- *Ron2* depends on *µpCox*, *Vb* and *VTHP* which vary with PVT
- Generating a precise value of *Vb* is complex, which makes circuit hard to use
- Triode loads consume lesser voltage headroom than diode-connected devices since *Vout,max* = *VDD* for the former whereas *Vout,max* = *VDD-|VTHP|* for the latter

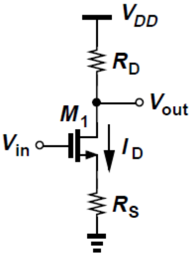
CS Stage with Source Degeneration

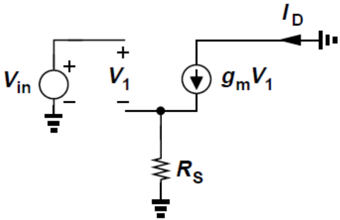




- Degeneration resistor *RS* in series with source terminal makes input device more linear
  - As *Vin* increases, so do *ID* and the voltage drop across *RS*
  - Part of the change in *Vin* appears across *RS* rather than gate-source overdrive, making variation in *ID* smoother
- Gain is now a weaker function of *gm*

CS Stage with Source Degeneration





- **Nonlinearity of circuit is due to nonlinear dependence of *ID* upon *Vin***
- **Equivalent transconductance *Gm* of the circuit can be defied as** $G_m = \partial I_D / \partial V_{in}$

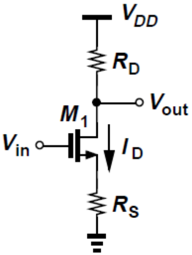
$$V_{out} = V_{DD} - I_D R_D$$

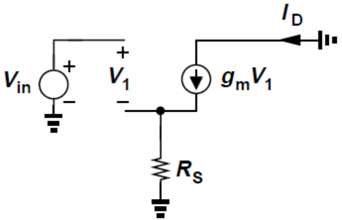
$$\partial V_{out} / \partial V_{in} = -(\partial I_D / \partial V_{in}) R_D$$

$$I_D = f(V_{GS})$$

$$G_m = \frac{\partial I_D}{\partial V_{in}} = \frac{\partial f}{\partial V_{GS}} \frac{\partial V_{GS}}{\partial V_{in}}$$

CS Stage with Source Degeneration





$$V_{GS} = V_{in} - I_D R_S$$

$$\partial V_{GS}/\partial V_{in} = 1 - R_S \partial I_D/\partial V_{in}$$

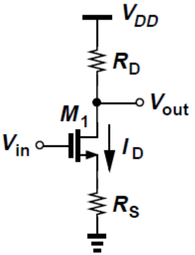
$$G_m = \left(1 - R_S \frac{\partial I_D}{\partial V_{in}}\right) \frac{\partial f}{\partial V_{GS}}$$

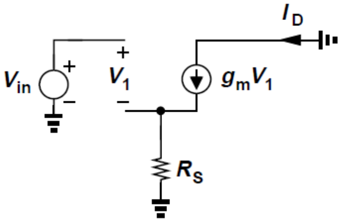
$$G_m = \frac{g_m}{1 + g_m R_S}$$

- ***gm*** **is the transconductance of** ***M1***
- **Small-signal voltage gain** ***Av*** **is then given by**

$$\begin{aligned} A_v &= -G_m R_D \\ &= \frac{-g_m R_D}{1 + g_m R_S} \end{aligned}$$

CS Stage with Source Degeneration





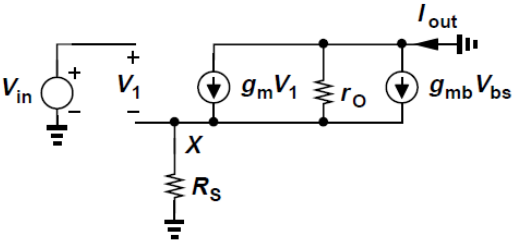
- Same result for *Gm* is obtained from small-signal equivalent circuit, by noting that

$$V_{in} = V_1 + I_D R_S$$

$$I_D = g_m V_1$$

- As *RS* increases, *Gm* becomes a weaker function of *gm* and hence *ID*
- For $R_S \gg 1/g_m$, $G_m \approx 1/R_S$, i.e., $\Delta I_D \approx \Delta V_{in}/R_S$
- Most of the change in *Vin* across *RS* and drain current becomes a "linearized" function of input voltage

CS Stage with Source Degeneration



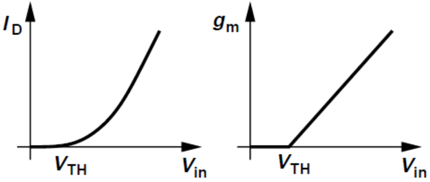
- Including body-effect and channel-length modulation, *Gm* is found from modified small-signal equivalent circuit

$$V_{in} = V_1 + I_{out} R_S$$

$$\begin{aligned}
I_{out} &= g_m V_1 - g_{mb} V_X - \frac{I_{out} R_S}{r_O} \\
&= g_m (V_{in} - I_{out} R_S) + g_{mb}(-I_{out} R_S) - \frac{I_{out} R_S}{r_O} \\
G_m &= \frac{I_{out}}{V_{in}} \\
&= \frac{g_m r_O}{R_S + [1 + (g_m + g_{mb}) R_S] r_O}
\end{aligned}$$

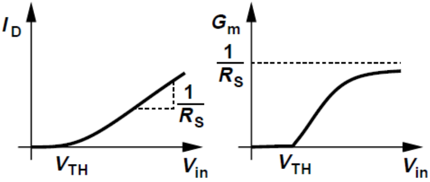
CS Stage with Source Degeneration

Large-signal behavior



***RS*=0**

- ***ID* and *gm* vary with *Vin* as derived in calculations in Chapter 2**



***RS*≠0**

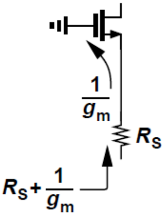
- **At low current levels, turn-on behavior is similar to when *RS*=0 since**
  an $1/g_m \gg R_S$
- **As ove** $G_m \approx g_m$ **d gm increase, effect of *RS* becomes more significant**

CS Stage with Source Degeneration

- Small-signal derived previously can be written as

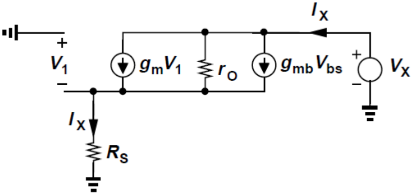
$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$

- Denominator = Series combination of inverse transconductance + explicit resistance seen from source to ground
- Called "resistance seen in the source path"
- Magnitude of gain = Resistance seen at the drain/ Total resistance seen in the source path



CS Stage with Source Degeneration

- **Degeneration causes increase in output resistance**



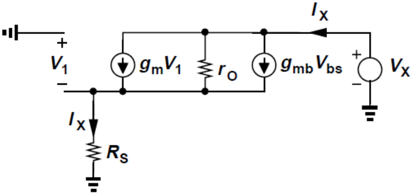
- **Ignoring *RD* and including body effect in small-signal equivalent model,**

$$
\begin{aligned}
V_1 &= -I_X R_S \\
I_X - (g_m + g_{mb})V_1 &= I_X + (g_m + g_{mb}) R_S I_X \\
R_{out} &= [1 + (g_m + g_{mb}) R_S] r_O + R_S \\
&= [1 + (g_m + g_{mb}) r_O] R_S + r_O
\end{aligned}
$$

- ***ro* is boosted by a factor of {1 + (*gm*+*gmb*)*RS*} and then added to *RS***
- **Alternatively, *RS* is boosted by a factor of {1 + (*gm*+*gmb*)*ro*} and then added to *ro***

CS Stage with Source Degeneration

- Compare *RS* = 0 with *RS* > 0

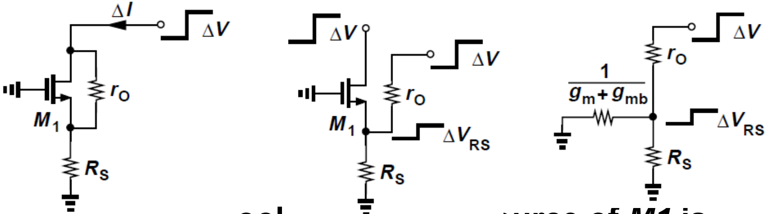


- If *RS* = 0, $g_m V_1 = g_{mb} V_{bs} = 0$ and $I_X = V_X / r_O$
- If *RS* > 0, $I_X R_S > 0$ and $V_1 < 0$, obtaining negative *gmV1* and *gmb*
- Thus, current supplied by *VX* is less than *VX*/*ro* and hence output impedance is greater than *ro*

CS Stage with Source Degeneration

<u>Intuitive understanding of increased output impedance</u>

- Apply voltage change *ΔV* at output and measure resulting change *ΔI* in output current, which is also the change in current through *RS*

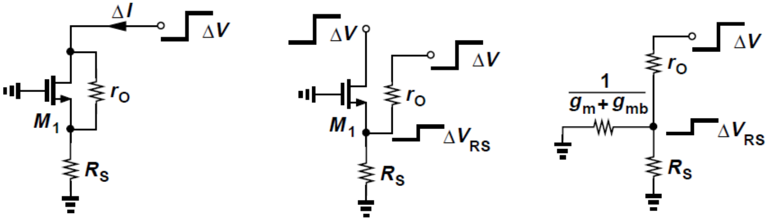


- Resistance seen looking into the source of *M1* is *1/(gm + gmb)*
- Voltage change across *RS* is

$$\Delta V_{RS} = \Delta V \frac{\frac{1}{g_m + g_{mb}} || R_S}{\frac{1}{g_m + g_{mb}} || R_S + r_O}$$

CS Stage with Source Degeneration

Intuitive understanding of increased output impedance



- Change in current across *RS* is

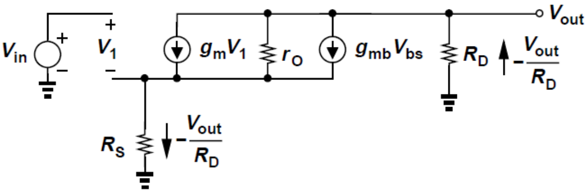
$$\Delta I = \frac{\Delta V_{RS}}{R_S}$$

$$= \Delta V \frac{1}{[1+(g_m+g_{mb})]R_S r_O + R_S},$$

- Output resistance is thus

$$\frac{\Delta V}{\Delta I} = [1+(g_m+g_{mb})R_S]r_O + R_S$$

CS Stage with Source Degeneration



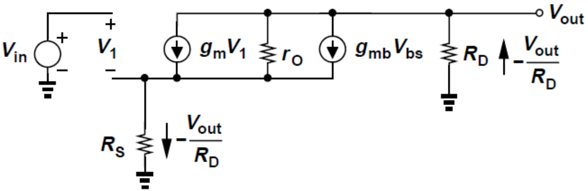
- To compute gain in the general case including body effect and channel-length modulation, consider above small-signal model
- From KVL at input,

$$V_1 = V_{in} + V_{out} R_S / R_D$$

- KCL at output gives

$$\begin{aligned} I_{ro} &= -\frac{V_{out}}{R_D} - (g_m V_1 + g_{mb} V_{bs}) \\ &= -\frac{V_{out}}{R_D} - \left[g_m \left(V_{in} + V_{out} \frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] \end{aligned}$$

CS Stage with Source Degeneration



- Since voltage drops across *rO* and *RS* must add up to *Vout*

$$V_{out} = I_{ro} r_O - \frac{V_{out}}{R_D} R_S$$

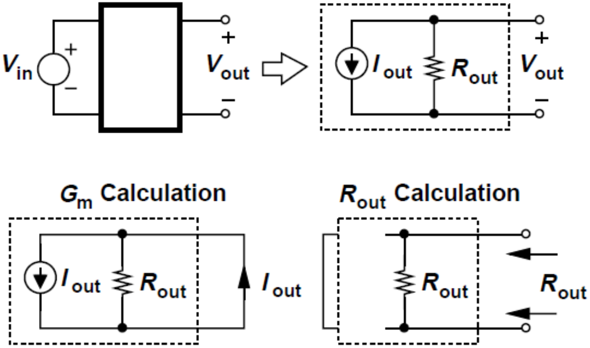
$$= -\frac{V_{out}}{R_D} r_O - \left[g_m \left(V_{in} + V_{out} \frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] r_O - V_{out} \frac{R_S}{R_D}$$

- Voltage gain is therefore

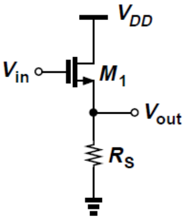
$$\frac{V_{out}}{V_{in}} = \frac{-g_m r_O R_D}{R_D + R_S + r_O + (g_m + g_{mb}) R_S r_O}$$

Lemma

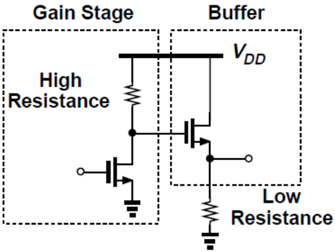
- In a linear circuit, the voltage gain is equal to –*GmRout*
  - *Gm* denotes the transconductance of the circuit when output is shorted to ground
  - *Rout* represents the output resistance of the circuit when the input voltage is set to zero
- Norton equivalent of a linear circuit



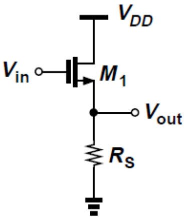
Source Follower

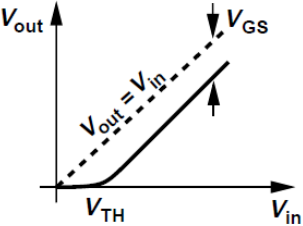


- Source follower (also called "common-drain" stage) senses the input at the gate and drives load at the source
- It presents a high input impedance, allowing source potential to "follow" the gate voltage
- Acts as a voltage buffer



Source Follower

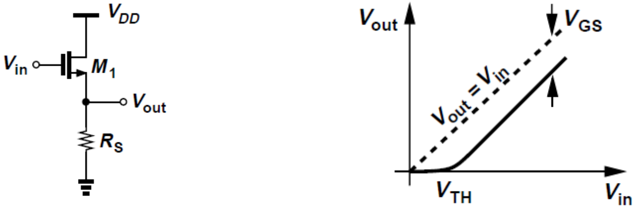




- For *Vin* < *VTH*, *M1* is off and *Vout* = 0
- As *Vin* exceeds *VTH*, *M1* turns on in saturation since *VDS* = *VDD* and *VGS* –*VTH* ≈ 0 and *ID1* flows through *RS*
- As *Vin* increases further, *Vout* follows the input with a difference (level shift) equal to *VGS*
- Input-output characteristic neglecting channel-length modulation can be expressed as

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out})^2 R_S = V_{out}$$

Source Follower



- For *Vin* < *VTH*, *M1* is off and *Vout* = 0
- Differentiating both sides of large-signal equation for *Vout*,

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}2(V_{in}-V_{TH}-V_{out})\left(1-\frac{\partial V_{TH}}{\partial V_{in}}-\frac{\partial V_{out}}{\partial V_{in}}\right)R_S=\frac{\partial V_{out}}{\partial V_{in}}$$

- Since

$$\partial V_{TH}/\partial V_{in}=(\partial V_{TH}/\partial V_{SB})(\partial V_{SB}/\partial V_{in})=\eta\partial V_{out}/\partial V_{in}$$

- Therefore,

$$\frac{\partial V_{out}}{\partial V_{in}}=\frac{\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{TH}-V_{out})R_S}{1+\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{TH}-V_{out})R_S(1+\eta)}$$

- Note that

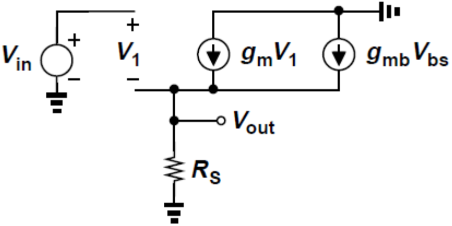
$$g_m=\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{TH}-V_{out})$$

- Therefore,

$$A_v=\frac{g_m R_S}{1+(g_m+g_{mb})R_S}$$

Source Follower

- **Small-signal gain can be obtained more easily using small-signal equivalent model**



- **We have,** $V_{in} - V_1 = V_{out}, V_{bs} = -V_{out}$
- **KVL:**

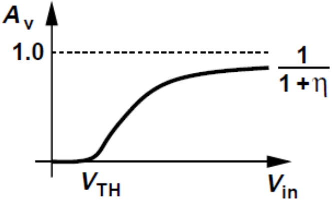
$$g_m V_1 - g_{mb} V_{out} = V_{out} / R_S$$

- **KCL:**

$$V_{out}/V_{in} = g_m R_S / [1 + (g_m + g_{mb}) R_S]$$

- **Therefore,**

Source Follower

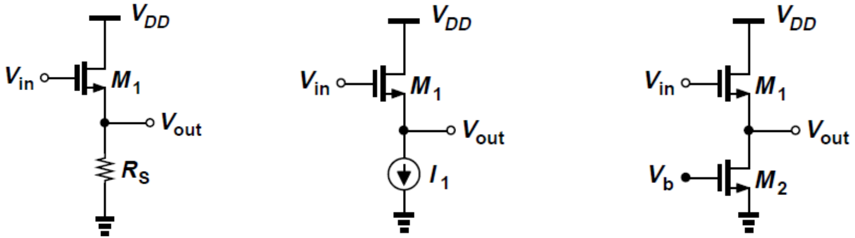


- Voltage gain begins from zero for *Vin* ≈ *VTH* (*gm* ≈ 0), and monotonically increases
- As drain current and *gm* increase, *Av* approaches

$$g_m/(g_m + g_{mb}) = 1/(1+\eta)$$

- Since *η* itself slowly decreases with *Vout, Av* would eventually become equal to unity, but for typical allowable source-bulk voltages, *η* remains greater than roughly than 0.2
- Even if *RS* = ∞, voltage gain of a source follower is not equal to one

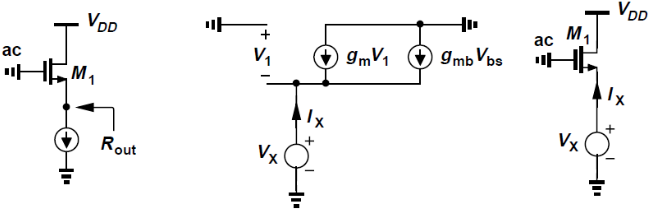
Source Follower



- **Drain current of *M1* depends heavily of input dc level**
- **Even if *VTH* is relatively constant, the increase in *VGS* means that *Vout* (=*Vin*-*VGS*) does not follow *Vin* faithfully, incurring nonlinearity**
- **To alleviate this issue, the resistor can be replaced by a constant current source**
- **Current source is itself is implemented as an NMOS transistor operating in the saturation region**

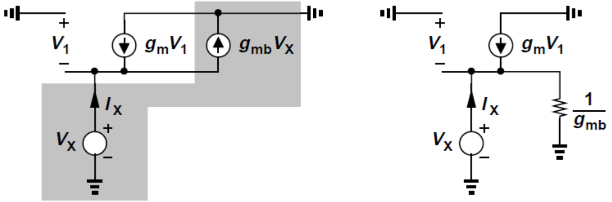
Source Follower

Calculation of output impedance



- From small-signal equivalent circuit, $V_X = -V_{bs}$
- It follows that $I_X - g_m V_X - g_{mb} V_X = 0$ and $R_{out} = \dfrac{1}{g_m + g_{mb}}$
- Body effect decreases output resistance of source followers
- If *VX* decreases by *ΔV* so the drain current increases
  - w/o body effect, *VGS* increases by *ΔV*
  - with body effect, *VTH* decreases as well, thus (*VGS*-*VTH*)2 and *ID1* increase by a greater amount, hence lower output impedance

Source Follower

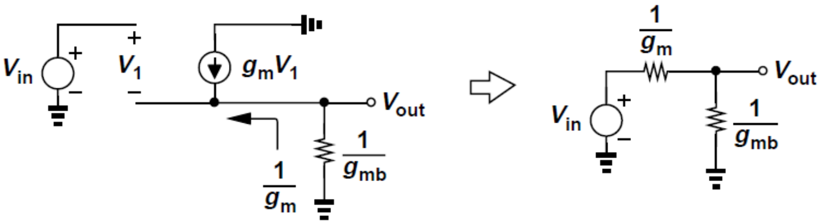


- Magnitude of the current source *gmbVbs* = *gmbVX* is linearly proportional to the voltage across it, can be modelled by a resistor equal to 1/*gmb* (valid only for source followers)
- This appears in parallel with the output, decreasing the overall output resistance
- Since without *1/gmb*, the output resistance is *1/gm*, we conclude that

$$R_{out} = \frac{1}{g_m} \| \frac{1}{g_{mb}}$$

$$= \frac{1}{g_m + g_{mb}}$$

Source Follower



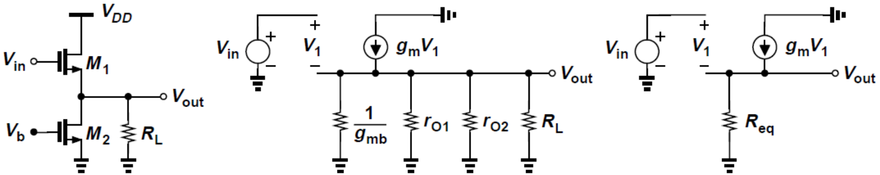
- **Modelling effect of *gmb* by a resistor helps explain lower than unity gain for *RS* = ∞**
- **From the Thevenin equivalent circuit**

$$A_v = \frac{\frac{1}{g_{mb}}}{\frac{1}{g_m} + \frac{1}{g_{mb}}}$$

$$= \frac{g_m}{g_m + g_{mb}}.$$

Source Follower

- **Small-signal equivalent circuit with a finite load resistance and channel-length modulation is shown**



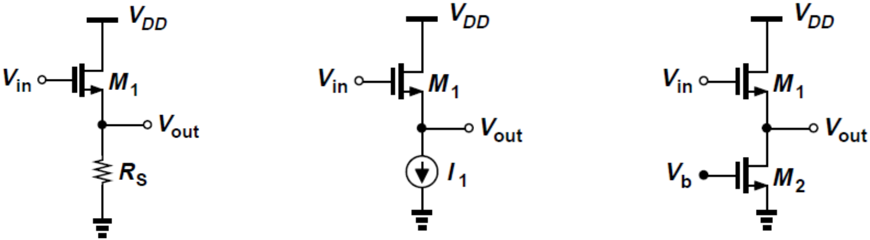
- ***1/gmb*, *rO1*, *rO2* and *RL* are in parallel, therefore,**

$$R_{eq} = (1/g_{mb})||r_{O1}||r_{O2}||R_L$$

- **It follows that**

$$A_v = \frac{R_{eq}}{R_{eq} + \frac{1}{g_m}}$$

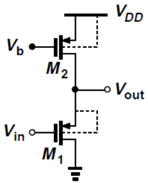
Issues with Source Follower

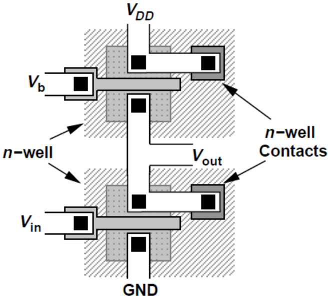


- **Source followers exhibit high input impedance and moderate output impedance, but at the cost of**
  - **Nonlinearity**
  - **Voltage headroom limitation**
- **Even when biased by ideal current source, there is input-output nonlinearity due to nonlinear dependence of *VTH* on the source potential**
- **In submicron technologies, *rO* changes substantially with *VDS* and introduces additional variation in small-signal gain**

Issues with Source Follower

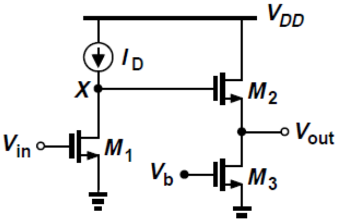
- Nonlinearity can be eliminated if the bulk is tied to the source
  - Possible only for PFETs since all NFETs usually share the same substrate
- PMOS source follower employing two separate n-wells can eliminate the body effect of *M1*
- Lower mobility of PFETs yields a higher output impedance than that available in the NMOS counterpart





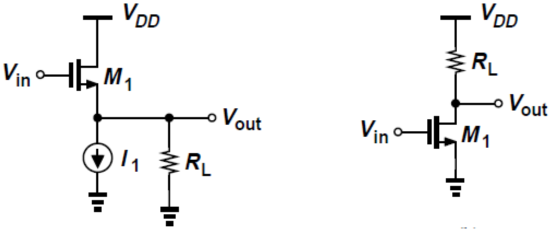
Issues with Source Follower

- Source followers also shift the dc level of the signal by *VGS*, thereby consuming voltage headroom



- In the cascade of CS stage and source follower shown above,
  - w/o source follower, minimum allowable value of *VX* would be *VGS1-VTH1* (for *M1* to remain in saturation)
  - with source follower, *VX* must be greater than *VGS2*+(*VGS3-VTH3*) so that *M3* is saturated
- For comparable overdrive voltages in *M1* and *M3*, allowable swing at X is reduced by *VGS2*

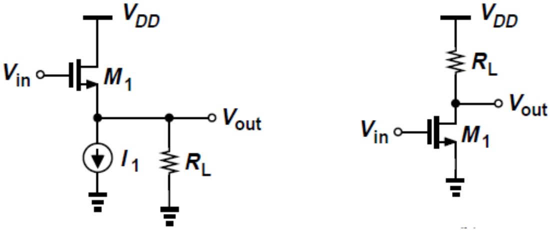
Comparison of CS stage and Source Follower



- **Comparing the gain of source followers and CS stage with a low load impedance**
  - **E.g., driving an external 50-Ω termination in a high-frequency environment**
- **When load is driven by a source follower, overall voltage gain is**

$$\frac{V_{out}}{V_{in}}\Big|_{SF} \approx \frac{R_L}{R_L + 1/g_{m1}} \approx \frac{g_{m1}R_L}{1+g_{m1}R_L}.$$

Comparison of CS stage and Source Follower



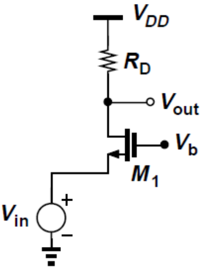
- Load can be included as part of a common-source stage, providing a gain of

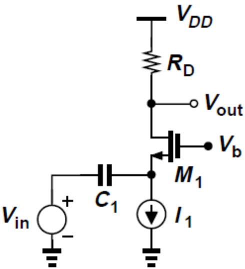
$$\frac{V_{out}}{V_{in}}\Big|_{CS} \approx -g_{m1}R_L.$$

- Key difference between the two topologies is the achievable voltage gain for a given bias current
- For example, if $1/g_{m1} \approx R_L$, source follower exhibits a gain of at most 0.5 whereas the common-source stage provides a gain close to unity
- Thus, source followers are not efficient drivers

Common-Gate Stage

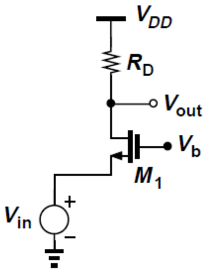
- A common-gate (CG) stage senses the input at the source and produces the output at the drain
- Gate is biased to establish proper operating conditions





- Bias current of *M1* flows through the input signal source
- Alternatively, *M1* can be biased by a constant current source, with the signal capacitively coupled to the circuit

Common-Gate Stage: Large-signal behavior



- Assume *Vin* decreases from a large positive value and that *λ=0*
- For *Vin* ≥ Vb-*VTH*, *M1* is off and *Vout* = *VDD*
- For lower values of *Vin*, if *M1* is in saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2$$

- As *Vin* decreases further, so does *Vout* driving *M1* into the triode region if

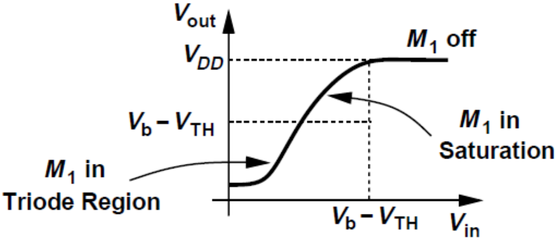
$$V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH}$$

- In the region where *M1* is saturated, we can express the output voltage as

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D$$

Common-Gate Stage

Input-output characteristic



- **For *M1* in saturation,** $V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D$
- **Small-signal gain can thus be obtained**

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})\left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right) R_D$$

- **Since** $\partial V_{TH}/\partial V_{in} = \partial V_{TH}/\partial V_{SB} = \eta$ **we have**

$$\frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox}\frac{W}{L}R_D(V_b - V_{in} - V_{TH})(1 + \eta)$$
$$= g_m(1 + \eta)R_D.$$

Common-Gate Stage

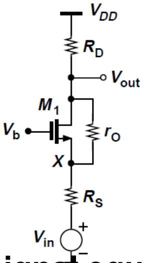
- **Gain of the common-gate (CG) stage is positive**

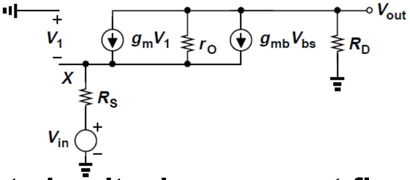
$$\frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox}\frac{W}{L}R_D(V_b - V_{in} - V_{TH})(1+\eta)$$
$$= g_m(1+\eta)R_D.$$

- **Body effect increases the effective transconductance of the stage**
- **For a given bias current and supply voltage (i.e., a given power budget), voltage gain of the CG stage can be maximized by**
  - **Increasing gm by widening the input device, eventually reaching subthreshold operation [*gm=ID/ζVT*]**
  - **Increasing *RD* and inevitably, the dc drop across it**
- **The minimum allowable value of *Vout* is *VGS-VTH+VI1*, where *VI1* denotes the minimum voltage required by *I1***

Common-Gate Stage

- Consider output impedance of transistor and impedance of the signal source





- In small-signal equivalent circuit, since current flowing *RS* is *–Vout/RD,*

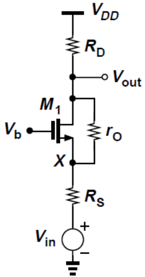
$$V_1 - \frac{V_{out}}{R_D} R_S + V_{in} = 0 \qquad (1)$$

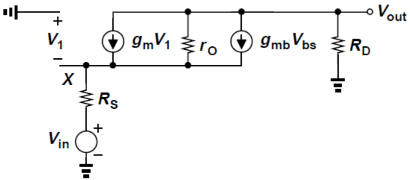
- Moreover, since current through *rO* is $-V_{out}/R_D - g_m V_1 - g_{mb} V_1$

$$r_O\left(\frac{-V_{out}}{R_D} - g_m V_1 - g_{mb} V_1\right) - \frac{V_{out}}{R_D} R_S + V_{in} = V_{out} \qquad (2)$$

Common-Gate Stage

Common-Gate Stage





- **Substituting *V1* from (1) in (2),**

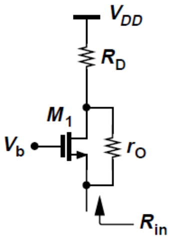
$$r_O\left[\frac{-V_{out}}{R_D} - (g_m + g_{mb})\left(V_{out}\frac{R_S}{R_D} - V_{in}\right)\right] - \frac{V_{out}R_S}{R_D} + V_{in} = V_{out}$$

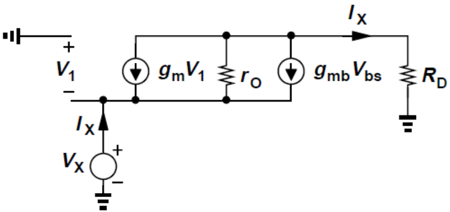
- **Therefore,**

$$\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_S + R_S + R_D} R_D$$

- **The voltage gain expression is similar to that of a degenerated CS stage**

Common-Gate Stage: Input Impedance





- From the small-signal equivalent circuit for finding input impedance, we have

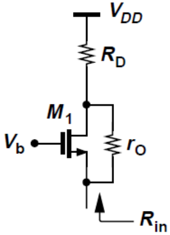
$$V_1 = -V_X$$

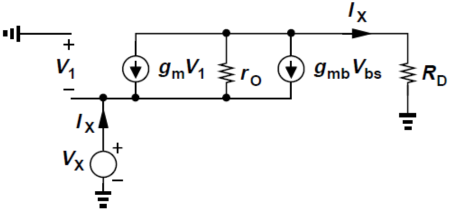
- The current through *rO* is equal to *IX* + *gmV1* + *gmbV1* = *IX* - (*gm*+*gmb*)*VX*

- Voltages across *rO* and *RD* can be added and equated to

$$R_D I_X + r_O[I_X - (g_m + g_{mb})V_X] = V_X$$

Common-Gate Stage: Input Impedance





- **Thus,**

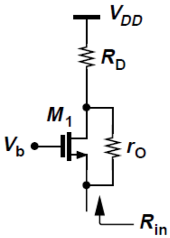
$$\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + (g_m + g_{mb})r_O}$$

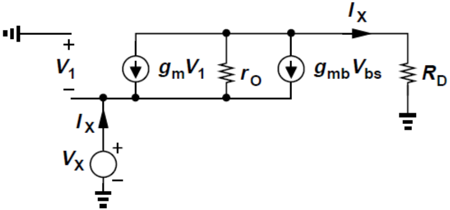
$$\approx \frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}},$$

If $(g_m + g_{mb})r_O \gg 1$

- **The drain impedance is divided by $(g_m + g_{mb})r_O$ when seen at the source**
  - **Important in short-channel devices because of their low intrinsic gain**

Common-Gate Stage: Input Impedance



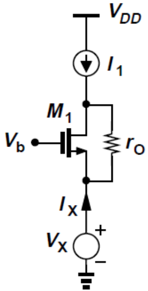


- Suppose *RD* = 0, then

$$\frac{V_X}{I_X} = \frac{r_O}{1+(g_m+g_{mb})r_O} = \frac{1}{\frac{1}{r_O}+g_m+g_{mb}},$$

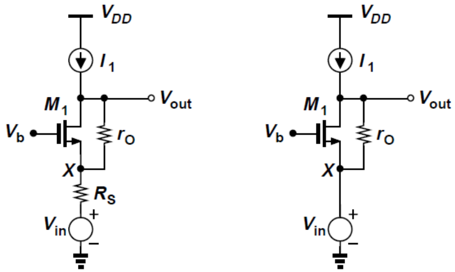
- This is the impedance seen at the source of a source follower, a predictable result since with *RD* = 0 the circuit configuration is the same as a source follower

Common-Gate Stage: Input Impedance



- If *RD* is replaced with an ideal current source, earlier result predicts that input impedance approaches infinity
- Total current through the transistor is fixed and is equal to *I1*
- Therefore, a change in the source potential cannot change the device current, and hence *IX* = 0
- The input impedance of a CG stage is relatively low *only* if the load impedance connected to the drain is small

Common-Gate Stage

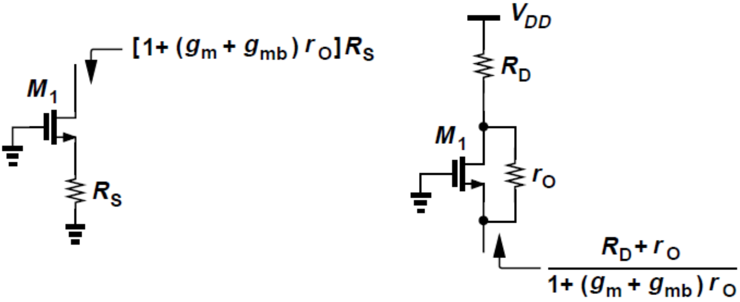


- In a CG stage with a current source load, substituting *RD*=∞ in the voltage gain equation, we get

$$A_v = (g_m + g_{mb})r_O + 1$$

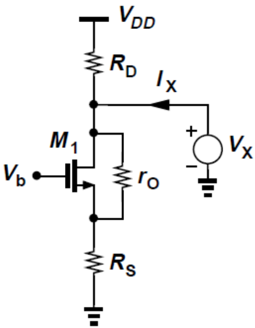
- Gain does not depend on *RS*
- From the foregoing discussion, if *RD*→∞, so does the impedance seen at the source of *M1*, and the small-signal voltage at node X becomes equal to *Vin*

Common-Gate Stage



- In a degenerated CS stage, we loosely say that a transistor transforms its source resistance *up*
- In a CG stage, the transistor transforms its drain resistance *down*
- The MOS transistor can thus be viewed as an resistance transformer

Common-Gate Stage: Output Impedance



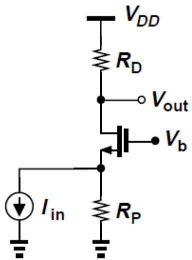
- From the above small-signal equivalent circuit, we can find output impedance as

$$R_{out} = \{[1 + (g_m + g_{mb})r_O]R_S + r_O\}||R_D$$

- Result is similar to that obtained for a degenerated CS stage

Common-Gate Stage

- Input signal of a common-gate stage may be a current rather than a voltage as shown below



- Input current source exhibits output impedance of *RP*
- To find the "gain" *Vout*/*Iin*, replace *Iin* and *RP* with a Thevenin equivalent and use derived result to write

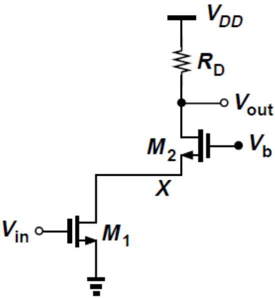
$$\frac{V_{out}}{I_{in}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_P + R_P + R_D} R_D R_P$$

- Output impedance is simply given by

$$R_{out} = \{[1 + (g_m + g_{mb})r_O]R_P + r_O\}||R_D$$

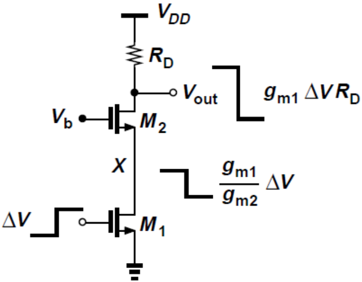
Cascode Stage

- The cascade of a CS stage and a CG stage is called a cascode topology



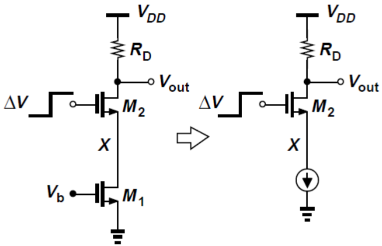
- *M1* generates a small-signal drain current proportional to the small-signal input *Vin* and *M2* simply routes the current to *RD*
- *M1* is called the input device and *M2* the cascode device
- *M1* and *M2* in this example carry equal bias and signal currents
  – Topology also called as “telescopic cascode”

Cascode Stage: Qualitative Analysis



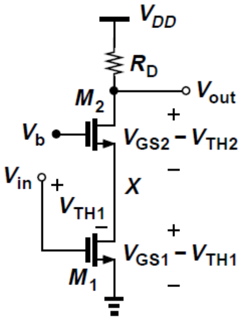
- Assume both transistors are in saturation and $\lambda = \gamma = 0$
- If *Vin* rises by *ΔV*, then *ID1* increases by *gm1ΔV*
- This change in current flows through the impedance seen at *X*, i.e., the impedance seen at the source of *M2*, which is equal to *1/gm2*
- Thus, *VX* falls by an amount given by *gm1ΔV·(1/gm2)*
- This change in *ID1* also flows through *RD*, producing a drop of *gm1ΔVRD* in *Vout*, just as in a simple CS stage

Cascode Stage: Qualitative Analysis



- **Consider the case when *Vin* is fixed and *Vb* increases by *ΔV***
- **Since *VGS1* is constant and *rO1*=∞, *M1* can be replaced by an ideal current source**
- **For node *X*, *M2* operates as a source follower, it senses an input *ΔV* at its gate and generates an output at *X***
- **With *λ* = *γ* = 0, the small-signal voltage of the follower is unity regardless of RD**
- ***VX* rises by *ΔV, but Vout* does not change since *ID2=ID1=constant, thus voltage gain from Vb to* Vout *is zero***

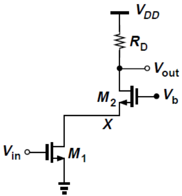
Cascode Stage: Bias Conditions

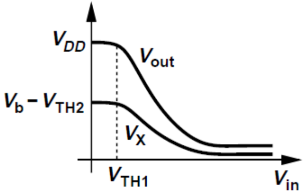


- For *M1* to operate in saturation, we must have $V_X \geq V_{in} - V_{TH1}$
- If *M1* and *M2* are both in saturation, *M2* operates as a source follower and *VX* is primarily determined by *Vb*: $V_X = V_b - V_{GS2}$
- Thus, $V_b - V_{GS2} \geq V_{in} - V_{TH1}$ and hence
  $V_b > V_{in} + V_{GS2} - V_{TH1}$

- For *M2* to be saturated, $V_{out} \geq V_b - V_{TH2}$
- Thus,
$$V_{out} \geq V_{in} - V_{TH1} + V_{GS2} - V_{TH2}$$
$$= (V_{GS1} - V_{TH1}) + (V_{GS2} - V_{TH2})$$
  if *Vb* is chosen to place *M1* at the edge of saturation
- Minimum output level for which both transistors are in saturation is equal to the sum of overdrives of *M1* and *M2*
- Addition of *M2* to the circuit reduces the output voltage swing by at least its overdrive voltage

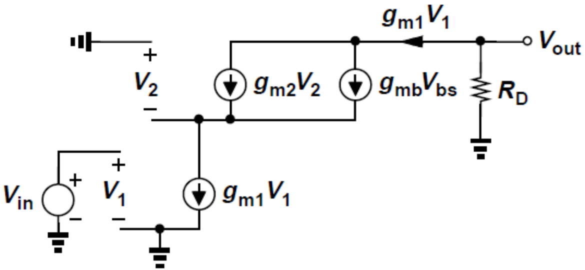
Cascode Stage: Large-Signal Behavior





- For $V_{in} \le V_{TH1}$, $M1$ and $M2$ are off, $V_{out} = V_{DD}$, and $V_X \approx V_b - V_{TH2}$
- As V_{in} exceeds V_{TH1}, $M1$ draws current, and V_{out} drops
- Since I_{D2} increases, V_{GS2} must increase as well, causing V_X to fall
- As V_{in} becomes sufficiently large, two effects can occur:
  - V_X falls below V_{in} by V_{TH1}, forcing $M1$ into the triode region
  - V_{out} drops below V_b by V_{TH2}, driving $M2$ into triode region
- Depending on device dimensions and R_D and V_b, one effect may occur before the other

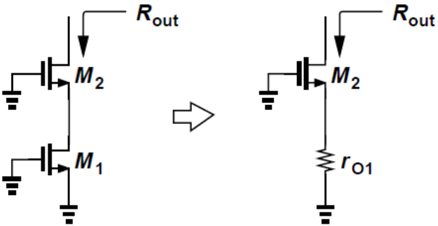
Cascode Stage: Small-signal characteristics



- Assume both transistors operate in saturation and λ=0
- Voltage gain is equal to that of a common-source stage because the drain current produced by the input device must flow through the cascode device
- This result is independent of the transconductance and body effect of *M2*, the cascode device
- Can be verified using *Av* = *-GmRout*

Cascode Stage: Output Impedance

- Important property of the cascode structure is its high output impedance



- For calculation of *Rout*, the circuit can be viewed as a common-source stage with a degeneration resistor equal to *rO1*
- Thus,

$$R_{out} = [1 + (g_{m2} + g_{mb2})r_{O2}]r_{O1} + r_{O2}$$

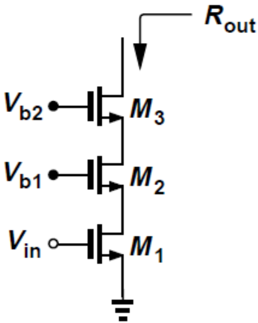
- Assuming g

$$R_{out} \approx (g_{m2} + g_{mb2})r_{O2}r_{O1}$$

- M2 boosts the output impeda *(gm2+gmb2)rO2*

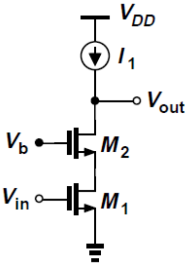
Triple Cascode

- Cascoding can be extended to three or more stacked devices to achieve higher output impedance
- But required additional voltage headroom makes it less attractive
- For a triple cascode, the minimum output voltage is equal to the sum of three overdrive voltages



Cascode stage with current source load

- Voltage gain can be maximized by maximizing *Gm* and/or *Rout*
- Since *Gm* is typically determined by the transconductance of a transistor and has trade-offs with the bias current and device capacitances, it is desirable to increase voltage gain by maximizing *Rout*

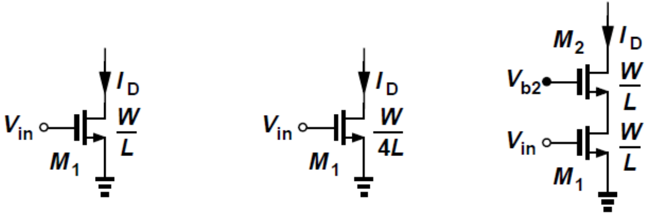


$$G_m \approx g_{m1}$$

$$R_{out} \approx (g_{m2}+g_{mb2})r_{O2}r_{O1} \qquad A_v = (g_{m2}+g_{mb2})r_{O2}g_{m1}r_{O1}$$

- If both *M1* and *M2* operate in saturation, and yeilwdddddddddddd yielding

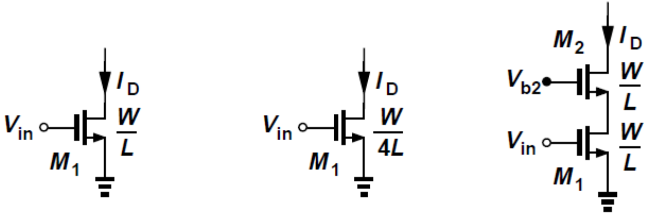
Cascode Stage vs Increasing Length



(a) (b) (c)

- **Increasing length of the input transistor for a given bias current increases the output impedance**
- **Suppose the length of the input transistor is quadrupled while the width remains constant**
- **Since** $I_D = (1/2)\mu_n C_{ox}(W/L)(V_{GS} - V_{TH})^2$**, the overdrive voltage is doubled and the transistor consumes the same amount of voltage headroom as does a cascode stage, i.e., circuits in (b) and (c) impose equal voltage swing constraints**

Cascode Stage vs Increasing Length



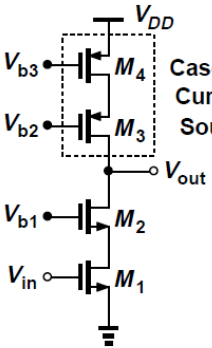
(a) (b) (c)

- **Since**

$$g_m r_O = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}\frac{1}{\lambda I_D}$$

- **And** $\lambda \propto 1/L$**, quadrupling *L* only doubles the value of *gmrO* while cascoding results in an output impedance of roughly *gmrO2***
- **Transconductance of *M1* in (b) is only half of that in (c), degrading the performance**
- **For a given voltage headroom, the cascode structure provides a higher output impedance**

Cascode Structure as Current Source



- High output impedance of cascode structure yields a current source closer to the ideal, but at the cost of voltage headroom
- The current source load in a cascode stage can be implemented as a PMOS cascode, exhibiting an impedance equal to

$$[1 + (g_{m3} + g_{mb3})r_{O3}]r_{O4} + r_{O3}$$

- To find the voltage gain, *Gm≈gm1*
- Rout is the parallel combination of the NMOS and PMOS cascode output impedances

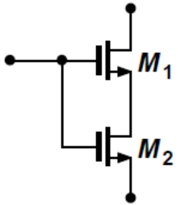
$$R_{out} = \{[1 + (g_{m2} + g_{mb2})r_{O2}]r_{O1} + r_{O2}\}||\{[1 + (g_{m3} + g_{mb3})r_{O3}]r_{O4} + r_{O3}\}$$

- The gain is given by $|A_v| \approx g_{m1}R_{out}$
- For typical values, this is approximated as

$$|A_v| \approx g_{m1}[(g_{m2}r_{O2}r_{O1})||(g_{m3}r_{O3}r_{O4})]$$

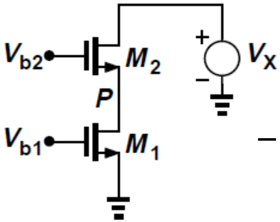
Poor Man's Cascode

- **A "minimalist" cascode current source omits the bias voltage necessary for the cascode device**



- **Called "poor man's cascode", *M2* is placed in the triode region because *VGS1>VTH1* and *VDS2=VGS2-VGS1* < *VGS2-VTH2***
- **If *M1* and *M2* have the same dimensions, the structure is equivalent to a single transistor having twice the length-not really a cascode**
- **In modern CMOS technologies, transistors with different threshold voltages are allowable, allowing *M2* to operate in saturation if *M1* has a lower threshold than *M2***

Poor Man's Cascode: Shielding Property



- High output impedance arises from the fact that if the output node voltage is changed by ΔV, the resulting change at the source of the cascode device is much less
  - Cascode transistor "shields" the input device from voltage variations at the output

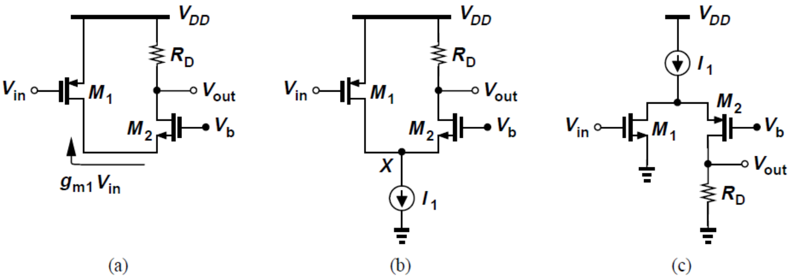
- Shielding property diminishes if cascode device enters triode region
- In above circuit, as *VX* falls below *Vb2-VTH2*, *M2* enters triode region and requires a greater gate-source overdrive to sustain the current drawn by *M1*, therefore

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 [2(V_{b2} - V_P - V_{TH2})(V_X - V_P) - (V_X - V_P)^2]$$

- As *VX* decreases, *VP* also drops to keep *ID2* constant so variation of *VX* is less attenuated as it appears at *P*

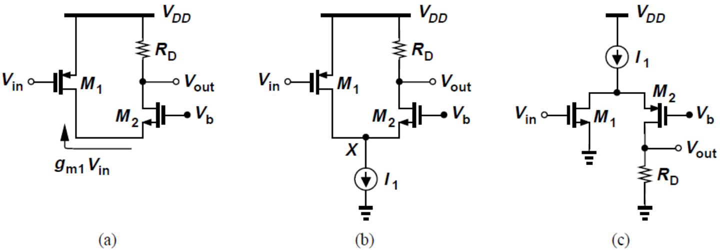
Folded Cascode

- The input device and the cascode device in a cascode structure need not be of the same type



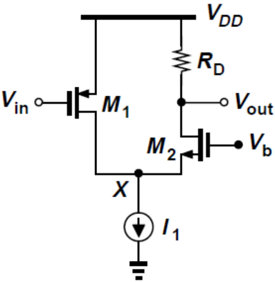
- In the figure above, (a) shows a PMOS-NMOS cascode combination that performs the same function as a telescopic cascode
- In order to bias *M1* and *M2*, a current source must be added as shown in (b)
- |*ID1*| + *ID2* is equal to *I1* and hence constant
- (c) shows an NMOS-PMOS folded cascode

Folded Cascode: Small-signal operation



- If *Vin* becomes more positive, |*ID1*| decreases, forcing *ID2* to increase and hence *Vout* to drop
- The voltage gain and output impedance can be obtained as calculated for the NMOS-NMOS cascode shown earlier
- (b) and (c) are called "folded cascode" stages because the small-signal current is "folded" up [in (b)] or down [in (c)]
- In the telescopic cascode, the bias current is reused whereas those of *M1* and *M2* add up to *I1* in (b) and (c), leading to a higher bias current

Folded Cascode: Large-signal operation

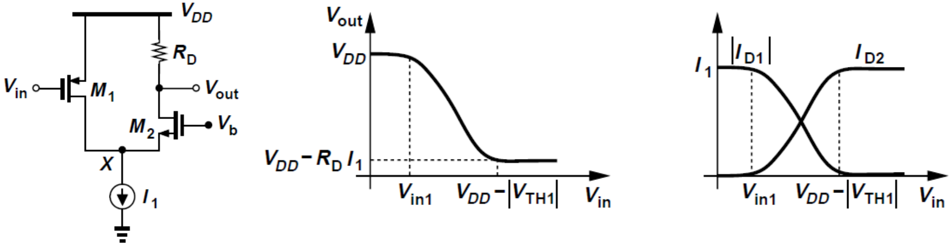


- Suppose *Vin* decreases from *VDD* to zero
- For *Vin* > *VDD*-|*VTH1*|, *M1* is off and *M2* carries all of *I1*, yielding *Vout* = *VDD* - *I1RD*
- For *Vin* < *VDD* - |*VTH1*|, *M1* turns on in saturation, giving

$$I_{D2} = I_1 - \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{DD} - V_{in} - |V_{TH1}|)^2.$$

- As *Vin* drops, *ID2* decreases further, falling to zero if *ID1*=*I1*

Folded Cascode: Large-signal operation



- **This occurs at *Vin* = *Vin1* if**

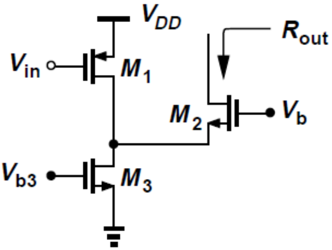
$$\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{DD} - V_{in1} - |V_{TH1}|)^2 = I_1$$

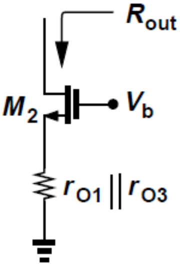
- **Thus,**

$$V_{in1} = V_{DD} - \sqrt{\frac{2I_1}{\mu_p C_{ox}(W/L)_1}} - |V_{TH1}|$$

- **If *Vin* falls below this level, *ID1* tends to be greater than *I1* and *M1* enters the triode region to ensure *ID1=I1***
- **As *ID2* drops, *VX* rises, reaching *Vb-VTH2* for *ID2*=0**
- **As *M1* enters the triode region, *VX* approaches *VDD***

Folded Cascode: Output Impedance





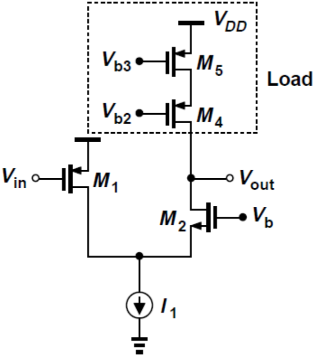
- *M3* operates as the bias current source
- Using earlier results,

$$R_{out} = [1 + (g_{m2} + g_{mb2})r_{O2}](r_{O1} || r_{O3}) + r_{O2}$$

- The circuit exhibits a lower output impedance than a nonfolded (telescopic) cascode

Folded Cascode with cascode load

- To achieve a high voltage gain, the load of a folded cascode can be implemented as a cascode itself



- Increasing the out age amplifiers to obtain a high gain may make the speed of the circuit susceptible to the load capacitance
- A high output impedance itself does not pose a serious issue if the amplifier is placed in a proper feedback loop