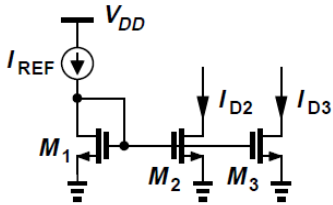
Chapter 12: Bandgap References

General Considerations

- Objective of reference generation is to establish a dc voltage or current independent of the supply and process and has a well-defined behavior with temperature
- Three forms of temperature dependence:
  - Proportional to absolute temperature (PTAT)
  - Constant-*Gm* behavior, i.e., such that the transconductance of certain transistors remains constant
  - Temperature independent
- Two design problems:
  - Supply-independent biasing
  - Definition of temperature variation

Supply-Independent Biasing

- Use of bias currents and current mirrors implicitly assumes a "golden" reference current is available
- As shown in Fig. (a), if *IREF* does not vary with *VDD*, and channel-length modulation of *M2* and *M3* is neglected, then *ID2* and *ID3* remain independent of the supply voltage
- How to generate *IREF*?



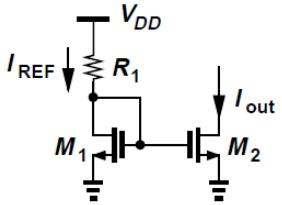
(a)

Supply-Independent Biasing

- As an approximation of a current source, we tie a resistor from *VDD* to the gate of *M1* [Fig. (b)]
- Output current of this circuit is quite sensitive to *VDD*:

$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \cdot \frac{(W/L)_2}{(W/L)_1}$$

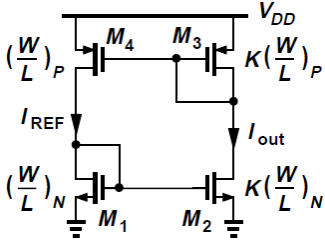
- To arrive at a less sensitive solution, we postulate that the circuit must bias itself, i.e., *IREF* must somehow be derived from *Iout*



(b)

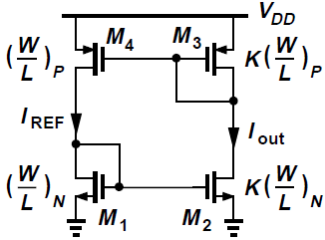
Supply-Independent Biasing

- If *Iout* is to independent of *VDD*, then *IREF* can be a replica of *Iout*
- In circuit below, *M3* and *M4* copy *Iout*, thus defining *IREF*
- *IREF* is "bootstrapped" to *Iout*
- Here, *Iout* = *KIREF* is channel-length modulation is neglected
- Since each diode-connected device feeds from a current source, *Iout* and *IREF* are relatively independent of *VDD*



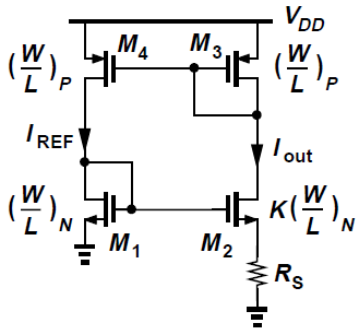
Supply-Independent Biasing

- If *M1 - M4* operate in saturation and □ □ *0*, the circuit is governed by only one equation, *Iout* = *KIREF*, and hence can support any current level
- If we initially force *IREF* to be 10 μA, the resulting *Iout* of *K* □ 10 μA "circulates" around the loop, sustaining these current levels in the left and right branches indefinitely



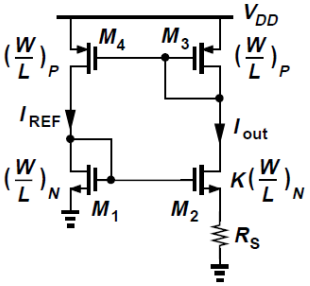
Supply-Independent Biasing

- To uniquely define the currents, we add another constraint to the circuit as in Fig. (a)
- Resistor *RS* decreases the current of *M2* while the PMOS devices need *Iout* = *IREF* due to identical dimensions and thresholds



(a)

Supply-Independent Biasing



(a)

- We can write, $V_{GS1} = V_{GS2} + I_{D2}R_S$, or,

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} + V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox}K(W/L)_N}} + V_{TH2} + I_{out}R_S$$

- Neglecting body effect,

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}}\left(1 - \frac{1}{\sqrt{K}}\right) = I_{out}R_S$$

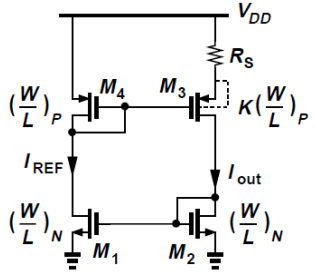
- Hence,

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

- As expected, the current is independent of the supply voltage (but still a function of process and temperature)

Supply-Independent Biasing

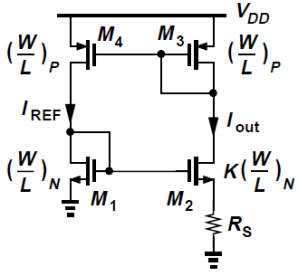
- The assumption *VTH1 = VTH2* introduces some error in the foregoing calculations because sources of *M1* and *M2* are at different voltages
- Simple remedy is to place the resistor at the source of *M3* while eliminating body effect by tying the source and bulk of each PMOS
- Relatively long channel lengths are used for all transistors in the circuit



(b)

Supply-Independent Biasing

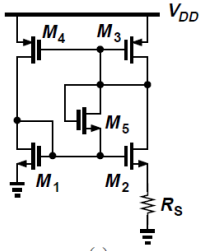
- Important issue in supply-independent biasing is the existence of "degenerate" bias points
- In circuit of Fig. (a), if all transistors carry zero current when supply is turned on, they remain off indefinitely
- Loop can support zero current in both branches
- Circuit can settle in one of two different operating conditions
- Called the "start-up" problem



(a)

Supply-Independent Biasing

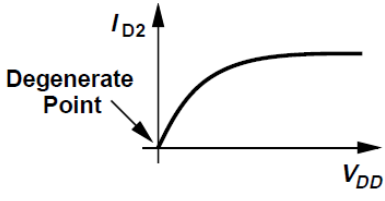
- Start-up problem can be solved by adding a mechanism to drive the circuit out of degenerate bias point when supply is turned on
- In Fig. (a), diode-connected device *M5* provides a current path from *VDD* through *M3* and *M1* to ground upon start-up
- *M3* and *M1*, and hence *M2* and *M4*, cannot remain off
- This technique is practical only if $V_{TH1} + V_{TH5} + |V_{TH3}| < V_{DD}$ and $V_{GS1} + V_{TH5} + |V_{GS3}| > V_{DD}$ to ensure *M5* remains off after start-up



(a)

Supply-Independent Biasing

- Problem of start-up requires careful analysis and simulation
- Supply voltage must be ramped from zero in a dc sweep simulation (such that parasitic capacitances do not cause false start-up) as well as in a transient simulation
- Behavior of the circuit must be examined for each supply voltage



(b)

Temperature-Independent References

- Reference voltages or currents exhibiting little dependence of temperature are useful in analog circuits
- If two quantities having opposite temperature coefficients (TCs) are added with proper weighting, the result displays a zero TC
- For two voltages *V1* and *V2* that vary in opposite directions with temperature, we choose *α1* and *α2* such that $\alpha_1 \partial V_1/\partial T + \alpha_2 \partial V_2/\partial T = 0$, obtaining a reference voltage, $V_{REF} = \alpha_1 V_1 + \alpha_2 V_2$, with zero TC
- Characteristics of bipolar transistors have proven the most reproducible and well-defined quantities that can provide positive and negative TCs

Negative-TC Voltage

- **The base-emitter voltage of bipolar transistors, or more generally, the forward voltage of a *pn*-junction diode exhibits a negative TC**
- **For a bipolar device,** $I_C = I_S \exp(V_{BE}/V_T)$, **where** $V_T = kT/q$
- **Saturation current *IS* is proportional to *μkTni2*, where *μ* denotes the mobility of minority carriers and *ni* is the intrinsic carrier concentration of silicon**
- **The temperature dependence of these quantities is expressed as *□ □ □0Tm*, where *m □ -3/2*, and *ni2□ T3exp[-Eg/(kT)]*, where *Eg □ 1.12 eV* is the bandgap energy of silicon**
- **Thus,**

$$I_S = bT^{4+m} \exp \frac{-E_g}{kT}$$

where *b* is proportionality factor.

Negative-TC Voltage

- **Writing $V_{BE} = V_T \ln(I_C/I_S)$, we can now compute the TC of the base-emitter voltage**
- **For simplicity, we assume *IC* is held constant**
- **Thus,**

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T}$$

- **Using expression derived for *IS*,**

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m} \exp \frac{-E_g}{kT} + bT^{4+m} \left(\exp \frac{-E_g}{kT} \right) \left(\frac{E_g}{kT^2} \right)$$

- **Therefore,**

- **Thus,**

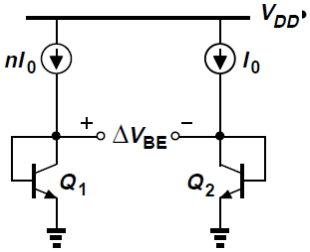
$$\frac{V_T}{I_S} \frac{\partial I_S}{\partial T} = (4+m) \frac{V_T}{T} + \frac{E_g}{kT^2} V_T$$

$$\begin{aligned} \frac{\partial V_{BE}}{\partial T} &= \frac{V_T}{T} \ln \frac{I_C}{I_S} - (4+m) \frac{V_T}{T} - \frac{E_g}{kT^2} V_T \\ &= \frac{V_{BE} - (4+m)V_T - E_g/q}{T}. \end{aligned}$$

Negative-TC Voltage

- TC of the base-emitter voltage at a given temperature *T* depends on the magnitude of *VBE* itself
- With *VBE* ≈ 750 mV and *T* = 300 K, we have $\partial V_{BE}/\partial T \approx -1.5\ \text{mV/K}$
- In old bipolar technologies, where *IC/IS* was relatively small, *VBE* ≈ 700 mV and $\partial V_{BE}/\partial T \approx -1.9\ \text{mV/K}$ at room temperature
- Modern bipolar transistors operate at much higher current densities, exhibiting *VBE* ≈ 800 mV and hence $\partial V_{BE}/\partial T \approx -1.5\ \text{mV/K}$ at *T* = 300 K
- TC of *VBE* itself depends on temperature, creating error in constant reference generation if the positive-TC quantity exhibits a constant (positive) TC

Positive-TC Voltage



If two BJTs operate at unequal current densities, the difference between their base-emitter voltages is directly proportional to the absolute temperature

- **As shown, if two identical transistors (*IS1* = *IS2*) are biased at collector currents of *nI0* and *I0* and their base currents are negligible,**

$$\begin{aligned}\Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{I_0}{I_{S2}} \\ &= V_T \ln n.\end{aligned}$$

- **Thus, *VBE* difference exhibits a positive-TC**

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n$$

Bandgap Reference

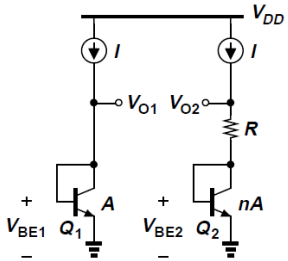
- With positive and negative-TC voltages, we can develop a reference having a nominally zero TC
- We write $V_{REF} = \alpha_1 V_{BE} + \alpha_2 (V_T \ln n)$, where *VT* ln *n* is the difference between the base-emitter voltages of two BJTs operating at different current densities
- At room temperature, $\partial V_{BE}/\partial T \approx -1.5\,\text{mV/K}$ whereas $\partial V_T/\partial T \approx +0.087\,\text{mV/K}$, we set *α1=1* and choose α2ln *n* such that $(\alpha_2 \ln n)(0.087\ \text{mV/K}) = 1.5\ \text{mV/K}$
- That is, $\alpha_2 \ln n \approx 17.2$, indicating that, for a zero TC:

$$\begin{aligned} V_{REF} &\approx V_{BE} + 17.2 V_T \\ &\approx 1.25\ \text{V}. \end{aligned}$$

- Need to devise a circuit that adds *VBE* to *17.2VT*

Bandgap Reference

- Consider the circuit shown below
- Base currents are assumed negligible
- Transistor *Q2* consists of *n* unit transistors in parallel, and *Q1* is a unit transistor
- If somehow *VO1* and *VO2* are forced to be equal, then *VBE1* = *RI* + *VBE2* and *RI* = *VBE1* – *VBE2* = *VT* ln *n*
- Thus, *VO2* = *VBE2* + *VT* ln *n*, suggesting that *VO2* can serve as a temperature-independent reference if ln *n* ≈ 17.2 (while *VO1* and *VO2* remain equal)

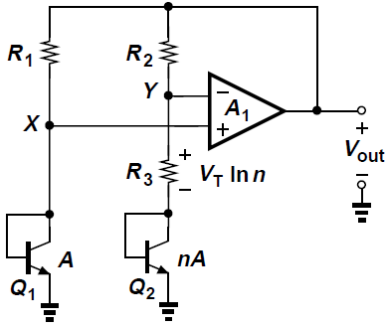


Bandgap Reference

- **Three modifications needed for previous circuit to be practical:**

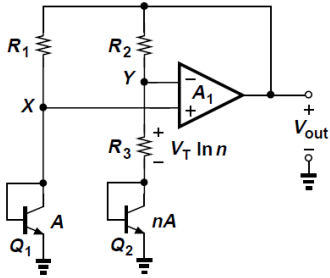
1) **A mechanism must be added to guarantee *VO1* = *VO2***
2) **Since ln *n* = *17.2* translates to a prohibitively large n, the term *RI* = *VT* ln *n* must be scaled up by a reasonable factor**
3) **VO2 cannot become temperature-independent because *VO2* ≈ *VBE1* ≈ *800 mV* whereas for temperature-independence, *VO2* = *VBE2* + *17.2VT* ≈ *1.25* V**

Bandgap Reference



- **Above implementation accomplishes all three tasks**
- **Amplifier *A1* senses *VX* and *VY*, driving the top terminals of *R1* and *R2* (*R1* = *R2*) such that *X* and *Y* settle to approximately equal voltages**
- **The reference voltage is obtained at output of the amplifier (rather than at node *Y*)**

Bandgap Reference

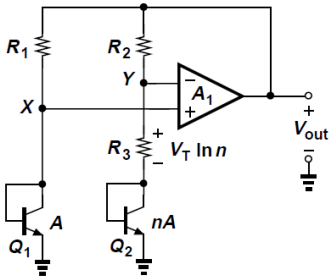


- **Following earlier analysis, *VBE1 – VBE2 = VT* ln *n*, arriving at a current of *VT* ln *n*/*R3* through the right branch and hence an output voltage of**

$$\begin{aligned} V_{out} &= V_{BE2} + \frac{V_T \ln n}{R_3}(R_3 + R_2) \\ &= V_{BE2} + (V_T \ln n)\left(1 + \frac{R_2}{R_3}\right) \end{aligned}$$

- **For a zero TC, we must have *(1+R2/R3)*ln *n* ≈ *17.2*, for example *n = 31* and *R2/R3 = 4***

Bandgap Reference: Issues



(1) Collector Current Variation:

- **Circuit violates earlier assumption: *IC1* and *IC2*, given by (*VT* ln *n*)/*R*3, are proportional to *T*, whereas**

$$\partial V_{BE}/\partial T \approx -1.5\ \text{mV/K}$$

a constant current

- **Assume *IC1* = *IC2* □ (*VT* ln *n*)/*R3***

- **Including $\partial I_C/\partial T$ in the equation for TC of *VBE*,**

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\frac{I_C}{I_S} + V_T\left(\frac{1}{I_C}\frac{\partial I_C}{\partial T} - \frac{1}{I_S}\frac{\partial I_S}{\partial T}\right)$$

- **Since $\partial I_C/\partial T \approx (V_T \ln n)/(R_3 T) = I_C/T$,**

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\frac{I_C}{I_S} + \frac{V_T}{T} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}$$

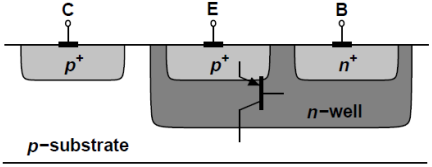
- **Thus, the TC is slightly less negative than -1.5 mV/K**

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (3+m)V_T - E_g/q}{T}$$

Bandgap Reference: Issues

(2) Compatibility with CMOS Technology:

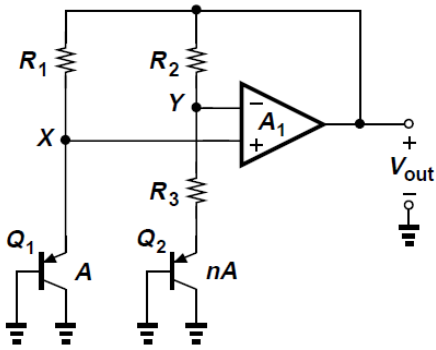
- **We must seek structures in a standard CMOS technology that exhibit negative- and positive-TC characteristics**
- **In *n*-well processes, a *pnp* transistor can be formed as depicted below**
- **A *p*+ region (same as S/D region of PFETs) inside an *n*-well serves as the emitter and the *n*-well itself as the base**
- **The *p*-type substrate acts as the collector and is connected to the most negative supply (usually ground)**



Bandgap Reference: Issues

(2) Compatibility with CMOS Technology:

- **The circuit can be redrawn as shown below**

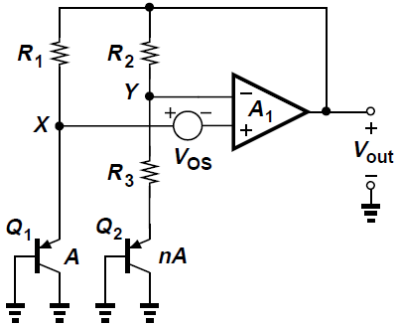


Bandgap Reference: Issues

(3) Op-Amp Offset and Output Impedance:

- **Op amps suffer from input "offsets", i.e., the output voltage of the op amp is not zero if the input is zero**
- **Input offset voltage introduces error in the output voltage**
- **Included below, the effect is quantified as**

$$V_{BE1} - V_{OS} \approx V_{BE2} + R_3 I_{C2}$$



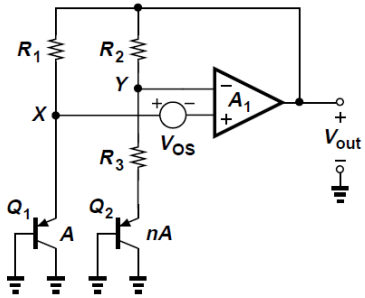
Bandgap Reference: Issues

(3) Op-Amp Offset and Output Impedance:

- **Thus,**

$$\begin{aligned} V_{out} &= V_{BE2} + (R_3 + R_2)\frac{V_{BE1} - V_{BE2} - V_{OS}}{R_3} \\ &= V_{BE2} + \left(1 + \frac{R_2}{R_3}\right)(V_T \ln n - V_{OS}), \end{aligned}$$

- **It is assumed that *IC2 [] IC1* despite the offset voltage**
- ***VOS* is amplified by *1+R2/R3*, introducing error in *Vout***



Bandgap Reference: Issues

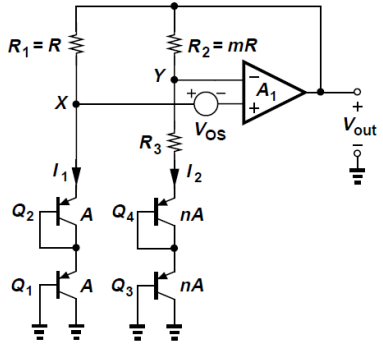
(3) Op-Amp Offset and Output Impedance:

- **Several methods employed to lower the effect of *VOS***
- **First, op amp incorporates large devices in a carefully chosen topology to lower the offset**
- **Second, the collector currents of *Q1* and *Q2* can be ratioed by a factor of *m* such that $\Delta V_{BE} = V_T \ln(mn)$**
- **Third, each branch may use two *pn* junctions in series to double ΔV_{BE}**

Bandgap Reference: Issues

(3) Op-Amp Offset and Output Impedance:

- **Circuit below shows a realization using last two techniques**
- ***R1* and *R2* are ratioed by a factor of *m*, so *I1* = *mI2***
- **Neglecting base currents and assuming *A1* is large, we can write *VBE1* + *VBE2* – *VOS* = *VBE3* + *VBE4* + *R3I2* and *Vout* = *VBE3* + *VBE4* + *(R3+R2)I2***



Bandgap Reference: Issues

(3) Op-Amp Offset and Output Impedance:

•It follows that

$$\begin{aligned} V_{out} &= V_{BE3} + V_{BE4} + (R_3 + R_2)\frac{2V_T \ln(mn) - V_{OS}}{R_3} \\ &= 2V_{BE} + \left(1 + \frac{R_2}{R_3}\right)[2V_T \ln(mn) - V_{OS}]. \end{aligned}$$

•The effect of *VOS* is reduced by the first term in brackets

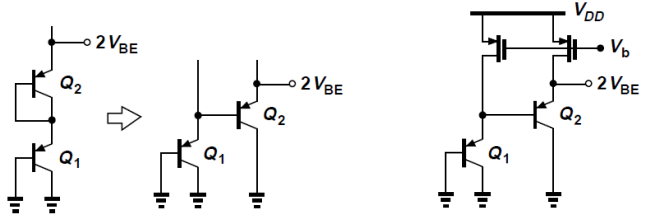
•However, *Vout* □ 2 □ 1.25 V = 2.5 V, a value difficult to generate by the op amp at low supply voltages

•In these circuit, the op amp drives two resistive branches and hence, must provide a low output impedance

Bandgap Reference: Issues

(3) Op-Amp Offset and Output Impedance:

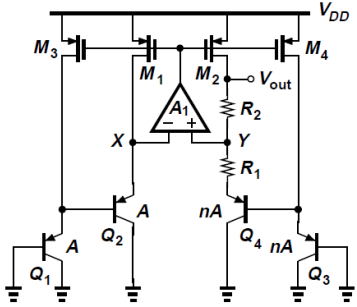
- **The implementation shown on slide 29 is not feasible since collectors of *Q2* and *Q4* are not grounded**
- **To use the bipolar structure of CMOS, we modify the series combination of the diodes shown in Fig. (a), converting one of the diodes to an emitter follower**
- **Both transistors are biased by a PMOS current source rather than a resistor to ensure uniform behavior with temperature [Fig. (b)]**



Bandgap Reference: Issues

(3) Op-Amp Offset and Output Impedance:

- **Overall circuit is shown below, where the op amp adjusts the gate voltage of the PMOS devices so as to equalize *VX* and *VY***
- **Op amp does not experience resistive loading, but the mismatch and channel-length modulation of the PMOS devices introduce error at the output**
- **Low current gain of the "native" *pnp* transistors**



Bandgap Reference: Issues

(4) Feedback Polarity:

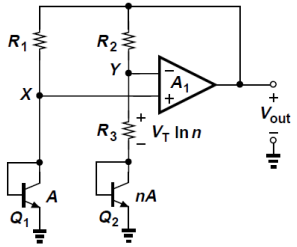
- **In circuit below, feedback signal produced by the op amp returns to both of its inputs, negative feedback factor is given by**

$$\beta_N = \frac{1/g_{m2} + R_3}{1/g_{m2} + R_3 + R_2}$$

- **Positive feedback factor is**

$$\beta_P = \frac{1/g_{m1}}{1/g_{m1} + R_1}$$

- **To ensure an overall negative feedback, *βP* must be less than *βN*, roughly by a factor of two**



Bandgap Reference: Issues

(5) Bandgap Reference:

- **To understand the origin of the terminology "bandgap reference", we rewrite the output voltage equation**

$$V_{REF} = V_{BE} + V_T \ln n$$

- **Hence**

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + \frac{V_T}{T} \ln n$$

- **Setting this to zero and substituting for** $\partial V_{BE}/\partial T$

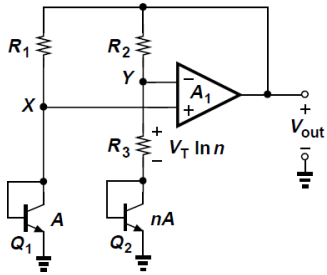
- **Substituting fo**$\frac{V_{BE} - (4+m)V_T - E_g/q}{T} = -\frac{V_T}{T} \ln n$**ltion,**

- ***VREF* is given by a**$V_{REF} = \frac{E_g}{q} + (4+m)V_T$ **numbers: the bandgap voltage of silicon, *Eg/q*, the temperature exponent of mobility, *m*, and the thermal voltage *VT***
- **The term "bandgap" is used because as *T*□*0*, *VREF* □*Eg/q***

Bandgap Reference: Issues

(6) Supply Dependence and Start-Up:

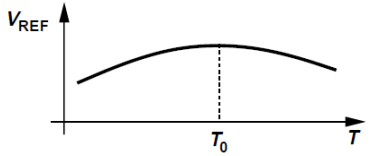
- **In the circuit below, output voltage is relatively independent of supply voltage as long as open-loop gain of the op amp is sufficiently high**
- **Circuit may require a start-up mechanism because if *VX* and *VY* are equal to zero, the input differential pair of the op amp may turn off**
- **Supply rejection of the circuit typically degrades at high frequencies, mandating "supply regulation"**

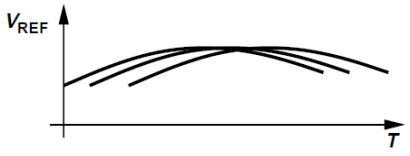


Bandgap Reference: Issues

(7) Curvature Correction:

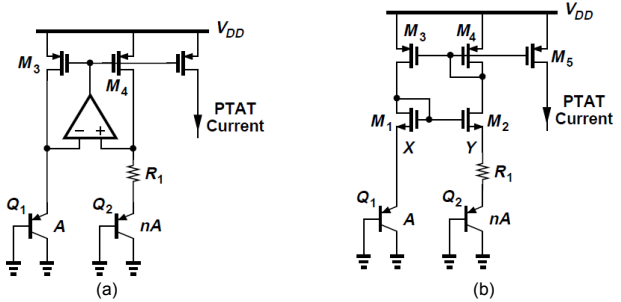
- **Bandgap voltages exhibit a finite "curvature", i.e., their TC is zero at one temperature and positive or negative at others**
- **Curvature arises from temperature variation of base-emitter voltages, collector currents, offset voltages**
- **Many curvature-correction techniques introduced in bipolar bandgap circuits, but rarely used in CMOS counterparts**
- **Samples of CMOS bandgap reference display substantially different zero-TC temperatures due to large offsets and process variations**





PTAT Current Generation

- PTAT currents can be generated by the topology shown in Fig. (a) below
- Alternatively, we can combine the supply-independent biasing scheme with a bipolar core, arriving at circuit in Fig. (b)
- Assume that *M1-M2* and *M3-M4* are identical pairs
- For *ID1 = ID2*, the circuit must ensure that *VX = VY*
- Thus, *ID1 = ID2 = (VT* ln *n)/R1*, yielding the same behavior for *ID5*

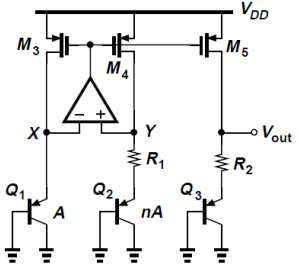


PTAT Current Generation

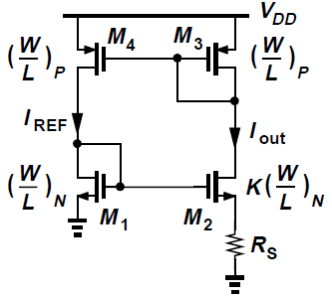
- A modified circuit to provide a bandgap reference voltage is shown below
- Idea is to add a PTAT voltage *ID5R2* to a base-emitter voltage; the output therefore equals

$$V_{REF} = |V_{BE3}| + \frac{R_2}{R_1} V_T \ln n$$

- All PMOS transistors are assumed identical
- The value of *VBE3* and size of *Q3* are somewhat arbitrary so long as their sum gives a zero TC



Constant-*Gm* biasing



- It is often desirable to bias transistors such that their transconductance does not depend on PVT
- Supply-independent bias topology shown can define the transconductance

- Bias current is given by

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N}\frac{1}{R_S^2}\left(1-\frac{1}{\sqrt{K}}\right)^2$$

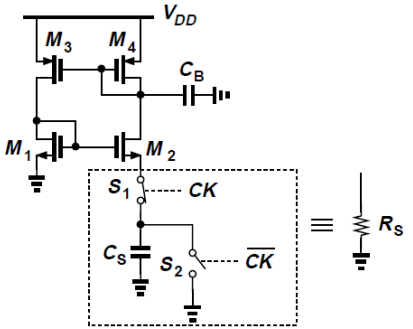
- Thus, transconductance of *M1* equals

$$g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_N I_{D1}}$$
$$= \frac{2}{R_S}\left(1-\frac{1}{\sqrt{K}}\right),$$

- If temperature coefficient of RS is known, different techniques can cancel the temperature dependence

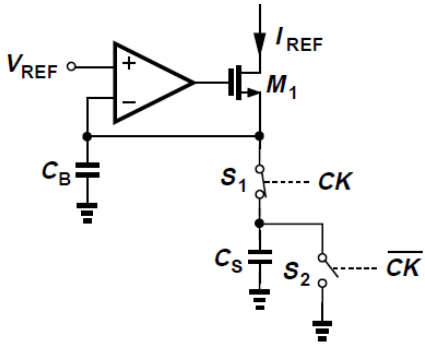
Constant-*Gm* biasing

- When a precise clock frequency is available, *RS* can be replaced by a switched-capacitor equivalent for higher accuracy
- Average resistance of *(CSfCK)-1* is established between source of *M2* and ground, where *fCK* is the clock frequency
- *CB* shunts high-frequency components resulting from switching to ground



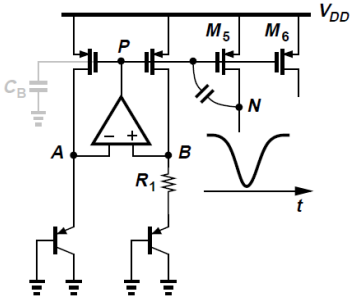
Constant-*Gm* biasing

- Switched-capacitor approach can be applied to other circuits as well
- As shown, a voltage-to-current converter with a relatively high accuracy can be constructed



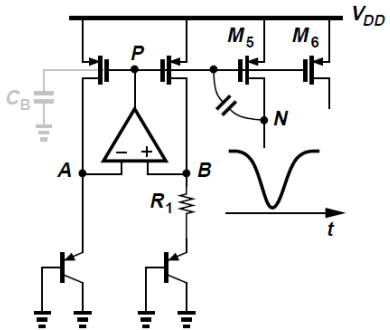
Speed and Noise Issues

- Reference generators are low-frequency circuits, but can impact speed of circuits they feed
- Various building blocks experience "crosstalk" through reference lines
- Caused by finite output impedance of reference generators
- In the configuration below, voltage at node *N* is heavily disturbed by circuit fed by *M5*



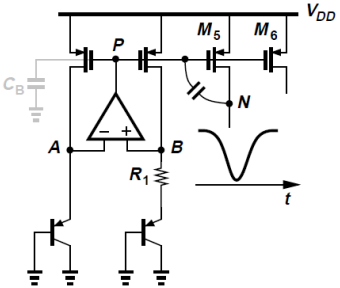
Speed and Noise Issues

- For fast changes in *VN* the op amp cannot maintain *VP* constant and bias currents of *M5* and *M6* experience large transient changes
- Duration of the transient at node *P* may be quite long if op amp has a slow response
- Reference generator may require a high-speed op amp



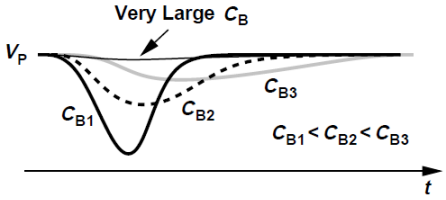
Speed and Noise Issues

- For low-power applications, high-speed op amp may not be feasible
- Alternatively, node *P* in circuit below can be bypassed to ground by a large capacitor *CB* to suppress external disturbances
- For stability of op amp to not degrade with addition of *CB*, op amp must be of one-stage nature
- *CB* must be much greater than the capacitance that couples the disturbance to node *P*

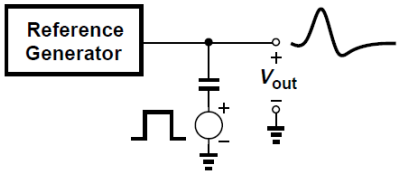


Speed and Noise Issues

- As shown below, if *CB* is not sufficiently large, *VP* experiences a change and takes a long time to return to its original value, degrading the settling speed of circuits biased by reference generator [Fig. (a)]
- Preferable to leave node *P* agile
- In general, response of the circuit must be analyzed by applying a disturbance at the output and observing the settling behavior [Fig. (b)]



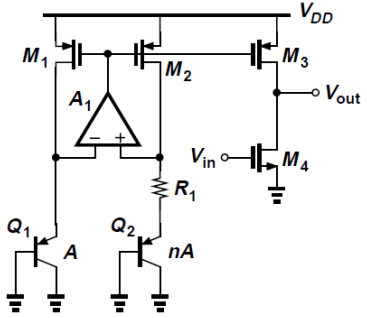
(a)



(b)

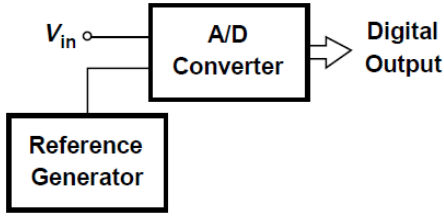
Speed and Noise Issues

- Output noise of reference generators may impact the performance of low-noise circuits
- As shown below, load current source of a CS stage is driven by a bandgap circuit with a current multiplication factor of *N*
- Thus, noise current of *M1* (or *M2*) is multiplied by the same factor as it appears in *M3*
- *M1-M3* carry noise due to the op amp *A1* as well



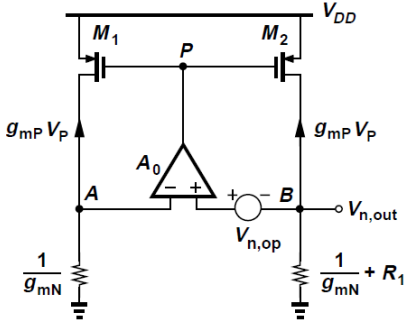
Speed and Noise Issues

- As another example, if a high-precision A/D converter employs a bandgap reference voltage with which the analog input signal is compared, then the noise in the reference is directly added to the input



Speed and Noise Issues

- As a simple example, let us calculate the output noise voltage of circuit below, considering only the input-referred noise voltage of the op amp, *Vn,op*
- Since the small-signal drain currents of *M1* and *M2* are equal, we have $V_{n,out}/(R_1 + g_{mN}^{-1})$ $V_P = -g_{mP}^{-1} V_{n,out}/(R_1 + g_{mN}^{-1})$, obtaining the differential voltage at the input of the op amp as $-g_{mP}^{-1} A_0^{-1} V_{n,out}/(R_1 + g_{mN}^{-1})$



Speed and Noise Issues

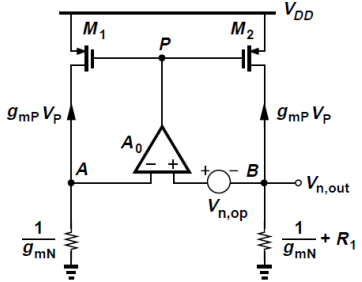
- **Beginning from node A, we can write**

$$\frac{V_{n,out}}{R_1 + g_{mN}^{-1}} \cdot \frac{1}{g_{mN}} - \frac{V_{n,out}}{g_{mP} A_0 (R_1 + g_{mN}^{-1})} = V_{n,op} + V_{n,out}$$

- **Hence,**

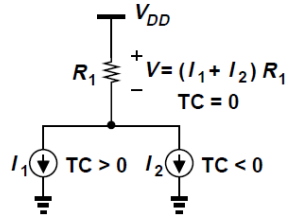
$$V_{n,out} \left[\frac{1}{R_1 + g_{mN}^{-1}} \left(\frac{1}{g_{mN}} - \frac{1}{g_{mP} A_0} \right) - 1 \right] = V_{n,op}$$

- **Since typically** $g_{mP} A_0 \gg g_{mN} \gg R_1^{-1}$, $|V_{n,out}| \approx V_{n,op}$
- **Thus, noise of the op amp directly appears at the output**



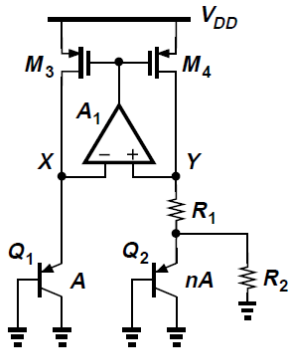
Low-Voltage Bandgap References

- Bandgap voltage obtained previously is around 1.25 V, eluding implementation in today's supplies
- Fundamental limitation of addition of *17.2VT* to one *VBE* to achieve a zero TC
- It may be possible to add two currents with positive and negative TCs and convert the result to an arbitrary voltage that has a zero TC
- We can readily generate a PTAT current given by *VT ln n/R*
- We need another current of the form *VBE/R* with a negative TC



Low-Voltage Bandgap References

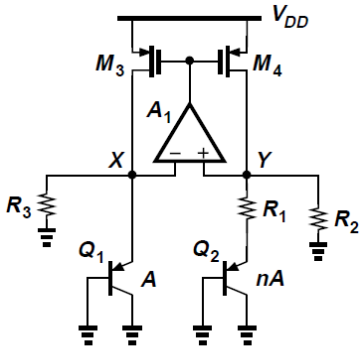
- Returning to original bandgap circuit of Fig. (a), note that $|ID4| = VT \ln n/R1$ is a PTAT current
- Resistor *R2* is placed in parallel with *Q2*
- *R1* now carries an additional current of $|VBE2|/R2$, i.e., a current with a negative TC
- PTAT behavior is now disturbed because $IC1 \neq IC2$



(a)

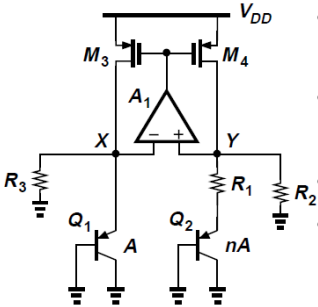
Low-Voltage Bandgap References

- A simple modification as shown in Fig. (b) can solve this issue
- We tie *R2* from *Y* to ground and place another resistor in parallel with *Q1*
- This topology lends itself to low-voltage implementation, requiring a minimum *VDD* of *VBE1* + |*VDS3*|



(b)

Low-Voltage Bandgap References



(b)

- To analyze the circuit, we observe that $V_X \approx V_Y \approx |V_{BE1}|$s
- $I_{D3} = I_{D4}$
- This yiel$I_{C1} + \frac{|V_{BE1}|}{R_3} = I_{C2} + \frac{|V_{BE1}|}{R_2}$
- We still hav$I_{C1} = I_{C2} \qquad R_2 = R_3$ and hence

$$|V_{BE1}| = |V_{BE2}| + I_{C2}R_1$$

$$I_{C2} = V_T \ln n / R_1$$

- **This current and the current flowing through *R2*, |*VBE1*|/*R2*, constitute |*ID4*|:**

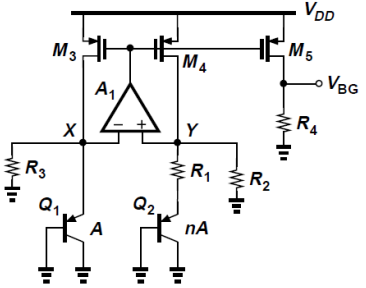
$$\begin{aligned} |I_{D4}| &= \frac{V_T \ln n}{R_1} + \frac{|V_{BE1}|}{R_2} \\ &= \frac{1}{R_2}\left(|V_{BE1}| + \frac{R_2}{R_1} V_T \ln n\right) \end{aligned}$$

Low-Voltage Bandgap References

- Selecting *(R2/R1)VT* ln *n* approximately equal to 17.2*VT* renders a zero TC for *ID4*
- This current is then copied and passed through a resistor to generate a zero-TC voltage [Fig. (c)]:

$$V_{BG} = \frac{R_4}{R_2}\left(|V_{BE1}| + \frac{R_2}{R_1} V_T \ln n\right)$$

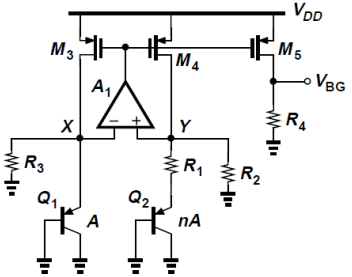
- We choose *(R2/R1)*ln *n* ≈ *17.2*, observing that *VBG* has a zero TC and its value can be lower than 1.25 V



(c)

Low-Voltage Bandgap References

- Instructive to estimate the lowest supply voltage with which circuit of Fig. (c) can operate properly
- With large bipolar transistors and a small bias current, e.g., 10 □A, the base-emitter voltage can be as low as 0.7 V
- Wide PMOS devices allow a |*VDS*| of about 50 mV
- Minimum *VDD* of 0.75 V is achievable
- In this case, *R4* tends to be a large resistor, e.g., 50 kΩ



(c)

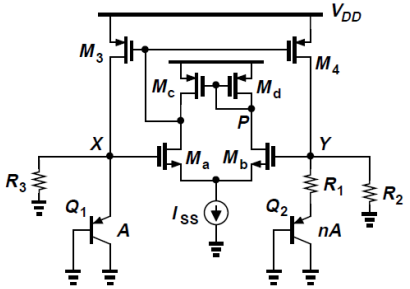
Low-Voltage Bandgap References

- **The op amp can be realized as a five-transistor OTA**
- **OTA design guidelines:**

(1) **Large transistor dimensions to minimize flicker noise and offset**

(2) **VGS of *Ma* and *Mb* plus headroom requires by *ISS* must not exceed |*VBE1*|**

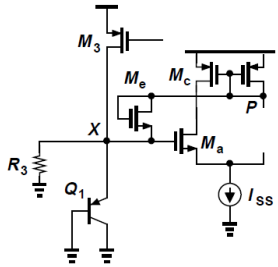
(3) **Transistors are chosen long enough to yield reasonable loop gain**



(a)

Low-Voltage Bandgap References

- Foregoing topology must include a start-up mechanism, else the circuit begins with *VX = VY = 0*, *Ma* and *Mb* remain off, and so do *M3* and *M4*
- Since, with *VDD* < 1 V, the voltage difference between node *P* and node *X* is initially positive but finally negative, we can tie a diode-connected NMOS transistor between these two nodes to ensure start-up [Fig. (b)]
- Alternatively, it can be connected between *X* and *VDD*



(b)

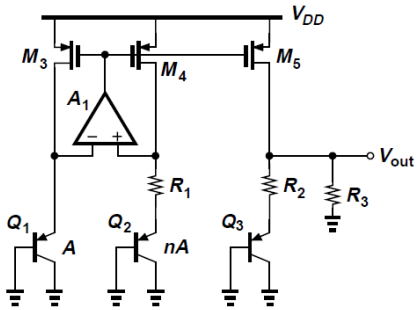
Low-Voltage Bandgap References

- Another low-voltage bandgap circuit can be derived by simply a tying a resistor from the output to ground
- As shown, the circuit allows some of *ID5* to flow through *R3*:

$$|I_{D5}| = \frac{V_{out}}{R_3} + \frac{V_{out} - |V_{BE3}|}{R_2}$$

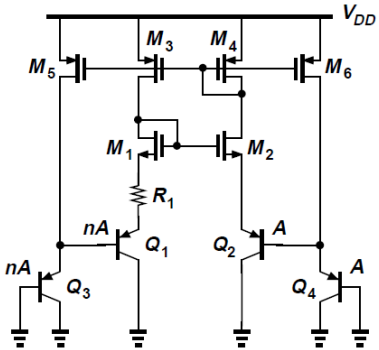
- If the PMOS devices are identical, $|I_{D5}| = V_T \ln n / R_1$

$$V_{out} = \frac{R_3}{R_2 + R_3}\left(|V_{BE3}| + \frac{R_2}{R_1} V_T \ln n\right)$$



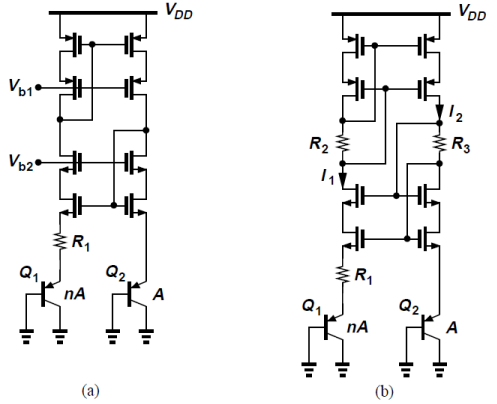
Case Study

- We study a bandgap reference circuit designed for high-precision analog systems
- A simplified version of the core is shown below, with two series base-emitter voltages in each branch to reduce the effect of MOSFET mismatches
- PMOS current mirror ensures equal collector currents for *Q1-Q4*



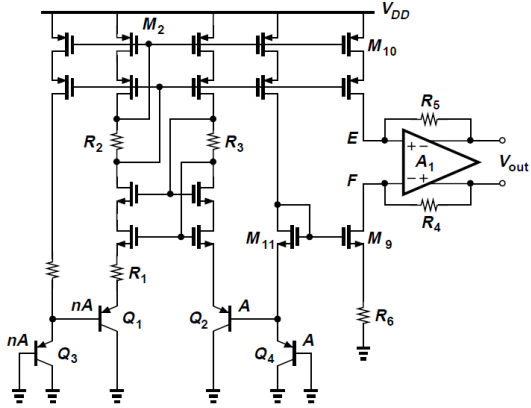
Case Study

- Channel-length modulation of MOS devices remains a significant issue
- To resolve this issue, each branch can employ both NMOS and PMOS cascode topologies
- Fig. (a) shows how the low-voltage cascode is utilized
- Fig. (b) shows a “self-biased” version



Case Study

- The bandgap circuit is designed to generate a floating reference, as shown in figure below
- *ID9* and *ID10* flow through *R4* and *R5* respectively
- *M11* sets the gate voltage of *M9* at *VBE4* + *VGS11*, establishing a voltage of *VBE4* across *R6* if *M9* and *M11* are identical

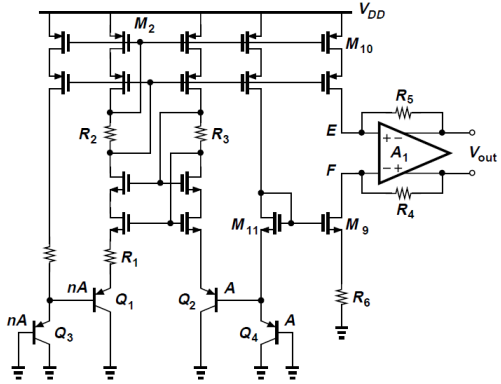


Case Study

- Thus, *ID9 = VBE4/R6*, yielding *VR4 = VBE4(R4/R6)*
- If *M10* is identical to *M2*, then *|ID10| = 2(VT* ln *n)/R1* and hence *VR5 = 2(VT* ln *n)(R5/R1)*
- Since the op amp ensures *VE ≅ VF*, we have

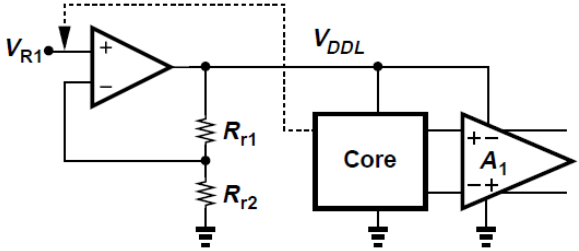
$$V_{out} = \frac{R_4}{R_6} V_{BE4} + 2\frac{R_5}{R_1} V_T \ln n$$

- Zero TC with proper choice of resistor ratios and *n*



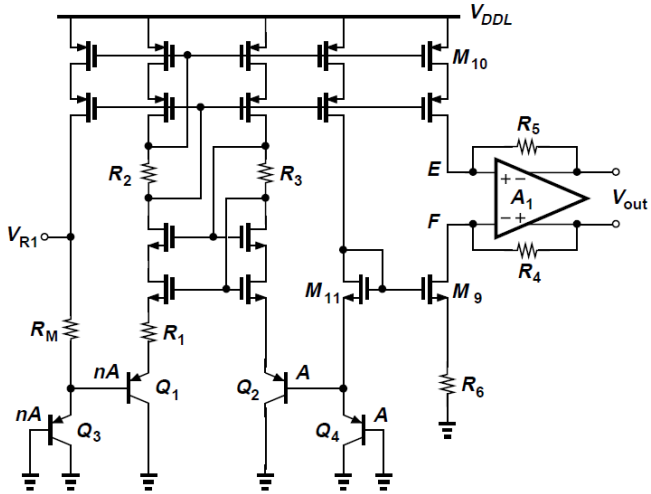
Case Study

- To enhance supply rejection, the design regulates the supply voltage of the core and the op amp
- Idea is to generate a local *VDDL*, that is defined by a reference *VR1* and the ratio of *Rr1* and *Rr2*
- Remains relatively independent of the supply voltage



Case Study

- To minimize dependence of *VR1* on the supply, it is established inside the core, as shown below
- *RM* is chosen such that *VR1* is a bandgap reference



Case Study

- Overall implementation is shown below, along with a start-up circuit
- Operating from a 5-V supply, reference generator produces a 2-V output consuming 2.2 mW
- Supply rejection is 94 dB at low frequencies and drops to 58 dB at 100 kHz