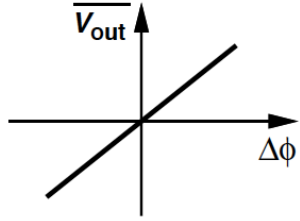
Chapter 16: Phase-Locked Loops

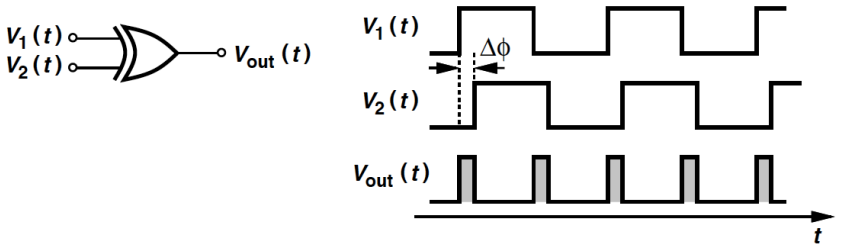
Phase Detector (PD) Definition

- **PLL: A feedback system that compares the output phase with the input phase.**
- **Phase detector: A circuit whose $\overline{V_{out}}$ is linearly proportional to the phase difference, Δϕ, between its two inputs:**



- **KPD: "Gain" of the PD = Slope of the line (V/rad).**

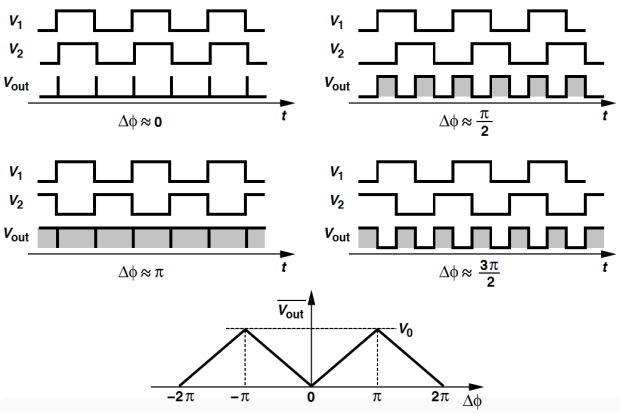
XOR Gate as PD



- As Δϕ varies, so does the width of the output pulses dc level proportional to Δϕ.
- XOR circuit produces error pulses on both rising and falling edges.
- Other PDs may respond only to positive or negative transitions.

Example 16.1

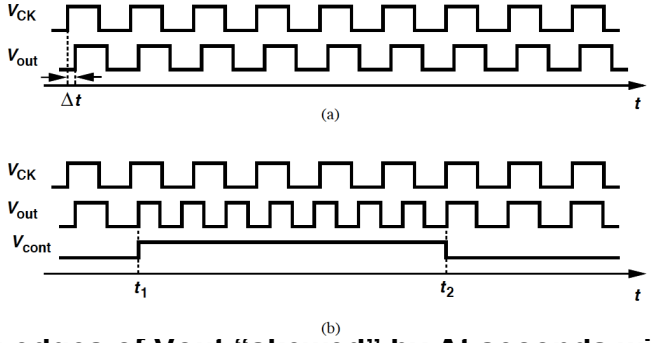
If output swing of the XOR = V0 volts, what is a the gain of a phase detector? Plot the input-output characteristics of the PD.



Solution:

- **Gain = V0/π.**
- **The input-output characteristics are plotted on the left:**
  - **The average output voltages rises to [V0/π] × π/2 = V0/2 for Δϕ = π/2 and V0 for Δϕ = π.**
  - **For Δϕ > π, the average begins to drop.**
- **Periodic characteristic: Both negative and positive gains.**

Skewed Waveforms Alignment



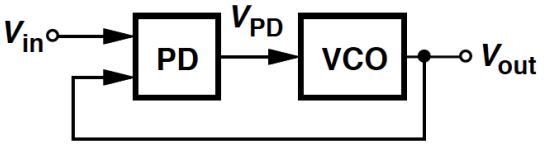
(a): Rising edges of Vout "skewed" by Δt seconds with respect to VCK.

Assume the VCO has a single Vcont. To vary the phase, we must vary the frequency and allow $\phi = \int (\omega_0 + K_{VCO} V_{cont}) dt$ **.**

(b): At t = t1, the VCO frequency stepped to a higher value □ phase accumulated faster and phase error decreases □ t = t2: phase error = 0.

PD & VCO in Feedback Loop

- **Output phase of a VCO can be aligned with phase of reference if**
  - **(1) frequency of the VCO is changed momentarily,**
  - **(2) a phase detector is used to determine when they are aligned.**

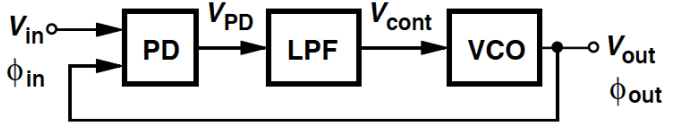


(a)

- **Task of "phase locking".**
- **(a): The PD compares the phase of Vout and Vin □ generates an error that varies the frequency until the phases are aligned.**

Basic PLL Topology

- Topology (a) (Slide 6) must be modified because VPD
  - (1) consists of a dc component (desirable) & high-frequency components (undesirable),
  - (2) must be filtered as Vcont must remain quiet in the steady state.



(b)

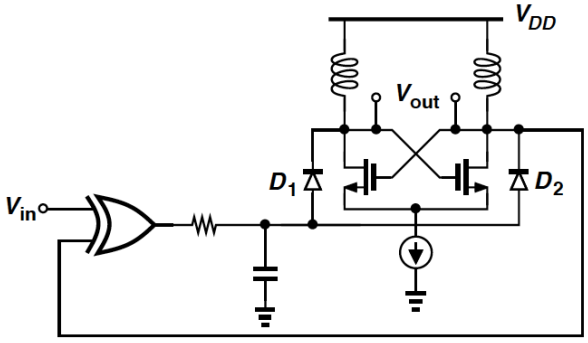
- (b): Basic PLL topology.
- We define the loop of (b) to be locked if $\phi_{out} - \phi_{in}$ is constant:

$$\frac{d\phi_{out}}{dt} - \frac{d\phi_{in}}{dt} = 0 \quad \square \quad \omega_{out} = \omega_{in}.$$

Example 16.2

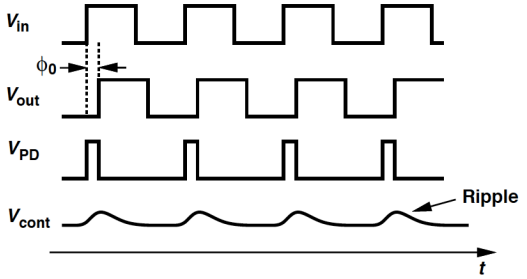
Implement a simple PLL in CMOS technology.

Solution



- **Utilize an XOR gate as the phase detector.**
- **The VCO configured as a negative-Gm LC oscillator whose frequency is tuned by varactor diodes.**

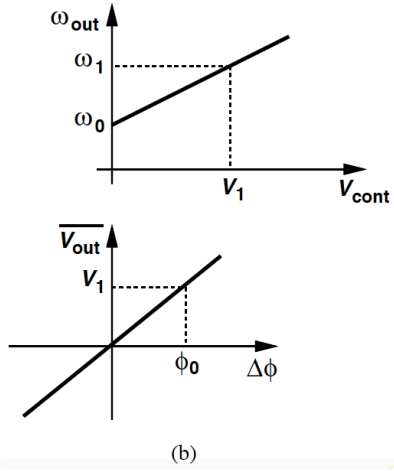
PLL Waveforms in Locked Condition



(a)

- **(a): Vin & Vout exhibit a small phase difference but equal frequencies.**
- **PD: Pulses as wide as the skew between input & output.**
- **Low-pass filter extracts the dc component of VPD □ apply result to the VCO (Assume gain of LPF = 1).**
- **“Ripple”: Small pulses in VLPF.**

Calculation of Phase Error



- (b): VCO and PD characteristics.
- If input/output frequencies = ω1, the required Vcont is unique and = V1.
- Since $\omega_{out} = \omega_0 + K_{VCO}V_{cont}$ and $\overline{V_{PD}} = K_{PD}\Delta\phi$ we can write:

and $V_1 = \frac{\omega_1 - \omega_0}{K_{VCO}},$

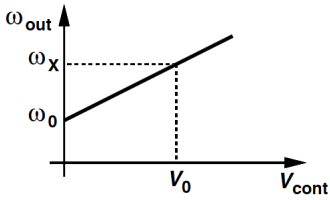
$$\phi_0 = \frac{V_1}{K_{PD}} = \frac{\omega_1 - \omega_0}{K_{PD}K_{VCO}}.$$

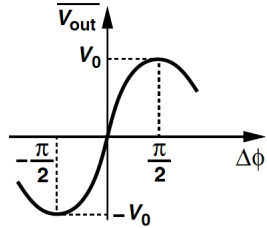
- Two important points:
  - Phase error varies as input frequency of the PLL varies.
  - To minimize phase error KPDKVCO maximized.

Example 16.3

A PLL incorporates a VCO and a PD having the characteristics shown below. Explain what happens as the input frequency varies in the locked condition.

Solution

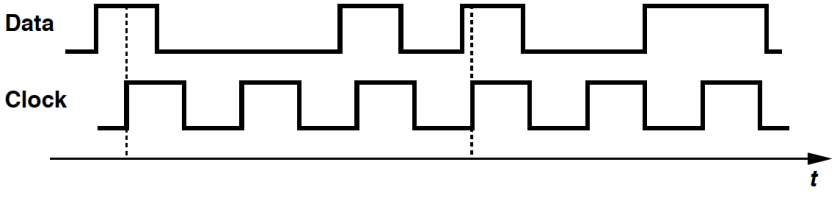




- **PD characteristic is relatively linear near the origin but exhibits a small-signal gain of zero if Δϕ = ±π/2, where the average output is equal to ±V0.**
- **If the input frequency is high enough (= ωx) to dictate Vcont = V0, the PD must operate at the peak of its characteristic, at which, however, PD gain = 0 and the feedback loop fails.**
- **The circuit cannot lock if the input frequency reaches ωx.**

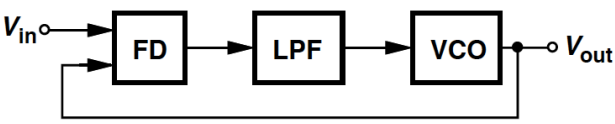
Equality of Input & Output Frequencies (I)

- The exact equality of the input and output frequencies of a PLL in the locked condition is a critical attribute.
- Even a very small (deterministic) frequency error may prove unacceptable.
- E.g. (below): A data stream is to be processed synchronously by a clocked system. Even a slight difference between the data rate and the clock frequency results in a “drift” □ errors.

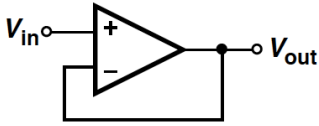


Equality of Input & Output Frequencies (II)

- The equality would not exist if the PLL compared the input and output frequencies rather than phases.



(a)



(b)

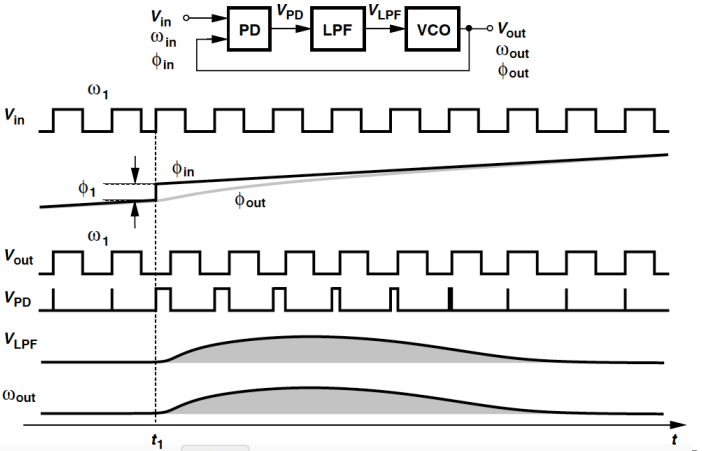
- (a): A loop employing a FD would suffer from a finite difference between ωin and ωout due to various mismatches and other nonidealities.
- (b): An analogy with the unity-gain feedback circuit. Even if the op-amp's open-loop gain is infinity, the input-referred offset voltage leads to a finite error between Vin and Vout.

Response of PLL to Phase Step (I)

- **For a PLL in the locked condition, assume:** $V_{in}(t) = V_A \cos \omega_1 t$

$$V_{out}(t) = V_B \cos(\omega_1 t + \phi_0)$$

- **The input experiences a phase step of ϕ1 at t = t1. The phase step manifests itself as a rising edge in Vin that occurs earlier (or later) than the periodicity would dictate.**



Response of PLL to Phase Step (II)

- Output of the LPF does not change instantaneously the VCO initially continues to oscillate at ω1.
- The growing phase difference between input & output creates wide pulses at the output of PD force VLPF to rise.
- VCO frequency begins to change, to minimize the phase error.
- Then if the loop is to return to lock, ωout eventually goes back to ω1 VLPF & ϕout – ϕin also returns to original values.
- The variation in the VCO frequency is such that:

$$\int_{t1}^{\infty} \omega_{out} dt = \phi_1.$$

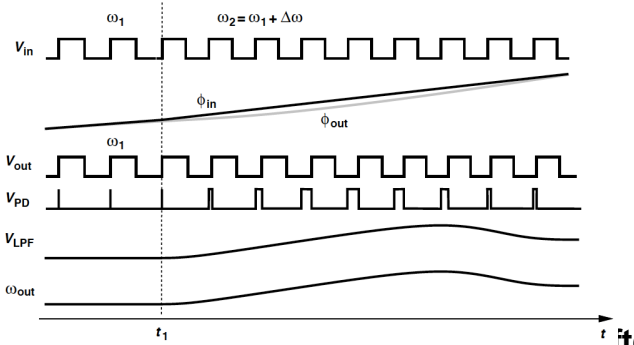
 when the loop settles, the output is:

$$V_{out}(t) = V_B \cos[\omega_1 t + \phi_0 + \phi_1 u(t - t_1)].$$

 ϕout gradually "catches up" with ϕin.

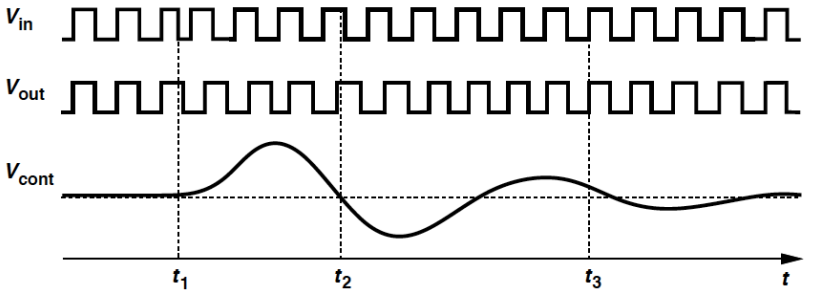
Response of PLL to Small Frequency Step

- Examine the response of PLLs to Δω at t = t1:



- The VCO continues to oscillate at ω1 immediately after t1.
  - PD generates increasingly wider pulses, VLPF rises with time.
- As ωout -> ω1 + Δω, the width of the pulses generated by the PD decreases, eventually settling to $(\omega_1 + \Delta\omega - \omega_0)/K_{VCO}$.
- If the input frequency is varied slowly, the PLL "tracks" ωin.

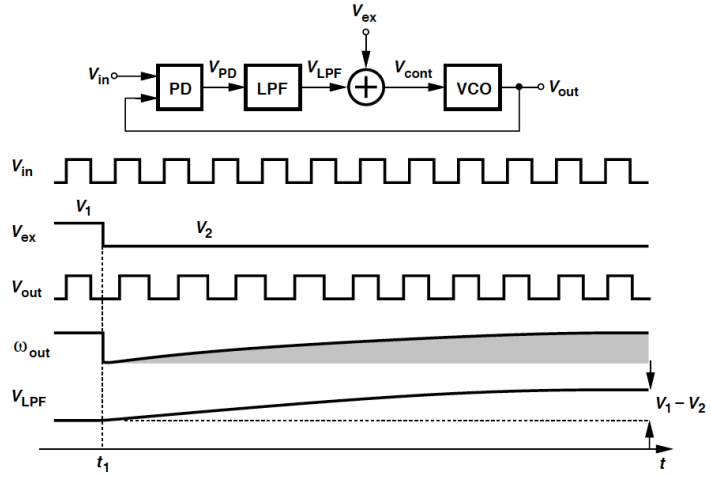
Example of Phase Step Response



- At t = t2, output frequency equals its final value, but the loop continues the transient because the phase error deviates from the required value.
- At t = t3, the phase error is equal to its final value but the output frequency is not.
- For the loop to settle, both the phase and the frequency must settle to proper values.

Example 16.4 (I)

In the below PLL, Vex is added to the output of the low-pass filter. (a) Determine the phase error and VLPF if the loop is locked and Vex = V1. (b) Suppose Vex steps from V1 to V2 at t = t1. How does the loop respond?



Example 16.4 (II)

Solution

•(a) If the loop is locked, ωout = ωin, Vcont = (ωin – ω0)/KVCO.

□ VLPF = (ωin – ω0)/KVCO – V1, Δϕ = VLPF/KPD = (ωin – ω0)/(KPDKVCO) – V1/KPD.

•(b)

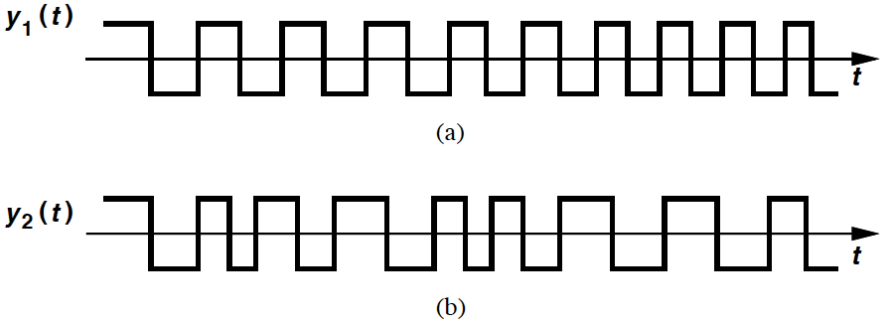
- When Vex steps from V1 to V2, Vcont immediately goes from (ωin – ω0)/KVCO to (ωin – ω0)/KVCO + (V2 – V1) □ change the VCO frequency to ωin – KVCO(V1 – V2).

- VLPF cannot change instantaneously □ PD begins to generate increasingly wider pulses, increasing VLPF & ωout.

- When the loop returns to lock, ωout = ωin, VLPF = (ωin – ω0)/KVCO – V2. Phase error also changes to (ωin – ω0)/(KPDKVCO) – V2/KPD.

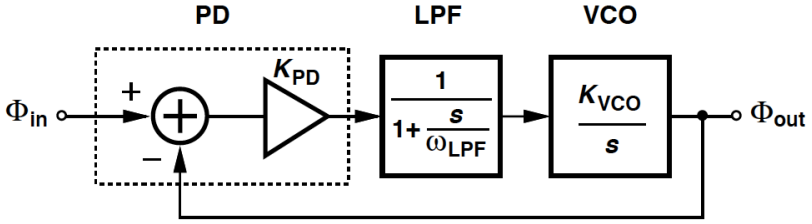
Change in the phase error: $$\int_{t1}^{\infty} \omega_{out}\, dt = \frac{V_1 - V_2}{K_{PD}}.$$

Variation of the Excess Phase with Time



- **Assume the loop is initially locked and treat the PLL as a feedback system output quantity is the (excess) phase of the VCO.**
- **ϕout(s)/ϕin(s): How the output phase tracks the input phase if the latter changes slowly or rapidly.**
- **y2(t) has faster phase variations than does y1(t).**

Linear Model of Type I PLL (I)



- **The overall PLL model consists of: Phase subtractor + LPF + VCO.**
- **In LPF transfer function, ωLPF is -3-dB bandwidth.**
- **ϕin and ϕout: Excess phases of the input and output waveforms, respectively.**
- **Open-loop transfer function:**

$$H(s)|_{\text{open}} = \frac{\Phi_{out}}{\Phi_{in}}(s)|_{\text{open}} = K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$

- **Two poles: s = -ωLPF, s = 0. (… at the origin → “type I” system).**

Linear Model of Type I PLL (II)

- **Close-loop transfer function:** $$H(s)|_{\text{closed}} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$$

- **If s -> 0, H(s) -> 1 because of the infinite loop gain. (Simply denote H(s)|closed by H(s).)**
- **H(s) also applies to:**

$$\frac{\omega_{out}}{\omega_{in}}(s) = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$$

  - If ωin changes very slowly (s -> 0) □ ωout tracks ωin.

  - If ωin changes abruptly but the system is given enough time to settle (s -> 0) □ change in ωout equals that in ωin.
- **We also have:**

$$H(s) = K_{VCO} \cdot \frac{V_{cont}}{\omega_{in}}(s)$$

Linear Model of Type I PLL (III)

- **Rewrite H(s) as:** $H(s) = \dfrac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$

  - where "natural frequency": $\omega_n = \sqrt{\omega_{LPF} K_{PD} K_{VCO}}$

  $$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD} K_{VCO}}}.$$

  - Two poles: $s_{1,2} = -\zeta\omega_n \pm \sqrt{(\zeta^2 - 1)\omega_n^2}$

  $= (-\zeta \pm \sqrt{\zeta^2 - 1})\omega_n.$

- **If ζ > 1, real po… …ystem is overdam…ped.**
- **If ζ < 1, complex poles → response to ωin = Δωu(t) is:**

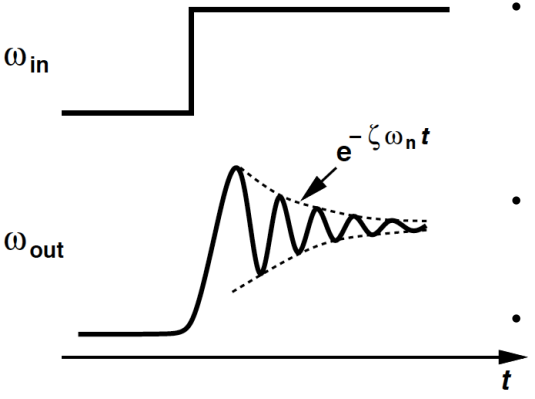
$$\omega_{out}(t) = \left\{1 - e^{-\zeta\omega_n t}[\cos(\omega_n\sqrt{1-\zeta^2}t) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin(\omega_n\sqrt{1-\zeta^2}t)]\right\}\Delta\omega u(t) \quad (16.2$$

$$= [1 - \frac{1}{\sqrt{1-\zeta^2}}e^{-\zeta\omega_n t}\sin(\omega_n\sqrt{1-\zeta^2}t + \theta)]\Delta\omega u(t), \quad (16.2$$

- where

$$\theta = \sin^{-1}\sqrt{1-\zeta^2}$$

Underdamped Step Response of PLL



- The step response contains a sinusoidal component with frequency $\omega_n\sqrt{1-\zeta^2}$ that decays with time constant $(\zeta\omega_n)^{-1}$.
- To maximize settling speed of PLLS □ $\zeta\omega_n$ is maximized.
- Trade-off between the settling speed and the ripple on the VCO control line.

Example 16.5

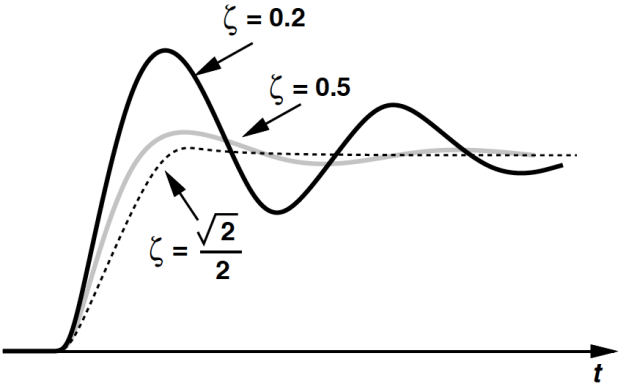
Consider a 900-MHz PLL. ωLPF = 2π × (20 kHz). Output frequency changes from 901 MHz to 901.2 MHz. How long does it take to settle within 100 Hz of its final value?

Solution

- **Step size = 200 kHz**
  - $[1 - e^{-\zeta\omega_n t_s}\sin(\omega_n\sqrt{1-\zeta^2}t_s + \theta)] \times 200\text{ kHz} = 200\text{ kHz} - 100\text{ Hz}.$
  - $e^{-\zeta\omega_n t_s}\sin(\omega_n\sqrt{1-\zeta^2}t_s + \theta) = \dfrac{100\text{ Hz}}{200\text{ kHz}}.$
- **In the worse case, the sinusoid is unity and** $e^{-\zeta\omega_n t_s} = 0.0005.$
- **That is,**

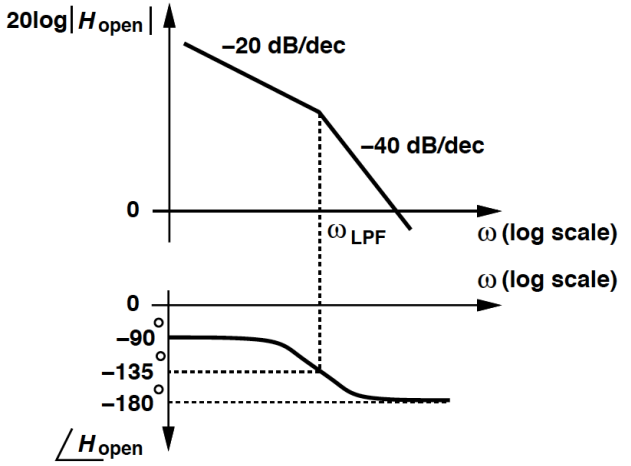
$$\begin{aligned} t_s &= \frac{7.6}{\zeta\omega_n} \\ &= \frac{15.2}{\omega_{LPF}} \\ &= 0.12\text{ ms}. \end{aligned}$$

Underdamped Step Response for Various ζ



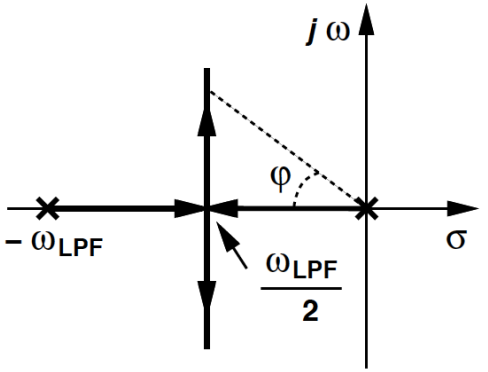
- **Severe ringing for ζ < 0.5.**
- **Trade-offs assciated with choice of ζ:**
  - Reduce ωLPF to minimize ripple on Vcont stability degrades.
  - Lower phase error system less stable.
  (Phase error and ζ inversely proportional to KPDKVCO.)

Bode Plots of Type I PLL



- **A higher KPDKVCO to minimize ϕout – ϕin gain plot shifted up & gain crossover to the right phase margin degrades.**
- **The above is consistent with dependence of ζ upon KPDKVCO.**

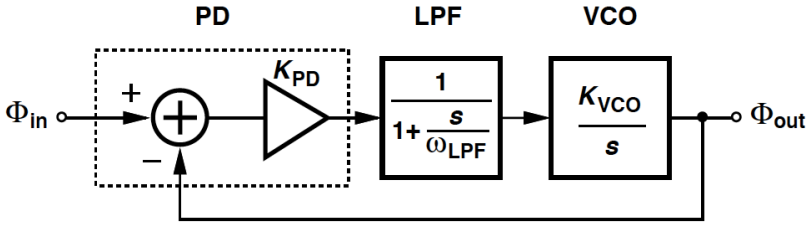
Root Locus of Type I PLL



- KPDKVCO = 0 □ loop is open, ζ = ∞, and s1 = -ωLPF, s2 = 0.
- KPDKVCO increases □ ζ drops and the two poles move toward each other on the real axis.

  - For ζ = 1 (i.e., KPDKVCO = ωLPF/4), s1 = s2 = -ζωn = -ωLPF/2.
- KPDKVCO increases further □ two poles become complex with real part equal to -ζωn = -ωLPF/2, , moving in parallel with jω axis.
- s1 and s2 moves away from the real axis □ system less stable.

PLL Transfer Function of Phase Error



- **Another transfer function involves the error at the output of the phase subtractor:**

$$H_e(s) = (\phi_{in} - \phi_{out})/\phi_{in}$$

- **He(s) can be obtained by** $\phi_{out}/\phi_{in} = H(s)$ **and from**

$$\begin{aligned} H_e(s) &= 1 - H(s) \\ &= \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n}. \end{aligned}$$

- **As expected, He(s) -> 0 if s -> 0.**

Example 16.6

A type-I PLL experiences a frequency step Δω at t = 0. Calculate the change in the phase error.

Solution

•The Laplace transform of the frequency step = Δω/s.

•

$$\Phi_{in}(s) = (\Delta\omega/s)/s = \Delta\omega/s^2$$

$$\Phi_e(s) = H_e(s) \cdot \frac{\Delta\omega}{s^2}$$

$$= \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \cdot \frac{\Delta\omega}{s^2}$$

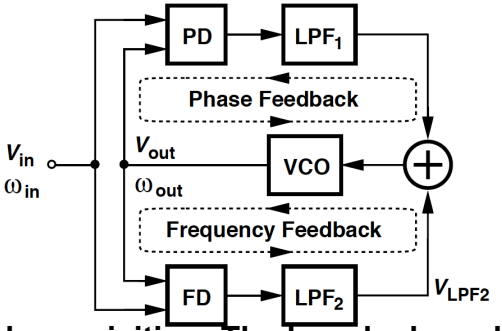
Fr

$$\phi_e(t = \infty) = \lim_{s \to 0} s\Phi_e(s)$$

$$= \frac{2\zeta}{\omega_n}\Delta\omega$$

$$= \frac{\Delta\omega}{K_{PD}K_{VCO}}$$

Aided Acquisition



Problem of lock acquisition: The loop locks only if the difference between ωin and ωout is less than ~ ωLPF.

Aided acquisition:

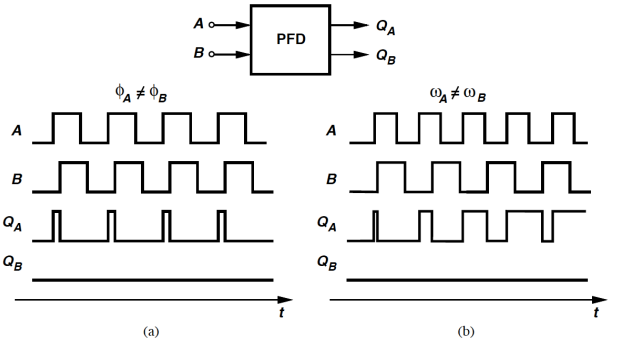
- Compare ωin and ωout by frequency detector.

- Generate a dc component VLPF2 proportional to ωin – ωout □ applied to VCO in a negative-feedback loop.

- Initially, FD drives ωout toward ωin, & PD output remains "quiet".

- As |ωout – ωin| sufficiently small □ PLL takes over □ Lock!

Phase/Frequency Detector (PFD)



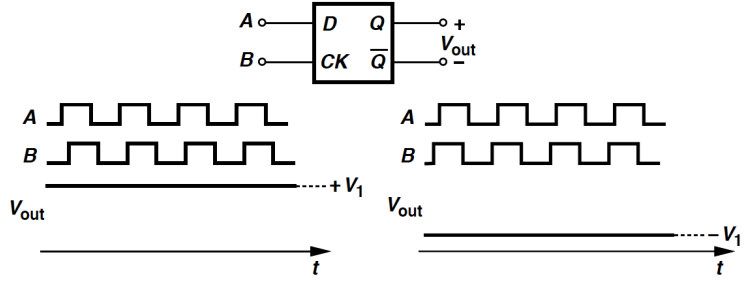
- If a rising edge on A followed by a rising edge on B QA goes high and returns to low, QB = 0. (Similar behavior for input B.)
- In (a), A leads B with equal frequencies QA continues to produce pulses with width proportional to ϕA – ϕB, QB = 0.
- In (b), A has a higher frequency & QA generates pulses, QB = 0.
- If A lags B or has a lower frequency than B QB produces pulses, QA = 0.
- QA: “UP” pulse, QB: “DOWN” pulse.

Example 16.7 (I)

Explain whether a master-slave D flipflop can operate as a phase detector or a frequency detector.

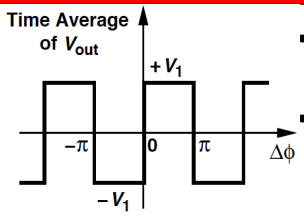
Solution

- **In (a), first apply inputs with equal equal frequencies & finite phase difference.**
- **If A leads B Vout remains high indefinitely because flipflop continues to sample high levels of A.**
- **If A lags B Vout remains low.**

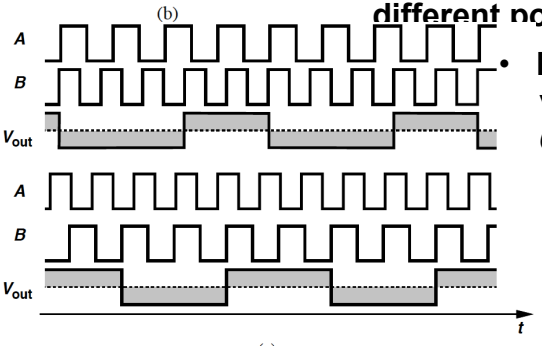


(a)

Example 16.7 (II)

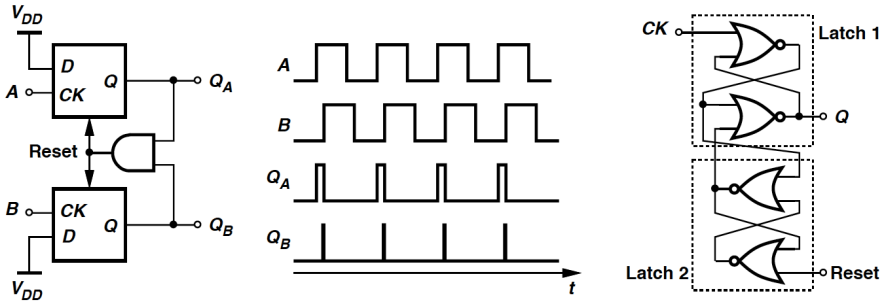


- (b): High gain at $\Delta\phi = 0, \pm\pi, \ldots$, zero gain at other $\Delta\phi$.
- D flipflop is called a "bang-bang" phase detector: The avergae value of Vout jumps from –V1 to +V1 as $\Delta\phi$ varies from 0- to 0+.
- If the flipflop is to behave as a frequency detector, then average value of Vout has different polarities for $\omega A > \omega B$ & $\omega A <$



- However, in (c), the average value of Vout is zero for both $\omega A > \omega B$ & $\omega A < \omega B$.

Implementation of PFD



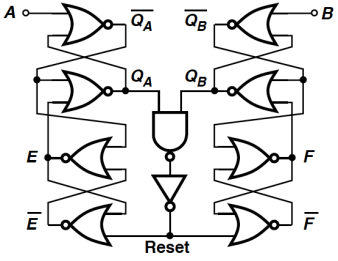
- **Simple implementation of PFD in (a): D inputs of two flipflops tied to logical ONE, A & B as clocks of the flipflops.**
- **If QA = QB = 0 & A goes high QA rises. Then if followed by rising on B QB goes high and the AND gate resets both flipflops.**
- **Each flipflop can be implemented as (b): Cross-coupled Latch 1 & Latch 2 respond to rising edges of CK and Reset, respectively.**

Example 16.8

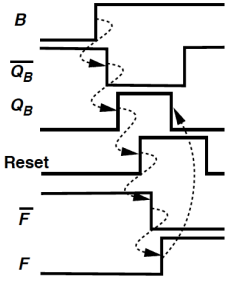
Determine the width of the narrow reset pulse that appear in the QB waveform in figure (a) (Slide 35).

Solution

- **(a) shown below illustrates the overall PFD at the gate level.**
- **If it begins with A = 1, QA = 1, and QB = 0, a rising edge on B forces $\overline{Q_B}$ to go low and, one gate delay later, QB to go high.**
- **In (b), this transition propagates to Reset, $\overline{E}$ and $\overline{F}$ E & F, and finally to QA and QB.**



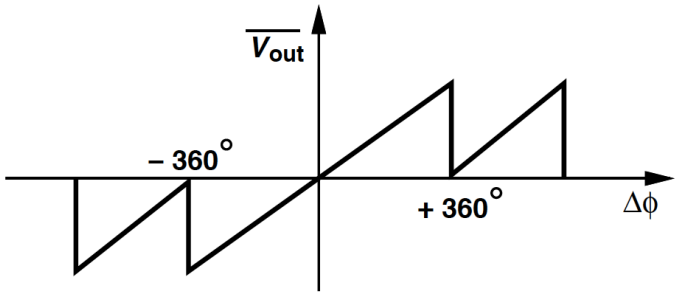
(a)



(b)

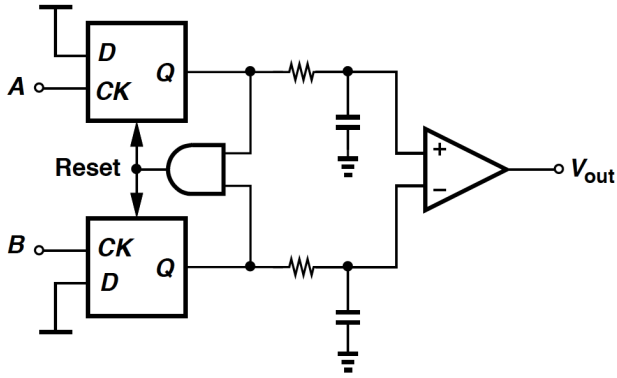
- **The width of the pulse on QB ≈ 5 gate delays.**

Input-output Characteristic of 3-state PFD



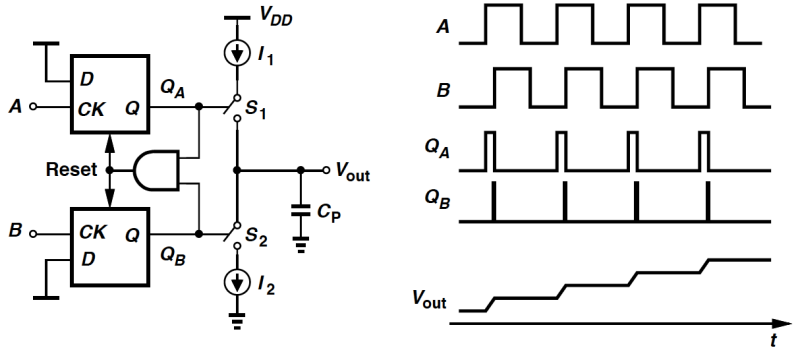
- Define output as the difference between average values of QA and QB when ωA = ωB.
- The output varies symmetrically as |Δϕ| begins from zero.
- For Δϕ = ±360°, Vout reaches extrema and subsequently changes sign.
- Slope of this characteristic = gain.

PFD Followed by Low-Pass Filters



- The difference between average values of QA and QB is of interest Two outputs low-pass filtered and sensed differently.
- A PLL with such topology always locks.
- Suffers from a finite phase error due to finite KPFDVVCO.

PFD with Charge Pump



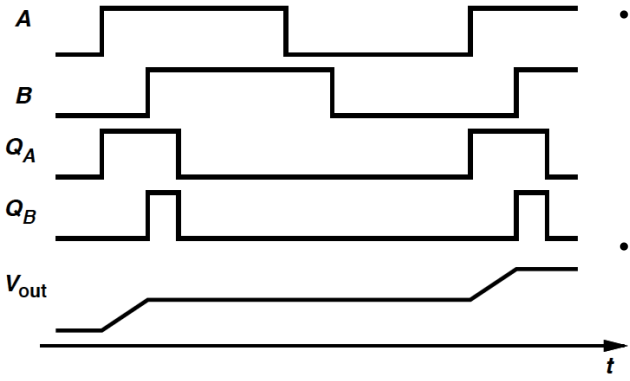
- To raise the loop gain to infinity, we first interpose a "charge pump" (CP) between PFD and loop filter.
- QA = QB = 0 □ S1 & S2 off, Vout remains constant.
- QA = 1, QB = 0 □ I1 charges CP.
- QA = 0, QB = 1 □ I2 discharges CP.
- E.g., A leads B □ QA continues to produce pulses, Vout rises steadily.

Example 16.9

What is the effect of the narrow pulses that appear in the QB waveform (Slide 39)?

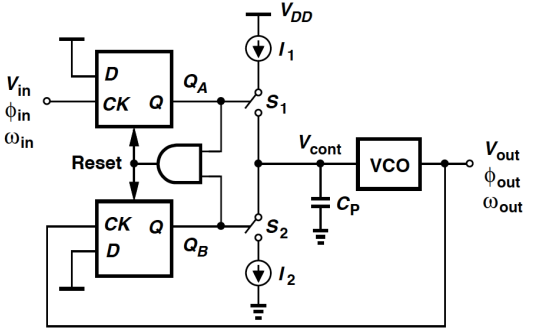
Solution

•QA and QB are simultaneously high for a finite period (Example 16.8) □ the current supplied by the charge pump to CP is affected.



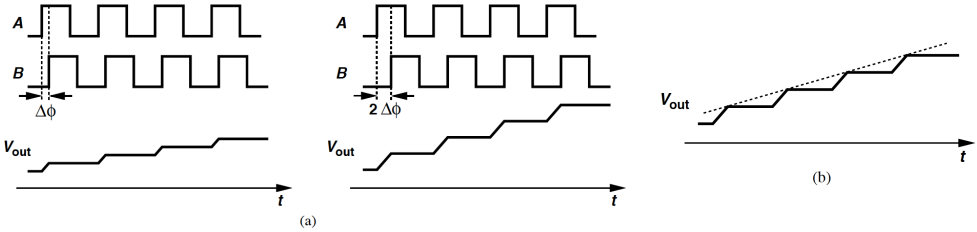
- **If I1 = I2, current through S1 simply flows through S2 during the narrow reset pulse □ no current to charge CP.**
- **Vout remains constant after QB goes high.**

Basic Charge-Pump PLL



- **Charge-pump PLL:**
  - **Senses transitions at input and output.**
  - **Detects phase/frequency differences.**
  - **Activates the charge pump accordingly.**
- **As ωout approaches ωin and when close enough □ PFD operates as phase detector, performing phase lock.**
- **When the loop is locked, Vcont is finite. □ Input phase error must be exactly zero (in contrast to type-I PLL).**

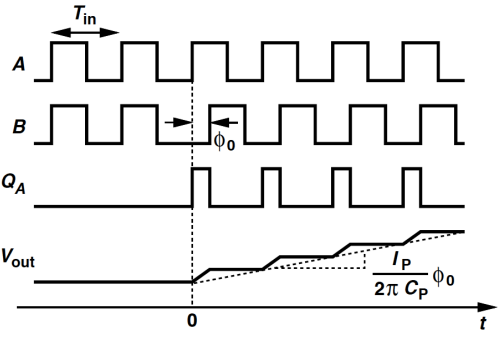
Dynamics of CPPLL



- To test linearity of PFD/CP/LPF combination: Double input phase difference and see if Vout exactly doubles.
- The flat sections of Vout double but not the ramp sections.
- The current charging/discharging CP is constant □ constant slope for the ramp.
- Not linear in the strict sense.
- Approximate the output waveform by a ramp in (b) □ linear relationship between Vout and $\Delta\varphi$.

Step Response of PFD/CP/LPF Combination

- Assume input period = TD & charge pump provides ±IP to the capacitor.
- Begin with zero phase difference, Δϕ = ϕ0u(t) □ QA or QB continues to produce pulses of ϕ0Tin/(2π) seconds wide.
- Approximated by a ramp □



$$V_{out}(t) = \frac{I_P}{2\pi C_P} t \cdot \phi_0 u(t)$$

- The impulse response:

$$h(t) = \frac{I_P}{2\pi C_P} u(t)$$

□ Transfer function:

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_P}{2\pi C_P} \cdot \frac{1}{s}$$

Example 16.10

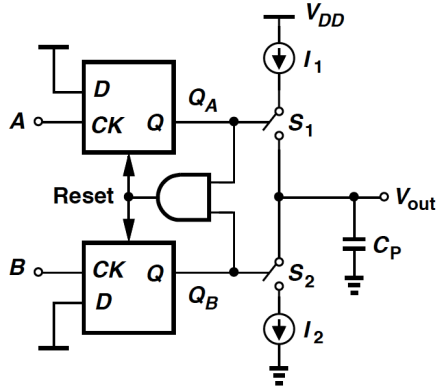
Suppose the output quantity of interest in the circuit below is the current injected by the charge pump into the capacitor. Determine the transfer function from Δϕ to this current, Iout.

Solution

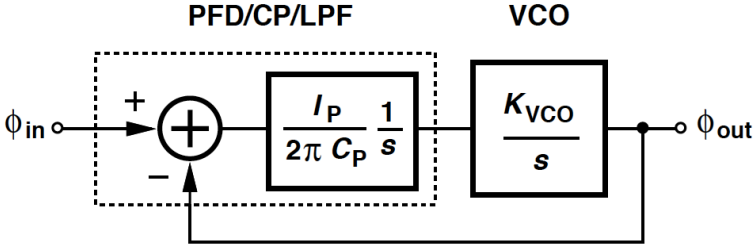
•Vout(s) = Iout/(CPs)

□

$$\frac{I_{out}}{\Delta\phi}(s) = \frac{I_P}{2\pi}.$$



Linear Model of Charge-pump PLL (I)



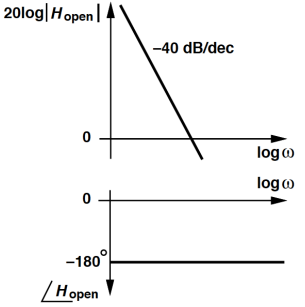
- **The linear model of charge-pump PLLs has an open-loop transfer function:** $\frac{\Phi_{out}}{\Phi_{in}}(s)|_{\text{open}} = \frac{I_P}{2\pi C_P}\frac{K_{VCO}}{s^2}$
- **Loop gain has two poles at the origin □ "type II" PLL.**
- **Close-loop transfer function:**

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}}{s^2 + \frac{I_P K_{VCO}}{2\pi C_P}}$$

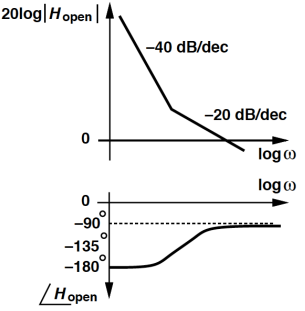
Linear Model of Charge-pump PLL (II)

- H(s) contains two imaginary poles at: $s1,2 = \pm j\sqrt{I_P K_{VCO}/(2\pi C_P)}$
  □ unstable system.
- In (a): constant total phase shift of 180° □ system oscillates at gain crossover frequency.

- To stabilize the system, phase shift < 180° at the gain crossover.
- (b): Accomplished by introducing a zero in loop gain, i.e., by adding a resistor in series with capacitor CP.

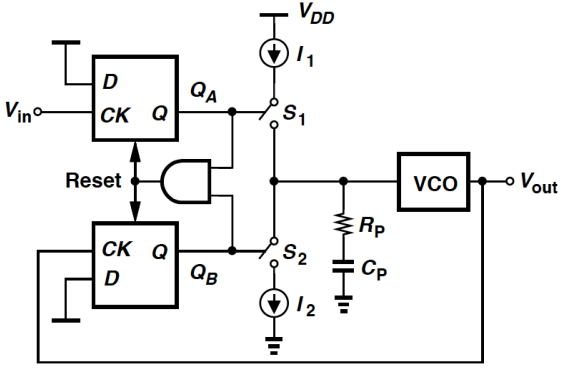


(a)



(b)

Linear Model of Charge-pump PLL (III)



- **In this circuit, transfer function of PFD/CP/LPF now becomes:**

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_P}{2\pi}(R_P + \frac{1}{C_P s})$$

and

$$\frac{\Phi_{out}}{\Phi_{in}}(s)|_{\text{open}} = \frac{I_P}{2\pi}(R_P + \frac{1}{C_P s})\frac{K_{VCO}}{s}$$

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi}K_{VCO}R_P s + \frac{I_P}{2\pi C_P}K_{VCO}}$$

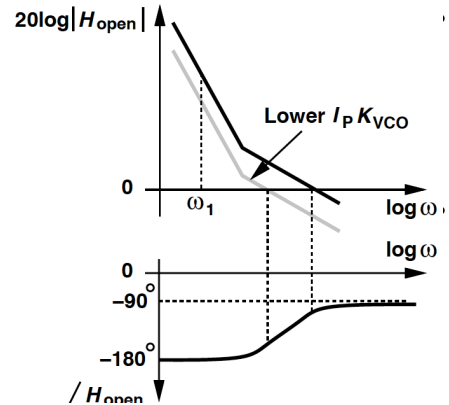
- **Close-loop system contains a zero at sz = -1/(RPCP).**

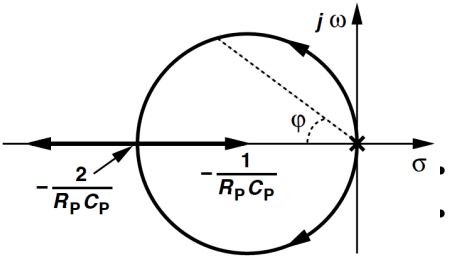
- **Using the same notation as before, we have:**

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P}}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi}}$$

Charge-pump PLL: Stability Issues





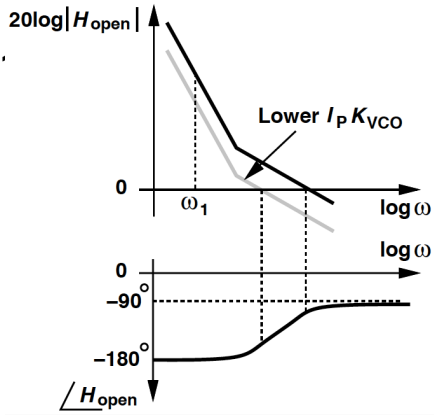
- In Bode plots of the loop gain: IPKVCO decreases □ gain crossover frequency moves toward the origin □ phase margin degrades.
- In root locus of the close-loop system in complex plane:
  - IPKVCO = 0 □ loop open, both poles at the origin
  - IPKVCO > 0 □ $s_{1,2} = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$
  - Complex poles if IPKVCO is small.
  - IPKVCO increases □ s1. s2 move on a circle centered $\sigma = -1/(R_P C_P)$ & radius = $1/(R_P C_P)$
- For ζ ≥ 1, poles are real.
- For complex s1, s2, ζ = cosψ: IPKVCO exceeds zero □ more stable.

Example 16.11

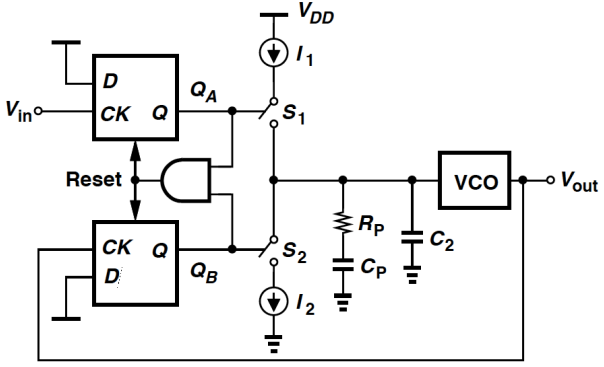
Explain the flaw: A student considers the Bode plots and observes that at ω1, the loop gain > 1 & phase shift = -180°. Then the PLL must oscillate at this frequency.

Solution

- **The phase shift is in fact slightly less than zero unless ω = 0.**
- **Using Nyquist's approach (Chapter 10), a system containing two integrators and one zero does not oscilate.**

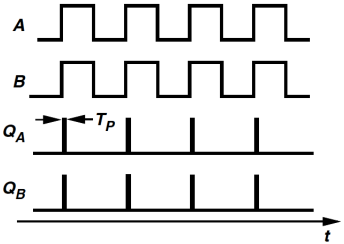


Charge-pump PLL: Addition of C2



- For the compensated type-II PLL: Vcont experiences large jump □ disturb VCO.
- A second capacitor added in parallel with RP and CP □ suppress the initial step.
- Third-order PLL. If C2 is about 1/5 to 1/10 of CP □ close-loop time and frequency responses remain relatively unchanged.
- In reality, RP becomes very large □ stability degrades again.

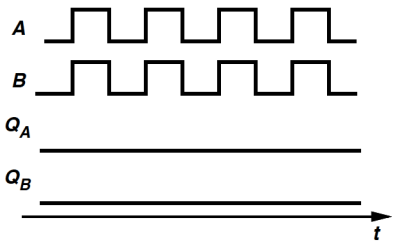
PFD/CP Nonidealities

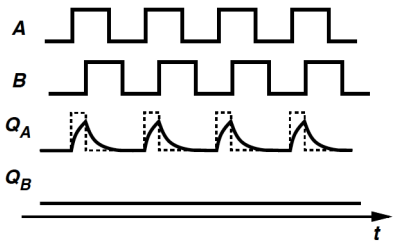


If A & B rise simultaneously, so do QA & QB □ activate reset.

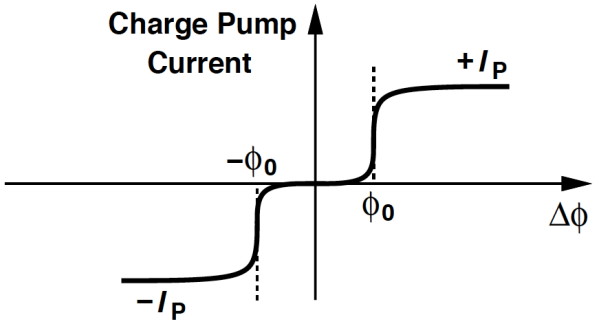
(a): A hypothetical PFD that produces no pulses for a zero input phase difference.

(b): The circuit generates very narrow pulses on QA or QB.



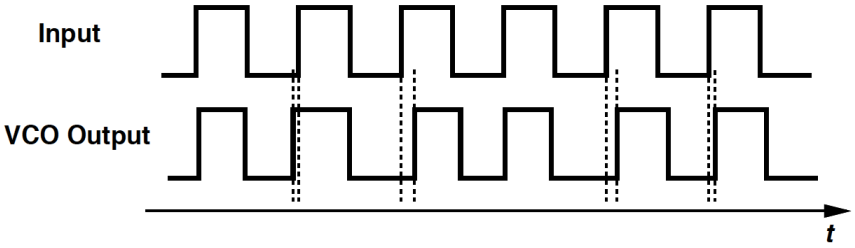


Dead Zone in Charge Pump Current



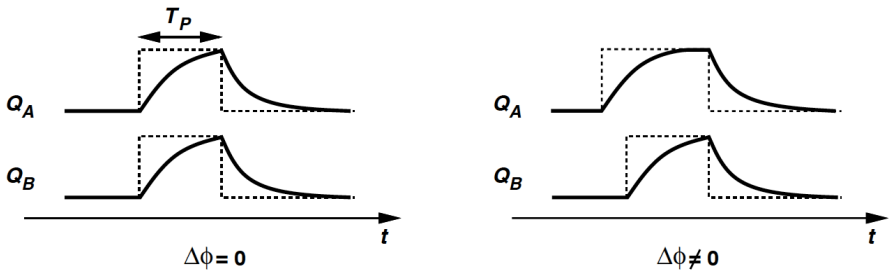
- If $\Delta\phi$ falls below $\phi 0$ □ output volatage of PFD/CP/LPF combination is no longer a function of $\Delta\phi$.
- For $|\Delta\phi| < \phi 0$, charge pump injects no current □ loop gain drops to zero and output phase is not locked.
- Thus PFD/CP circuit suffers from a dead zone equal to $\pm\phi 0$ around $\Delta\phi = 0$.

Jitter from Dead Zone



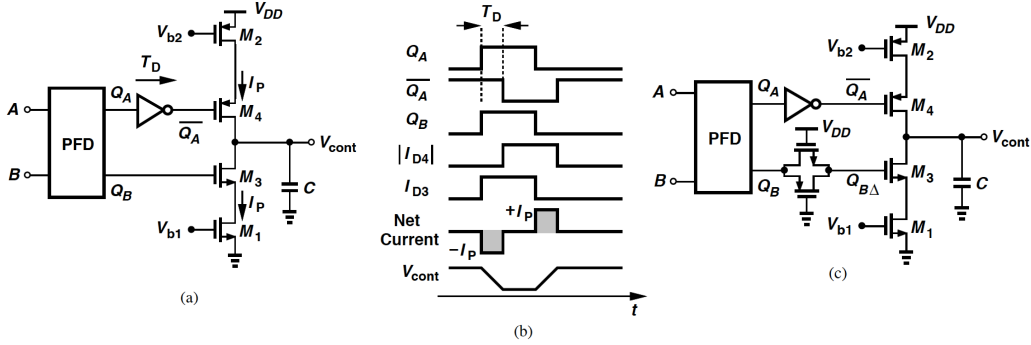
- Dead zone allows VCO to accumulate as much random phase error as $\varphi 0$ with respect to input while receiving no corrective feedback.
- The zero crossing points of the VCO output experience substantial random variations □ "jitter."

Response of Actual PD to a small $\Delta\varphi$



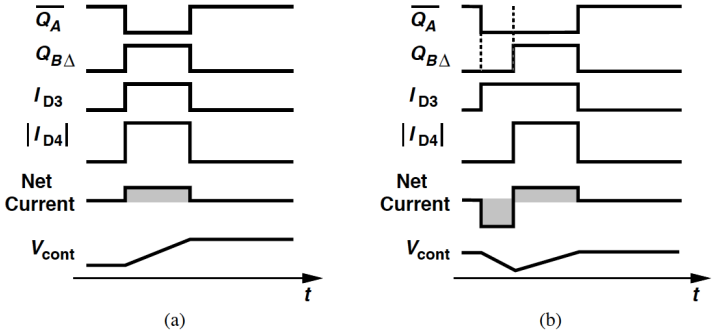
- **The coincident pulses on QA and QB can eliminate dead zone.**
- **An infinitesimal increment in Δϕ proportional increase in net current produced by the charge pump.**

Effect of Skew



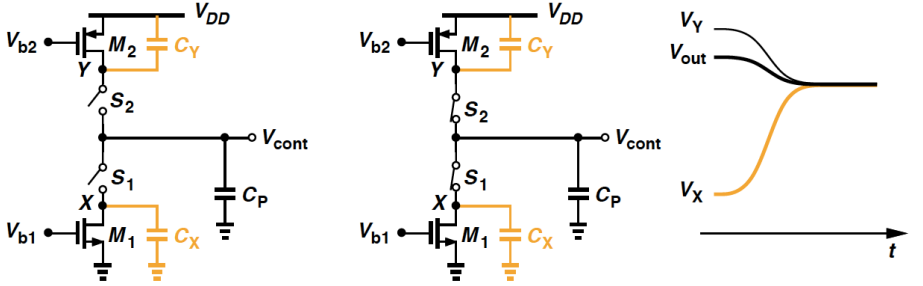
- **(a): M1 & M2 as Current sources, M3 & M4 as Switches. Output QA is inverted. QA goes high M4 turns on.**
- **Issue of (a): As in (b), net current injected by the charge pump into loop filter jumps to +IP & -IP disturb Vcont periodically.**
- **(c) can equalize the delays and suppress the above effect.**

Effect of UP & DOWN Current Mismatch



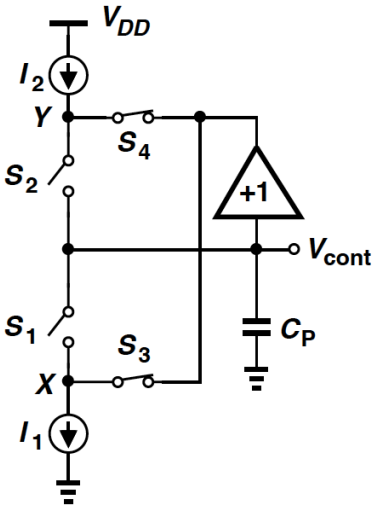
- **(a): Even with perfect alignment of UP & DOWN pulses, net current ≠ 0 □ charge Vcont by a constant increment at each phase comparison instant.**
- **For the loop to remain locked, average value of Vcont must remain constant □ (b): PLL creates a phase error between input & output such that net current in every cycle = 0.**

Charge Sharing between CP, CX & CY



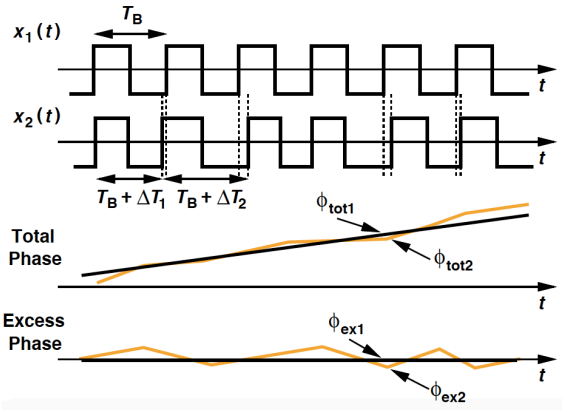
- **Suppose in (a), S1 & S2 off □ M1 discharge X to ground, M2 charge Y to VDD.**
- **(b): Next phase comparison instant, both S1 & S2 on □ VX rises, VY falls, VX ≈ VY ≈ Vcont.**
- **Even if CX = CY, change in VX is not equal to that in VY □ difference between the two changes must be supplied by CP □ a jump in Vcont.**

Bootstrapping



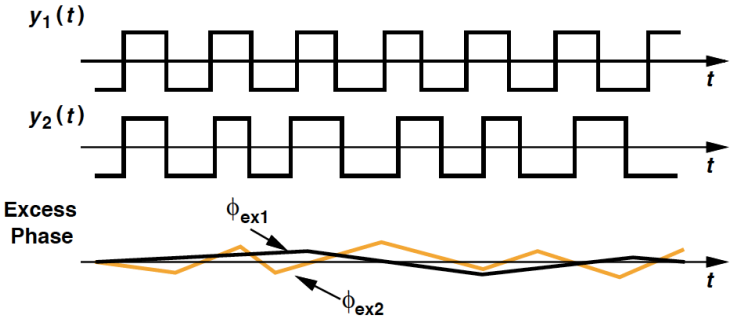
- Charge sharing can be suppressed by "bootstrapping."
- When S1 & S2 off, S3 & S4 on □ allow unity-gain amplifier to hold VX & VY at Vcont.
- Next phase comparison instant, S1 & S2 on, S3 & S4 off □ VX & VY begin with Vcont □ no charge sharing between CP and capacitances at X & Y.

Ideal vs. Jittery Waveforms



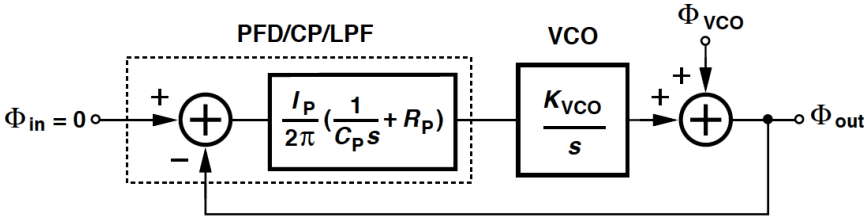
- **Strictly periodic x1(t) contains zero crossings evenly spaced in time.**
- **Nearly periodic x2(t) displaces zero crossings from ideal points.**
- **We say x2(t) suffers from jitter.**
- **From plots of ϕout and ϕex, jitter manifests itself as variation of ϕex with time.**

Slow vs. Fast Jitter



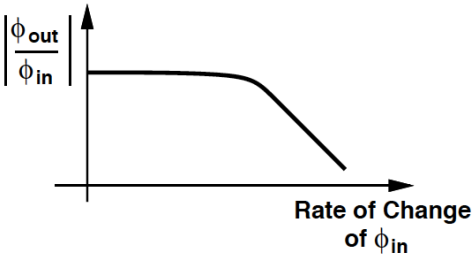
- y1(t): instantaneous frequency varies slowly from one period to the next □ "slow jitter."
- y2(t): "fast jitter."
- Rate of change is also evident from ϕex plots of the two waveforms.
- Slow jitter at input propagates to output unattenuated but fast jitter does not.

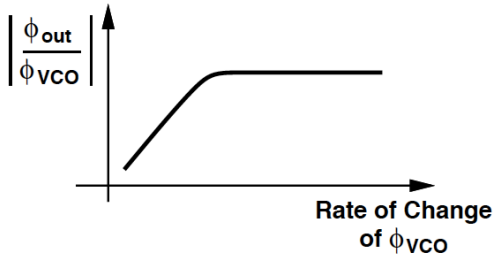
Effect of VCO Jitter



- **Suppose input is strictly periodic but VCO suffers from jitter.**
- **In this model, xin(t) = A cosωt, a random component ΦVCO is added to the output of VCO to represent its jitter.**
  - **For type-II PLL:** $\frac{\Phi_{out}}{\Phi_{VCO}}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$
- **The characteristic has a high-pass nature slow jitter components generated by VCO are suppressed but fast jitter components are not.**

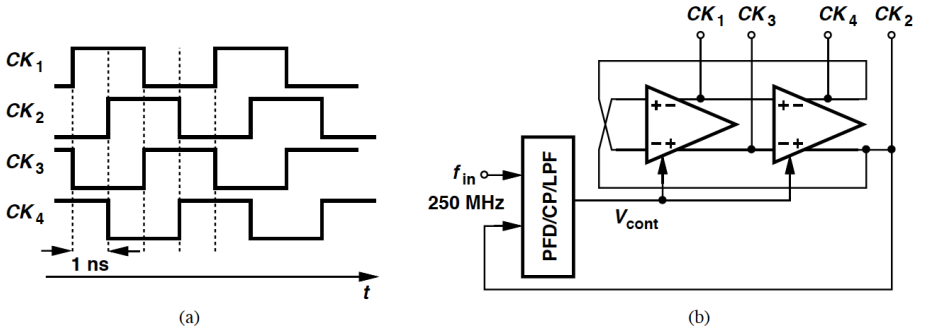
Response of PLL to Input Jitter & VCO Jitter





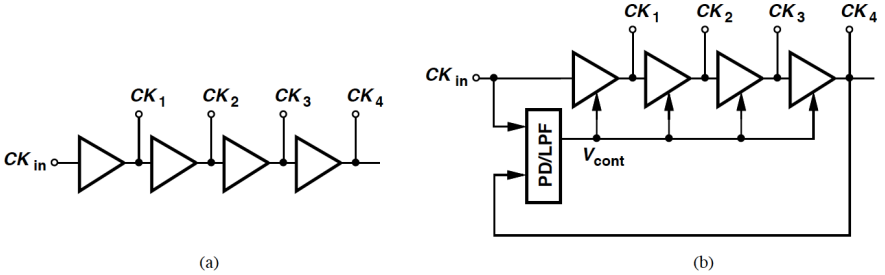
- **Depending on the application and the application, one or both sources (input jitter & VCO jitter) may be significant, requiring an optimum choice of the loop bandwidth.**

Generation of Clock Edges



- **(a): Four clock phases with ΔT = 1 ns between consecutive edges.**
- **(b): To generate phases in (a), use a two-stage differential ring oscillator, locked to a 250-MHz reference output period is exactly 4 ns.**

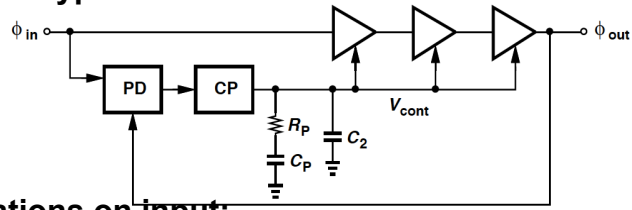
Simple Delay-Locked Loop (DLL)



- **(a) also generates the clock phases (Slide 63): Apply input clock to four delay stages in a cascade.**
  - **Does not produce a well-defined edge spacing.**
- **(b): Simple delay-locked loop (incorporates VCDL not a VCO)**
  - **Phase difference between Ckin and CK4 sensed by a PD.**
  - **A proportional average voltage, Vcont, generated.**
  - **Delay adjusted with negative feedback.**
  - **Large loop gain □ small phase difference between Ckin & CK4 □ establish precise edge spacing.**

Example 16.12

Explain qualitatively what type of transfer function the DLL shown below has.



Solution

- **For slow phase fluctuations on input:**
  - **Phase error sees a high gain through PD/CP/LPF.**
  - **Delay of the line is adjusted so as to minimize this error.**

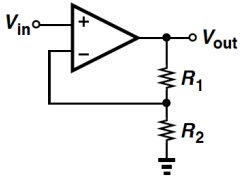
  □ φout tracks φin, gain is about unity.

- **For very fast phase changes on input:**
  - **Feedback loop has little gain, Vcont relatively constant.**
  - **Input phase variations directly propagates to output**

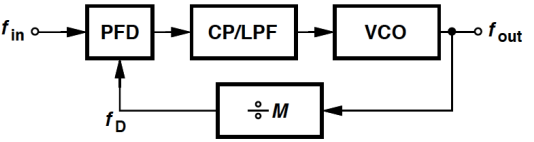
  □ gain of about unity.

- **The DLL exhibits all-pass response, but the response may have a dip or a peak for moderately fast phase changes.**

Frequency Multiplication



(a)



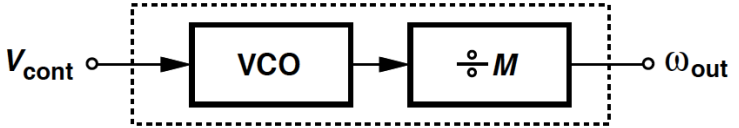
(b)

- (a) Voltage amplification: A feedback system amplifies Vin by a factor M if R2/(R1 + R2) = 1/M, and compare the result with Vin.
- (b) Frequency multiplication: fout of a PLL divided by M and applied to the phase detector □ fout = Mfin.
- Rewrite the equation on Slide 50 as:

$$H(s) = \frac{\frac{I_P}{2\pi}(R_P + \frac{1}{C_P s})\frac{K_{VCO}}{s}}{1 + \frac{1}{M}\frac{I_P}{2\pi}(R_P + \frac{1}{C_P s})\frac{K_{VCO}}{s}} = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi}\frac{K_{VCO}}{M}R_P s + \frac{I_P}{2\pi C_P}\frac{K_{VCO}}{M}}$$

- Compare the denominators of two equations of H(s) □ frequency division in the loop manifests itself as division of KVCO by M.

VCO/Divider combination



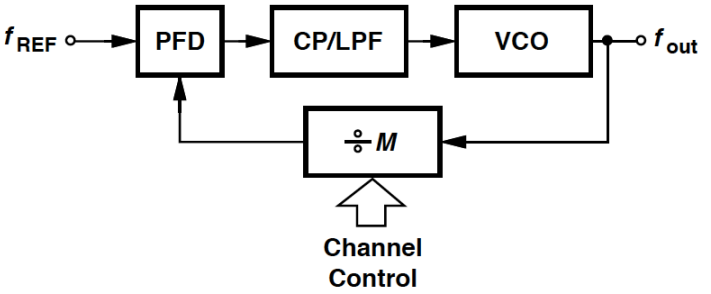
- **For the VCO/divider cascade, we have:** $\omega_{out} = \frac{\omega_0 + K_{VCO}V_{cont}}{M} = \frac{\omega_0}{M} + \frac{K_{VCO}}{M}V_{cont}$
- **This combination is equivalent to a VCO with an intercept frequency = ω0/M and gain = KVCO/M.**
- **Then we can rewrite:**

$$\omega_n = \sqrt{\frac{I_P}{2\pi C_P}\frac{K_{VCO}}{M}}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P}{2\pi}\frac{K_{VCO}}{M}}.$$

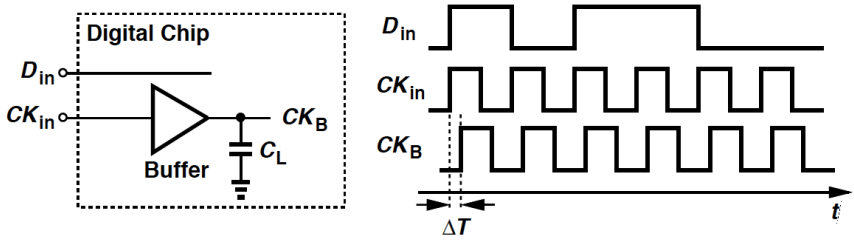
- **Decay time constant is** $(\zeta\omega_n)^{-1} = 4\pi M/(R_P I_P K_{VCO})$
  - **Inserting a divider in a type-II loop [illegible] and settling speed.**

Phase-Locked Frequency Synthesizer



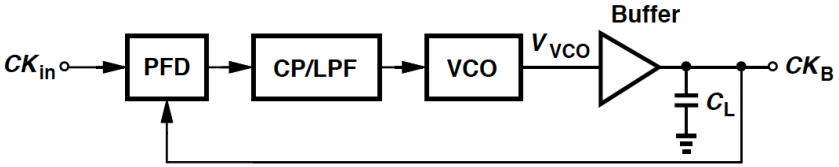
- **Channel control input: A digital word that defines value of M.**
- **fout = MfREF, the relative accuracy of fout is equal to that of fREF.**
  - **fREF derived from a stable, low-noise oscillator.**

Skew between Data and Buffered Clock



- A synchronous pair of data and clock lines enter a large digital chip.
- The clock typically drives a large number of transistors and long interconnects be the first applied to a large buffer.
- The clock distributed on the chip may suffer from substantial skew, ΔT, with respect to the data.

Use of PLL to Eliminate Skew



- An CKin is applied to an on-chip PLL and the buffer is placed inside the loop.
- The PLL guarantees a nominally-zero phase difference between Ckin and CKB □ skew is eliminated.
- Constant phase shift introduced by buffer is divided by infinite loop gain of the feedback system.

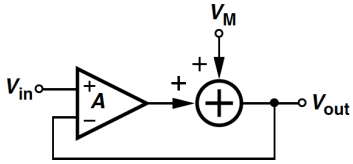
Example 16.13

Construct the voltage-domain counterpart of the loop (Slide 70).

Solution

•The buffer creates a constant phase shift in the signal generated by VCO.

□ voltage-domain counterpart assumes the below topology:

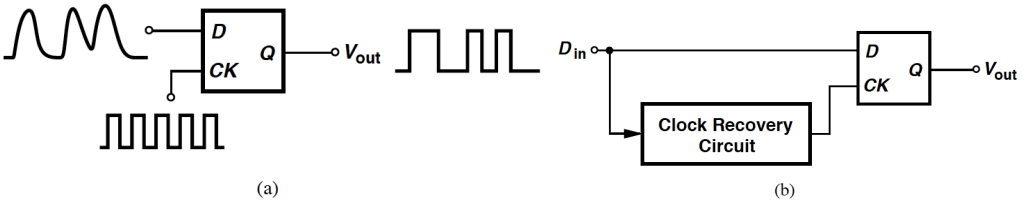


•We have:

$$(V_{in} - V_{out})A + V_M = V_{out} \quad \square \quad V_{out} = \frac{AV_{in} + V_M}{1 + A}.$$

•As A -> ∞, Vout -> Vin.

Jitter Reduction



- **Jittery waveforms: Typically "retimed" by a low-noise clock.**
- **(a): Resample the midpoint of each bit by a D flipflop driven by the clock.**
  - However the clock may not be available independently.
- **Modified as (b): A "clock recovery circuit" (CRC) produces clock from the data.**
  ⇨ minimize effect of input jitter on the recovered clock.