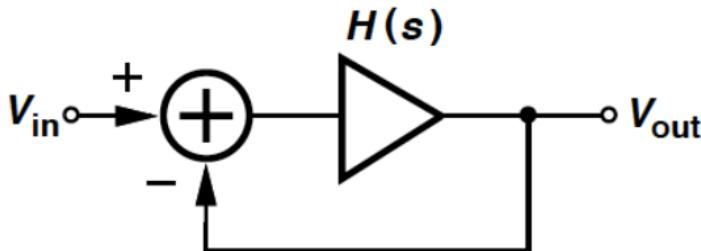


Chapter 15: Oscillators

- 15.1 General Considerations**
- 15.2 Ring Oscillators**
- 15.3 LC Oscillators**
- 15.4 Voltage-Controlled Oscillators**
- 15.5 Mathematical Model of VCOs**

Oscillatory Feedback System

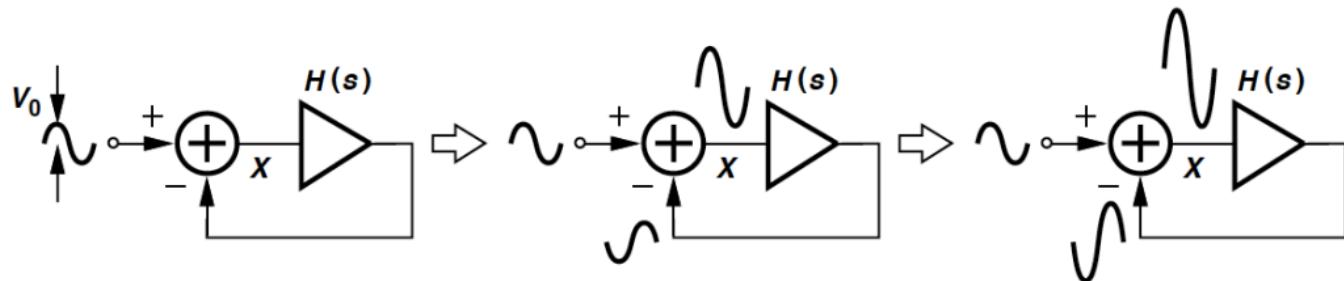
- Consider a unity-gain negative feedback circuit:



$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 + H(s)}.$$

- Recall: Negative feedback systems may oscillate.
- If for $s = j\omega_0$, $H(j\omega_0) = -1$
 - close-loop gain $\rightarrow \infty$ at ω_0
 - its own noise components amplified at ω_0 indefinitely.

Evolution of Oscillatory System with Time



- A noise component at $j\omega_0$
 - experiences unity gain & a phase shift = 180° .
 - returns as a negative replica of the input.
 - a larger difference obtained -> continues to grow.
- Over many cycles,

$$V_X = V_0 + |H(j\omega_0)|V_0 + |H(j\omega_0)|^2V_0 + |H(j\omega_0)|^3V_0 + \dots$$

- If $|H(j\omega_0)| < 1$,

$$V_X = \frac{V_0}{1 - |H(j\omega_0)|} < \infty.$$

Barkhausen Criteria

- A negative-feedback circuit may oscillate at ω_0 if it satisfies:

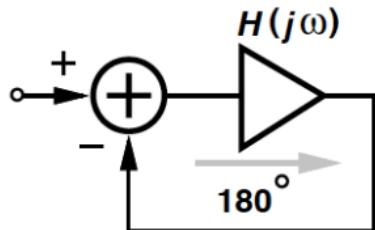
$$|H(j\omega_0)| \geq 1$$

$$\angle H(j\omega_0) = 180^\circ$$

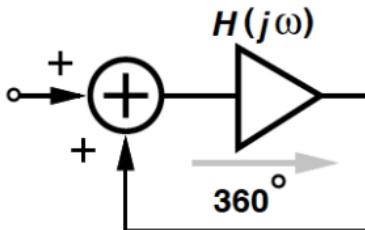
- “Barkhausen criteria.” (necessary but not sufficient.)
- May state 2nd criterion as a total phase shift of 360° .
- Loop gain typically chosen to be at least 2 or 3 times the required value.

2nd Barkhausen Criterion

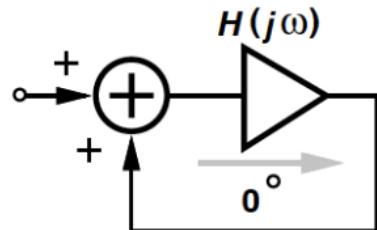
- Equivalent in terms of the second Barkhausen criterion:



(a)



(b)

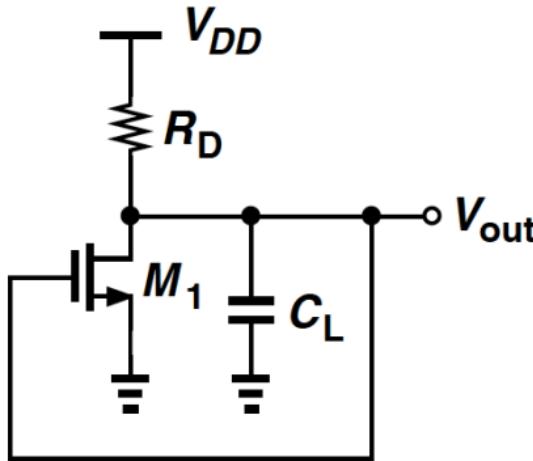


(c)

- (a): Frequency-dependent phase shift = 180° (arrow), dc phase shift = 180° .
- (b): Total phase shift at ω_0 = 360° .
- (c): No phase shift at ω_0 is provided.

Example 15.1

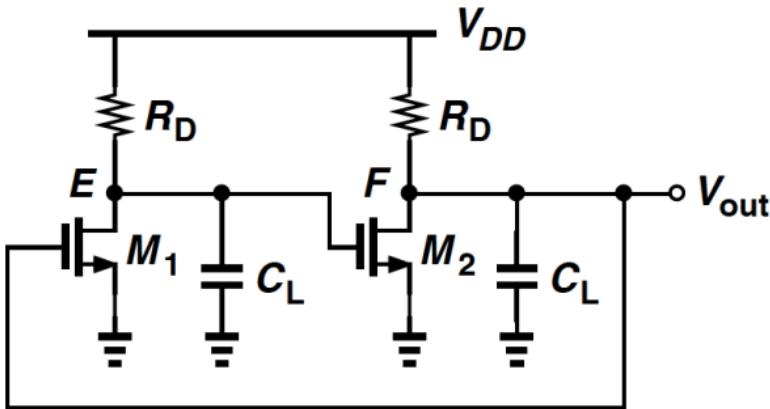
Explain why a single common-source stage does not oscillate if it is placed in a unity-gain loop?



Solution

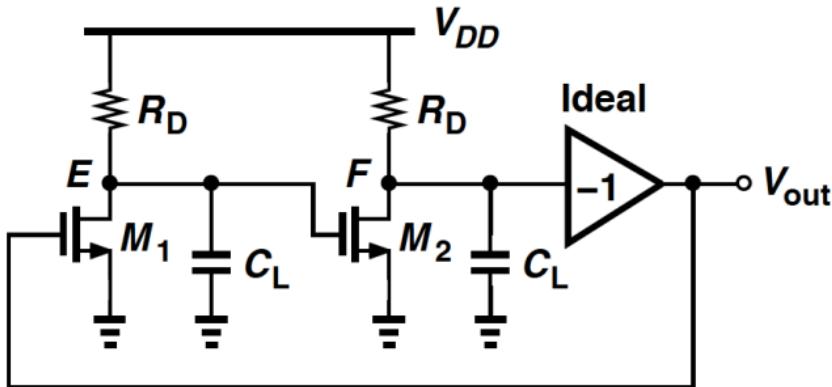
- Open-loop circuit of a single CS stage contains only one pole.
 - Maximum frequency-dependent phase shift = 90° (at a frequency of infinity).
 - DC phase shift = 180° .
 - Maximum total phase shift = 270° ($<360^\circ$).
- Fail to sustain oscillation growth.

Two-Pole Feedback System



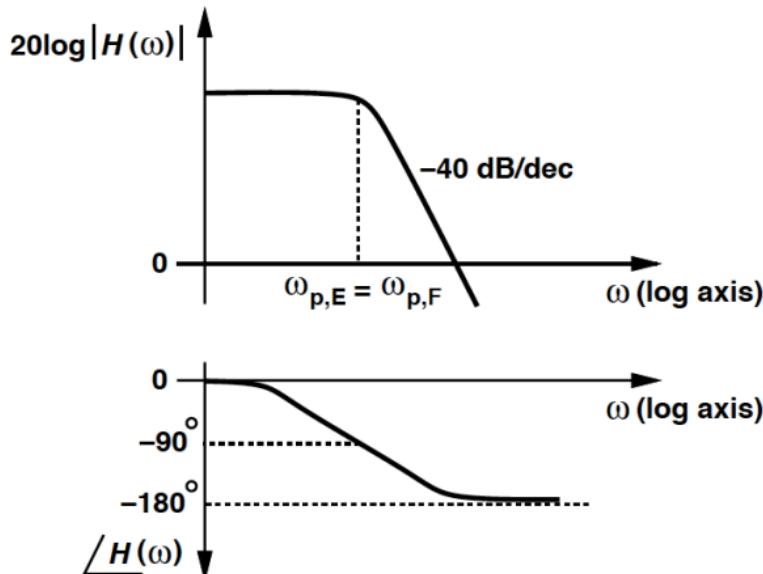
- Two significant poles appear in the signal path □ frequency-dependent phase shift can approach 180°.
- Signal inversion through each common-source stage □ positive feedback!
- It simply “latches up” rather than oscillates.

Additional Signal Inversion



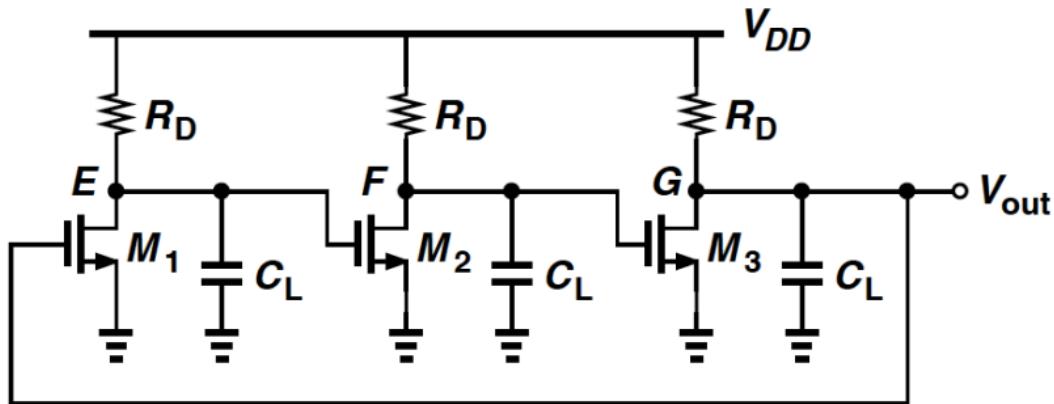
- This provides negative feedback near zero frequency & eliminates “latch-up”.
- Two poles: One at E and another at F.
- Does this circuit oscillate?

Two-Pole System: Loop Gain Characteristics



- Frequency-dependent phase shift reaches 180° but at $\omega = \infty$.
- Loop gain vanishes at very high frequencies \square the circuit (Slide 8) does not satisfy both Barkhausen criteria at the same frequency.
- It fails to oscillate!

Three-Stage Ring Oscillator



- If three stages are identical, total phase shift around the loop (ϕ) = -135° at $\omega = \omega_p$, E(= ω_p , F = ω_p , G) and -270° at $\omega = \infty$.
- $\phi = 180^\circ$ at $\omega < \infty$, where the loop gain can be still ≥ 1 .

Minimum Voltage Gain Per Stage

- For the three-stage ring oscillator, denote the transfer function of each stage by $-A_0/(1+s/\omega_0)$ and the loop gain is:

$$H(s) = -\frac{A_0^3}{(1 + \frac{s}{\omega_0})^3}.$$

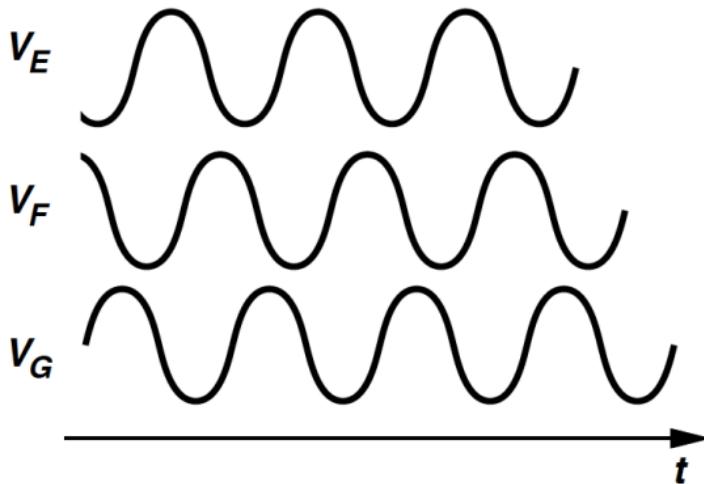
- The circuit oscillates if each stage contributes 60° :

$$\tan^{-1} \frac{\omega_{osc}}{\omega_0} = 60^\circ \quad \omega_{osc} = \sqrt{3}\omega_0.$$

- Minimum voltage gain per stage (A_0) is such that the magnitude of the loop gain at ω_{OSC} is unity:

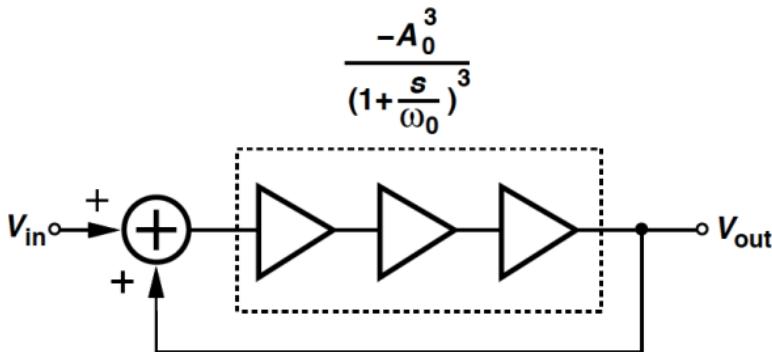
$$\frac{A_0^3}{\left[\sqrt{1 + (\frac{\omega_{osc}}{\omega_0})^2}\right]^3} = 1. \quad \square \quad A_0 = 2.$$

Waveforms of Three-Stage Ring Oscillator



- Each stage contributes a frequency-dependent shift of 60° and a dc signal inversion.
- Thus the waveform at each node is 240° (or 120°) out of phase with respect to its neighboring nodes.

Linear Model of Three-Stage Oscillator



- The close-loop transfer function of the linear feedback model is:

$$\begin{aligned}\frac{V_{out}(s)}{V_{in}(s)} &= \frac{\frac{-A_0^3}{(1+s/\omega_0)^3}}{1 + \frac{A_0^3}{(1+s/\omega_0)^3}} \\ &= \frac{-A_0^3}{(1+s/\omega_0)^3 + A_0^3}.\end{aligned}$$

- Expand the denominator as:

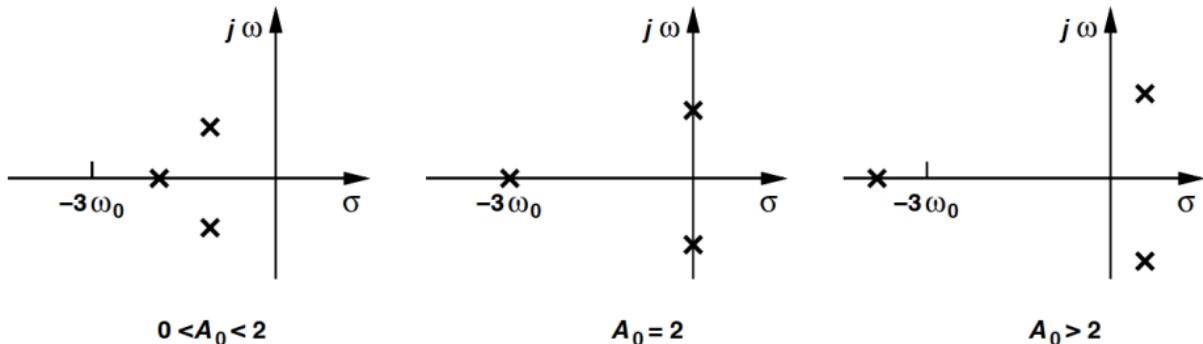
3 Poles:

$$(1 + \frac{s}{\omega_0})^3 + A_0^3 = (1 + \frac{s}{\omega_0} + A_0) \left[(1 + \frac{s}{\omega_0})^2 - (1 + \frac{s}{\omega_0})A_0 + A_0^2 \right].$$

$$s_1 = (-A_0 - 1)\omega_0$$

$$s_{2,3} = [\frac{A_0(1 \pm j\sqrt{3})}{2} - 1]\omega_0.$$

Poles of Three-Stage Ring Oscillator



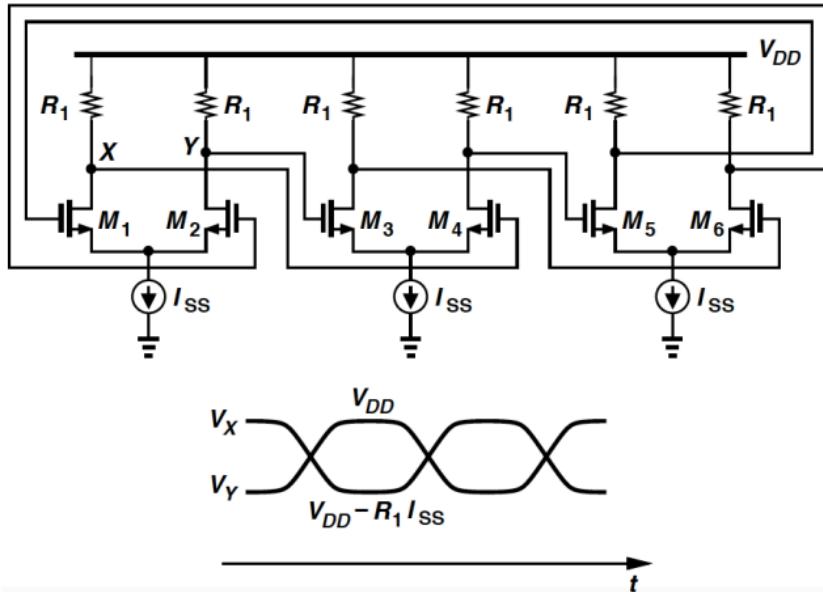
- For $A_0 > 2$, the two complex poles exhibit a positive real part, which give rise to a growing sinusoid.
- Express the output waveform as: (neglect effect of s1.)

$$V_{out}(t) = a \exp\left(\frac{A_0 - 2}{2}\omega_0 t\right) \cos\left(\frac{A_0\sqrt{3}}{2}\omega_0 t\right).$$

- The exponential envelope grows to infinity if $A_0 > 2$.

Example 15.2

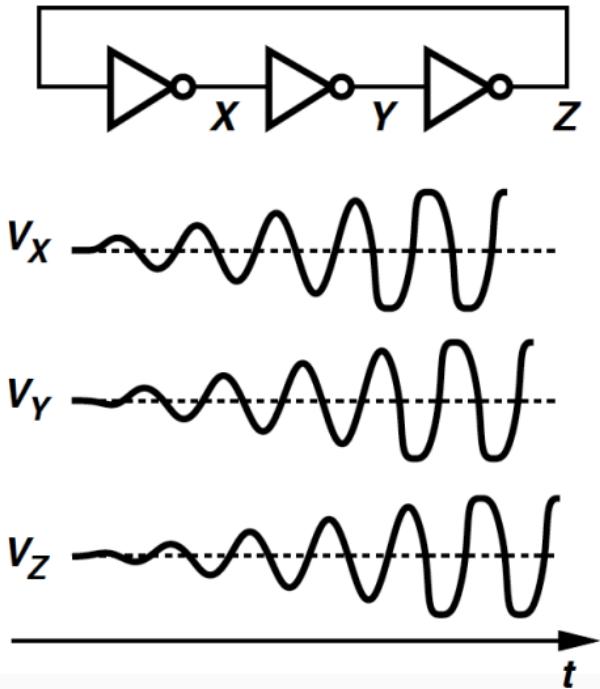
For a differential implementation of the three-stage ring oscillator, what is the maximum voltage swing of each stage?



Solution

- If the gain per stage is well above 2, the amplitude grows until each differential pair experiences complete switching.
- The swing at each node is equal to $I_{SS}R_1$.
- As shown in the waveforms, each stage is in its high-gain region for only a fraction of the period.

Ring Oscillator Using CMOS Invertors (I)



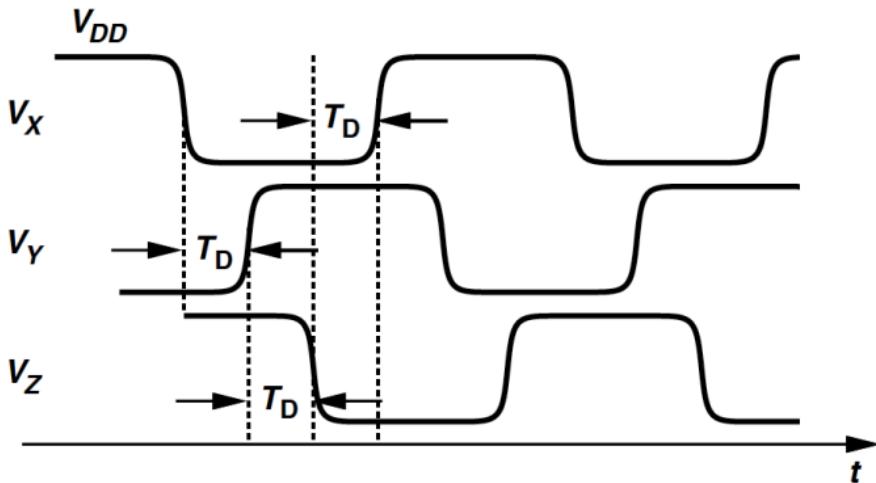
The circuit is released with an initial voltage at each node = V_{trip} .

Noise components disturb each node voltage, yielding a growing waveform.

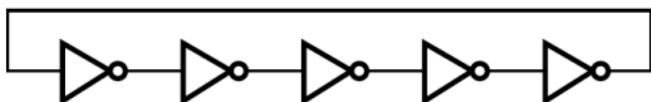
The signal eventually exhibits rail-to-rail swings.

Ring Oscillator Using CMOS Invertors (II)

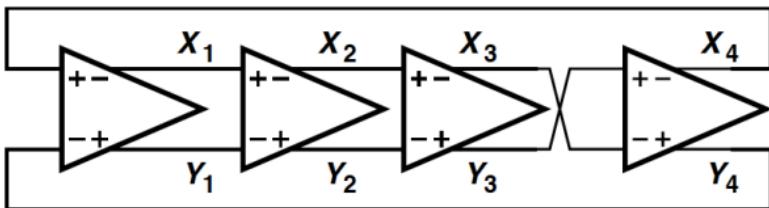
- Begin with $V_X = VDD \square VY = 0, VZ = VDD$.
- VX begins to fall to zero when the circuit is released
 - \square forces VY to rise to VDD after one TD , and VZ to fall to zero after another TD .
- Oscillate with a delay of TD between consecutive node voltages \square period = $6TD$.



Ring Oscillators: More Than Three Stages



(a)



(b)

- Total number of inversions in the loop must be odd to prevent “latch-up”.
- (a): a ring incorporates five inverters \square frequency = $1/(10\text{TD})$.
- (b): The differential implementation can utilize an even number of stages by configuring one stage such that it does not invert.

Example 15.3

What is the minimum required voltage gain per stage in circuit (b) (Slide 18)? How many signal phases are provided by the circuit?

Solution

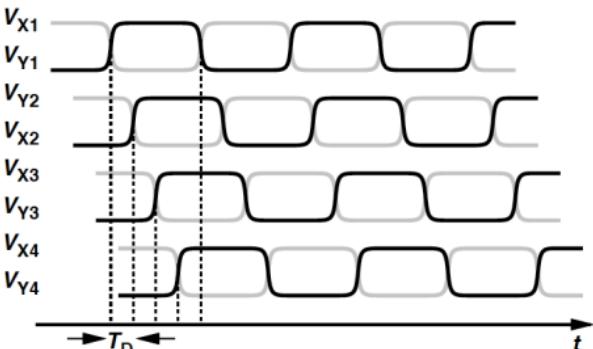
- Using similar notation as before, we have: $H(s) = -\frac{A_0^4}{(1 + \frac{s}{\omega_0})^4}$.
- For the circuit to oscillate, each stage must contribute a frequency-dependent phase shift of $180^\circ/4 = 45^\circ$.

• $\tan^{-1}\omega_{osc}/\omega_0 = 45^\circ \quad \square \quad \omega_{osc} = \omega_0$

$$\frac{A_0}{\sqrt{1 + (\frac{\omega_{osc}}{\omega_0})^2}} = 1.$$

□ minimum voltage gain:

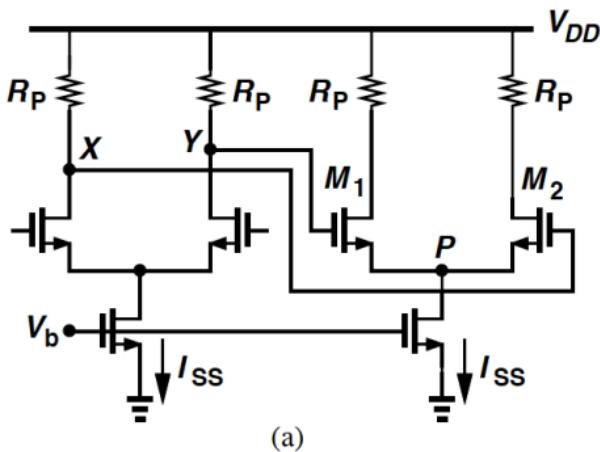
- The oscillator provides four phases and their complements, as illustrated in the figure.



Example 15.4 (I)

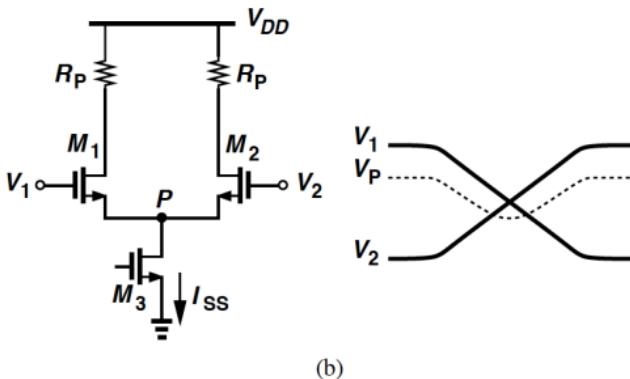
Determine the maximum voltage swings and minimum supply voltage of a ring oscillator incorporating differential pairs with resistive loads if no transistor must enter the triode region.

Solution



- In (a), complete switching \square V_X or V_Y varies between V_{DD} and $V_{DD} - I_{SS}R_P$.
- M_1 fully on: Its gate and drain voltages are equal to V_{DD} and $V_{DD} - I_{SS}R_P$, respectively.
- To remain in saturation, $I_{SS}R_P \leq V_{TH}$.
- The peak-to-peak at each swing at each drain must not exceed V_{TH} .

Example 15.4 (II)



In (b), assume the inputs vary between V_{DD} and V_{DD} – ISSRP.

When V₁ is equal to V_{DD} and M₁ carries all of I_{SS} we have:

$$V_P = V_{DD} - \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}(W/L)_{1,2}}} - V_{TH}.$$

- When the difference between V₁ and V₂ reaches $\sqrt{2}(V_{GS,eq} - V_{TH})$, M₂ turns on. Calculate V_P after this point:

$$\square \quad \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_{1,2}(V_1 - V_P - V_{TH})^2 + \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_{1,2}(V_2 - V_P - V_{TH})^2 = I_{SS}$$

$$\square \quad 2V_P^2 - 2(V_1 - V_{TH} + V_2 - V_{TH})V_P + (V_1 - V_{TH})^2 + (V_2 - V_{TH})^2 - \frac{2I_{SS}}{\mu_n C_{ox}(W/L)_{1,2}} = 0$$

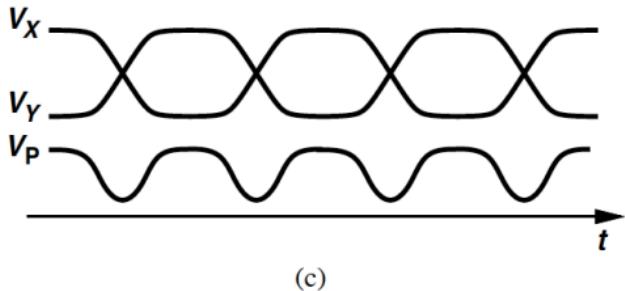
$$\square \quad V_P = \frac{1}{2}[V_1 + V_2 - 2V_{TH} \pm \sqrt{-(V_1 - V_2)^2 + \frac{4I_{SS}}{\mu_n C_{ox}(W/L)_{1,2}}}]$$

- If V₁ – V_{CM} + ΔV and V₂ – V_{CM} – ΔV, where V_{CM} = V_{DD} – ISSRP/2.

$$\square \quad V_P = V_{CM} - V_{TH} \pm \frac{1}{2}\sqrt{-(2\Delta V)^2 + \frac{4I_{SS}}{\mu_n C_{ox}(W/L)_{1,2}}}.$$

$$V_{P,min} = V_{CM} - V_{TH} - \sqrt{\frac{I_{SS}}{\mu_n C_{ox}(W/L)_{1,2}}}.$$

Example 15.4 (III)



(c)

- (c) shows typical waveforms in the oscillator.
- VP varies at twice the oscillation frequency.

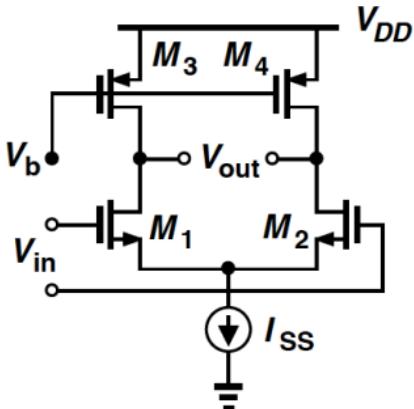
- Write $V_{P,\min} \geq V_{ISS}$, where V_{ISS} denotes the minimum required voltage across ISS. Thus,

$$V_{DD} - \frac{R_P I_{SS}}{2} - V_{TH} - \sqrt{\frac{I_{SS}}{\mu_n C_{ox} (W/L)_{1,2}}} \geq V_{ISS}$$

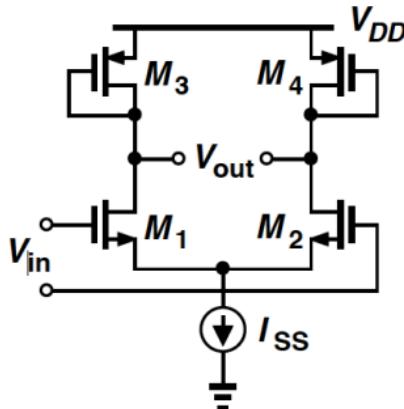
and

$$V_{DD} \geq V_{ISS} + V_{TH} + \sqrt{\frac{I_{SS}}{\mu_n C_{ox} (W/L)_{1,2}}} + \frac{R_P I_{SS}}{2}$$

Differential Stage Using PMOS Loads (I)



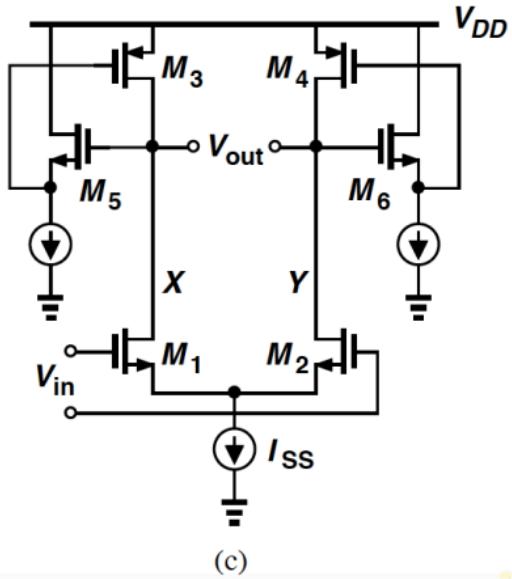
(a)



(b)

- (a): A PMOS transistor operating in the deep triode region can serve as the load.
- (b): Diode-connected load, at the cost of one threshold voltage in the headroom.

Differential Stage Using PMOS Loads (II)



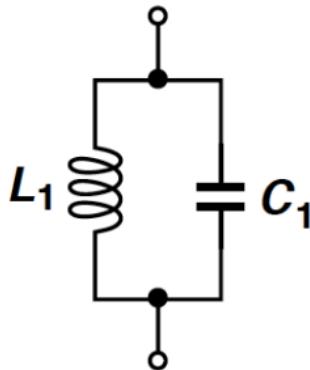
(c): A more efficient load where NMOS source followers are inserted.

M3 & M4 consume only a voltage headroom = $|V_{DS3,4}|$.

If $V_{GS5} \approx V_{TH3}$ □ M3 operates at the edge of triode region and the small-signal resistance of the load $\approx 1/gm_3$.

Gate-source capacitance of M3 driven by the source follower □ time constant associated with the load is smaller than that of a diode-connected transistor.

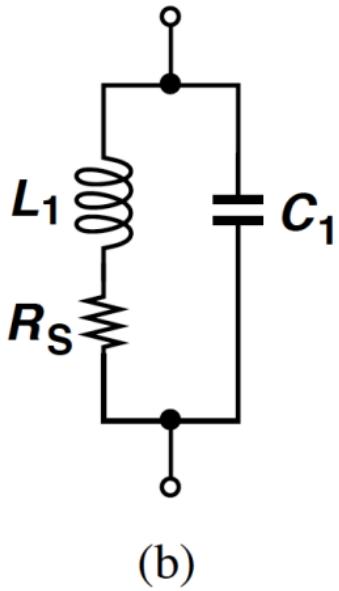
Ideal LC Tank



(a)

- (a): **L1 in parallel with C1 (ideal LC tank), resonates at**
 $\omega_{res} = 1/\sqrt{L_1 C_1}$
- **At ω_{res} , impedances $jL_1\omega_{res}$ and $1/(jC_1\omega_{res})$ are equal and opposite,** infinite impedance infinite quality factor, Q.

Realistic LC Tank



- In practice, inductors (and capacitors) suffer from resistive components.
- Series resistance of the metal wire used in the inductor can be modeled as (b).
- Define Q of the inductor as $L_1\omega/R_S$.
- The equivalent impedance is:

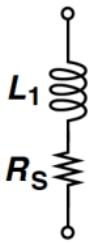
$$Z_{eq}(s) = \frac{R_S + L_1 s}{1 + L_1 C_1 s^2 + R_S C_1 s}.$$

□

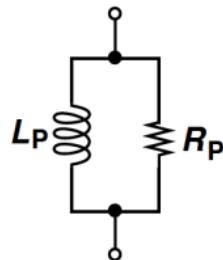
$$|Z_{eq}(s = j\omega)|^2 = \frac{R_S^2 + L_1^2 \omega^2}{(1 - L_1 C_1 \omega^2)^2 + R_S^2 C_1^2 \omega^2}.$$

- Impedance never goes to infinity. The circuit has a finite Q.

Conversion of Series to Parallel Combination



(a)



(b)

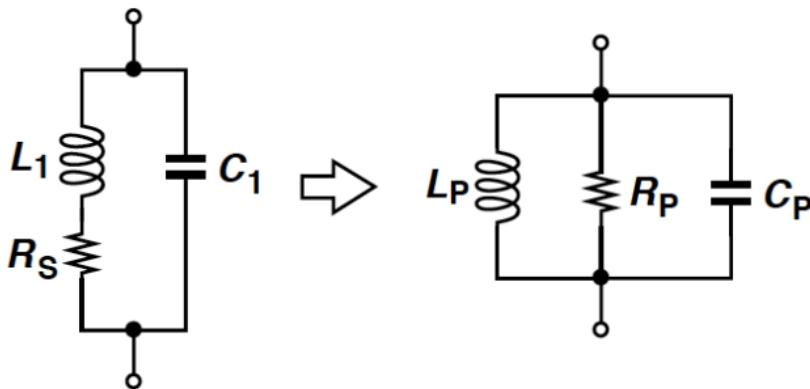
- **For the two impedances to be equivalent:** $L_1s + R_S = \frac{R_P L_P s}{R_P + L_P s}$.
- **Assuming $s = j\omega$:** $(L_1 R_P + L_P R_S)j\omega + R_S R_P - L_1 L_P \omega^2 = R_P L_P j\omega$.
- **This relationship must hold for all ω (in a narrow range):**

$$L_1 R_P + L_P R_S = R_P L_P$$

- $R_S R_P - L_1 L_P \omega^2 = 0.$ $L_P = L_1 \left(1 + \frac{R_S^2}{L_1^2 \omega^2}\right).$
- **Recall $L_1 \omega / R_S = Q$, typically greater than 10^3 for monolithic inductors** \square and

$$\begin{aligned} L_P &\approx L_1 & R_P &\approx \frac{L_1^2 \omega^2}{R_S} \\ &&&\approx Q^2 R_S. \end{aligned}$$

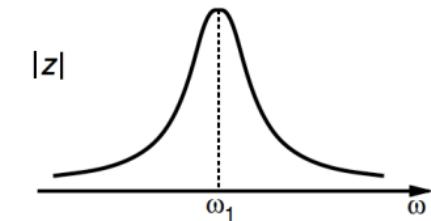
Conversion of Tank to Parallel Components



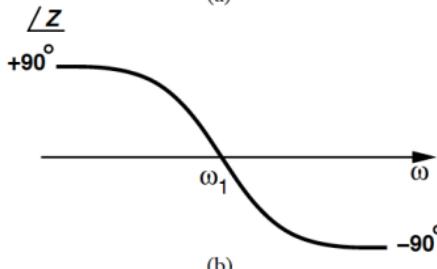
- The previous series/parallel transformation allows this conversion, and $C_P = C_1$.
- The equivalence of course breaks down as ω departs substantially from the resonance frequency.
- At $\omega_1 = 1/\sqrt{L_p C_p}$, the tank reduces to a simple resistor.

Tank Impedance vs. Frequency

- Plotting magnitude of the tank impedance vs. frequency in (a), we note that the behavior is:
 - inductive for $\omega < \omega_1$.
 - capacitive for $\omega > \omega_1$.
- surmise that the phase of the impedance is positive for $\omega < \omega_1$ and negative for $\omega > \omega_1$, as in (b).

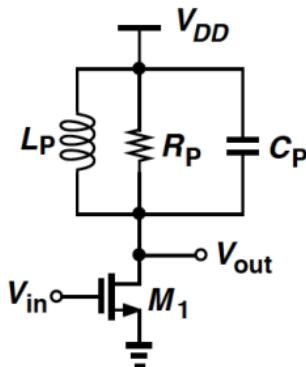


(a)

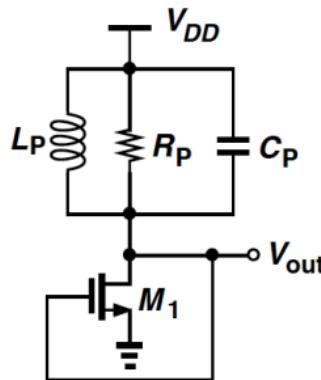


(b)

Tuned Gain Stage



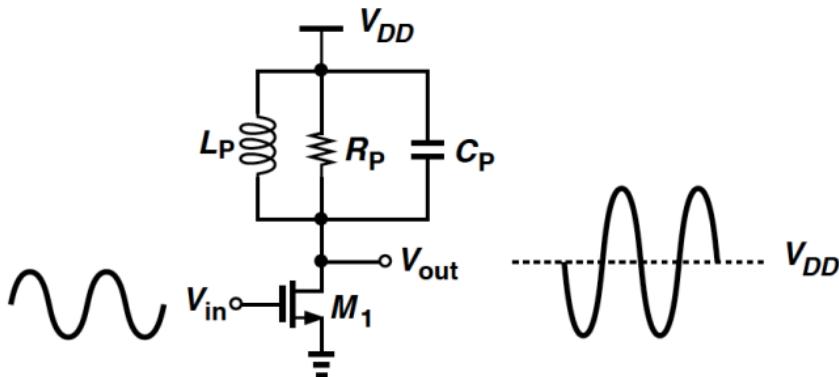
(a)



(b)

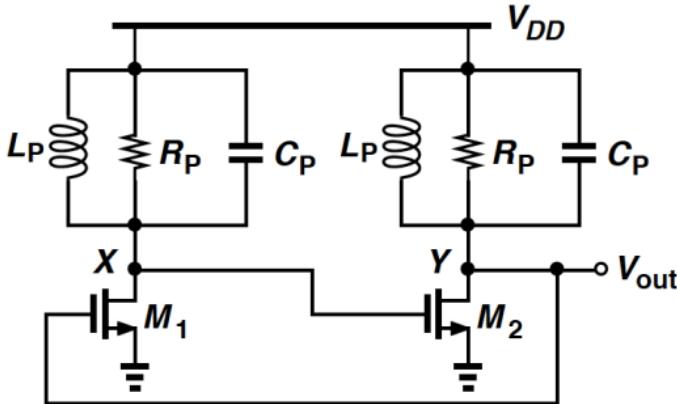
- (a): At resonance, $jL_P\omega = 1/(jC_P\omega)$, voltage gain equals $-gm_1R_P$.
- From (b), the frequency-dependent phase shift of the tank never reaches 180° .
 - circuit (b) does not oscillate.

Output Signal Levels in Tuned Stage



- The stage is biased at a drain current I_1 .
- If the series resistance of L_P is small, dc level of V_{out} is close to V_{DD} .
- Apply a small sinusoidal voltage at the resonance frequency at input □ V_{out} : An inverted sinusoid with an average value near V_{DD} .
- The peak output level exceeds the supply voltage.

Two Tuned Stage in Feedback Loop

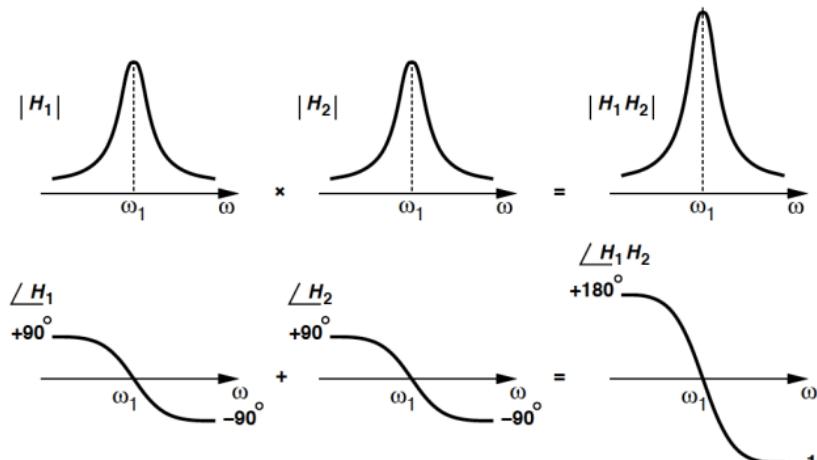


- This configuration does not latch up because its low-frequency gain is very small.
- At resonance, total phase shift around the loop is zero.
- If $gm_1RPgm_2RP \geq 1$, then the loop oscillates.

Example 15.5

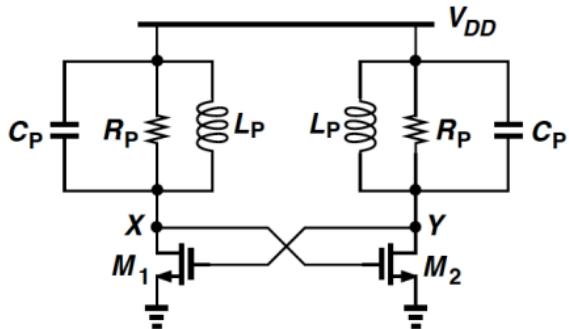
Sketch the open-loop voltage gain and phase of the previous circuit. Neglect transistor capacitances.

Solution

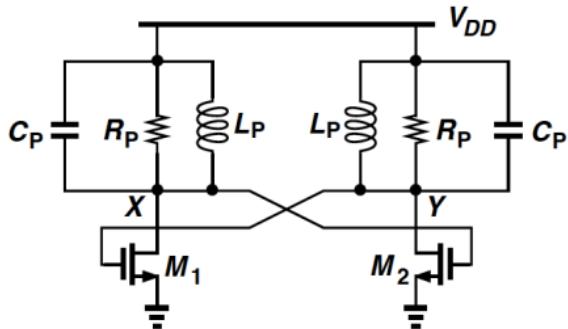


- The magnitude has a shape with sharper rise and fall because it results from the product of those of the two stages.
- The total phase at low frequency is given by signal inversion by each cs-stage plus a 90° phase shift due to each tank. A similar behavior occurs at high frequencies.

Crossed-Coupled Oscillator



(a)

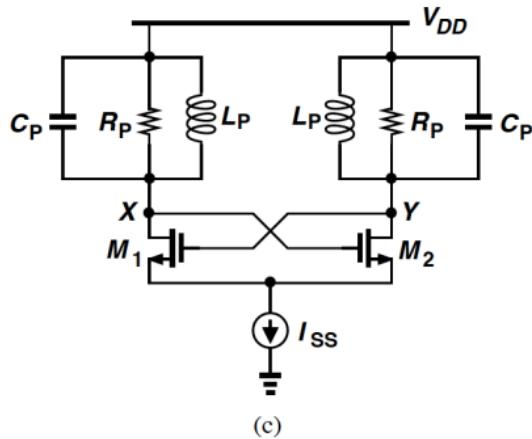


(b)

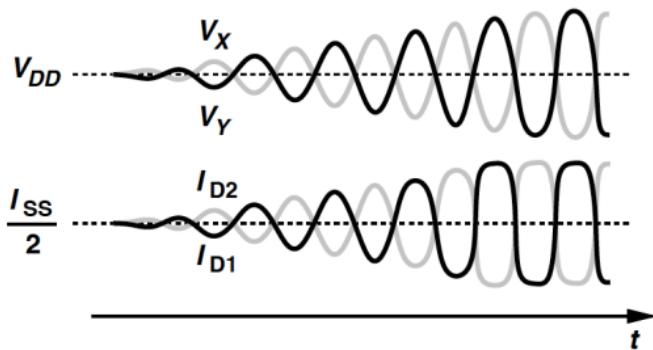
- The previous circuit (Slide 35) is sometimes drawn as in above configuration (a) or (b).
- However, the drain currents of M_1 and M_2 and hence the output swings heavily depend on V_{DD} .
- The waveforms at X and Y are differential □ (b) suggests that M_1 and M_2 can be converted to differential pair as depicted in Example 15.6.

Example 15.6

For the circuit configuration (c), plot V_X and V_Y and ID_1 and ID_2 as the oscillation begins.

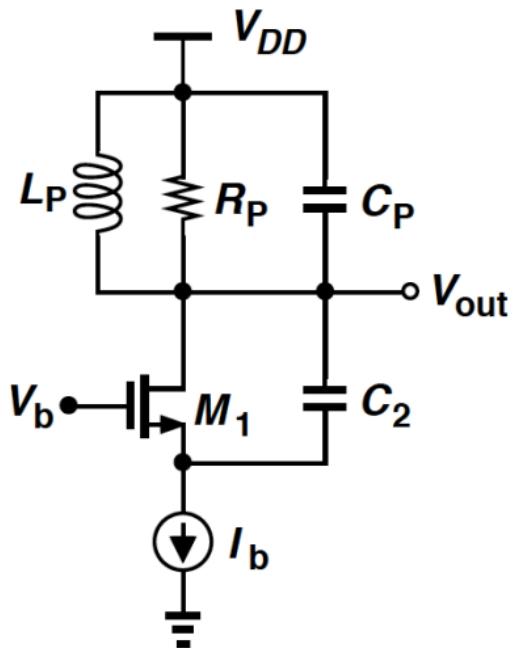


Solution



- The oscillation amplitude grows until the loop gain drops at the peaks.
- In fact, if $gm_{1,2}RP$ is large enough, the difference between $V_X - V_Y$ reaches a level that steers the entire tail current to one transistor, turning the other off.
- In the steady state, ID_1 and ID_2 vary between 0 and ISS .

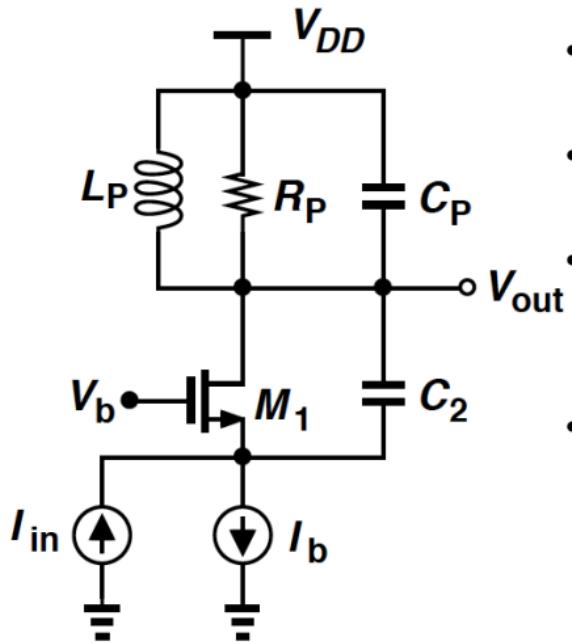
Tuned Stage with Feedback (I)



(a)

- (a): We surmise that if the drain voltage is returned to the source rather than the gate, the circuit may oscillate.
- Capacitor incorporated to avoid disturbing the bias point of M_1 .
- Unfortunately, the circuit does not oscillate due to insufficient loop gain.

Tuned Stage with Feedback (II)



(b)

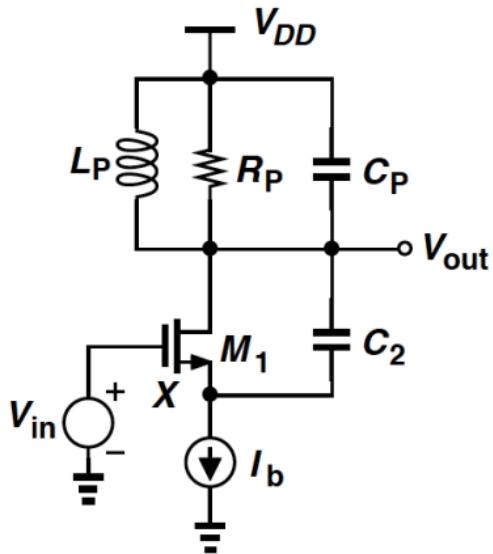
- Apply an input current as in (b).
- M_1 and C_2 directly conduct the input current to the tank.
- Obtain the close-loop gain as:

$$\frac{V_{out}}{I_{in}} = L_P s \parallel \frac{1}{C_P s} \parallel R_P$$

- Since the close-loop gain cannot be equal to infinity at any frequency, the circuit fails to oscillate.

Example 15.7

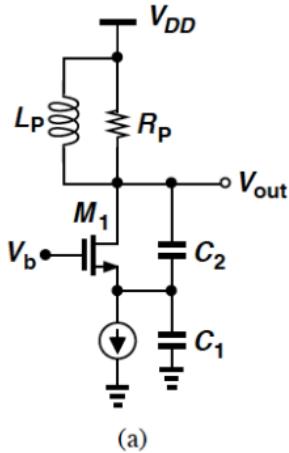
Why the input to the feedback system is realized as a current source applied to the source of the transistor rather than a voltage source applied to its gate?



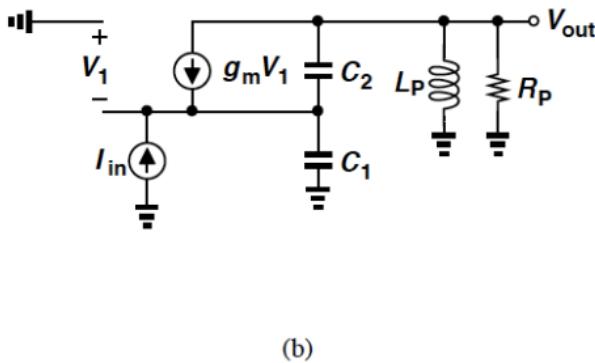
Solution

- With a finite variation of V_{in} , the change in I_b is still zero if the bias current source is ideal.
- Neglect source-bulk junction capacitance of M_1 □ change in tank current is zero, yielding $V_{out}/V_{in} = 0$.
- V_X does vary with V_{in} , but M_1 generates a small-signal current that cancels that through C_2 .
- $V_X/V_{in} = gm/(gm + C_2 s)$.

Colpitts Oscillator (I)



(a)



(b)

- Add C1 to node X and remove CP as shown in (a).
- Approximating M1 by a single voltage-dependent current source, we construct equivalent circuit (b).
- We obtain:

$$V_1 = -\left(I_{in} - \frac{V_{out}}{L_P s} - \frac{V_{out}}{R_P}\right) \frac{1}{C_1 s}.$$

Colpitts Oscillator (II)

- We sum all of the currents at the output node:

$$-g_m(I_{in} - \frac{V_{out}}{L_P s} - \frac{V_{out}}{R_P})\frac{1}{C_1 s} + [V_{out} - (I_{in} - \frac{V_{out}}{L_P s} - \frac{V_{out}}{R_P})\frac{1}{C_1 s}]C_2 s + \frac{V_{out}}{L_P s} + \frac{V_{out}}{R_P} = 0.$$

□ $\frac{V_{out}}{I_{in}} = \frac{R_P L_P s(g_m + C_2 s)}{R_P C_1 C_2 L_P s^3 + (C_1 + C_2) L_P s^2 + [g_m L_P + R_P(C_1 + C_2)]s + g_m R_P}.$

- The circuit oscillates if the close-loop transfer function goes to infinity at an imaginary value of s , $sR = j\omega_R$.

□

$$-R_P C_1 C_2 L_P \omega_R^3 + [g_m L_P + R_P(C_1 + C_2)]\omega_R = 0$$

$$-(C_1 + C_2)L_P \omega_R^2 + g_m R_P = 0.$$

- With typical values, $g_m L_P \ll R_P(C_1 + C_2)$, we obtain:

$$\omega_R^2 = \frac{1}{L_P \frac{C_1 C_2}{C_1 + C_2}}, \quad \text{and} \quad \begin{aligned} g_m R_P &= \frac{(C_1 + C_2)^2}{C_1 C_2} \\ &= \frac{C_1}{C_2} \left(1 + \frac{C_2}{C_1}\right)^2. \end{aligned}$$

Colpitts Oscillator (III)

- **gmRP** is the voltage gain from the source of M1 to the output. C1/C2 for minimum required gain occurs for C1/C2 = 1, requiring

$$g_m R_P \geq 4.$$

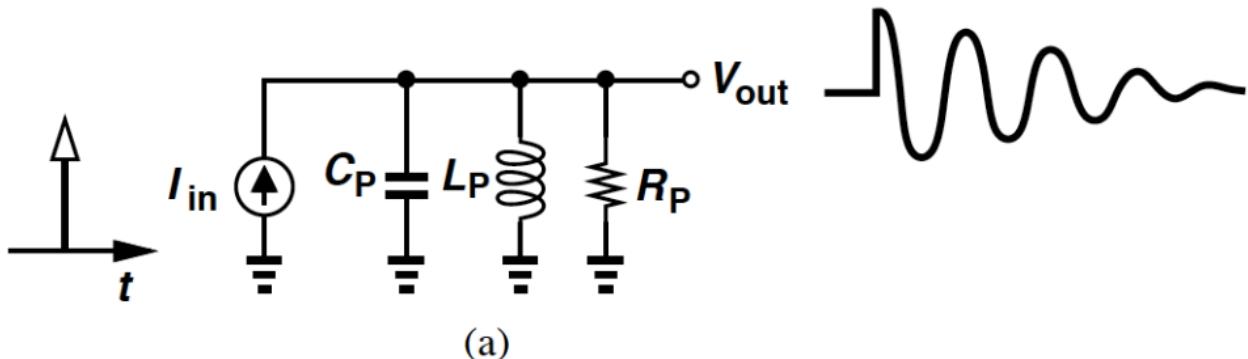
- If the capacitance that appears in parallel with the inductor, CP, is included in the equivalent circuit, ω_R^2 is modified as:

$$\omega_R^2 = \frac{1}{L_P(C_P + \frac{C_1 C_2}{C_1 + C_2})}$$

remaining unchanged.
 $g_m R_P \geq 4.$

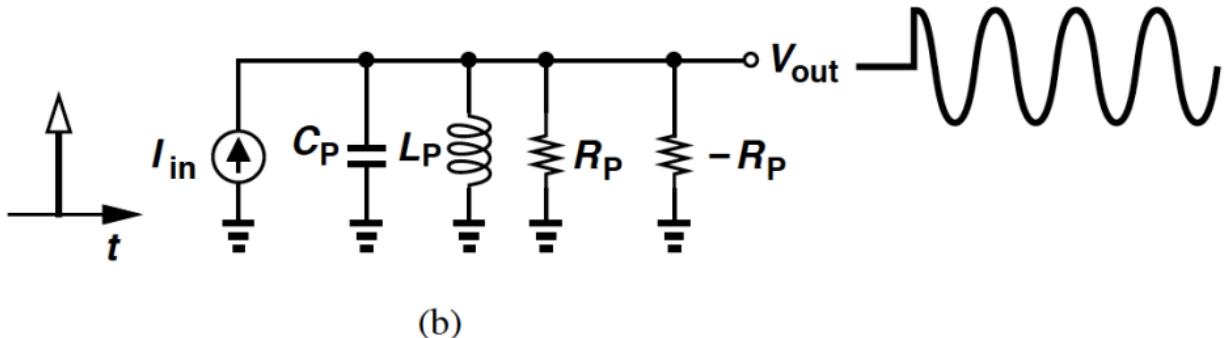
- CP is simply included in parallel with the series combination of C1 and C2.

Decaying Impulse Response of Tank

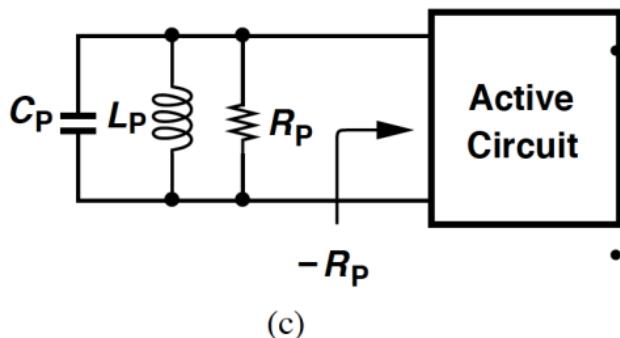


- (a): A simple tank that is stimulated by a current impulse.
- The tank responds with a decaying oscillatory behavior.
- In every cycle, some of the energy that reciprocates between the capacitor and the inductor is lost in the form of heat in the resistor.

One-Port Oscillator

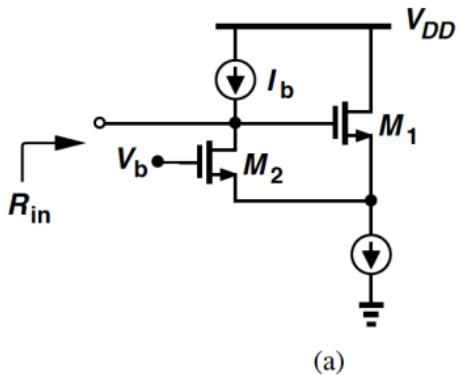


- (b): $R_P||(-R_P) = \infty \square$ the tank oscillates indefinitely.



- (c): A one-port circuit exhibiting a negative resistance placed in parallel with a tank \square the combination may oscillate.
- (c) is called a one-port oscillator.

Negative Resistance



(a)

- (a): Implement the feedback by a common-gate stage and add I_b to provide the bias current of M_2 .
- From the equivalent circuit in (b), we have:

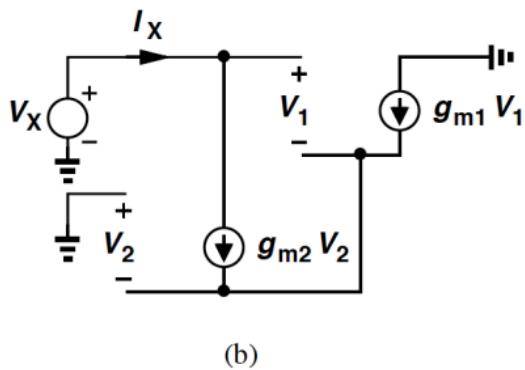
$$I_X = g_{m2}V_2 = -g_{m1}V_1$$

and

$$\begin{aligned} V_X &= V_1 - V_2 \\ \square &= -\frac{I_X}{g_{m1}} - \frac{I_X}{g_{m2}}. \end{aligned}$$

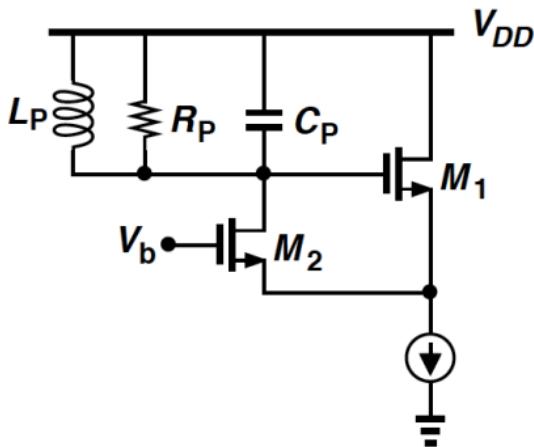
$$\square \frac{V_X}{I_X} = -\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right),$$

If $\frac{1}{g_{m1}} = \frac{1}{g_{m2}}$,



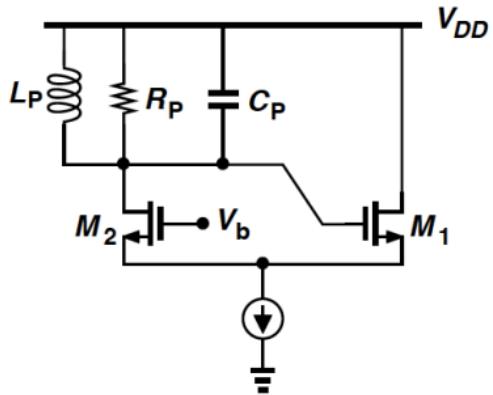
$$\frac{V_X}{I_X} = \frac{-2}{g_m}.$$

Oscillator Using Negative Rin (I)

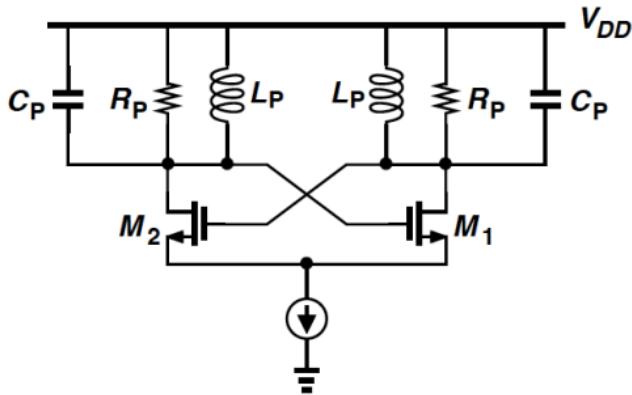


- RP denotes the equivalent parallel resistance of the tank.
- For oscillation build-up, $RP - 2/gm \geq 0$.
- If the small-signal resistance represented by M_1 and M_2 to the tank is less negative than $-RP$ □ the circuit experiences large swings such that each transistor is nearly off for part of the period.
- This yields an “average” resistance of $-RP$.

Oscillator Using Negative Rin (II)



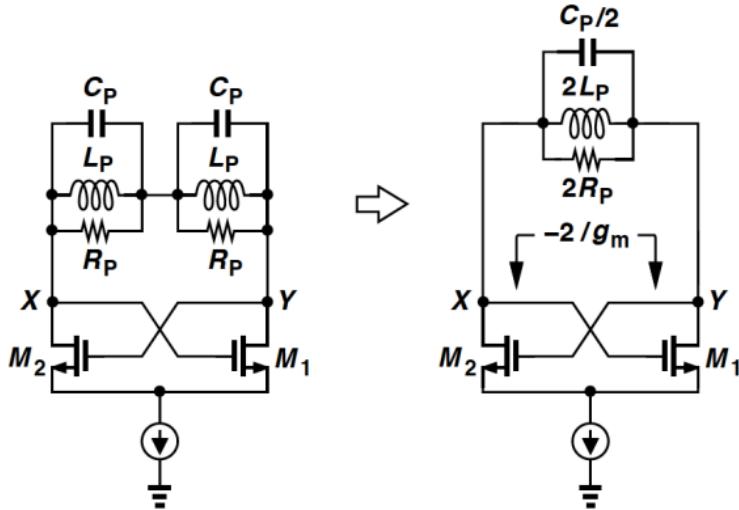
(a)



(b)

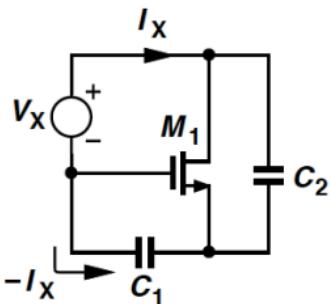
- The circuit (Slide 45) can be redrawn as (a).
- (b) is obtained, if the drain current of M1 flows through a tank and the resulting voltage is applied to the gate of M2.

Negative-Gm Oscillator

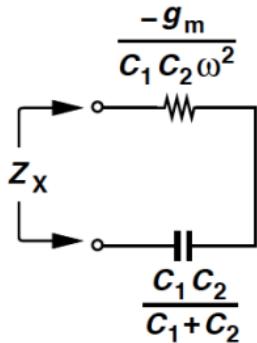


- We ignore bias paths and merge the two tanks in previous topology (b) (Slide 46) into one, as shown above.
- To enable oscillation, the cross-coupled pair must provide a negative resistance of $-RP$ between nodes X and Y.
- $-RP = -2/g_m$ and hence it is necessary that $RP \geq 1/g_m$.
- Also called a “negative-Gm oscillator”.

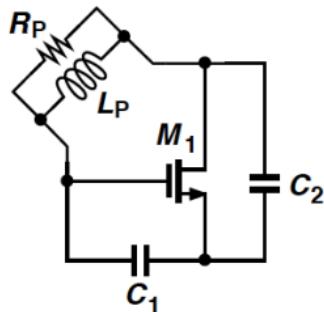
Another Way to Create Negative R (I)



(a)



(b)

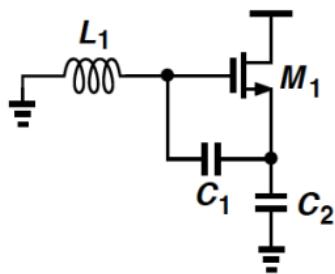


(c)

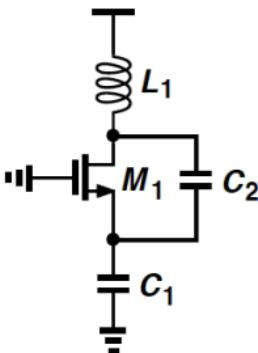
- (a) shows another method of creating negative resistance. We have:
$$V_X = (I_X - \frac{-I_X g_m}{C_1 s}) \frac{1}{C_2 s} + \frac{I_X}{C_1 s} \quad \square \quad \frac{V_X}{I_X} = \frac{g_m}{C_1 C_2 s^2} + \frac{1}{C_2 s} + \frac{1}{C_1 s}.$$
- This impedance consists of a negative resistance equal to $-gm/(C_1 C_2 \omega^2)$ in series with the series combination of C_1 and C_2 , as in (b).
- (c): If an inductor is placed between the gate and drain of M_1 , the circuit may oscillate.

Another Way to Create Negative R (II)

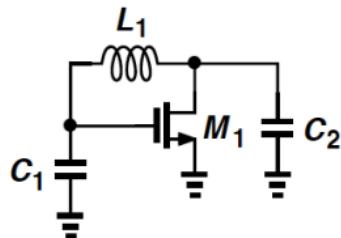
- Three oscillator topologies derived from previous circuit (c) (Slide 48).



(a)



(b)



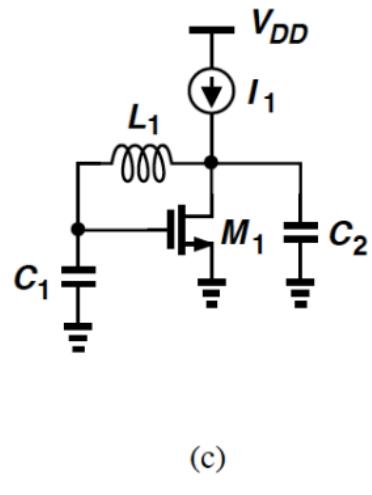
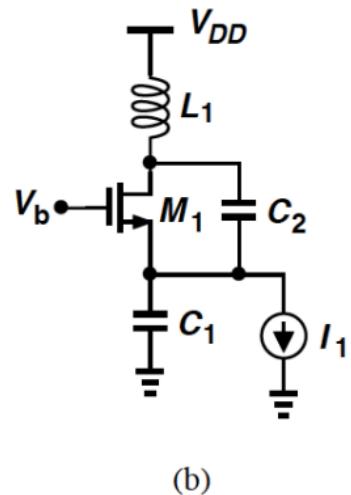
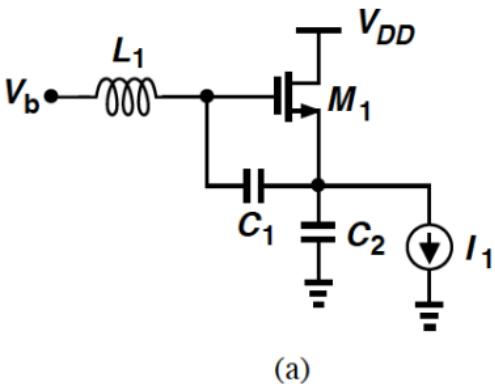
(c)

- (a): Based on a source follower.
- (b): Colpitts oscillator.

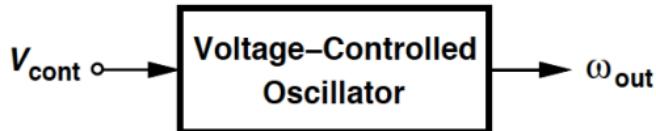
Example 15.8

Redraw the three circuits (Slide 49) with proper biasing.

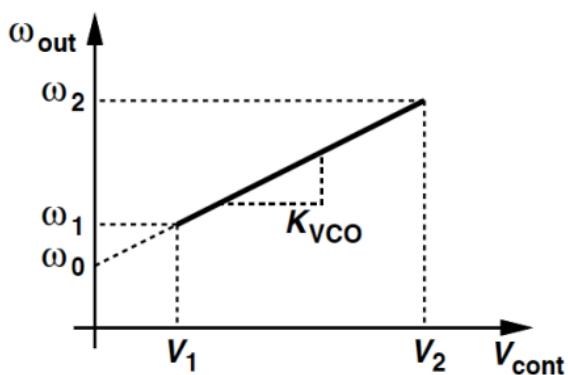
Solution



Voltage-Controlled Oscillator: Definition



- Ideal voltage-controlled oscillator (VCO): Output frequency is a linear function of its control voltage:



$\omega_{out} = \omega_0 + K_{VCO}V_{cont}$.
 ω_0 : intercept corresponding to $V_{cont} = 0$.
 K_{VCO} : “Gain” or “sensitivity” of the circuit.
 $\omega_2 - \omega_1$: “Tuning range”.

Example 15.9

In the negative-Gm oscillator (Slide 35), CP = 0, consider only CDB of M1 and M2. Explain why VDD can be viewed as the control voltage. Calculate the gain of the VCO.

Solution

- CDB varies with VDB $\square \omega_{res}$ changes with VDD.
- The average voltage across CDB \approx VDD, we write:

and

$$C_{DB} = \frac{C_{DB0}}{\left(1 + \frac{V_{DD}}{\phi_B}\right)^m}, \quad K_{VCO} = \frac{\partial \omega_{out}}{\partial V_{DD}}$$
$$= \frac{\partial \omega_{out}}{\partial C_{DB}} \cdot \frac{\partial C_{DB}}{\partial V_{DD}}.$$

\square

$$K_{VCO} = \frac{-1}{2\sqrt{L_P C_{DB}} C_{DB}} \cdot \frac{-m C_{DB}}{\phi_B \left(1 + \frac{V_{DD}}{\phi_B}\right)}$$
$$= \frac{m}{2\phi_B \left(1 + \frac{V_{DD}}{\phi_B}\right)} \cdot \omega_{out}.$$

- Th and Vcont is nonlinear because KVCO varies with VDD and ω_{out} .

Parameters of VCO (I)

Center Frequency:

- determined by the environment in which the VCO is used.
- can achieve as high as hundreds of gigahertz.

Tuning Range:

- The required tuning range is dictated by:
 - (1) variation of the VCO center frequency with process and temperature.
 - (2) frequency range necessary for the application.
- Noise in the output frequency is proportional to KVCO because $\omega_{out} = \omega_0 + KVCOV_{cont}$.
- To minimize the effect of noise in V_{cont} □ VCO gain must be minimized, which conflicts with the required tuning range.
- If allowable range of V_{cont} : From V_1 to V_2 , tuning range must span at least ω_1 to ω_2 □

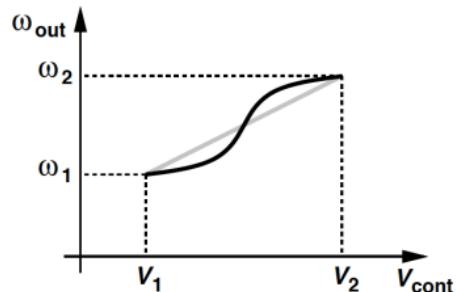
$$KVCO \geq \frac{\omega_2 - \omega_1}{V_2 - V_1}.$$

Parameters of VCO (II)

Tuning Linearity:

- Tuning characteristics of VCOs exhibit nonlinearity, i.e., their gain, KVCO, is not constant.
- Actual oscillator characteristics typically exhibit a high gain region in the middle of the range and a low gain at the two extremes.
- As shown on the right, compared to a linear characteristics (gray line), the actual behavior displays a maximum gain greater than that predicted by

$$K_{VCO} \geq \frac{\omega_2 - \omega_1}{V_2 - V_1}.$$



Parameters of VCO (III)

Output Amplitude:

- Desirable to achieve a large output oscillation amplitude □
Waveform less sensitive to noise.
- Trades with power dissipation, supply voltage, and tuning range.

Power Dissipation:

- Oscillators suffer from trade-offs between speed, power dissipation, and noise.

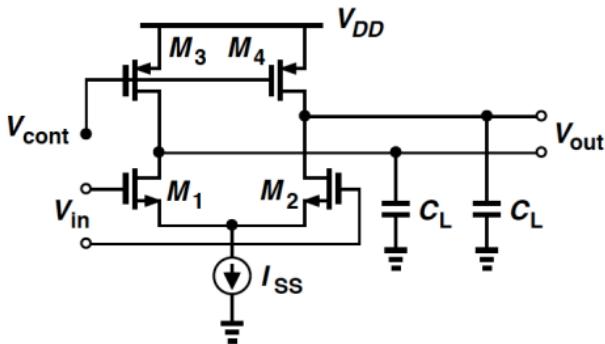
Supply and Common-Mode Rejection:

- Oscillators are quite sensitive to noise, especially when realized in single-ended form.

Output Signal Purity:

- Even with a constant V_{cont} , the output waveform of a VCO is not perfectly periodic.

Differential Pair with Variable Output τ



- M3 and M4 operate in the triode region, each acting as a variable resistor controlled by V_{cont} .
- If M3 and M4 remain in the deep triode region:

$$\begin{aligned} \square \quad \tau_1 &= R_{on3,4} C_L \\ &= \frac{C_L}{\mu_p C_{ox} \left(\frac{W}{L} \right)_{3,4} (V_{DD} - V_{cont} - |V_{THP}|)}. \end{aligned}$$

- Delay of the circuit is roughly proportional to τ_1 , yielding:

$$\begin{aligned} f_{osc} &\propto \frac{1}{T_D} \\ &\propto \frac{\mu_p C_{ox} \left(\frac{W}{L} \right)_{3,4} (V_{DD} - V_{cont} - |V_{THP}|)}{C_L}. \end{aligned}$$

Example 15.10

For given device dimensions and bias currents in previous circuit (Slide 56), determine the maximum allowable value of V_{cont} . What happens if M3 and M4 enter saturation?

Solution

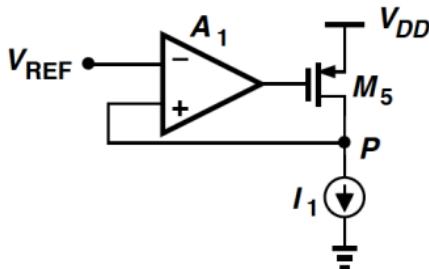
- Assume: M3 and M4 remain in the deep triode region if $|V_{DS3,4}| \leq 0.2 \times 2|V_{GS3,4} - V_{THP}|$.
- If each stage has complete switching \square maximum drain current of M3 and M4 is I_{SS} .
- To satisfy the above condition, we must have $I_{SS} \leq 0.4(V_{DD} - V_{cont}) \cdot \frac{I_{SS}}{\mu_p C_{ox} (\frac{W}{L})_{3,4} (V_{DD} - V_{cont} - |V_{THP}|)}$

\square

$$V_{cont} \leq V_{DD} - |V_{THP}| - \sqrt{\frac{I_{SS}}{0.4\mu_p C_{ox} (\frac{W}{L})_{3,4}}}.$$

- If V_{cont} exceeds ... level, M3 and M4 eventually enter saturation. Each stage then requires common-mode feedback to produce the output swings around a well-defined CM Level.

Replica Circuit for Stages of Ring Oscillator



(a)

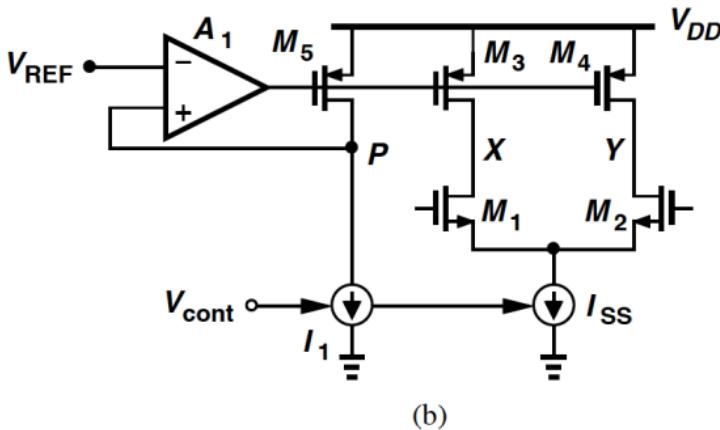
(a): M5 operates in the deep triode region and amplifier A1 applies negative feedback to the gate of M5.

If the loop gain is sufficiently large, the differential input voltage of A1 must be small $\square V_P \approx V_{REF}$ and $|V_{DS5}| \approx V_{DD} - V_{REF}$.

The feedback ensures a relatively constant drain-source voltage even if I_1 varies.

I_1 decreases \square A1 rises the gate voltage of M5 such that $R_{on5}I_1 \approx V_{DD} - V_{REF}$.

Replica Biasing to Define Voltage Swing



(b)

- (b): To “servo” the on-resistance of M_3 and M_4 to that of M_5 and vary the frequency by adjusting I_1 and I_{ss} simultaneously.
- If M_3 and M_4 are identical to M_5 and I_{ss} to I_1 \square V_X and V_Y vary from V_{DD} to $V_{DD} - V_{REF}$ as M_1 and M_2 steer the tail current to one side or the other.
- If process and temperature variations, say, decrease, I_1 and I_{ss} \square A_1 increases the on-resistance of M_3 - M_5 , forcing V_p and hence V_X and $V_Y = V_{REF}$.

Example 15.11

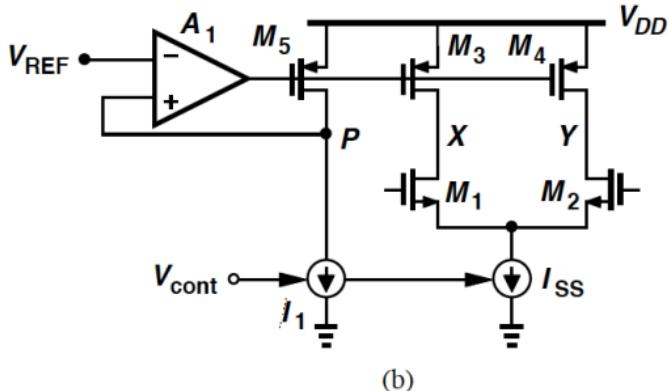
How does the oscillation frequency depend on ISS for a VCO incorporating the stage of previous topology (b) (Slide 59).

Solution

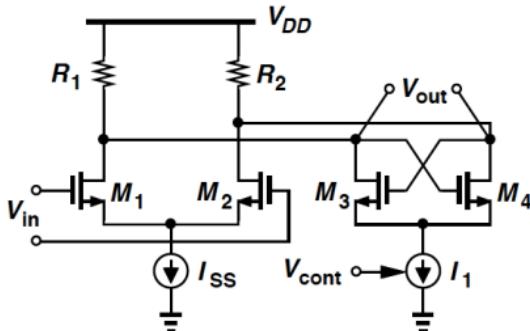
- $R_{on3,4}ISS \approx VDD - VREF$, we have $R_{on3,4} \approx (VDD - VREF)/ISS$ and hence:

$$f_{osc} \propto \frac{1}{R_{on3,4}C_L}$$
$$\propto \frac{I_{SS}}{(VDD - VREF)C_L}.$$

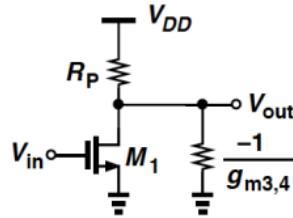
- Thus, the characteristic is relatively linear.



Differential Stage with Variable -R Load



(a)

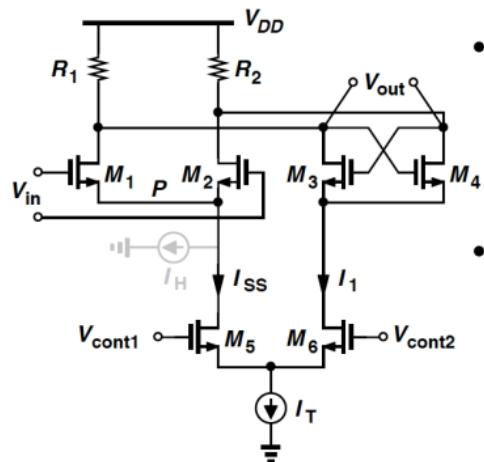


(b)

- (a): As I_1 increases,
 - the small-signal differential resistance $-2/gm_{3,4}$ becomes less negative.
 - from the half circuit (b), equivalent resistance $R_P||(-1/gm_{3,4}) = R_P/(1 - gm_{3,4}R_P)$ increases □ lower the frequency of oscillation.
- In (a), as I_1 varies, so do the currents steered by M_3 and M_4 to R_1 and R_2 □ the output voltage swing is not constant across the tuning range.

Differential Pair to Steer Current

- The below circuit is to employ a differential pair M5-M6 to steer I_T to M1-M2 or M3-M4, so $I_{SS} + I_1 = I_T$.
- I_T must flow through R_1 and R_2 . If M1-M4 experience complete switching in each cycle of oscillation □ I_T is steered to R_1 in half a period and to R_2 in the other half, giving a differential swing of $2RPI$.



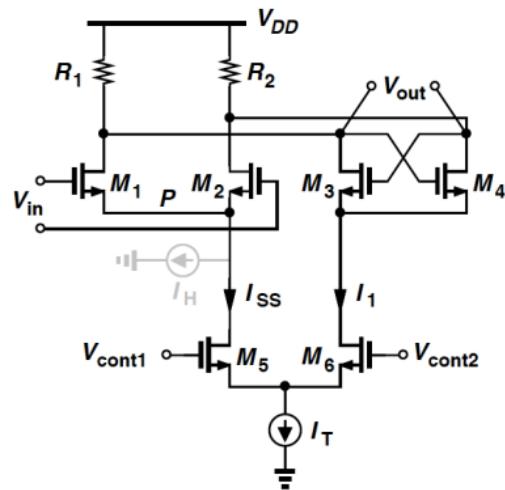
- V_{cont1} and V_{cont2} are differential control lines if they vary by equal and opposite amounts □ higher noise immunity.
- As V_{cont1} decreases and V_{cont2} increases □ cross-coupled pair exhibits a greater transconductance □ raise the time constant at the output nodes.

Example 15.12

Calculate the minimum value of I_H in previous circuit (Slide 62) to guarantee a low-frequency gain of 2 when all of I_T is steered to the cross-coupled pair.

Solution

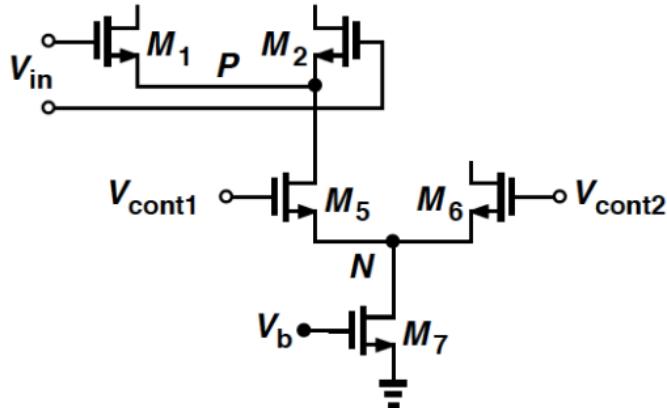
- The small-signal voltage gain of the circuit = $gm_{1,2}R_P/(1 - gm_{3,4}R_P)$.
- Assuming square-law devices, we have



$$Tr \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2} I_H} \frac{R_P}{1 - \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{3,4} I_T R_P}} \geq 2.$$

$$I_H \geq \frac{4 \left[1 - \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{3,4} I_T R_P} \right]^2}{\mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2} R_P^2}.$$

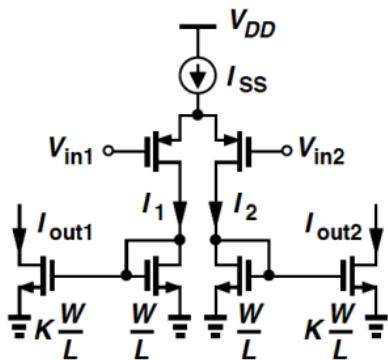
Headroom Calculation



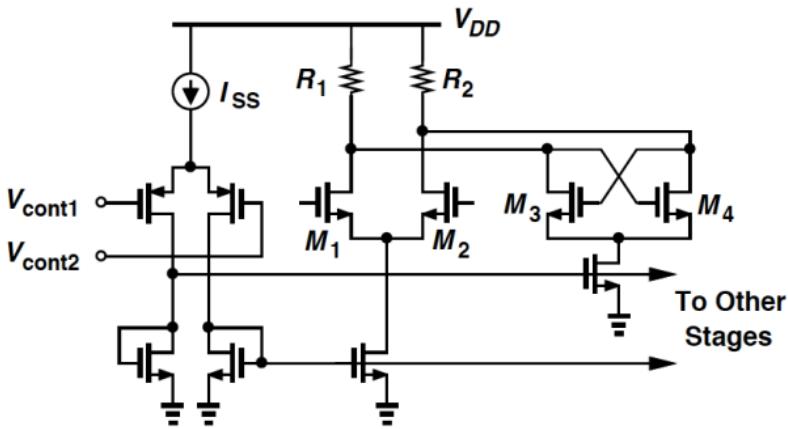
for M5 to remain in saturation, V_P must be sufficiently higher than V_N . When $V_{cont1} = V_{cont2}$, minimum allowable V_{DS} of M5 is equal to its equilibrium overdrive voltage.

- If V_{cont1} or V_{cont2} is allowed to vary above its equilibrium value by more than V_{TH} , M5 or M6 enters the triode region.
- To minimize the sensitivity, the transconductance of M5-M6 must be minimized.
- However, for a given tail current, $gm = 2ID/(VGS - VTH)$, indicating a large equilibrium overdrive for M5-M6 and a correspondingly higher value for the minimum required supply voltage.

Current Folding



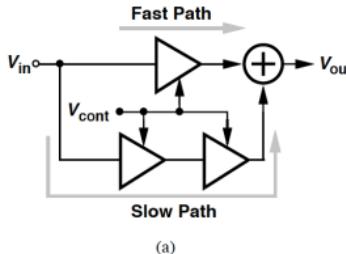
(a)



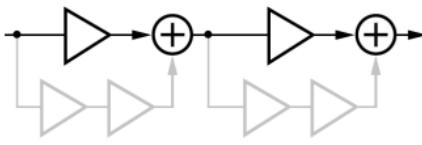
(b)

- (a): $I_1 + I_2 = I_{SS}$, $I_{out1} = KI_1$, $I_{out2} = KI_2$ \square $I_{out1} + I_{out2} = KI_{SS}$.
- (a) has a behavior similar to that of a differential pair.
- (b): Application of current folding to current steering. The circuit operates from a low supply voltage.
- However in (b), the devices in the control path contribute substantial noise \square modulate the oscillation frequency.

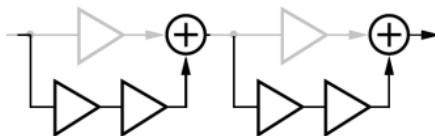
Interpolating Delay Stage (I)



(a)



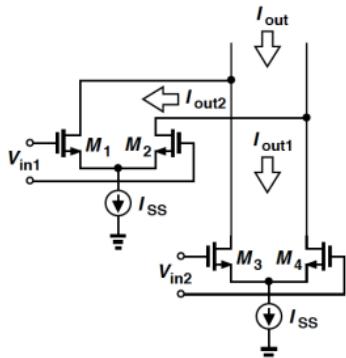
(b)



(c)

- (a): at one extreme of V_{cont} , only the fast path is on and the slow path is disabled, yielding the maximum oscillation frequency shown in (b).
- At the other extreme in (a), only the slow path is on and the fast path is off, providing the minimum oscillation frequency as shown in (c).
- If V_{cont} lies between the 2 extremes, each path is partially on and total delay = weighted sum of their delays.

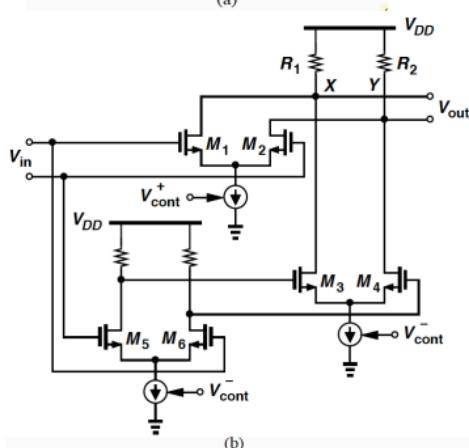
Interpolating Delay Stage (II)



(a)

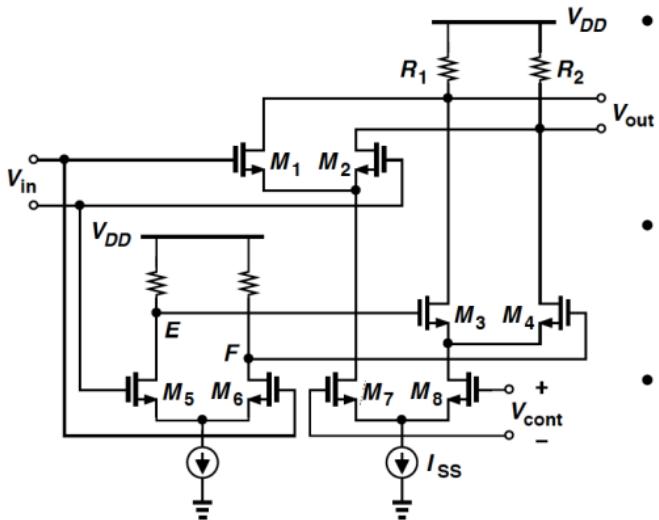
- (a): Simply shorting the outputs of two differential pairs performs the current addition.
- The overall interpolating stage therefore assumes the configuration (b).
- (b): Gain of each stage varied by the tail current to achieve interpolation.
- But it is desirable to maintain constant voltage swings.

The gain of the differential pair M_5-M_6 need not be varied because even if only the gain of M_3-M_4 drops to zero, the slow path is fully disabled.



(b)

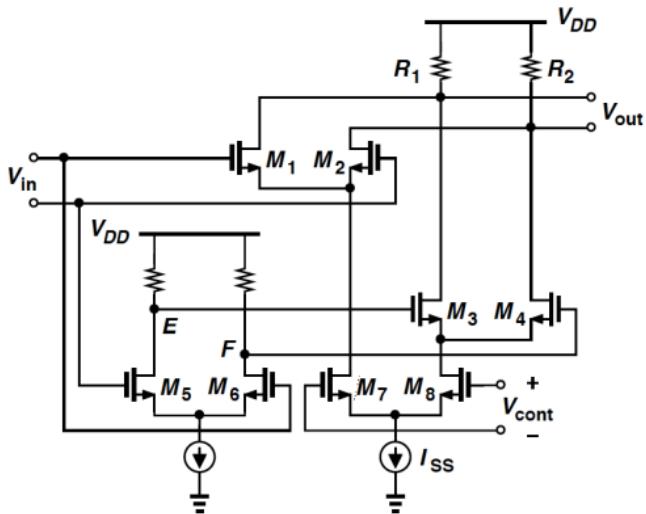
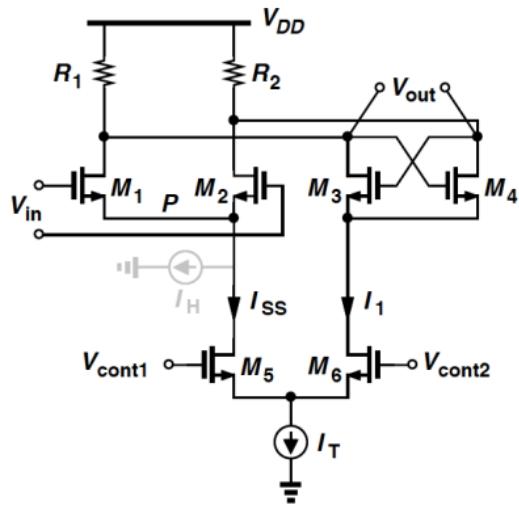
Interpolating Delay Stage with I Steering



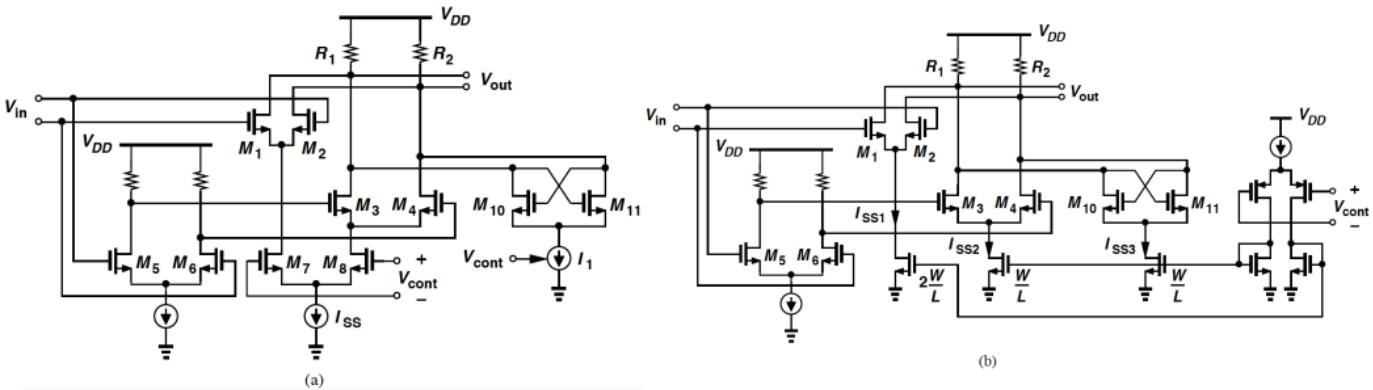
- The circuit employs the differential pair M_7 - M_8 to steer ISS between M_1 - M_2 and M_3 - M_4 .
- If V_{cont} is very negative $\square M_8$ off and only the fast path amplifies the input.
- If V_{cont} is very positive $\square M_7$ off and only the slow path is enabled.
- Since the slow path employs more stage than the fast path, the VCO achieves a tuning range of roughly two to one.

Example 15.13 (I)

Combine the two previously discussed tuning techniques, as shown in the following two circuit topologies, to achieve a wider tuning range.

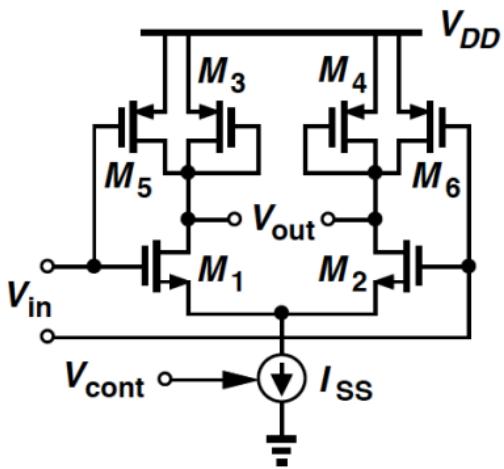


Example 15.13 (II)



- Interpolate the second tuning technique and add a cross-coupled pair to the output nodes, depicted in (a).
- However, to obtain constant voltage swings, the resulting configuration (b) steers the current to M_1 - M_2 to speed up the circuit and to M_3 - M_4 and M_{10} - M_{11} to slow down the circuit.
- The tail current source dimensions satisfy $ISS1 = ISS2 + ISS3$.

Wide-Range Tuning



- In applications where the frequency must be varied by orders of magnitude, the topology (left) can be used.
- Driven by the input, the additional PMOS transistors M5 and M6 pull each output node to VDD.
- These create a relatively constant output swing even with large variations in ISS.
- The oscillation frequency of a ring incorporating this stage can be varied by more than four orders of magnitude with less than a twofold variation in the amplitude.

Varactor

- Difficult to vary the value of monolithic inductors, so we simply change the tank capacitance to tune the oscillator.
- A reversed-biased pn junction can serve as a voltage-dependent capacitor, called a “varactor”:

$$C_{var} = \frac{C_0}{\left(1 + \frac{V_R}{\phi_B}\right)^m}$$

- C_0 : Zero-bias value.
- V_R : Reverse-bias voltage.
- ϕ_B : Built-in potential of the junction.
- m : Typically between 0.3 and 0.4.
- Important drawback of LC oscillators: At low supply voltages V_R has a very limited range \square a small range for C_{var} and hence for f_{osc} .

Example 15.14

Suppose in the equation of Cvar, $\phi B = 0.7$ V, $m = 0.35$, VR can vary from zero to 2 V. How much tuning range can be achieved?

$$C_{var} = \frac{C_0}{\left(1 + \frac{V_R}{\phi_B}\right)^m}$$

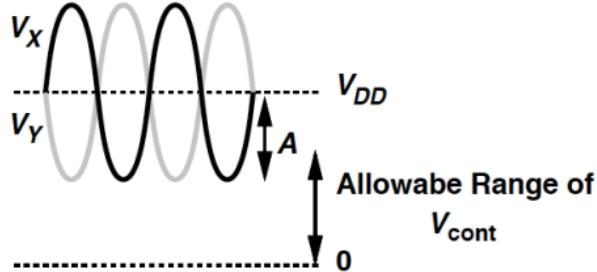
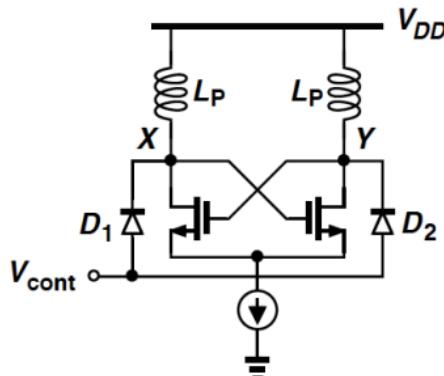
Solution

- For $V_R = 0$, $C_j = C_0$ and $f_{osc,min} = 1/(2\pi\sqrt{LC_0})$.
- For $V_R = 2$ V, $C_j \approx 0.62C_0$ and

$$f_{osc,max} = 1/(2\pi\sqrt{L \times 0.62C_0}) \approx 1.27 f_{osc,min}$$

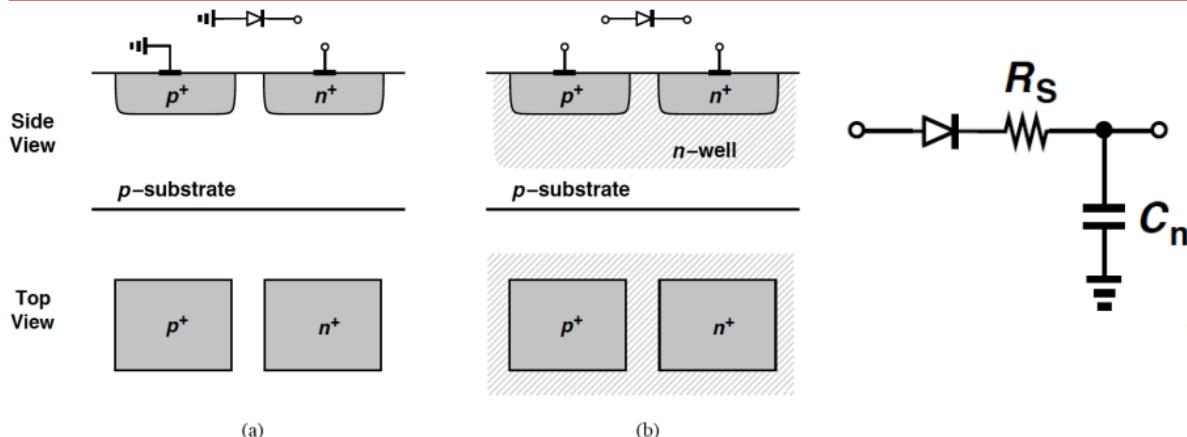
- Thus, the tuning range is approximately equal to 27%.

LC Oscillator Using Varactor Diodes



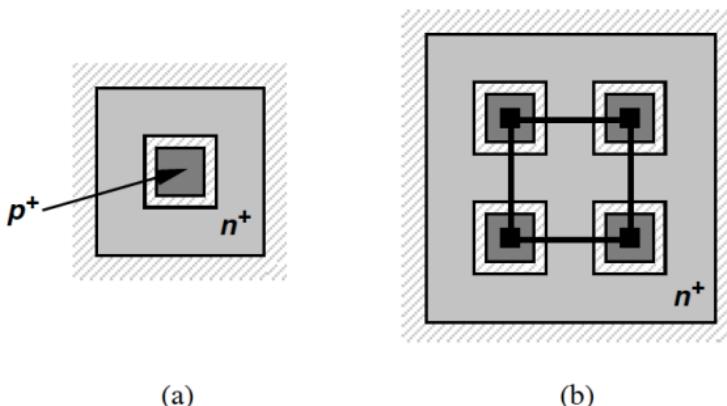
- To avoid forward-biasing D1 and D2 significantly, V_{cont} must not exceed V_X or V_Y by more than a few hundred mV.
- If the peak amplitude at each node = A , then $0 < V_{cont} < V_{DD} - A + 300 \text{ mV}$.
- The circuit suffers from a trade-off between output swing and tuning range.
- The capacitance of D1 and D2 varies with time due to typically large swings at X and Y.
- “Average” value of the capacitance is still a function of V_{cont} .

Diodes Realized in CMOS Technology



- 2 types of pn junctions: (a) the anode is inevitably grounded, (b) both terminals are floating.
- First drawback of (b): n-well material has a high resistivity create a resistance in series with the reverse-biased diode, lower Q factor of the capacitance.
- Another drawback of (b): n-well displays substantial capacitance to the substrate, C_n (right) contribute a constant capacitance to the tank, limit the tuning range.

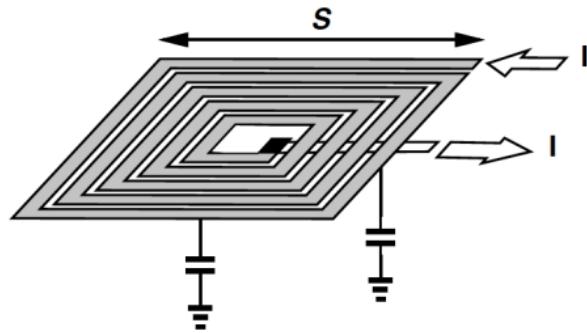
Reduction of Series Resistance



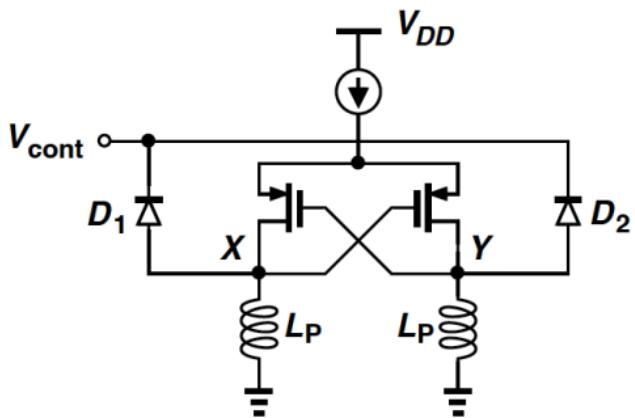
- (a): Used to decrease the series resistance of the second pn junction type (Slide 78).
- In (a), p^+ region surrounded by an n^+ ring \square the displacement current flowing through the junction capacitance see a low resistance in all four directions.
- Many of these units of (a) can be placed in parallel, as in (b).

Tuning in LC Oscillators

- Examine unwanted capacitances in the circuit (Slide 74). We identify three such capacitances:
 - capacitance between n-well and substrate associated with D1 & D2;
 - CGD, 2CGD, and CDB;
 - parasitic capacitance of the inductor itself.
- Monolithic inductors typically implemented as metal spiral structure (right)
 - relatively large dimensions ($S \approx 100\text{-}200 \mu\text{m}$).

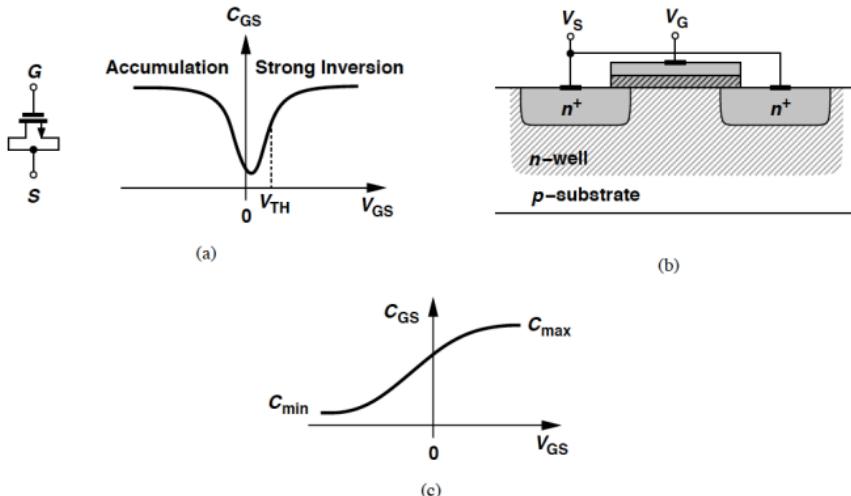


Use of PMOS to Eliminate n-well Capacitance



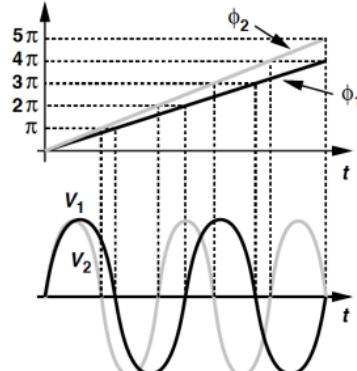
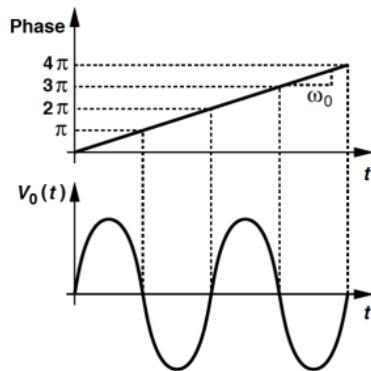
- Desirable to connect the anode of the diodes to X & Y \square eliminate the parasitic n-well capacitances from the tank.
- Here, the cross-coupled pair incorporates PMOS devices, providing swings around the ground potential.
- Use of PMOS devices also leads to less flicker noise appearing around the oscillation frequency.

MOS Varactor



- (a): Recall CGS of MOSFETs varies with VGS.
- (b): An NMOS transistor can be placed inside an n-well, forming an “accumulation-mode” varactor.
- (c) shows how the capacitance of structure (b) varies monotonically with VGS.

Phase for Signal



Consider $V_0(t) = V_m \sin \omega_0 t$, and the phase varies linearly with time at a slope of ω_0 (left).

Every time $\omega_0 t$ crosses an integer multiple of π , $V_0(t)$ crosses 0.

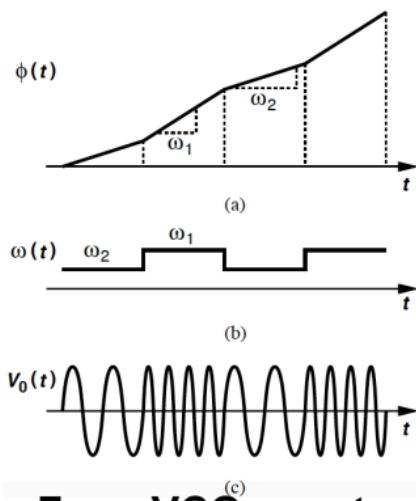
Now consider $V_1(t) = V_m \sin[\phi_1(t)]$ and $V_2(t) = V_m \sin[\phi_2(t)]$, where $\phi_1(t) = \omega_1 t$, $\phi_2(t) = \omega_2 t$, and $\omega_1 < \omega_2$ (right).

$\phi_2(t)$ crosses integer multiples of π faster than $\phi_1(t)$ does, yielding faster variations in $V_2(t)$ □ $V_2(t)$ accumulates phase faster.

The frequency can be defined as $\omega = \frac{d\phi}{dt}$.

Example 15.15

(a) shows the phase of a sinusoidal waveform with constant amplitude as a function of time. Plot the waveform.



Solution

- Taking the time derivative of $\phi(t)$, we obtain (b).
- The frequency periodically toggles between ω_1 and ω_2 , yielding the waveform in (c).
- If the frequency of a waveform is known as a function of time, the phase can be computed as

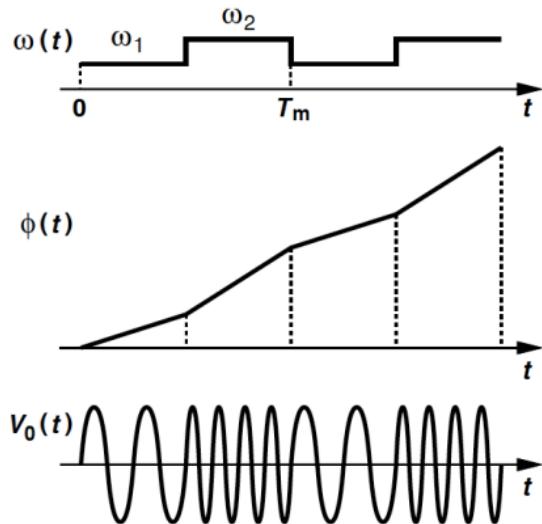
$$\phi = \int \omega dt + \phi_0.$$

- For a VCO, $\omega_{out} = \omega_0 + K_{VCO}V_{cont}$, we have:

$$\begin{aligned} V_{out}(t) &= V_m \cos\left(\int \omega_{out} dt + \phi_0\right) \\ &= V_m \cos\left(\omega_0 t + K_{VCO} \int V_{cont} dt + \phi_0\right). \end{aligned}$$

Example 15.16

The control line of a VCO senses a rectangular signal toggling between V_1 and V_2 at a period T_m . Plot the frequency, phase, and output waveform as a function of time.



Solution

- $\omega_{\text{out}} = \omega_0 + K_{\text{VCO}} V_{\text{cont}}$ □ the output frequency toggles between $\omega_1 = \omega_0 + K_{\text{VCO}} V_1$ and $\omega_2 = \omega_0 + K_{\text{VCO}} V_2$, as shown in the $V_0(t)$ waveform.
- The phase is equal to the time integral of this result, rising linearly with time at a slope of ω_1 for half the input period and ω_2 for the other half.
- A VCO can operate as a frequency modulator.

Example 15.17

A VCO senses a small sinusoidal control voltage $V_{cont} = V_m \cos \omega_m t$. Determine the output waveform and its spectrum.

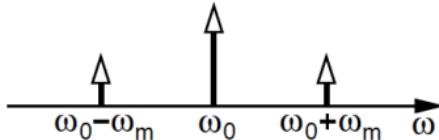
The output is expressed as

$$\begin{aligned}V_{out}(t) &= V_0 \cos(\omega_0 t + K_{VCO} \int V_{cont} dt) = V_0 \cos(\omega_0 t + K_{VCO} \frac{V_m}{\omega_m} \sin \omega_m t) \\&= V_0 \cos \omega_0 t \cos(K_{VCO} \frac{V_m}{\omega_m} \sin \omega_m t) \\&\quad - V_0 \sin \omega_0 t \sin(K_{VCO} \frac{V_m}{\omega_m} \sin \omega_m t).\end{aligned}$$

If V_m is small enough that $K_{VCO} V_m / \omega_m$...

$$\begin{aligned}V_{out}(t) &\approx V_0 \cos \omega_0 t - V_0 (\sin \omega_0 t) (K_{VCO} \frac{V_m}{\omega_m} \sin \omega_m t) \\&= V_0 \cos \omega_0 t - \frac{K_{VCO} V_m V_0}{2\omega_m} [\cos(\omega_0 - \omega_m)t - \cos(\omega_0 + \omega_m)t].\end{aligned}$$

The output consists of three sinusoids having frequencies of ω_0 , $\omega_0 - \omega_m$ and $\omega_0 + \omega_m$. The spectrum is:



Expression of Phase

Explain why this is incorrect: The output frequency of a VCO is $\omega_0 + KVCOV_{cont}$, then the output waveform can be written as $V_m \cos[(\omega_0 + KVCOV_{cont})t]$.

Compute the frequency as derivative of the phase:

$$\begin{aligned}\omega &= \frac{d}{dt}[(\omega_0 + KVCOV_{cont})t] \\ &= KVCO \frac{dV_{cont}}{dt} t + \omega_0 + KVCOV_{cont}.\end{aligned}$$

The first term in the above expression vanishes only if $dV_{cont}/dt = 0$.

- In general case, the phase cannot be written as product of time & frequency.

Output Harmonics

- In practice, output of the VCO may contain significant harmonics, even approaching a rectangular waveform.
- We expect $V_{out}(t)$ expressed as a Fourier series:

$$V_{out}(t) = V_1 \cos(\omega_0 t + \phi_1) + V_2 \cos(2\omega_0 t + \phi_2) + \dots$$

- If V_{cont} varies by ΔV □ frequency of the first harmonic varies by $K_{VCO}\Delta V$, frequency of the second harmonic by $2K_{VCO}\Delta V$, etc.

$$V_{out}(t) = V_1 \cos(\omega_0 t + K_{VCO} \int V_{cont} dt + \theta_1) + V_2 \cos(2\omega_0 t + 2K_{VCO} \int V_{cont} dt + \theta_2) + \dots$$

- Often limit calculations to the 1st harmonic.