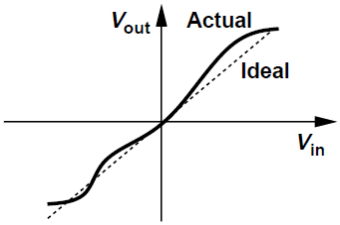
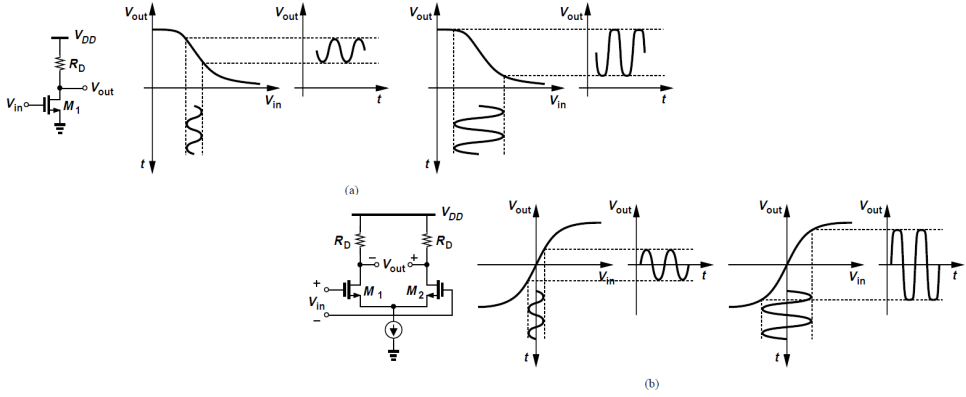
Chapter 14: Nonlinearity and Mismatch

14.1 Nonlinearity
14.2 Mismatch

Nonlinearity: General Considerations



- Nonlinear characteristic deviates from a straight line as the input swing increases
- E.g., Common-source stage or differential pair

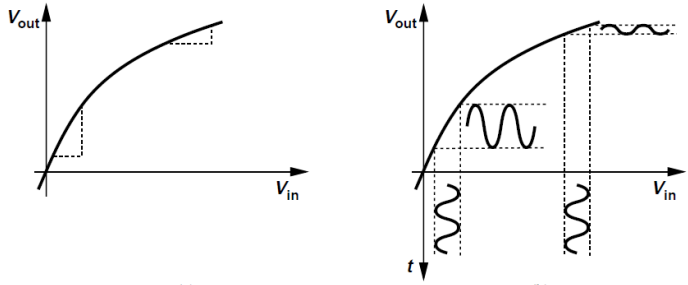


Nonlinearity: General Considerations

- **Nonlinear input/output characteristic can be approximated by a polynomial in the range of interest**

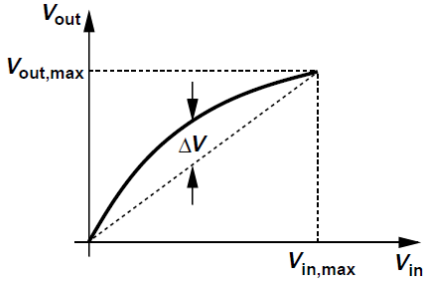
$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots.$$

- **For small *x*, *y(t)* ≈ *α1x*, indicating that *α1* is the small-signal gain in the vicinity of *x* ≈ *0***



Nonlinearity: General Considerations

- Nonlinearity can be quantified by specifying maximum deviation of characteristic from an ideal one



- For voltage range of interest [0, *Vin,max*], pass straight line through end points of actual characteristic and obtain maximum deviation ΔV
- Normalize to maximum output swing *Vout,max*
- 1% nonlinearity for an input range of 1 V means

$$(\Delta V / V_{out,max} = 0.01)$$

Nonlinearity: General Considerations

- **Nonlinearity can also be characterized by applying a sinusoid at input and measuring harmonic content of output**
- **If** $x(t) = A\cos\omega t$, **then**

$$\begin{aligned} y(t) &= \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3\cos^3\omega t + \cdots \\ &= \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}[1+\cos(2\omega t)] + \frac{\alpha_3 A^3}{4}[3\cos\omega t + \cos(3\omega t)] + \cdots \end{aligned}$$

- **Magnitude of *n*th harmonic grows roughly in proportion to *n*th power of input amplitude**
- **Quantified by summing the power of all harmonics except fundamental and normalizing to power of fundamental, metric called as "total harmonic distortion" (THD)**
- **For a third-order nonlinearity,**

$$THD = \frac{(\alpha_2 A^2/2)^2 + (\alpha_3 A^3/4)^2}{(\alpha_1 A + 3\alpha_3 A^3/4)^2}$$

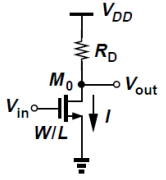
Nonlinearity of Differential Circuits

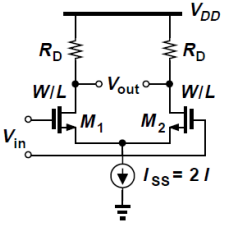
- Differential circuits exhibit “odd-symmetric” characteristic
- Even-order terms *α2j* in polynomial must be zero:

$$y(t) = \alpha_1 x(t) + \alpha_3 x^3(t) + \alpha_5 x^5(t) + \cdots$$

- Differential circuit driven by a differential signal produces no even harmonics
- Consider two amplifiers providing equal small-signal voltage gain of

$$\begin{aligned} |A_v| &\approx g_m R_D \\ &= \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) R_D \end{aligned}$$





Nonlinearity of Differential Circuits

- If an input $V_m \cos\omega t$ is applied to each circuit, for common-source stage,

$$I_{D0} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH} + V_m \cos\omega t)^2$$

$$= I + \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_m \cos\omega t + \frac{1}{4}\mu_n C_{ox}\frac{W}{L}V_m^2[1 + \cos(2\omega t)]$$

- Amplitude of second harmonic normalized to fundamental is

$$\frac{A_{HD2}}{A_F} = \frac{V_m}{4(V_{GS} - V_{TH})}$$

- For the differential pair, it can be shown that

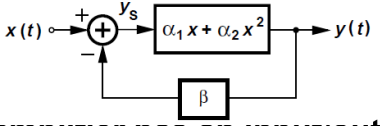
$$I_{D1} - I_{D2} = g_m\left[V_m - \frac{3V_m^3}{32(V_{GS} - V_{TH})^2}\right]\cos\omega t - g_m\frac{V_m^3\cos(3\omega t)}{32(V_{GS} - V_{TH})^2}.$$

- If $V_m \ll 3V_m^3/[8(V_{GS} - V_{TH})^2]$

- Differential pair ex $\frac{A_{HD3}}{A_F} \approx \frac{V_m^2}{32(V_{GS} - V_{TH})^2}$ distortion for same gain and output swing, at the cost of higher power

Effect of Negative Feedback on Nonlinearity

- Expected that negative feedback would yield higher linearity for a closed-loop system
- Consider a "mildly nonlinear" system below



- Assume core amplifier has an input/output characteristic $y \approx \alpha_1 x + \alpha_2 x^2$
- Apply a sinusoidal input $x(t) = V_m \cos \omega t$ postulating that output contains a fundamental and second harmonic approximated as $y \approx a \cos \omega t + b \cos 2\omega t$
- Through simple analysis, we can get

$$a = (\alpha_1 - \alpha_2 \beta b)(V_m - \beta a)$$

$$b = -\alpha_1 \beta b + \frac{\alpha_2 (V_m - \beta a)^2}{2}$$

Effect of Negative Feedback on Nonlinearity

- Small nonlinearity means *α2* and *b* are small quantities, so that $a \approx \alpha_1(V_m - \beta a)$ and hence

$$a = \frac{\alpha_1}{1 + \beta\alpha_1} V_m$$

- b can be found as

$$b = \frac{\alpha_2 V_m^2}{2} \frac{1}{(1 + \beta\alpha_1)^3}$$

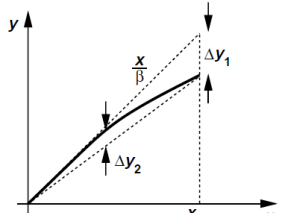
- Normalize amplitude of second harmonic to that of fundamental

$$\frac{b}{a} = \frac{\alpha_2 V_m}{2} \frac{1}{\alpha_1} \frac{1}{(1 + \beta\alpha_1)^2}$$

- Without feedback, this ratio would be $\alpha_2 V_m/(2\alpha_1)$
- Negative feedback reduces relative second harmonic by a factor of $(1 + \beta\alpha_1)^2$ and gain by $1 + \beta\alpha_1$

Effect of Negative Feedback on Nonlinearity

- Feedforward amplifier in a feedback system suffers from gain error
- For a feedforward gain *A0* and feedback factor *β*, relative gain error is approximately *1/(βA0)*
- Possible to derive a relationship between gain error and maximum nonlinearity of overall feedback circuit



- In above fig., nonlinearity is always less than gain error Δy_2
- Choose Δy_1 high open-loop amplifier gain so that to guarantee $\Delta y_2 < \epsilon$

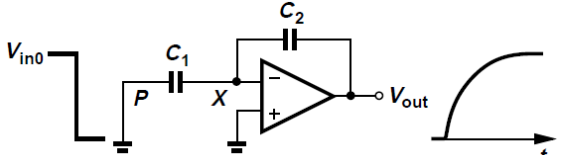
$$\Delta y_1 < \epsilon$$

Capacitor Nonlinearity

- For a linear capacitor, $Q = CV$ while for a voltage-dependent capacitor $dQ = C\,dV$
- Total charge on a capacitor sustaining a voltage *V1* is

$$Q(V_1) = \int_0^{V_1} C\,dV.$$

- Charge depends on "history" of voltage rather than instantaneous value
- Express each capacitor as $C = C_0(1 + \alpha_1 V + \alpha_2 V^2 + \cdots)$
- Consider noninverting amplifier below



- At the start of amplification mode, *C1* has a voltage of *Vin0* and *C2* a voltage of zero

Capacitor Nonlinearity

- Assuming $C_1 \approx MC_0(1+\alpha_1 V)$ where *M* is the nominal closed-loop gain, charge across *C1* is

$$\begin{aligned} Q_1 &= \int_0^{V_{in0}} C_1\, dV \\ &= \int_0^{V_{in0}} MC_0(1+\alpha_1 V)\, dV \\ &= MC_0 V_{in0} + MC_0 \frac{\alpha_1}{2} V^2. \end{aligned}$$

- Similarly, if $C_2 \approx C_0(1+\alpha_1 V)$, charge across it at the end of amplification mode is

$$\begin{aligned} Q_2 &= \int_0^{V_{out}} C_2\, dV \\ &= C_0 V_{out} + C_0 \frac{\alpha_1}{2} V_{out}^2 \end{aligned}$$

- Equating *Q1* and *Q2* and solving for *Vout*,

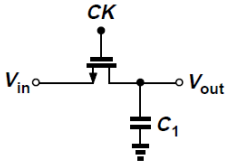
$$V_{out} = \frac{1}{\alpha_1}\left(-1 + \sqrt{1 + M\alpha_1^2 V_{in0}^2 + 2M\alpha_1 V_{in0}}\right)$$

- For $\alpha_1 \ll 1$ and
- Second term represents nonlinearity due to capacitor voltage-dependence

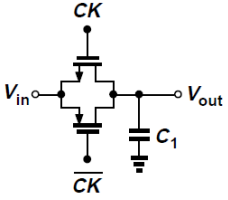
$$V_{out} \approx MV_{in0} + (1-M)\frac{M\alpha_1}{2} V_{in0}^2$$

Nonlinearity in Sampling Circuits

- On-resistance of MOS switches varies with input and output levels
- NMOS switch in Fig. (a) exhibits rising resistance as *Vin* and *Vout* increase
- Complementary topology of Fig. (b) displays varying equivalent resistance as *Vin* and *Vout* go from 0 to *VDD*
- *Ron* reaches a peak here due to dependence of mobility on the vertical field in the channel



(a)



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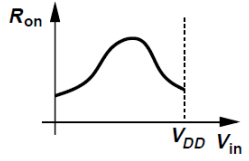
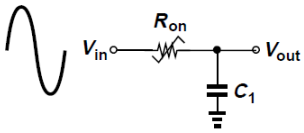


Nonlinearity in Sampling Circuits

- We apply a large sinusoid to the input, $V_{in} = V_0 \cos \omega_0 t + V_0$ where *V0 = VDD/2* and seek harmonics at the output



- First assume resistance is linear and write output as

$$V_{out}(t) = \frac{V_0}{\sqrt{R_{on}^2 C_1^2 \omega_0^2 + 1}} \cos[\omega_0 t - \tan^{-1}(R_{on} C_1 \omega_0)] + V_0$$

- In practice, bandwidth must be large enough to negligibly attenuate the signal, i.e., $R_{on} C_1 \omega_0 \ll 1$ so that

$$V_{out}(t) \approx V_0 \cos(\omega_0 t - R_{on} C_1 \omega_0) + V_0$$

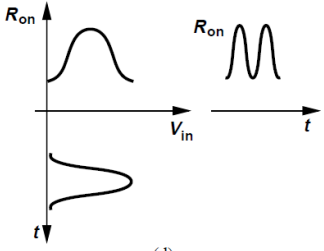
- Assume this expression holds for the nonlinear circuit if *Ron* is represented properly
- Phase shift from input to output varies as *Vin* and *Vout* vary, creating distortion

Nonlinearity in Sampling Circuits

- **For a periodic input, *Ron* also varies periodically and can be approximated by a Fourier series**

$$R_{on}(t) = R_0 + R_1 \cos\omega_0 t + R_2 \cos(2\omega_0 t) + \cdots$$

- **For a roughly symmetric behavior of *Ron*, the time-domain behavior below is observed where *Ron* varies at twice the input frequency**



(d)

- **Thus,**

$$V_{out}(t) \approx V_0 \cos[\omega_0 t - R_0 C_1 \omega_0 - R_1 C_1 \omega_0 \cos\omega_0 t - R_2 C_1 \omega_0 \cos(2\omega_0 t) - \cdots] + V_0.$$

Nonlinearity in Sampling Circuits

- **For cosine terms with arguments much less than 1 rad,**

$$V_{out}(t) \approx V_0 \cos(\omega_0 t - R_0 C_1 \omega_0) + [R_1 C_1 \omega_0 \cos\omega_0 t + R_2 C_1 \omega_0 \cos(2\omega_0 t) + \cdots] V_0 \sin(\omega_0 t - R_0 C_1 \omega_0) + V_0$$

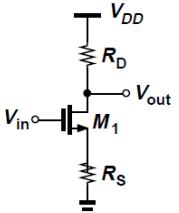
- **If only first two harmonics are retained, then**

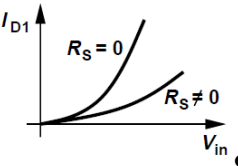
$$\text{THD} = \frac{R_1^2 + R_2^2}{4} C_1^2 \omega_0^2$$

- **In a differential sampling switch, even-order harmonics are suppressed**

Linearization Techniques

- Principle behind linearization is to reduce dependence of circuit's gain on input level
- Make gain relatively independent of bias currents
- Simplest method is by means of a linear resistor





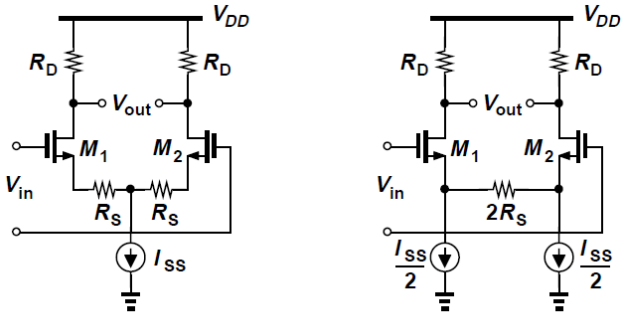
- Overall transconductance of degenerated CS stage is

$$G_m = \frac{g_m}{1 + g_m R_S}$$

- For large $g_m R_S$, the gain is $1/R_S$, an input-independent value

Linearization Techniques

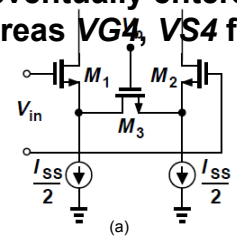
- Differential pair can be degenerated as shown in Figs. (a) and (b)



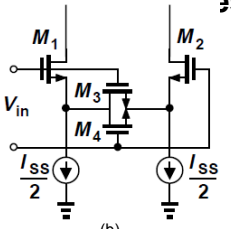
- In Fig. (a), degeneration resistors consume headroom of *ISSRS/2*
- Circuit of Fig. (b) does not have this issue but suffers from higher noise and offset voltage

Linearization Techniques

- Degeneration resistor can be replaced by a MOSFET operating in deep triode region [Fig. (a)]
- For large input swings, *M3* may not remain in deep triode
- *Vb* must track *Vin,CM* so that *Ron* is defined accurately
- Fig. (b) shows more a practical solution where *M3* and M4 are in deep triode for *Vin = 0*
- As *VG1 > VG2*, *M3* stays in triode since *VD3 = VG3 – VGS1*
- *M4* eventually enters saturation since *VD4* rises whereas *VG4*, *VS4* fall



(a)



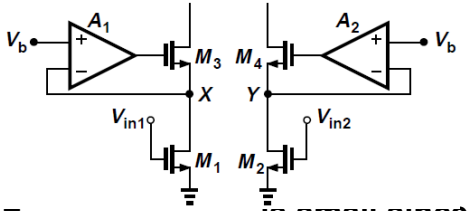
(b)

Linearization Techniques

- **MOSFET operating in triode region can provide a linear *ID/VDS* characteristic if *VDS* is held constant**

$$I_D = (1/2)\mu C_{ox}(W/L)[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]$$

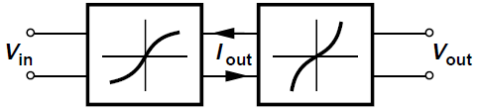
- **This technique employs amplifiers *A1* and *A2* with cascode devices *M3* and *M4* to force *VX* and *VY* to be equal to *Vb* for varying input levels**



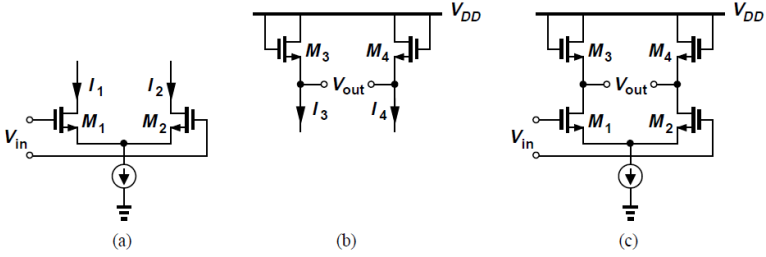
- ***gm1* = *gm2* = $\mu_n C_{ox}(W/L)V_{DS}$ is small since *VDS* must be low to ensure operation remain in triode region**
- ***Vin,CM* must be tightly controlled to track *Vb* to define *ID1* and *ID2***

Linearization Techniques

- Another approach to linearization: “post-correction”
- View the amplifier as a cascade of voltage-to-current (V/I) converter and a current-to-voltage (I/V) converter

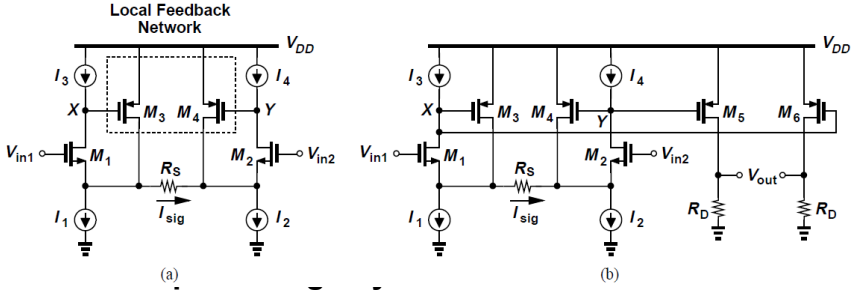


- If the V/I converter can be described as $I_{out} = f(V_{in})$ and the I/V converter as $V_{out} = f^{-1}(I_{in})$, then V_{out} is a linear function of *Vin* , for e.g. Figs. (a), (b), (c)



Linearization Techniques

- Possible to linearize differential pair further by adding local feedback



- return a proportional current to the sources of *M1* and *M2*
- Assume circuit is symmetric and *I1* = … = *I4*
- Ignoring CLM and body-effect, *ID1* = *I3* and *ID2* = *I4* regardless of the input signal

Linearization Techniques

- **Input transistors maintain a constant *VGS* as *Vin* = *Vin1* – *Vin2* varies**
- **Current through *RS* (*Isig*) must be provided only by *M3* and *M4*, we have**

$$\begin{aligned} V_{in} &= V_{GS1} + I_{sig}R_S - V_{GS2} \\ &= I_{sig}R_S \end{aligned}$$

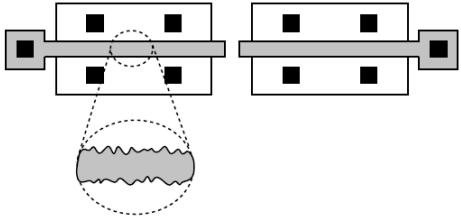
- **Output voltage of this topology can be found to be**

$$V_{out} = \frac{2R_D}{R_S}V_{in}$$

- **Large number of devices in signal path produce significant noise**
- **Dependence of *rO* upon *VDS* in short-channel devices introduces some nonlinearity**

Mismatch

- Nominally-identical devices suffer from finite mismatch due to uncertainties in manufacturing process
- Gate dimensions of MOSFETs suffer from random, microscopic variations and introduce mismatches between two transistors identically laid out
- MOS devices exhibit *VTH* mismatches since *VTH* is a function of doping levels in the channel and gate which vary randomly



Mismatch

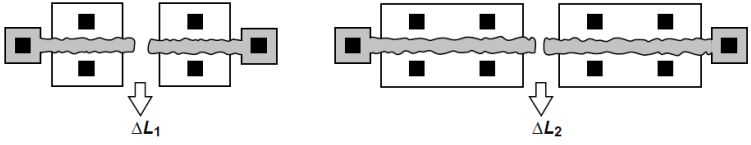
- Study of mismatch consists of two steps:
- Identify and formulate the mechanisms leading to mismatch between devices
- Analyze the effect of device mismatches upon the performance of circuits
- For a MOSFET in saturation,

$$I_D = (1/2)\mu C_{ox}(W/L)(V_{GS} - V_{TH})^2$$

- Mismatches between μ, C_{ox}, W, L, and V_{TH} result in mismatches between I_D's (for a given V_{GS}) or V_{GS}'s (for a given I_D) of two nominally-identical transistors
- Intuitively, as W and L increase, their relative mismatches $\Delta W/W$ and $\Delta L/L$, i.e., larger devices exhibit smaller mismatches

Mismatch

- All mismatches decrease as the area, WL increases
- As WL increases, random variations experience greater "averaging", falling in magnitude



- For the above case, $\Delta L2 < \Delta L1$ because if the device is viewed as many smaller parallel transistors, each with width W0, equivalent length is

$$L_{eq} \approx (L_1 + L_2 + \cdots + L_n)/n$$

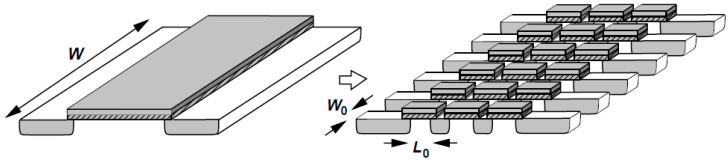
- Overall variation is given by

$$\Delta L_{eq} \approx (\Delta L_1^2 + \Delta L_2^2 + \cdots + \Delta L_n^2)^{1/2}/n = \frac{(n\Delta L_0^2)^{1/2}}{n} = \frac{\Delta L_0}{\sqrt{n}}$$

- If ΔL_0 is the variation of a transistor with width *W0*

Mismatch

- ***μCox*** **and** ***VTH*** **suffer from less mismatch if device area increases**



- **A large transistor can be decomposed into a series and parallel combination of small unit transistors with dimensions** ***W0*** **and** ***L0*****, each exhibiting** ***(μCox)j*** **and** ***VTHj***
- **These experience greater averaging as number of unit transistors increases**

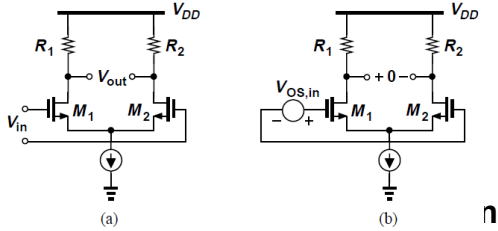
$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}}$$

$$\Delta\left(\mu C_{OX}\frac{W}{L}\right) = \frac{A_K}{\sqrt{WL}},$$

- ***AVTH*** **and** ***AK*** **are proportionality factors**

Effect of Mismatch

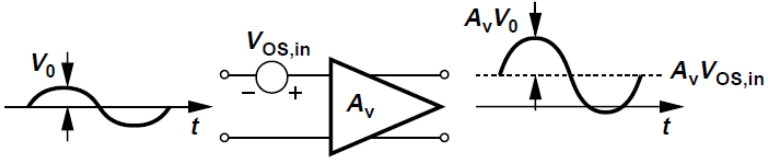
- Mismatches lead to three distinct phenomena:
- DC offsets
- Finite even-order distortion
- Lower common-mode rejection
- **DC Offsets**:



- In different[illegible]nd perfect symmetry, *Vout = 0* but with mismatches *Vout ≠ 0*
- Circuit suffers from a "dc offset" equal to the observed value of *Vout* when *Vin* is set to zero

Effect of Mismatch

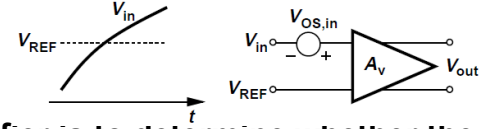
- More meaningful to specify input-referred offset voltage, defined as the input level that forces the output to go to zero
- Note that $|V_{OS,in}| = |V_{OS,out}|/A_v$
- If a differential pair is to amplify a small input voltage, output contains amplified replicas of both the signal and the offset



- In a cascade of direct-coupled amplifiers, the dc offset may experience so much gain that it drives the latter stage into nonlinear operation

Effect of Mismatch

- DC offset also affects the precision with which signals can be measured



- If an amplifier is to determine whether the input signal is greater or less than a reference, *VREF*, then the input-referred offset imposes a lower bound on the minimum *Vin – VREF* that can detected reliably
- Input-referred offset voltage of a differential pair can be found as

$$V_{OS,in} = \frac{V_{GS} - V_{TH}}{2}\left[\frac{\Delta R_D}{R_D} + \frac{\Delta(W/L)}{(W/L)}\right] - \Delta V_{TH}$$

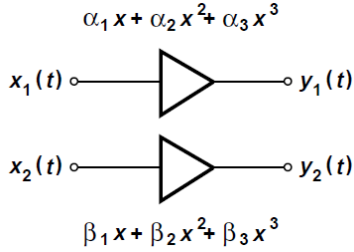
- More accu

$$V_{OS,in}^2 = \left(\frac{V_{GS} - V_{TH}}{2}\right)^2 \left\{\left(\frac{\Delta R_D}{R_D}\right)^2 + \left[\frac{\Delta(W/L)}{(W/L)}\right]^2\right\} + \Delta V_{TH}^2$$

Effect of Mismatch

- **Even-Order Distortion:**
- **Mismatches introduce finite even-order nonlinearity in differential circuits**
- **If the two signal paths in a differential circuit are represented by** $y_1 \approx \alpha_1 x_1 + \alpha_2 x_1^2 + \alpha_3 x_1^3$ **and** $y_2 \approx \beta_1 x_2 + \beta_2 x_2^2 + \beta_3 x_2^3$ **the differential output is given by** $y_1 - y_2 = (\alpha_1 x_1 - \beta_2 x_2) + (\alpha_2 x_1^2 - \beta_2 x_2^2) + (\alpha_3 x_1^3 - \beta_3 x_2^3)$
- **For** $x_1 = -x_2$**, this reduces to**

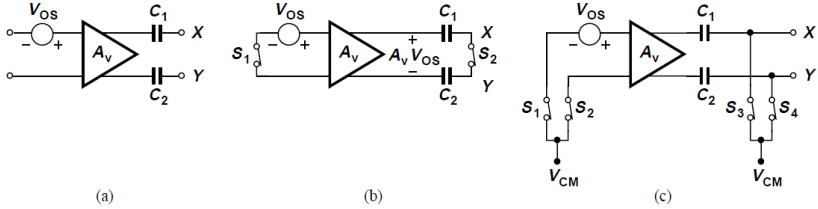
$$y_1 - y_2 = (\alpha_1 + \beta_1)x_1 + (\alpha_2 - \beta_2)x_1^2 + (\alpha_3 + \beta_3)x_1^3$$



Effect of Mismatch

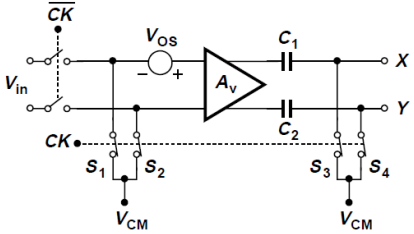
- If $x_1(t) = A\cos\omega t$, the second harmonic has an amplitude of $(\alpha_2 - \beta_2)A^2/2$, i.e., proportional to the mismatch between second-order coefficients of the input/output characteristic
- At high frequencies, signals experience considerable phase shift, even-order distortion may arise from phase mismatch
- In circuits dissipating a high power, thermal gradients across the chip may create asymmetries

Offset Cancellation Techniques



- **Differential amplifier with an input-referred offset is followed by two series capacitors [Fig. (a)]**
- **As shown in Fig. (b), inputs are shorted together, driving amplifier output to *Vout* = *AvVOS***
- **Assume *VX* and *VY* are shorted during this period as well**
- ***AvVOS* is stored across *C1* and *C2*, zero differential input results in zero differential output**
- **After *S1* and *S2* turn off, there is zero offset voltage**
- **Proper CM voltage needed at input and output**

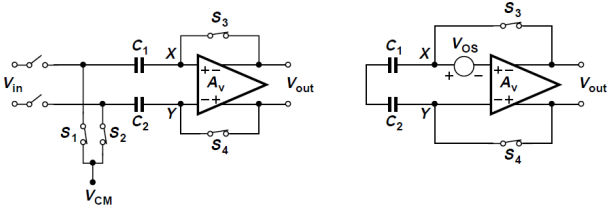
Offset Cancellation Techniques



- This technique "measures" the offset by setting the differential input to zero and stores the result on capacitors in series with the output
- Requires a dedicated offset-cancellation period during which actual input is disabled
- Called "output offset storage", this technique reduces overall mismatch if *S3-S4* do not have charge injection mismatch
- Large *Av* may saturate output, hence *Av* of roughly 10 is used

Offset Cancellation Techniques

- In application requiring high voltage gain, topology of Fig. (a) may be used
- Called "input offset storage", this incorporates two series capacitors at the input and places amplifier in unity-gain feedback loop during offset cancellation



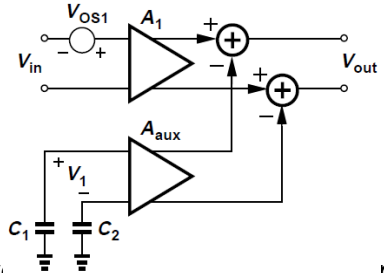
- From Fig. (b),

$$V_{out} = \frac{A_v}{1 + A_v} V_{OS}$$

- $V_{OS,in}$ equal V_{OS} $\approx V_{OS}$. natch perfectly

Offset Cancellation Techniques

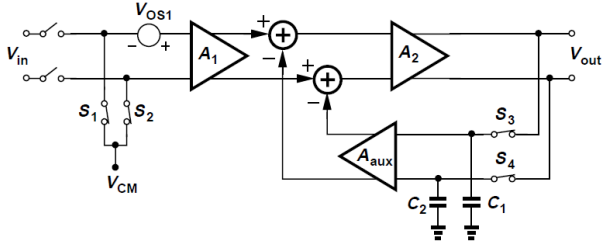
- Offset cancellation can isolate signal path from offset storage capacitors by use of "auxiliary" amplifier



- Consider above circuit, where Aaux amplifies the differential voltage *V1* stored across *C1* and *C2* and subtracts the result from the output of *A1*
- If $V_{OS1}A_1 = V_1A_{aux}$, then for *Vin = 0*, *Vout = 0* and circuit cancels offsets
- *C1* and *C2* do not appear in the signal path

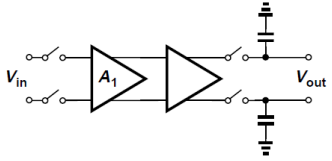
Offset Cancellation Techniques

- ***V1*** **is generated by adding a second stage,** ***A2*** **and the output is sensed by** ***Aaux*** **during offset cancellation**
- **First only** ***S1*** **and** ***S2*** **are on, yielding** $V_{out} = V_{OS1}A_1A_2$
- **Next, assume** ***S3*** **and** ***S4*** **turn on , placing** ***A2*** **and** ***Aaux*** **in a negative feedback loop**
- ***Vout*** **drops by a factor approximately equal to the loop gain:** $V_{OS1}A_1A_2/(A_2A_{aux}) = V_{OS1}A_1/A_{aux}$
- **Stored across** ***C1*** **and** ***C2*****, this value is indeed the required** ***V1*** **because** $(V_{OS1}A_1/A_{aux})A_{ux} = V_{OS1}A_1$

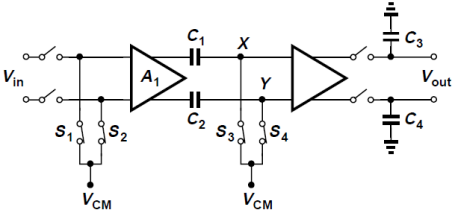


Reduction of Noise by Offset Cancellation

- Offset of a differential amplifier can be viewed as a noise component having a very low frequency
- Consider a differential amplifier to be used at the front end of a sampling system [Fig. (a)]
- Noise of *A1* directly corrupts *Vin*, especially *1/f* noise
- In Fig. (b), amplifier undergoes offset cancellation before every sampling operation
- If time elapsed from end of offset cancellation to end of sampling is *[]t*, noise frequencies below *1/[]t* are suppressed



(a)



(b)

Alternative Definition of CMRR

- **Consider a differential circuit sensing an input CM change, *Vin,CM***
- **If the differential output voltage changes by *Vout* while the differential input voltage is zero, we can say that the output offset voltage of the circuit has changed by *Vout***
- **In other words,**

$$A_{CM-DM} = \frac{\Delta V_{OS,out}}{\Delta V_{CM,in}}$$

- **Since** $CMRR = A_{DM}/A_{CM-DM}$**, we have**

$$CMRR = \frac{A_{DM}}{\frac{\Delta V_{OS,out}}{\Delta V_{CM,in}}} = \frac{\frac{\Delta V_{CM,in}}{\Delta V_{OS,out}}}{A_{DM}}$$

Alternative Definition of CMRR

- Since $\Delta V_{OS,out}/A_{DM}$ is the input-referred offset voltage, we have

$$CMRR = \frac{\Delta V_{CM,in}}{\Delta V_{OS,in}}$$

- This result proves useful in analyzing behavior of circuits
- In circuit of Fig. (a), body effect is eliminated and *VTH1,2* does not depend on *Vin,CM*
- *M1*, *M2* in Fig. (b) experience body effect and thus have mismatch in *VTH1* and *VTH2*, degrading its CMRR