Digital Laboratory Lab02 Report

(Experiment Record Template)

Watch Lab video before the lab day. Playlist:

<https://youtube.com/playlist?list=PLcGCikr5PJAilEccmMP_1dyEHuudl4W_0>

**You can finish the lab at home before you enter the classroom.**

Note:

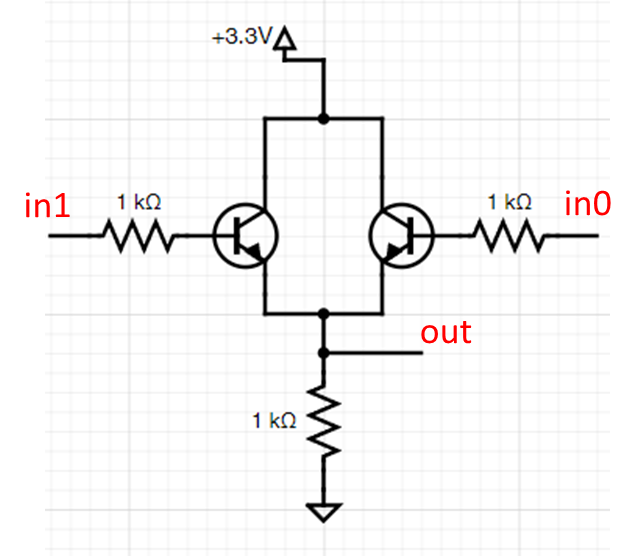
All transistors are “2N2222”. All resistors are “1k Ohm”.

Logic(1) can be expressed as 1. Logic(0) can be expressed as 0.

**Experiment-01**

Please use Analog Discovery 2 to test and complete the truth table.

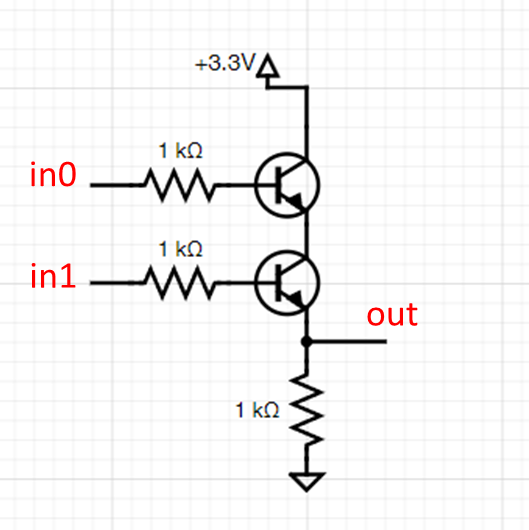
**exp01-1: unknown circuit.**

****

**Truth Table**

|  |  |  |
| --- | --- | --- |
| **in1** | **in0** | **out** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**exp01-2: unknown circuit.**



**Truth Table**

|  |  |  |
| --- | --- | --- |
| **in1** | **in0** | **out** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**What is the “unknown circuit” in exp01-1?**

It’s an OR gate.

**What is the “unknown circuit” in exp01-2?**

It’s an AND gate.

**After this week’s experiment, I decided to look up “how do transistors work?”. Here’s what I learned:**

Before talking about transistors, we have to know what a diode is: A diode is an electronic component that allows current to flow in one direction while blocking current in the opposite direction. We achieve that by using p-type semiconductors and n-type semiconductors. P-type semiconductors are silicon doped with trivalent(三價)element. This process causes p-type semiconductors to lack electrons, forming electron holes. N-type semiconductors are silicon doped with pentavalent(五價)element. This process causes n-type semiconductors to have free electrons. If we combine p-types and n-types together, the free electrons diffuse from n to p at the junction, and vice versa for the electron holes. After that, the n section has a positive charge(because it now has less electrons and more holes) and the p section has a negative charge(because it now has more electrons and less holes). This forms a electric field that pushes atoms away from the p-n junction, forming a region called the depletion layer since it has been depleted of charge carriers. When current flows from N to P(reverse biased 逆向偏壓), the depletion layer acts as a barrier, blocking the flow. When current flows from P to N(forward biased 正向偏壓), the depletion layer gets thinner, allowing current to get through.

What we used in our experiment are NPN BJTs(Bipolar Junction Transistors 雙極性接面型電晶體), the collector pin is linked to a mildly doped N, while the emitter pin is linked to heavily doped N. The base pin is linked to a thin layer of P. When we flow current through the base pin(p-type), we can reduce the depletion layers between the P and the Ns, allowing current to flow from the collector to the emitter.

**Experiment-02**

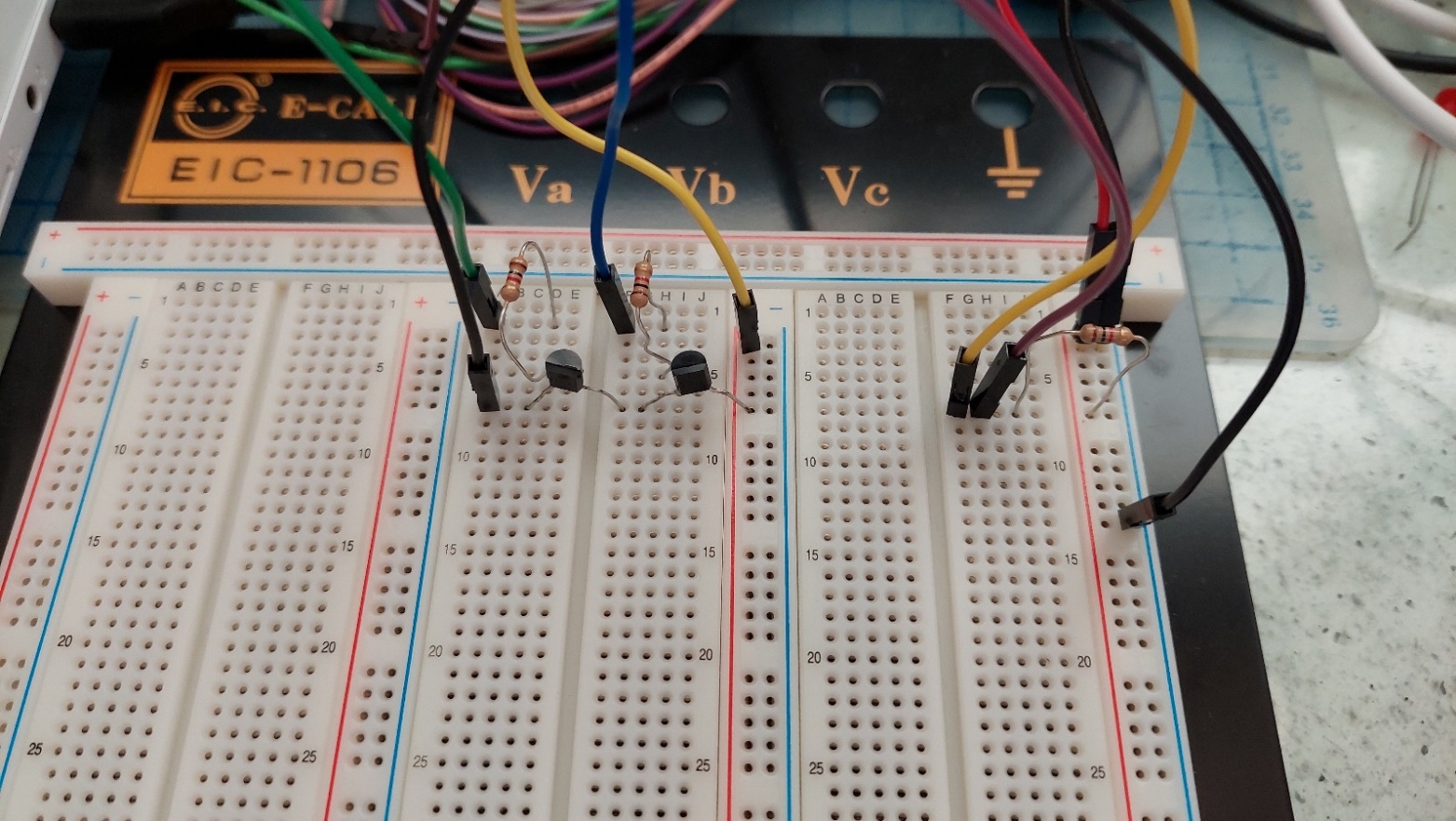
Design the required circuit and prove it can be satisfied the requirements.

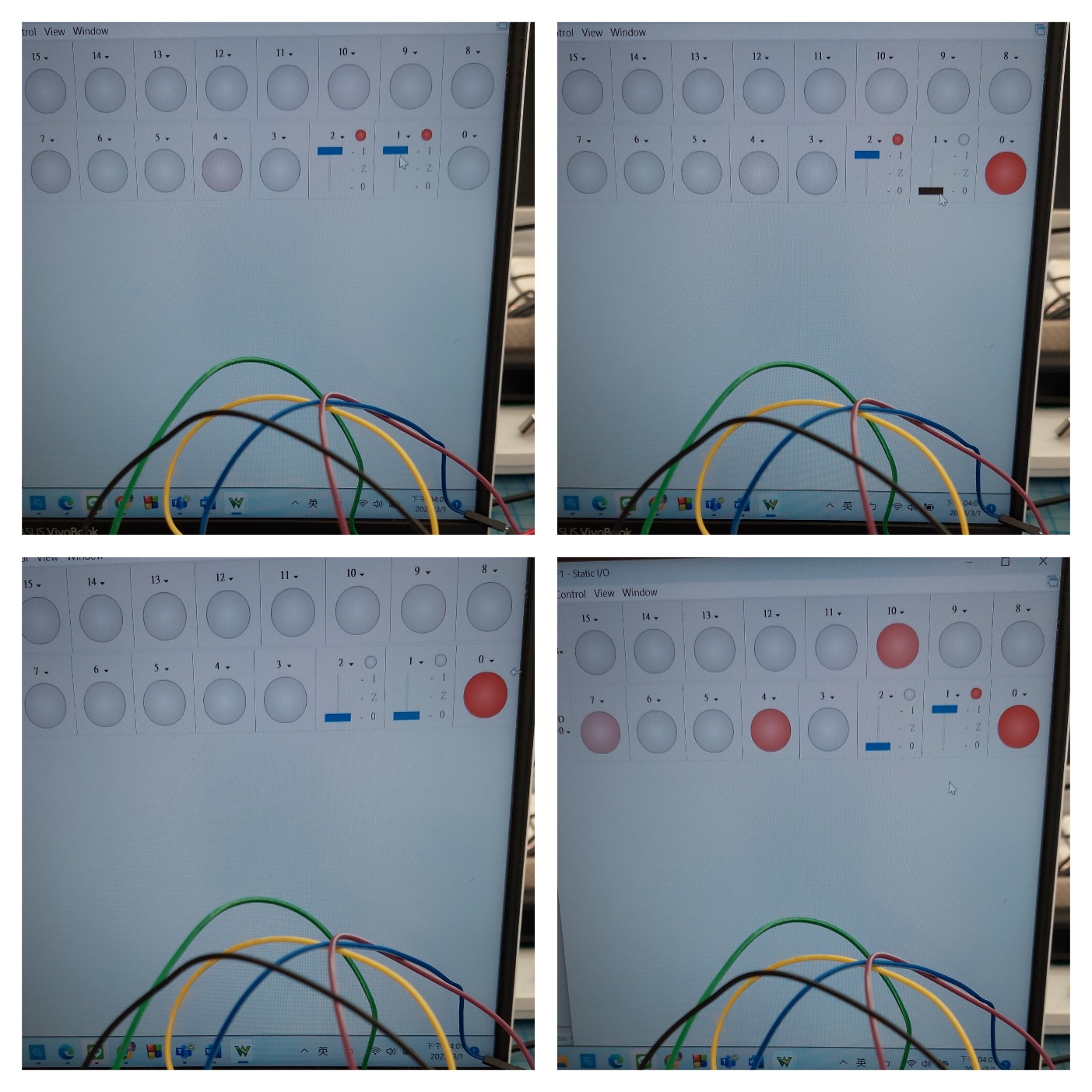
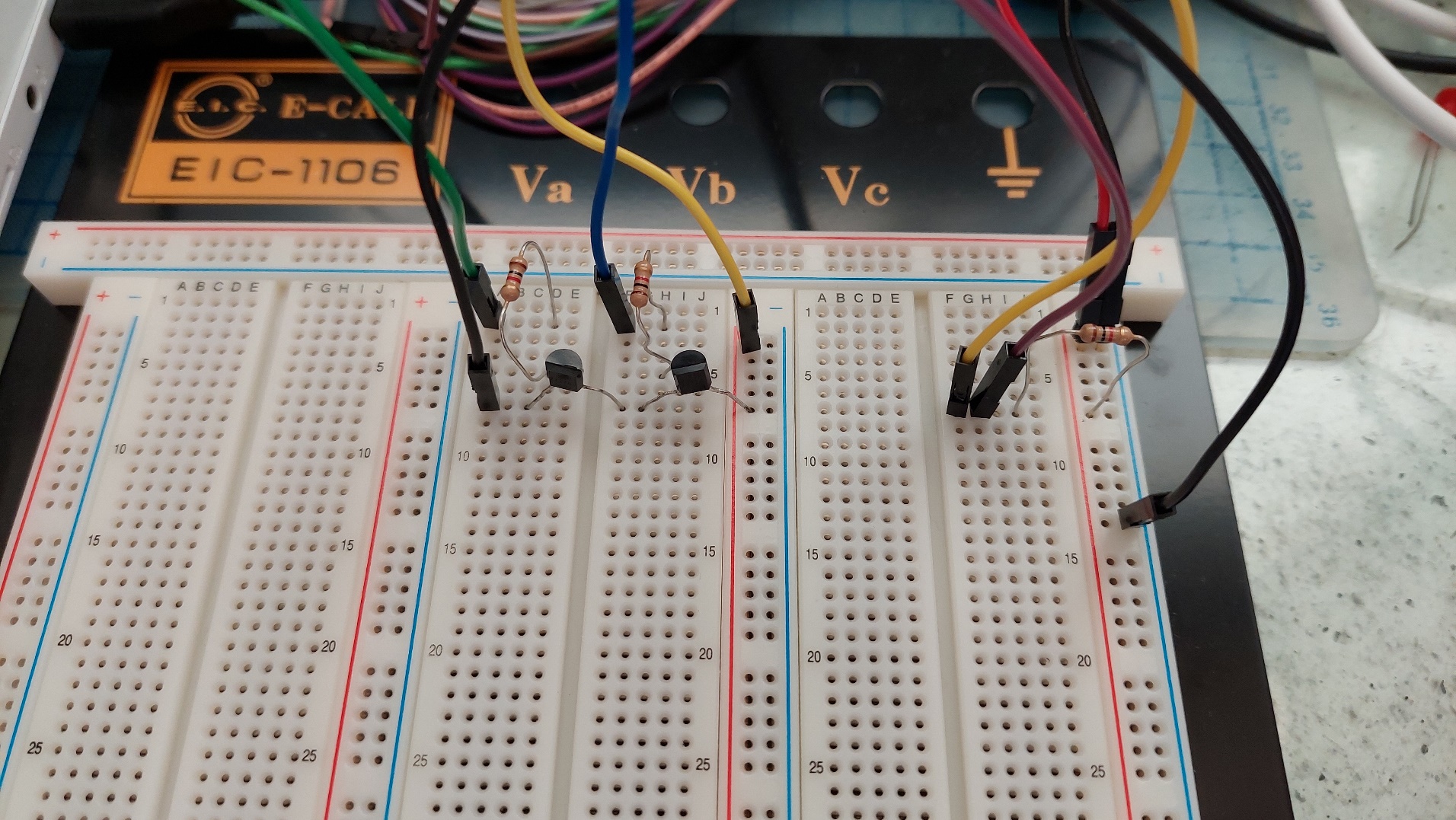
**exp02-1: Use transistor switch circuit to design a 2-input NAND gate.**

Circuit diagram **(You can attach hand-drawing plot or use software to generate the diagram)**



How to prove that your design is a 2-input NAND gate circuit?



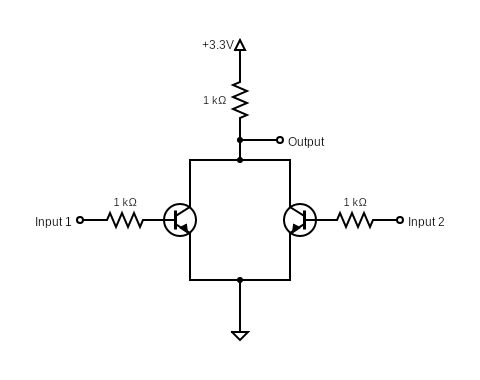


**Truth Table**

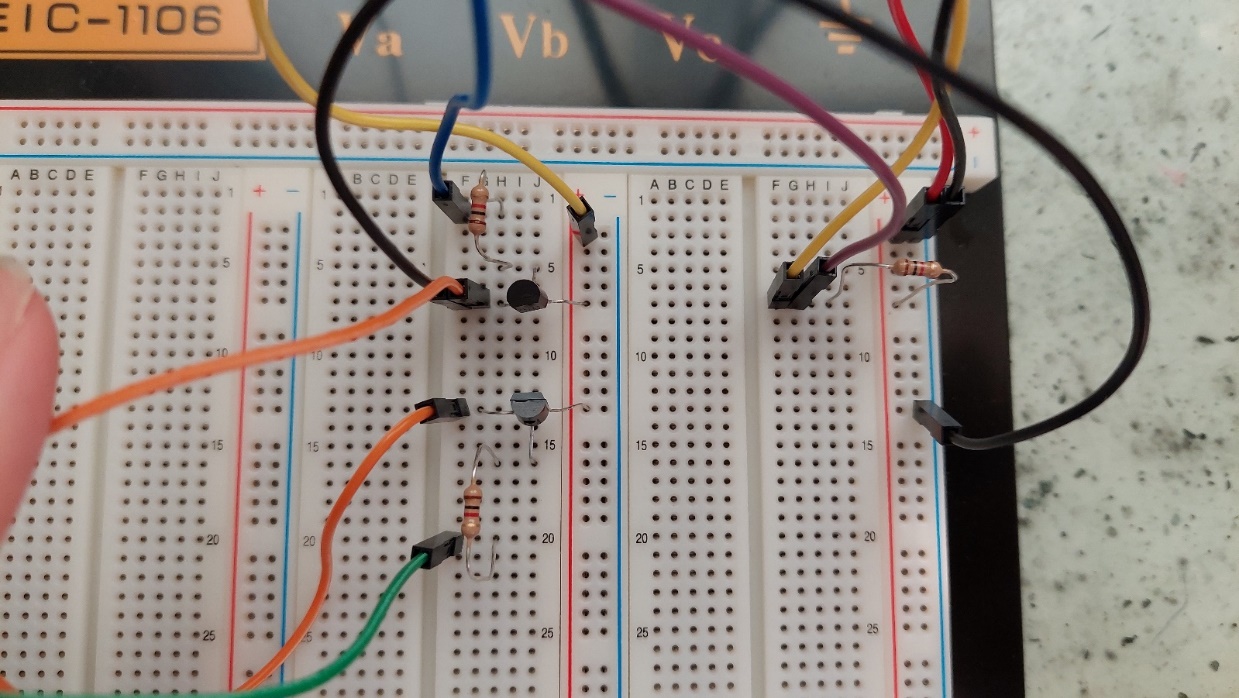
|  |  |  |
| --- | --- | --- |
| **in1** | **in0** | **out** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

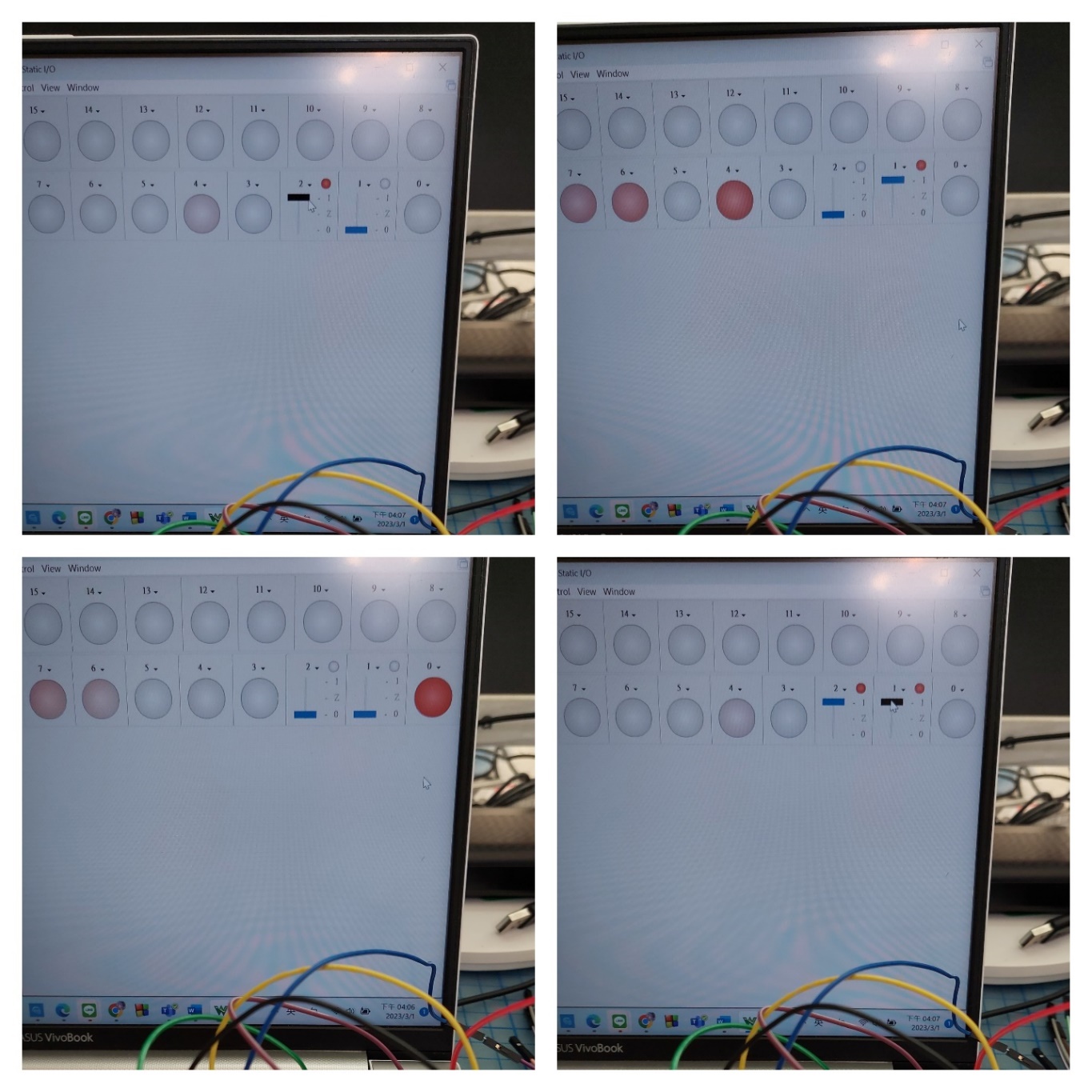
**exp02-2: Use transistor switch circuit to design a 2-input NOR gate.**

Circuit diagram **(You can attach hand-drawing plot or use software to generate the diagram)**

****

How to prove that your design is a 2-input NOR gate circuit?





**Truth Table**

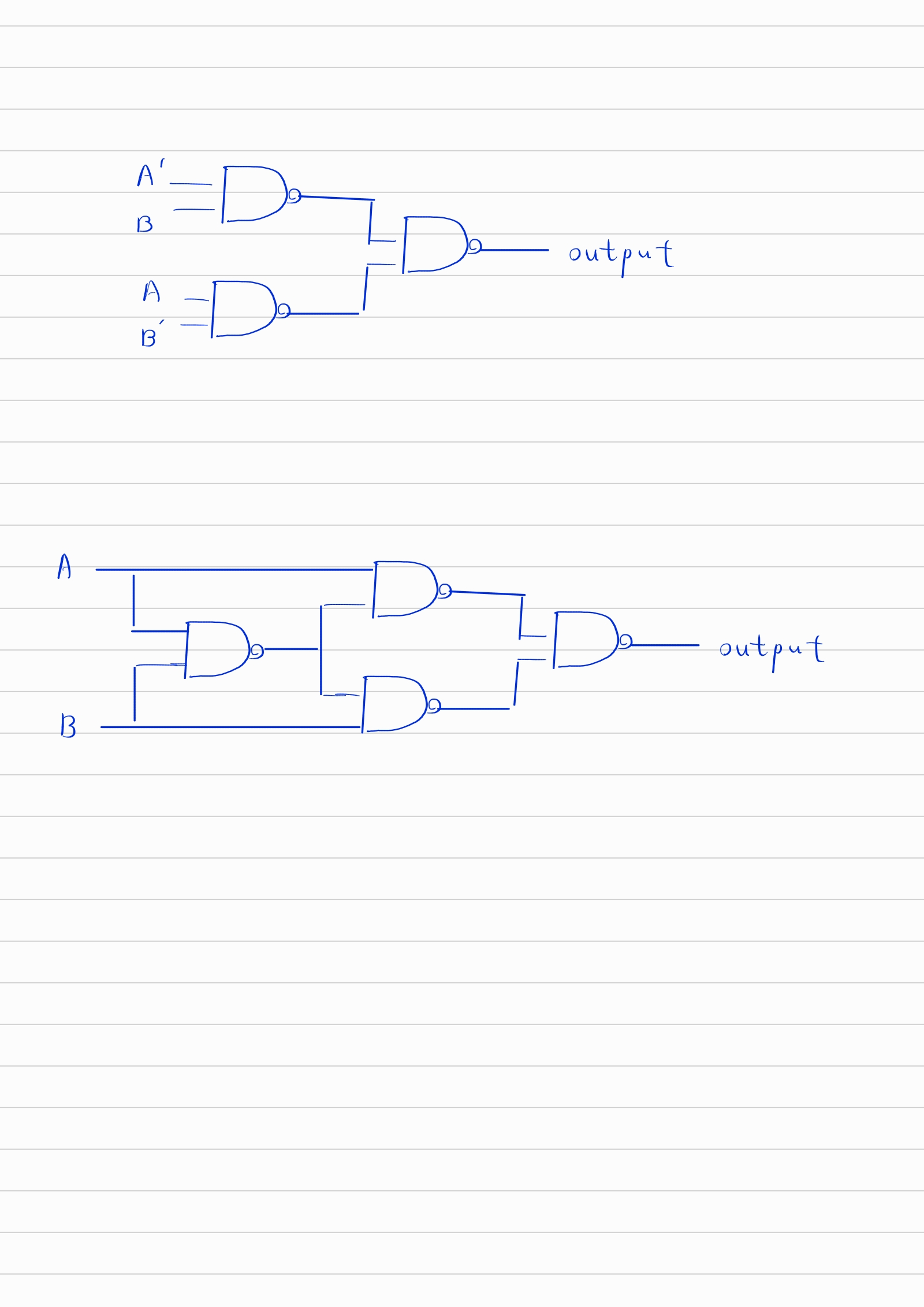
|  |  |  |
| --- | --- | --- |
| **in1** | **in0** | **out** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Experiment-03**

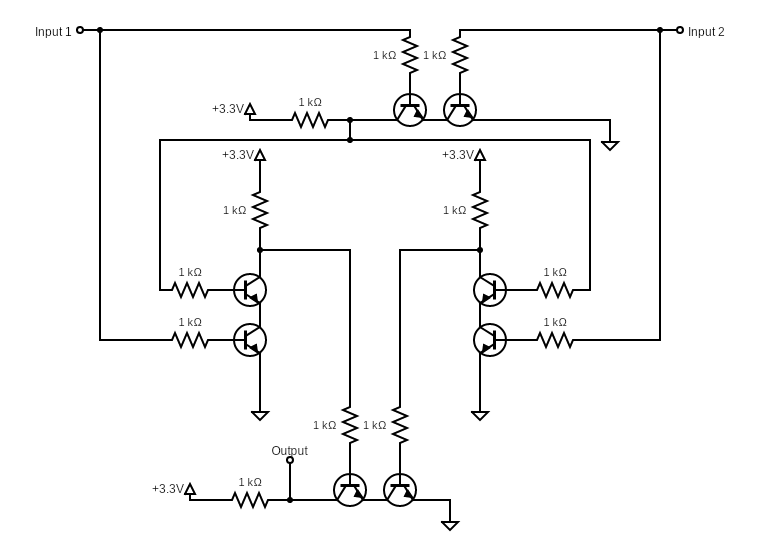
**According to previous experiment results, please implement a 2-input XOR gate by applying only 2-input NAND gates.**

NOTE: Try your best to eliminate the count of 2-input NAND gates.

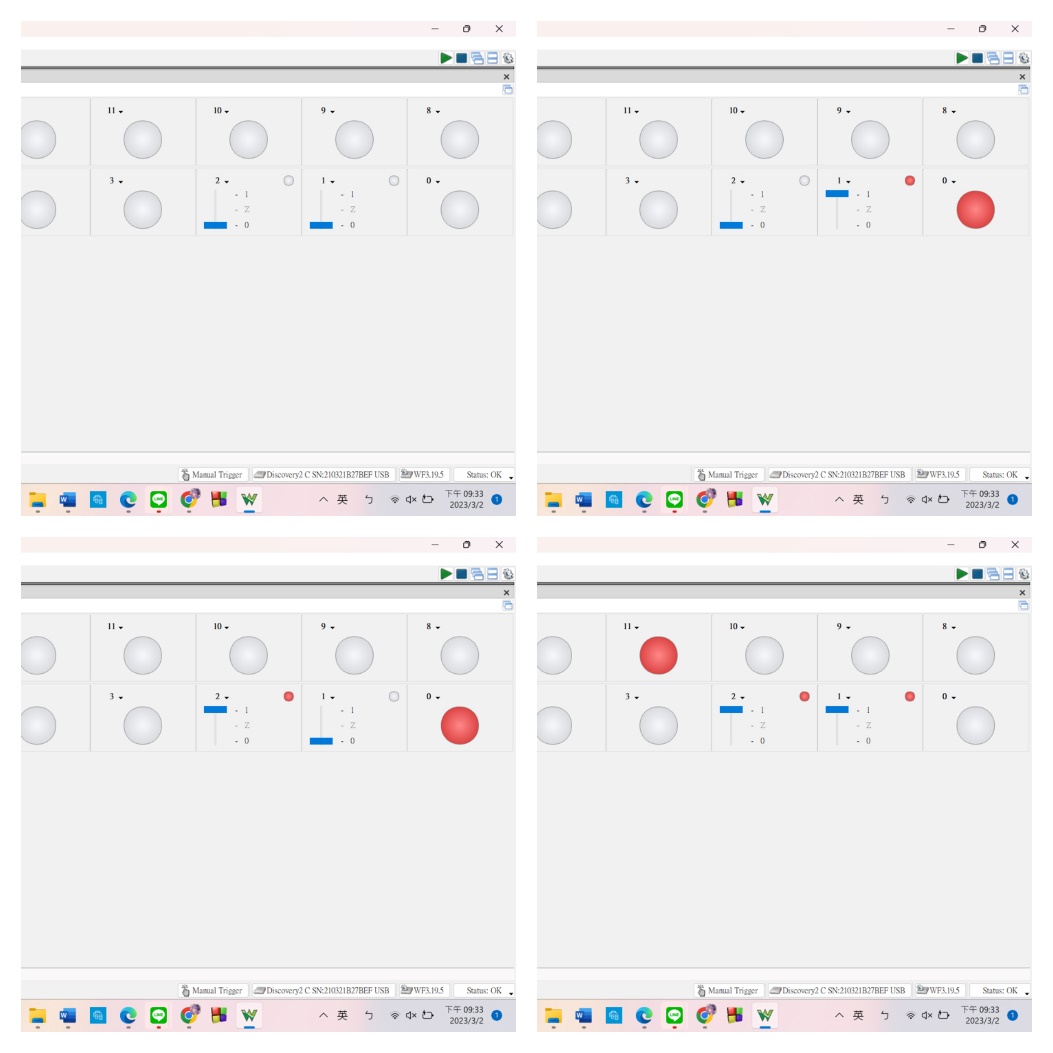
Logic diagram **(Use NAND gate to show your design)**



Circuit diagram **(You can attach hand-drawing plot or use software to generate the diagram)**



How to prove that your design is a 2-input XOR gate circuit?



**Truth Table**

|  |  |  |
| --- | --- | --- |
| **In2** | **In1** | **out** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Questions: **(Solve it at home. No live demo)**

How many transistors did it take to implement the design?

One NAND gate requires 2 transistors. This circuit required 4 NAND gates, so I used 8 transistors in total.

How many NAND gates did you use to finish the design?

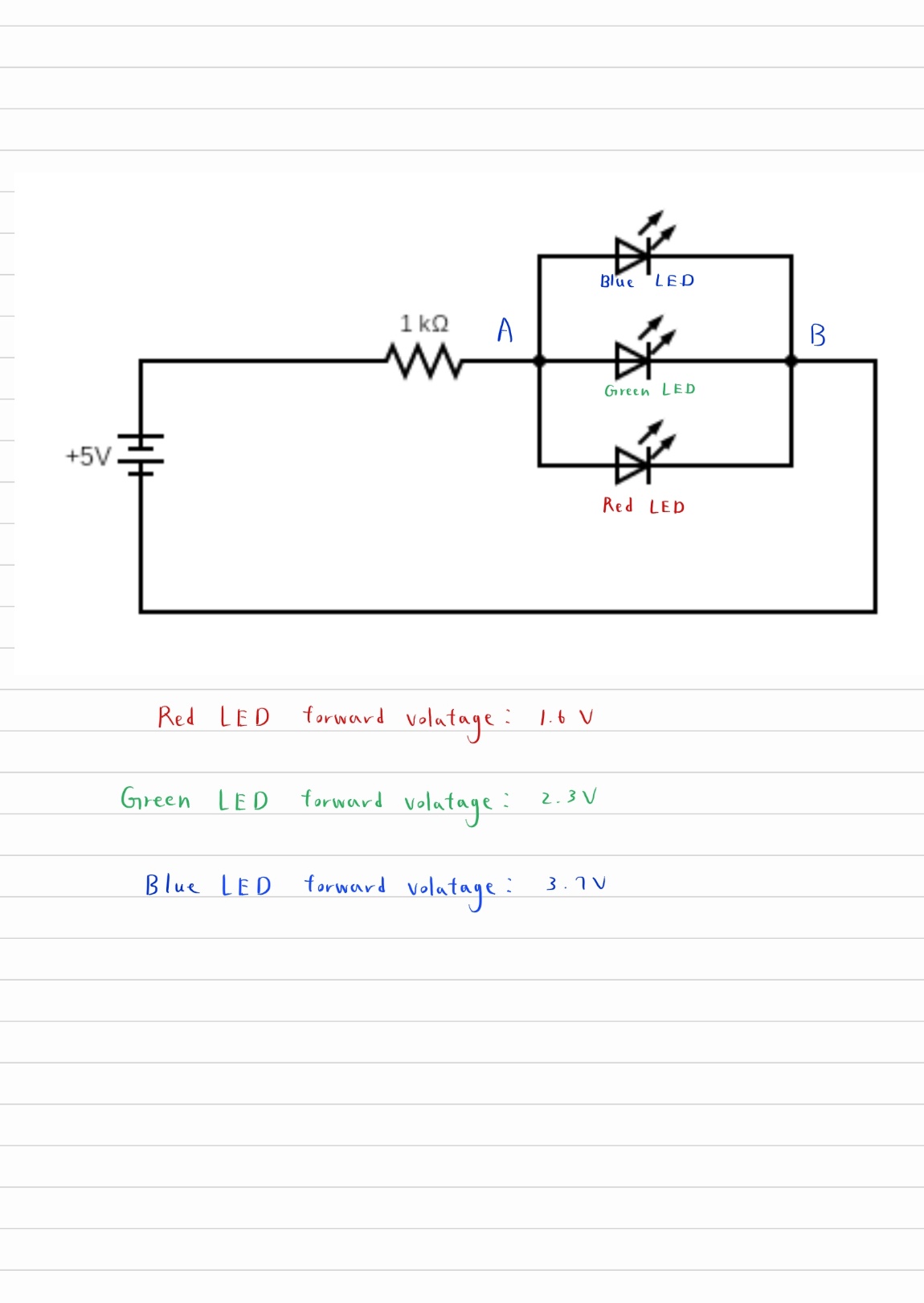
This circuit required 4 NAND gates.

How many resistors did you use to finish the design?

One NAND gate requires 3 resistors. This circuit required 4 NAND gates, so I used 12 resistors in total.

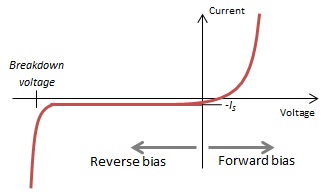
**(Ask your own questions and answer them by yourself)**

**In order to fully implement the design, we needed 12 resistors. However, we were only given 10. I thought that I could conserve resistors by sharing a single resistor between 2 parallel NAND gate inputs like so (using LEDs as example):**



**Many managed to pass their demo doing so, but it didn’t work for me. Frustrated, I asked the TA for help. We verified that my logic diagram and circuit diagram were both correct and that my 4 NAND gates on the breadboard worked fine individually. I explained how we did not get enough transistors and why I did what I did. He provided me with some additional transistors and voilà! Everything worked after I gave every input their individual resistor. Why is this?**

Basically, different diodes have different forward voltage values. If the voltage from the supply is not enough, a diode would have a high resistance because its depletion layer is still present. Once the voltage supplied goes above the forward voltage threshold(knee voltage), the resistance of the diode becomes much smaller, allowing current to easily flow through (as shown in the graph below). In other words, the smaller the forward voltage is, the easier it is for that diode to draw current.

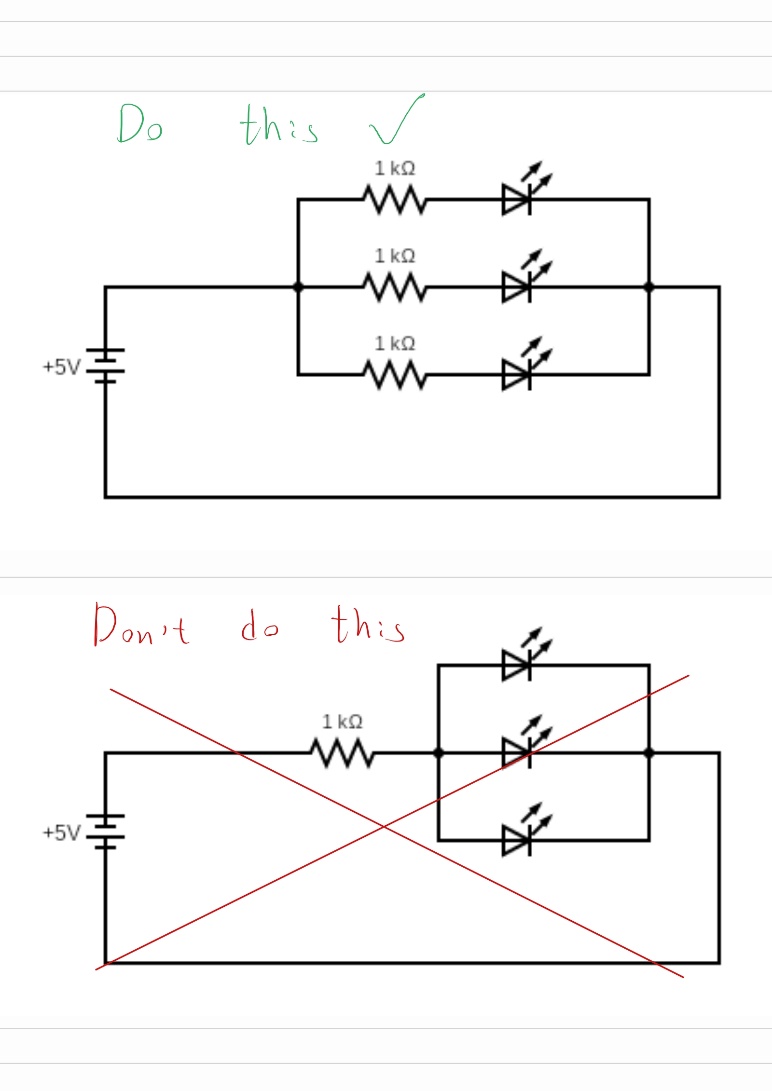
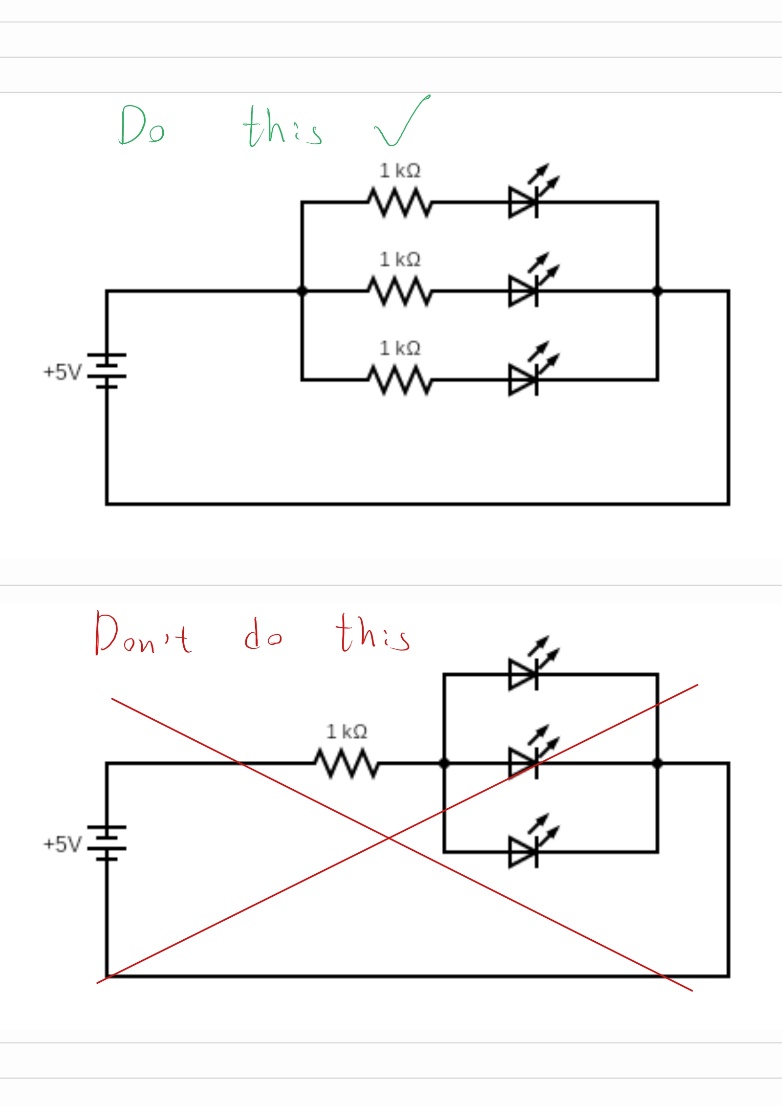


Knee Voltage

When I share one resistor with 3 diodes like the picture above, this becomes a problem. It is much easier for the red LED to draw current than the green or the blue one. What would happen if we were to implement this circuit is: the red LED would be super bright because it’s getting a lot of current, while the green and the blue might not turn on at all. Eventually, the red LED may get fried.

**If this the case, why were so many classmates able to finish their demo successfully despite having to share the resistors?**

I think this is because we are all using the same 2N2222 transistors; therefore there is not much difference in forward voltage between one transistor and the other. This problem mentioned above becomes less significant when the forward voltage values of the semiconductor devices in parallel are nearly the same as each other. However, it is possible for there to be some errors during manufacturing. I guess I was just extra unlucky and used transistors that had a greater difference in their forward voltage values. My main takeaway from this experience is:



**While working on my circuit, I accidently reversed my collector and emitter pin. The circuit worked. However, after looking it up. I realized that this is a very bad practice. Here’s why:**

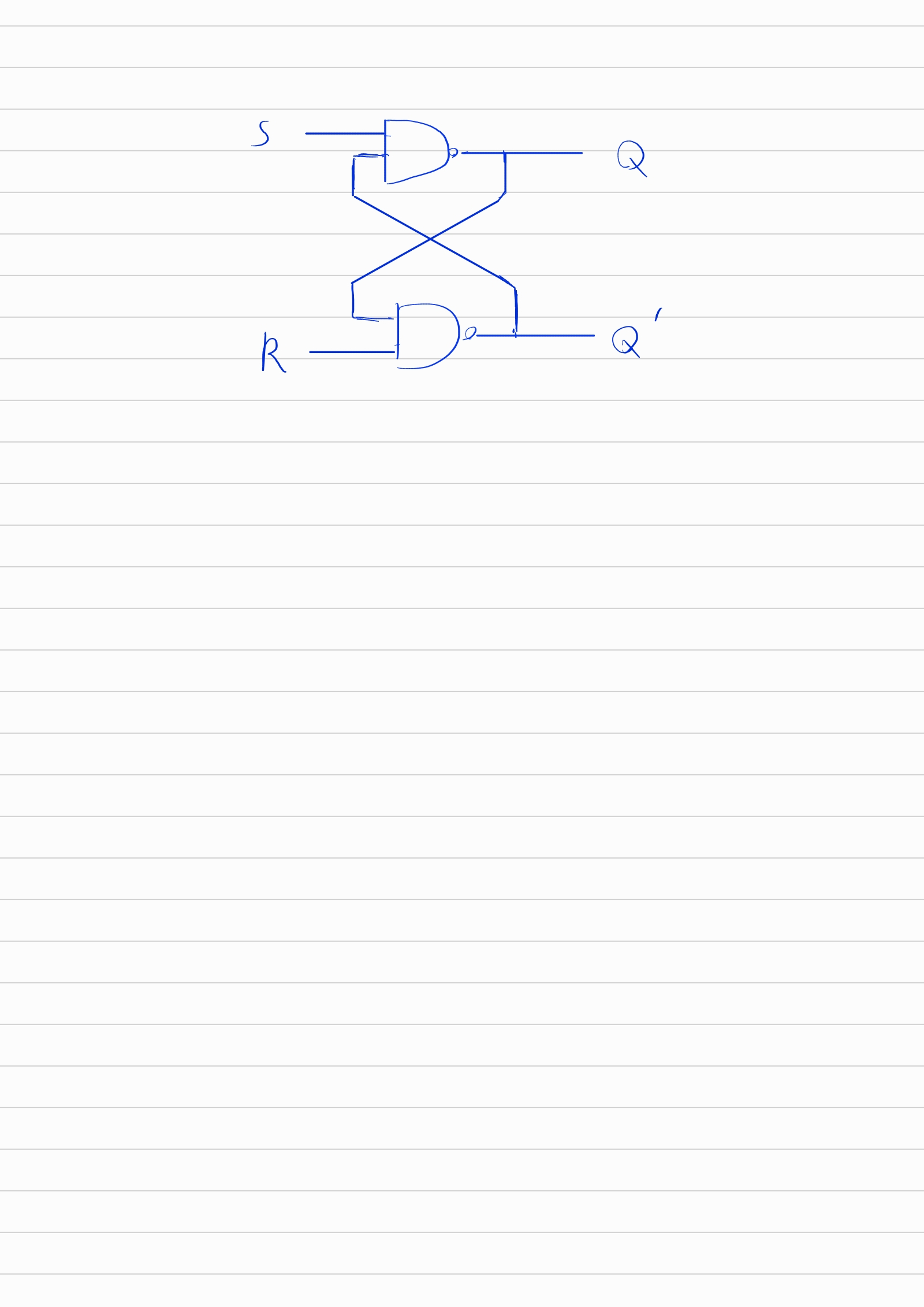
As I mentioned earlier in the report, the emitter is heavily doped and is designed to emit electrons, while the collector is lightly doped and is designed to collect electrons. Normally, current does not flow from the collector to the base in an NPN BJT. However, it does when you reverse the connection. This will result in a large amount of current flowing through the device, which may fry it.

**Experiment-04**

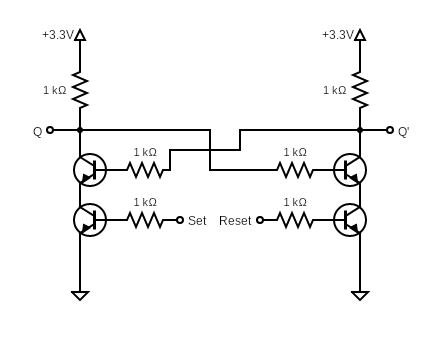
**According to exp02 results, please implement a 2-input SR Latch circuit by applying only 2-input NAND gates.**

Logic diagram **(Use NAND gate to show your design)**

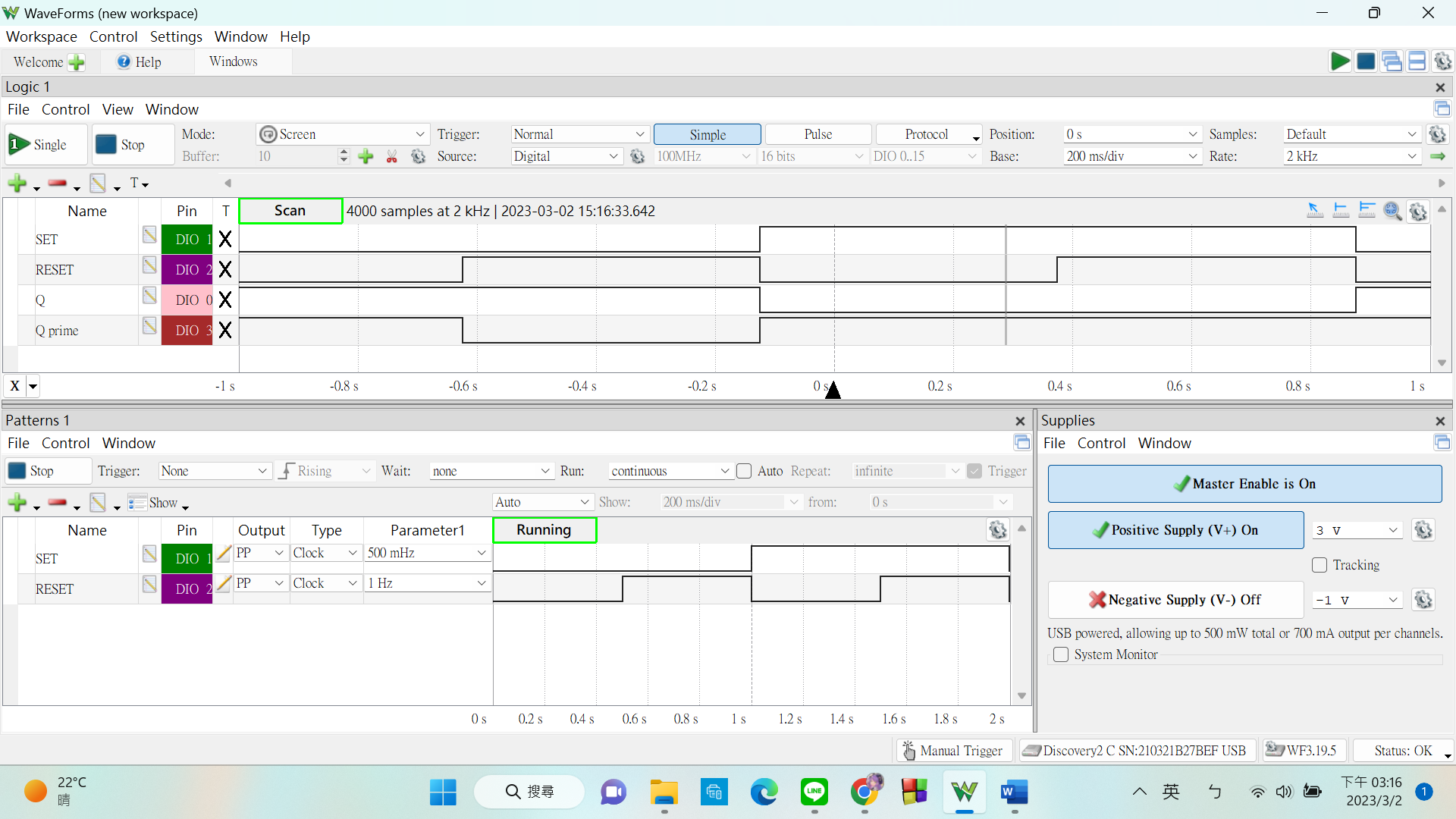
**Note: You should label every node name clearly. (e.g., set/reset/Q/~Q)**

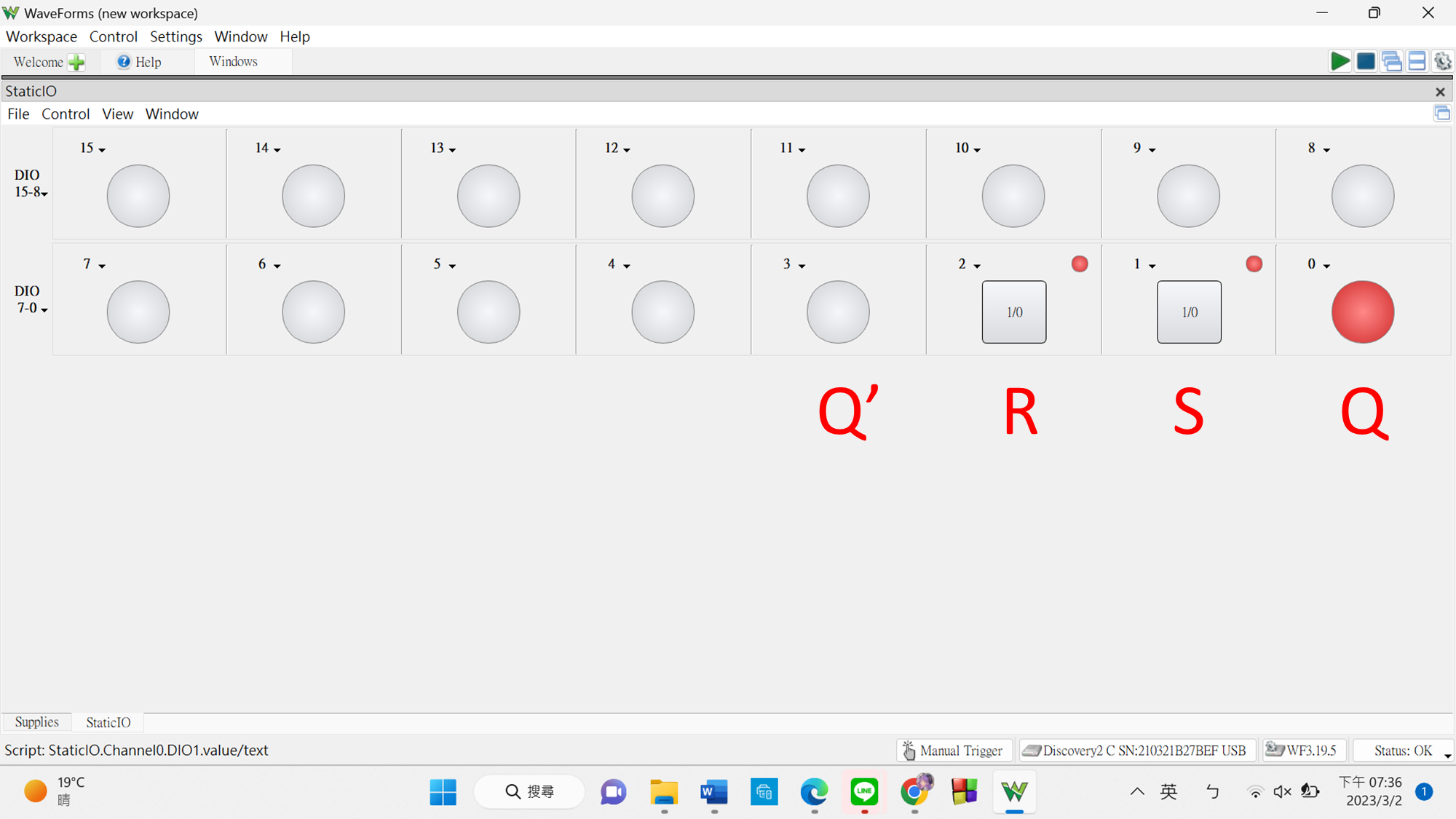
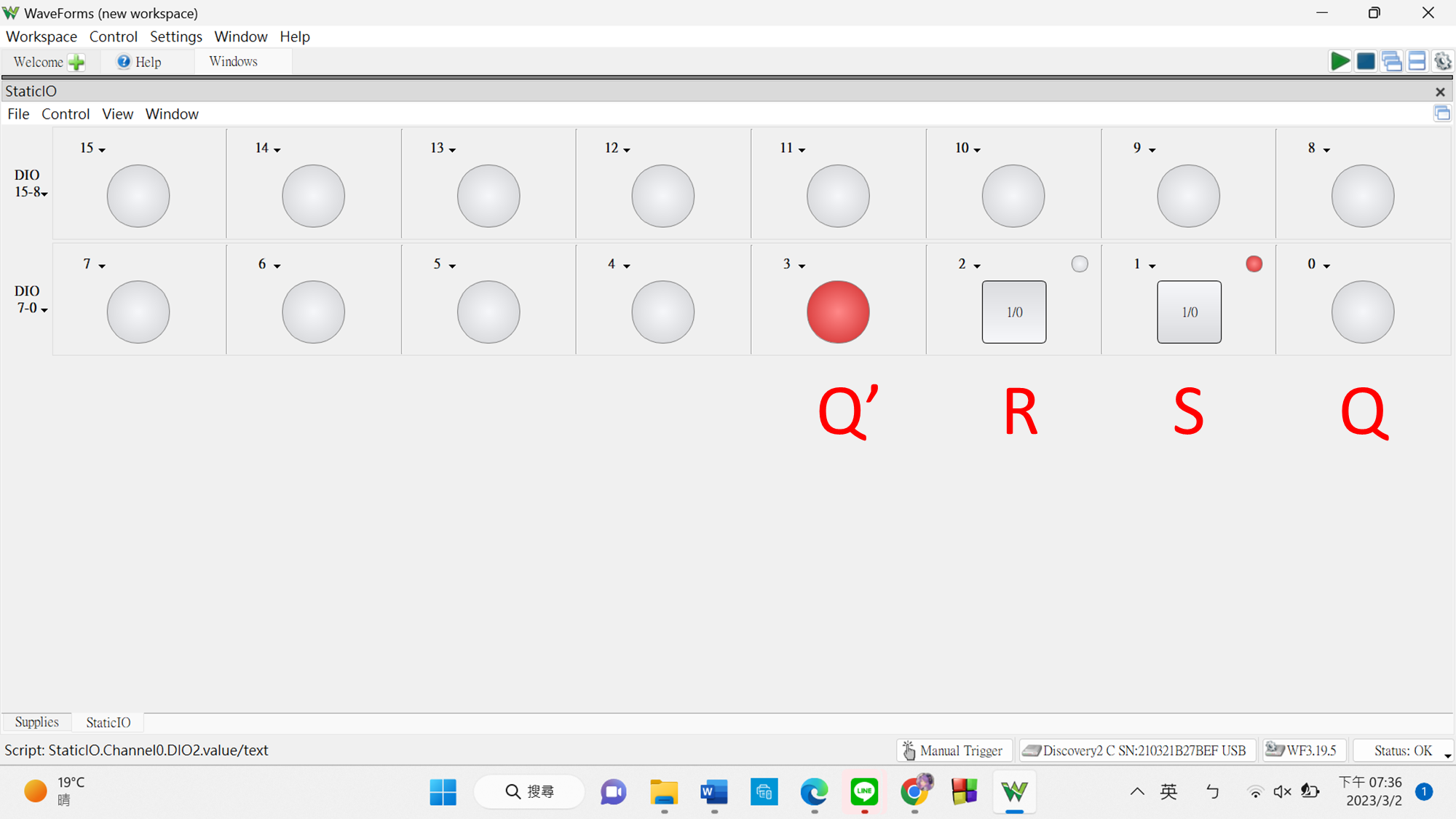


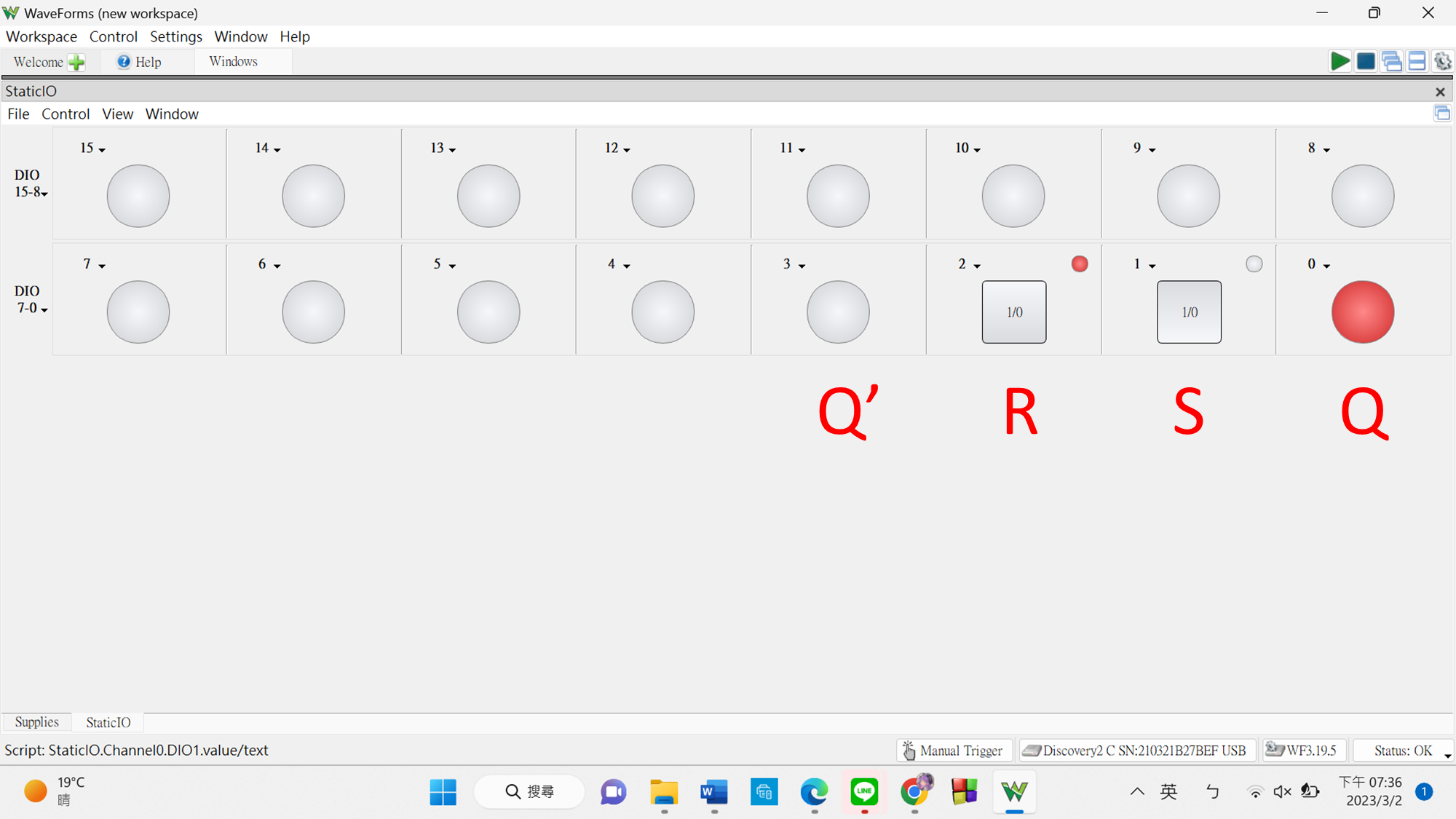
Circuit diagram **(You can attach hand-drawing plot or use software to generate the diagram)**



Your test record (photo or video)





**Truth Table**

|  |  |  |
| --- | --- | --- |
| **Set** | **Reset** | **Q** |
| 0 | 0 | Illegal state |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | No change |

**Initially, I had my circuit correctly implemented. Yet, when I turned on the power supply, both Q and Q’ were logic 1 on my Waveform display. I couldn’t figure out how to get it out of this state. Here’s how I fixed it:**

Originally, I set my buttons(pin 1: Set, pin 2: Reset) to 0/1 (0 when released, 1 when pressed). Since this SR latch is made with NAND gates, it is active low. The S = 0, R = 0 state is actually illegal. When I set the buttons like so, I accidentally put the circuit in this state. I realized this and changed the buttons to 1/0 (1 when released, 0 when pressed) and fixed the problem.