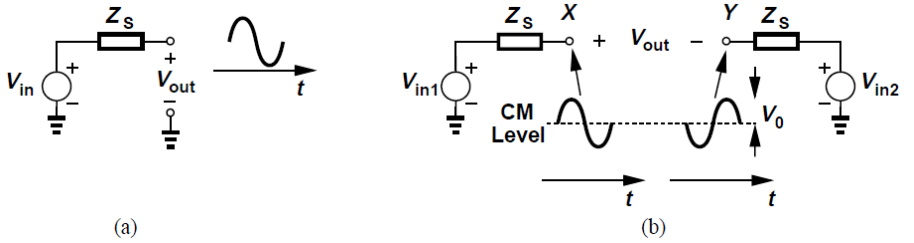
Chapter 4: Differential Amplifiers

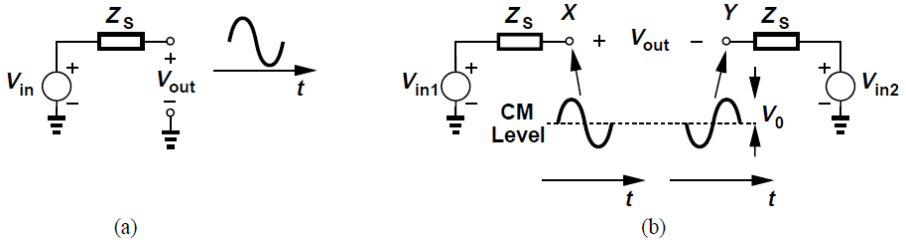
Single-Ended and Differential Operation

- A "single-ended" signal is one that is measured with respect to a fixed potential, usually the ground [Fig. (a)]
- A differential signal is one that is measured between two nodes that have equal and opposite signal excursions around a fixed potential [Fig. (b)]



- The "center" potential in differential signaling is called the "common-mode" (CM) level
  - bias value of the voltages, i.e., value in the absence of signals

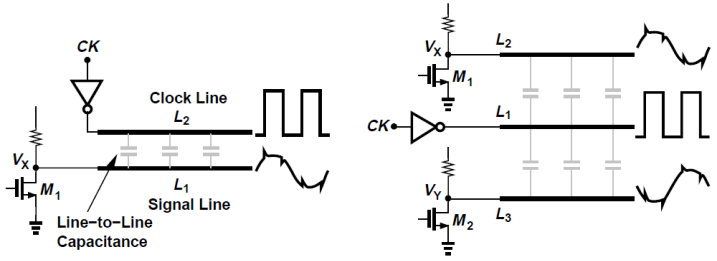
Single-Ended and Differential Operation



- **Suppose each single-ended output in Fig. (b) has a peak amplitude of *V0***
- **Then single-ended peak-to-peak swing is 2*V0* and differential peak-to-peak swing is 4*V0***
- **For example, if voltage at X (w.r.t. ground) is *V0*cos*ωt* + *VCM* and that at Y is -*V0*cos*ωt* + *VCM*, then the peak-to-peak swing of *VX* - *VY* is 4*V0***

Advantages of Differential Operation

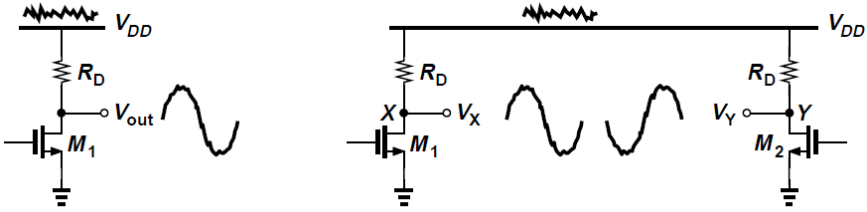
- **Higher immunity to "environmental" noise in differential operation as compared to single-ended signaling**



- **In Fig. (a), transitions on the clock line *L2* corrupt the signal on sensitive signal line *L1* due to capacitive coupling between the lines**
- **If the sensitive signal is distributed as two equal and opposite phases as in Fig. (b), the clock line placed midway disturbs the differential phases equally and keeps the difference intact, called common-mode (CM) rejection**

Advantages of Differential Operation

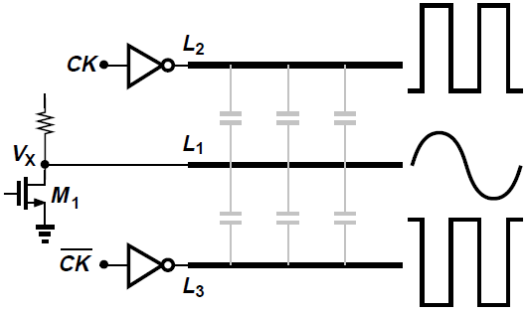
- CM rejection also occurs with noisy supply voltages



- In the CS stage of Fig. (a), if *VDD* varies by *ΔV*, then *Vout* changes by roughly the same amount, i.e., output is susceptible to noise on *VDD*
- In the symmetric circuit of Fig. (b), noise on *VDD* affects *VX* and *VY*, but not *VX – VY = Vout*
- The differential circuit is more robust to supply noise than its single-ended counterpart

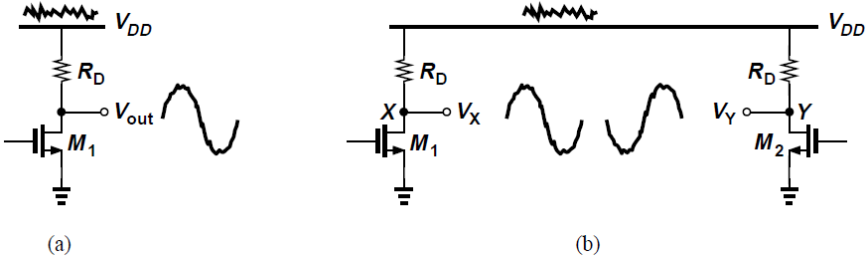
Advantages of Differential Operation

- Differential operation is as beneficial for sensitive signals ("victims") as for noisy lines ("aggressors")



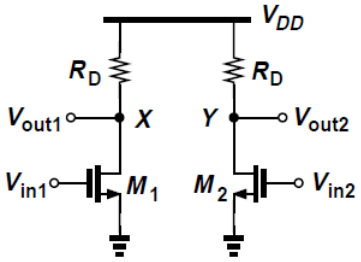
- Clock signal is distributed in differential form on two lines
- With perfect symmetry, the components coupled from *CK* and $\overline{CK}$ to the signal line cancel each other

Advantages of Differential Operation



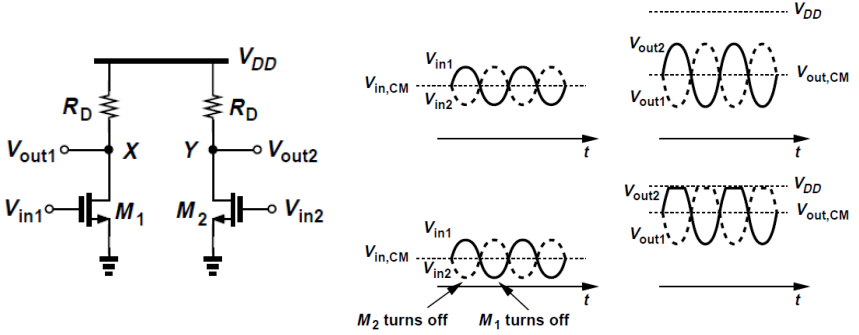
- **Differential signaling increases maximum achievable voltage swings**
- **In the above differential circuit, the maximum output swing at *X* or *Y* is equal to *VDD* – (*VGS* – *VTH*)**
- **For *VX* – *VY*, the maximum swing is 2[*VDD* – (*VGS* – *VTH*)]**
- **Other advantages of differential circuits include simpler biasing and higher linearity**
- **Advantages of differential operation outweigh the possible increase in area**

Basic Differential Pair: Introduction



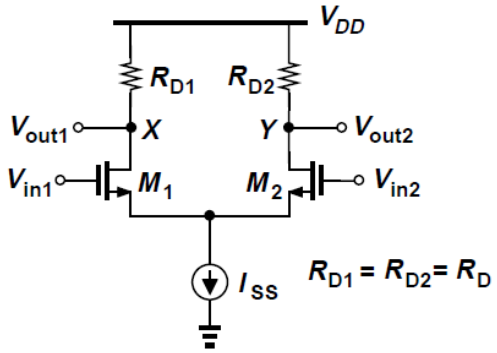
- **The simple differential circuit shown incorporates two identical single-ended paths to process the two phases**
- **The two differential inputs *Vin1* and *Vin2*, having a certain CM level *Vin,CM* are applied to the gates**
- **The outputs are differential too and swing around the output CM level *Vout,CM***
- **This circuit offers all advantages of differential signaling: supply noise rejection, higher output swings, etc.**

Basic Differential Pair: Introduction



- As the input CM level, *Vin,CM* changes, so do the bias currents of *M1* and *M2*, thus varying both the transconductance of the devices and the output CM level
- As shown in Fig. (b), if the input CM level is excessively low, the minimum values of *Vin1* and *Vin2* may turn off *M1* and *M2*, leading to severe clipping at the output
- Bias currents of the devices should have minimal dependence on the input CM level

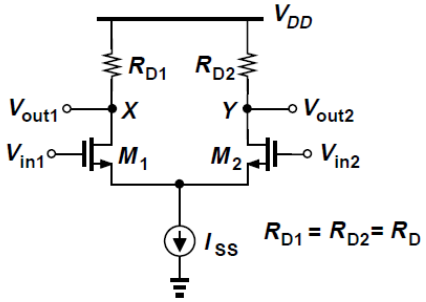
Basic Differential Pair



- **A "differential pair" incorporates a current source *ISS* to make *ID1* + *ID2* independent of *Vin,CM***

- **If *Vin1* = *Vin2*, the bias current of both *M1* and *M2* is *ISS*/2 and the output CM level is *VDD* – *RDISS*/2**

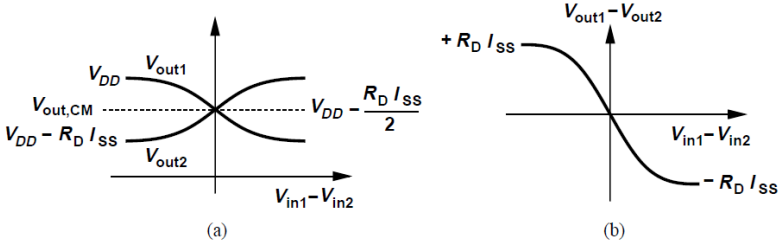
Basic Differential Pair: Qualitative Analysis



- When *Vin1* is much more negative than *Vin2*, *M1* is off, *M2* is on and *ID2* = *ISS*, *Vout1* = *VDD* and *Vout2*=*VDD* – *RDISS*
- As *Vin1* is brought closer to *Vin2*, *M1* gradually turns on, drawing a fraction of *ISS* from *RD1* and lowering *Vout1*

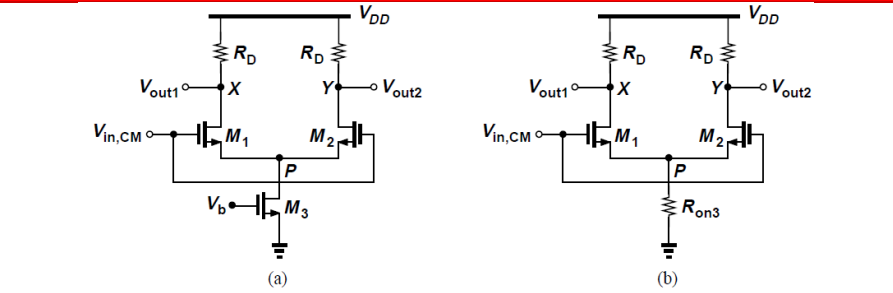
- Since *ID1* + *ID2* = *ISS*, *ID2* falls and *Vout2* rises
- For *Vin1*=*Vin2*, *Vout1*=*Vout2*=*VDD* – *RDISS*/2, which is the output CM level
- When *Vin1* becomes more positive than *Vin2*, *ID1* becomes higher than *ID2* and *Vout1* drops below *Vout2*
- For sufficiently large *Vin1* – *Vin2*, *M1* "hogs" all of *ISS*, turning M2 off, therefore, *Vout1* = *VDD* – *RDISS* and *Vout2* = *VDD*

Basic Differential Pair: Qualitative Analysis



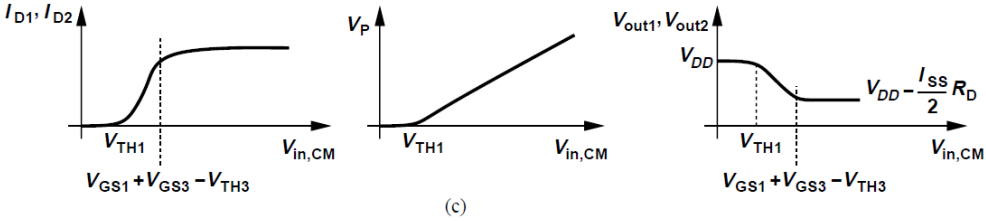
- **The circuit contains three differential quantities: *Vin1* – *Vin2*, *Vout1* – *Vout2*, and *ID1* – *ID2***
- **The maximum and minimum levels at the output are well-defined and independent of the input CM level**
- **The small-signal gain (slope of *Vout1* – *Vout2* versus *Vin1* – *Vin2*) is maximum for *Vin1* = *Vin2* and gradually falls to zero as |*Vin1* – *Vin2*| increases**
- **Circuit becomes more nonlinear as input voltage swing increases**
- **For *Vin1* = *Vin2*, circuit is said to be in "equilibrium"**

Basic Differential Pair: Common-mode behavior



- **Tail current source suppresses the effect of input CM level variations on the output level**
- **Set *Vin1* = *Vin2* = *Vin,CM* and vary *Vin,CM* from 0 to *VDD* [Fig. (a)]**
- **Due to symmetry, *Vout1* = Vout2**
- **For *Vin,CM* = 0, *M1* and *M2* are off, *ID3* = 0 and *M3* operates in the deep triode region [Fig. (b)]**
- **With *ID1* = *ID2* = 0, circuit is incapable of signal amplification; *Vout1* = *Vout2* = *VDD*, and *VP* = 0**

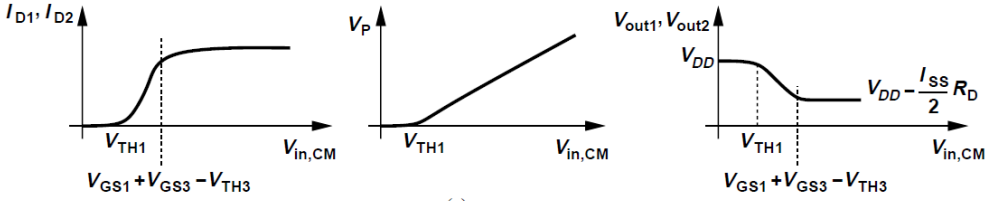
Basic Differential Pair: Common-mode behavior



(c)

- ***M1*** **and** ***M2*** **turn on if** ***Vin,CM*** **≥** ***VTH***
- **Beyond this point,** ***ID1*** **and** ***ID2*** **continue to increase and** ***VP*** **also rises [Fig. (c)]**
- ***M1*** **and** ***M2*** **act as a source follower, forcing** ***VP*** **to follow** ***Vin,CM***
- **When** ***Vin,CM*** **is sufficiently high,** ***VDS3*** **exceeds** ***VGS3*** **–** ***VTH3***, **and** ***M3*** **operates in saturation so that** ***ID1+ID2*** **is constant**
- **For proper operation,** ***Vin,CM*** **≥** ***VGS1*** **+ (***VGS3* **–** ***VTH3***)

Basic Differential Pair: Common-mode behavior



(c)

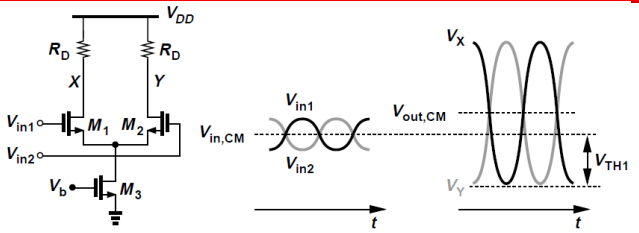
- As *Vin,CM* rises further, *Vout1* and *Vout2* stay relatively constant, therefore, *M1* and *M2* enter the triode region if *Vin,CM* > *Vout1* + *VTH* = *VDD* – *RDISS*/2 + *VTH*

- The allowable value of *Vin,CM* is bounded as follows:

$$V_{GS1} + (V_{GS3} - V_{TH3}) \leq V_{in,CM} \leq \min\left[V_{DD} - R_D\frac{I_{SS}}{2} + V_{TH},\ V_{DD}\right]$$

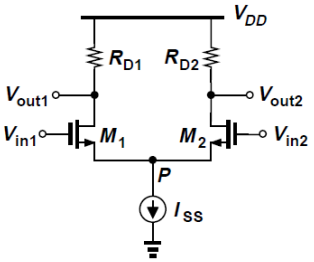
- Beyond the upper bound, the CM characteristics of Fig. (c) do not change, but the differential gain drops

Basic Differential Pair: Output Swings



- Suppose the input and output bias levels are *Vin,CM* and *Vout,CM* respectively, and *Vin,CM* < *Vout,CM*
- Assume a high voltage gain so that input swing is much lesser than the output swing
- For *M1* and *M2* to remain saturated, each output can go as high as *VDD* and as low as *Vin,CM – VTH*
- *Vin,CM* can be no less than *VGS1* + (*VGS3 – VTH3*)
- With this choice of *Vin,CM*, single-ended peak-to-peak swing is *VDD* – (*VGS1 – VTH1*) – (*VGS3 – VTH3*)

Basic Differential Pair: Large-signal Analysis



- **Objective is to determine *Vout1 – Vout2* as a function of *Vin1 – Vin2***
- **If *RD1 = RD2 = RD*, we have**

$$V_{out1} = V_{DD} - R_{D1}I_{D1}$$

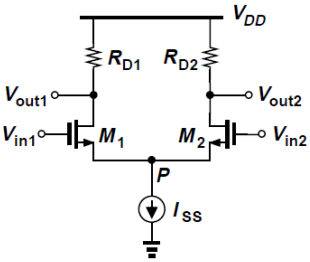
$$V_{out2} = V_{DD} - R_{D2}I_{D2}$$

$$V_{out1} - V_{out2} = R_{D2}I_{D2} - R_{D1}I_{D1} = R_D(I_{D2} - I_{D1})$$

- **Assume the circuit is symmetric, *M1* and *M2* are saturated and $\lambda = 0$**
- **Since *VP = Vin1 – VGS1 = Vin2 – VGS2* , *Vin1 – Vin2 = VGS1 – VGS2***
- **For a square-law device,** $(V_{GS} - V_{TH})^2 = \dfrac{I_D}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}$
- **Therefore,**

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} + V_{TH}$$

Basic Differential Pair: Large-signal Analysis



- **It follows from previous derivation that**

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}.$$

- **To find *ID1 – ID2*, square both sides of above eqn., and recognize that *ID1 + ID2 = ISS***

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox}\frac{W}{L}}(I_{SS} - 2\sqrt{I_{D1}I_{D2}})$$

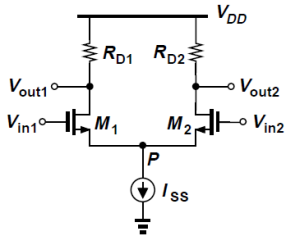
- **Thus,**

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 - I_{SS} = -2\sqrt{I_{D1}I_{D2}}.$$

- **Squaring both sides and noting that 4*ID1ID2* = (*ID1* + *ID2*)2 – (*ID1* – *ID2*)2, we arrive at**

$$(I_{D1} - I_{D2})^2 = -\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2 (V_{in1} - V_{in2})^4 + I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2$$

Basic Differential Pair: Large-signal Analysis



- **Thus**

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

$$= \sqrt{\mu_n C_{ox}\frac{W}{L} I_{SS}}(V_{in1} - V_{in2})\sqrt{1 - \frac{\mu_n C_{ox}(W/L)}{4I_{SS}}(V_{in1} - V_{in2})^2}$$

- ***ID1 – ID2*** **is an odd function of** ***Vin1 – Vin2*** **falling to zero for** ***Vin1 = Vin2***
- **As |*Vin1 – Vin2*| increases from zero, |*ID1 – ID2*| increases**
- **To find the equivalent *Gm* of *M1* and *M2*, denote *ID1 – ID2* and *Vin1 – Vin2* as *ΔID* and *ΔVin* respectively**
- **It can be shown**

$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}}$$

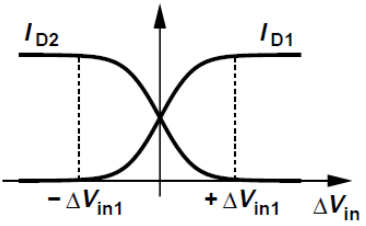
Basic Differential Pair: Large-signal Analysis

- For *ΔVin* = 0, *Gm* is maximum and equal to $\sqrt{\mu_n C_{ox}(W/L)I_{SS}}$.
- Since *Vout1 – Vout2* = *RDΔID* = *-RDGmΔVin* , small-signal differential voltage gain in equilibrium condition is

$$|A_v| = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}} R_D$$

- Since each transistor carries *ISS*/2 in equilibrium, the factor $\sqrt{\mu_n C_{ox}(W/L)I_{SS}}$ is the same as *gm*, i.e., $\Delta V_{in} = \sqrt{2I_{SS}/(\mu_n C_{ox} W/L)}$
- Previous result suggests that *Gm* falls to zero for
- As *ΔVin* exceeds a limit *ΔVin1*, one transistor carries the entire *ISS*, turning off the other
- For this *ΔVin, ID1* = $\Delta V_{in1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$ = *VGS1 – VTH* since *M2* is nearly off, thu

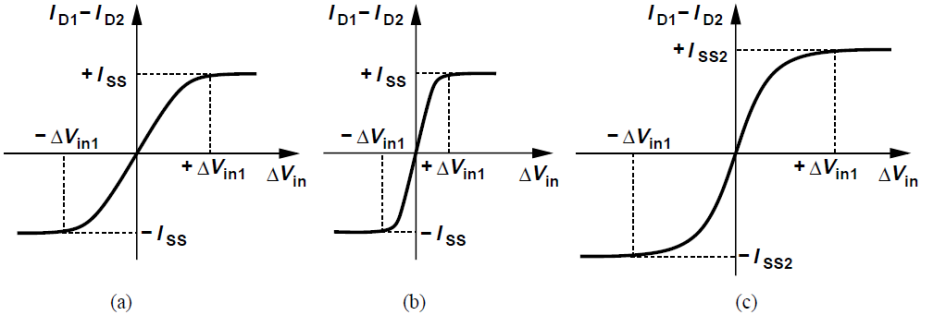
Basic Differential Pair: Large-signal Analysis



- For ***ΔVin > ΔVin1***, ***M2*** **is off and the equation derived for** ***ΔID*** **no longer holds [Fig. (a)]**

- ***Gm*** **is maximum for** ***ΔVin*** **= 0 and falls to zero for** ***ΔVin*** **=** ***ΔVin1*** **[Fig. (b)]**

Basic Differential Pair: Large-signal Analysis



- As *W/L* increases, *ΔVin1* decreases, narrowing the input range across which both devices are on [Fig. (b)]
- As *ISS* increases, both the input range and the output current swing increase [Fig. (c)]
- Intuitively, circuit becomes more linear as *ISS* increases or *W/L* decreases

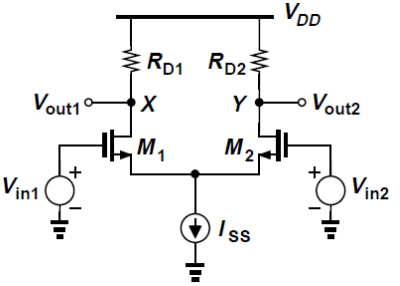
Basic Differential Pair: Large-signal Analysis

- ***ΔVin1*** **represents the maximum differential input the circuit can "handle"**
- ***ΔVin1*** **can be tied to the overdrive voltage of *M1* and *M2* in equilibrium**
- **For zero differential input, *ID1* = *ID2* = *ISS*/2, yielding**

$$(V_{GS} - V_{TH})_{1,2} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

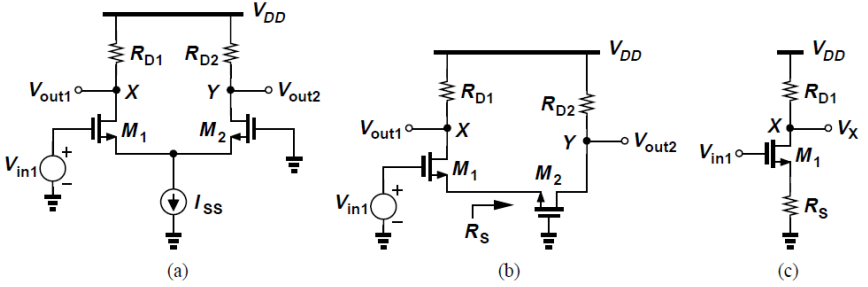
- **Thus, *ΔVin1* is equal to √2 times the equilibrium overdrive**
- **Increasing *ΔVin1* to improve linearity increases overdrive of *M1* and *M2*, which for a given *ISS* is achieved only by decreasing *W/L* and hence *gm*, thereby reducing differential gain**
- **Alternatively, *ISS* can be increases but with higher power consumption**

Basic Differential Pair: Small-signal Analysis



- Assume *M1* and *M2* are saturated and apply small-signal inputs *Vin1* and *Vin2*
- The differential gain (*Vout1* – *Vout2*)/(*Vin1* – *Vin2*) was found $\sqrt{\mu_n C_{ox} I_{SS} W/L} R_D$ from large-signal analysis
- Since each transistor carries approximately *ISS*/2 current in the vicinity of equilibrium, this expression reduces to *gmRD*
- Assume *RD1* = *RD2* = *RD*, the small-signal analysis is carried out using two methods

Basic Differential Pair: Small-signal Analysis (I)

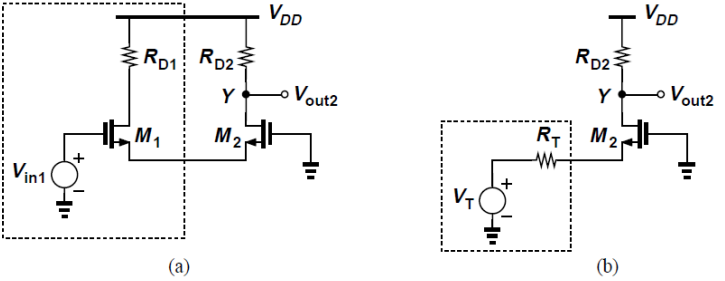


Method 1: Superposition

- First set *Vin2* = 0 and find the effect of *Vin1* at *X* and *Y*
- To find *VX*, note that *M1* forms a CS stage with a degeneration resistance equal to the impedance looking into the source of *M2*, *RS* = 1/*gm2*, neglecting channel-length modulation and body effect [Fig. (b)]
- Then from Fig. (c),

$$\frac{V_X}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

Basic Differential Pair: Small-signal Analysis (I)



Method 1: Superposition

- To find *VY*, we note that *M1* drives *M2* as a source follower and replace *Vin1* and *M1* by a Thevenin equivalent
- Thevenin voltage *VT* = *Vin1*, and resistance *RT* = *1*/*gm1*
- M2 operates as a common-gate stage, with a gain

$$\frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

Basic Differential Pair: Small-signal Analysis (I)

- From previous analysis, the overall voltage gain for *Vin1* is

$$(V_X - V_Y)|_{\text{Due to } Vin1} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in1}$$

- For *gm1* = *gm2* = *gm*, this reduces to

$$(V_X - V_Y)|_{\text{Due to } Vin1} = -g_m R_D V_{in1}$$

- By symmetry, the effect of *Vin2* at *X* and *Y* is identical to that of *Vin1* with reverse polarities

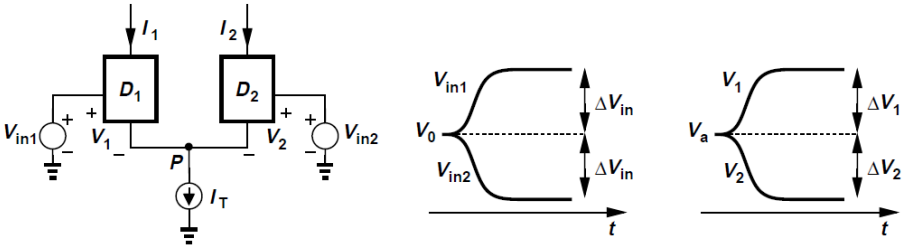
$$(V_X - V_Y)|_{\text{Due to } Vin2} = g_m R_D V_{in2}$$

- Adding the two results to perform superposition,

$$\frac{(V_X - V_Y)_{tot}}{V_{in1} - V_{in2}} = -g_m R_D$$

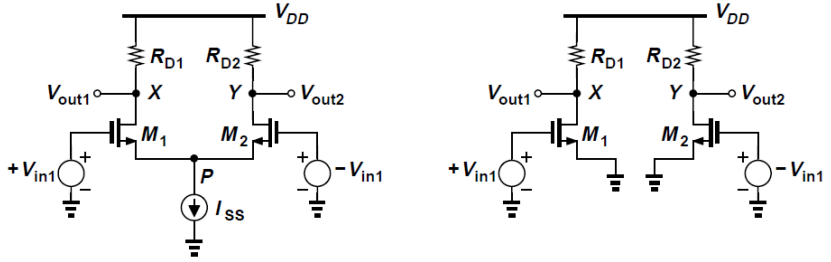
- Magnitude of gain is $g_m R_D$ regardless of how inputs are applied, halved for single-ended output

Half-Circuit Lemma/Concept



- ***D1*** **and** ***D2*** **represent any three-terminal active device in a symmetric circuit**
- **Assume** ***Vin1*** **and** ***Vin2*** **change differentially, from** ***V0*** **to** ***V0 + ΔVin*** **and from** ***V0*** **to** ***V0 – ΔVin*** **respectively**
- **If the circuit remains linear,** ***VP*** **does not change (acts as a virtual or ac ground)**
- **This is referred to as the "half-circuit concept"**

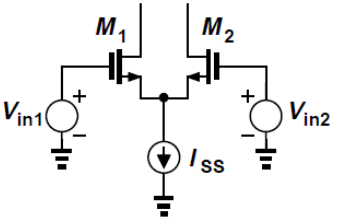
Basic Differential Pair: Small-signal Analysis (II)



- Using the half-circuit concept, *VP* experiences no change node *P* can be considered "ac ground" or virtual ground and the circuit can be decomposed into two separate halves
- We can write $V_X/V_{in1} = -g_m R_D$ and $V_Y/(-V_{in1}) = -g_m R_D$
- *Vin1* and *–Vin1* represent the voltage *change* on each side
- Thus, $(V_X - V_Y)/(2V_{in1}) = -g_m R_D$, same result as in Method 1

Half-Circuit Technique

- **The half-circuit technique can be applied even if the two inputs are not fully differential**

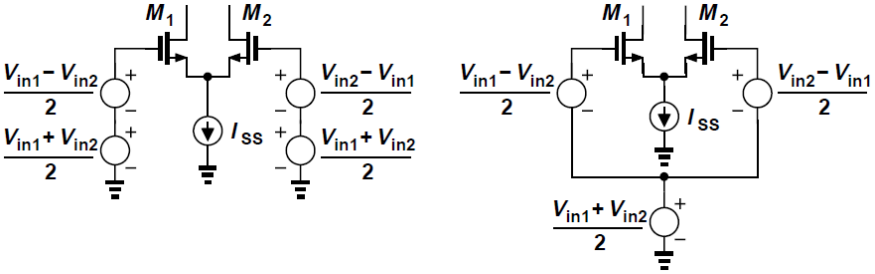


- **The unsymmetrical inputs *Vin1* and *Vin2* each can be viewed as the sum of a differential component and a common-mode component, as**

$$V_{in1} = \frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2}$$

$$V_{in2} = \frac{V_{in2} - V_{in1}}{2} + \frac{V_{in1} + V_{in2}}{2}$$

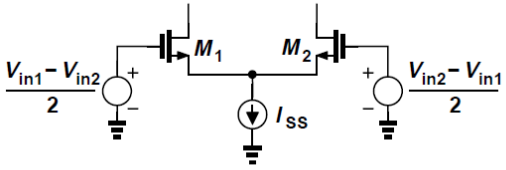
Half-Circuit Technique



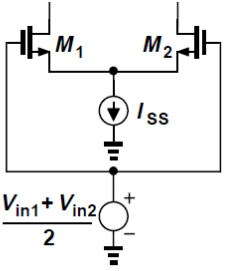
- The circuit can be visualized as shown above
- The circuit senses a combination of a differential input and a common-mode variation
- Effect of each type of input can be computed by superposition, with the half-circuit applied to the differential-mode operation

Half-Circuit Technique: Example

- **Unsymmetrical inputs *Vin1* and *Vin2* are superposed as differential [Fig. (a)] and common-mode [Fig. (b)] signals**



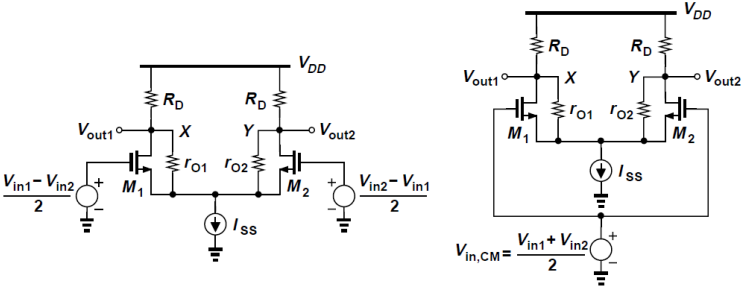
(a)



(b)

Half-Circuit Technique: Example

- For differential-mode operation, circuit reduces to Fig. (a)



- Thus,

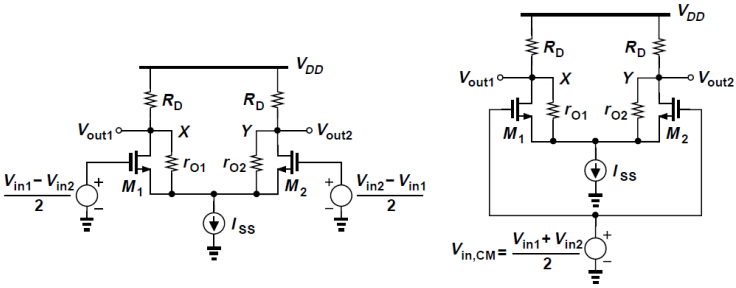
$$V_X = -g_m(R_D \| r_{O1}) \frac{V_{in1} - V_{in2}}{2}$$

$$V_Y = -g_m(R_D \| r_{O2}) \frac{V_{in2} - V_{in1}}{2}$$

$$V_X - V_Y = -g_m(R_D \| r_O)(V_{in1} - V_{in2})$$

Half-Circuit Technique: Example

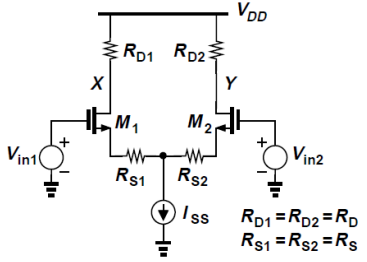
- For common-mode operation, circuit reduces to that in Fig. (b)

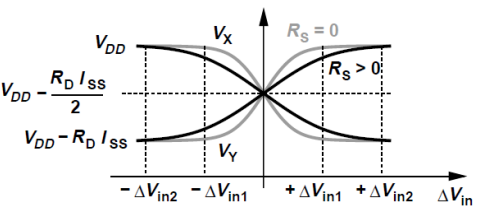


- If circuit is fully symmetric and *ISS* is an ideal current source, the currents drawn by *M1* and *M2* from *RD1* and *RD2* are exactly equal to *ISS*/2 and independent of *Vin,CM*
- *VX* and *VY* remain equal to *VDD* – *RD*(*ISS*/2) and do not vary with *Vin,CM*, therefore, circuit simply amplifies *Vin1* – *Vin2* while eliminating the effect *Vin,CM*

Degenerated Differential Pair

- **A differential pair can incorporate resistive degeneration to improve linearity [Fig. (a)]**

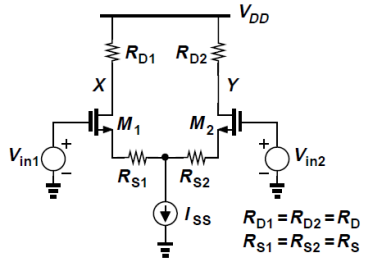


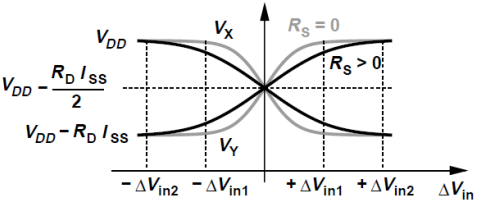


- ***RS1* and *RS2* soften the nonlinear behavior of *M1* and *M2* by increasing the differential voltage necessary to turn off one side [Fig. (b)]**
- **Suppose at *Vin1 – Vin2 = ΔVin2*, *M2* turns off and *ID1 = ISS*, then *VGS2 = VTH* and hence**

$$V_{in1} - V_{GS1} - R_S I_{SS} = V_{in2} - V_{TH}.$$

Degenerated Differential Pair





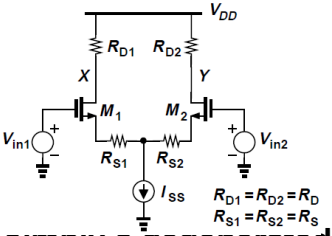
- **Thus**

$$\begin{aligned} V_{in1} - V_{in2} &= V_{GS1} - V_{TH} + R_S I_{SS} \\ &= \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} + R_S I_{SS} \end{aligned}$$

- **First term on RHS is *ΔVin1*, the input difference needed to turn off *M2* if *RS* = 0, giving** $\Delta V_{in2} - \Delta V_{in1} = R_S I_{SS}$
- **Linear input range is widened by approximately *±RSISS***

Degenerated Differential Pair

- The small-signal voltage gain can be found using the half-circuit concept



- The half-circuit is simply a degenerated CS stage exhibiting a gain of

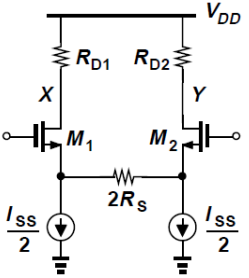
$$|A_v| = \frac{R_D}{\frac{1}{g_m} + R_S}$$

if $\lambda = \gamma = 0$

- The degenerated circuit trades gain for linearity
- *AV* is less sensitive to *gm* variations

Degenerated Differential Pair

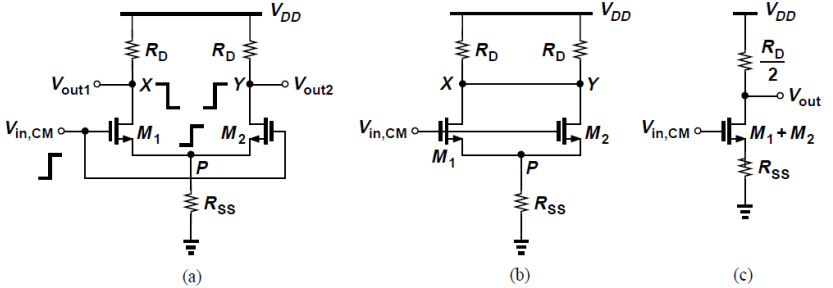
- Degeneration resistors consume voltage headroom
- In equilibrium, each resistor sustains a voltage drop of $RSISS/2$ and maximum allowable differential swing is reduced by $RSISS/2$



- This can be resolved by splitting the tail current source in half and connecting each to the source terminal
- No headroom is sacrificed across the degeneration resistance in equilibrium

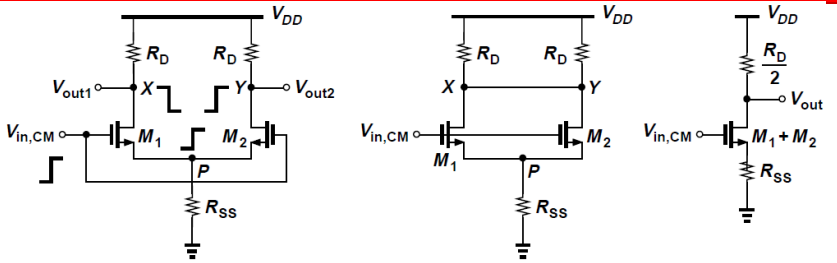
Basic Differential Pair: Common-Mode Response

- In reality, the differential pair is not fully symmetric and the tail current source exhibits a finite output impedance
- A fraction of the input CM variations appear at the output



- First assume that circuit is symmetric but tail current source has a finite output impedance *RSS* [Fig. (a)]
- Increase in *Vin,CM* causes *VP* to increase and both *VX*, *VY* to drop, which remain equal due to symmetry [Fig. (b)]

Basic Differential Pair: Common-Mode Response



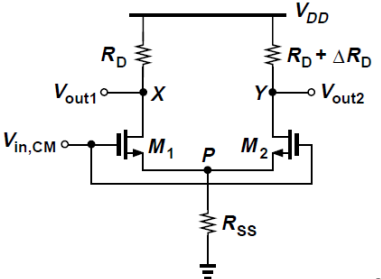
- ***M1*** **and** ***M2*** **are "in parallel" and can be reduced to one composite device with twice the width, bias current and transconductance**
- **"Common-mode gain" of the circuit is (*λ* = *γ* = 0)**

$$A_{v,CM} = \frac{V_{out}}{V_{in,CM}} = -\frac{R_D/2}{1/(2g_m) + R_{SS}}$$

- **Input CM variations disturb bias points and affect small-signal gain and output swings**

Basic Differential Pair: Common-Mode Response

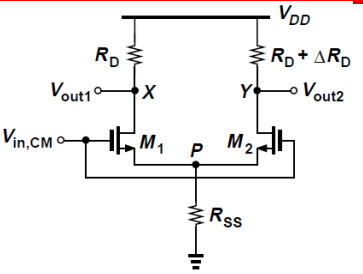
- There is variation in differential output due to change in *Vin,CM* since the circuit is not fully symmetric, i.e., slight mismatches between the two sides



- *RD1 = RD*, *RD2 = RD + ΔRD*, where *ΔRD* denotes a small mismatch and circuit is otherwise symmetric (*λ = γ = 0* for *M1* and *M2*)
- *M1* and *M2* operate as one source follower, raising *VP* by

$$\Delta V_P = \frac{R_{SS}}{R_{SS} + \dfrac{1}{2g_m}} \Delta V_{in,CM}$$

Basic Differential Pair: Common-Mode Response



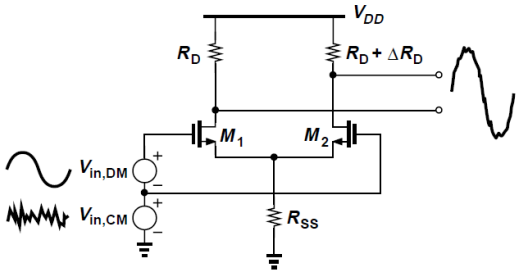
- **Since *M1* and *M2* are identical, *ID1* and *ID2* increase by** $[g_m/(1+2g_m R_{SS})]\Delta V_{in,CM}$
- ***VX* and *VY* change by different amounts**

$$\Delta V_X = -\Delta V_{in,CM}\frac{g_m}{1+2g_m R_{SS}}R_D$$

$$\Delta V_Y = -\Delta V_{in,CM}\frac{g_m}{1+2g_m R_{SS}}(R_D+\Delta R_D)$$

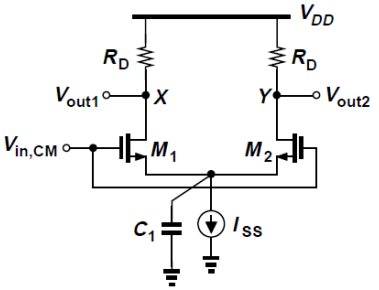
- **Common-mode change at the input introduces a differential component at the output – common-mode to differential conversion**

Basic Differential Pair: Common-Mode Response



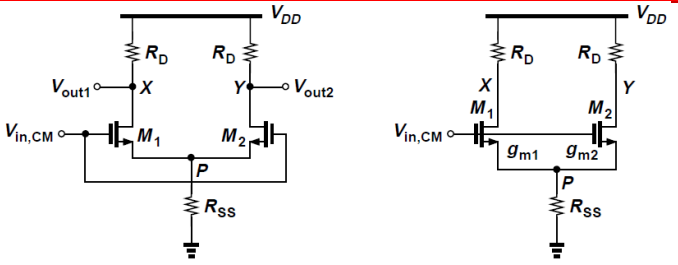
- Common-mode response depends on output impedance of tail current source and asymmetries in the circuit
- Two effects:
- Variation of output CM level (in the absence of mismatches)
- Conversion of input CM variations to output differential components (more severe)

Common-mode to differential conversion



- CM to differential conversions become significant at high frequencies since the total capacitance shunting the tail current source introduces larger tail current variations
- This capacitance is arises from parasitics of the current source and source-bulk junctions of *M1* and *M2*
- Asymmetry in the circuit stems from both the load resistors and the input transistors
- Latter contributes a greater mismatch

Common-Mode Response: Transistor Mismatch



- ***M1*** **and** ***M2*** **exhibit unequal transconductances** ***gm1*** **and** ***gm2*** **due to dimension and VTH mismatches (assume** $\lambda = \gamma = 0$**)**
- **Calculate small-signal gain from** ***Vin,CM*** **to** ***X*** **and** ***Y*** **[Fig. (b)]**

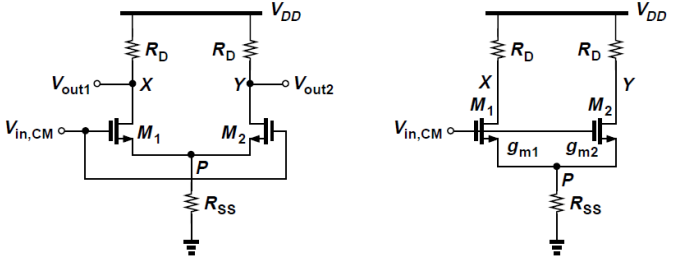
$$I_{D1} = g_{m1}(V_{in,CM} - V_P)$$

$$I_{D2} = g_{m2}(V_{in,CM} - V_P)$$

$$(I_{D1} + I_{D2})R_{SS} = V_P$$

- **Also,**

Common-Mode Response: Transistor Mismatch



- **Thus,**

$$V_P = \frac{(g_{m1} + g_{m2})R_{SS}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM}$$

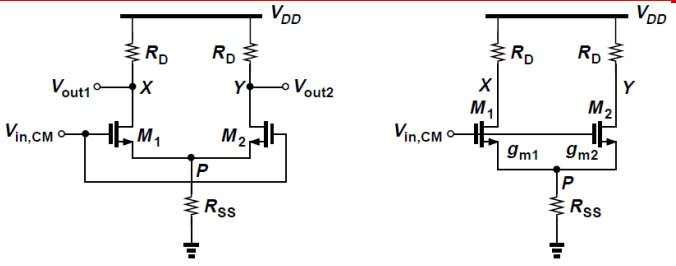
- **We now obtain the output voltages as**

$$\begin{aligned} V_X &= -g_{m1}(V_{in,CM} - V_P)R_D \\ &= \frac{-g_{m1}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM} \end{aligned} \qquad \begin{aligned} V_Y &= -g_{m2}(V_{in,CM} - V_P)R_D \\ &= \frac{-g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM} \end{aligned}$$

- **The differential component at the output is**

$$V_X - V_Y = -\frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM}$$

Common-Mode Response: Transistor Mismatch



- **The circuit converts input CM variations to a differential error by a factor of**

$$A_{CM-DM} = -\frac{\Delta g_m R_D}{(g_{m1} + g_{m2}) R_{SS} + 1}$$

- ***ACM-DM* denotes common-mode to differential-mode conversion and *Δgm = gm1 – gm2***

Common-Mode Response

- **Common-mode rejection ratio (CMRR) is defined as the desired gain divided by undesired gain**

$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

- **If only *gm* mismatch is considered, it can be shown that**

$$|A_{DM}| = \frac{R_D}{2} \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{1 + (g_{m1} + g_{m2})R_{SS}}$$

- **Hence,**

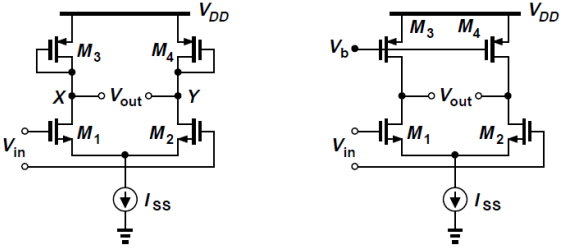
$$\begin{aligned} CMRR &= \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{2\Delta g_m} \\ &\approx \frac{g_m}{\Delta g_m}(1 + 2g_m R_{SS}), \end{aligned}$$

- ***gm* denotes the mean value, i.e., *gm* = (*gm1* + *gm2*)/2**
- **2*gmRSS* >> 1 and hence**

$$CMRR \approx 2g_m^2 R_{SS}/\Delta g_m$$

Differential Pair with MOS Loads

- Differential pairs can employ diode-connected [Fig. (a)] or current-source loads [Fig. (b)]

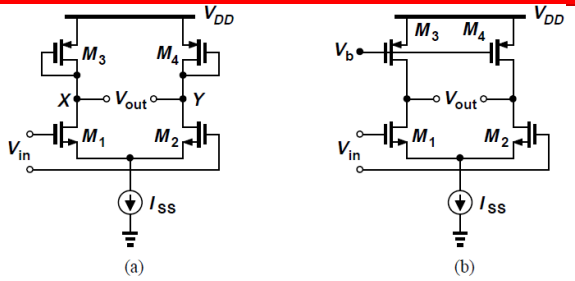


- For Fig. (a), small-signal differential gain is

$$A_v = -g_{mN}\left(g_{mP}^{-1} \| r_{ON} \| r_{OP}\right)$$
$$\approx -\frac{g_{mN}}{g_{mP}},$$

- *N* and *P* subscripts denote NMOS and PMOS respectively

Differential Pair with MOS Loads



- **Expressing *gmN* and *gmP* in terms of device dimensions,**

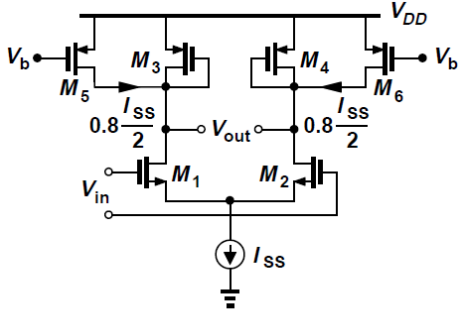
$$A_v \approx -\sqrt{\frac{\mu_n (W/L)_N}{\mu_p (W/L)_P}}$$

- **For current-source loads [Fig. (b)], the gain is**

$$A_v = -g_{mN}(r_{ON} \| r_{OP})$$

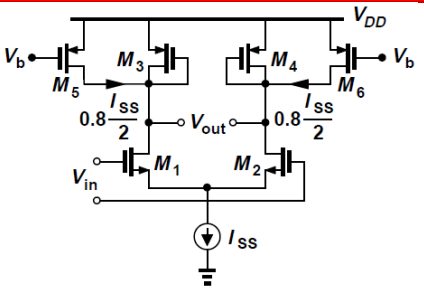
Differential Pair with MOS Loads

- Diode-connected loads consume voltage headroom and create trade-off between output voltage swing, input CM range and gain
- For higher gain, $(W/L)P$ must decrease, thereby increasing $|VGS - VTHP|$ and lowering output CM level
- Solved by adding PMOS current sources *M5* and *M6* to supply part of input pair bias current [Fig. (a)]



(a)

Differential Pair with MOS Loads

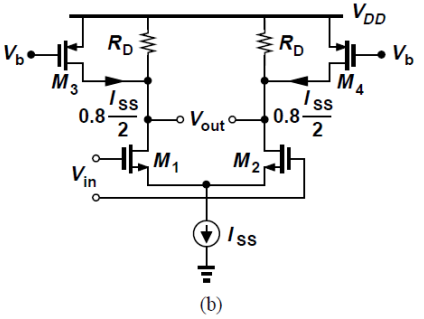


(a)

- In Fig. (a), *gm* of load devices *M3* and *M4* is lowered by reducing their current instead of (*W/L*)*P*
- For *ID5* = *ID6* = 0.8*ID1* = 0.8*ID2*, *ID3* and *ID4* are reduced by a factor of 5
- For a given overdrive, *gmP* is lowered by the same factor
- Differential gain is five times that of the case without auxiliary PMOS current sources (if $\lambda = 0$)

Differential Pair with MOS Loads

- Since diode-connected loads limit output swings, loads are realized by resistors

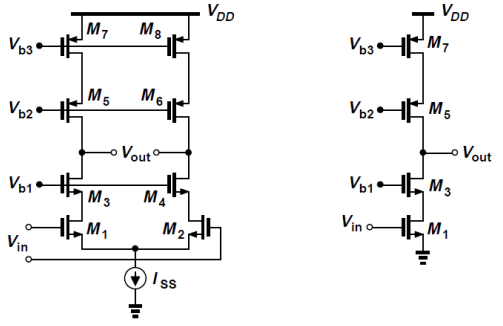


(b)

- Maximum voltage at each output node is *VDD* - |*VGS3,4* – *VTH3,4*| instead of *VDD* - |*VTH3,4*| for diode-connected loads
- For a given output CM level and 80% auxiliary currents, RD can be five times larger, yielding a voltage gain of

$$|A_v| = g_{mN}(R_D||r_{ON}||r_{OP})$$

Cascode Differential Pair

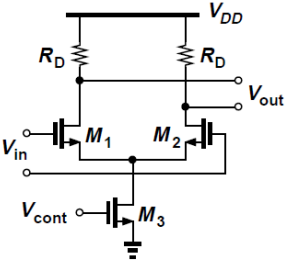


- **Small-signal voltage gain can be increased by increasing output impedance of both NMOS and PMOS devices via cascoding [Fig. (a)], but at the cost of less headroom**
- **The gain is calculated using the half-circuit technique [Fig. (b)]**

$$|A_v| \approx g_{m1}[(g_{m3}r_{O3}r_{O1})||(g_{m5}r_{O5}r_{O7})]$$

Gilbert Cell

- Differential pair whose gain is controlled by a control voltage [Fig. (a)]

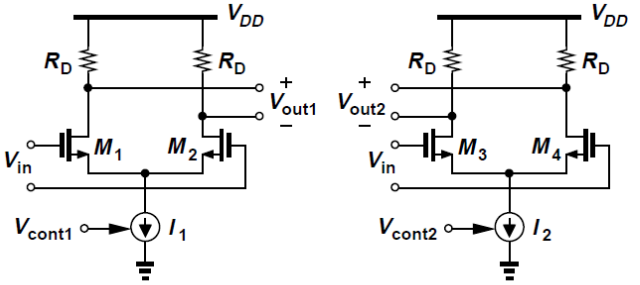


(a)

- In Fig.(a), the control voltage Vcont controls the tail current and hence the gain
- Here, *Av = Vout/ Vin* varies from zero (if *ID3* = 0)to a maximum value given by voltage headroom limitations and device dimensions
- Simple example of Variable Gain Amplifier (VGA)

Gilbert Cell

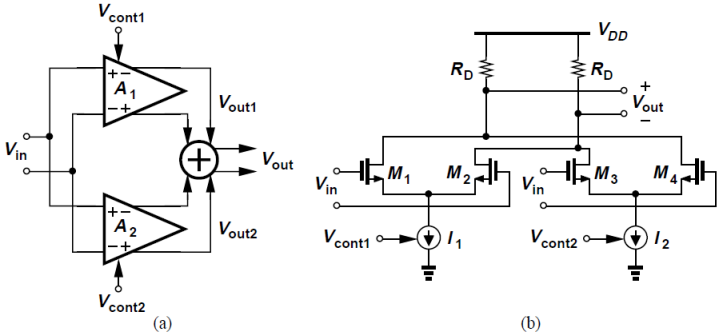
- An amplifier is sought whose gain can be continuously varied from a negative to a positive value



(b)

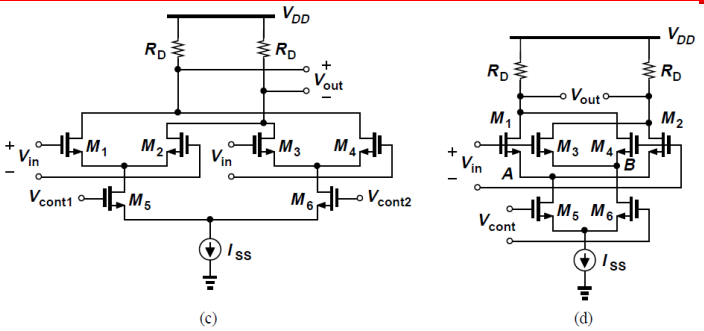
- Fig. (b) shows two differential pairs that amplify the input by opposite gains
- Here, $Vout1/Vin = -gmRD$ and $Vout2/Vin = +gmRD$
- If $I1$ and $I2$ vary in opposite directions, so do $|Vout1/Vin|$ and $|Vout2/Vin|$

Gilbert Cell



- ***Vout1*** **and** ***Vout2*** **are combined into a single output as shown in Fig. (a)**
- **The two voltages are summed , producing** ***Vout*** **=** ***Vout1*** **+** ***Vout2*** **=** ***A1Vin*** **+** ***A2Vin*****, where** ***A1*** **and** ***A2*** **are controlled by** ***Vcont1*** **and** ***Vcont2*** **respectively**
- **Actual implementation shown in Fig. (b) where drain terminals are shorted to sum the currents and generate the output voltage**

Gilbert Cell



- ***Vout1*** **and** ***Vout2*** **must change** ***I1*** **and** ***I2*** **in opposite directions so that the amplifier gain changes monotonically**
- **This is done using a differential pair, as shown in Fig. (c)**
- **For large |*Vcont1* – *Vcont2*|, all of *ISS* is steered to one of the top differential pairs and |*Vout*/*Vin*| is maximum**
- **If *Vcont1* = *Vcont2*, the gain is zero**
- **Simplified structure in Fig.(d), called a "Gilbert Cell"**