

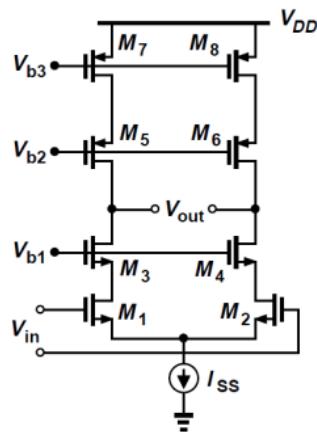
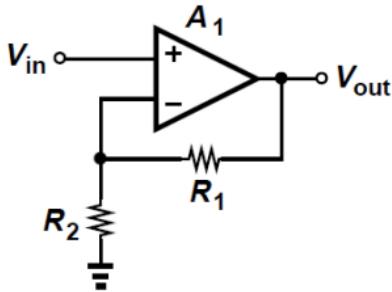
## *Chapter 9: Operational Amplifiers*

9.1 General Considerations  
9.2 One-Stage Op Amps  
9.3 Two-Stage Op Amps  
9.4 Gain Boosting  
9.5 Comparison  
9.6 Output Swing

9.7 Common Feedback  
9.8 Input Range Limitations  
9.9 Slew Rate  
9.10 High-Slew-Rate Op Amps  
9.11 Power Supply Rejection  
9.12 Noise in Op Amps

# Op Amp Definition

- We loosely define an op amp as a “high-gain differential amplifier.”
- Usually employed in a feedback system when precision is a requirement.
- Applications ranging from DC generation, high-speed amplification or filtering.



# Op Amp Design Challenge

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Three decades ago

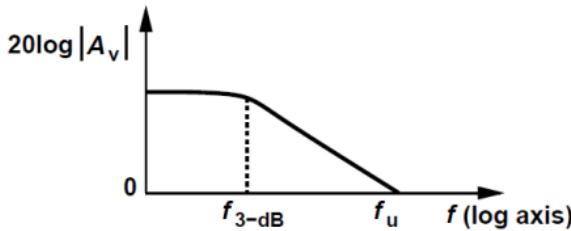
- General-purpose blocks as an “ideal” op amp
- Design effort is to satisfy an ideal op amp
  - infinite gain
  - infinite input impedance
  - zero output impedance

Today

- Design effort is to make trade-offs for a specific application, often sacrificing the unimportant aspects to improve the critical ones.
- E.g., gain error vs speed, open loop gain vs VDD

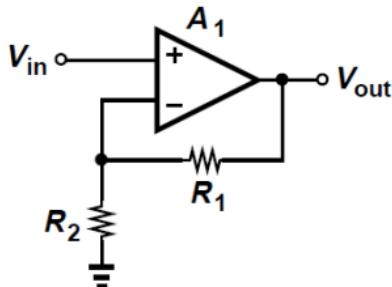
# Performance Parameter

- Gain(Precision), Bandwidth(Speed): 3-dB/f<sub>u</sub>  
Output Swing, Power dissipation
- Noise, Linearity, Supply Rejection, offset
- Input CM Range, Input/Output Impedance
- Large-Signal behavior (e.g. slew rate)



## Example 9.1

The circuit has a nominal gain of 10. i.e.,  $1+R_1/R_2=10$ .  
Determine the minimal value of  $A_1$  for a gain error 1%:



**Solution:**

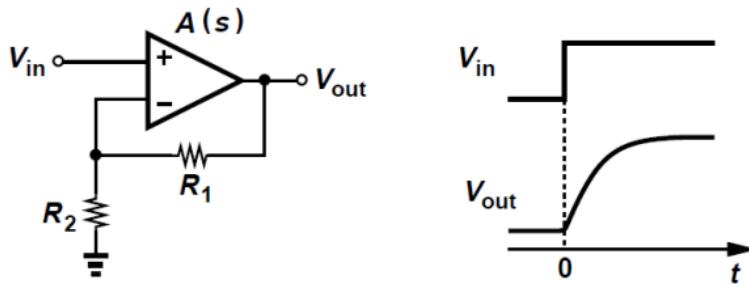
$$\begin{aligned}\frac{V_{out}}{V_{in}} &= \frac{A_1}{1 + \frac{R_2}{R_1 + R_2} A_1} \\ &= \frac{R_1 + R_2}{R_2} \frac{A_1}{\frac{R_1 + R_2}{R_2} + A_1}\end{aligned}$$

$$\frac{V_{out}}{V_{in}} \approx \left(1 + \frac{R_1}{R_2}\right) \left(1 - \frac{R_1 + R_2}{R_2} \frac{1}{A_1}\right)$$

**Thus,  $A_1 > 1000$ . Open-loop gain determines precision.**

## Example 9.2

Assume the op amp is a single-pole voltage amplifier. For a small step input, calculate the time required for the output to reach within 1% and its unity-gain bandwidth if  $1+R_1/R_2=10$  and its settling time is less than 5ns.



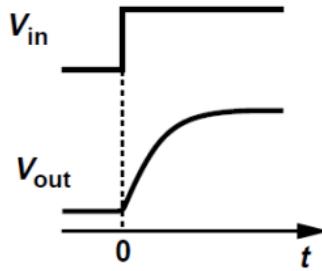
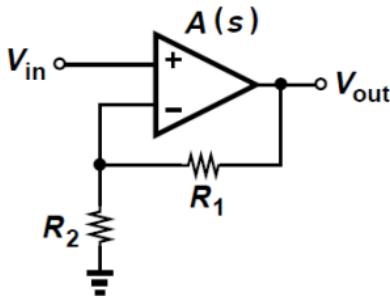
### Solution: Speed vs. Bandwidth

$$\tau \approx \left(1 + \frac{R_1}{R_2}\right) \frac{1}{A_0 \omega_0} \quad \tau \approx 1.09 \text{ ns}$$

$$1 - \exp \frac{-t_{1\%}}{\tau} = 0.99 \quad A_0 \omega_0 \approx (1 + R_1 / R_2) / \tau = 9.21 \text{ Grad/s (1.47 GHz)}$$

## Example 9.3

Explain the circuit behavior if we swap the inverting and non-inverting inputs of the op amp.



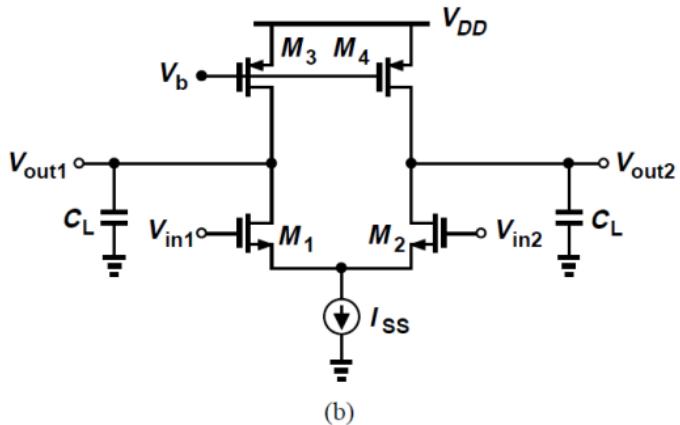
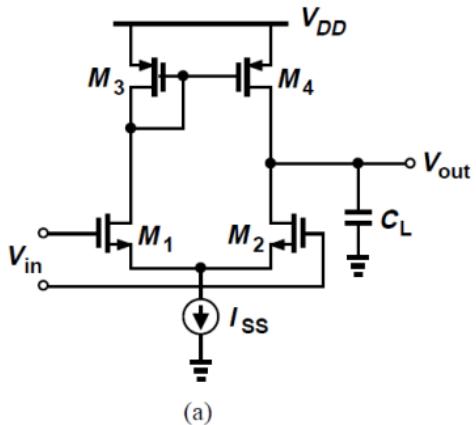
**Solution:** Positive feedback destabilizes the circuit.  
Output grows exponentially to non-linearity range.

$$\frac{V_{out}}{V_{in}}(s) = \frac{\frac{A_0}{1 - \frac{R_2}{R_1 + R_2} A_0}}{1 - \frac{\frac{R_2}{s}}{(1 + \frac{R_2}{R_1 + R_2} A_0) \omega_0}}$$

$$V_{out}(t) \approx a \left(1 + \frac{R_1}{R_2}\right) \left(\exp \frac{t}{\tau} - 1\right) u(t)$$

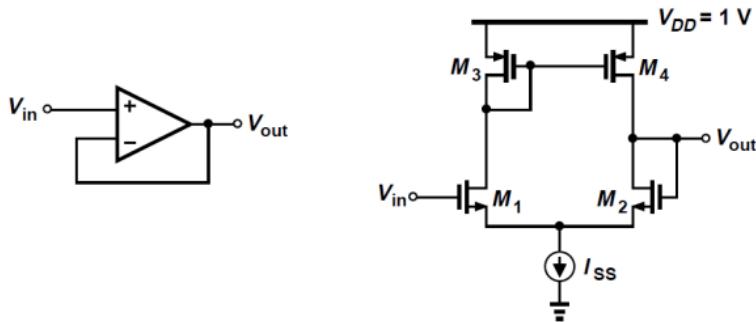
# One-Stage Op Amps

- Low-frequency gain:  $g_{mN}(r_{ON} \parallel r_{OP})$
- Bandwidth: usually proportional to  $1/(CL^*R_{out})$
- Output Swing (single-side): VDD-3Overdrive
- Mirror pole in single-ended circuit
- Power and noise: good, with four devices  $\rightarrow$  input noise



## Example 9.4

Calculate the input common-mode voltage range and the closed-loop output impedance of the unity-gain buffer.



**Solution:**

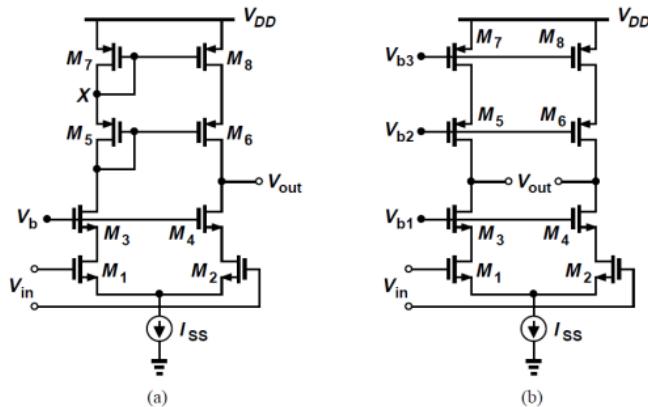
$$V_{ISS} + V_{GS1} < V_{in} < V_{in,max} = V_{DD} - |V_{GS3}| + V_{TH1}$$

**Output impedance:**  $(r_{OP} \| r_{ON}) / [g_{mN}(r_{OP} \| r_{ON})] = 1/g_{mN}$

**The closed-loop pole is independent of open-loop output impedance.**

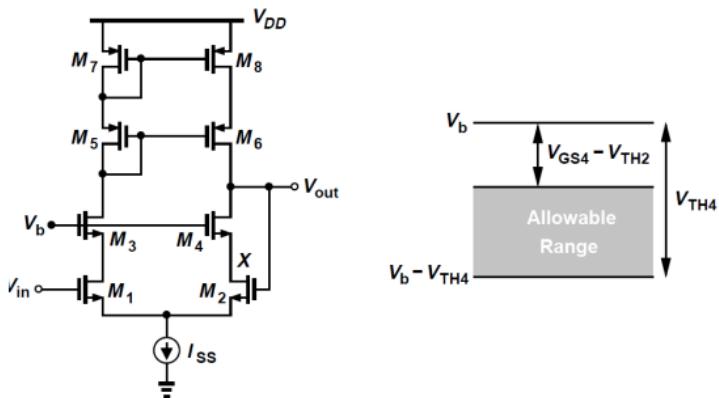
# Telescopic Cascode Op Amps

- **Low-frequency gain:**  $g_{mN}[(g_{mN}r_{ON}^2)\|(g_{mP}r_{OP}^2)]$
- **Speed:** Additional poles
- **Output Swing (single-side):** VDD-5Overdrive
- **Mirror pole in single-ended**
- **Difficult to short telescopic op amp output to input**
- **Power and noise:** good, input noise mainly has four devices contribution



## Example 9.5

For this unity-gain buffer configuration, explain in which region each transistor operates as  $V_{in}$  varies from below  $V_b - V_{GS4} + V_{TH2}$  to above  $V_b - V_{TH4}$



**Solution: Remedy in switched-capacitor circuit**

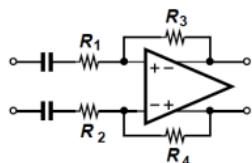
**When  $V_{in} < V_b - V_{TH4}$ ,  $M_4$  is in triode, others are saturated;**

$V_b - V_{TH4} < V_{in} < V_b - (V_{GS4} - V_{TH2})$   **$M_2$ ,  $M_4$  are saturated;**

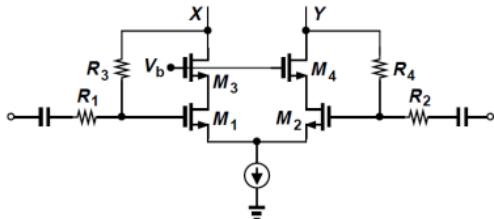
$V_{in} > V_b - (V_{GS4} - V_{TH2})$   **$M_2$ ,  $M_1$  in triode,  $M_4$  is in saturation.**

## Example 9.6

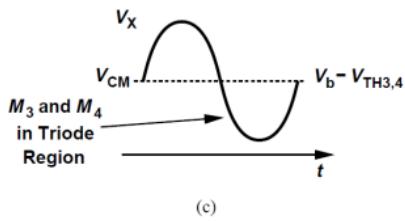
Assuming that the op amp has a high open-loop gain, determine the maximum allowable output swing.



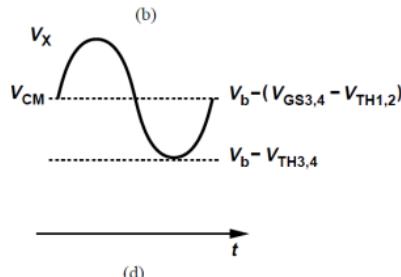
(a)



(b)



(c)



(d)

**Solution:**  $\pm(\text{one threshold-one overdrive})$

# Telescopic Cascode Op Amps Design

- Generally, power budget determines branch current
- Gain and Output voltage swing
- Deal with  $I_D$ ,  $V_{GS} - V_{TH}$ ,  $W/L$ ,  $g_m$  and  $r_O$

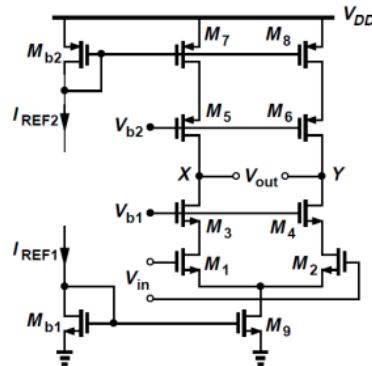
## Design Procedure (Example 9.7)

- Define drain current
- Distribute overdrive voltage
- Calculate the aspect ratio

$$I_D = (1/2)\mu C_{ox}(W/L)(V_{GS} - V_{TH})^2$$

~~-Calculate the gain with Lmin~~

- Iteration by increasing W,L until achieving gain criterion
- Finally, DC bias voltage setup and exam residual goals
- CMFB is necessary



$$g_m r_O = \sqrt{2\mu C_{ox}(W/L)I_D}/(\lambda I_D)$$

PMOS>Cascode\_N>Input\_N

- How to modify design if power budget is different while all the other specifications are the same?
- Only scale the widths of all the transistors while keeping the lengths constant.

## Example 9.6

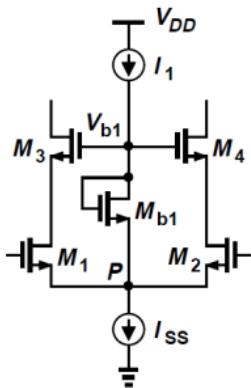
Explain what aspects of the performance degrade for a low-power op amp design when we scale down the transistor width.

### Solution:

- (1)The speed of the op amp in driving a capacitive load
- (2)The input-referred noise voltage rises by a square root factor of scale constant. (for input device)

# Gate Bias Voltage Generation

- Ensure bias voltage to track the input CM level
- Choose Mb1 to be a narrow, long, “weak” device



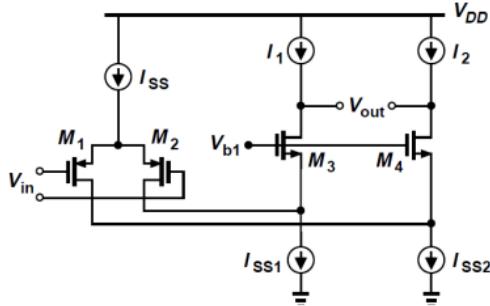
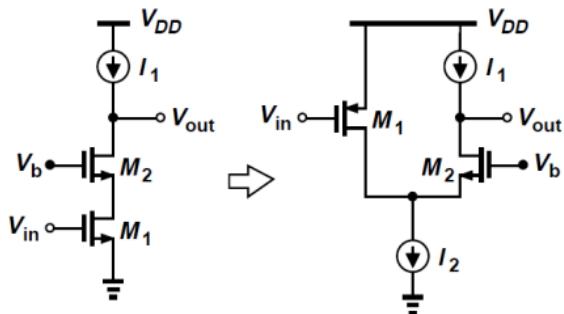
$$V_{b1} = V_P + V_{GS,b1}$$

$$V_{GS,b1} = (V_{GS1,2} - V_{TH1,2}) + V_{GS3,4}$$

# Folded Cascode Op Amps

## Recall Folded Cascode

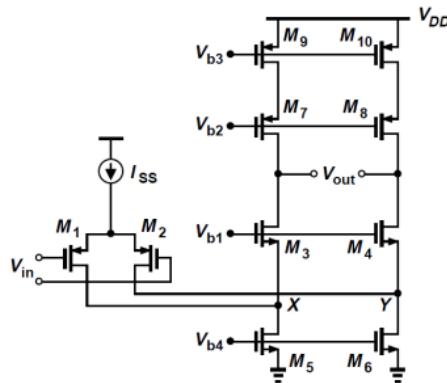
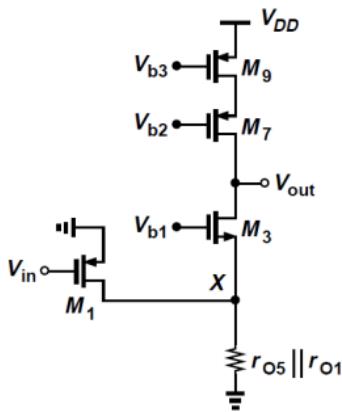
- Not “stack” the cascode transistor on the input device
- Consume higher power
- Output Voltage Swing:  $V_{DD} - 4$  overdrive
- Output and input could short together



# Folded Cascode Voltage Gain

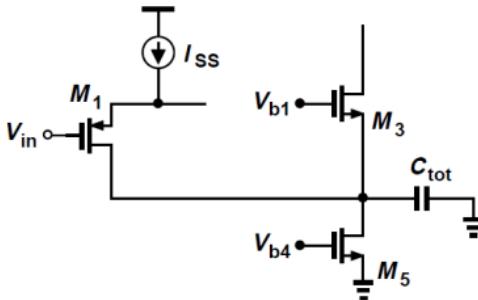
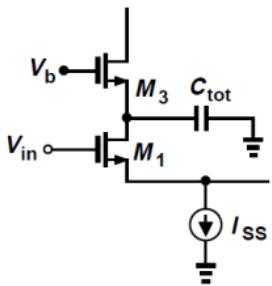
$$|A_v| = G_m R_{out}$$

- Since  $(g_{m3} + g_{mb3})^{-1} \| r_{O3} \ll r_{O1} \| r_{O5}$ , thus  $G_m \approx g_m$
- $|A_v| \approx g_m \{ [(g_{m3} + g_{mb3})r_{O3}(r_{O1}\|r_{O5})] / [(g_{m7} + g_{mb7})r_{O7}r_{O9}] \}$
- Two or three times lower than a telescopic topology



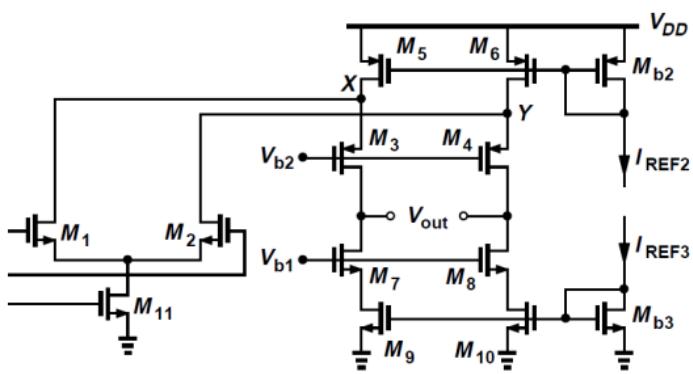
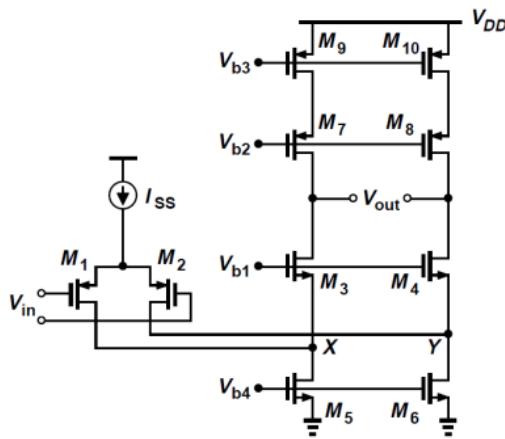
## Effect capacitance on the nondominant pole

- At “folding point”, a large capacitance due to a large current device M5 would be added to the total capacitance.



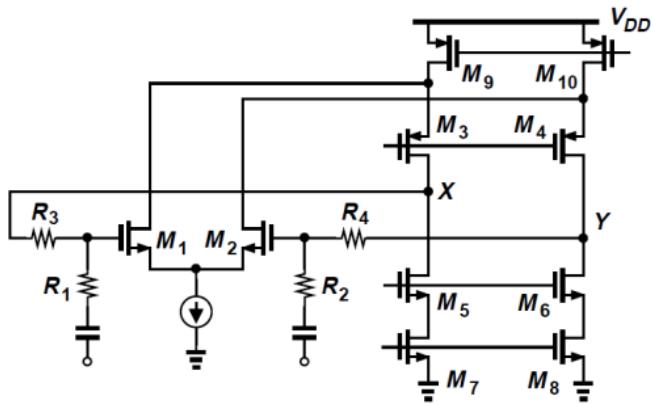
# NMOS vs. PMOS input

- Greater mobility from NMOS input leads to higher gain
- Lowering the pole at folding point
- PMOS input is less sensitive to flicker noise(wider WL)



# Folded Cascode Properties

- Slighter Higher Output Swing than telescopic
- Higher Power dissipation, lower voltage gain, lower pole frequency and higher noise
- Input and output can be shorted: 2overdrive from bound
- A better input CM range



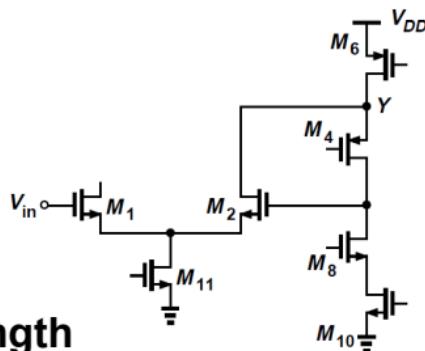
## Example 9.9

Design a folded-cascode op amp with an NMOS pair.

Specifications:  $V_{DD} = 3V$ , differential output swing =  $3V$ ,  
Power dissipation =  $10mW$ , voltage gain =  $2000$ .

**Solution:**

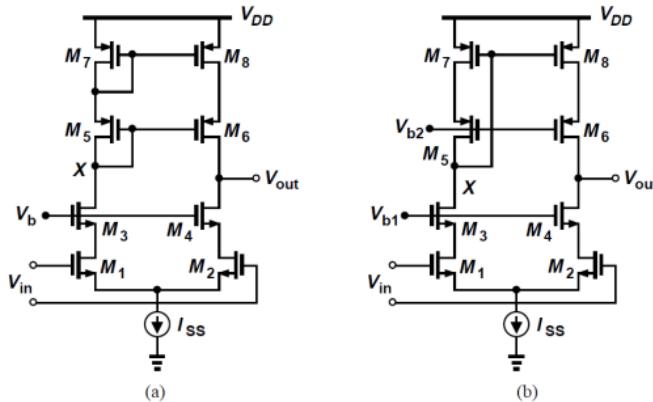
- (1) Current allocation
- (2) Overdrive voltage allocation
- (3) Aspect ratio calculation
- (4) Small-signal gain with minimal length
- (5) Iteration by increase  $M_5/M_1/M_4$  in turns



Note that the folding point capacitance may limit here.

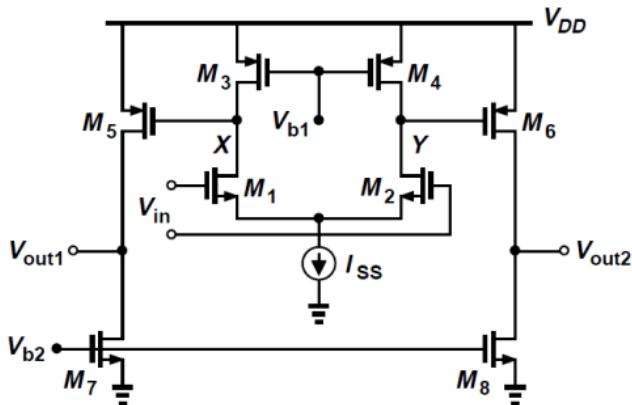
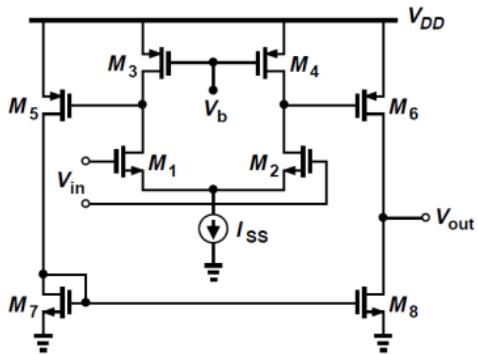
# Low Voltage Single-ended Output

- M7 is biased at the edge of triode  
Could M5 always in saturation?
- Left implementation wastes one threshold voltage
- Still, single-ended output is unfavorable due to half output swing and a mirror pole
- Note that almost all the differential output circuits need a CMFB



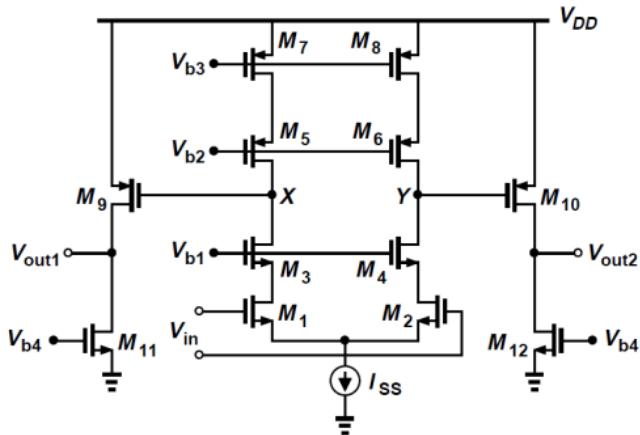
# Two-Stage Op Amps

- Voltage headroom in today's design is constrained with low supply voltage and large output swing
- Gain:**  $g_{m1,2}(r_{O1,2}||r_{O3,4}) g_{m5,6}(r_{O5,6}||r_{O7,8})$
- Output Swing:** Vdd-2Overdrive



# Two-Stage Op Amps with cascode devices

- Voltage headroom in today's design is constrained with low supply voltage and large output swing
- Gain:  $A_v \approx \{g_{m1,2}[(g_{m3,4} + g_{mb3,4})r_{O3,4}r_{O1,2}]\|[(g_{m5,6} + g_{mb5,6})r_{O5,6}r_{O7,8}]\}$   
 $\times [g_{m9,10}(r_{O9,10}\|r_{O11,12})].$
- Can we have more stages? Feedback stability limits



# Two-Stage Op Amps Design

## Example 9.10

Design the two-stage op amp for  $VDD = 1V$ ,  $P = 1mW$ , a differential output swing of 1 Vpp, and a gain of 100.

**Solution:**

(1) Current allocation

(2) Voltage allocation:

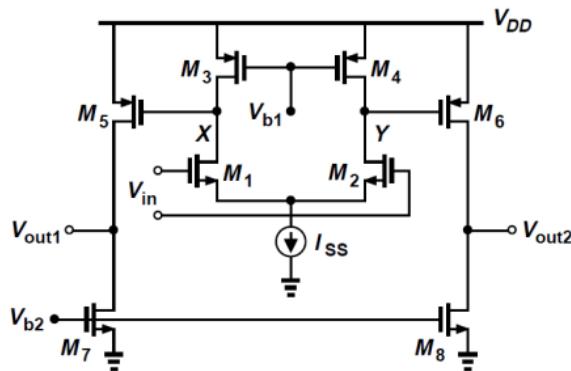
300mV to M7, 200mV to M5,

400mV to M3, 100mV to M1

(noise and gm consideration)

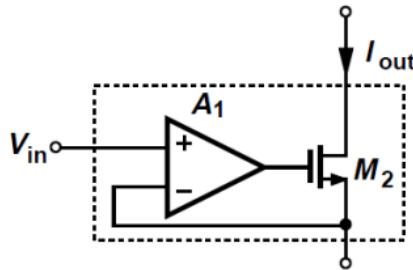
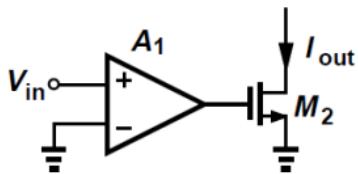
(3) Calculate aspect ratio

(4) Calculate gain > 2000



# Gain Boosting

- Increase the output impedance without adding more cascode devices. But how?
- A transistor preceded by an ideal voltage amplifier exhibits a transconductance of  $gmA_1$  and a output resistance of  $r_o$ .

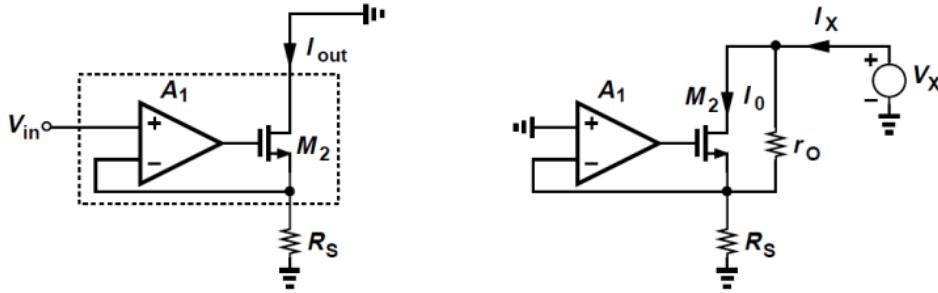


# Gain Boosting

- Increase the output impedance without adding more cascade devices. But how?
- First Perspective:  
**A degenerated transistor preceded by an ideal voltage amplifier**

$$\frac{I_{out}}{V_{in}} = \frac{A_1 g_m}{1 + (A_1 + 1)g_m R_S}, \quad R_{out} = r_O + (A_1 + 1)g_m r_O R_S + R_S.$$

In fact, the output resistance is “boosted. The headroom is similar to a simple degenerated transistor



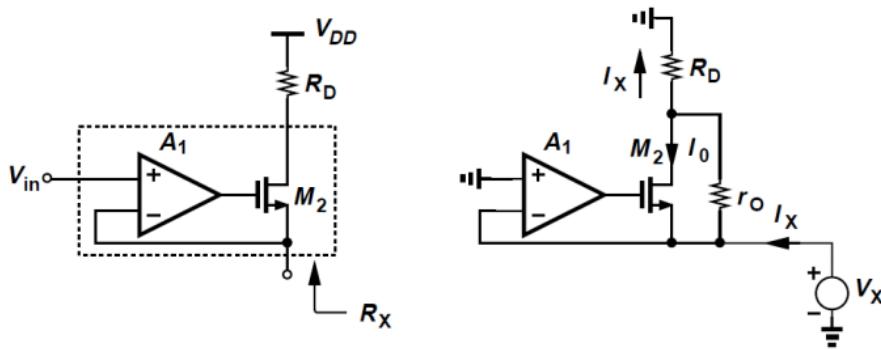
# Example 9.11

Determine the resistance seen at the source of M<sub>2</sub> without considering body effect.

**Solution:**

$$\frac{I_X R_D - V_X}{r_O} + (-A_1 V_X - V_X) g_m + I_X = 0$$

$$R_X = \frac{R_D + r_O}{1 + (A_1 + 1)g_m r_O}$$

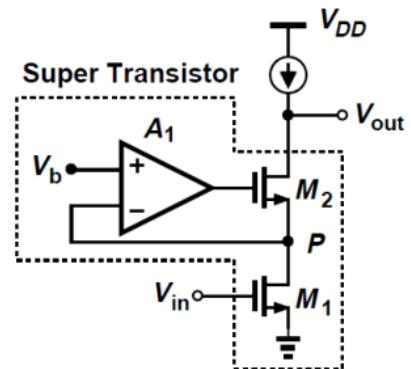


# Basic gain-boosted stage

- Current-Voltage feedback increase the output impedance by a factor of  $A_1 + 1$ , while the real  $g_m$  raised by  $A_1$  is reduced by  $A_1 + 1$  when feedback is applied.

- **R<sub>out</sub>:**  $R_{out} = r_O + (A_1 + 1)g_m r_O R_S + R_S$ .
- **G<sub>m</sub>:**  $g_m \dots \dots \dots \dots \dots \dots \dots$
- **R<sub>p</sub>:** (look above P, see example 9.11)

$$(r_{O2}/[1 + (A_1 + 1)g_{m2}r_{O2}]) \approx [(A_1 + 1)g_{m2}]^{-1}$$

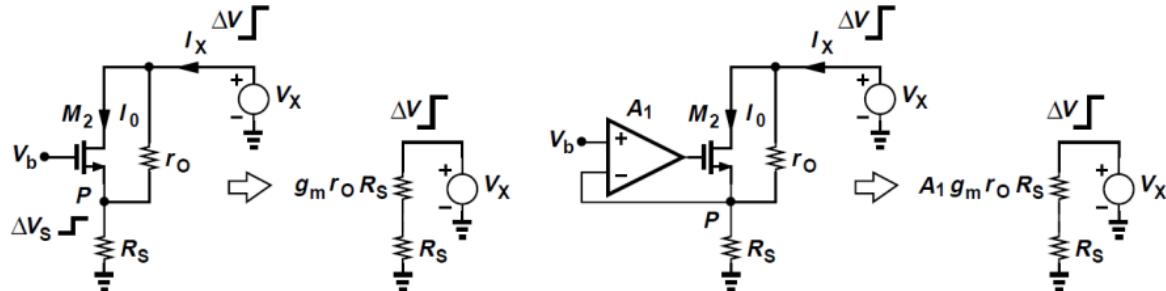


$$\begin{aligned}|A_v| &\approx g_{m1}[r_{O2} + (A_1 + 1)g_{m2}r_{O2}r_{O1} + r_{O1}] \\ &\approx g_{m1}g_{m2}r_{O1}r_{O2}(A_1 + 1).\end{aligned}$$

# Regulated Cascode

## Second Perspective

- Loosely view the voltage change divided by  $R_s$  and  $g_m r_o R_s$ .
- Drain current response can be suppressed as
  - $V_p$  is constant
  - Current through  $R_s$  is constant
- $V_p$  is “pinned” to  $V_b$  by feedback regulation.



## Example 9.12

Determine the small-signal values of  $V_P$ ,  $V_G$ ,  $I_0$ , and  $I_{ro}$ .  
Assume  $(A_1 + 1)g_m r_O R_S$  is large.

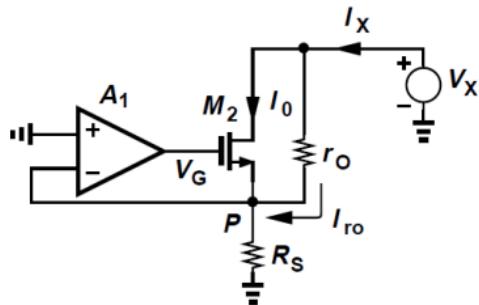
**Solution: Current circulates M2**

$$V_X = [r_O + (A_1 + 1)g_m r_O R_S + R_S] I_X$$

$$\begin{aligned} V_P &= I_X R_S \\ &= \frac{R_S}{r_O + (A_1 + 1)g_m r_O R_S + R_S} V_X. \end{aligned}$$

$$\begin{aligned} V_G &= -A_1 V_P \\ &= \frac{-A_1 R_S}{r_O + (A_1 + 1)g_m r_O R_S + R_S} V_X \end{aligned}$$

$$V_G - V_P \approx -V_X / (g_m r_O).$$



$$I_0 \approx -V_X / r_O$$

$$\begin{aligned} I_{ro} &= \frac{V_X - V_P}{r_O} \\ &= \frac{r_O + (A_1 + 1)g_m r_O R_S}{r_O + (A_1 + 1)g_m r_O R_S + R_S} \frac{V_X}{r_O} \\ &\approx \frac{V_X}{r_O}. \end{aligned}$$

# **Gain boosting Key**

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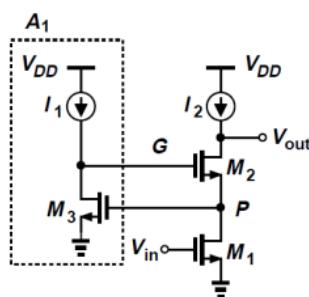
- The amplifier boosts the gm of the cascode device
- The amplifier regulates the output current by monitoring and pinning the source voltage

# Gain Boosting Circuit Implementation

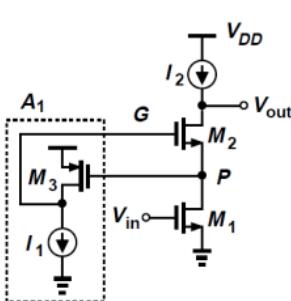
- Simplest a common-source stage

$$|V_{out}/V_{in}| \approx g_m r_{O1} g_m r_{O2} (g_m r_{O3} + 1)$$

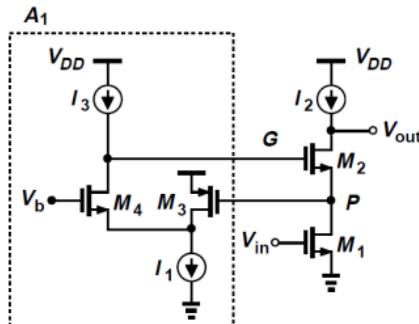
- Avoid headroom limitation, PMOS common-source stage is better, but M3 could go in triode
- Folded-cascode inserts one more stage



(a)



(b)



(c)

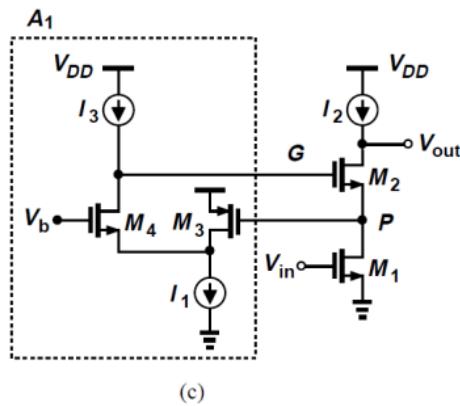
# Example 9.13

Determine the allowable range for  $V_b$ .

**Solution:**

$$V_{b,min} = V_{GS4} + V_{I1}$$

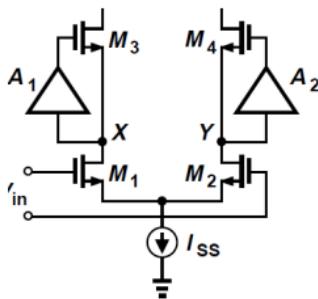
$$V_{b,max} = V_{GS2} + V_P + V_{TH4}$$



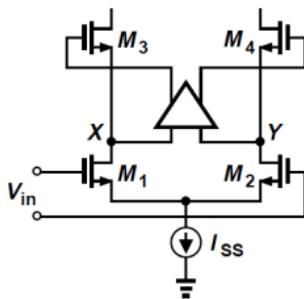
(c)

# Gain Boosting with a Differential Pair

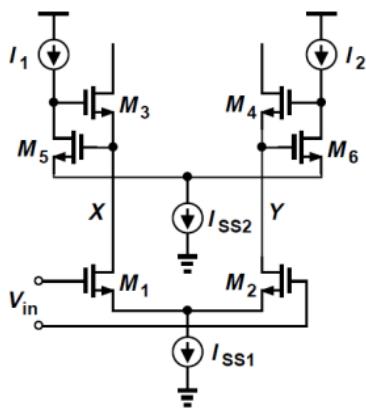
- One threshold higher than a simple differential circuit
- Merge two gain boosting blocks to differential one



(a)



(b)



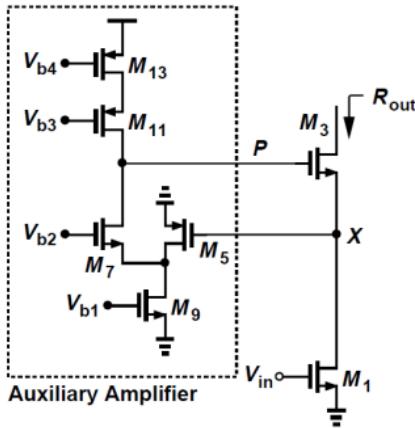
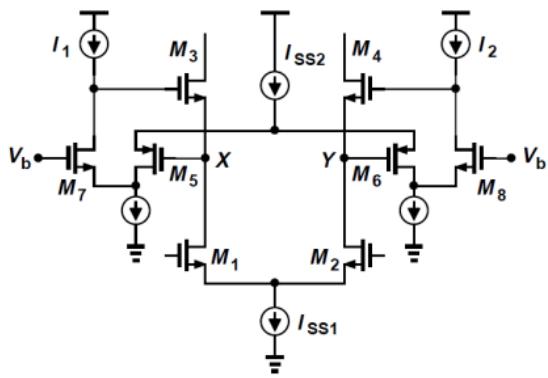
(c)

# Differential Folded Cascode Gain Boosting

- The minimal allowable  $V_x, V_y$  is  $V_{OD12} + V_{ISS1}$
- The output impedance of the circuit (Example 9.14)

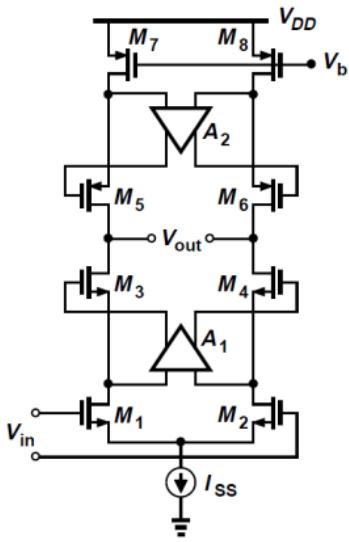
$$R_{out1} \approx [g_{m7}r_{O7}(r_{O9}\|r_{O5})]\|(g_{m11}r_{O11}r_{O13})$$

$$R_{out} \approx g_{m3}r_{O3}r_{O1}g_{m5}R_{out1}$$

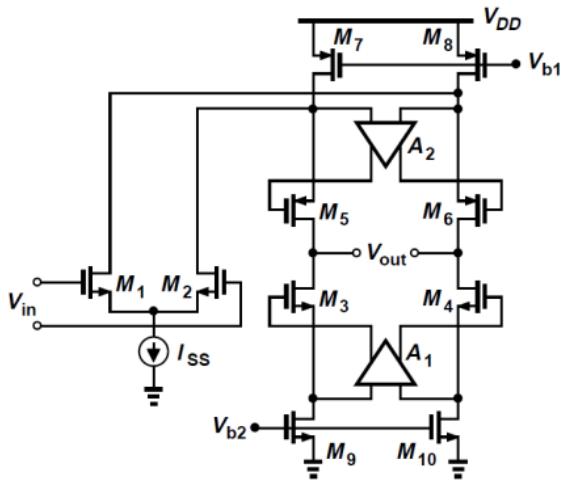


# Gain Boosting in Signal Path and Load

- Gain boosting can be utilized in the load current source
- To allow maximum swings, A2 employs NMOS-input.

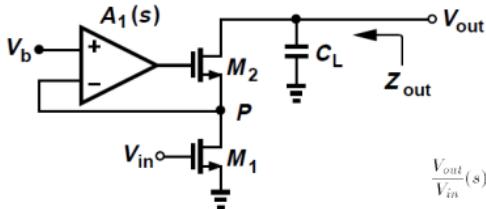


(a)



(b)

# Gain Boosting Frequency Response



$$G_m(s) = g_{m1} \frac{r_{O1}}{r_{O1} + \frac{r_{O2}}{1 + (A_1 + 1)g_{m2}r_{O2}}}$$

$$Z_{out} = [r_{O1} + (A_1 + 1)g_{m2}r_{O2}r_{O1} + r_{O2}] \parallel \frac{1}{C_L s}$$

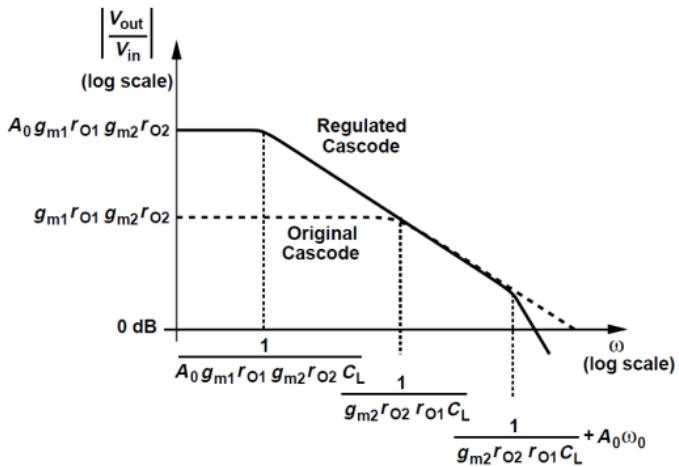
$$V_{out}(s) = \frac{-g_{m1}r_{O1}[(1 + g_{m2}r_{O2})\frac{s}{\omega_0} + (A_0 + 1)g_{m2}r_{O2} + 1]}{(r_{O1} + r_{O2})C_L [1 + g_{m2}(r_{O2}||r_{O1})]s^2 + [(r_{O1} + r_{O2})C_L + (A_0 + 1)g_{m2}r_{O2}r_{O1}C_L + \frac{1}{\omega_0}]s + 1}$$

- **Zero:**  $|\omega_z| \approx (A_0 + 1)\omega_0$
- **Dominant pole:**  $|\omega_{p1}| = \frac{1}{[r_{O1} + (A_0 + 1)g_{m2}r_{O2}r_{O1} + r_{O2}]C_L + \frac{1}{\omega_0}}$   
 $\approx \frac{1}{A_0 g_{m2}r_{O2}r_{O1}C_L}$ .
- **Non-dominant pole: Above the original-3dB bandwidth**

$$|\omega_{p2}| = \frac{[r_{O1} + (A_0 + 1)g_{m2}r_{O2}r_{O1} + r_{O2}]C_L + \frac{1}{\omega_0}}{\frac{(r_{O1} + r_{O2})C_L}{\omega_0} [1 + g_{m2}(r_{O1}||r_{O2})]}$$
$$\approx (A_0 + 1)\omega_0 + \frac{1}{g_{m2}r_{O2}r_{O1}C_L},$$

# Frequency Response Bode Plot

- Gain boosting frequency response bode plot
- Two poles, non-dominant is below the original 3dB pole



## Example 9.15

**Is the dominant-pole approximation valid here.**

**Solution:**

$$\begin{aligned}\frac{\omega_{p2}}{\omega_{p1}} &\approx \left[ (A_0 + 1)\omega_0 + \frac{1}{g_{m2}r_{O2}r_{O1}C_L} \right] \left[ (A_0 + 1)g_{m2}r_{O2}r_{O1}C_L + \frac{1}{\omega_0} \right] \\ &\approx (A_0 + 1)^2 g_{m2}r_{O2}r_{O1}C_L \omega_0 + 2(A_0 + 1) + \frac{1}{g_{m2}r_{O2}r_{O1}C_L \omega_0}.\end{aligned}$$

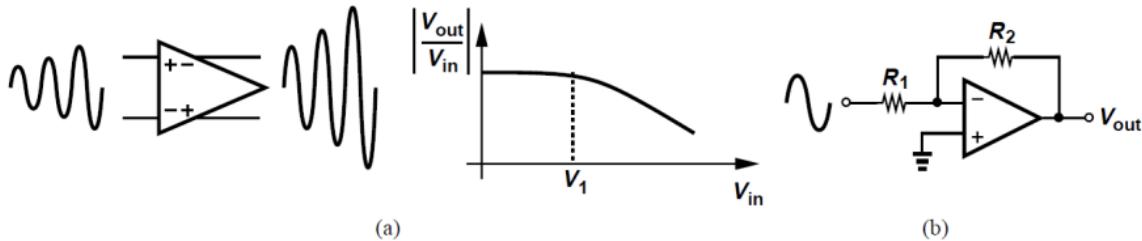
**The system has two poles near unity and the approximation is valid.**

# Comparison

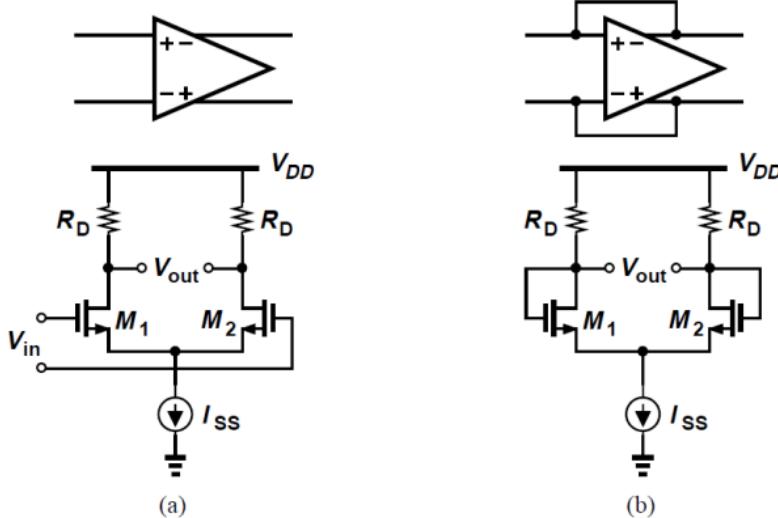
	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

# Output Swing Calculation

- Be careful about distortion and gain error
- The maximum output amplitude that yields an acceptable distortion or gain error
- Apply a growing sinusoid wave, monitor the resulting output, and calculate the maximum allowable gain



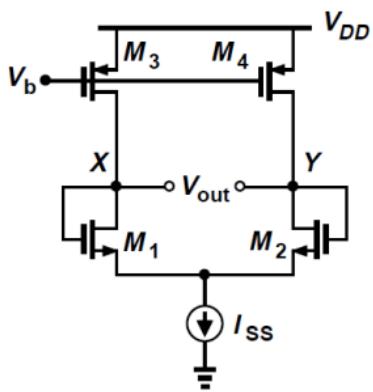
# Common-Mode Feed Back



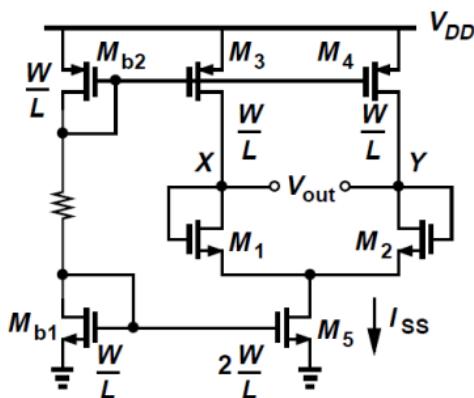
- **$V_{cm(in)}$  and  $V_{cm(out)}$ :**  $V_{DD} - I_{ss}R_D/2$

# Basic Concepts

- In fully-differential op amps, the output CM level is usually not well defined.
  - Case 1:  $I_{D3,4} < I_{SS}/2$ ,  $V_x, V_y$  decreases,  $I_{SS}$  triode;
  - Case 2: In reverse,  $V_x, V_y$  increases,  $M_3, M_4$  triode.



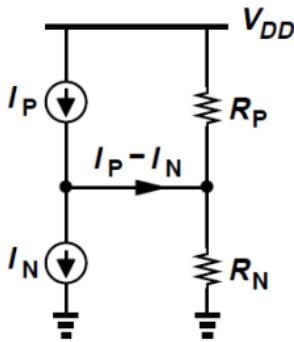
(a)



(b)

# Basic Concepts

- In high-gain amplifiers, CMFB balances the PMOS and NMOS current mismatches, thus avoid driving one of them into triode region.
- Differential feedback cannot define CM level
- In simulation, CM may be well-defined around half VDD, yet in real world, random mismatches and device variations would degrade CM easily without CMFB.



## Example 9.16

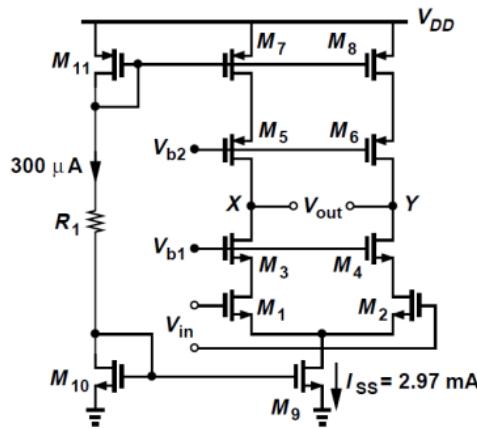
Consider the telescopic op amp below. Suppose M9 suffers from a 1% current mismatch with respect to M10, producing  $I_{ss} = 2.97 \text{ mA}$  rather than  $3 \text{ mA}$ . Assuming perfect matching for the others. Explain what happens in the circuit.

**Solution:**

**Output voltage error:**  $(I_P - I_N)(R_P \parallel R_N) = 3.99 \text{ V}$

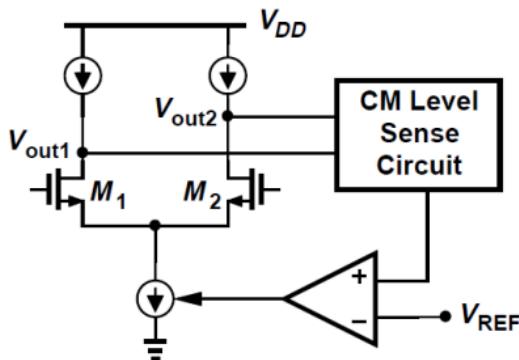
**Vx, Vy must rise so much that  
M5, M6, M7, M8 go to triode,  
yielding  $ID7 = 1.485 \text{ mA}$ .**

**Current mismatch is largely depended on different drain-source voltage.**



# Conceptual topology

- Measure output CM level;
- Compare with a reference;
- Apply the error to correct the level.



# CM Sensing Techniques

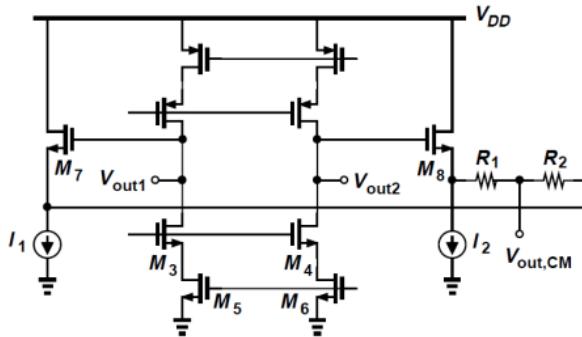
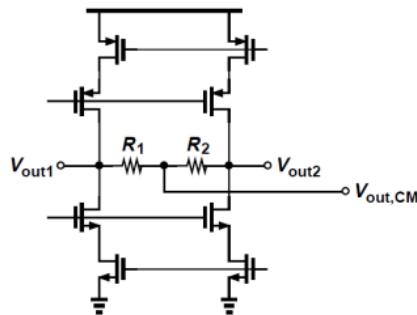
- **Resistive sensing**

$$V_{out,CM} = (R_1 V_{out2} + R_2 V_{out1}) / (R_1 + R_2)$$

- large  $R_1, R_2$  to avoid loading effect
- large chip area and parasitic capacitance
- reduce frequency performance

- **Source follower sensing**

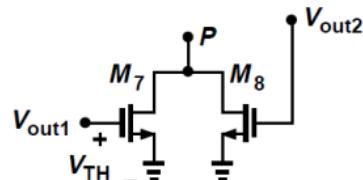
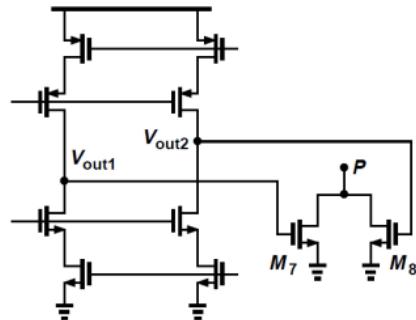
- lose one  $V_{th}$  in swing
- large  $R_1, I_1$  to avoid “starved”



# CM Sensing Techniques

- Capacitive sensing
- Switched-capacitor
- Deep triode sensing
  - $R_{tot} \sim v_{out1} + v_{out2}$
  - $R_{tot}$  has no relationship with differential voltage
  - may go to saturation region

$$\begin{aligned} R_{tot} &= R_{on7} || R_{on8} \\ &= \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{out1} - V_{TH})} \parallel \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{out2} - V_{TH})} \\ &= \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{out2} + V_{out1} - 2V_{TH})}, \end{aligned}$$

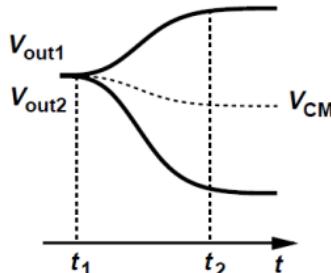


## Example 9.17

A student simulates the step response of a closed-loop op amp circuit and observes the output waveforms shown in below. Explain why  $V_{out1}$  and  $V_{out2}$  do not change symmetrically.

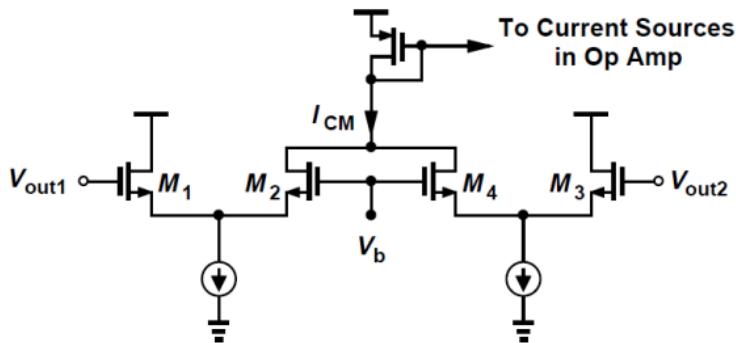
**Solution:**

As evident from waveforms, the output CM levels change from  $t_1$  to  $t_2$ , indicating CM sensing mechanism is nonlinear. For example, if M7 or M8 in last slide does not enter deep triode at  $t_2$ , the CM level would change because now it is a function of differential output.



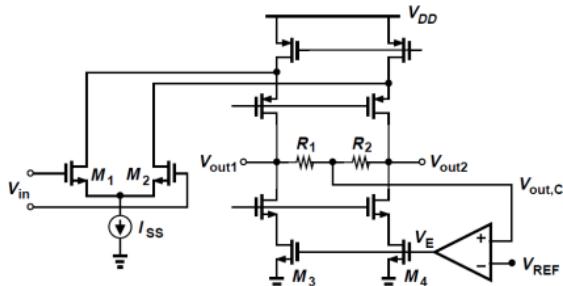
# CM Sensing Techniques

- Differential pair sensing
  - $I_{CM} \propto V_{out1} + V_{out2}$  by small signal analysis
  - Under Large swings situation, sensing is not valid due to large non-linearity.

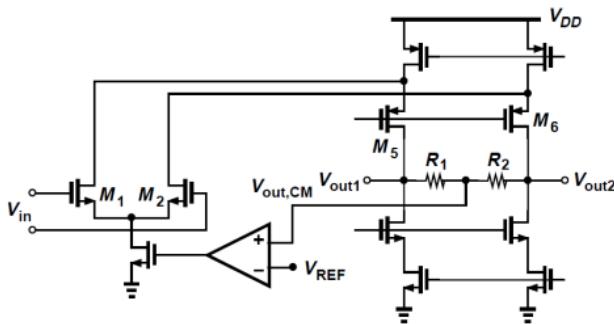


# CM Feedback Techniques

- Control cascade current source



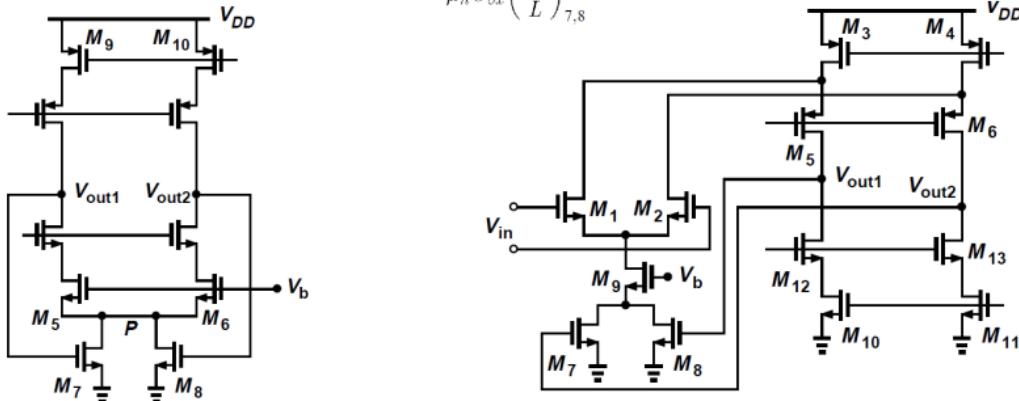
- Control tail current source



# CM Feedback Techniques

- Deep triode sensing feedback
  - Limited headroom
  - Large C
  - Device variation
- Deep triode folded-cascade sensing feedback

$$V_{out1} + V_{out2} = \frac{2I_D}{\mu_n C_{ox} \left(\frac{W}{L}\right)_{7,8}} \frac{1}{V_b - V_{GS5}} + 2V_{TH}$$



## Example 9.18

Determine the sensitivity of  $V_{out,CM}$  to  $V_b$ , i.e.,  $dV_{out,CM}/dV_b$ .

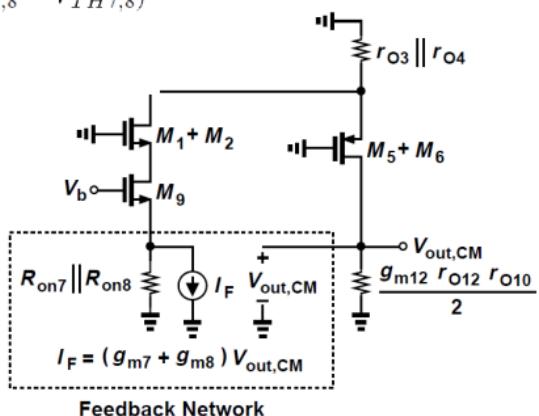
**Solution:**

**CMFB small signal analysis**

$$\begin{aligned}\beta &= \frac{V_2}{V_1} \Big|_{I_2=0} \\ &= -(g_{m7} + g_{m8})(R_{on7} \parallel R_{on8}) \\ &= -2\mu_n C_{ox} \left(\frac{W}{L}\right)_{7,8} V_{DS7,8} \cdot \frac{1}{2\mu_n C_{ox} (W/L)_{7,8} (V_{GS7,8} - V_{TH7,8})} \\ &= -\frac{V_{DS7,8}}{V_{GS7,8} - V_{TH7,8}},\end{aligned}$$

$$\left| \frac{dV_{out,CM}}{dV_b} \right|_{closed} \approx \frac{V_{GS7,8} - V_{TH7,8}}{V_{DS7,8}}$$

**Maximize  $V_{DS7,8}$  for Sensitivity**



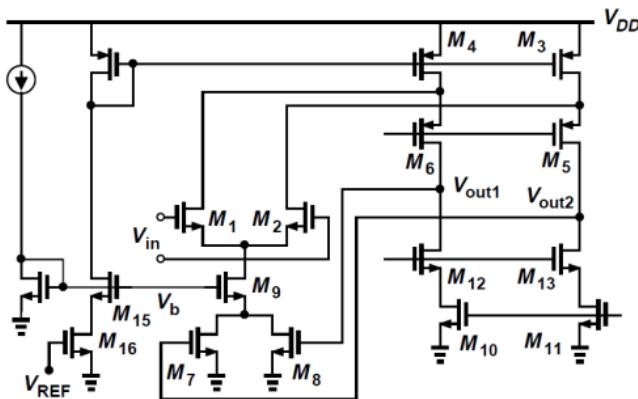
# CM Feedback Techniques

- Modification of deep triode sensing feedback

$$(W/L)_{15} = (W/L)_9$$

$$(W/L)_{16} = (W/L)_7 + (W/L)_8$$

- The output level is relatively independent of device parameters and lowers sensitivity of  $V_b$

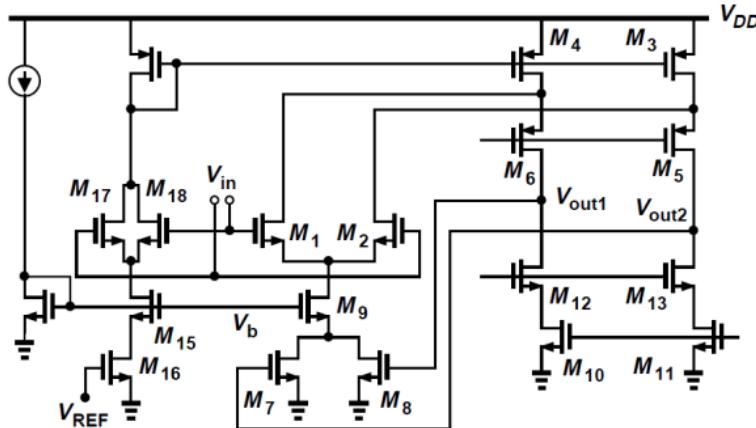


# CM Feedback Techniques

- Modification of deep triode sensing feedback

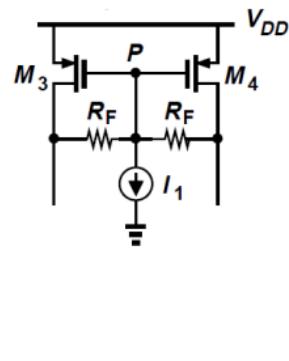
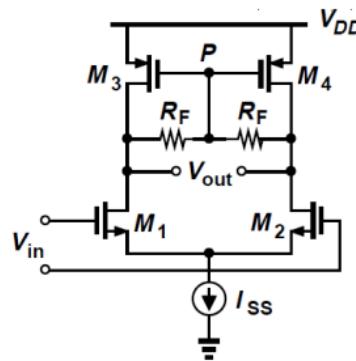
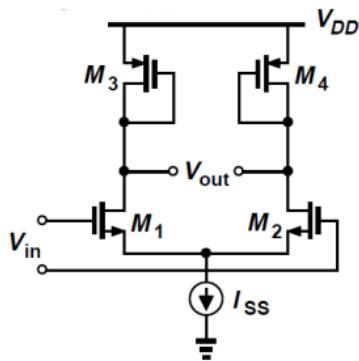
$$(W/L)_{15} = (W/L)_9 \quad (W/L)_{16} = (W/L)_7 + (W/L)_8$$

- M17, M18 reproduces the drain of M15 a voltage equal to the source voltage of M1 and M2



# CM Feedback Techniques

- Another type of CM feedback topology
- Diode-connected loads' output CM level is well-defined
- Differential small signal gain  $g_{m1,2}(r_{O1,2} \parallel r_{O3,4} \parallel R_F)$
- Common-mode work as a diode-connected  $R_F \gg r_{O1,2} \parallel r_{O3,4}$
- Low supply voltage design  $I_1 R_F / 2 = |V_{TH3,4}|$



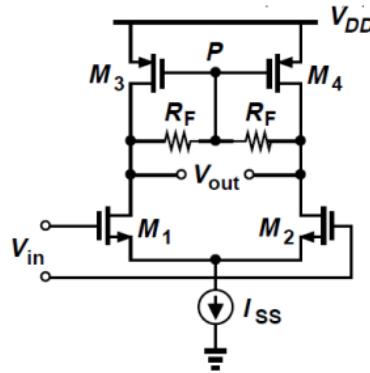
## Example 9.19

Determine the maximum allowable output swings.

Solution:

Each output can fall to two overdrive voltages above ground if  $V_{in,CM}$  is chosen to place  $I_{ss}$  at the edge of the triode region. The highest level allowed at the output is equal to the output CM level at P plus  $|V_{th3,4}|$  (by selecting suitable  $R_F$ ). Thus, output swing is  $V_{DD} - 3V_{ov}$ .

(RF is small, not like previous setup)



## Example 9.20

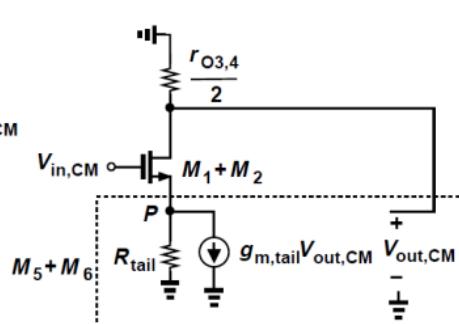
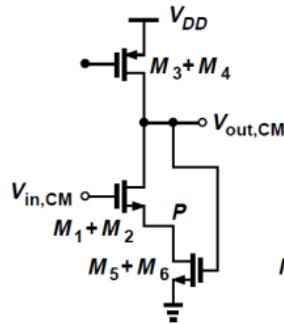
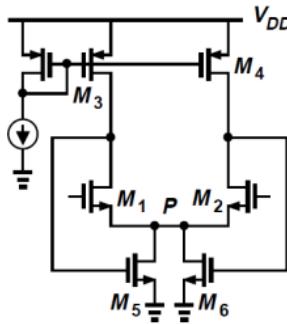
Facing voltage headroom limitations, a student constructs the circuits below. Determine the small-signal gain from the input CM level to the output CM level.

**Solution:**  $g_{m5} + g_{m6} = 2\mu_n C_{ox} (W/L)_{5,6} V_P$

$$R_{tail} = [2\mu_n C_{ox} (W/L)_{5,6} (V_{out,CM} - V_{TH5,6})]^{-1}$$

$$\frac{V_{out,CM}}{V_{in,CM}} = -\frac{1}{\frac{2R_{tail}}{r_{O3,4}} + g_{m,tail} R_{tail} + (g_{m1,2} r_{O3,4})^{-1}}.$$

(A poor CMRR)



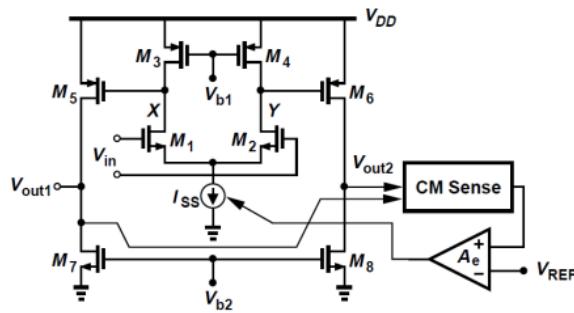
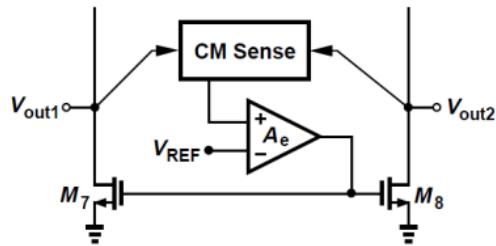
(a)

(b)

(c)

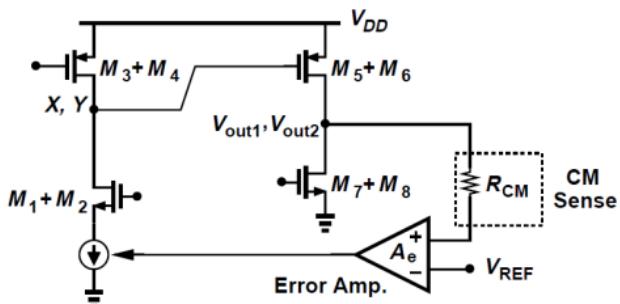
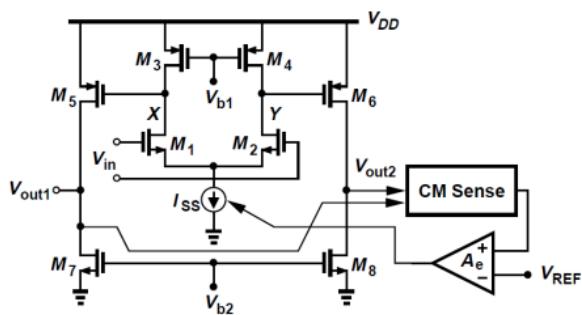
# CMFB in Two-Stage Op Amps

- CMFB around second stage (not good)
  - May establish a current beyond nominal value
- CMFB from second stage to first stage
  - Global loop control of both stages



# CMFB from Second to First Stage

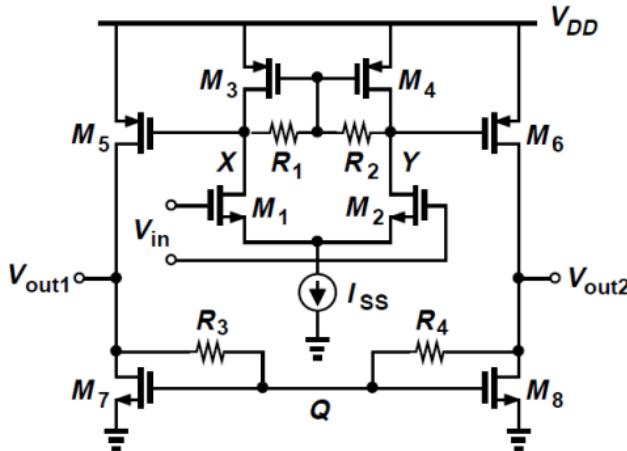
- CMFB from second stage to first stage limitation
  - 3 or 4 poles, which makes it difficult for the loop stable



# CMFB at both Stages

- All the drain currents are copied from  $I_{SS}$
- The differential voltage gain is equal to

$$g_{m1}(r_{O1}||r_{O3}||R_1)g_{m5}(r_{O5}||r_{O7}||R_3)$$

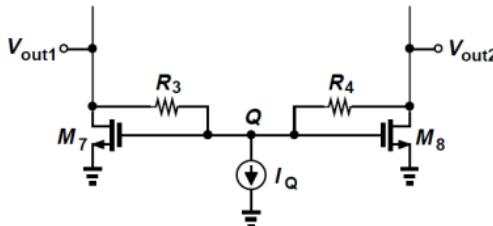
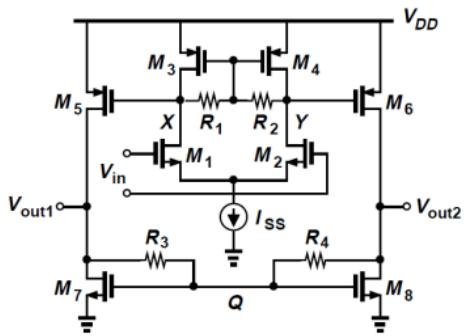


## Example 9.21

For the below design explain why the output CM level is inevitably well below VDD/2 and hence the output swings are limited. Devise a solution.

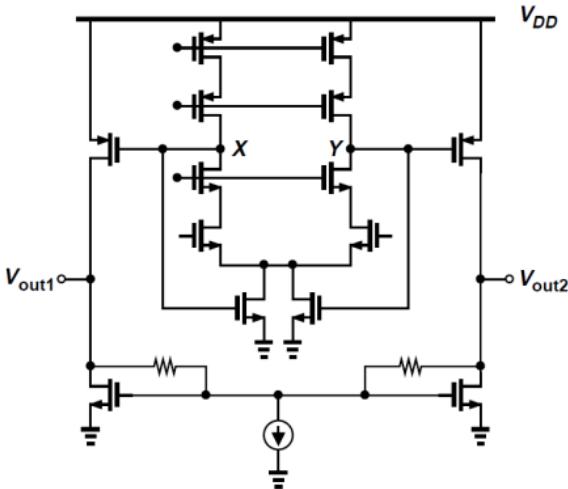
**Solution:**

The output CM is equal to  $VG7,8$ , which is only slightly greater than one threshold. The issue can be resolved by drawing a small current from node Q. It can be upwards to desired output and the device is still in saturation.



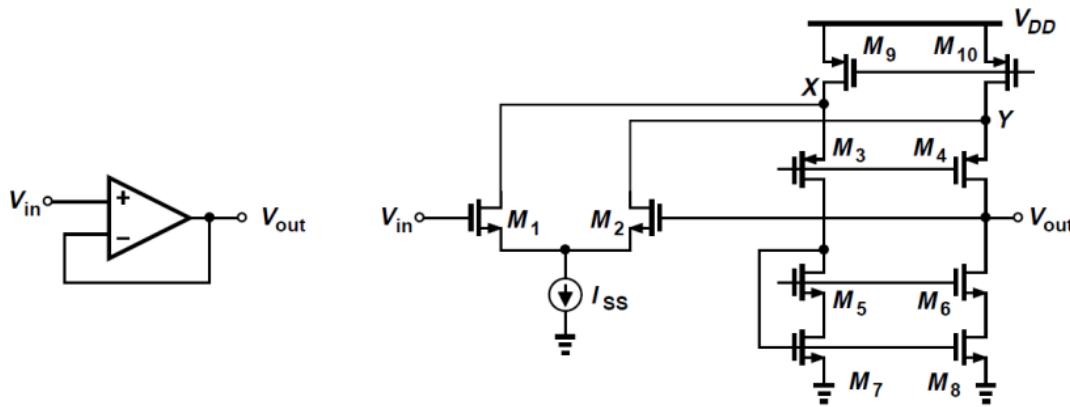
# CMFB for Cascode First Stage

- First stage use deep triode feedback loop to avoid loading.
- Achieving high gain while not precise



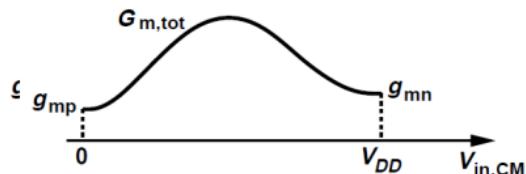
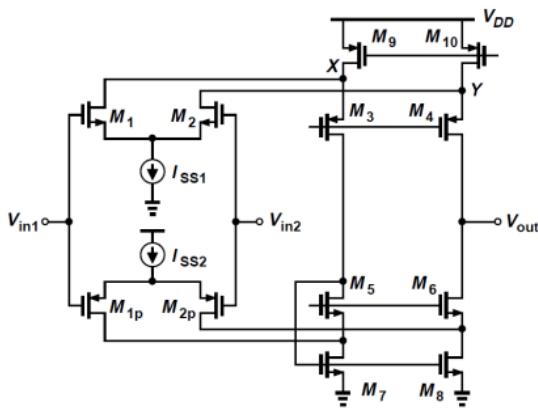
# Input Range Limitations

- Input common-mode level may need to vary over a wide range, e.g. ADC input comparator.
- Input swing limits the total range sometimes.
- In the below single-end unity-gain buffer the input CM minimal voltage is  $V_{GS1,2} + V_{ISS}$ , which is one threshold greater than  $2V_{ov}$  in the output CM.



# Extension of Input Range

- Incorporate both NMOS and PMOS differential pair to keep a necessary transconductance
- The transconductance variation should be concerned
- Gain, speed and noise may vary



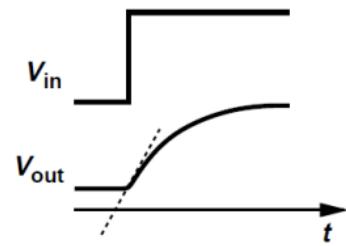
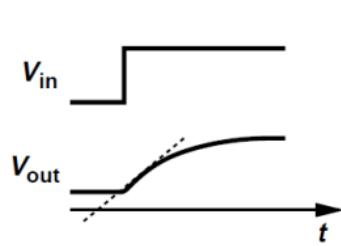
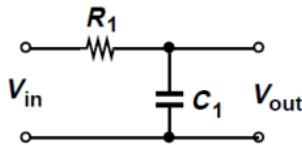
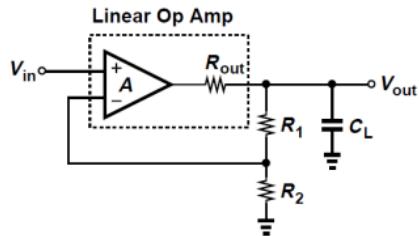
# Slew Rate

- In a linear circuit, the slope of the step depends on final output value

$$\frac{dV_{out}}{dt} = \frac{V_0}{\tau} \exp \frac{-t}{\tau}$$

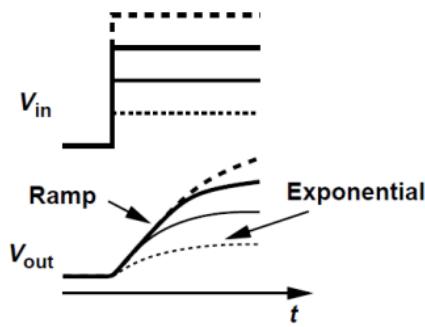
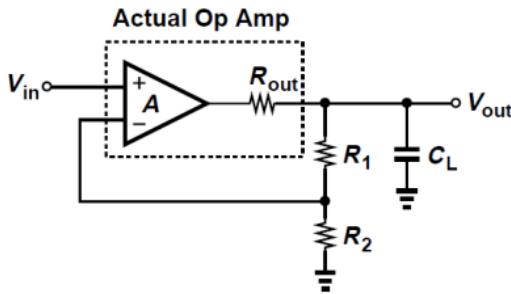
- The observation applies to linear feedback system

$$V_{out} = V_0 \frac{A}{1 + A \frac{R_2}{R_1 + R_2}} \left[ 1 - \exp \frac{-t}{\frac{C_L R_{out}}{1 + AR_2/(R_1 + R_2)}} \right] u(t)$$



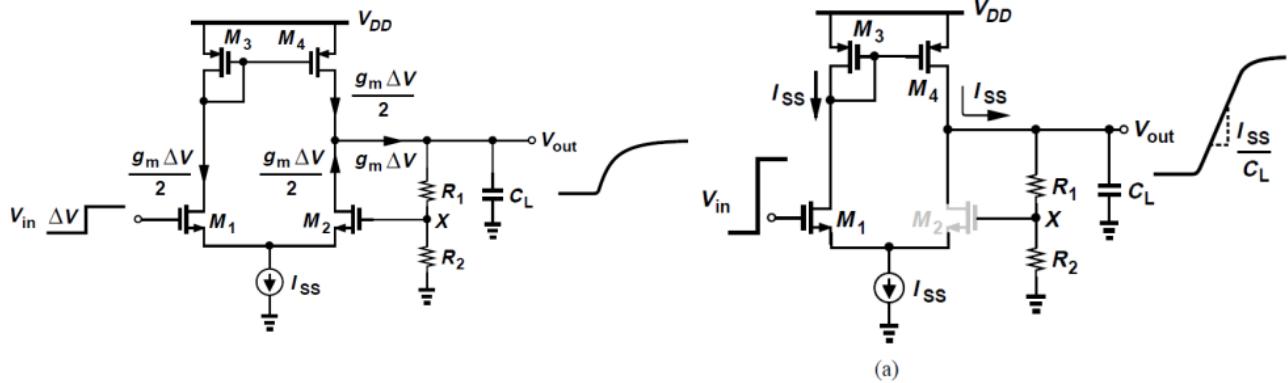
# Slew Rate

- In a realistic case, with large input steps, the output displays a linear ramp having a constant slope. The slope of ramp is the “slew rate”.
- It seems that the maximum current to charge the load capacitance is limited.
- Nonlinear behavior. Reduce speed and increase distortion.
- Increase SR would consume power and wider device



# Slew Rate Example

- A small step rises  $V_{out}$  by  $g_m \Delta V$  and hence adjusts through  $R_1, R_2$  negative feedback circuit.
- When  $M_1$  experiences a large step,  $M_2$  turns off. Thus,  $C_L$  is charged by a constant current  $I_{SS}$ .
- Feedback is broken but after  $M_2$  turns on, the circuit returns to a linear operation.



# Example 9.22

- (a) Determine the small-signal step response of the circuit.  
 (b) Calculate the positive and negative slew rates.**

**Solution:**

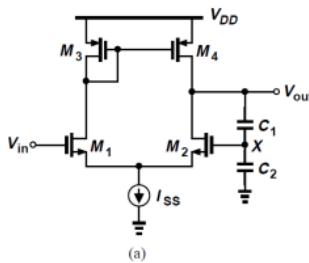
$$\frac{V_{out}(s)}{V_{in}} = \frac{A_v}{1 + A_v \frac{C_1}{C_1 + C_2} + \frac{C_1 C_2}{C_1 + C_2} R_{out} s}$$

$$= \frac{A_v / \left(1 + A_v \frac{C_1}{C_1 + C_2}\right)}{1 + \frac{C_1 C_2}{C_1 + C_2} R_{out} s / \left(1 + A_v \frac{C_1}{C_1 + C_2}\right)}$$

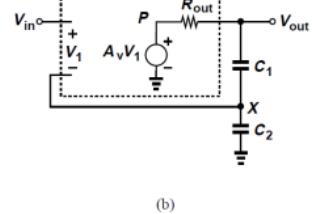
$$V_{out}(t) = \frac{A_v}{1 + A_v \frac{C_1}{C_1 + C_2}} V_0 \left(1 - \exp \frac{-t}{\tau}\right) u(t)$$

$$V_{out}(t) = I_{SS} / [C_1 C_2 / (C_1 + C_2)] t$$

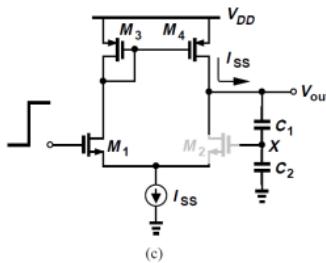
$$V_{out} = -I_{SS} / [C_1 C_2 / (C_1 + C_2)] t$$



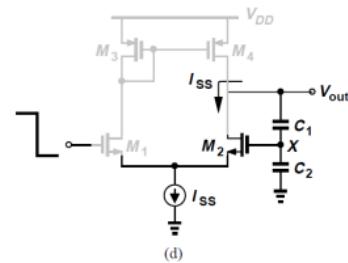
(a)



(b)



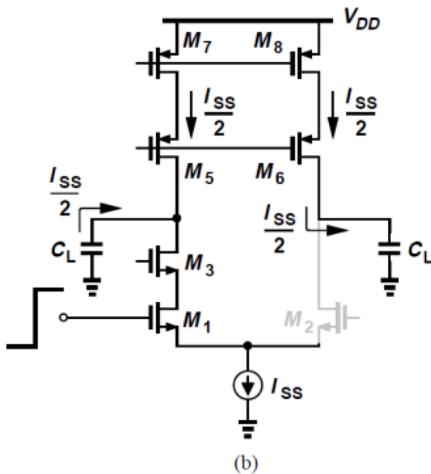
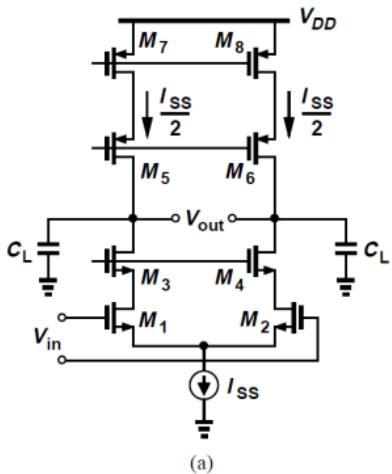
(c)



(d)

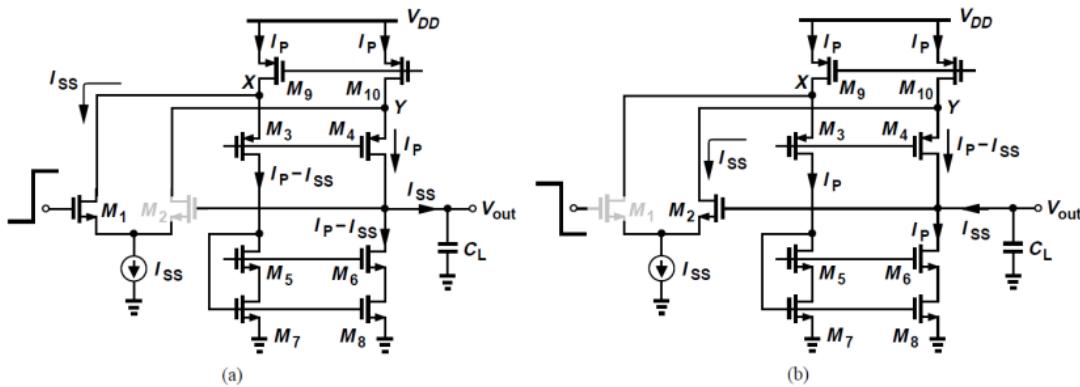
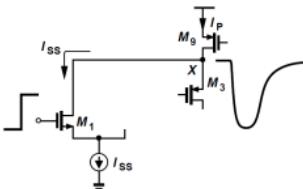
# Slew Rate of Telescopic Op Amp

- Each side appears a ramp with slope equal to  $\pm I_{SS}/(2C_L)$
- The total slew rate for  $V_{out1} - V_{out2}$  equal to  $I_{SS}/C_L$



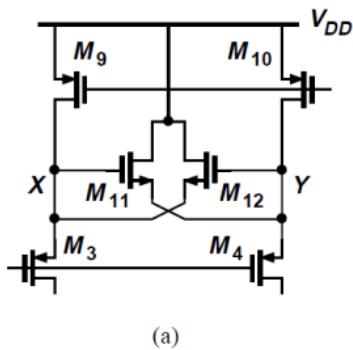
# Slew Rate of Folded-cascode Op Amp

- Yield a slew rate of  $I_{SS}/C_L$  if  $I_P \geq I_{SS}$
- Otherwise, M3 turns off and tail current source enters the triode region. The settling time increases.

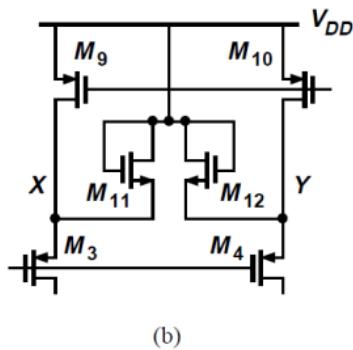


# Clamp transistor

- Limit  $V_x, V_y$  to produce large different voltage
- More aggressive design,  $V_x, V_y$  higher than  $V_{DD} - V_{THN}$



(a)



(b)

## Example 9.23

As  $V_{out}$  rises, so does  $V_x$ , eventually turning  $M_2$  on. As  $ID_2$  increases from zero, the plot becomes linear. Considering  $M_1$  and  $M_2$  becomes linear if difference between their drain current is less than  $\alpha I_{SS}$  (e.g.,  $\alpha = 0.1$ ).

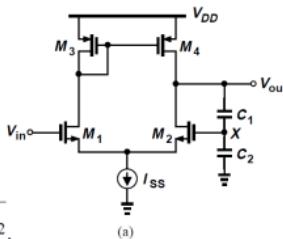
Calculate the time to linear.

Solution:

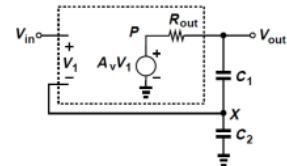
$$\alpha I_{SS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2}) \sqrt{\frac{4I_{SS}}{W} - (V_{in1} - V_{in2})^2},$$

$$\Delta V_G \approx \alpha \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

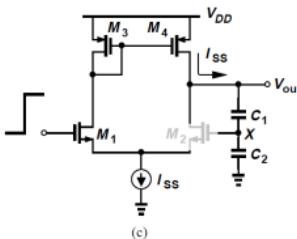
$$t = \frac{C_2}{I_{SS}} \left( V_0 - \alpha \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} \right)$$



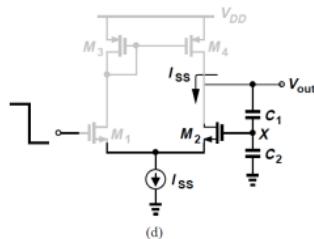
(a)



(b)



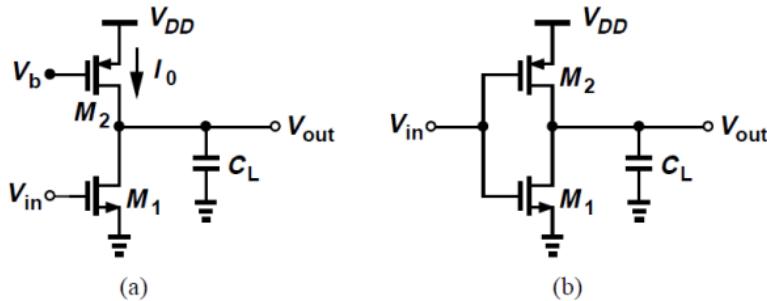
(c)



(d)

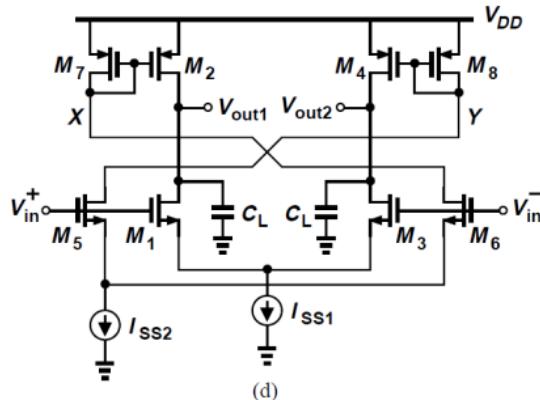
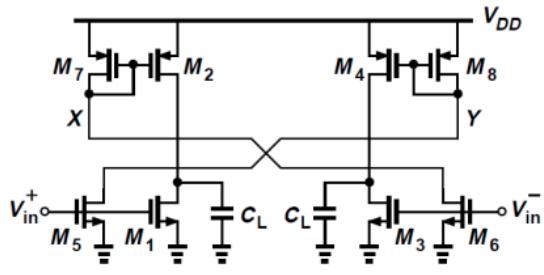
# High-Slew-Rate Op Amp

- Slew rate is limited by power consumption
- The trade-off could be mitigated if the capacitor could be charged to a desired value quickly. And the voltage falls back to original value.
- Complementary topology jumps fast but suffer from poor power supply rejection



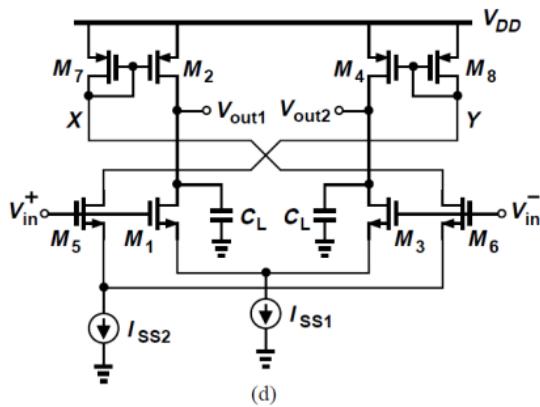
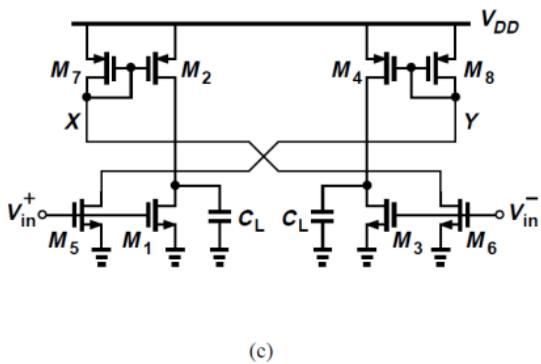
# Push-Pull Stages

- Use current-mirror. E.g. If  $V_{in+}$  jumps down, and  $V_{in-}$  jumps up then
  - $M_5$  draws less current, lowering  $ID_4$ ;
  - $M_3, M_6$  draws more current;
  - $M_7$  draws more current, raising  $ID_2$ ;
  - $M_1$  draws less current, charging  $C_L$ .



# Push-Pull Stages

- Improve the input common-mode rejection by adding tail current sources to build differential circuits
- The differential slew rate is  $[I_{SS1} + I_{SS2}(W_4/W_8)]/C_L$
- SR increases with a around twofold power penalty

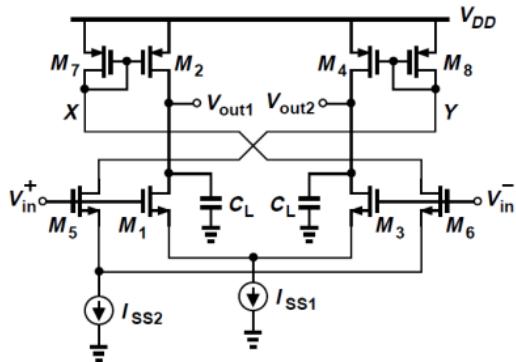


## Example 9.24

Calculate the small-signal voltage gain of the class-AB op amp shown below.

**Solution:**

$$\begin{aligned}|A_v| &\approx g_{m1}(r_{O3}||r_{O4}) + (W_4/W_8)g_{m5}(r_{O3}||r_{O4}) \\ &\approx [g_{m1} + (W_4/W_8)g_{m5}](r_{O3}||r_{O4}).\end{aligned}$$



# Frequency Response and Mirror Pole

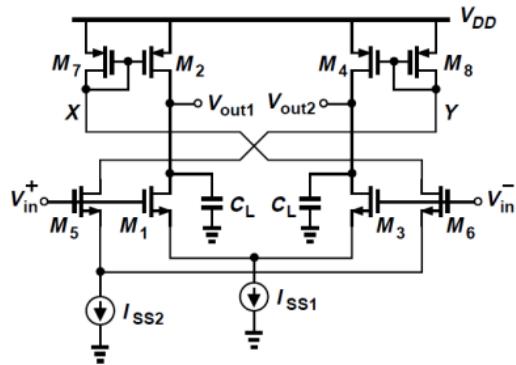
- It is not possible to equate zero and pole
- Raise SR would decrease mirror pole frequency

$$g_{m8}/C_Y \quad C_Y \approx 2(W_4 + W_8)LC_{ox}$$

$$H_{mirr}(s) = \frac{W_4}{W_8} g_{m5} (r_{O3} || r_{O4}) \frac{1}{1 + \frac{s}{\omega_{p,X}}} \frac{1}{1 + \frac{s}{\omega_{out}}}$$

$$\omega_{p,X} \approx g_{m8}/C_Y \text{ and } \omega_{out} = [(r_{O3} || r_{O4})C_L]^{-1}$$

$$\begin{aligned} H_{tot}(s) &= H_{main}(s) + H_{mirr}(s) \\ &= \frac{r_{O3} || r_{O4}}{1 + \frac{s}{\omega_{out}}} \left[ \frac{W_4}{W_8} \frac{g_{m5}}{1 + \frac{s}{\omega_{p,X}}} + g_{m1} \right] \\ &= \frac{r_{O3} || r_{O4}}{1 + \frac{s}{\omega_{out}}} \cdot \frac{(W_4/W_8)g_{m5} + g_{m1} + g_{m1}s/\omega_{p,X}}{1 + \frac{s}{\omega_{p,X}}} \end{aligned}$$



$$|\omega_z| = \left( \frac{W_4}{W_8} \frac{g_{m5}}{g_{m1}} + 1 \right) \omega_{p,X}.$$

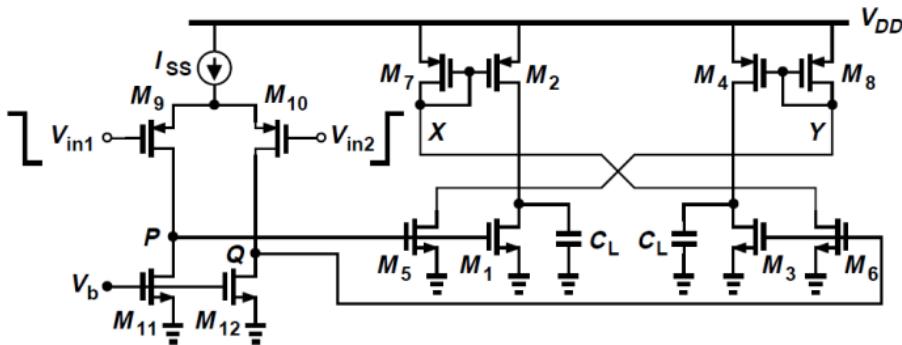
# Two-Stage Op Amp with High SR

- **Voltage Gain:**

$$|A_v| = g_{m9}(r_{O9}||r_{O11})[g_{m1} + (W_4/W_8)g_{m5}](r_{O1}||r_{O2})$$

- **Slew Rate**

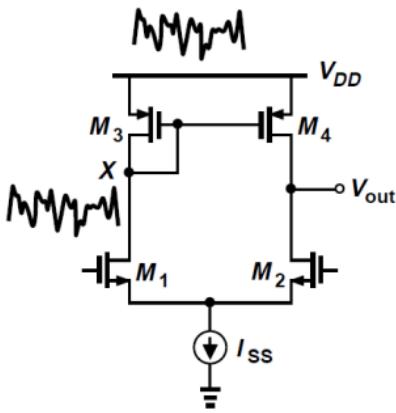
- If P is low capacitance, it is “agile” enough to go upon to VDD, thus providing a large SR.



# Power Supply Rejection

- Power line contains noise
- PSRR(power supply rejection ration):
  - Gain from input to output divided by the gain from supply to the output
- At low frequency

$$PSRR \approx g_{mN}(r_{OP} \parallel r_{ON})$$



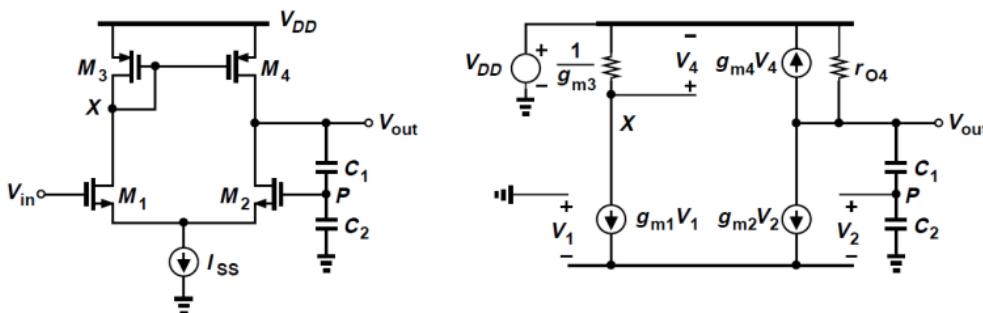
## Example 9.25

Calculate the low-frequency PSRR of the feedback circuit shown below

**Solution:**  $\frac{V_{out}}{V_{DD}} = \frac{\frac{1}{C_1}}{g_{m2}r_{O4}\frac{C_1}{C_1+C_2} + 1}$ .

$$PSRR \approx (1 + \frac{C_2}{C_1})(g_{m2}r_{O4}\frac{C_1}{C_1+C_2} + 1)$$
$$\approx g_{m2}r_{O4}.$$

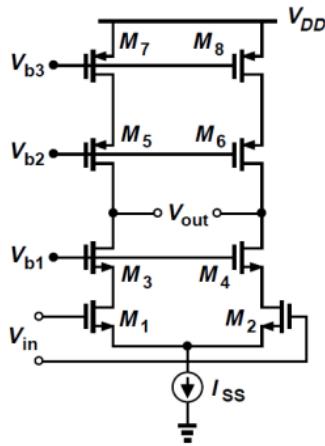
**Feedback reduce  $\partial V_{out}/\partial V_{DD}$  and  $\partial V_{out}/\partial V_{in}$  the same and PSRR is relatively constant.**



# Noise in Telescopic Op Amp

- At low frequency the cascode devices contribute negligible noise

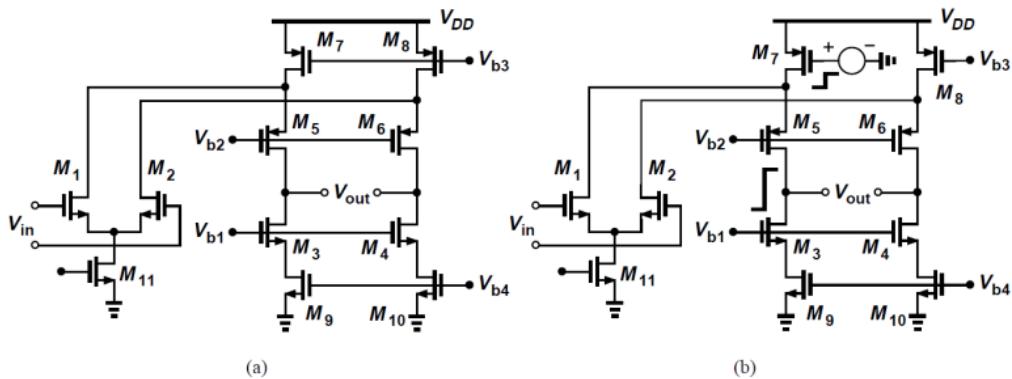
$$\overline{V_n^2} = 4kT \left( 2 \frac{\gamma}{g_{m1,2}} + 2 \frac{\gamma g_{m7,8}}{g_{m1,2}^2} \right) + 2 \frac{K_N}{(WL)_{1,2} C_{ox} f} + 2 \frac{K_P}{(WL)_{7,8} C_{ox} f} \frac{g_{m7,8}^2}{g_{m1,2}^2}$$



# Noise in Folded-Cascode Op Amp

- At low frequency the cascode devices contribute negligible noise

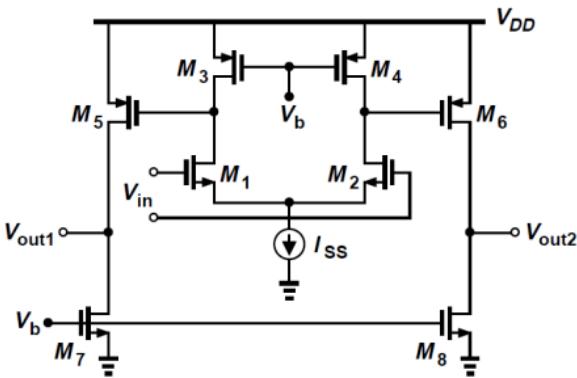
$$\overline{V_{n,int}^2} = 8kT \left( \frac{\gamma}{g_{m1,2}} + \gamma \frac{g_{m7,8}}{g_{m1,2}^2} + \gamma \frac{g_{m9,10}}{g_{m1,2}^2} \right)$$



# Noise in two-stage Op Amp

- The noise in the second stage contributes negligible noise

$$\overline{V_{n,tot}^2} = 8kT\gamma \frac{1}{g_{m1}^2} \left[ g_{m1} + g_{m3} + \frac{g_{m5} + g_{m7}}{g_{m5}^2(r_{O1}\parallel r_{O3})^2} \right]$$



## Example 9.26

A simple amplifier is constructed below. Note that the first stage incorporates diode-connected – rather than current-source loads. Assuming all the transistors in saturation.  
 $(W/L)1=50/0.6$   $(W/L)3=10/0.6$   $(W/L)5=20/0.6$   $(W/L)7=56/0.6$   
Solution:

$$\begin{aligned} A_{v1} &\approx \frac{g_{m1}}{g_{m3}} & (8kT/3)(g_{m3} + g_{m1})/g_{m1}^2 &= 1.10 \times 10^{-17} \text{ V}^2/\text{Hz}. \\ &= \sqrt{\frac{50 \times 75}{10 \times 30}} & 4kT(2/3)(g_{m5} + g_{m7})/g_{m5}^2 A_{v1}^2 &= 2.29 \times 10^{-18} \text{ V}^2/\text{Hz} \\ &\approx 3.54. & \end{aligned}$$
$$\begin{aligned} \overline{V_{n,in}^2} &= 2(2.29 \times 10^{-18} + 1.10 \times 10^{-17}) \\ &= 2.66 \times 10^{-17} \text{ V}^2/\text{Hz}, \end{aligned}$$

