Digital Laboratory Lab03 Report

(Experiment Record Template)

Watch Lab video before the lab day. Playlist:

<https://youtube.com/playlist?list=PLcGCikr5PJAjmQK4UDKF_IvetUyXElN0i>

**You can finish the lab at home before you enter the classroom.**

Note:

All transistors are “2N2222”. Most of resistors in the circuit are “1k Ohm”.

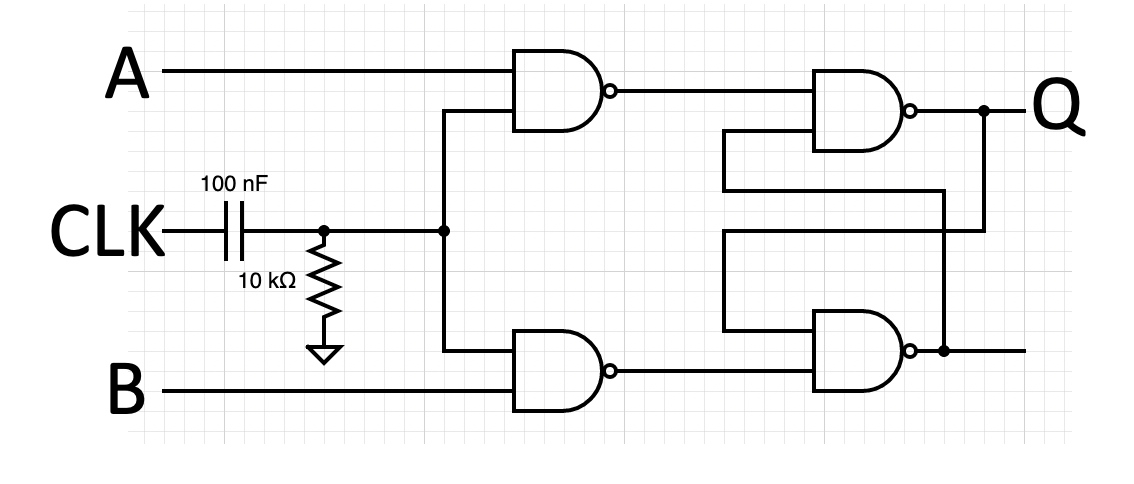
Logic(1) can be expressed as 1. Logic(0) can be expressed as 0.

↑ this symbol is the rising edge of the clock signal.

**Experiment-01**

Please use Analog Discovery 2 to test and complete the truth table.

**Implement the following circuit and finish the truth table.**



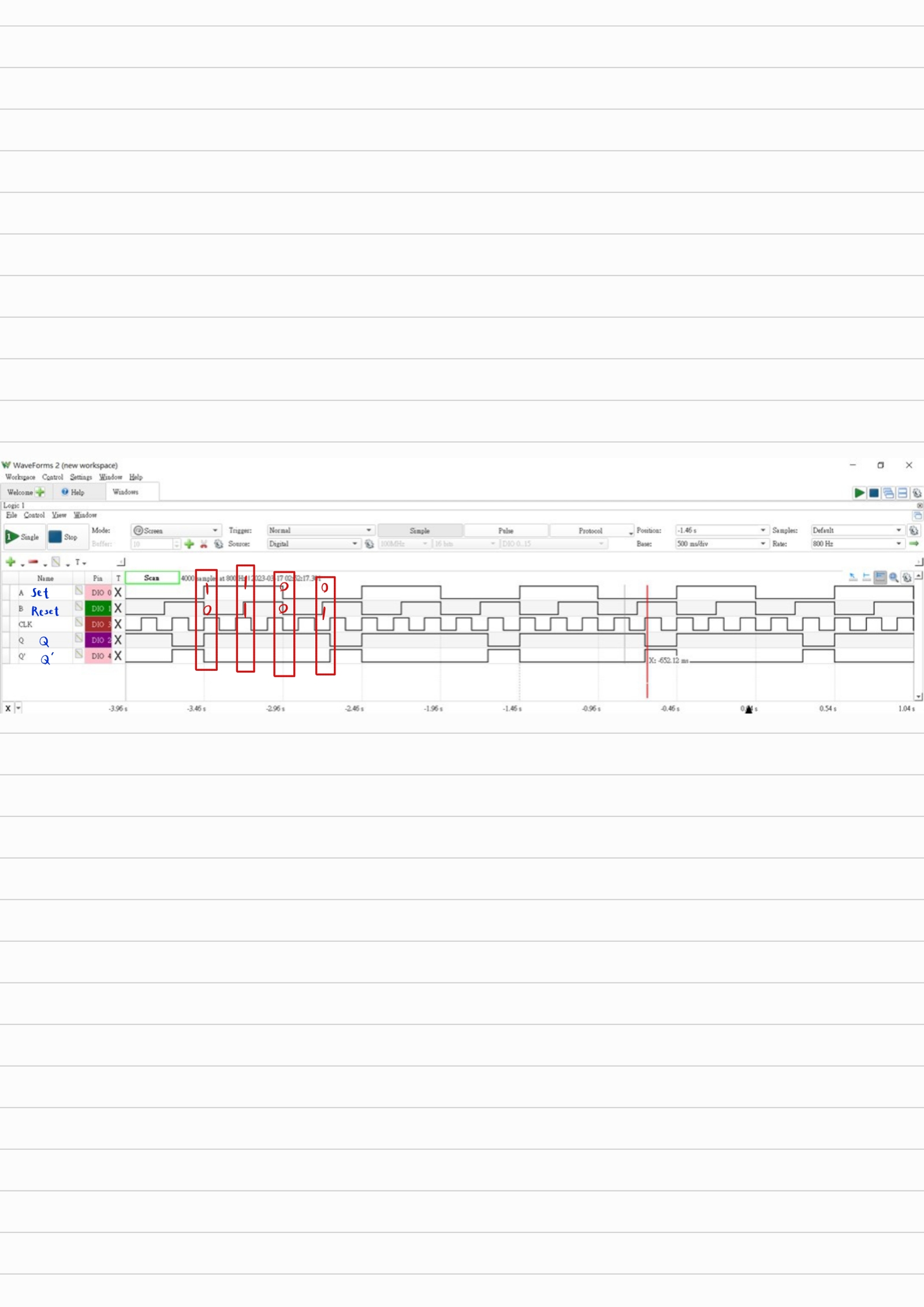
NOTE:

CLK = 0.5 Hz square wave from pattern generator of AD2.

The color code of the 10k Ohm resistor is BROWN BLACK ORANGE GOLD.

Live demonstrate these transitions to the TA.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLK** | **A(Set)** | **B(Reset)** | **Qt** | **Qt+1** |
| X | X | X | 0 | 0 |
| X | X | X | 1 | 1 |
| ↑ | 1 | 0 | 0 | 1 |
| ↑ | 1 | 0 | 1 | 1 |
| ↑ | 0 | 1 | 0 | 0 |
| ↑ | 0 | 1 | 1 | 0 |

Attach your logic analyzer waveform.

Questions: **(Solve it at home. No live demo)**

**(Ask your own questions and answer them by yourself)**

**What is this circuit?**

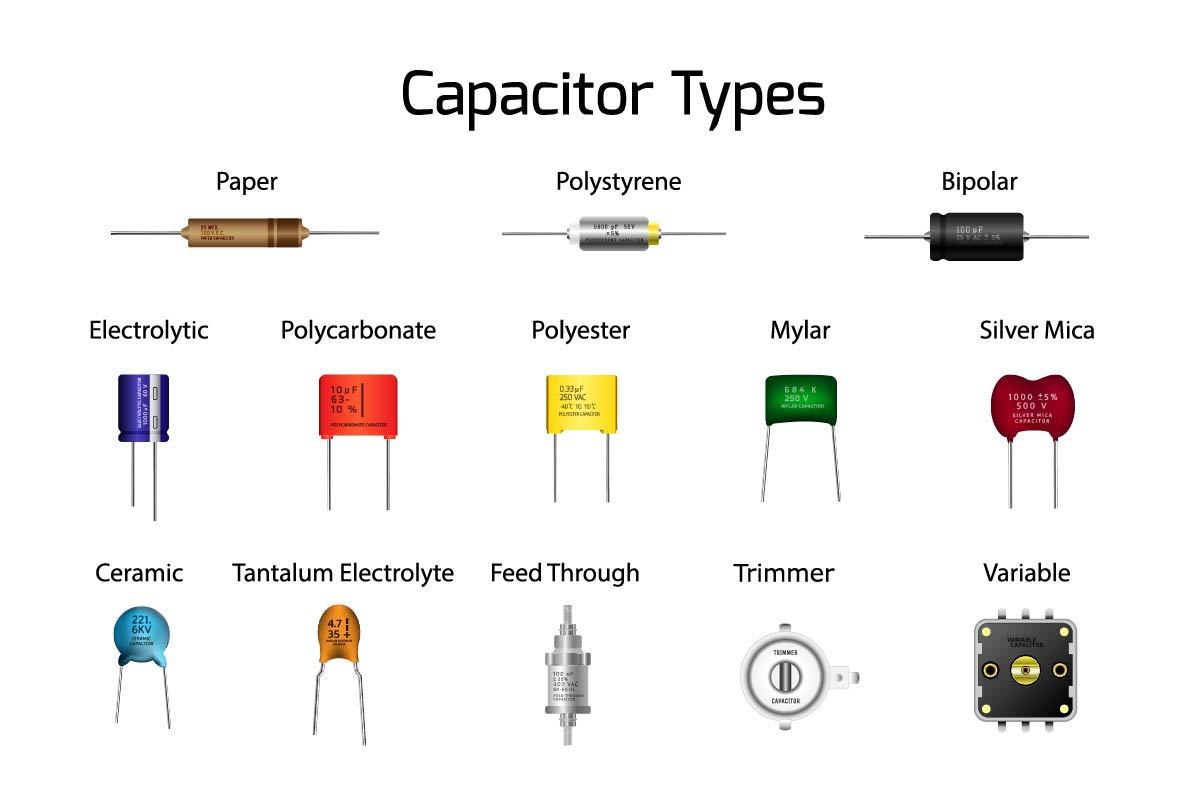
It’s a gated SR latch.

**What’s the purpose of connecting a grounded capacitor to the CLK signal?**

This creates a high-pass filter.A high pass filter can be used to remove noise from our CLK input and improve the quality of the signal, which can improve the accuracy and reliability of the data transmission.

**While working on my circuit, I wondered, “Which pin on this capacitor is positive and which one’s negative?” I didn’t know that the one we were using was a ceramic capacitor. A ceramic capacitor does not have polarity. I only got my answer after doing searching on the Internet.**

Here’s a picture of different capacitor types.

In Lab 3, we used a ceramic capacitor. The following is some of its features:

* Ceramic capacitors are NOT polarized.
* Ceramic capacitors have excellent stability over time and temperature
* Smaller in size and have a low capacitance range.
* Ceramic capacitors have a lower voltage rating

In lab 4, we used an electrolytic capacitor. The following is some of its features:

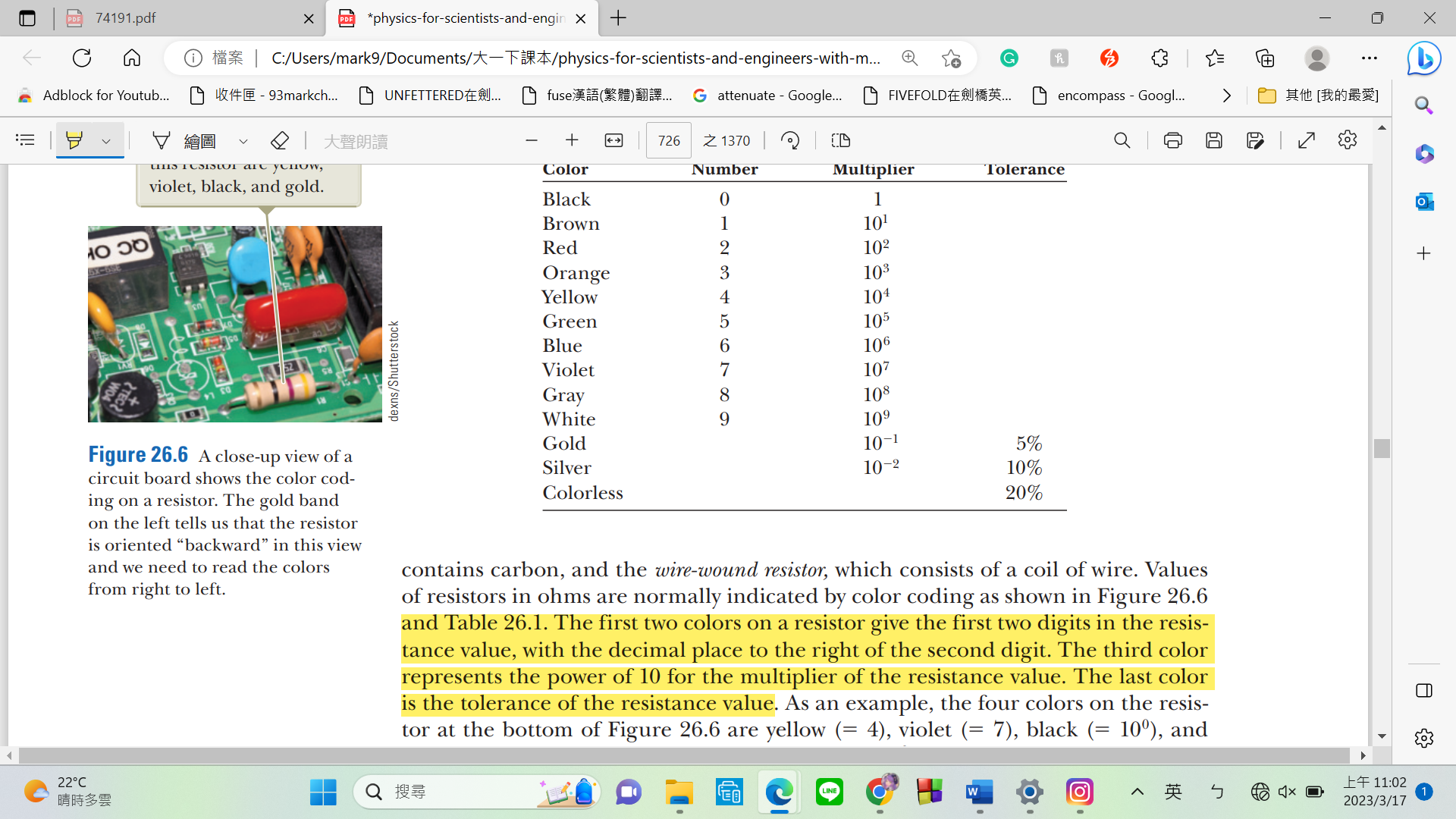
* Electrolytic capacitors are polarized.
* Electrolytic capacitors have a higher likelihood of changing in capacitance over time when exposed to each t
* Smaller in size and have a high capacitance range.
* Electrolytic capacitors have a higher voltage rating than ceramic capacitors

To sum up, the main difference between these two is that ceramic capacitors are better suited for low-capacitance and high-stability applications, while electrolytic capacitors are better suited for high-capacitance and high-voltage applications.

I think the reason we had to swap to using the electrolytic capacitor in Lab 4 was that the ICs would only run at 5V. This voltage level would be too much for the ceramic one to handle.

**Recently, we are learning about current, voltage, and resistance in our physics class. Also, in this experiment, we had to use a 10k ohm resistor. I didn’t know how to tell which resistor had how much resistance. It just so happens that there’s a chart explaining this in our physics textbook.**

Below is an excerpt from our physics textbook,



To read the resistance value of a resistor using the color code, you need to:

1. Identify the tolerance band, which is usually gold or silver.
2. Read the color of the first band from the left to right. This color represents the first digit of the resistance value.
3. Read the color of the second band. This represents the second digit of the resistance value.
4. Read the color of the third band. This represents the multiplier, which is the number of zeros that follow the first two digits.
5. Calculate the resistance value using the following formula:

Resistance = (First Digit \* 10 + Second Digit) \* 10^(Multiplier)

For example, if the first band is brown, the second band is black, and the third band is red, the resistance value of the resistor would be:

Resistance = (1 \* 10 + 0) \* 10^2 = 1000 ohms

**Experiment-02**

Please read and practice configuring the 74191 IC (you need some other logic IC to control the counter).

**Design and implement frequency divider that can satisfied the following requirements.**

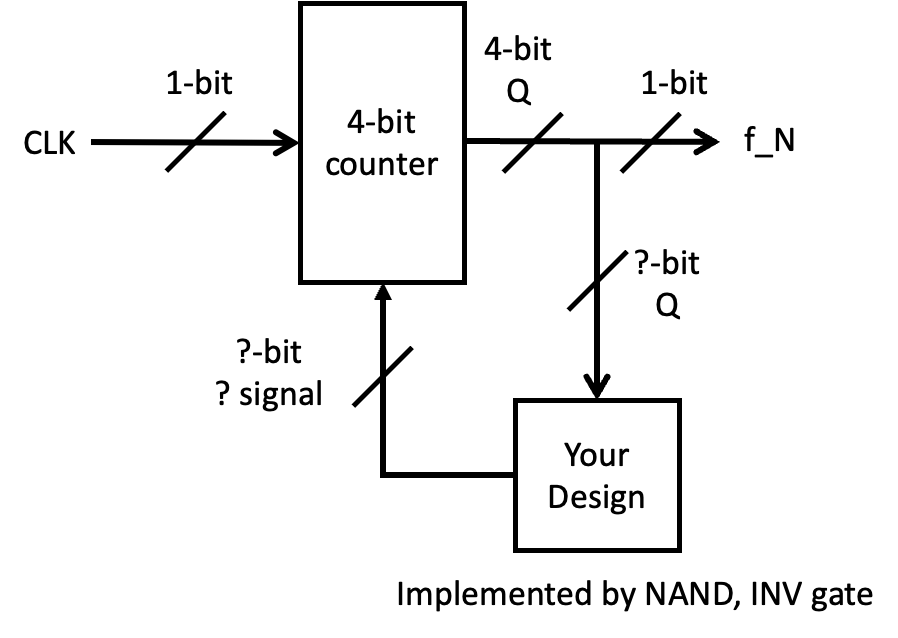
Live demonstrate these functions to the TA.

Source clock frequency

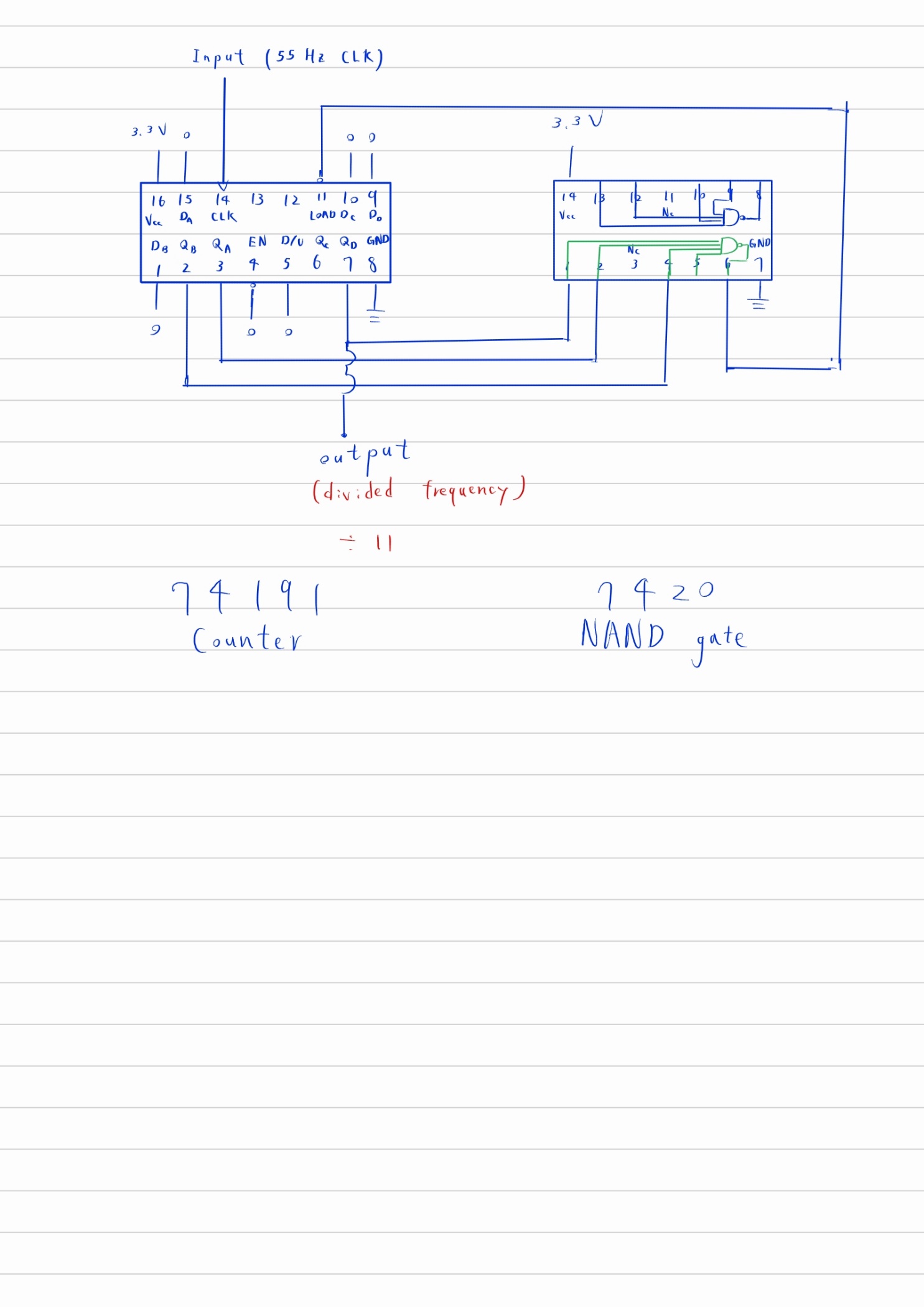
|  |  |  |
| --- | --- | --- |
| units digit your student ID (6) | source frequency (Hz) | ÷ N |
| 0 or 3 | 6 | 3 |
| 4 or 8 | 15 | 5 |
| 1 or 5 | 36 | 9 |
| 6 or 9 | 55 | 11 |
| 2 or 7 | 78 | 13 |

e.g., ID = 1234567 🡪 units digit = 7 🡪 source freq. = 78 🡪 target frequency = 78 / 13 = 6 Hz.

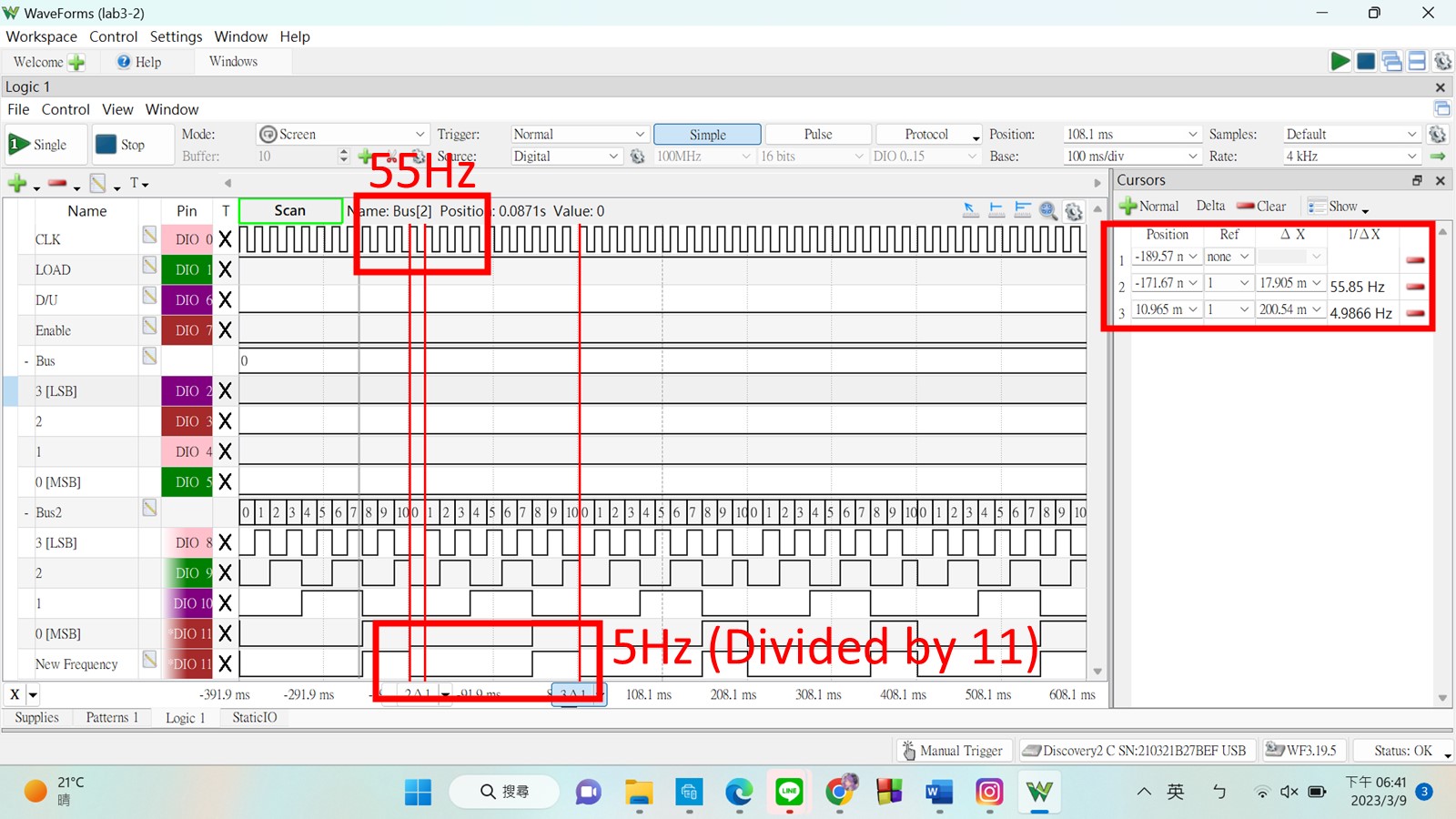
Reference:



Circuit diagram **(You can attach hand-drawing plot or use software to generate the diagram)**

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Attach your logic analyzer waveform. (You should mark some labels or cursors to show the information)

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Questions: **(Solve it at home. No live demo)**

**(Ask your own questions and answer them by yourself)**

**Is it necessary for the clock signal to have 50% duty cycle?**

No, it’s not necessary. Originally, we thought that the signal with our new divided frequency had to have 50% duty cycle. We ended up overcomplicating our circuit and created a design that was prone to error. However, nowhere did the experiment description state that this was required. I think this is a learning experience for both sides, the TA and ourselves. I realized that it was not just us who had this confusion. Other classmates were also trying to figure out ways to obtain a 50% duty cycle signal. I think that the reason we had this confusion was that: (It would probably be confusing if I wrote this in English, so I am swapping over to Chinese) 除頻對我們來說都是一個上學期邏輯設計課程沒有提到或沒有深入琢磨的概念，所以學生大多都不了解。看到題目說要對CLK除頻，第一時間的想法就是要取得一個新頻率的CLK，而在大家看過的那些邏設習題裡，CLK都是1和0的工作時間相等、完美對稱的方波，因而會不自覺產生這種「除頻完CLK波形必須長相一樣」的誤解。或許助教在下學期的課程中，若有要再出同樣的題目，可以特別強調這一點，讓雙方對題目的理解能更一致。

**Why isn’t an inverter needed in the design?**

To divide by 11, the counter is supposed to reset back to zero once it hits 11. In binary:

0000 -> 0

0001 -> 1

0010 -> 2

0011 -> 3

0100 -> 4

0101 -> 5

0110 -> 6

0111 -> 7

1000 -> 8

1001 -> 9

1010 -> 10

1011 -> 11

DCBA

Since the counter never needs to count more than 11, connecting D, B, A to the NAND gate is enough to differentiate 11 from the other numbers. Inverting C and connecting it to the NAND gate is redundant. However, I have observed many classmates taking this less efficient approach. I believe it’s crucial to fully understand the logic behind the circuit and what each component is doing before you start building your actual circuit. Doing that may seem like extra work, but it might save you more time than going into it headfirst.