```
1   module reg_mux #(
2       parameter DATA_WIDTH = 18,
3                 REG = 1,
4                 RSTTYPE = "SYNC"
5   ) (
6       input [DATA_WIDTH - 1 : 0] data,
7       input rst, CE, clk,
8       output [DATA_WIDTH - 1 : 0] mux_out
9   );
10
11  reg [DATA_WIDTH - 1 : 0] Reg;
12
13  generate if (RSTTYPE == "ASYNC") begin
14
15      always @(posedge clk or posedge rst) begin
16          if(rst) begin
17              Reg <= 0;
18          end
19          else if (CE) begin
20              Reg <= data;
21          end
22      end
23  end
24      else if (RSTTYPE == "SYNC") begin
25
26          always @(posedge clk) begin
27              if(rst) begin
28                  Reg <= 0;
29              end
30              else if (CE) begin
31                  Reg <= data;
32              end
33          end
34      end
35
36  endgenerate
37
38  assign mux_out = (REG)? Reg : data;
39
40  endmodule
41
```

D:\MiniProject\DSP.v - Sublime Text (UNREGISTERED)

reg_mux.v | module DSP48A1_tb (); | DSP.v | run_DSP.do | Constraints_basys3.xdc

```
module DSP48A1 #(
    parameter A0REG = 0,
              A1REG = 1,
              B0REG = 0,
              B1REG = 1,
              CREG = 1,
              DREG = 1,
              MREG = 1,
              PREG = 1,
              CARRYINREG = 1,
              CARRYOUTREG = 1,
              OPMODEREG = 1,
              CARRYINSEL = "OPMODE5",
              B_INPUT = "DIRECT",
              RSTTYPE = "SYNC"

) (
    input [17:0] A, B, D, BCIN,
    input [47:0] C, PCIN,
    input [7:0] OPMODE,
    input clk, CARRYIN,
    input RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE,
    input CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE,
    output [17:0] BCOUT,
    output [47:0] PCOUT, P,
    output [35:0] M,
    output CARRYOUT, CARRYOUTF
);


//Multiplexers outputs
wire [17:0] A0_mux, A1_mux, B0_mux, B1_mux, D_mux, B_IN, Pre_adder_mux;
wire [35:0] M_mux;
wire [47:0] C_mux;
wire [7:0] opmode_mux;
wire CYI_mux, Carry_in_Cascade;
reg [47:0] x_mux, z_mux;


//Outputs of adder-subtructor and multiplier
wire [17:0] Pre_adder_out;
wire [35:0] mult_out;
wire [47:0] Post_adder_out;
wire CYO;


//Instantiations
reg_mux #(18, A0REG, RSTTYPE)      A0reg (A, RSTA, CEA, clk, A0_mux);
reg_mux #(18, A1REG, RSTTYPE)      A1reg (A0_mux, RSTA, CEA, clk, A1_mux);
```

D:\MiniProject\DSP.v - Sublime Text (UNREGISTERED)

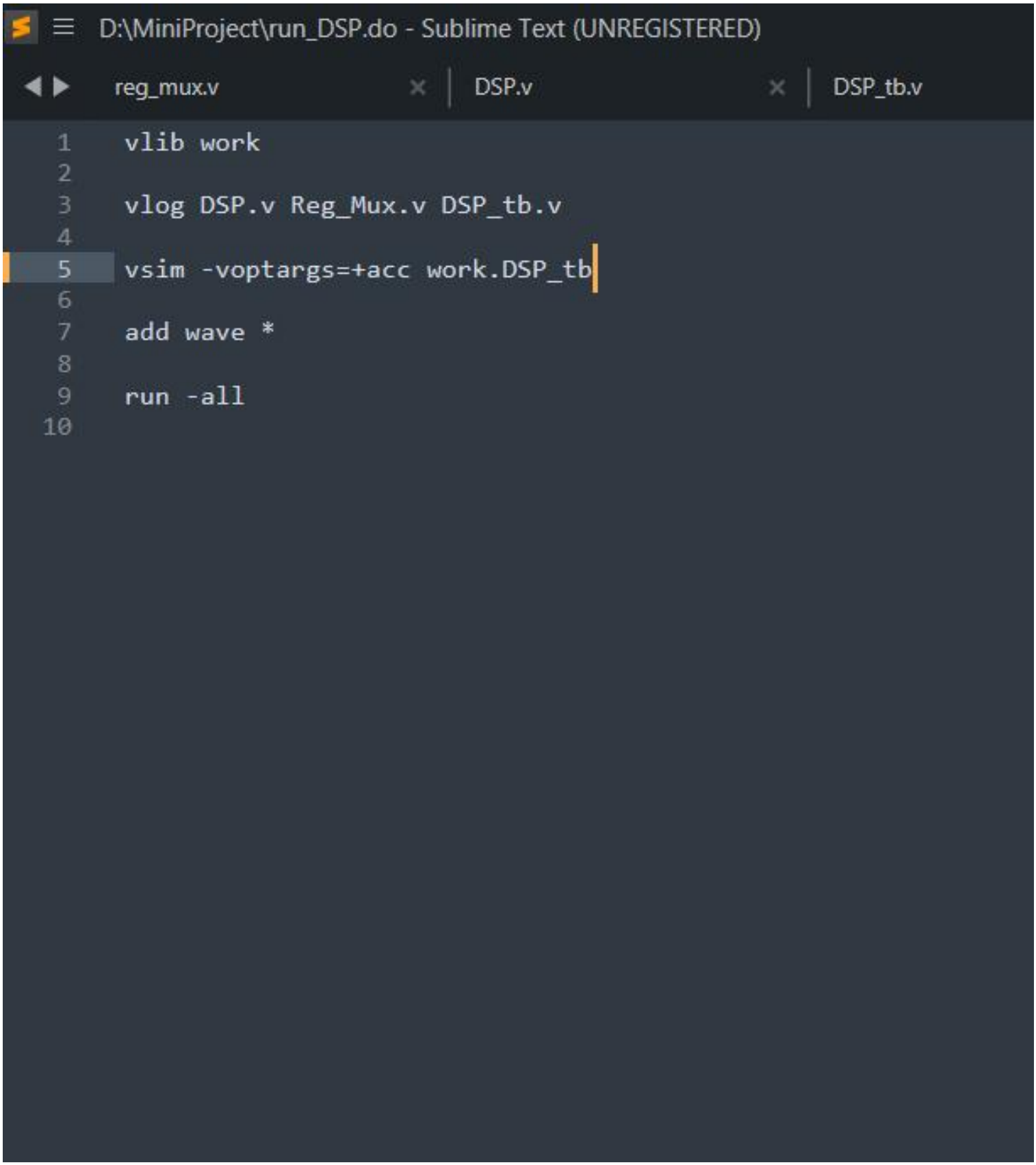
reg_mux.v | module DSP48A1_tb (); | DSP.v | run_DSP.do | Constraints_basys3.xdc

```
39
40  //Outputs of adder-subtructor and multiplier
41  wire [17:0] Pre_adder_out;
42  wire [35:0] mult_out;
43  wire [47:0] Post_adder_out;
44  wire CYO;
45
46
47  //Instantiations
48  reg_mux #(18, A0REG, RSTTYPE)      A0reg (A, RSTA, CEA, clk, A0_mux);
49  reg_mux #(18, A1REG, RSTTYPE)      A1reg (A0_mux, RSTA, CEA, clk, A1_mux);
50  reg_mux #(18, B0REG, RSTTYPE)      B0reg (B_IN, RSTB, CEB, clk, B0_mux);
51  reg_mux #(18, B1REG, RSTTYPE)      B1reg (Pre_adder_mux, RSTB, CEB, clk, B1_mux);
52  reg_mux #(48, CREG, RSTTYPE)       Creg (C, RSTC, CEC, clk, C_mux);
53  reg_mux #(18, DREG, RSTTYPE)       Dreg (D, RSTD, CED, clk, D_mux);
54  reg_mux #(8, OPMODEREG, RSTTYPE)   OPMODEreg (OPMODE, RSTOPMODE, CEOPMODE, clk, opmode_mux);
55  reg_mux #(36, MREG, RSTTYPE)       Mreg (mult_out, RSTM, CEM, clk, M_mux);
56  reg_mux #(48, PREG, RSTTYPE)       Preg (Post_adder_out, RSTP, CEP, clk, P);
57  reg_mux #(1, CARRYINREG, RSTTYPE)  CYOreg (Carry_in_Cascade, RSTCARRYIN, CECARRYIN, clk, CYI_mux);
58  reg_mux #(1, CARRYOUTREG, RSTTYPE) CYIreg (CYO, RSTCARRYIN, CECARRYIN, clk, CARRYOUT);
59
60
61  //input B
62  assign B_IN = (B_INPUT == "DIRECT")? B : (B_INPUT == "CASCADE")? BCIN : 0 ;
63  assign Pre_adder_mux = (opmode_mux[4])? Pre_adder_out : B0_mux;
64  assign BCOUT = B1_mux;
65
66
67  //buffer M
68  assign M = M_mux;
69
70
71  //buffer PCOUT
72  assign PCOUT = P;
73
74
75  //carry in
76  assign Carry_in_Cascade = (CARRYINSEL == "OPMODE5")? opmode_mux[5] : (CARRYINSEL == "CARRYIN")? CARRYIN : 0 ;
77
78
79  //buffer CARRYOUTF
80  assign CARRYOUTF = CARRYOUT;
81
82
83  //Arithmetic Operations
84  assign Pre_adder_out = (opmode_mux[6])? (D_mux - B0_mux) : (D_mux + B0_mux) ;
85  assign mult_out = A1_mux * B1_mux;
86  assign {CYO, Post_adder_out} = (opmode_mux[7])? (z_mux - (x_mux + CYI_mux)) : (z_mux + x_mux + CYI_mux) ;
```

D:\MiniProject\DSP.v - Sublime Text (UNREGISTERED)

reg_mux.v | module DSP48A1_tb (); | DSP.v | run_DSP.do | Constraints_basys3.xdc

```
74
75  //carry in
76  assign Carry_in_Cascade = (CARRYINSEL == "OPMODE5")? opmode_mux[5] : (CARRYINSEL == "CARRYIN")? CARRYIN : 0 ;
77
78
79  //buffer CARRYOUTF
80  assign CARRYOUTF = CARRYOUT;
81
82
83  //Arithmetic Operations
84  assign Pre_adder_out = (opmode_mux[6])? (D_mux - B0_mux) : (D_mux + B0_mux) ;
85  assign mult_out = A1_mux * B1_mux;
86  assign {CYO, Post_adder_out} = (opmode_mux[7])? (z_mux - (x_mux + CYI_mux)) : (z_mux + x_mux + CYI_mux) ;
87
88
89  //X & Z multiplexers
90  always @(*) begin
91
92      case (opmode_mux[1:0])
93        0 : x_mux = 0;
94        1 : x_mux = {{12{M_mux[35]}}, M_mux} ;
95        2 : x_mux = P;   //may cause compinational loop
96        3 : x_mux = {D_mux[11:0], A1_mux[17:0], B1_mux[17:0]};
97      endcase
98
99
100     case (opmode_mux[3:2])
101       0 : z_mux = 0;
102       1 : z_mux = PCIN;
103       2 : z_mux = P;   //may cause compinational loop
104       3 : z_mux = C_mux;
105     endcase
106 end
107
108
109 endmodule
```


D:\MiniProject\run_DSP.do - Sublime Text (UNREGISTERED)
reg_mux.v
DSP.v
DSP_tb.v
vlib work
vlog DSP.v Reg_Mux.v DSP_tb.v
vsim -voptargs=+acc work.DSP_tb
add wave *
run -all

```
module DSP_tb ();

parameter A0REG = 0,
          A1REG = 1,
          B0REG = 0,
          B1REG = 1,
          CREG = 1,
          DREG = 1,
          MREG = 1,
          PREG = 1,
          CARRYINREG = 1,
          CARRYOUTREG = 1,
          OPMODEREG = 1,
          CARRYINSEL = "OPMODE5",
          B_INPUT = "DIRECT",
          RSTTYPE = "SYNC";

 reg [17:0] A,B,D,BCIN;
 reg [47:0] C,PCIN;
 reg [7:0] OPMODE;
 reg CLK,CARRYIN;
 reg RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE;
 reg CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
 wire [17:0] BCOUT;
 wire [47:0] PCOUT,P;
 wire [35:0] M;
 wire CARRYOUT,CARRYOUTF;


////////instantiation
 DSP #(A0REG,A1REG,B0REG,B1REG,CREG,DREG,MREG,PREG,CARRYINREG,CARRYOUTREG,OPMODEREG,CARRYINSEL,B_INPUT,RSTTYPE) DUT(
    A,B,D,BCIN,C,PCIN,OPMODE,CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);


    //////////clock generation
 initial begin
    CLK=0;
    forever
        #1 CLK=~CLK;
 end




integer i;
initial begin
// Initialize and reset signals
    RSTA = 1; RSTB = 1; RSTM = 1; RSTP = 1; RSTC = 1; RSTD = 1; RSTCARRYIN = 1; RSTOPMODE = 1;
    CEA = 1; CEB = 1; CEM = 1; CEP = 1; CEC = 1; CED = 1; CECARRYIN = 1; CEOPMODE = 1;
```

D:\MiniProject\DSP_tb.v - Sublime Text (UNREGISTERED)

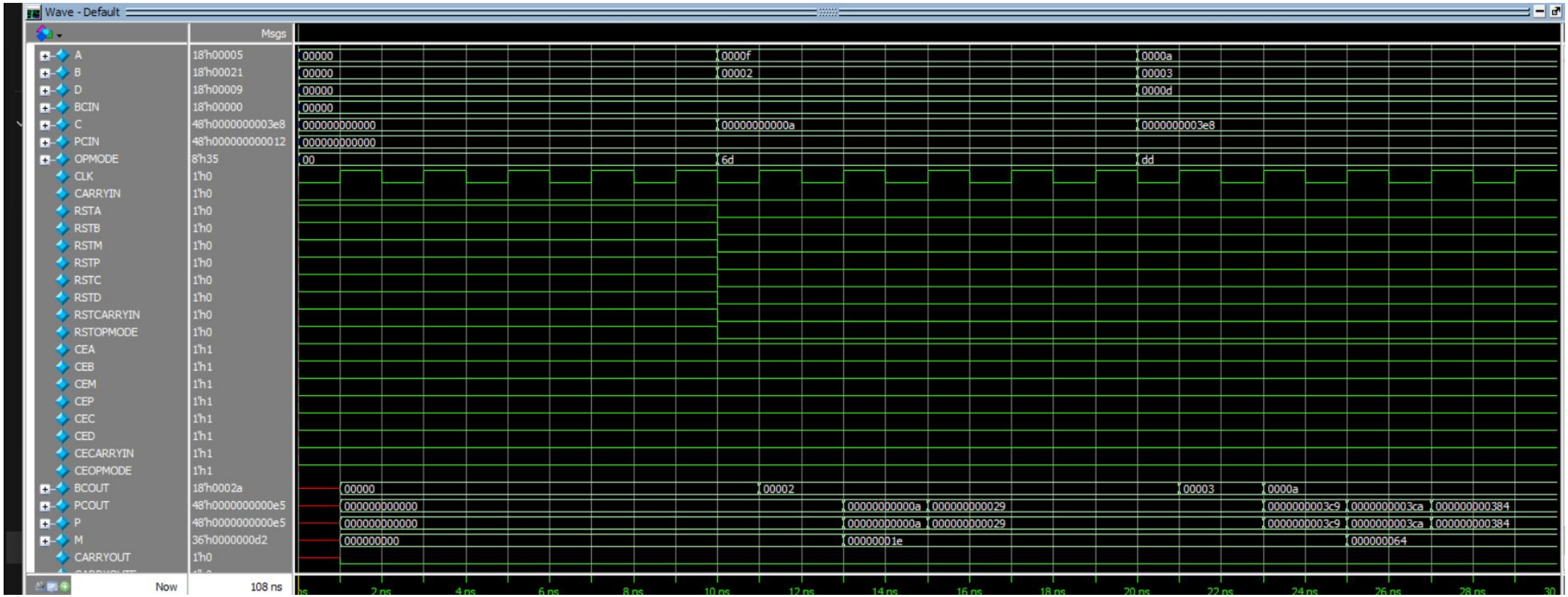
reg_mux.v | DSP.v | DSP_tb.v | run_DSP.do | Constraints_basys3.xdc

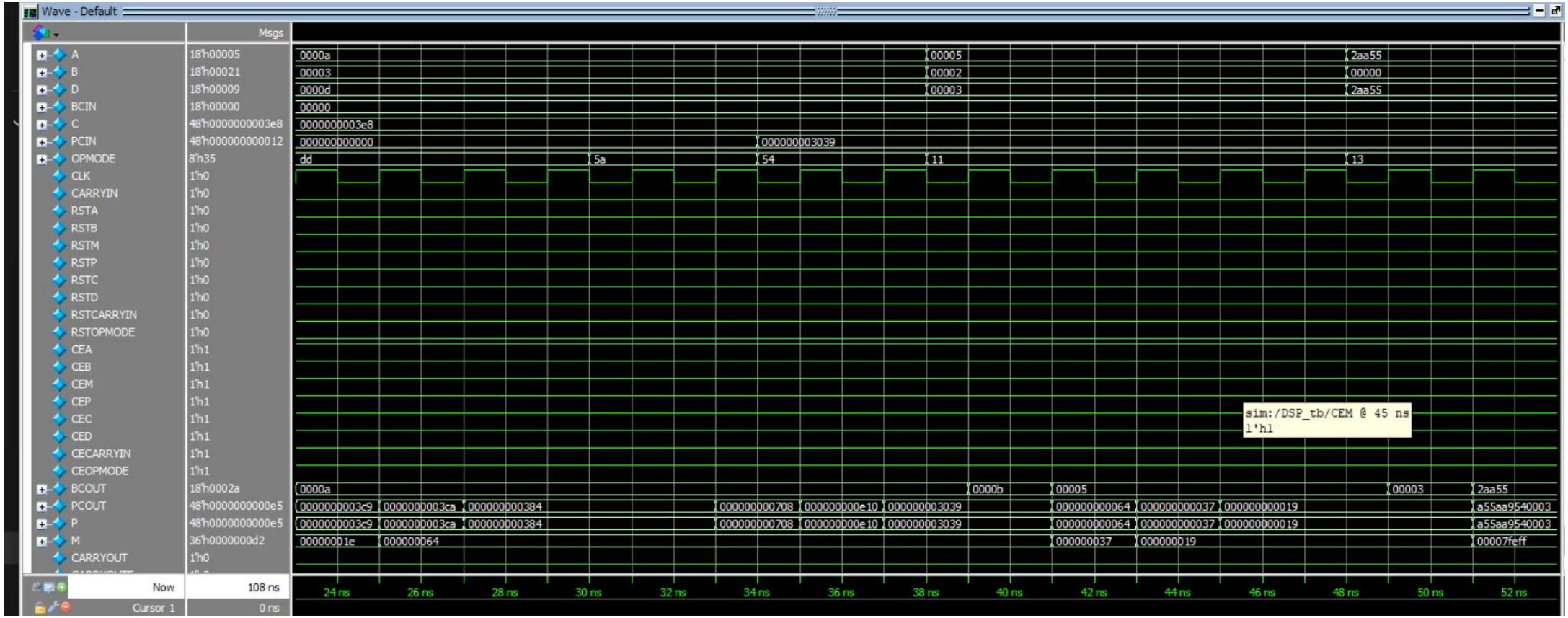
```
47  // Initialize and reset signals
48      RSTA = 1; RSTB = 1; RSTM = 1; RSTP = 1; RSTC = 1; RSTD = 1; RSTCARRYIN = 1; RSTOPMODE = 1;
49      CEA = 1; CEB = 1; CEM = 1; CEP = 1; CEC = 1; CED = 1; CECARRYIN = 1; CEOPMODE = 1;
50      A = 0; B = 0; C = 0; D = 0; CARRYIN = 0; BCIN = 0; PCIN = 0;
51      OPMODE = 8'b00000000;
52      repeat(5)
53       @(negedge CLK);
54
55      // reset signal
56      RSTA = 0; RSTB = 0;
57      RSTM = 0;
58      RSTP = 0;
59      RSTC = 0;
60      RSTD = 0;
61      RSTCARRYIN = 0;
62      RSTOPMODE = 0;
63
64
65      //B*A+C+opmode[5] =41
66      OPMODE=8'b01101101;
67      A=15;B=2;C=10;
68      repeat(5)
69      @(negedge CLK);
70
71
72
73      //C-((D-B)*A)=1000-((13-3)*10)=900
74      OPMODE=8'b11011101;
75      D=13;B=3;A=10;C=1000;
76      repeat(5)
77      @(negedge CLK);
78
79
80
81      //X_m=P,Z_m=P:x+z=900+900=1800
82      OPMODE=8'b01011010;
83      repeat(2)
84      @(negedge CLK);
85
86
87      //P=PCIN=12345;
88      OPMODE=8'b01010100;
89      PCIN=12345;
90      repeat(2)
91      @(negedge CLK);
92
93
94
95      //(D+B)*A=25
```

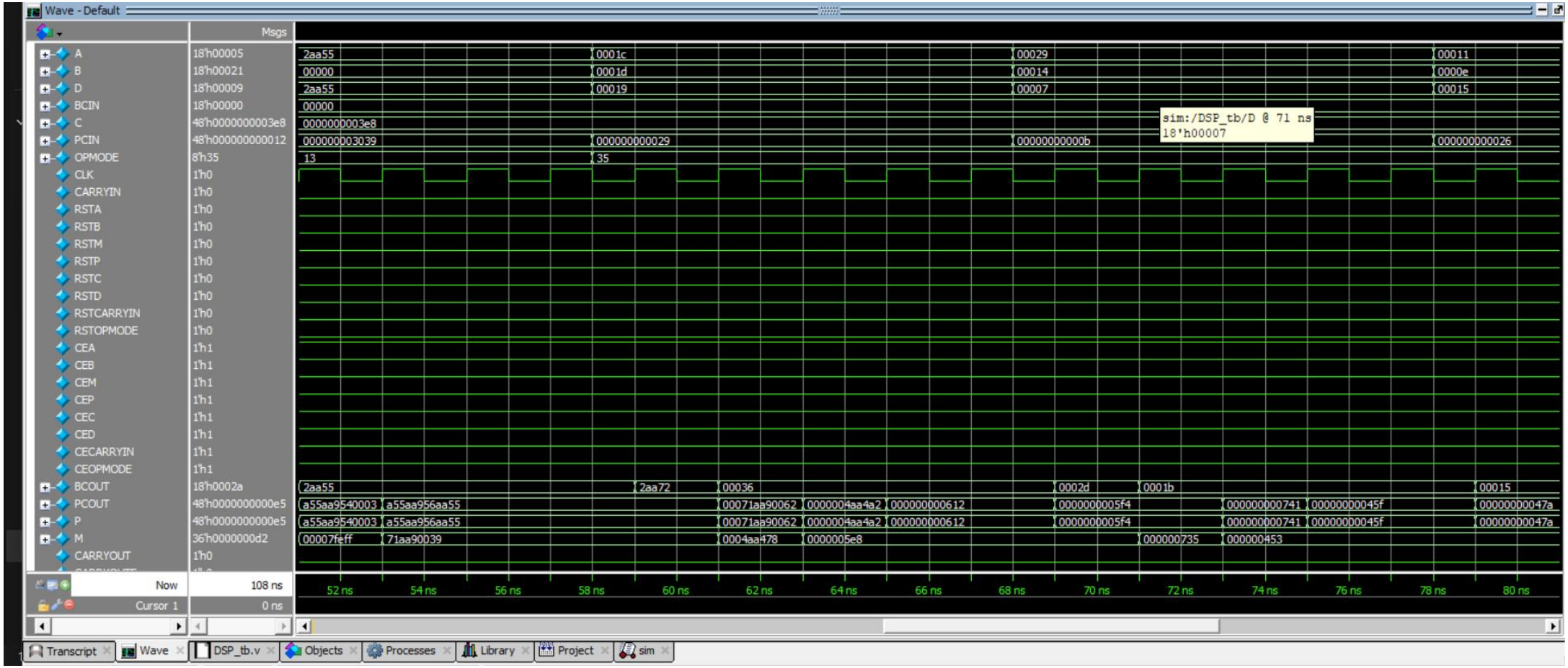
D:\MiniProject\DSP_tb.v - Sublime Text (UNREGISTERED)

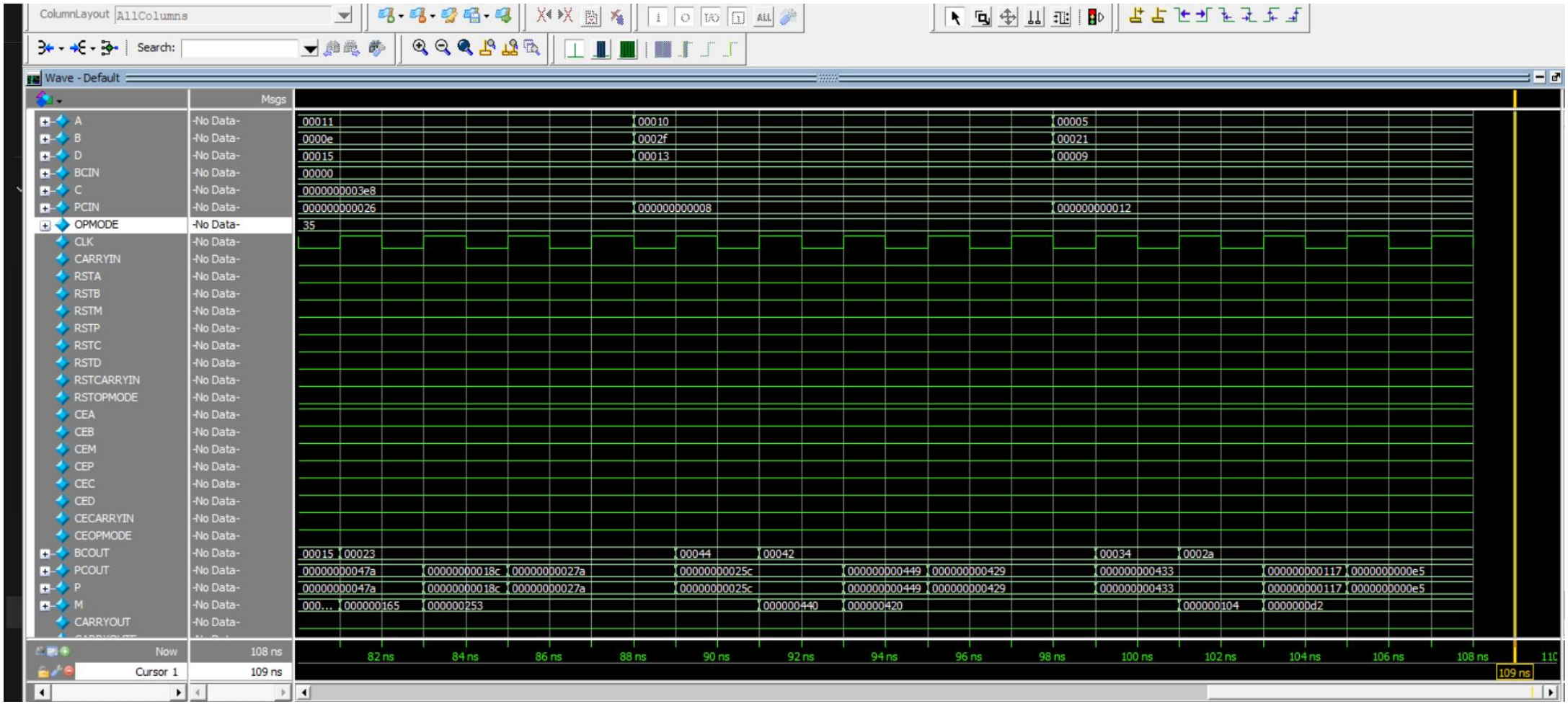
reg_mux.v | DSP.v | DSP_tb.v | run_DSP.do | Constraints_basys3.xdc

```
89      PCIN=12345;
90      repeat(2)
91      @(negedge CLK);
92
93
94
95      //(D+B)*A=25
96      OPMODE=8'b00010001;
97      D=3;B=2;A=5;
98      repeat(5)
99      @(negedge CLK);
100
101
102     OPMODE = 8'b00010011;
103     D=20'b10101010101001010101;
104     B=0;
105     A=20'b10101010101001010101;
106     repeat(5)
107     @(negedge CLK);
108     $display("P=%b",P);
109
110
111     OPMODE = 8'b00110101;
112     for(i=0;i<5;i=i+1) begin
113         A=$urandom_range(1,50);
114         B=$urandom_range(1,50);
115         D=$urandom_range(1,50);
116         PCIN=$urandom_range(1,50);
117         repeat(5)
118         @(negedge CLK);
119     end
120
121     $stop;
122 end
123
124 initial begin
125     $monitor("A=%d, B=%d, C=%d, D=%d, CARRYIN=%d ,PCIN=%d , OPMODE=%b, P=%d,BCOUT=%d ,M=%d ,CARRYOUT=%d", A, B, C, D,CARRYIN ,PCIN , OPMODE, P,BCOUT ,M , CARRYOUT);
126 end
127 endmodule
128
```


Wave - Default
Msgs
A
B
D
BCIN
C
PCIN
OPMODE
CLK
CARRYIN
RSTA
RSTB
RSTM
RSTP
RSTC
RSTD
RSTCARRYIN
RSTOPMODE
CEA
CEB
CEM
CEP
CEC
CED
CECARRYIN
CEOPMODE
BCOUT
PCOUT
P
M
CARRYOUT
18'h00005
18'h00021
18'h00009
18'h00000
48'h0000000003e8
48'h000000000012
8'h35
1'h0
1'h1
18'h0002a
48'h0000000000e5
48'h0000000000e5
36'h0000000d2
00000
0000f
0000a
00002
00003
0000d
0000000000a
0000000003e8
000000000000
00
6d
dd
0000000000a
000000000029
0000000003c9
0000000003ca
000000000384
000000000000
000000000
000000001e
000000064
Now
108 ns
2 ns
4 ns
6 ns
8 ns
10 ns
12 ns
14 ns
16 ns
18 ns
20 ns
22 ns
24 ns
26 ns
28 ns
30


Wave - Default
Msgs
A 18'h00005
B 18'h00021
D 18'h00009
BCIN 18'h00000
C 48'h0000000003e8
PCIN 48'h000000000012
OPMODE 8'h35
CLK 1'h0
CARRYIN 1'h0
RSTA 1'h0
RSTB 1'h0
RSTM 1'h0
RSTP 1'h0
RSTC 1'h0
RSTD 1'h0
RSTCARRYIN 1'h0
RSTOPMODE 1'h0
CEA 1'h1
CEB 1'h1
CEM 1'h1
CEP 1'h1
CEC 1'h1
CED 1'h1
CECARRYIN 1'h1
CEOPMODE 1'h1
BCOUT 18'h0002a
PCOUT 48'h0000000000e5
P 48'h0000000000e5
M 36'h0000000d2
CARRYOUT 1'h0
0000a
00005
2aa55
00003
00002
00000
0000d
00003
2aa55
00000
0000000003e8
000000000000
000000003039
dd
5a
54
11
13
sim:/DSP_tb/CEM @ 45 ns
1'h1
0000a
0000b
00005
00003
2aa55
0000000003c9
0000000003ca
000000000384
000000000708
000000000e10
000000003039
000000000064
000000000037
000000000019
a55aa9540003
000000001e
000000064
000000037
000000019
00007feff
Now
108 ns
Cursor 1
0 ns
24 ns
26 ns
28 ns
30 ns
32 ns
34 ns
36 ns
38 ns
40 ns
42 ns
44 ns
46 ns
48 ns
50 ns
52 ns


Wave - Default
Msgs
A 18'h00005 2aa55 0001c 00029 00011
B 18'h00021 00000 0001d 00014 0000e
D 18'h00009 2aa55 00019 00007 00015
BCIN 18'h00000 00000
C 48'h0000000003e8 0000000003e8
PCIN 48'h000000000012 000000003039 000000000029 00000000000b 000000000026
OPMODE 8'h35 13 35
sim:/DSP_tb/D @ 71 ns
18'h00007
CLK 1'h0
CARRYIN 1'h0
RSTA 1'h0
RSTB 1'h0
RSTM 1'h0
RSTP 1'h0
RSTC 1'h0
RSTD 1'h0
RSTCARRYIN 1'h0
RSTOPMODE 1'h0
CEA 1'h1
CEB 1'h1
CEM 1'h1
CEP 1'h1
CEC 1'h1
CED 1'h1
CECARRYIN 1'h1
CEOPMODE 1'h1
BCOUT 18'h0002a 2aa55 2aa72 00036 0002d 0001b 00015
PCOUT 48'h0000000000e5 a55aa9540003 a55aa956aa55 00071aa90062 0000004aa4a2 000000000612 0000000005f4 000000000741 00000000045f 00000000047a
P 48'h0000000000e5 a55aa9540003 a55aa956aa55 00071aa90062 0000004aa4a2 000000000612 0000000005f4 000000000741 00000000045f 00000000047a
M 36'h0000000d2 00007feff 71aa90039 0004aa478 0000005e8 000000735 000000453
CARRYOUT 1'h0
Now 108 ns
Cursor 1 0 ns
52 ns 54 ns 56 ns 58 ns 60 ns 62 ns 64 ns 66 ns 68 ns 70 ns 72 ns 74 ns 76 ns 78 ns 80 ns
Transcript
Wave
DSP_tb.v
Objects
Processes
Library
Project
sim


ColumnLayout
AllColumns
Search:
Wave - Default
Msgs
A
B
D
BCIN
C
PCIN
OPMODE
CLK
CARRYIN
RSTA
RSTB
RSTM
RSTP
RSTC
RSTD
RSTCARRYIN
RSTOPMODE
CEA
CEB
CEM
CEP
CEC
CED
CECARRYIN
CEOPMODE
BCOUT
PCOUT
P
M
CARRYOUT
-No Data-
00011
00010
00005
0000e
0002f
00021
00015
00013
00009
00000
0000000003e8
000000000026
000000000008
000000000012
35
00015
00023
00044
00042
00034
0002a
00000000047a
00000000018c
00000000027a
00000000025c
000000000449
000000000429
000000000433
000000000117
0000000000e5
000...
000000165
000000253
000000440
000000420
000000104
0000000d2
Now
108 ns
Cursor 1
109 ns
82 ns
84 ns
86 ns
88 ns
90 ns
92 ns
94 ns
96 ns
98 ns
100 ns
102 ns
104 ns
106 ns
108 ns
109 ns

D:\MiniProject\Constraints_basys3.xdc - Sublime Text (UNREGISTERED)

reg_mux.v | DSP.v | DSP_tb.v | run_DSP.do | Constraints_basys3.xdc

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

## Clock signal
set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports clk]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports clk]


## Switches
#set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports {sw[0]}]
#set_property -dict { PACKAGE_PIN V16   IOSTANDARD LVCMOS33 } [get_ports {sw[1]}]
#set_property -dict { PACKAGE_PIN W16   IOSTANDARD LVCMOS33 } [get_ports {sw[2]}]
#set_property -dict { PACKAGE_PIN W17   IOSTANDARD LVCMOS33 } [get_ports {sw[3]}]
#set_property -dict { PACKAGE_PIN W15   IOSTANDARD LVCMOS33 } [get_ports {sw[4]}]
#set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports {sw[5]}]
#set_property -dict { PACKAGE_PIN W14   IOSTANDARD LVCMOS33 } [get_ports {sw[6]}]
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports {sw[7]}]
#set_property -dict { PACKAGE_PIN V2    IOSTANDARD LVCMOS33 } [get_ports {sw[8]}]
```

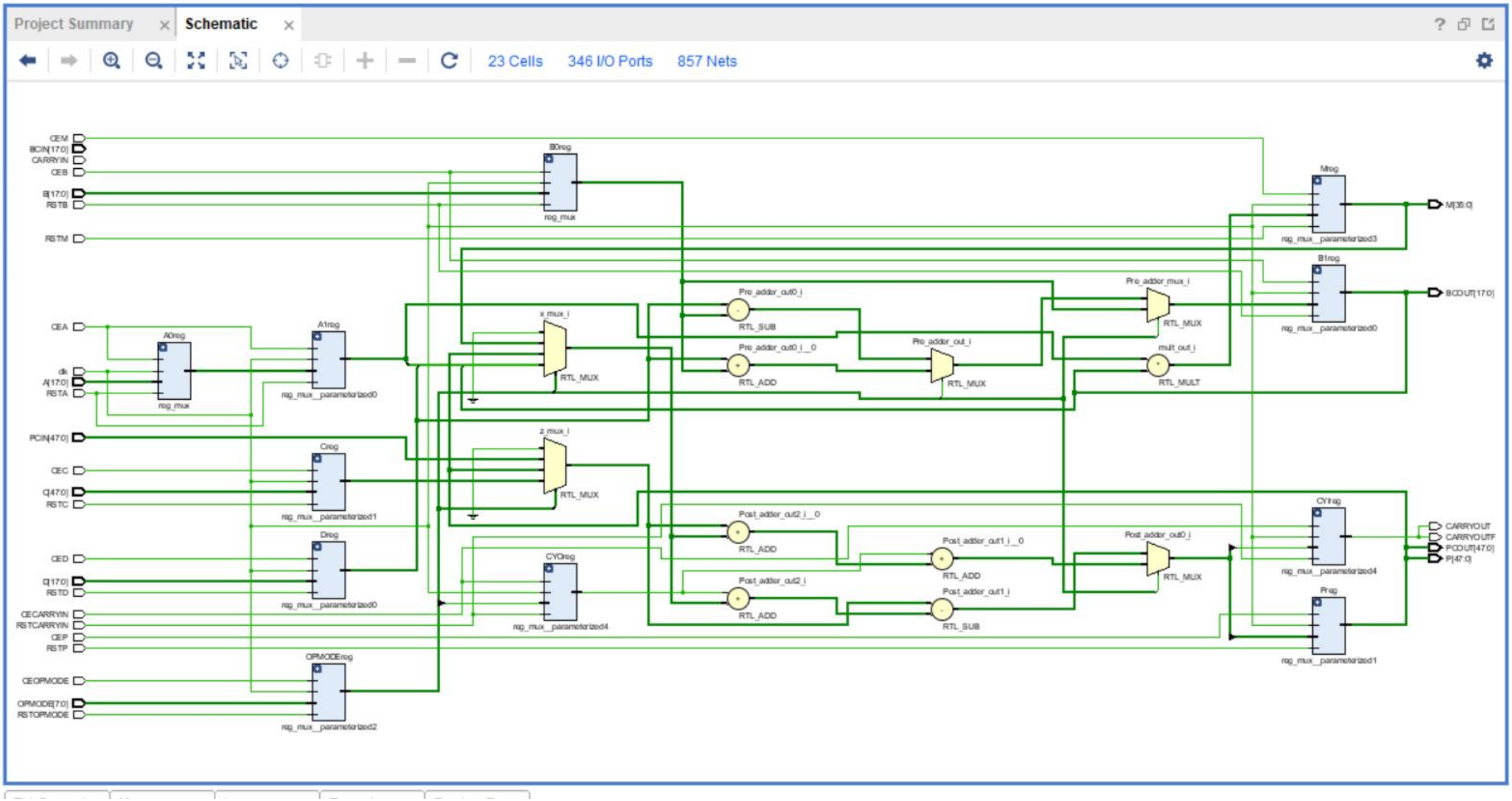
```
#set_property -dict { PACKAGE_PIN K19   IOSTANDARD LVCMOS33 } [get_ports QspiCSn]


## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]

create_debug_core u_ila_0 ila
set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
set_property port_width 1 [get_debug_ports u_ila_0/clk]
connect_debug_port u_ila_0/clk [get_nets [list clk_IBUF_BUFG]]
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
set_property port_width 8 [get_debug_ports u_ila_0/probe0]
connect_debug_port u_ila_0/probe0 [get_nets [list {OPMODE_IBUF[0]} {OPMODE_IBUF[1]} {OPMODE_IBUF[2]} {OPMODE_IBUF[3]} {OPMODE_IBUF[4]} {OPMODE_IBUF[5]} {OPMODE_IBUF[6]} {OPMODE_IBUF[7
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
set_property port_width 18 [get_debug_ports u_ila_0/probe1]
connect_debug_port u_ila_0/probe1 [get_nets [list {D_IBUF[0]} {D_IBUF[1]} {D_IBUF[2]} {D_IBUF[3]} {D_IBUF[4]} {D_IBUF[5]} {D_IBUF[6]} {D_IBUF[7]} {D_IBUF[8]} {D_IBUF[9]} {D_IBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
set_property port_width 36 [get_debug_ports u_ila_0/probe2]
connect_debug_port u_ila_0/probe2 [get_nets [list {M_OBUF[0]} {M_OBUF[1]} {M_OBUF[2]} {M_OBUF[3]} {M_OBUF[4]} {M_OBUF[5]} {M_OBUF[6]} {M_OBUF[7]} {M_OBUF[8]} {M_OBUF[9]} {M_OBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
set_property port_width 48 [get_debug_ports u_ila_0/probe3]
connect_debug_port u_ila_0/probe3 [get_nets [list {C_IBUF[0]} {C_IBUF[1]} {C_IBUF[2]} {C_IBUF[3]} {C_IBUF[4]} {C_IBUF[5]} {C_IBUF[6]} {C_IBUF[7]} {C_IBUF[8]} {C_IBUF[9]} {C_IBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
set_property port_width 18 [get_debug_ports u_ila_0/probe4]
connect_debug_port u_ila_0/probe4 [get_nets [list {BCOUT_OBUF[0]} {BCOUT_OBUF[1]} {BCOUT_OBUF[2]} {BCOUT_OBUF[3]} {BCOUT_OBUF[4]} {BCOUT_OBUF[5]} {BCOUT_OBUF[6]} {BCOUT_OBUF[7]} {BCOU
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe5]
set_property port_width 18 [get_debug_ports u_ila_0/probe5]
connect_debug_port u_ila_0/probe5 [get_nets [list {A_IBUF[0]} {A_IBUF[1]} {A_IBUF[2]} {A_IBUF[3]} {A_IBUF[4]} {A_IBUF[5]} {A_IBUF[6]} {A_IBUF[7]} {A_IBUF[8]} {A_IBUF[9]} {A_IBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe6]
```

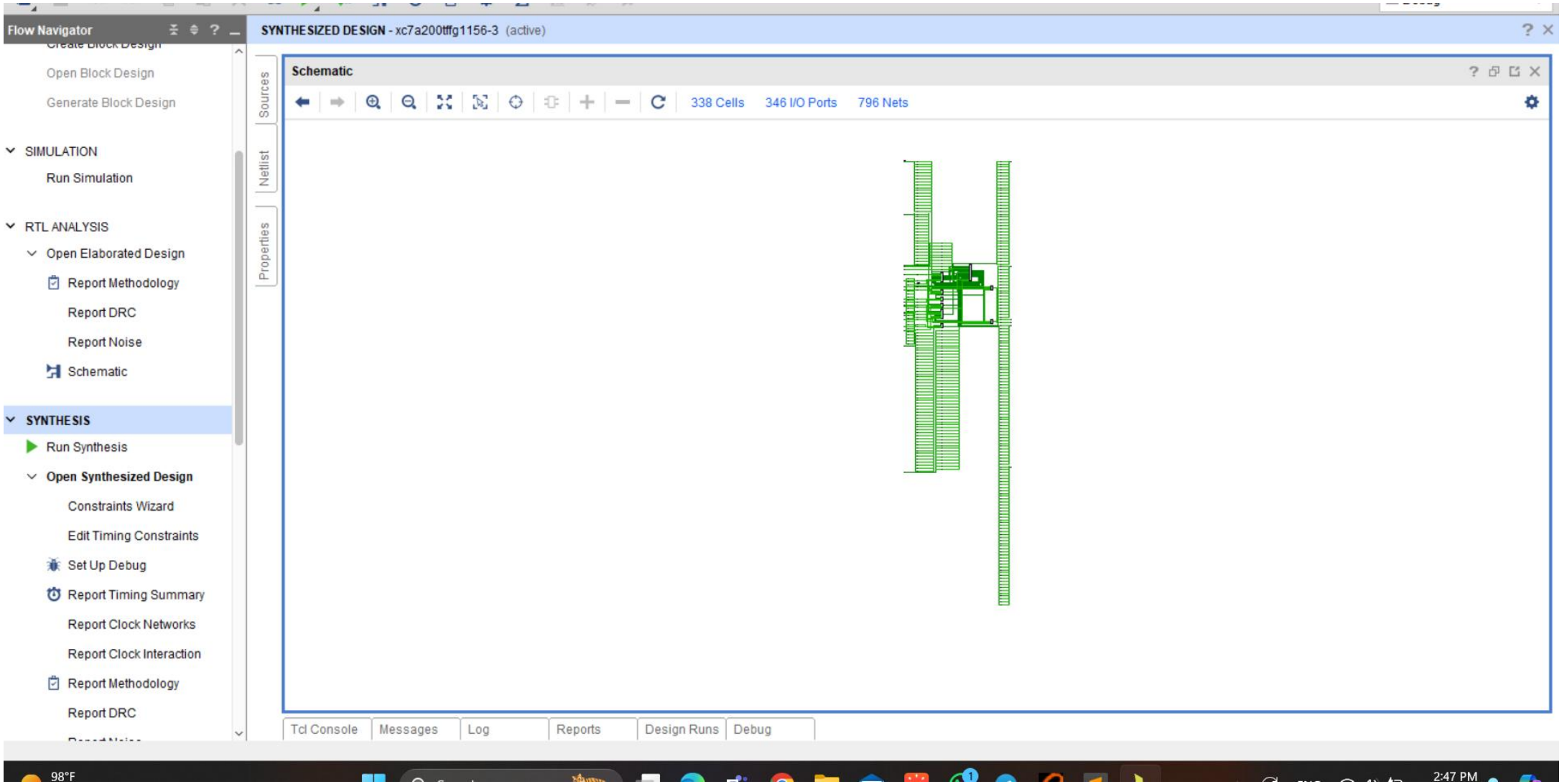
reg_mux.v | DSP.v | DSP_tb.v | run_DSP.do | Constraints_basys3.xdc

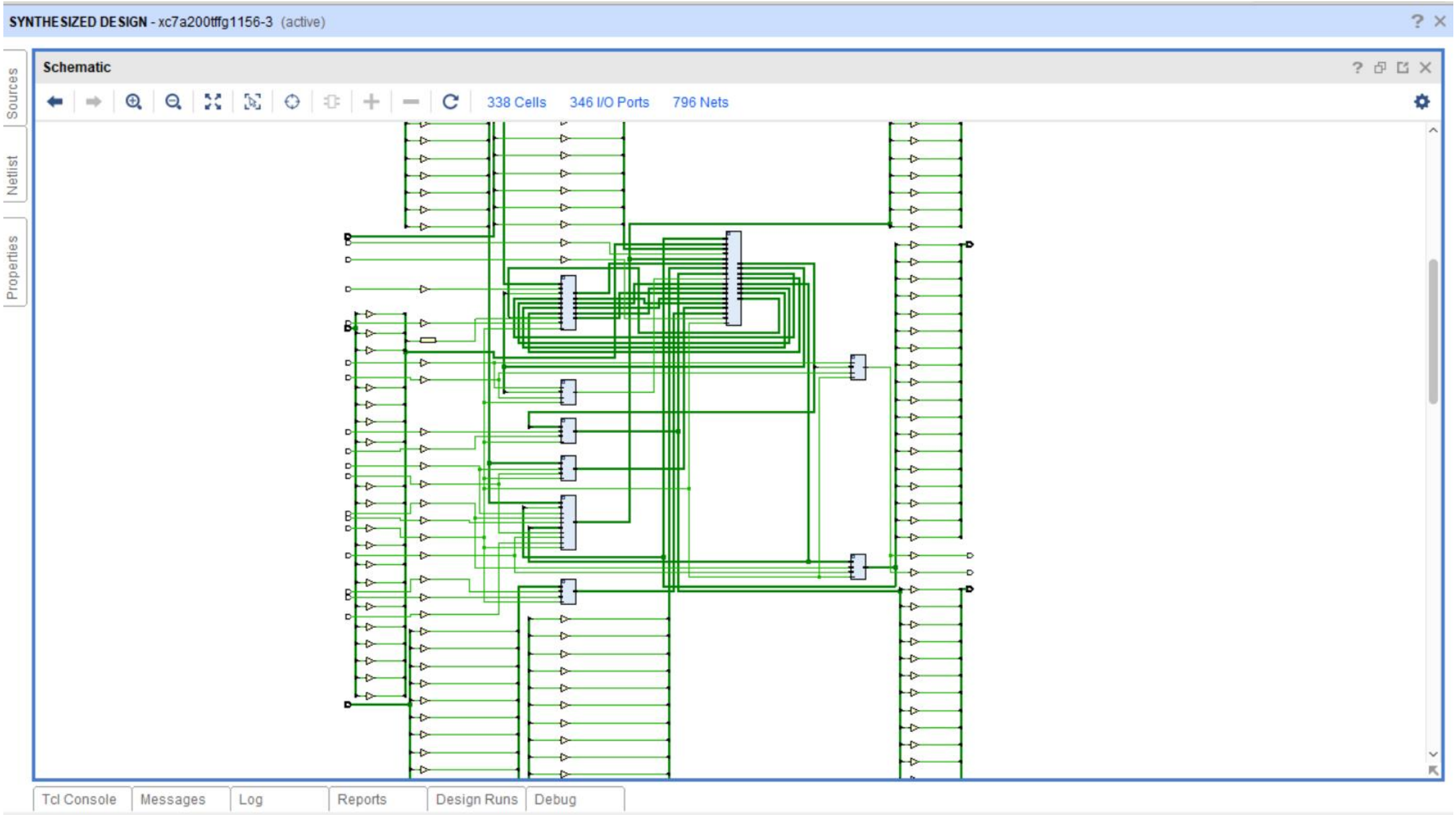
```
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
set_property port_width 18 [get_debug_ports u_ila_0/probe4]
connect_debug_port u_ila_0/probe4 [get_nets [list {BCOUT_OBUF[0]} {BCOUT_OBUF[1]} {BCOUT_OBUF[2]} {BCOUT_OBUF[3]} {BCOUT_OBUF[4]} {BCOUT_OBUF[5]} {BCOUT_OBUF[6]} {BCOUT_OBUF[7]} {BCOU
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe5]
set_property port_width 18 [get_debug_ports u_ila_0/probe5]
connect_debug_port u_ila_0/probe5 [get_nets [list {A_IBUF[0]} {A_IBUF[1]} {A_IBUF[2]} {A_IBUF[3]} {A_IBUF[4]} {A_IBUF[5]} {A_IBUF[6]} {A_IBUF[7]} {A_IBUF[8]} {A_IBUF[9]} {A_IBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe6]
set_property port_width 18 [get_debug_ports u_ila_0/probe6]
connect_debug_port u_ila_0/probe6 [get_nets [list {B_IBUF[0]} {B_IBUF[1]} {B_IBUF[2]} {B_IBUF[3]} {B_IBUF[4]} {B_IBUF[5]} {B_IBUF[6]} {B_IBUF[7]} {B_IBUF[8]} {B_IBUF[9]} {B_IBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe7]
set_property port_width 48 [get_debug_ports u_ila_0/probe7]
connect_debug_port u_ila_0/probe7 [get_nets [list {PCIN_IBUF[0]} {PCIN_IBUF[1]} {PCIN_IBUF[2]} {PCIN_IBUF[3]} {PCIN_IBUF[4]} {PCIN_IBUF[5]} {PCIN_IBUF[6]} {PCIN_IBUF[7]} {PCIN_IBUF[8]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe8]
set_property port_width 48 [get_debug_ports u_ila_0/probe8]
connect_debug_port u_ila_0/probe8 [get_nets [list {P_OBUF[0]} {P_OBUF[1]} {P_OBUF[2]} {P_OBUF[3]} {P_OBUF[4]} {P_OBUF[5]} {P_OBUF[6]} {P_OBUF[7]} {P_OBUF[8]} {P_OBUF[9]} {P_OBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe9]
set_property port_width 1 [get_debug_ports u_ila_0/probe9]
connect_debug_port u_ila_0/probe9 [get_nets [list CARRYOUTF_OBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe10]
set_property port_width 1 [get_debug_ports u_ila_0/probe10]
connect_debug_port u_ila_0/probe10 [get_nets [list CEA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
set_property port_width 1 [get_debug_ports u_ila_0/probe11]
connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
set_property port_width 1 [get_debug_ports u_ila_0/probe12]
connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
set_property port_width 1 [get_debug_ports u_ila_0/probe13]
connect_debug_port u_ila_0/probe13 [get_nets [list CECARRYIN_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
set_property port_width 1 [get_debug_ports u_ila_0/probe14]
connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
set_property port_width 1 [get_debug_ports u_ila_0/probe15]
connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
create_debug_port u_ila_0 probe
```

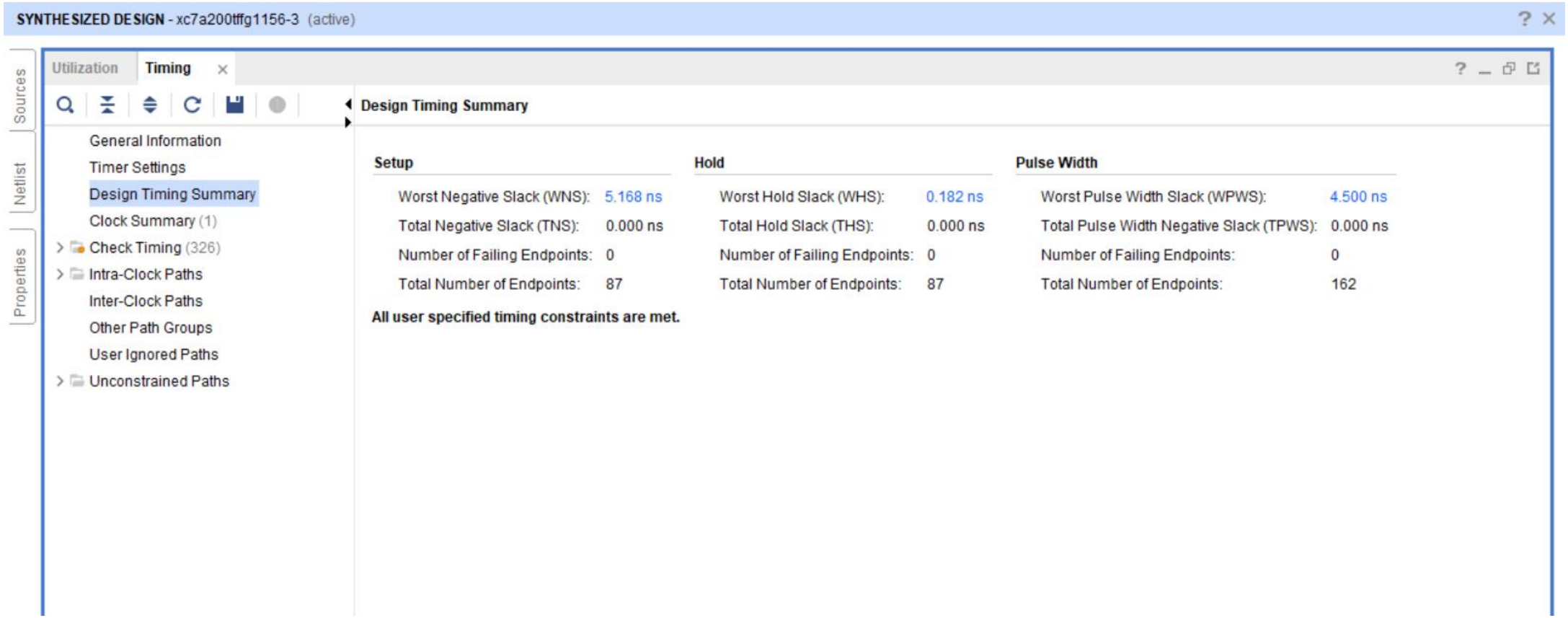
reg_mux.v | DSP.v | DSP_tb.v | run_DSP.do | Constraints_basys3.xdc

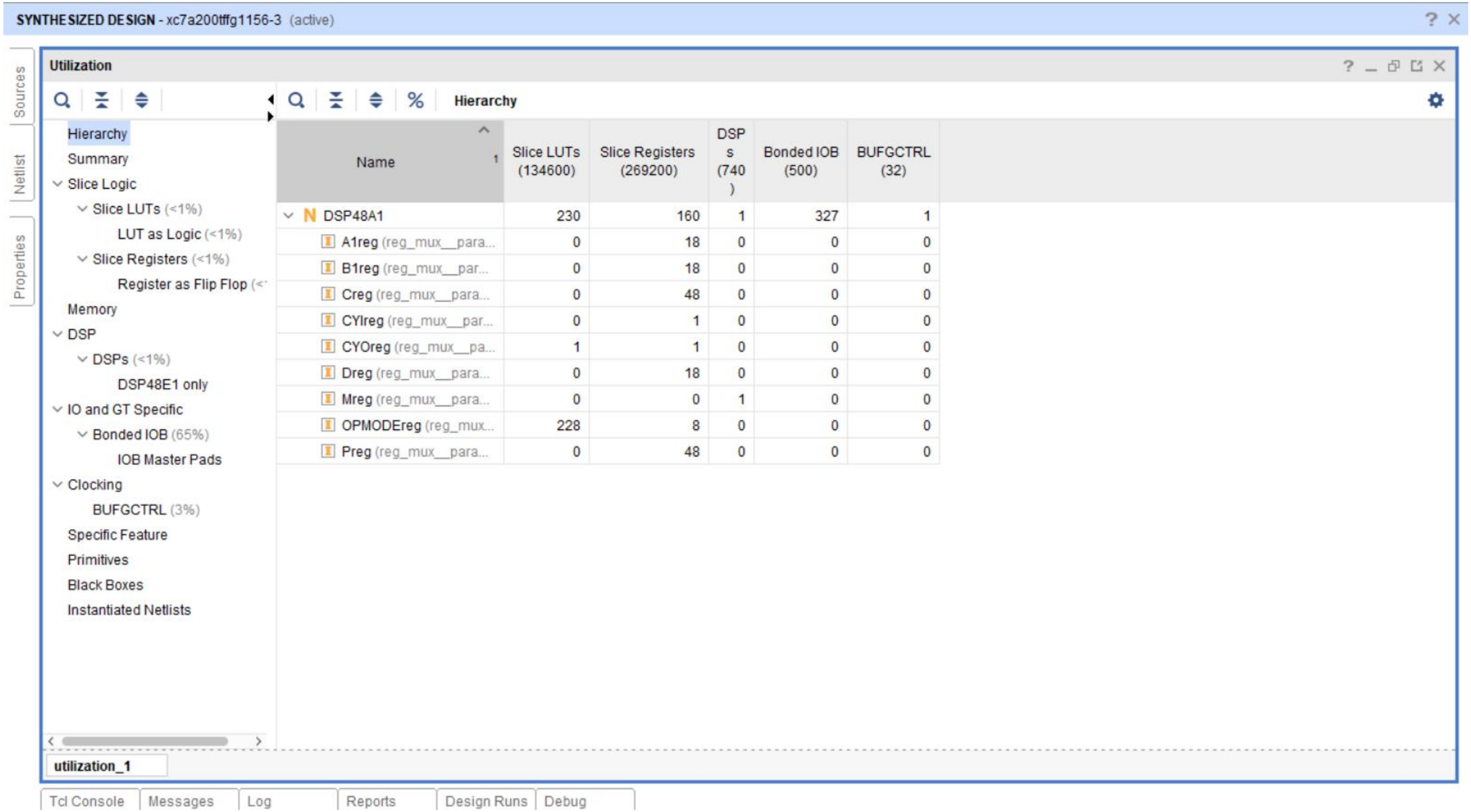
```
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe16]
set_property port_width 1 [get_debug_ports u_ila_0/probe16]
connect_debug_port u_ila_0/probe16 [get_nets [list CEOPMODE_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe17]
set_property port_width 1 [get_debug_ports u_ila_0/probe17]
connect_debug_port u_ila_0/probe17 [get_nets [list CEP_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
set_property port_width 1 [get_debug_ports u_ila_0/probe18]
connect_debug_port u_ila_0/probe18 [get_nets [list clk_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
set_property port_width 1 [get_debug_ports u_ila_0/probe19]
connect_debug_port u_ila_0/probe19 [get_nets [list RSTA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
set_property port_width 1 [get_debug_ports u_ila_0/probe20]
connect_debug_port u_ila_0/probe20 [get_nets [list RSTB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
set_property port_width 1 [get_debug_ports u_ila_0/probe21]
connect_debug_port u_ila_0/probe21 [get_nets [list RSTC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
set_property port_width 1 [get_debug_ports u_ila_0/probe22]
connect_debug_port u_ila_0/probe22 [get_nets [list RSTCARRYIN_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
set_property port_width 1 [get_debug_ports u_ila_0/probe23]
connect_debug_port u_ila_0/probe23 [get_nets [list RSTD_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
set_property port_width 1 [get_debug_ports u_ila_0/probe24]
connect_debug_port u_ila_0/probe24 [get_nets [list RSTM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe25]
set_property port_width 1 [get_debug_ports u_ila_0/probe25]
connect_debug_port u_ila_0/probe25 [get_nets [list RSTOPMODE_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe26]
set_property port_width 1 [get_debug_ports u_ila_0/probe26]
connect_debug_port u_ila_0/probe26 [get_nets [list RSTP_IBUF]]
set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
connect_debug_port dbg_hub/clk [get_nets clk_IBUF_BUFG]
```

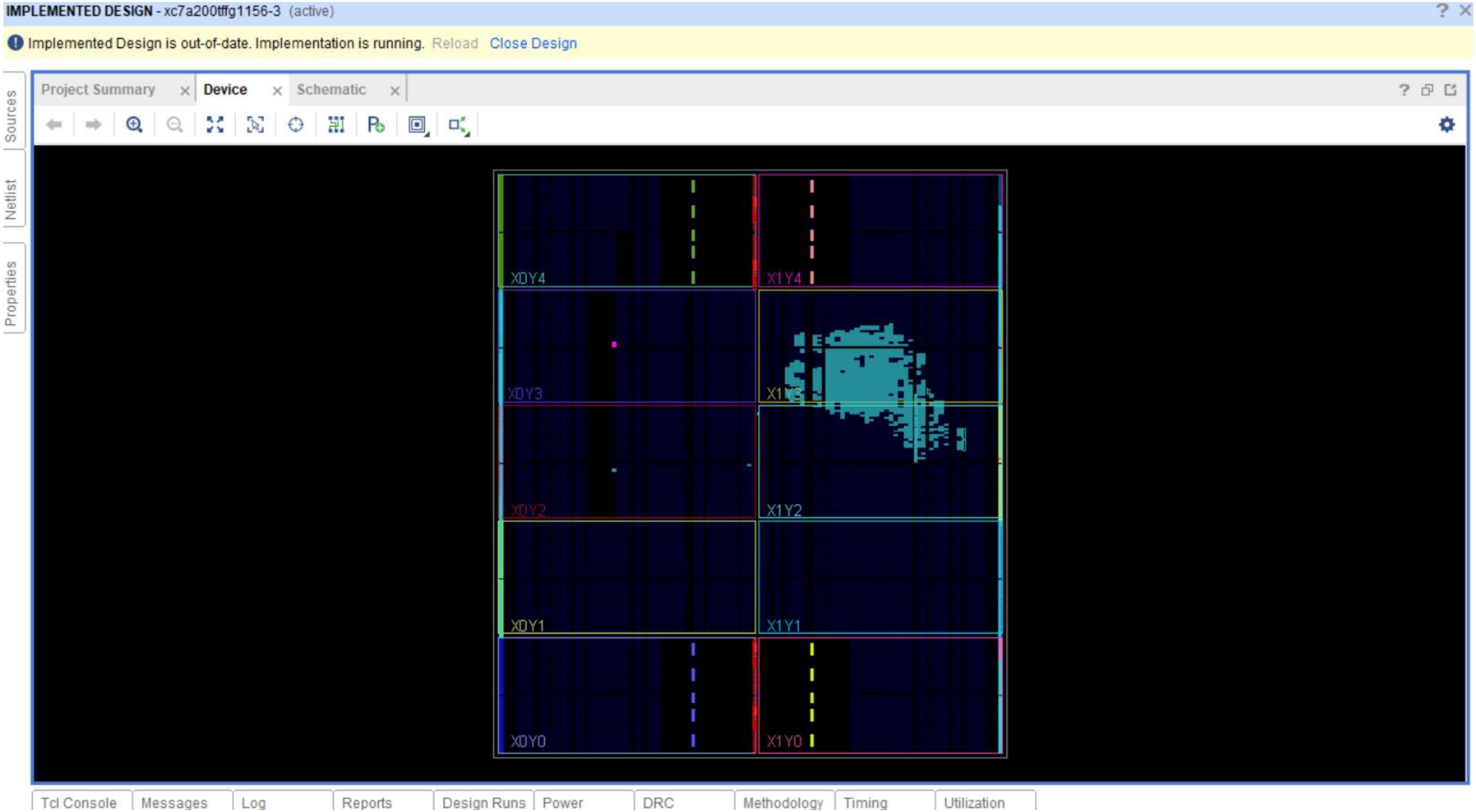

Project Summary
Schematic
23 Cells
346 I/O Ports
857 Nets
CEM
BCIN[17:0]
CARRYIN
CEB
B[17:0]
RSTB
RSTM
CEA
A[17:0]
RSTA
PCIN[47:0]
CEC
C[47:0]
RSTC
CED
D[17:0]
RSTD
CECARRYIN
RSTCARRYIN
CEP
RSTP
CEOPMODE
OPMODE[7:0]
RSTOPMODE
clk
B0reg
A0reg
A1reg
Creg
Dreg
CYOreg
OPMODEreg
reg_mux
reg_mux__parameterized0
reg_mux__parameterized1
reg_mux__parameterized2
reg_mux__parameterized4
x_mux_i
z_mux_i
RTL_MUX
Pre_adder_out0_i
Pre_adder_out0_i__0
RTL_SUB
RTL_ADD
Pre_adder_out_i
Pre_adder_mux_i
mult_out_i
RTL_MULT
Post_adder_out2_i__0
Post_adder_out2_i
Post_adder_out1_i__0
Post_adder_out1_i
Post_adder_out0_i
Mreg
B1reg
CYOreg
Preg
reg_mux__parameterized3
reg_mux__parameterized4
M[35:0]
BCOUT[17:0]
CARRYOUT
CARRYOUTF
PCOUT[47:0]
P[47:0]

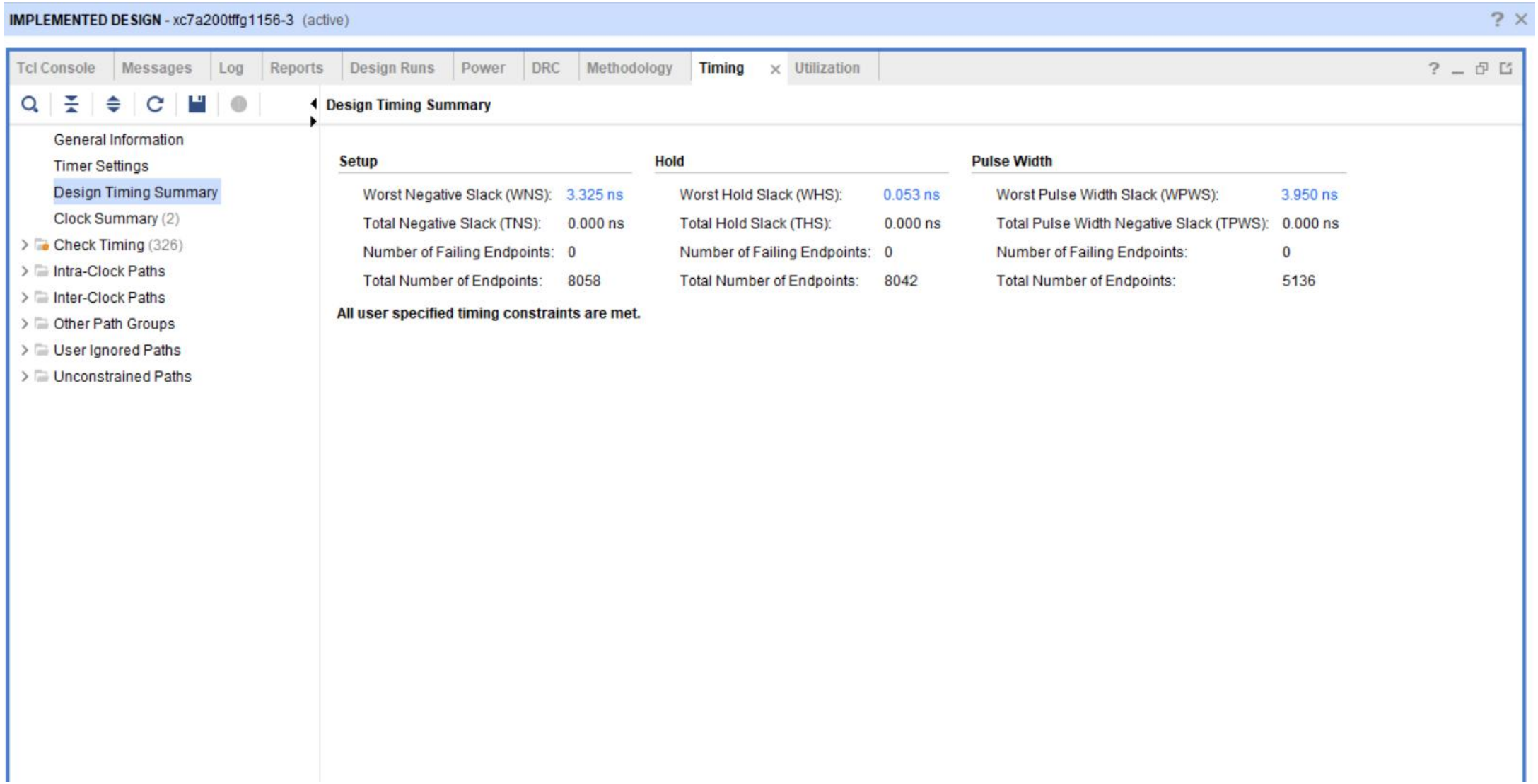

Flow Navigator
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
SYNTHESIZED DESIGN - xc7a200tffg1156-3 (active)
Sources
Netlist
Properties
Schematic
338 Cells
346 I/O Ports
796 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Debug
98°F
2:47 PM

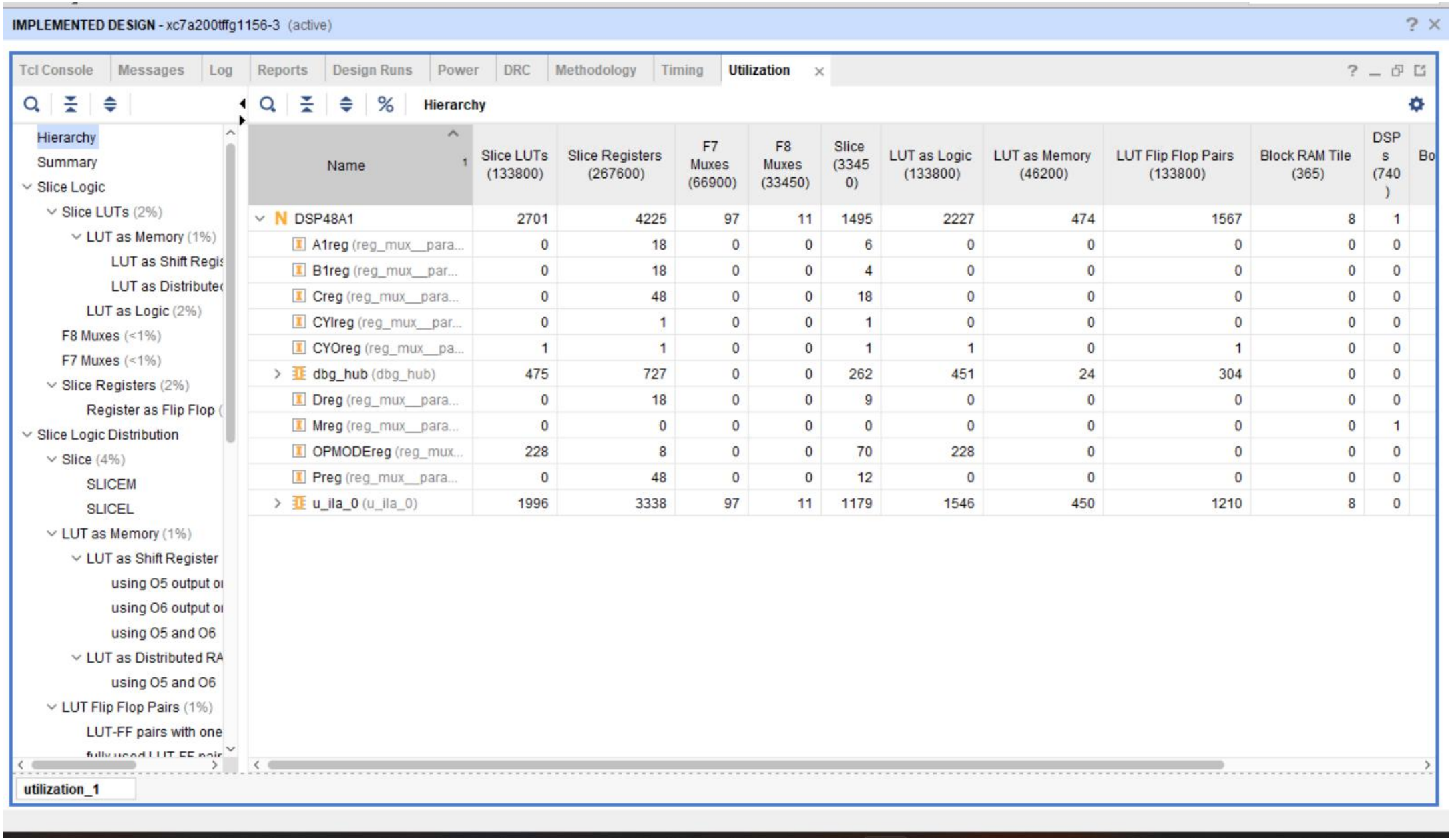

SYNTHESIZED DESIGN - xc7a200tffg1156-3 (active)
Schematic
338 Cells
346 I/O Ports
796 Nets
Sources
Netlist
Properties
Tcl Console
Messages
Log
Reports
Design Runs
Debug


SYNTHESIZED DESIGN - xc7a200tffg1156-3 (active)
Sources
Netlist
Properties
Utilization
Timing
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (326)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Design Timing Summary
Setup
Worst Negative Slack (WNS): 5.168 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 87
Hold
Worst Hold Slack (WHS): 0.182 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 87
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 162
All user specified timing constraints are met.


SYNTHESIZED DESIGN - xc7a200tffg1156-3 (active)
Utilization
Sources
Netlist
Properties
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Registers (<1%)
Register as Flip Flop (<
Memory
DSP
DSPs (<1%)
DSP48E1 only
IO and GT Specific
Bonded IOB (65%)
IOB Master Pads
Clocking
BUFGCTRL (3%)
Specific Feature
Primitives
Black Boxes
Instantiated Netlists
Hierarchy
Name
Slice LUTs (134600)
Slice Registers (269200)
DSPs (740)
Bonded IOB (500)
BUFGCTRL (32)
DSP48A1 230 160 1 327 1
A1reg (reg_mux__para... 0 18 0 0 0
B1reg (reg_mux__par... 0 18 0 0 0
Creg (reg_mux__para... 0 48 0 0 0
CYIreg (reg_mux__par... 0 1 0 0 0
CYOreg (reg_mux__pa... 1 1 0 0 0
Dreg (reg_mux__para... 0 18 0 0 0
Mreg (reg_mux__para... 0 0 1 0 0
OPMODEreg (reg_mux... 228 8 0 0 0
Preg (reg_mux__para... 0 48 0 0 0
utilization_1
Tcl Console
Messages
Log
Reports
Design Runs
Debug


IMPLEMENTED DESIGN - xc7a200tffg1156-3 (active)
Implemented Design is out-of-date. Implementation is running. Reload Close Design
Sources
Netlist
Properties
Project Summary
Device
Schematic
X0Y4
X1Y4
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Utilization


IMPLEMENTED DESIGN - xc7a200tffg1156-3 (active)
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Utilization
General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (326)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Design Timing Summary
Setup
Worst Negative Slack (WNS): 3.325 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 8058
Hold
Worst Hold Slack (WHS): 0.053 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 8042
Pulse Width
Worst Pulse Width Slack (WPWS): 3.950 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 5136
All user specified timing constraints are met.


IMPLEMENTED DESIGN - xc7a200tffg1156-3 (active)
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Utilization
Hierarchy
Summary
Slice Logic
Slice LUTs (2%)
LUT as Memory (1%)
LUT as Shift Regis
LUT as Distributed
LUT as Logic (2%)
F8 Muxes (<1%)
F7 Muxes (<1%)
Slice Registers (2%)
Register as Flip Flop
Slice Logic Distribution
Slice (4%)
SLICEM
SLICEL
LUT as Memory (1%)
LUT as Shift Register
using O5 output o
using O6 output o
using O5 and O6
LUT as Distributed RA
using O5 and O6
LUT Flip Flop Pairs (1%)
LUT-FF pairs with one
Hierarchy
Name
Slice LUTs (133800)
Slice Registers (267600)
F7 Muxes (66900)
F8 Muxes (33450)
Slice (33450)
LUT as Logic (133800)
LUT as Memory (46200)
LUT Flip Flop Pairs (133800)
Block RAM Tile (365)
DSPs (740)
Bo
DSP48A1 2701 4225 97 11 1495 2227 474 1567 8 1
A1reg (reg_mux__para... 0 18 0 0 6 0 0 0 0 0
B1reg (reg_mux__par... 0 18 0 0 4 0 0 0 0 0
Creg (reg_mux__para... 0 48 0 0 18 0 0 0 0 0
CYIreg (reg_mux__par... 0 1 0 0 1 0 0 0 0 0
CYOreg (reg_mux__pa... 1 1 0 0 1 1 0 1 0 0
dbg_hub (dbg_hub) 475 727 0 0 262 451 24 304 0 0
Dreg (reg_mux__para... 0 18 0 0 9 0 0 0 0 0
Mreg (reg_mux__para... 0 0 0 0 0 0 0 0 0 1
OPMODEreg (reg_mux... 228 8 0 0 70 228 0 0 0 0
Preg (reg_mux__para... 0 48 0 0 12 0 0 0 0 0
u_ila_0 (u_ila_0) 1996 3338 97 11 1179 1546 450 1210 8 0
utilization_1


IMPLEMENTED DESIGN - xc7a200tffg1156-3 (active)
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Utilization
Warning (49)
Info (250)
Status (492)
Show All
Synthesis (43 warnings)
[Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP.v:1]
[Synth 8-3331] design reg_mux has unconnected port rst (40 more like this)
[Constraints 18-5210] No constraint will be written out.
Implementation (2 warnings)
Implemented Design (2 warnings)
General Messages (2 warnings)
[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met. (1 more like this)