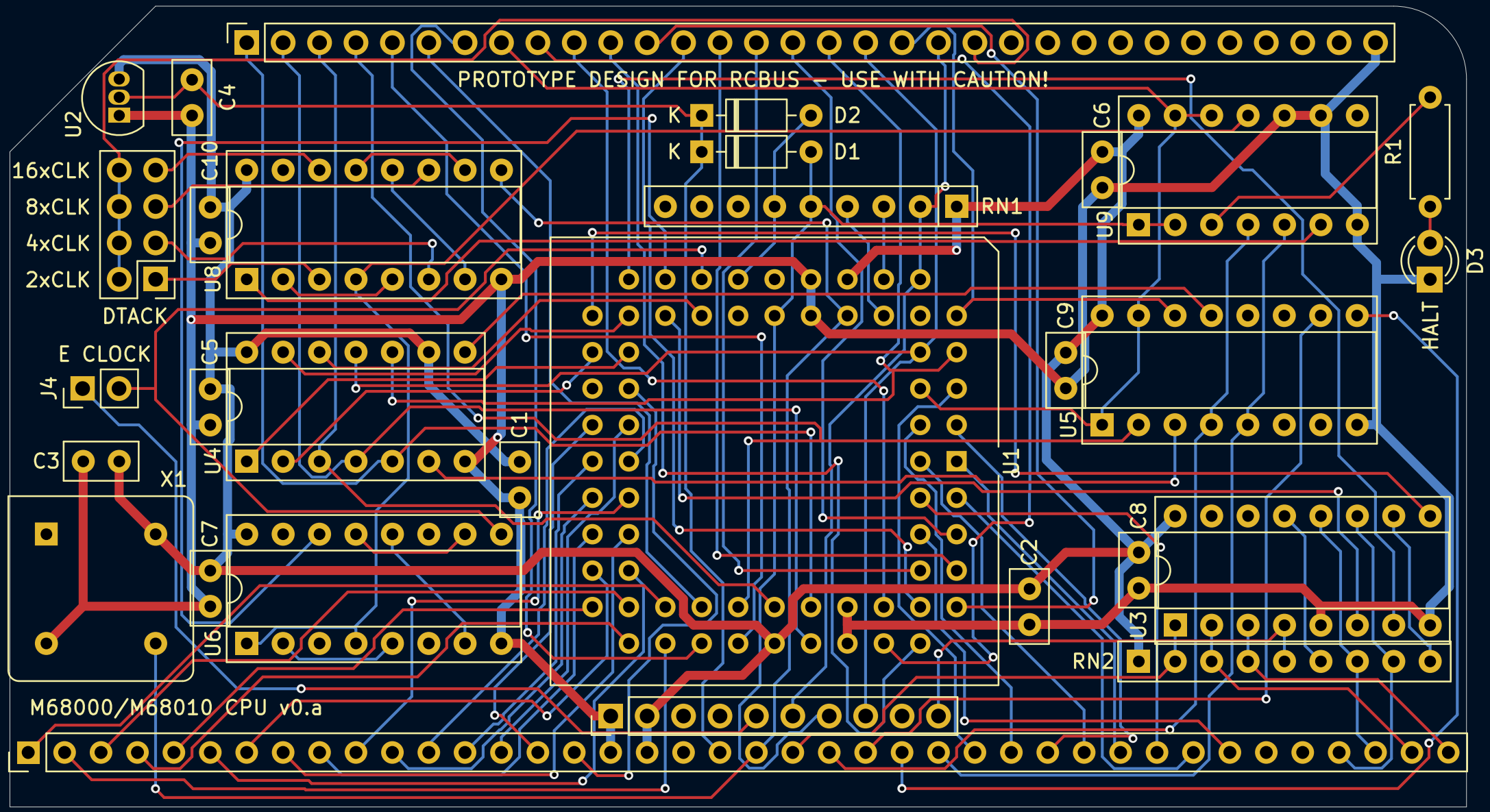
PROTOTYPE DESIGN FOR RCBUS - USE WITH CAUTION!
U2
C4
16xCLK
8xCLK
4xCLK
2xCLK
DTACK
E CLOCK
J4
C3
X1
C10
U8
C5
U4
C7
U6
C1
K
D2
K
D1
RN1
C6
U9
R1
D3
HALT
C9
U5
U1
C8
U3
C2
RN2
M68000/M68010 CPU v0.a