

June 1999

ADC0844/ADC0848 8-Bit μP Compatible A/D Converters with Multiplexer Options

General Description

The ADC0844 and ADC0848 are CMOS 8-bit successive approximation A/D converters with versatile analog input multiplexers. The 4-channel or 8-channel multiplexers can be software configured for single-ended, differential or pseudo-differential modes of operation.

The differential mode provides low frequency input common mode rejection and allows offsetting the analog range of the converter. In addition, the A/D's reference can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

The A/Ds are designed to operate from the control bus of a wide variety of microprocessors. TRI-STATE® output latches that directly drive the data bus permit the A/Ds to be configured as memory locations or I/O devices to the microprocessor with no interface logic necessary.

Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 4-channel or 8-channel multiplexer with address logic
- Internal clock
- 0V to 5V input range with single 5V power supply
- 0.3" standard width 20-pin or 24-pin DIP
- 28 Pin Molded Chip Carrier Package

Key Specifications

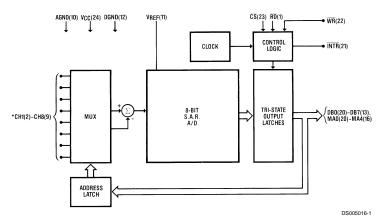
■ Resolution 8 Bits

■ Total Unadjusted Error ±½ LSB and ± 1 LSB
■ Single Supply 5 V_{DC}

■ Single Supply 5 V_{DC}
■ Low Power 15 mW

■ Conversion Time 40 µs

Block and Connection Diagrams

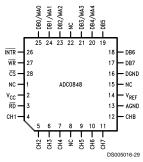


*ADC0848 shown in DIP Package CH5-CH8 not included on the ADC0844

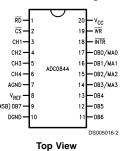
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Block and Connection Diagrams (Continued)

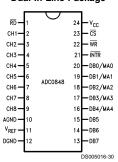
Molded Chip Carrier Package



Dual-In-Line Package



Dual-In-Line Package



Top View

Top View See Ordering Information

Ordering Information

Temperature	Total Unad	usted Error	MUX	Package
Range	±½ LSB	±1 LSB	Channels	Outline
		ADC0844CCN	4	N20A
0°C to +70°C				Molded Dip
	ADC0848BCN		8	N24C
		ADC0848CCN		Molded Dip
	ADC0844BCJ		4	J20A
-40°C to +85°C		ADC0844CCJ		Cerdip
-40 C to +65 C	ADC0848BCV		8	V28A
		ADC0848CCV		Molded Chip Carrier

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) 6.5V

Voltage

-0.3V to +15V Logic Control Inputs At Other Inputs and Outputs -0.3V to $\ensuremath{\text{V}_{\text{CC}}\text{+}0.3\text{V}}$ Input Current at Any Pin (Note 3) 5 mA Package Input Current (Note 3) 20 mA

Storage Temperature -65°C to +150°C Package Dissipation at T_A=25°C 875 mW

ESD Susceptibility (Note 4) 800V **Operating Conditions** (Notes 1, 2)

4.5 V_{DC} to 6.0 V_{DC} Supply Voltage (V_{CC}) Temperature Range $T_{MIN} \le T_A \le T_{MAX}$ 0°C≤T_A≤70°C

260°C

300°C

215°C

220°C

ADC0844CCN, ADC0848BCN, ADC0848CCN

Dual-In-Line Package (Plastic)

Molded Chip Carrier Package

Vapor Phase (60 seconds)

Infrared (15 seconds)

Dual-In-Line Package (Ceramic)

Lead Temperature (Soldering, 10 seconds)

ADC0844BCJ, ADC0844CCJ, -40°C≤T_A≤85°C

ADC0848BCV, ADC0848CCV

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits T_A = T_j = 25°C.

			ADC0844BCJ ADC0844CCJ			ADC0844CC 348BCN, ADC0 348BCV, ADC0	0848CCN	- Limit Units
Parameter	Conditions	Тур	Tested	Design	Тур	Tested	Design	
		(Note 5)	Limit	Limit	(Note 5)	Limit	Limit	
			(Note 6)	(Note 7)		(Note 6)	(Note 7)	
CONVERTER AND MULTIPLEXER CHA	ARACTERISTICS							
Maximum Total	V _{REF} =5.00 V _{DC}							
Unadjusted Error	(Note 8)							
ADC0844BCN, ADC0848BCN, BCV						±1/2	±1/2	LSB
ADC0844CCN, ADC0848CCN, CCV						±1	±1	LSB
ADC0844CCJ			±1					LSB
Minimum Reference		2.4	1.1		2.4	1.2	1.1	kΩ
Input Resistance								
Maximum Reference		2.4	5.9		2.4	5.4	5.9	kΩ
Input Resistance								
Maximum Common-Mode	(Note 9)		V _{CC} +0.05			V _{CC} +0.05	V _{CC} +0.05	V
Input Voltage								
Minimum Common-Mode	(Note 9)		GND-0.05			GND-0.05	GND-0.05	V
Input Voltage								
DC Common-Mode Error	Differential Mode	±1/16	±1/4		±1/16	±1/4	±1/4	LSB
Power Supply Sensitivity	V _{CC} =5V±5%	±1/16	±1/8		±1/16	±1/8	±1/8	LSB
Off Channel Leakage	(Note 10)							
Current	On Channel=5V,		-1			-0.1	-1	μA
	Off Channel=0V							
	On Channel=0V,		1			0.1	1	μA
	Off Channel=5V							
DIGITAL AND DC CHARACTERISTICS								
V _{IN(1)} , Logical "1" Input	V _{CC} =5.25V		2.0			2.0	2.0	V
Voltage (Min)								
V _{IN(0)} , Logical "0" Input	V _{CC} =4.75V		0.8			0.8	0.8	V
Voltage (Max)								
I _{IN(1)} , Logical "1" Input	V _{IN} =5.0V	0.005	1		0.005		1	μA
Current (Max)								
I _{IN(0)} , Logical "0" Input Current (Max)	V _{IN} =0V	-0.005	-1		-0.005		-1	μA
V _{OUT(1)} , Logical "1"	V _{CC} =4.75V							
Output Voltage (Min)	I _{OUT} =-360 μA		2.4			2.8	2.4	V
	I _{OUT} =-10 μA		4.5			4.6	4.5	V

The following specifications apply for V_{CC} = 5 V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A = T_j = 25^{\circ}C$.

			ADC0844BCJ ADC0844CCJ		ADC08	Limit			
Parameter	Conditions	Тур	Tested	Design	Тур	Tested	Design	Units	
		(Note 5)	Limit	Limit	(Note 5)	Limit	Limit		
			(Note 6)	(Note 7)		(Note 6)	(Note 7)		
DIGITAL AND DC CHARACTERISTICS									
V _{OUT(0)} , Logical "0"	V _{CC} =4.75V		0.4			0.34	0.4	V	
Output Voltage (Max)	I _{OUT} =1.6 mA								
I _{OUT} , TRI-STATE Output	V _{OUT} =0V	-0.01	-3		-0.01	-0.3	-3	μA	
Current (Max)	V _{OUT} =5V	0.01	3		0.01	0.3	3	μA	
I _{SOURCE} , Output Source	V _{OUT} =0V	-14	-6.5		-14	-7.5	-6.5	mA	
Current (Min)									
I _{SINK} , Output Sink	V _{OUT} =V _{CC}	16	8.0		16	9.0	8.0	mA	
Current (Min)									
I _{CC} , Supply Current (Max)	CS =1, V _{REF} Open	1	2.5		1	2.3	2.5	mA	

AC Electrical Characteristics

The following specifications apply for $V_{CC} = 5V_{DC}$, $t_r = t_f = 10$ ns unless otherwise specified. **Boldface limits apply from T_{MIN}** to T_{MAX}; all other limits T_A = T_j = 25°C.

			Tested	Design	
Parameter	Conditions	Тур	Limit	Limit	Units
		(Note 5)	(Note 6)	(Note 7)	
t _C , Maximum Conversion Time (See Graph)		30	40	60	μs
t _{W(WR)} , Minimum WR Pulse Width	(Note 11)	50	150		ns
t _{ACC} , Maximum Access Time (Delay from Falling Edge of	C _L = 100 pF	145		225	ns
RD to Output Data Valid)	(Note 11)				
t _{1H} , t _{0H} , TRI-STATE Control (Maximum Delay from Rising	$C_L = 10 \text{ pF}, R_L = 10 \text{k}$	125		200	ns
Edge of RD to Hi-Z State)	(Note 11)				
t_{WI} , t_{RI} , Maximum Delay from Falling Edge of \overline{WR} or \overline{RD} to	(Note 11)	200	400		ns
Reset of INTR					
t _{DS} , Minimum Data Set-Up Time	(Note 11)	50	100		ns
t _{DH} , Minimum Data Hold Time	(Note 11)	0	50		ns
C _{IN} , Capacitance of Logic Inputs		5			pF
C _{OUT} , Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground pins.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails $(V_{IN} < V^- or V_{IN} > V^+)$ the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Design limits are guaranteed by not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 8: Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.

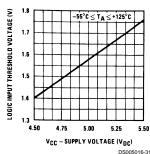
Note 9: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 10: Off channel leakage current is measured after the channel selection.

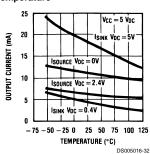
Note 11: The temperature coefficient is 0.3%/°C.

Typical Performance Characteristics

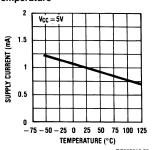
Logic Input Threshold Voltage vs Supply Voltage



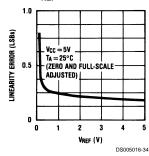
Output Current vs Temperature



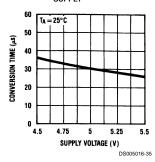
Power Supply Current vs Temperature



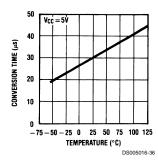
Linearity Error vs V_{REF}



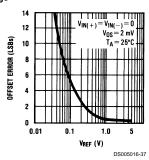
Conversion Time vs V_{SUPPLY}



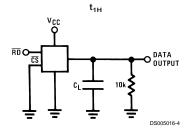
Conversion Time vs Temperature

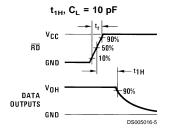


Unadjusted Offset Error vs V_{REF} Voltage



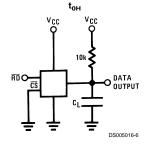
TRI-STATE Test Circuits and Waveforms

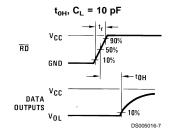




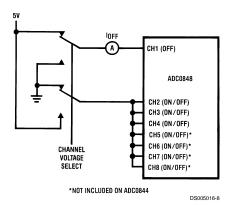
t_r = 20 ns

t_r = 20 ns



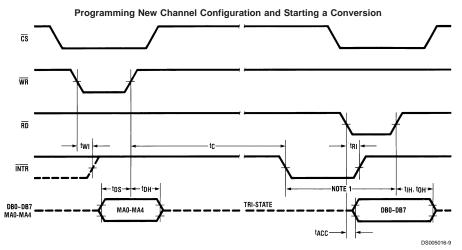


Leakage Current Test Circuit



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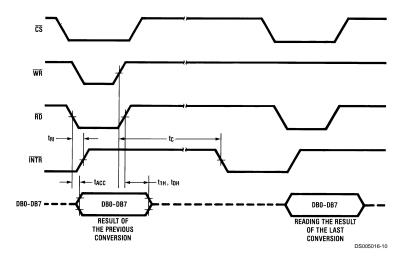
Timing Diagrams

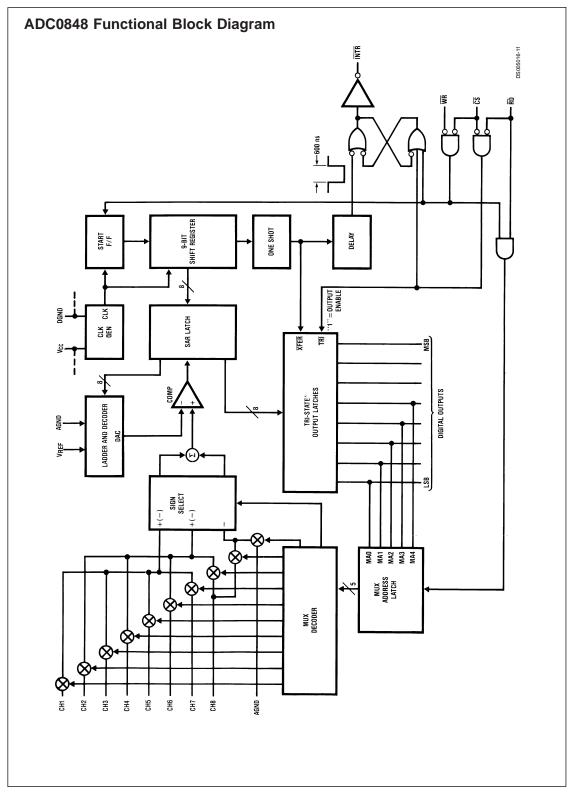


 $\textbf{Note 12:} \ \ \text{Read strobe must occur at least 600 ns after the assertion of interrupt to guarantee reset of } \overline{\text{INTR}} \ .$

Note 13: MA stands for MUX address.

Using the Previously Selected Channel Configuration and Starting a Conversion





Functional Description

The ADC0844 and ADC0848 contain a 4-channel and 8-channel analog input multiplexer (MUX) respectively. Each MUX can be configured into one of three modes of operation differential, pseudo-differential, and single ended. These modes are discussed in the Applications Information Section. The specific mode is selected by loading the MUX address latch with the proper address (see Table 1 and Table 2). Inputs to the MUX address latch (MA0-MA4) are common with data bus lines (DB0-DB4) and are enabled when the RD line is high. A conversion is initiated via the $\overline{\text{CS}}$ and $\overline{\text{WR}}$ lines. If the data from a previous conversion is not read, the INTR line will be low. The falling edge of $\overline{\rm WR}$ will reset the $\overline{\rm INTR}$ line high and ready the A/D for a conversion cycle. The rising edge of WR, with RD high, strobes the data on the MAO/ DB0-MA4/DB4 inputs into the MUX address latch to select a new input configuration and start a conversion. If the RD line is held low during the entire low period of $\overline{\mbox{WR}}$ the previous MUX configuration is retained, and the data of the previous conversion is the output on lines DB0-DB7. After the conversion cycle ($t_C \le 40 \,\mu s$), which is set by the internal clock frequency, the digital data is transferred to the output latch and the INTR is asserted low. Taking CS and RD low resets INTR output high and outputs the conversion result on the data lines (DB0-DB7).

Applications Information

1.0 MULTIPLEXER CONFIGURATION

The design of these converters utilizes a sampled-data comparator structure which allows a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "-" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "-" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single ended, or pseudo-differential. Figure 1 shows the three modes using the 4-channel MUX ADC0844. The eight inputs of the ADC0848 can also be configured in any of the three modes. In the differential mode, the ADC0844 channel inputs are grouped in pairs, CH1 with CH2 and CH3 with CH4. The polarity assignment of each channel in the pair is interchangeable. The single-ended mode has CH1-CH4 assigned as the positive input with the negative input being the analog ground (AGND) of the device. Finally, in the pseudo-differential mode CH1-CH3 are positive inputs referenced to CH4 which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

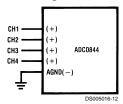
The analog input voltages for each channel can range from 50 mV below ground to 50 mV above $V_{\rm CC}$ (typically 5V) without degrading conversion accuracy.

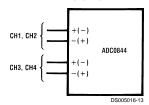
TABLE 1. ADC0844 MUX ADDRESSING

	MUX A	ddress		cs	WR	RD		Channel#				MUX
MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	AGND	Mode
X	L	L	L	L		Н	+	-				
X	L	L	Н	L	7_F	Н	_	+				Differential
X	L	Н	L	L		Н			+	-		
X	L	Н	Н	L		Н			-	+		
L	Н	L	L	L		Н	+				-	
L	Н	L	Н	L	ᄺ	Н		+			-	Single-Ended
L	Н	Н	L	L		Н			+		-	
L	Н	Н	Н	L		Н				+	-	
Н	Н	L	L	L		Н	+			-		Pseudo-
Н	Н	L	Н	L	ᄺ	Н		+		-		Differential
Н	Н	Н	L	L		Н			+	-		
X	Х	Х	Х	L	7_F	L	Previous Channel Configuration					

X=don't care

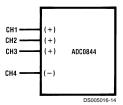
4 Single-Ended





2 Differential

3 Pseudo-Differential



Combined

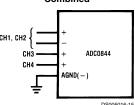


FIGURE 1. Analog Input Multiplexer Options

2.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input of these converters defines the voltage span of the analog input (the difference between $V_{\mathsf{IN}(\mathsf{MAX})}$ and $V_{\mathsf{IN}(\mathsf{MIN})}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the minimum reference input resistance of 1.1 k Ω . This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 2a*), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the $V_{\rm REF}$ pin can be tied to $V_{\rm CC}$. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (Figure 2b), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the $V_{\rm CC}$ supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{\rm REF}/256$).

most typical). The time interval between sampling the "+" input and then the "-" inputs is ½ of a clock period. The change in the common-mode voltage during this short time

put and then the — Inputs is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{\text{ERROR}(\text{MAX})} = V_{\text{peak}} (2\pi f_{\text{CM}}) \times 0.5 \times \left(\frac{t_{\text{C}}}{8}\right)$$

where f_{CM} is the frequency of the common-mode signal, V_{peak} is its peak voltage value and t_C is the conversion time. For a 60 Hz common-mode signal to generate a ½ LSB error (=5 mV) with the converter running at 40 µS, its peak value would have to be 5.43V. This large a common-mode signal is much greater than that generally found in a well designed data acquisition system.

3.0 THE ANALOG INPUTS

3.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "-" inputs for a conversion (60 Hz is

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TABLE 2. ADC0848 MUX Addressing

	MU	X Addı	ress		CS	WR	RD					Chann	el				MUX
MA4	MA3	MA2	MA1	MA0				CH1	CH2	СНЗ	CH4	CH5	CH6	CH7	CH8	AGND	Mode
X	L	L	L	L	L		Н	+	-								
Χ	L	L	L	Н	L		Н	_	+								
Χ	L	L	Н	L	L		Н			+	-						
Χ	L	L	Н	Н	L	¬_r	Н			-	+						Differential
Χ	L	Н	L	L	L		Н					+	-				
Χ	L	Н	L	Н	L		Н					_	+				
Χ	L	Н	Н	L	L		Н							+	-		
Х	L	Н	Н	Н	L		Н							_	+		
L	Н	L	L	L	L		Н	+								-	
L	Н	L	L	Н	L		Н		+							-	
L	Н	L	Н	L	L		Н			+						-	
L	Н	L	Н	Н	L	ᄺ	Н				+					-	Single-Ended
L	Н	Н	L	L	L		Н					+				-	
L	Н	Н	L	Н	L		Н						+			_	
L	Н	Н	Н	L	L		Н							+		-	
L	Н	Н	Н	Н	L		Н								+	-	
Н	Н	L	L	L	L		Н	+							-		
Н	Н	L	L	Н	L		Н		+						-		
Н	Н	L	Н	L	L		Н			+					-		Pseudo-
Н	Н	L	Н	Н	L	7_F	Н				+				-		Differential
Н	Н	Н	L	L	L		Н					+			-		
Н	Н	Н	L	Н	L		Н						+		-		
Н	Н	Н	Н	L	L		Н							+	_		
X	Х	Х	Х	Х	L	7LF	L			Prev	ious Cl	nannel	Config	uration			

3.2 Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "–" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 $k\Omega$.

3.3 Input Source Resistance

The limitation of the input source resistance due to the DC leakage currents of the input multiplexer is important. A worst-case leakage current of \pm 1 μA over temperature will create a 1 mV input error with a 1 k Ω source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

4.0 OPTIONAL ADJUSTMENTS

4.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{\text{IN(MIN)}}$, is not ground, a zero offset can be done. The converter can be made to out-

put 0000 0000 digital code for this minimum input voltage by biasing any $V_{\rm IN}$ (–) input at this $V_{\rm IN(MIN)}$ value. This is useful for either differential or pseudo-differential modes of input channel configuration.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V $^-$ input and applying a small magnitude positive voltage to the V $^+$ input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0001 and the ideal ½ LSB value (½ LSB=9.8 mV for V_{REF} =5.000 V_{DC}).

4.2 Full-Scale

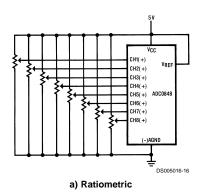
The full-scale adjustment can be made by applying a differential input voltage which is 1 $\frac{1}{2}$ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code changing from 1111 1110 to 1111 11111.

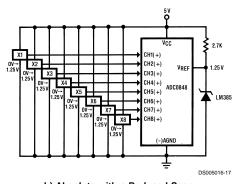
4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A $\rm V_{IN}$ (+) voltage which equals this desired zero reference plus ½ LSB (where the

LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero

reference voltage at the corresponding "–" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.





b) Absolute with a Reduced Span

FIGURE 2. Referencing Examples

The full-scale adjustment should be made [with the proper $V_{\rm IN}$ (–) voltage applied] by forcing a voltage to the $V_{\rm IN}$ (+) input which is given by:

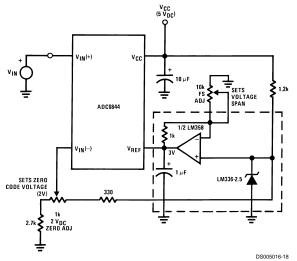
$$V_{IN}$$
 (+) fs adj = $V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{256} \right]$

where V_{MAX} =the high end of the analog input range and V_{MIN} =the low end (the offset zero) of the analog range. (Both are ground referenced.)

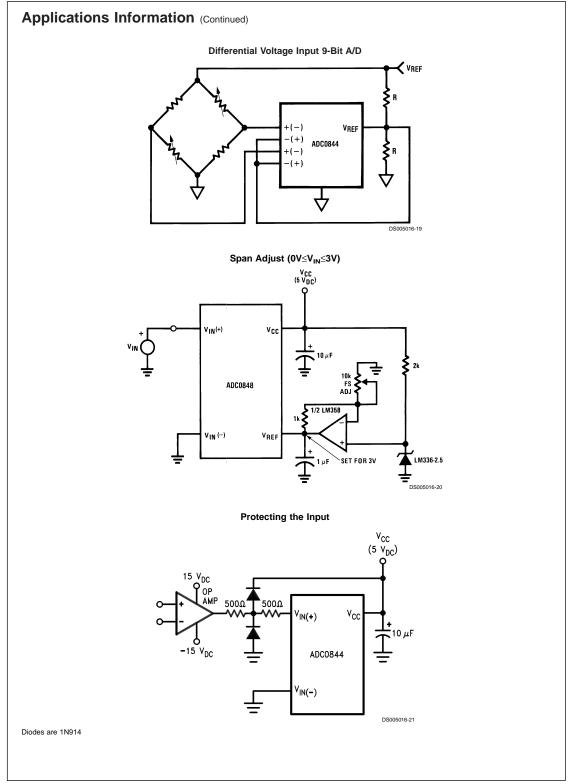
The V_{REF} (or $V_{CC})$ voltage is then adjusted to provide a code change from FE $_{HEX}$ to FF $_{HEX}$. This completes the adjustment procedure.

For an example see the Zero-Shift and Span Adjust circuit below.

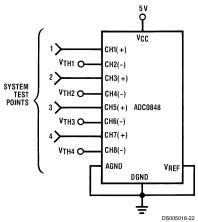
Zero-Shift and Span Adjust (2 $V \le V_{IN} \le 5V$)



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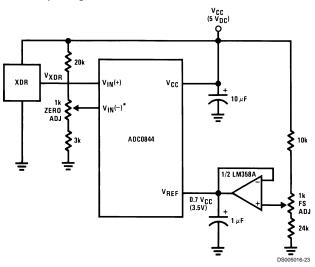


High Accuracy Comparators

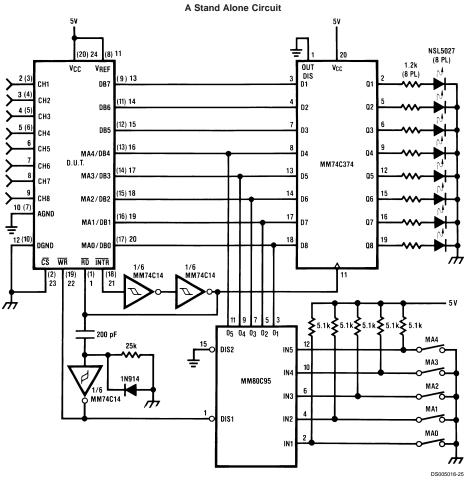


DO=all 1s if $V_{IN}(+)>V_{IN}(-)$ DO=all 0s if $V_{IN}(+)< V_{IN}(-)$

Operating with Automotive Ratiometric Transducers

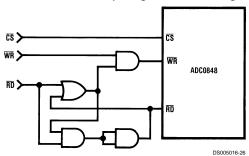


*V_{IN}(-)=0.15 V_{CC} 15% of V_{CC} \leq V_{XDR} \leq 85% of V_{CC}



Note: DUT pin numbers in parentheses are for ADC0844, others are for ADC0848.

Start a Conversion without Updating the Channel Configuration



 \overline{\text{CS} •\width{\text{WR}}} will update the channel configuration and start a conversion.

 \overline{\text{CS} •\text{RD}} will read the conversion data and start a new conversion without updating the channel configuration.

 Waiting for the end of this conversion is not necessary. A \overline{\text{CS} •\width{\text{WR}} \overline{\text{can immediately follow the } \overline{\text{CS} •\text{RD}} .

Applications Information (Continued) ADC0844 — INS8039 Interface DB0 DBO/MAO $\mathbf{V}_{\mathsf{REF}}$ 16 (+)CH1 DB1 DB1/MA1 (—)CH2 15 DB2 DB2/MA2 14 DB3 DB3/MA3 13 DB4 DB4 12 ADC0844 DB5 DB5

11 DB6

9

18

DB7 19

WR

 \overline{RD} $\overline{\mathtt{CS}}$

SAMPLE PROGRAM FOR ADC0844—INS8039 INTERFACE CONVERTING TWO RATIOMETRIC, DIFFERENTIAL SIGNALS

18

27

DB6

DB7

WR

 $\overline{\text{RD}}$

PI1

INS8039

0000 04 10 JMP BEGIN :START PROGRAM AT ADD	R 10
1111 1 22011 ,011111110011111111102	
ORG 10H ;MAIN PROGRAM	
0010 B9 FF BEGIN: MOV R1,#0FFH ;LOAD R1 WITH A UNUSED	ADDR
;LOCATION	
0012 B8 20 MOV R0,#20H ;A/D DATA ADDRESS	
0014 89 FF ORL P1,#0FFH ;SET PORT 1 OUTPUTS HIG	H
0016 23 00 MOV A,00H ;LOAD THE ACC WITH A/D I	MUX DATA
;CH1 AND CH2 DIFFERENT	IAL
0018 14 50 CALL CONV ;CALL THE CONVERSION S	UBROUTINE
001A 23 02 MOV A,#02H ;LOAD THE ACC WITH A/D	MUX DATA
;CH3 AND CH4 DIFFERENT	IAL
001C 18 INC RO ;INCREMENT THE A/D DATA	A ADDRESS
001D 14 50 CALL CONV ;CALL THE CONVERSION S	UBROUTINE

(+)CH3

(-)CH4 AGND

DS005016-27

;CONTINUE MAIN PROGRAM

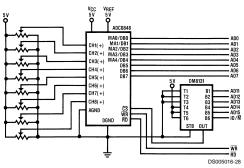
;CONVERSION SUBROUTINE ;ENTRY:ACC — A/D MUX DATA ;EXIT: ACC — CONVERTED DATA

			ORG	50H	
0050	99 FE	CONV:	ANL	P1,#0FEH	;CHIP SELECT THE A/D
0052	91		MOVX	@R1,A	;LOAD A/D MUX & START CONVERSION
0053	09	LOOP:	IN	A.P1	:INPUT INTR STATE

SAMPLE PROGRAM FOR ADC0844—INS8039 INTERFACE CONVERTING TWO RATIOMETRIC, DIFFERENTIAL SIGNALS (Continued)

0054	32 53	JB1	LOOP	;IF INTR = 1 GOTO LOOP
0056	81	MOVX	A,@R1	;IF INTR = 0 INPUT A/D DATA
0057	89 01	ORL	P1,&01H	;CLEAR THE A/D CHIP SELECT
0059	A0	MOV	@R0,A	;STORE THE A/D DATA
005A	83	RET		;RETURN TO MAIN PROGRAM

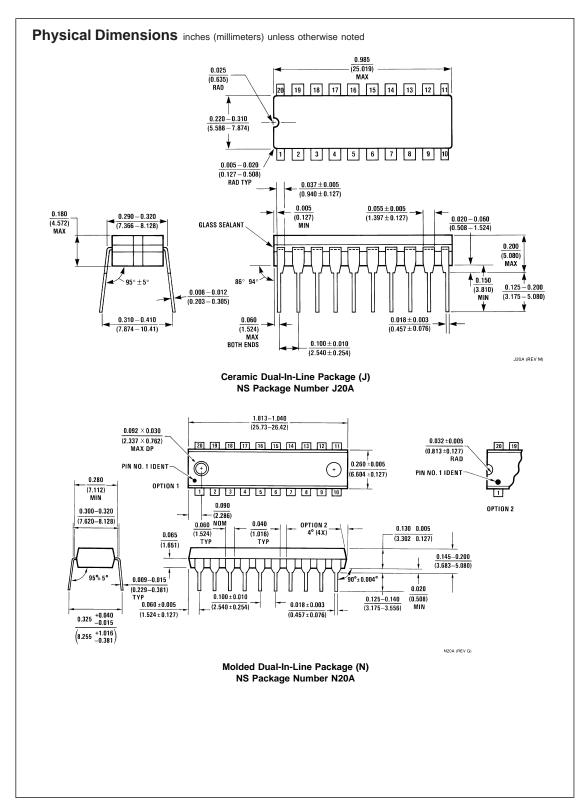
I/O Interface to NSC800

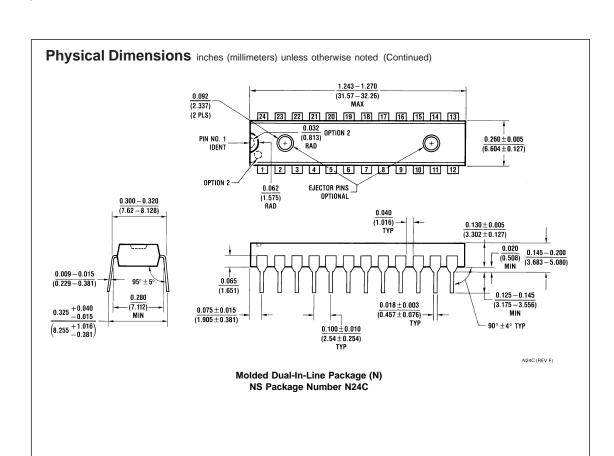


SAMPLE PROGRAM FOR ADC0848 — NSC800 INTERFACE

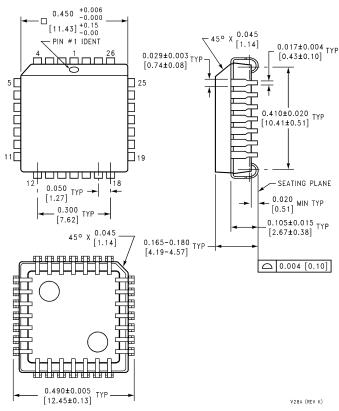
	NCONV	EQU	16	
	DEL	EQU	15	;DELAY 50 µsec CONVERSION
	CS	EQU	1FH	;THE BOARD ADDRESS
	ADDTA	EQU	003CH	;START OF RAM FOR A/D
				;DATA
08 09 0A 0B	MUXDTA:	DB	08H,09H,0AH,0BH	;MUX DATA
0C 0D 0E 0F		DB	0CH,0DH,0EH,0FH	
0E 1F	START:	LD	C,CS	
06 16		LD	B,NCONV	
21 0000'		LD	HL,MUXDTA	
11 003C		LD	DE,ADDTA	
ED A3	STCONV:	OUTI		;LOAD A/D'S MUX DATA
				;AND START A CONVERSION
EB		EX	DE,HL	;HL=RAM ADDRESS FOR THE
				;A/D DATA
3E 0F		LD	A,DEL	
3D	WAIT:	DEC	Α	;WAIT 50 µsec FOR THE
C2 0013'		JP	NZ,WAIT	;CONVERSION TO FINISH
ED A2		INI		;STORE THE A/D'S DATA
				;CONVERTED ALL INPUTS?
EB		EX	DE,HL	
C2 000E'		JP	NZ,STCONV	;IF NOT GOTO STCONV
		END		
	OC OD OE OF OE 1F O6 16 21 0000' 11 003C ED A3 EB 3E OF 3D C2 0013' ED A2 EB	DEL CS ADDTA 08 09 0A 0B MUXDTA: 0C 0D 0E 0F 0E 1F 06 16 21 0000' 11 003C ED A3 STCONV: EB 3E 0F 3D WAIT: C2 0013' ED A2 EB	DEL EQU CS EQU ADDTA EQU 08 09 0A 0B MUXDTA: DB 0C 0D 0E 0F DB 0E 1F START: LD 06 16 LD 21 0000' LD 11 003C LD ED A3 STCONV: OUTI EB EX 3E 0F 3D WAIT: DEC C2 0013' JP ED A2 INI EB C2 000E' JP	DEL CS EQU 1FH ADDTA EQU 003CH 08 09 0A 0B MUXDTA: DB 08H,09H,0AH,0BH 0C 0D 0E 0F DB 0CH,0DH,0EH,0FH 0E 1F START: LD C,CS 06 16 LD B,NCONV 21 0000' LD HL,MUXDTA 11 003C LD DE,ADDTA ED A3 STCONV: OUTI EB EX DE,HL 3E 0F JP NZ,WAIT ED A2 INI EB C2 000E' JP NZ,STCONV

Note 14: This routine sequentially programs the MUX data latch in the signal-ended mode. For CH1-CH8 a conversion is started, then a 50 µs wait for the A/D to complete a conversion and the data is stored at address ADDTA for CH1, ADDTA + 1 for CH2, etc.





Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Chip Carrier Package (V) NS Package Number V28A

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