CDA 4930 002
Digital Circuit Synthesis
Summer 2014
Instructor: Dr. Srinivas Katkoori
Programming Assignment 2 Report
VHDL Behavioral Modeling

Today's Date:	06/11/14
Your Name:	Mark Little
Your U Number:	84134627
No. of Hours Spent:	20
Exercise Difficulty: (Easy, Average, Hard)	Hard
Any Other Feedback:	

Question 1:

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    18:26:35 06/11/2014
-- Design Name:
-- Module Name:    alu - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity alu is
port(ain : in bit;
            bin : in bit;
            cin_add : in bit;
            cin_sub : in bit;
            sel : in bit_vector(1 downto 0);
            cout_add : out bit;
            cout_sub : out bit;
            aout : out bit
                  );
end alu;

architecture Behavioral of alu is
```

```
begin

process(sel, ain, bin, cin_add, cin_sub)
begin
	case sel is
	when "00" =>
	aout <= ain xor bin xor cin_add;--adding two integers
	cout_add <= ((bin and cin_add) or (ain and cin_add) or (ain and bin));
	when "01" =>
	aout <= ain xor bin xor cin_sub;--subtracting two integers
	cout_sub <= (((not ain) and bin) or ((not ain) and cin_sub) or (bin and cin_sub));
	when "10" =>
	aout <=  ain and bin;--two inputs anded together
	when "11" =>
	aout <= not ain;--inverting input a
	when others =>
	aout <= '0';
	end case;
end process;


end Behavioral;



----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    18:49:07 06/11/2014
-- Design Name:
-- Module Name:    alu8 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity alu8 is

port(ain : in bit_vector(7 downto 0);
          bin : in bit_vector (7 downto 0);
          sel : in bit_vector (1 downto 0);
          aout : out bit_vector (7 downto 0)
          );

end alu8;

architecture struct of alu8 is

signal c0 : bit := '0';
signal carout_add, carout_sub, c1, c2, c3, c4, c5, c6, c7, c8, c9,
c10, c11, c12, c13, c14 : bit;

begin

bit0 : entity work.alu(Behavioral)
        port map (ain(0), bin(0), c0, c0, sel, carout_add,
        carout_sub, aout(0));

bit1 : entity work.alu(Behavioral)
        port map (ain(1), bin(1),carout_add,
        carout_sub, sel, c1, c2, aout(1));

bit2 : entity work.alu(Behavioral)
        port map (ain(2), bin(2), c1, c2, sel, c3, c4, aout(2));

bit3 : entity work.alu(Behavioral)
        port map (ain(3), bin(3), c3, c4, sel, c5, c6, aout(3));

bit4 : entity work.alu(Behavioral)
        port map (ain(4), bin(4), c5, c6, sel, c7, c8, aout(4));
```

```
bit5 : entity work.alu(Behavioral)
        port map (ain(5), bin(5), c7, c8, sel, c9, c10, aout(5));

bit6 : entity work.alu(Behavioral)
        port map (ain(6), bin(6), c9, c10, sel, c11, c12, aout(6));

bit7 : entity work.alu(Behavioral)
        port map (ain(7), bin(7), c11, c12, sel, c13, c14, aout(7));


end architecture struct;
```

Question 1: VHDL Testbench

Where possible test the model exhaustively. If this is not possible, then test with at least 8 different input vectors.

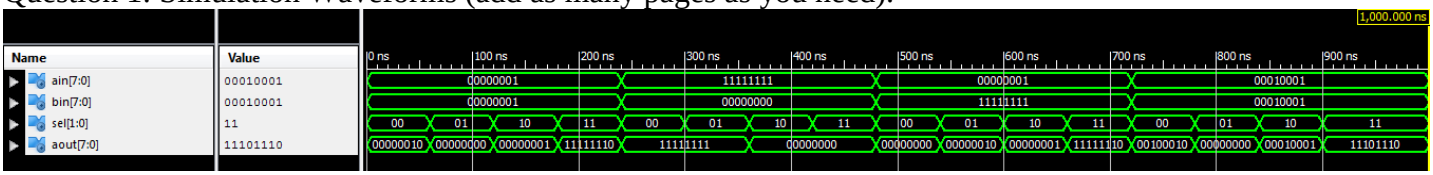
```
--------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:   19:28:08 06/11/2014
-- Design Name:
-- Module Name:   E:/Desktop/School Docs/5/SummerC/CIS 4930-002 Digital Circuit
Synthesis/ass2/redo/alu8_tb.vhd
-- Project Name:  redo
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: alu8
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test.  Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--------------------------------------------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY alu8_tb IS
END alu8_tb;

ARCHITECTURE behavior OF alu8_tb IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT alu8
```

```
    PORT(
         ain : IN  bit_vector(7 downto 0);
         bin : IN  bit_vector(7 downto 0);
         sel : IN  bit_vector(1 downto 0);
         aout : OUT  bit_vector(7 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal ain : bit_vector(7 downto 0) := (others => '0');
   signal bin : bit_vector(7 downto 0) := (others => '0');
   signal sel : bit_vector(1 downto 0) := (others => '0');

          --Outputs
   signal aout : bit_vector(7 downto 0);
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

--   constant <clock>_period : time := 10 ns;

BEGIN

          -- Instantiate the Unit Under Test (UUT)
   uut: alu8 PORT MAP (
          ain => ain,
          bin => bin,
          sel => sel,
          aout => aout
        );

--   -- Clock process definitions
--   <clock>_process :process
--   begin
--                   <clock> <= '0';
--                   wait for <clock>_period/2;
--                   <clock> <= '1';
--                   wait for <clock>_period/2;
--   end process;


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      --wait for 100 ns;
```

```
--      wait for <clock>_period*10;

      -- insert stimulus here
                  --test1

                  ain <= "00000001";
                  bin <= "00000001";

                  sel <= "00";

                  wait for 60 ns;
                  sel <= "01";

                  wait for 60 ns;
                  sel <= "10";

                  wait for 60 ns;
                  sel <= "11";

                  --test2
                  wait for 60 ns;

                  ain <= "11111111";
                  bin <= "00000000";

                  sel <= "00";

                  wait for 60 ns;
                  sel <= "01";

                  wait for 60 ns;
                  sel <= "10";

                  wait for 60 ns;
                  sel <= "11";

                  --test3
                  wait for 60 ns;

                  ain <= "00000001";
                  bin <= "11111111";

                  sel <= "00";

                  wait for 60 ns;
                  sel <= "01";
```

```
        wait for 60 ns;
        sel <= "10";

        wait for 60 ns;
        sel <= "11";

        --test4
        wait for 60 ns;

        ain <= "00010001";
        bin <= "00010001";

        sel <= "00";

        wait for 60 ns;
        sel <= "01";

        wait for 60 ns;
        sel <= "10";

        wait for 60 ns;
        sel <= "11";

    wait;
  end process;

END;
```

Question 1: Simulation Waveforms (add as many pages as you need).



Question 2:

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    20:04:23 06/11/2014
-- Design Name:
-- Module Name:    flipflop - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity flipflop is
port (Clk : in std_logic;
                d : in std_logic;
                d_out : out std_logic
                );
end flipflop;

architecture struct of flipflop is

begin

process(Clk)
        begin
```

```
                if(rising_edge (Clk))then
                d_out <= d;
                end if;
end process;

end struct;

----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    20:10:54 06/11/2014
-- Design Name:
-- Module Name:    nbit_reg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity nbit_reg is
generic (n : integer);
port (Clk : in std_logic;
                d_out : out std_logic_vector (0 to n-1);
                ind : in std_logic
                );
end nbit_reg;
```

```
architecture gen of nbit_reg is

component flipflop
        port (Clk : in std_logic;
                        d : in std_logic;
                        d_out : out std_logic
                        );
end component flipflop;

signal wire1 : std_logic_vector(0 to n-1);

begin
        flipflopa : for i in 0 to n-1 generate
                wire1(i) <= ind;

                        flipflopb : flipflop port map (Clk, wire1(i), d_out(i));
                        end generate;

end gen;
```

Question 2: VHDL Testbench

Where possible test the model exhaustively. If this is not possible, then test with at least 8 different input vectors.

```
--------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:   20:43:10 06/11/2014
-- Design Name:
-- Module Name:   E:/Desktop/School Docs/5/SummerC/CIS 4930-002 Digital Circuit
Synthesis/ass2/redo/nbit_reg_tb.vhd
-- Project Name:  redo
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: nbit_reg
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test.  Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--------------------------------------------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY nbit_reg_tb IS
END nbit_reg_tb;

ARCHITECTURE behavior OF nbit_reg_tb IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT nbit_reg
```

```
        generic (n : integer := 8);
 PORT(
      Clk : IN  std_logic;
      d_out : OUT  std_logic_vector(0 to n-1);
      ind : IN  std_logic
     );
 END COMPONENT;


 --Inputs
 signal Clk : std_logic := '0';
 signal ind : std_logic := '0';

       --Outputs
 signal d_out : std_logic_vector(0 to 7);

 -- Clock period definitions
 constant Clk_period : time := 10 ns;

BEGIN

       -- Instantiate the Unit Under Test (UUT)
 uut: nbit_reg PORT MAP (
      Clk => Clk,
      d_out => d_out,
      ind => ind
     );

 -- Clock process definitions
 Clk_process :process
 begin
                Clk <= '0';
                wait for Clk_period/2;
                Clk <= '1';
                wait for Clk_period/2;
 end process;


 -- Stimulus process
 stim_proc: process
 begin
   -- hold reset state for 100 ns.
   wait for 100 ns;

   wait for Clk_period*10;

   -- insert stimulus here
```

```
                ind <= '1';
                wait for 10 ns;
                ind <= '0';
                wait for 10 ns;
                ind <= '1';
                wait for 10 ns;
                ind <= '0';
                wait for 10 ns;
                ind <= '1';
                wait for 10 ns;
                ind <= '0';
                wait for 10 ns;
                ind <= '1';

    wait;
  end process;

END;
```

Question 2: Simulation Waveforms (add as many pages as you need).