THE AMERICAN
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الجـامـعة الأمـريكيـة بالقـاهـرة

School of Sciences and Engineering
Department of Computer Science and Engineering
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CSCE 231: Computer Architecture

Project 01 Milestone 02: RISC-V FPGA Implementation and Testing

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1. Implementation Description:

The project is to design and implement a pipelined RISC-V processor (femtoRV32) that supports the RV32I instruction set, with specific modifications, and to test it on our Nexys A7 FPGA board. The implementation will be fully tested using a custom set of test cases covering all supported instructions and pipeline hazard scenarios. The implementation will focus on achieving a balanced design that incorporates pipeline stages, hazard handling, and a single memory model for both instructions and data. The project will use a three-stage pipeline architecture with each stage carefully organized to address both structural and data hazards. The project will be developed in Verilog, with the processor architecture, control unit, and memory components integrated to support the 42 instructions. This Verilog implementation will undergo synthesis and timing analysis on the Nexys A7 FPGA later on.

2. Design Decisions and Assumptions:

1. RV32I Base Instruction Set Support

The core instruction set includes 42 user-level instructions as per the RISC-V Volume 1 Unprivileged Specification. Certain instructions are adjusted:

- ECALL: Implemented as a halting instruction, effectively ending program execution by freezing the Program Counter (PC).

- EBREAK, PAUSE, FENCE, FENCE.TSO: Treated as No-Operation (NOP) instructions and will not affect our program execution.

Instruction Categories:

- Arithmetic and Logical: ADD, SUB, XOR, OR, AND, and their variants with immediate operands

- Shift: SLL, SRL, and SRA

- Branch and Jump: BEQ, BNE, BLT, BGE, JAL, JALR

- Load/Store: LW, SW

- Miscellaneous Instructions: LUI, AUIPC

All instructions will be validated to ensure they behave according to the specification.

2. Pipeline Architecture

- Pipeline Structure: The design requires a 3-stage pipeline with each stage taking 2 clock cycles:

    - Stage 0 (IF/ID): Instruction Fetch on cycle C0, followed by Register Read (ID) on C1

    - Stage 1 (EX/MEM): Execution on cycle C0, followed by Memory Access on C1.

    - Stage 2 (WB): Write Back on cycle C0, with C1 being idle in this stage.

Verilog Modules

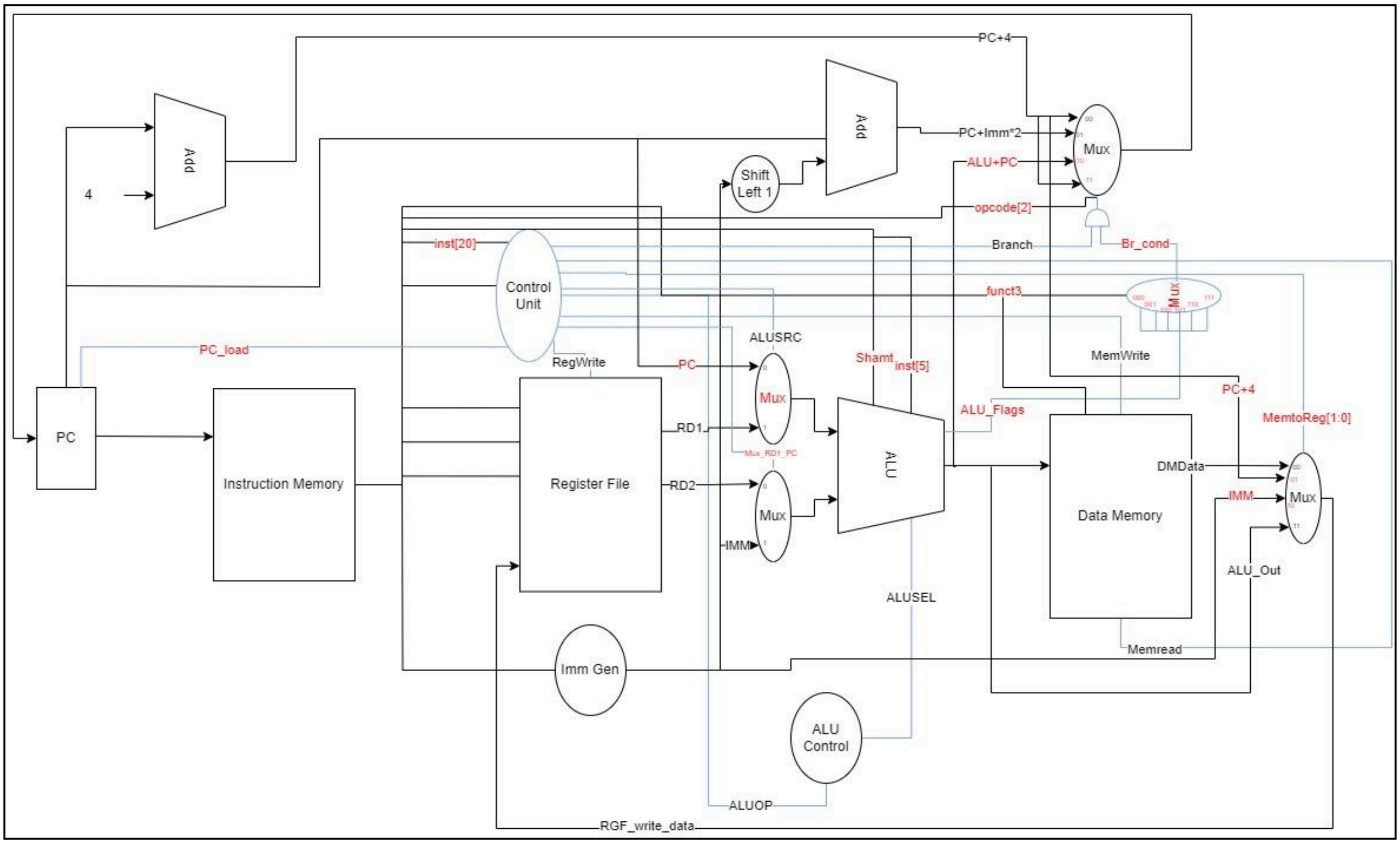
As for our modules developed using Verilog programming language, we have developed numerous modules to support our complete pipelined RISC-V processor.

Here is a list of the module names:

1. ALUCU
2. ALUCU_TB
3. CPU_TB
4. CU
5. DataMem
6. defines
7. DFlipFlop
8. DM_TB
9. Four_Digit_Seven_Segment_Driver_Optimized
10. Full_Adder
11. ImmGen
12. InstMem
13. mux_2x1
14. mux_4to1
15. mux_8to1
16. mux_8to1_TB
17. nbit_mux_2x1
18. Nbit_Regfile
19. nbit_shiftleft1
20. Nbit_ShiftRegister
21. prv32_ALU
22. RCA_8bit
23. Scy_CPU
24. Scy_CPU_TopModule
25. ScyCPU_TB
26. ScyTopmodule_const

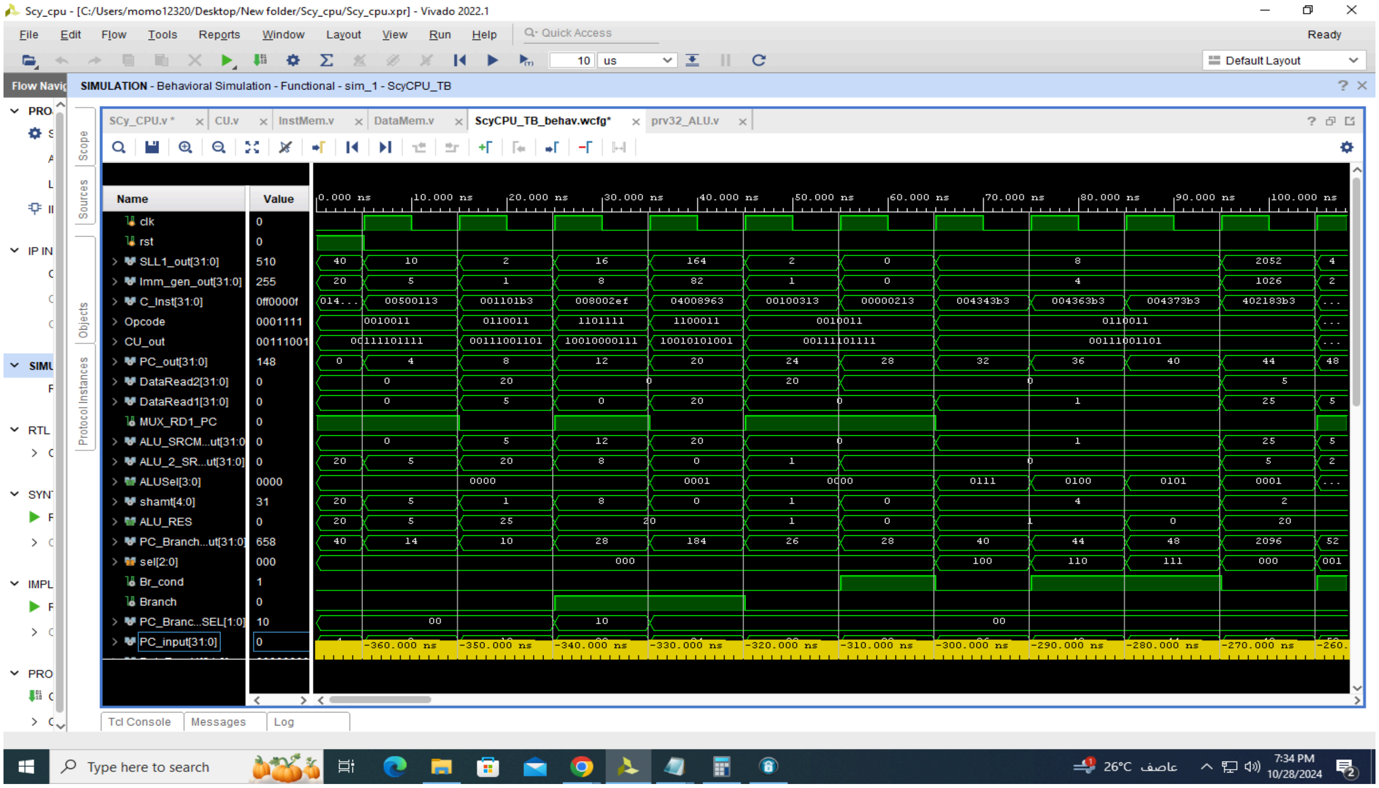
3. Data Flow

Here is our comprehensive block diagram of the single-cycle datapath that will be prepared to clarify data flow and control signals, with all wire, adders, and the other main components.



4. Simulation

To visualize our entire datapath, here are some screenshots of what our simulated datapath would look like taking into account all values of all components at every instance and every clock cycle.


Scy_cpu - [C:/Users/momo12320/Desktop/New folder/Scy_cpu/Scy_cpu.xpr] - Vivado 2022.1
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Ready
Default Layout
Flow Navig
SIMULATION - Behavioral Simulation - Functional - sim_1 - ScyCPU_TB
SCy_CPU.v * CU.v InstMem.v DataMem.v ScyCPU_TB_behav.wcfg* prv32_ALU.v
Scope Sources Objects Protocol Instances
0.000 ns 10.000 ns 20.000 ns 30.000 ns 40.000 ns 50.000 ns 60.000 ns 70.000 ns 80.000 ns 90.000 ns 100.000 ns
-360.000 ns -350.000 ns -340.000 ns -330.000 ns -320.000 ns -310.000 ns -300.000 ns -290.000 ns -280.000 ns -270.000 ns
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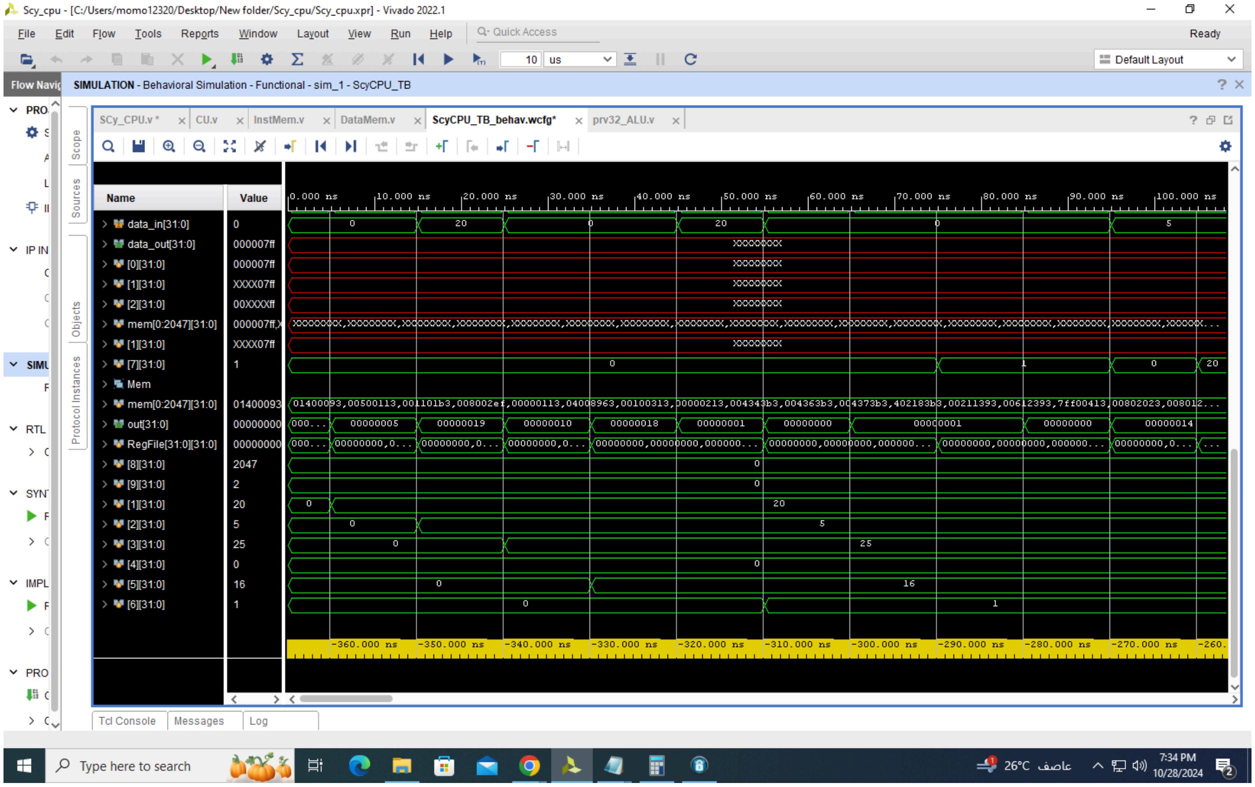
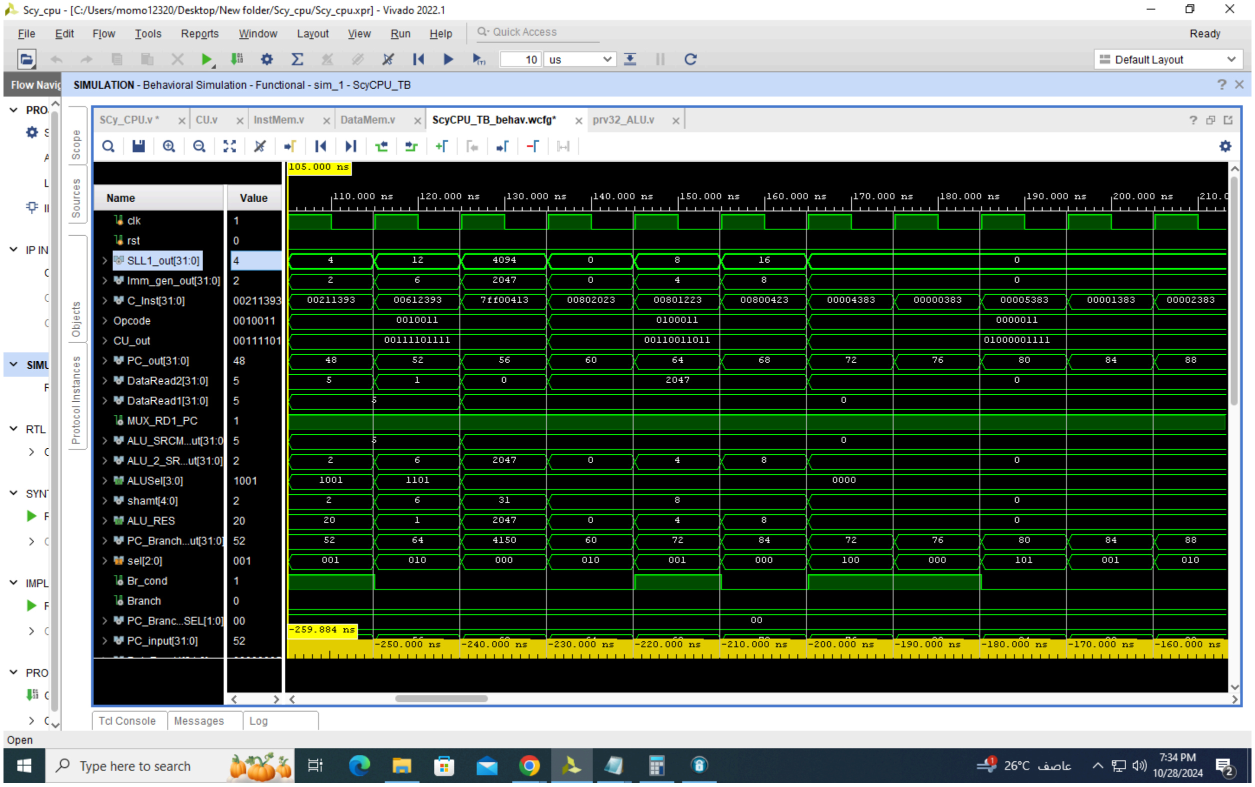
Name	Value
clk	0
rst	0
SLL1_out[31:0]	510
Imm_gen_out[31:0]	255
C_Inst[31:0]	0ff0000f
Opcode	0001111
CU_out	00111001
PC_out[31:0]	148
DataRead2[31:0]	0
DataRead1[31:0]	0
MUX_RD1_PC	0
ALU_SRCM...ut[31:0	0
ALU_2_SR...ut[31:0]	0
ALUSel[3:0]	0000
shamt[4:0]	31
ALU_RES	0
PC_Branch...ut[31:0]	658
sel[2:0]	000
Br_cond	1
Branch	0
PC_Branc...SEL[1:0]	10
PC_input[31:0]	0



Scy_cpu - [C:/Users/momo12320/Desktop/New folder/Scy_cpu/Scy_cpu.xpr] - Vivado 2022.1

SIMULATION - Behavioral Simulation - Functional - sim_1 - ScyCPU_TB

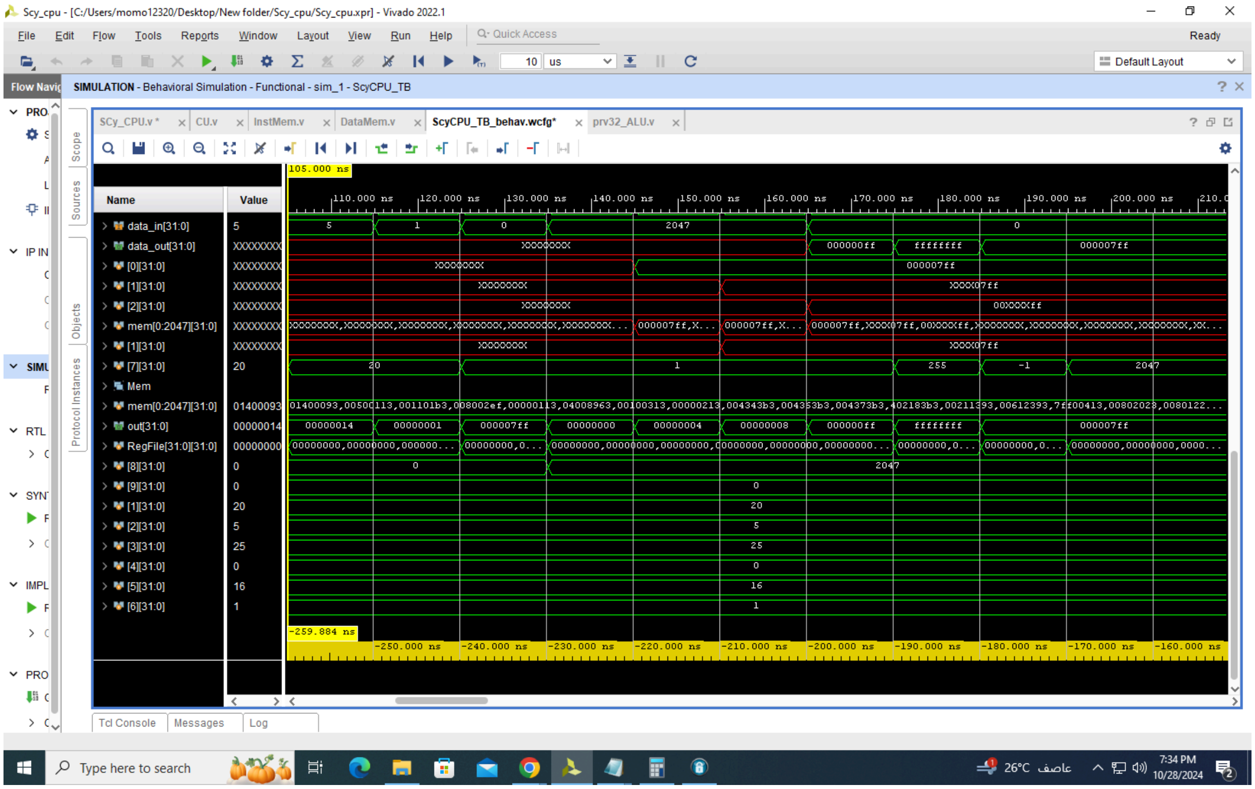
```
Name                    Value
data_in[31:0]           0
data_out[31:0]          000007ff
[0][31:0]               000007ff
[1][31:0]               XXXX07ff
[2][31:0]               00XXXXff
mem[0:2047][31:0]       000007ff,X
[1][31:0]               XXXX07ff
[7][31:0]               1
Mem
mem[0:2047][31:0]       01400093
out[31:0]               00000000
RegFile[31:0][31:0]     00000000
[8][31:0]               2047
[9][31:0]               2
[1][31:0]               20
[2][31:0]               5
[3][31:0]               25
[4][31:0]               0
[5][31:0]               16
[6][31:0]               1
```



Scy_cpu - [C:/Users/momo12320/Desktop/New folder/Scy_cpu/Scy_cpu.xpr] - Vivado 2022.1

SIMULATION - Behavioral Simulation - Functional - sim_1 - ScyCPU_TB

```
Name                    Value
clk                     1
rst                     0
SLL1_out[31:0]          4
Imm_gen_out[31:0]       2
C_Inst[31:0]            00211393
Opcode                  0010011
CU_out                  00111101
PC_out[31:0]            48
DataRead2[31:0]         5
DataRead1[31:0]         5
MUX_RD1_PC              1
ALU_SRCM...ut[31:0      5
ALU_2_SR...ut[31:0]     2
ALUSel[3:0]             1001
shamt[4:0]              2
ALU_RES                 20
PC_Branch...ut[31:0]    52
sel[2:0]                001
Br_cond                 1
Branch                  0
PC_Branc...SEL[1:0]     00
PC_input[31:0]          52
```

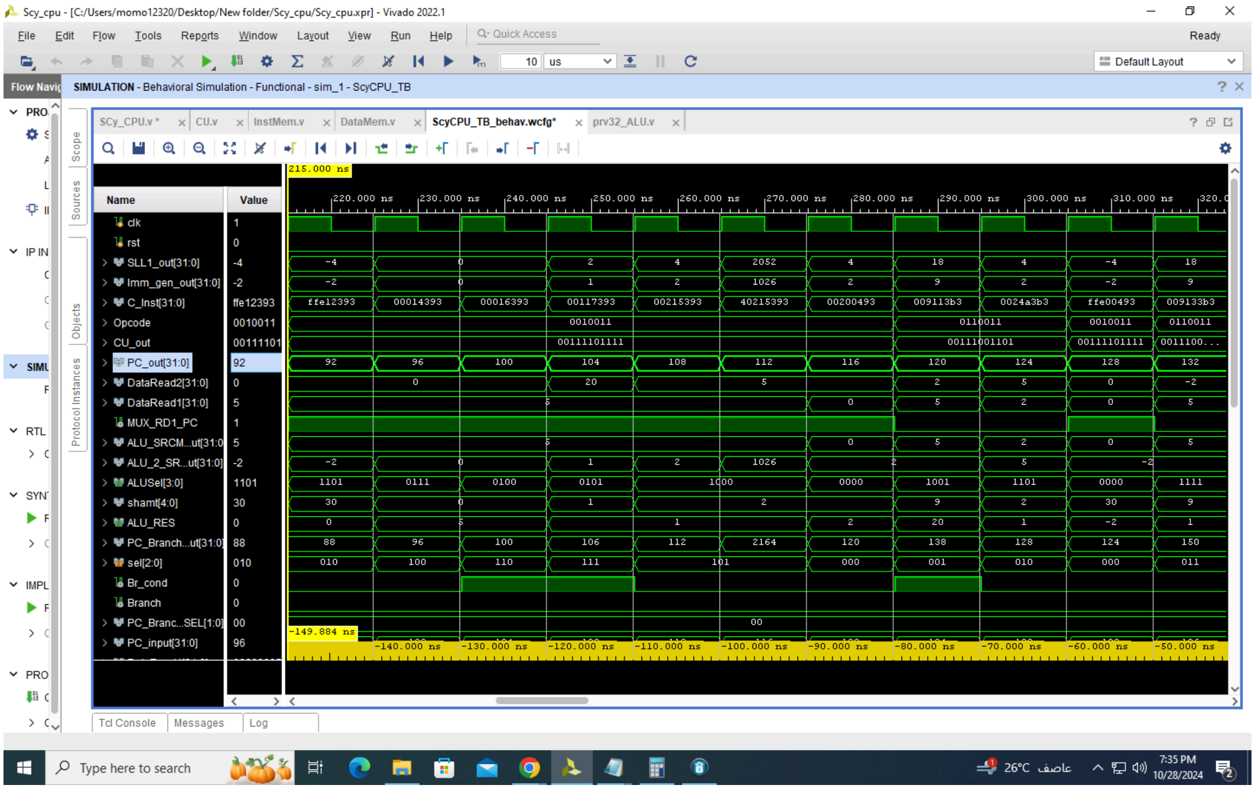


Scy_cpu - [C:/Users/momo12320/Desktop/New folder/Scy_cpu/Scy_cpu.xpr] - Vivado 2022.1

SIMULATION - Behavioral Simulation - Functional - sim_1 - ScyCPU_TB

105.000 ns

Name	Value
data_in[31:0]	5
data_out[31:0]	XXXXXXXX
[0][31:0]	XXXXXXXX
[1][31:0]	XXXXXXXX
[2][31:0]	XXXXXXXX
mem[0:2047][31:0]	XXXXXXXX
[1][31:0]	XXXXXXXX
[7][31:0]	20
Mem	
mem[0:2047][31:0]	01400093
out[31:0]	00000014
RegFile[31:0][31:0]	00000000
[8][31:0]	0
[9][31:0]	0
[1][31:0]	20
[2][31:0]	5
[3][31:0]	25
[4][31:0]	0
[5][31:0]	16
[6][31:0]	1

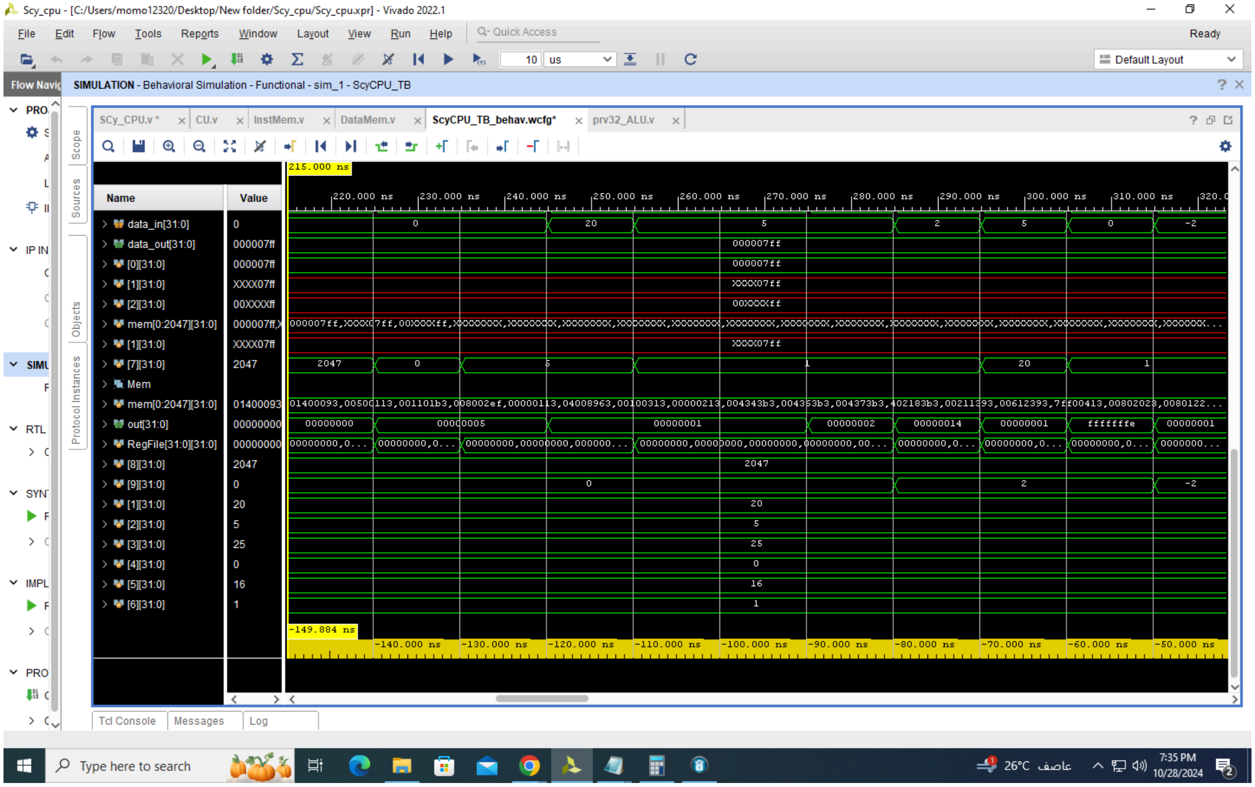


Scy_cpu - [C:/Users/momo12320/Desktop/New folder/Scy_cpu/Scy_cpu.xpr] - Vivado 2022.1

SIMULATION - Behavioral Simulation - Functional - sim_1 - ScyCPU_TB

215.000 ns

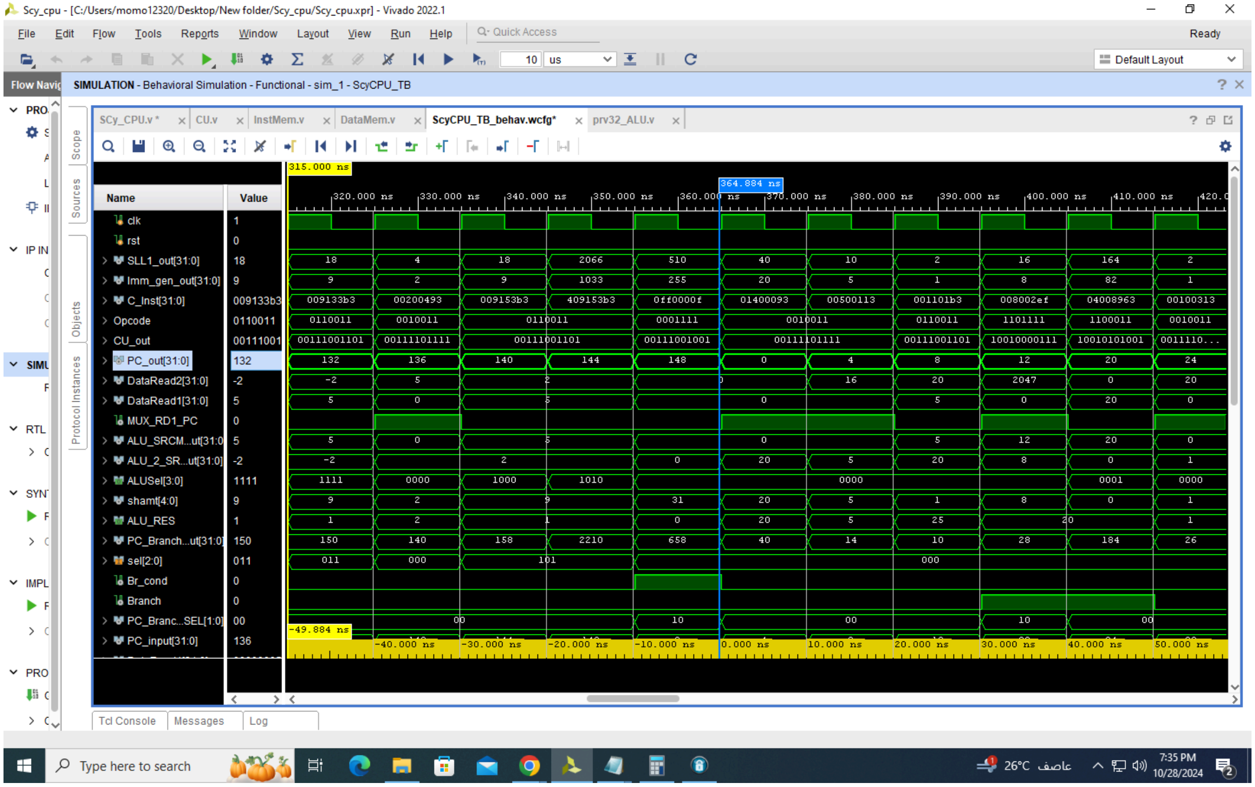
Name	Value
clk	1
rst	0
SLL1_out[31:0]	-4
Imm_gen_out[31:0]	-2
C_Inst[31:0]	ffe12393
Opcode	0010011
CU_out	00111101
PC_out[31:0]	92
DataRead2[31:0]	0
DataRead1[31:0]	5
MUX_RD1_PC	1
ALU_SRCM...ut[31:0]	5
ALU_2_SR...ut[31:0]	-2
ALUSel[3:0]	1101
shamt[4:0]	30
ALU_RES	0
PC_Branch...ut[31:0]	88
sel[2:0]	010
Br_cond	0
Branch	0
PC_Branc...SEL[1:0]	00
PC_input[31:0]	96



Scy_cpu - [C:/Users/momo12320/Desktop/New folder/Scy_cpu/Scy_cpu.xpr] - Vivado 2022.1

SIMULATION - Behavioral Simulation - Functional - sim_1 - ScyCPU_TB

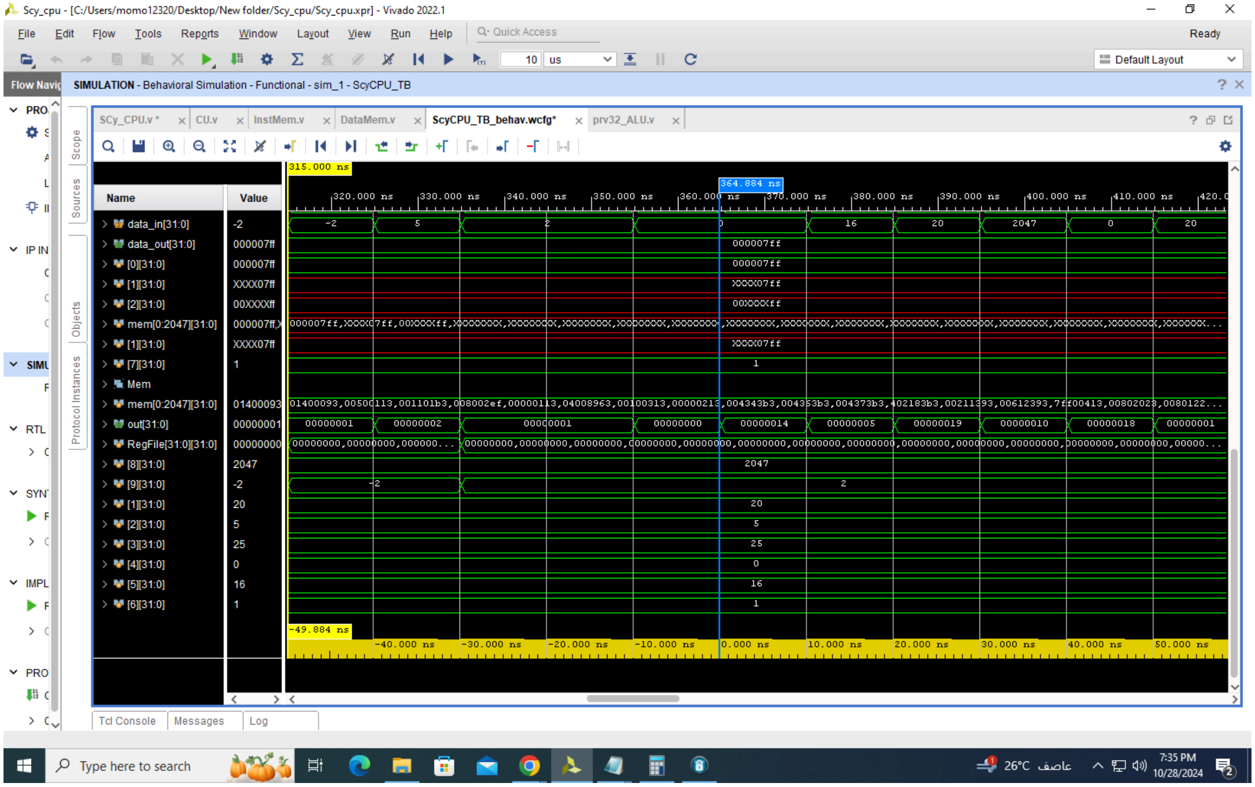
Name	Value
data_in[31:0]	0
data_out[31:0]	000007ff
[0][31:0]	000007ff
[1][31:0]	XXXX07ff
[2][31:0]	00XXXXff
mem[0:2047][31:0]	000007ff,X
[1][31:0]	XXXX07ff
[7][31:0]	2047
Mem	
mem[0:2047][31:0]	01400093
out[31:0]	00000000
RegFile[31:0][31:0]	00000000
[8][31:0]	2047
[9][31:0]	0
[1][31:0]	20
[2][31:0]	5
[3][31:0]	25
[4][31:0]	0
[5][31:0]	16
[6][31:0]	1



Scy_cpu - [C:/Users/momo12320/Desktop/New folder/Scy_cpu/Scy_cpu.xpr] - Vivado 2022.1

SIMULATION - Behavioral Simulation - Functional - sim_1 - ScyCPU_TB

Name	Value
clk	1
rst	0
SLL1_out[31:0]	18
Imm_gen_out[31:0]	9
C_Inst[31:0]	009133b3
Opcode	0110011
CU_out	00111001
PC_out[31:0]	132
DataRead2[31:0]	-2
DataRead1[31:0]	5
MUX_RD1_PC	0
ALU_SRCM...ut[31:0]	5
ALU_2_SR...ut[31:0]	-2
ALUSel[3:0]	1111
shamt[4:0]	9
ALU_RES	1
PC_Branch...ut[31:0]	150
sel[2:0]	011
Br_cond	0
Branch	0
PC_Branc...SEL[1:0]	00
PC_input[31:0]	136



Name	Value
data_in[31:0]	-2
data_out[31:0]	000007ff
[0][31:0]	000007ff
[1][31:0]	XXXX07ff
[2][31:0]	00XXXXff
mem[0:2047][31:0]	000007ff,X
[1][31:0]	XXXX07ff
[7][31:0]	1
Mem	
mem[0:2047][31:0]	01400093
out[31:0]	00000001
RegFile[31:0][31:0]	00000000
[8][31:0]	2047
[9][31:0]	-2
[1][31:0]	20
[2][31:0]	5
[3][31:0]	25
[4][31:0]	0
[5][31:0]	16
[6][31:0]	1

5. Conclusion:

In conclusion, this project successfully demonstrates the design and implementation of a pipelined RISC-V processor on the Nexys A7 FPGA board, meeting the requirements of the RV32I instruction set. Through our Verilog design, we integrated all necessary components, including the ALU, control unit, memory, and hazard handling mechanisms, to ensure correct and efficient instruction execution. The three-stage pipeline architecture and effective CPI=2 strategy effectively manage structural hazards associated with single-port memory.