# Contents



## Preface

The work contained in this PDF is an attempt on my part to synthesize the entirety of my understanding of monolithic, or "fully integrated" power conversion. I am doing this to improve my technical writing and communication abilities, in addition to furthering my own understanding of the material on which I write,

hopefully someone can make some use of these writings. At the time of writing this, I have no idea how long this will take, or if I will ever actually complete this work, but I hope to make some progress.

The current plan for writing this is to write it in such a way that it appeals to the reader from first principles, as much of the work and theory presented is without real world validation, or chip fabrication. The required background on the part of the reader is essentially that they understand:

- Circuit theory - Resistors, capacitors, inductors, nodal analysis, etc.
- Electronics - Comfortable with diodes, and transistors, along with there various uses. Transistors in saturation, triode, on resistance of transistors, gate capacitance, etc.
- Mathematics - Differential equations, laplace transforms, frequency domain analysis.

Provided the reader has background in these topics, it is my hope that my communication abilities are sufficient enough to make the following writings understandable.

# Chapter 1

# Introduction

# Chapter 2

# Switched Capacitor Power Converters - Fundamentals

Switched Capacitor Power Converters (SCPCs)

## 2.1 Four Terminal Model

The four terminal model is the simplest place to begin the explanation of how SCPCs operate. In this, the circuit in Fig. 2.1 represents the most fundamental unit of the SCPC, with 4 different voltages being connected to a single capacitor through switches. This capacitor is referred to frequently as the flying capacitor in much of the literature, presumably because both the top and bottom plate voltages vary over time, and the capacitor is not "grounded".

The four terminal device operates in two different phases, referred to as phases 1 and 2. Phase one can be seen in Fig. 2.2a, where the clock ($\phi$) is high, causing switches $S_{T1}$ and $S_{B1}$ to be enabled. This results in a short circuit between the top plate and $V_{T1}$ (the top terminal voltage in phase 1), and a short between $V_{B1}$ and the bottom plate of the flying capacitor. The circuit corresponding to phase 2 can be seen in Fig. 2.2b, where the top plate is shorted to $V_{T2}$ and the bottom plate to $V_{B2}$.

This circuit effectively delivers current from $T2$ to $T1$ as well as moving current from $B2$ to $B1$. This occurs through the mechanism of stored charge on the flying capacitor. Consider phase 1, where the voltage drop across the capacitor ($V_C$) is $V_{T1} - V_{B1}$. In phase 2 however, the voltage drop across the capacitor is $V_{T2} - V_{B2}$, resulted in a change in voltage, and thus a charge flow ($Q$) equal to $Q = C_{Fly}(V_{T2} - V_{B2} - V_{T1} + V_{B1})$.

This charge flow will then occur in opposite value in the first phase. These charge transfers occur repeatedly, determined by the switching frequency ($f_{SW}$) of the clock. Given the switching frequency, the

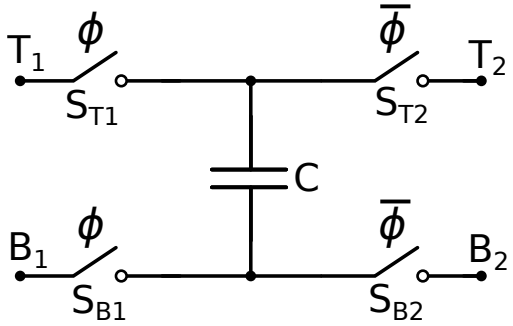
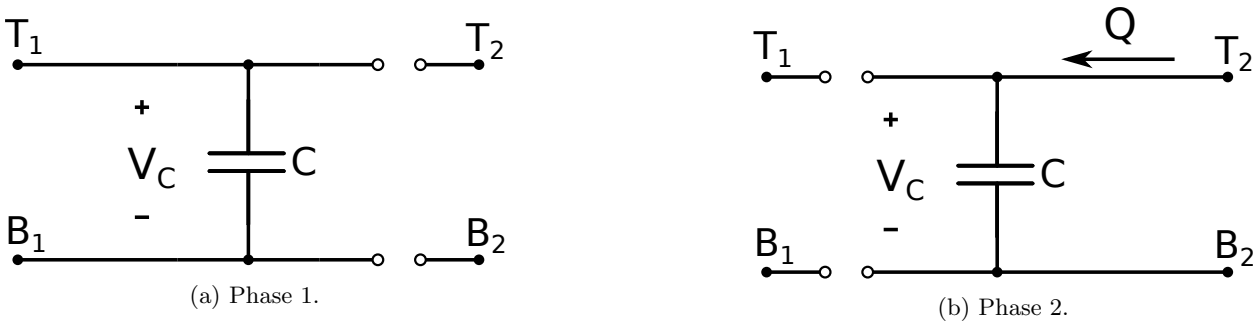



Figure 2.1: The fundamental Switched Capacitor cell.




(a) Phase 1.

(b) Phase 2.

Figure 2.2: Different phase representations of the circuit in Fig. 2.1

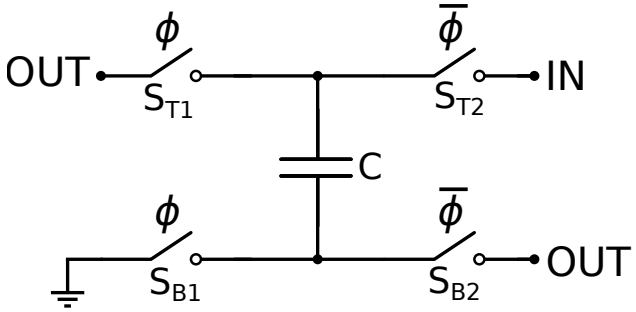



Figure 2.3: Switched capacitor cell in the buck configuration.

steady state/average current delivered by the flying capacitor can be calculated as,

$$I_{CFly} = Qf_{SW} = C_{Fly}f_{Sw}(V_{T2} - V_{B2} - V_{T1} + V_{B1}), \tag{2.1}$$

which in this case is the power moved between the different voltage domains. Consider the structure in the case where it is operating as a buck converter, corresponding to Fig. 2.3. The output current will be comprised of the current flowing through $S_{T1}$ and $S_{B2}$, which in this case is,

$$I_{OUT} = 2I_{CFly} = 2C_{Fly}f_{Sw}(V_{IN} - 2V_{OUT}), \tag{2.2}$$

while the input current is,

$$I_{IN} = I_{CFly} = C_{Fly}f_{Sw}(V_{IN} - 2V_{OUT}). \tag{2.3}$$

From these two equations, the power conversion efficiency ($\eta$) can be calculated by assessing the ratio between the output and input power,

$$\eta = \frac{P_{OUT}}{P_{IN}}, \tag{2.4}$$

given that $P_{OUT} = V_{OUT}I_{OUT}$, and $P_{IN} = V_{IN}I_{IN}$, this resolves to,

$$\eta = \frac{2V_{OUT}}{V_{IN}}. \tag{2.5}$$

This indicates a clear relationship between the input and output voltages, where the conversion ratio ($\gamma$) determines the efficiency of the structure. Unfortunately, this is presents a very large challenge for SCPCs, as many applications require different conversion ratios to operate optimally, resulting in an inevitable loss in efficiency.

An equivalent steady state model can also be developed, using resistors and dependent voltage sources, seen in Fig. 2.4 where $R_{Fly} = \frac{1}{C_{Fly}f_{Sw}}$.

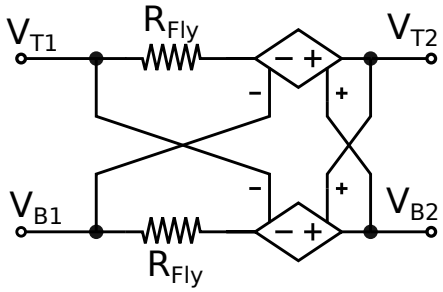



Figure 2.4: Resistive steady state model of the circuit in, Fig. 2.1.

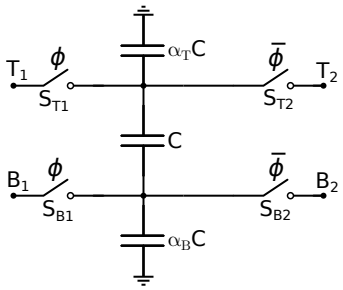



Figure 2.5: Switched capacitor cell incorporating effects of $\alpha_B$ and $\alpha_T$.

### 2.1.1 Parasitic Capacitance

It must be noted that the prior model of the flying capacitor presented was a simplification of the real model. Actual flying capacitors designed on-chip have stray or parasitic capacitances, where the top and bottom plate are capacitively coupled to other structures within the IC. Most notably is usually the capacitance between the bottom plate of $C_{Fly}$ and the substrate.

These stray capacitances are almost always directly proportional to the flying capacitor by some fixed ratio. This can be factored into the model of the flying capacitor, where the bottom plate parasitic ratio is $\alpha_B$ and the top plate is $\alpha_T$, as in Fig. 2.5. The details surrounding these parasitic capacitances will be covered in Chap. 3.

The impact of $\alpha_B$ and $\alpha_T$ on the four terminal model will now be covered. Consider first the impact of $\alpha_T$, in the first phase it is charged to $V_{T1}$, while in the second it is charged to $V_{T2}$. This corresponds to a charge flow of $Q_{\alpha T} = C_{Fly}\alpha_T(V_{T2} - V_{T1})$, which as a steady state current is, $I_{\alpha T} = f_{SW}C_{Fly}\alpha_T(V_{T2} - V_{T1})$. Similarly the current flow associated $\alpha_B$ is $I_{\alpha B} = C_{Fly}\alpha_B(V_{B2} - V_{B1})$.

From this, the current from $T2 \rightarrow T1$ is,

$$I_{T2,T1} = I_{CFly} + I_{\alpha_T} = f_{SW}C_{Fly}\left((V_{T2} - V_{B2} - V_{T1} + V_{B1}) + \alpha_T(V_{T2} - V_{T1})\right), \tag{2.6}$$

while the current from $B2 \rightarrow B1$ is,

$$I_{B2,B1} = -I_{CFly} + I_{\alpha_B} = f_{SW}C_{Fly}\left((V_{B2} - V_{T2} - V_{B1} + V_{T1}) + \alpha_B(V_{B2} - V_{B1})\right). \tag{2.7}$$

The resistive equivalent circuit can be seen in Fig. 2.6, which adds the effects of the parasitic capacitance to Fig. 2.4.

### 2.1.2 Switch Resistance

The prior models assumed that the switches had no effective resistance. This only models the behaviour correctly when the frequency is low enough that the capacitors can fully charge and discharge. In reality, the switches have some finite resistance $R_{SW}$, which will degrade the performance of the converter.

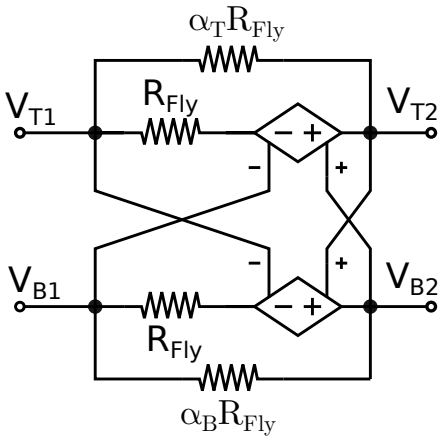
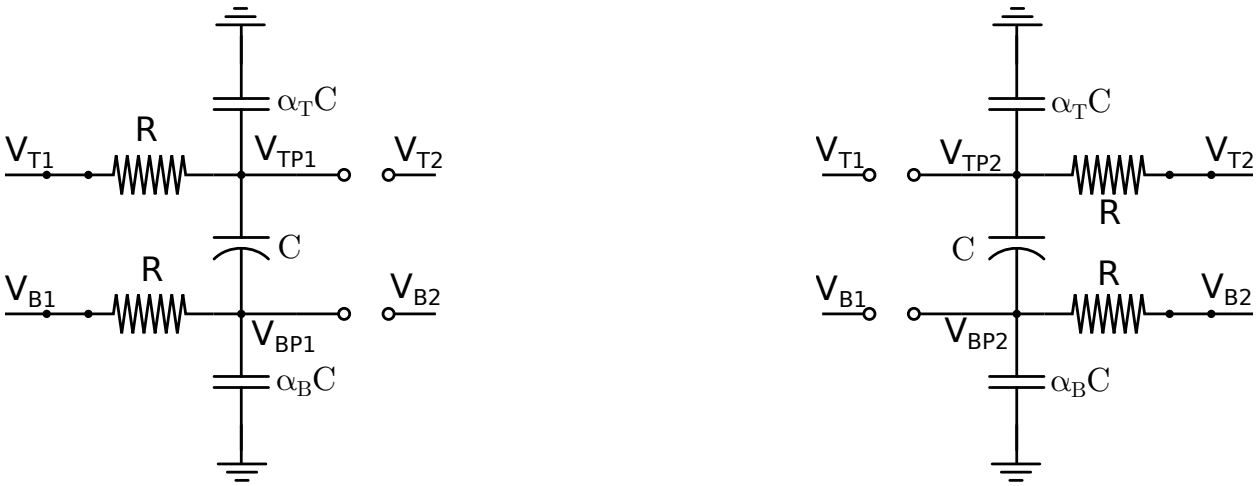



Figure 2.6: Resistive steady state model of the circuit in Fig. 2.5. Note that $R_{Fly} = \frac{1}{C_{Fly} f_{Sw}}$.




(a) Phase 1.

(b) Phase 2.

Figure 2.7: Circuit level equivalents of the circuit in Fig. 2.2a and 2.2b.

To begin, consider Fig. 2.7a, in which the switch resistance is included in the phase 1 circuit. Here we can see that the top and bottom plate voltages ($V_{TP1}$ and $V_{BP1}$) are separated from $T_1$ and $B_1$ by an equivalent switch resistance element. In order to describe $V_{TP1}$ and $V_{BP1}$ with respect to time, nodal analysis must be used.

The first nodal analysis occurs at node $V_{TP1}$, yielding,

$$s\alpha_T C_{Fly} V_{TP1} + sC_{Fly}(V_{TP1} - V_{BP1}) + \frac{V_{TP1} - V_{T1}}{R_{SW}} = 0. \tag{2.8}$$

Similarly, a nodal analysis at the bottom plate node yields,

$$s\alpha_B C_{Fly} V_{BP1} + sC_{Fly}(V_{BP1} - V_{TP1}) + \frac{V_{BP1} - V_{B1}}{R_{SW}} = 0. \tag{2.9}$$

The goal of the nodal analysis is to identify the dominant poles of the circuit so that a first order approximation can be used to describe the voltage. For simplicity we set $V_{B1} = 0$, though the choice of $V_{T1}$ or $V_{B1}$ is arbitrary. The resulting transfer function for $V_{TP1}$ is,

$$V_{TP1} = \frac{sV_C CR(\alpha_B CRs + 1)}{s^2 C^2 R^2(\alpha_B + \alpha_T + \alpha_B\alpha_T) + sCR(2 + \alpha_B + \alpha_T) + 1}, \tag{2.10}$$

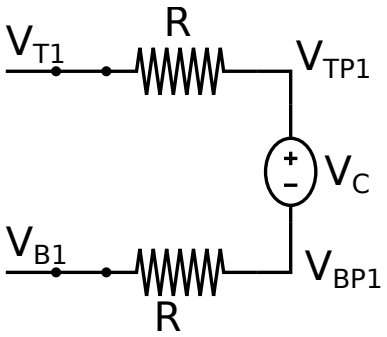



Figure 2.8: Electrical equivalent to Fig. 2.7a at t=0.

the dominant pole of the circuit is located at, $s \approxeq \frac{2}{RC(4+\alpha_B+\alpha_T)}$. Using the dominant pole, a first order approximation of the exponential decay can be used. For example, the exponential first order decay at node $V_{TP1}$ is,

$$V_{TP1}(t) = V_{initial} \exp\left(\frac{-t}{\tau}\right) + V_{T1}\left(1 - \exp\left(\frac{-t}{\tau}\right)\right), \tag{2.11}$$

where $\tau$ is determined by the dominant pole,

$$\tau \approxeq \frac{2}{RC(4+\alpha_B+\alpha_T)}. \tag{2.12}$$

Given that each phase occurs for time equal to half of the switching period, the final voltage at the end of the time step is,

$$V_{TP1,final} = V_{TP1}\left(t = \tfrac{T_{SW}}{2}\right) = V_{initial} \exp\left(\frac{-T_{SW}}{2\tau}\right) + V_{T1}\left(1 - \exp\left(\frac{-T_{SW}}{2\tau}\right)\right). \tag{2.13}$$

A substitution can be made for the exponential decay, where

$$A = \exp\left(\frac{-T_{SW}}{2\tau}\right) = \exp\left(\frac{-1}{f_{SW} RC(4+\alpha_B+\alpha_T)}\right). \tag{2.14}$$

The corresponding equations for the final voltages and their relationship is then as follows for all 4 nodes,

$$V^f_{TP1} = AV^i_{TP1} + (1-A)V_{T1}, \tag{2.15}$$

$$V^f_{BP1} = AV^i_{BP1} + (1-A)V_{B1}, \tag{2.16}$$

$$V^f_{TP2} = AV^i_{TP2} + (1-A)V_{T2}, \tag{2.17}$$

$$V^f_{BP2} = AV^i_{BP2} + (1-A)V_{B2}. \tag{2.18}$$

Next, to determine the initial conditions, consider the value of $V_C$. During the start of phase 1, $V_C$ will be directly related to the voltage drop across the capacitor at the end of phase 2 $V_C = V^f_{TP2} - V^f_{BP2}$. The initial conditions can then be acquired using Fig. 2.8, which represents Fig. 2.7a immediately at the start of Phase 1. From this,

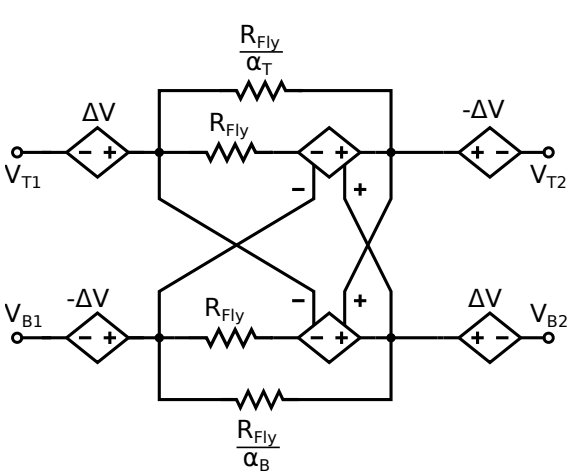
$$V^i_{TP1} = \frac{V_{T1} + V_{B1} + V^f_{TP2} - V^f_{BP2}}{2}, \tag{2.19}$$

while

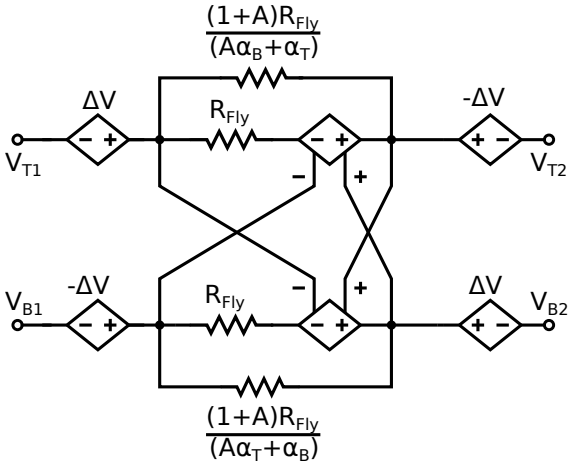
$$V^i_{BP1} = \frac{V_{T1} + V_{B1} + V^f_{TP2} - V^f_{BP2}}{2}. \tag{2.20}$$

A similar procedure can be followed to acquire the initial conditions for phase 2, where

$$V^i_{TP2} = \frac{V^f_{TP1} - V^f_{BP1} + V_{T2} + V_{B2}}{2}, \tag{2.21}$$




(a) Steady state 4 terminal model.




(b) Modified version incorporating high frequency effects on $\alpha_B$ and $\alpha_T$.

Figure 2.9: Two models of for the switched capacitor cell incorporating switch resistance.

and

$$V^i_{BP2} = \frac{V^f_{BP1} - V^f_{TP1} + V_{T2} + V_{B2}}{2}. \tag{2.22}$$

These equations can be substituted into the equations for the final voltages, to yield the solved equations,

$$V^f_{TP1} = V_{T1} + \Delta V, \tag{2.23}$$

$$V^f_{BP1} = V_{B1} - \Delta V, \tag{2.24}$$

$$V^f_{TP2} = V_{T2} - \Delta V, \tag{2.25}$$

and

$$V^f_{BP2} = V_{B2} + \Delta V \tag{2.26}$$

where

$$\Delta V = \frac{A(V_{B1} - V_{T1} - V_{B2} + V_{T2})}{2(A+1)}. \tag{2.27}$$

From this, the 4 terminal device model in 2.9a can be generated, which can easily be implemented in pspice, verilogA, or a number of other simulators. The accuracy of the model was tested using pspice, where the circuit in Fig. 2.5 was implemented using switches with on resistance. The resulting comparisons run can be seen in Fig. 2.10, it can be seen that while the model is very accurate for the $\alpha_B = \alpha_T$ case, there is substantial error when $\alpha_B \neq \alpha_T$.

This error can be understood by considering Fig. 2.7b at high frequencies. Consider the transfer function for $V_{TP2}$ with respect to $V_{T2}$ and $V_{B2}$ is,

$$V_{TP2} = \frac{sRC(V_{T2}(1+\alpha_B) + V_{B2}) + V_{T2}}{s^2C^2R^2(\alpha_B + \alpha_T + \alpha_B\alpha_T) + sCR(2 + \alpha_B + \alpha_T) + 1}, \tag{2.28}$$

indicating that at high frequencies, the voltage at node $V_{TP2}$ is determined by $V_{T2}$ and $V_{B2}$ in roughly equal parts. This is incorporated into the model as seen in Fig. 2.9b, and the resulting comparisons can be seen in Fig. 2.11, where the new model appears accurate.

It should be noted however, that while the model in Fig. 2.9a is compact, it does not lend itself nicely to hand calculation. Instead, the circuit in Fig. 2.12 is more appropriate, where

$$R_1 = \frac{(A+1)^2}{fC(1 - A^2(1+\alpha_B) - A\alpha_T)}, \tag{2.29}$$

and

$$R_2 = \frac{(A+1)^2}{fC(1 - A^2(1+\alpha_T) - A\alpha_B)}. \tag{2.30}$$

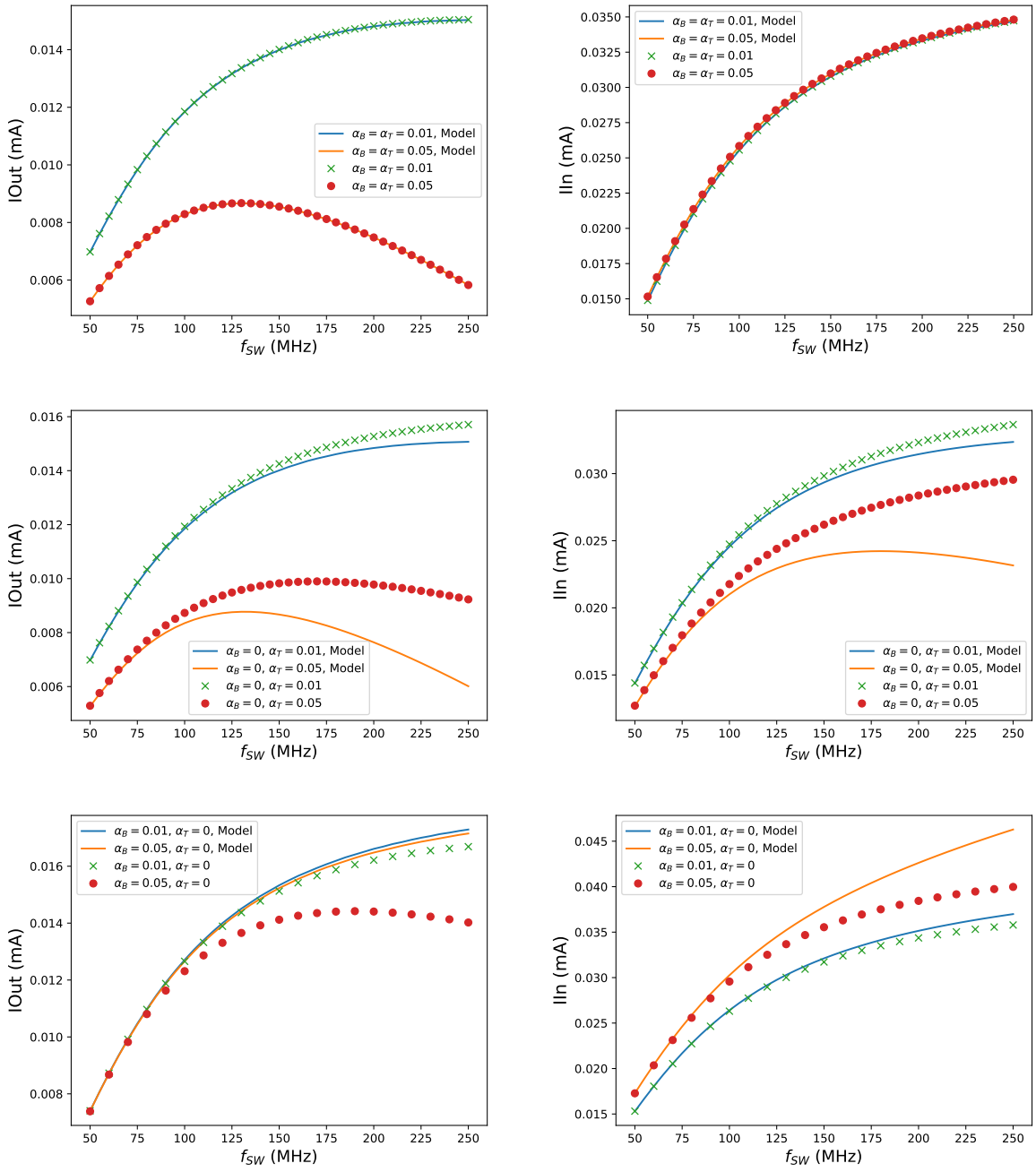



Figure 2.10: Comparison between simulation and model data, for the switched capacitor cell seen in Fig. 2.5. The circuit conditions were $V_{OUT} = 1.85\,\mathrm{V}$, $V_{IN} = 1\,\mathrm{V}$, $R = 1\omega$ and $C = 1n$.

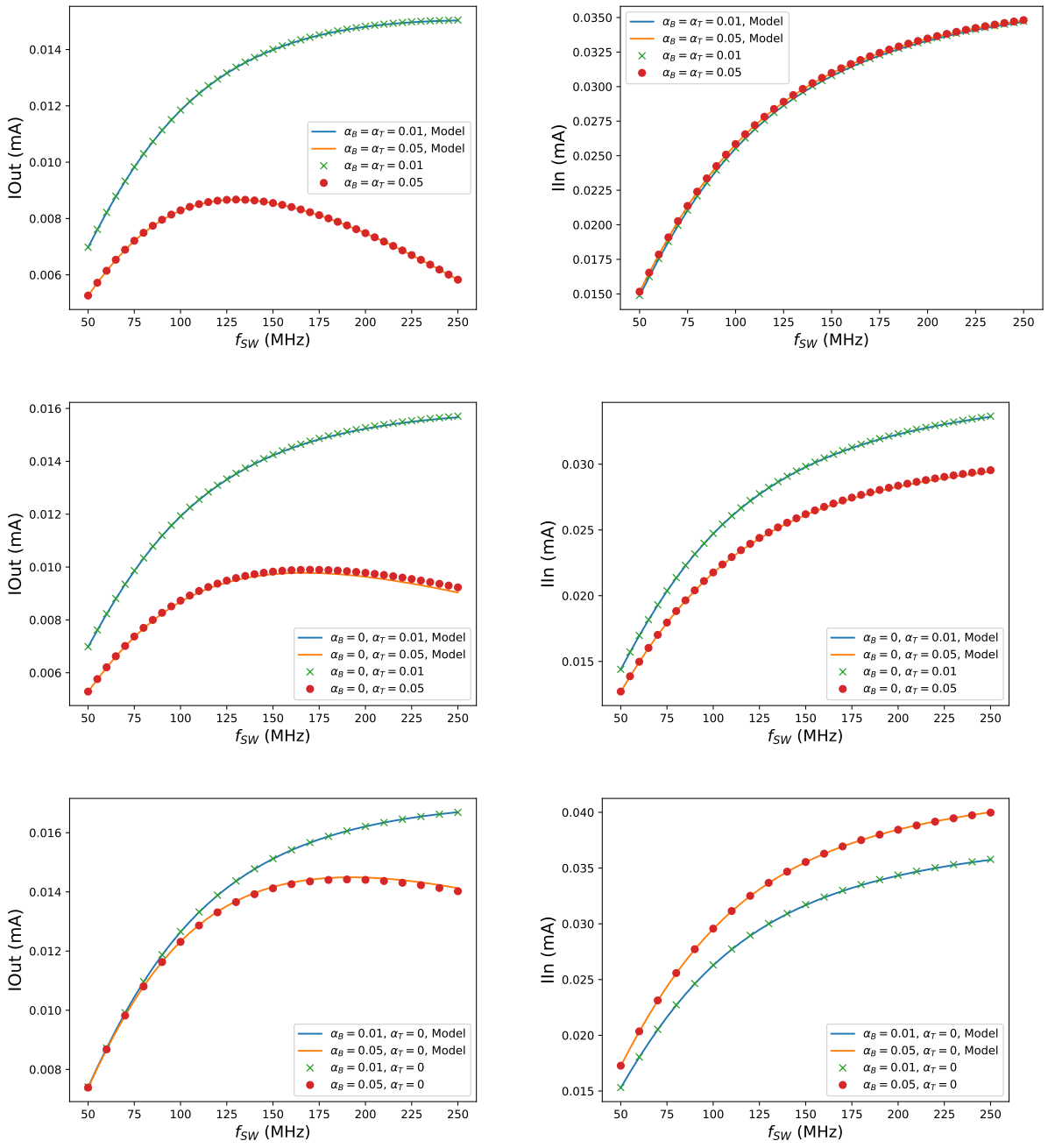



Figure 2.11: Comparison between simulation and model data, for the switched capacitor cell seen in Fig. 2.5. The model has been modified to incorporate the circuit back-flow approximation. The circuit conditions were $V_{OUT} = 1.85\,\mathrm{V}$, $V_{IN} = 1\,\mathrm{V}$, $R = 1\omega$ and $C = 1n$.

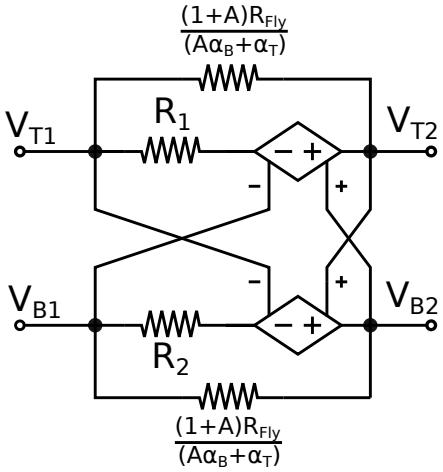



Figure 2.12: Equivalent circuit to 2.9a.

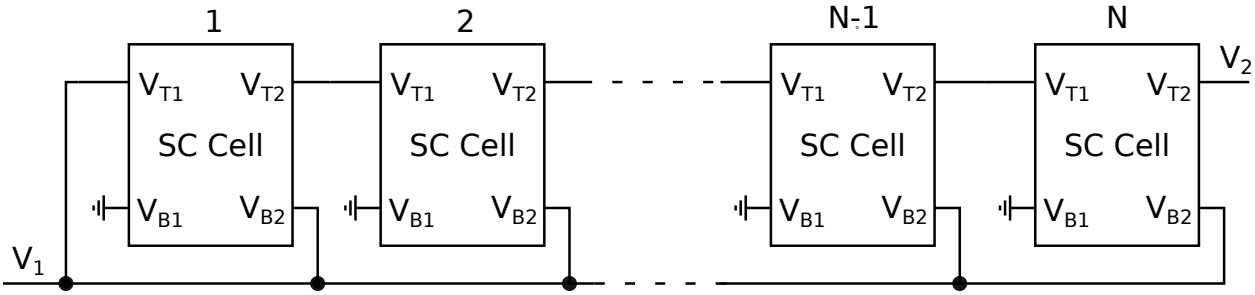



Figure 2.13: N-stage Dickson converter comprised of the cells in **??**.

## 2.2 SCPC Architectures

There are numerous architectures which are used in SCPC design in order to implement different voltage conversion ratios. While the SC cell in **??** is capable of implementing 2:1 or 1:2 conversion, many applications require different voltage conversion ratios, facilitating different architectures.

### 2.2.1 Dickson

The Dickson topology can be understood from the diagram in 2.13, in which a generic $N$ stage Dickson is shown. The resulting voltage conversion ratio is N+1:1 in a buck conversion ratio, and 1:N+1 in a boost.

The benefits of the structure are that it has a constant voltage stress across all of its transistors, with increasing voltage stress across its capacitors per stage. The output resistance and efficiency can be acquired using the 4-terminal models developed in Section 2.1, though the choice to include switch resistance depends on how close to the FSL the converter is.

### 2.2.2 Series Parallel

A diagram of the Series Parallel topology is in Fig. 2.14 for a generic $N$ stages. Similar to the Dickson, the resulting conversion ratio is N+1:1 in a buck configuration, and 1:N+1 in a boost.

The structure features a constant stress across the flying capacitors, with switch voltage stresses depending on $N$.

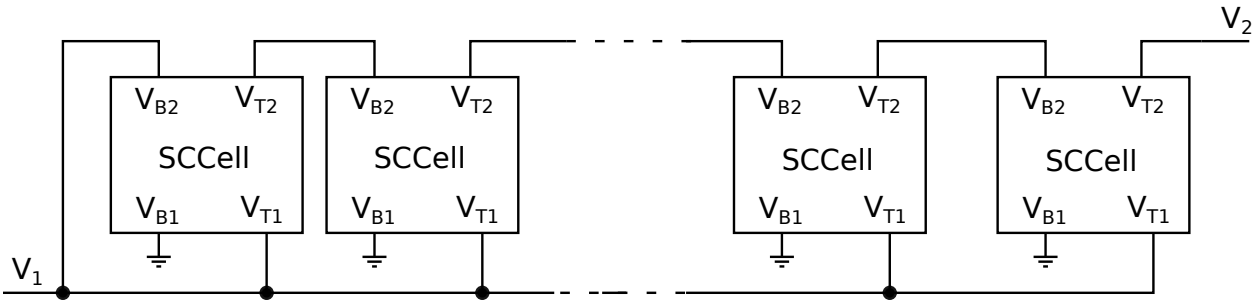



Figure 2.14: N-stage Series Parallel converter comprised of the cells in **??**.

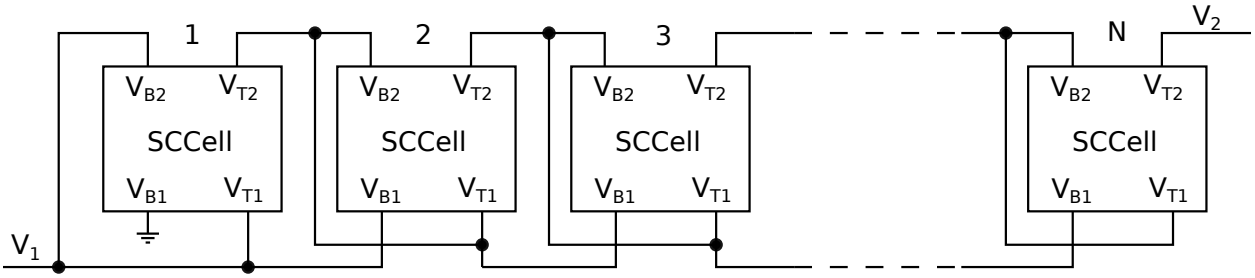



Figure 2.15: N-Stage Cockcroft-Walton SCPC.

### 2.2.3 Cockcroft and Walton

An N-Stage Cockcroft and Walton (CW) configuration can be seen in Fig. 2.15. The corresponding voltage conversion ratio is 1:N+1.

The primary feature of the CW SCPC architecture is its constant voltage stress across both its flying capacitors and transistors. This comes at a substantial increase in output resistance however.

The structure features a constant stress across the flying capacitors, in addition to constant stress across the transistors.

### 2.2.4 Fractional Converters

### 2.2.5 Fibonacci and Exponential

The Fibonacci charge pump refers to the architecture in 2.16, in which the VCR follows the Fibonacci sequence. The exponential charge pump architecture refers to Fig. 2.17, in which the VCR $= 2^N$.

Both these architectures feature voltage, and capacitor stresses which are dependent on the number of stages.

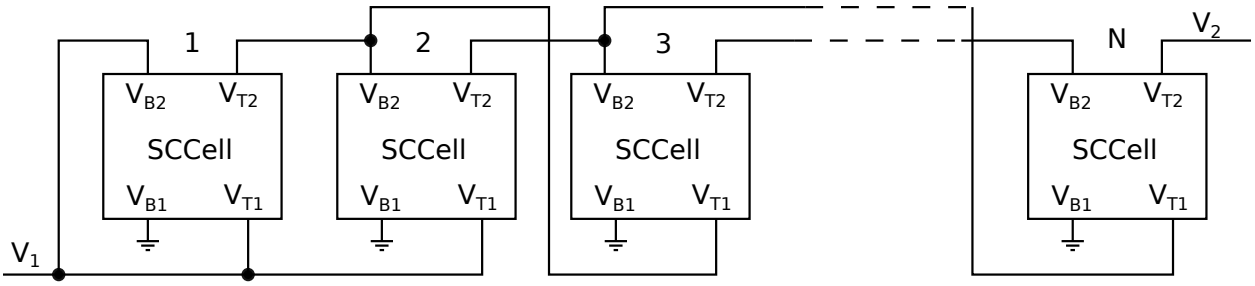



Figure 2.16: N-Stage Fibonacci SCPC.

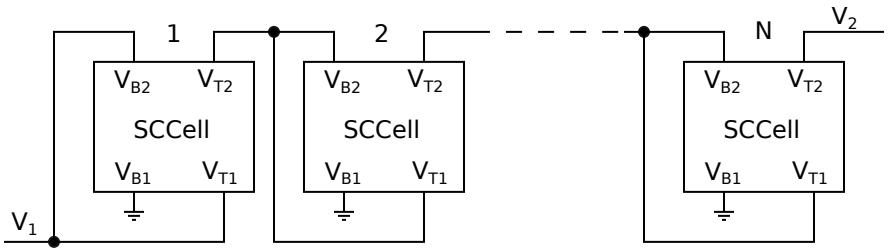



Figure 2.17: N-Stage Exponential SCPC.

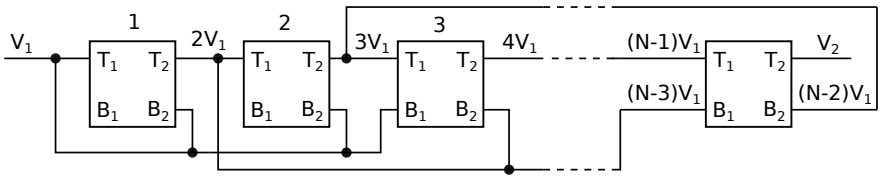



Figure 2.18: Modified Cockcroft-Walton architecture acommodating stage skipping.

### 2.2.6 Hybrid Architectures

Here are various SCPC architectures which are potentially useful in a number of scenarios, depending entirely on the technology, and the desired conversion ratio.

For example, consider the circuit in Fig. 2.18, which could be considered a modified CW architecture. The structure maintains a constant transistor voltage stress with a capacitor voltage stress of $2V_1$, the benefit over CW being a reduction in output resistance.

## 2.3 Isolating Stage

# Chapter 3

# Flying Capacitor Design

# Chapter 4

# Transistor Considerations

# Chapter 5

# Time Interleaving

# Chapter 6

# Charge Reuse

# Chapter 7

# Stage Outphasing

# Chapter 8

# Reconfigurable Architectures

# Chapter 9

# Advanced Models

There are a number of other important effects not accounted for by the models in Chap. 2. The chapter developed functioning steady state models, but no time, or frequency domain models were developed. In addition, there are a number of technology dependent effects which can impact performance which need to be considered.

## 9.1 Transistor Leakage

One increasingly important design variable at smaller technology nodes is the impact of leakage between the various nodes of the transistors.

### 9.1.1 Sub-Threshold Leakage

Sub-Threshold leakage refers to the current that flows between the drain and the source of the transistor when the transistor is turned off.

The analysis begins by assuming that the flying capacitor cell almost completely charges and discharges each cycle. The assumption is based on the fact that this is the region in which the leakage effects have the largest impact on performance.

Next, the impact on the SCPC can be understood by considering the various phases of the converter, as in Fig. **??**. In phase 1, $V_{TP1} = V_{T1}$, resulting in a $V_{DS}$ of $V_{T2} - V_{T1}$ across $S_{T2}$. Similarly, $V_{BP1} = V_{B1}$, making $V_{DS} = V_{B2} - V_{B1}$ for $S_{B2}$. Likewise in phase 2, the $V_{DS}$ of $S_{T1} = V_{T2} - V_{T1}$, while the $V_{DS}$ of $S_{B1} = V_{B2} - V_{B1}$.

Assuming the phases occupy equal portions of the period, then

$$I_{Leak,T2,T1} = \frac{I_{Leak,ST2} = I_{Leak,ST1}}{2}, \tag{9.1}$$

where $I_{VDS,ST2}$ denotes the drain to source leakage of $S_{T2}$, while

$$I_{Leak,B2,B1} = \frac{I_{Leak,SB2} = I_{Leak,SB1}}{2}, \tag{9.2}$$

which get incorporated into the model as in Fig. **??**. In order to acquire their leakage values, the transistors comprising switches must be simulated at their corresponding $V_{DS}$. Additionally, if the leakage varies substantially with $V_{DS}$, then it is advisable to include a voltage dependence. Lastly, there is temperature variation in the sub-threshold leakage which will impact performance and may need to be considered.

## 9.2 Frequency Domain Model

Depending on the way in which the SCPCs are used, there is a need to develop models which approximate the impedance of the structure. If it is assumed that the switching frequency of the structure is constant

with respect to time, then the model in Fig. **??** provides an excellent first order approximation. The added impedance between the top and bottom plate is a result of the instantaneous connections which occur in both Phase 1 and Phase 2. As the converter is split between these two phases 50% of the time, the impedance of the elements is doubled.

# Chapter 10

# Control

# Chapter 11

# Design Examples

# Chapter 12

# Continuously Scalable