A Four Terminal Charge Pump Model Incorporating Device Leakage Effects

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I. Abstract

This paper constructs a steady state model of the continuous conversion ratio charge pump architecture from first principles, incorporating incomplete charge transfer and finite switch resistance. The model is then verified using a pspice model of the circuit, and the limitations of the assumptions are discussed.

II. Introduction

There are several pre-existing models of switched capacitor power converters (SCPCs) which model the performance of the structures under ideal switching conditions, with full charge transfer and minimal device parasitics. However, to the best of the authors knowledge, there exist no models which incorporate both the effect of transistor leakage, or non-ideal clock generation. These factors are becoming increasingly important, as technology nodes scale down, increasing leakage effects which need to be incorporated to ensure the accuracy of models.

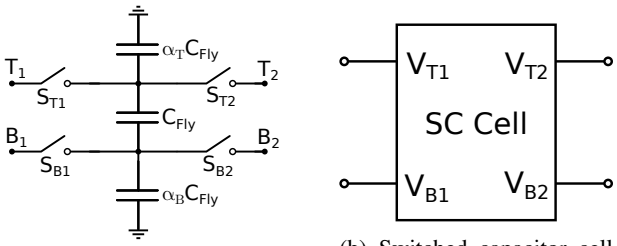
The following work develops a model of the SCPC incorporating finite switch resistance on both the top and bottom plates, along with transistor and capacitor leakage effects.

III. Steady State Model

The foundational building block of most Switched Capacitor Power Converter (SCPC) architectures is the circuit in Fig. 1a, where the flying capacitor connects to 4 unique voltage domains. This switched capacitor (SC) cell can then be abstracted as the four terminal device seen in Fig. 1b. The SC cell can be used to construct various dc-dc converter configurations, such as the three stage Dickson in Fig. 2 or the series parallel converter in Fig. 3.

A steady state circuit representation of the four terminal model can be seen in Fig. 4, where $R_{Fly} = \frac{1}{f_{SW} C_{Fly}}$. However, this model neglects the impact switch resistance has on the equivalent resistance of the cell.

The effect of incomplete charge transfer on the output and input charge characteristics of a dc-dc converter has been studied [1]. However, the model studied assumed ideal clock generation. The following analysis incorporates the resistance of clock drivers into the equations for input and output current.



(a) Switched capacitor circuit diagram.

(b) Switched capacitor cell abstraction.

Fig. 1: Four terminal circuit, and equivalent block level abstraction.

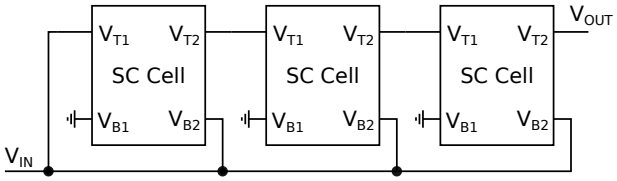


Fig. 2: Three Stage Dickson configuration using four terminal devices.

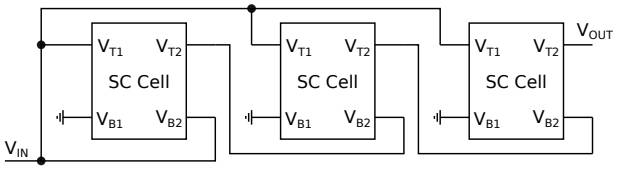


Fig. 3: Three Stage Series Parallel configuration using four terminal devices.

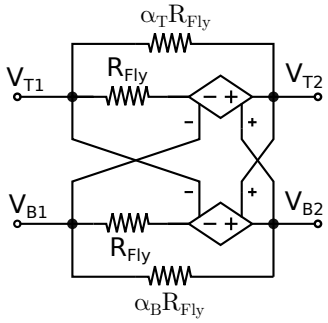
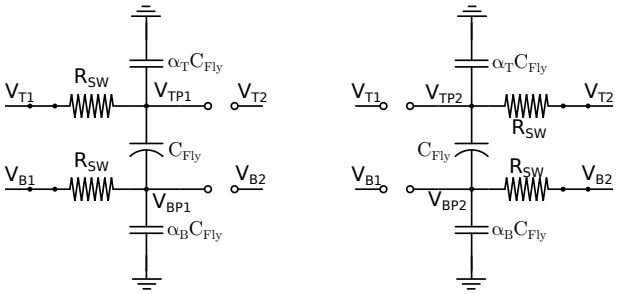


Fig. 4: Equivalent circuit model of the four terminal device operating under SSL conditions.



(a) Phase 1. (b) Phase 2.

Fig. 5: Equivalent representation of 1a, with switch resistance R_{SW}, for both of its phases.

A. Incomplete Charge Transfer

The associated analysis occurs at steady state with some assumptions:

- All the capacitors and resistors used in the analysis are linear and time invariant.
- The value of $\alpha_T + \alpha_B < 0.1$.

The circuit in Fig.1a, can be represented as Fig. 5a in its first phase, with Fig. 5b representing its second phase. The voltage at the top and bottom plates of the capacitor are labeled V_{TP} and V_{BP}, V_{TP1} for example, would specify top plate voltage in the first phase.

The first order approximation of V_{TP1} is,

$$V_{TP1}(t) = \exp\left(\frac{-t}{\tau}\right) V_{TP1}^{i} + \left(1 - \exp\left(\frac{-t}{\tau}\right)\right) V_{T1}, \tag{1}$$

where τ is the first order time constant of the circuit, and V_{TP1}^{i} is the initial value of V_{TP1} at the start of the first phase.

In order to acquire the value of τ, a frequency domain analysis of the structure in Fig. 5a can be performed. To simplify the analysis, the value of $V_{B1} = 0$, and the initial conditions on the capacitors are ignored, and the structure is analyzed with respect to V_{T1}, the resulting nodal equation at V_{TP1} is

$$\tfrac{V_{TP1}-V_{T1}}{R_{SW}} + s\alpha_T C V_{TP1} + sC(V_{TP1} - V_{BP1}) = 0, \tag{2}$$

similarly, a nodal analysis at V_{BP1} yields,

$$\tfrac{V_{BP1}}{R_{SW}} + s\alpha_B C V_{BP1} + sC(V_{BP1} - V_{TP1}) = 0. \tag{3}$$

These two nodal equations can then be used to solve for the dominant pole of the circuit, yielding

$$V_{TP1} = \tfrac{V_{T1}(sC(\alpha_B+1))}{s^2C^2R^2(\alpha_B+\alpha_T+\alpha_B\alpha_T)+sRC(2+\alpha_B+\alpha_T)+1}, \tag{4}$$

however, if it is assumed that $\alpha_T = \alpha_B$ then the simplified expression is,

$$V_{TP1} = \tfrac{V_{T1}(sC(\alpha_B+1))}{(s\alpha_B CR+1)(sCR(2+\alpha_B)+1)}. \tag{5}$$

The resulting first order time constant is then,

$$\tau = R_{ON} C_{Fly} (2 + \alpha_B), \tag{6}$$

The final value of V_{TP1} can be evaluated at $t = \frac{T_{SW}}{2}$, as phase 1 occupies approximately half the period,

$$V_{TP1}^{f} = \exp\left(\tfrac{-T_{SW}}{2\tau}\right) V_{TP1}^{i} + \left(1 - \exp\left(\tfrac{-T_{SW}}{2\tau}\right)\right) V_{T1}. \tag{7}$$

Finally, a substitution can be made, relating to the exponential decay at the end of the time step,

$$A = \exp\left(-\tfrac{T_{SW}}{2\tau}\right) = \exp\left(\tfrac{T_{SW}}{2R_{ON}C_{Fly}(2+\alpha_B)}\right), \tag{8}$$

which can be used to create a simplified expression for V_{TP1}^{f},

$$V_{TP1}^{f} = AV_{TP1}^{i} + (1 - A)V_{T1}. \tag{9}$$

A similar procedure can then be repeated for the other nodal voltages,

$$V_{BP1}^{f} = AV_{TP1}^{i} + (1 - A)V_{B1}, \tag{10}$$

$$V_{TP2}^{f} = AV_{TP2}^{i} + (1 - A)V_{T2}, \tag{11}$$

$$V_{BP2}^{f} = AV_{BP2}^{i} + (1 - A)V_{B2}. \tag{12}$$

The initial conditions of C_{Fly} at the start of each phase can be acquired using the voltage stored on the capacitor. The voltage stored on the capacitor at the end of any phase is $V_{TPx} - V_{BPx}$, where x is the phase. Using the voltage on the capacitor, the initial conditions can be constructed,

$$V_{TP1}^{i} = \tfrac{V_{TP2}^{f} - V_{BP2}^{f} + V_{T1} + V_{B1}}{2}, \tag{13}$$

$$V_{BP1}^{i} = \tfrac{V_{BP2}^{f} - V_{TP2}^{f} + V_{B1} + V_{T1}}{2}, \tag{14}$$

$$V_{TP2}^{i} = \tfrac{V_{TP1}^{f} - V_{BP1}^{f} + V_{T2} + V_{B2}}{2}, \tag{15}$$

$$V_{BP2}^{i} = \tfrac{V_{BP1}^{f} - V_{TP1}^{f} + V_{T2} + V_{B2}}{2}. \tag{16}$$

Using the equations for the initial conditions and the final voltages, the final voltages can be solved,

$$V_{TP1}^{f} = V_{T1} + \Delta V, \tag{17}$$

$$V_{BP1}^{f} = V_{B1} - \Delta V, \tag{18}$$

$$V_{TP2}^{f} = V_{T2} - \Delta V, \tag{19}$$

and

$$V_{BP2}^{f} = V_{B2} + \Delta V \tag{20}$$

where

$$\Delta V = \frac{A(V_{B1} - V_{T1} - V_{B2} + V_{T2})}{2(A+1)}. \tag{21}$$

This can then be used to generate the circuit model seen in Fig. 6, which will incorporate the effects of incomplete charge transfer.

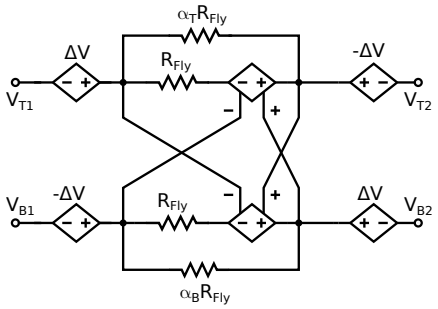


Fig. 6: Four terminal device model incorporating switch resistance.

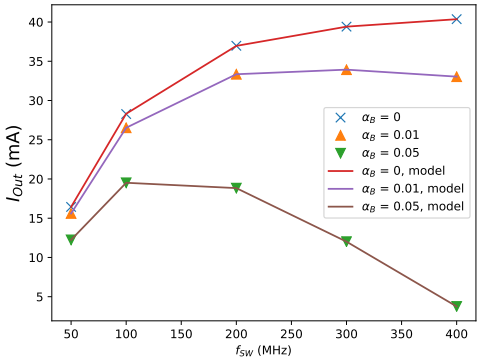


Fig. 7: Comparison of the modelled and simulated output current.

This can then be verified using simulations of the circuit, in which ideal switches are used. The simulated circuit is the N=3 Dickson Charge pump seen in Fig. 2, with two cores per stage 180° out of phase. The parameters used in the circuit are V_{IN} = 1V, V_{OUT} = 3.5V, C = 1n, R_{SW} = 1Ω. The simulations were run long enough to reach steady state, and the final values were recorded. The output and input currents of the structure were simulated for various frequencies and values of $\alpha_B = \alpha_T$. The corresponding comparisons between the simulation and model data can be seen in Fig. 7, and Fig. 8.

B. Leakage Effects

The leakage effects associated with the transistors are modelled using theory from the [] transistor models. The testing is performed in pspice, using the PTM to simulate the transistors used.

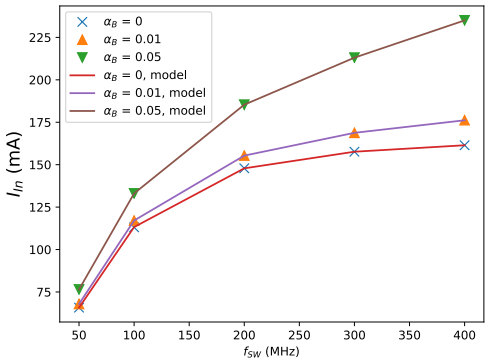


Fig. 8: Comparison of the modelled and simulated input current.

REFERENCES

[1] T. Tanzawa, "A switch-resistance-aware dickson charge pump model for optimizing clock frequency," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 6, pp. 336–340, 2011.