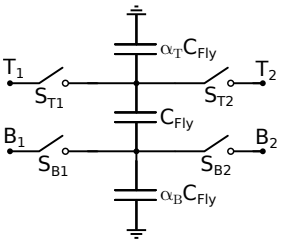
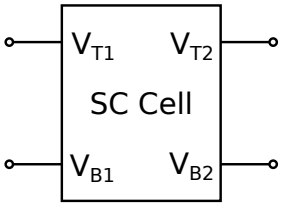
A Four Terminal Charge Pump Model Incorporating Device Leakage Effects

Mark Lipski



(a) Switched capacitor circuit diagram.



(b) Switched capacitor cell abstraction.

Fig. 1: Four terminal circuit, and equivalent block level abstraction.

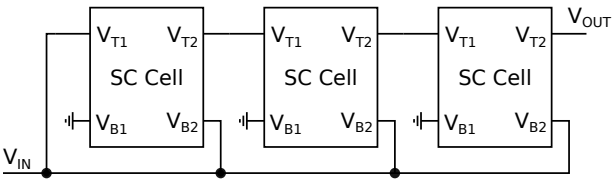


Fig. 2: Three Stage Dickson configuration using four terminal devices.

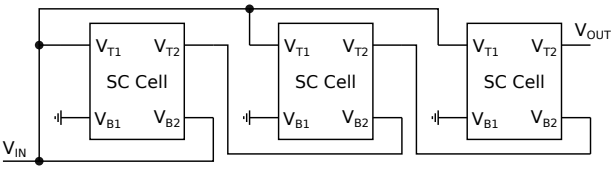


Fig. 3: Three Stage Series Parallel configuration using four terminal devices.

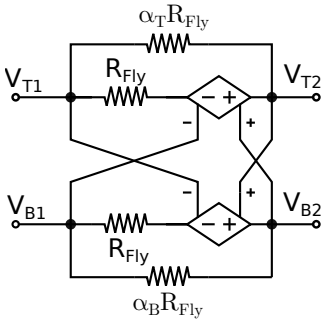


Fig. 4: Equivalent circuit model of the four terminal device operating under SSL conditions.

I. Abstract

This paper constructs a steady state model of the continuous conversion ratio charge pump architecture from first principles, incorporating incomplete charge transfer and finite switch resistance. The model is then verified using a pspice model of the circuit, and the limitations of the assumptions are discussed.

II. Introduction

III. Steady State Model

Most charge pump architectures can be using as a set of flying capacitors cells which switch between 4 unique voltage domains, as in Fig. 1a. The flying capacitor cell can then be abstracted as the four terminal device seen in Fig. 1b. These four terminal devices can then be used to construct various dc-dc converter configurations, such the three stage Dickson in Fig. 2 or the series parallel converter in Fig. 3.

The internal circuit representation of the four terminal model can be seen in Fig. **??**, where $R_{Fly} = \frac{1}{f_{SW} C_{Fly}}$. However, this model neglects the impact of incomplete charge transfer on the output charge delivered, which limits its usefulness.

The effect of incomplete charge transfer on the output and input charge characteristics of a dc-dc converter has been studied []. However, the model studied assumed ideal clock generation. The following analysis incorporates the resistance of clock drivers into the equations for input and output current.

A. Incomplete Charge Transfer

The associated analysis occurs at steady state some assumptions:

- All the capacitors and resistors used in the analysis are linear and time invariant.
- The value of $\alpha_T + \alpha_B < 0.1$.

The circuit in Fig.1a, can be represented as Fig. **??** in its first phase, with Fig. **??** representing its second phase. The voltage at the top and bottom plates are labeled V_{TP} and V_{BP} respectively, while V_{TP1}, would specify the top plate voltage in the first phase.

The first order approximation of the voltage at V_{TP1} is,

$$V_{TP1}(t) = \exp\left(\frac{-t}{\tau}\right) V_{TP1}^{i} + \left(1 - \exp\left(\frac{-t}{\tau}\right)\right) V_{T1}, \tag{1}$$

where τ is,

$$\tau = 2R_{ON}C_{Fly}\left(1 + \frac{\alpha_B + \alpha_T}{2}\right), \tag{2}$$

and V_{TP1}^{i} is the initial value of V_{TP1} at the start of the first phase. The final value of V_{TP1} can be evaluated at $t = \frac{T_{SW}}{2}$, as phase 1 occupies half the period,

$$V_{TP1}^{f} = \exp\left(\tfrac{-T_{SW}}{2\tau}\right) V_{TP1}^{i} + \left(1 - \exp\left(\tfrac{-T_{SW}}{2\tau}\right)\right) V_{T1}. \tag{3}$$

Finally, a substitution can be made, relating to the exponential decay at the end of the time step,

$$A = \exp\left(-\tfrac{T_{SW}}{2\tau}\right) = \exp\left(\tfrac{T_{SW}}{2R_{ON}C_{Fly}(2+\alpha_B+\alpha_T)}\right), \tag{4}$$

which can be used to create a simplified expression for V_{TP1}^{f},

$$V_{TP1}^{f} = AV_{TP1}^{i} + (1 - A)V_{T1}. \tag{5}$$

A similar procedure can then be repeated for the other nodal voltages,

$$V_{BP1}^{f} = AV_{TP1}^{i} + (1 - A)V_{B1}, \tag{6}$$

$$V_{TP2}^{f} = AV_{TP2}^{i} + (1 - A)V_{T2}, \tag{7}$$

$$V_{BP2}^{f} = AV_{BP2}^{i} + (1 - A)V_{B2}. \tag{8}$$

The initial conditions of C_{Fly} at the start of each phase can be acquired using the voltage stored on the capacitor. The voltage stored on the capacitor at the end of any phase is $V_{TPx} - V_{BPx}$, where x is the phase. Using the voltage on the capacitor, the initial conditions can be constructed,

$$V_{TP1}^{i} = \tfrac{V_{TP2}^{f} - V_{BP2}^{f} + V_{T1} + V_{B1}}{2}, \tag{9}$$

$$V_{BP1}^{i} = \tfrac{V_{BP2}^{f} - V_{TP2}^{f} + V_{B1} + V_{T1}}{2}, \tag{10}$$

$$V_{TP2}^{i} = \tfrac{V_{TP1}^{f} - V_{BP1}^{f} + V_{T2} + V_{B2}}{2}, \tag{11}$$

$$V_{BP2}^{i} = \tfrac{V_{BP1}^{f} - V_{TP1}^{f} + V_{T2} + V_{B2}}{2}. \tag{12}$$

Using the equations for the initial conditions and the final voltages, the final voltages can be solved,

$$V_{TP1}^{f} = V_{T1} + \Delta V, \tag{13}$$

$$V_{BP1}^{f} = V_{B1} - \Delta V, \tag{14}$$

$$V_{TP2}^{f} = V_{T2} - \Delta V, \tag{15}$$

and

$$V_{BP2}^{f} = V_{B2} + \Delta V \tag{16}$$

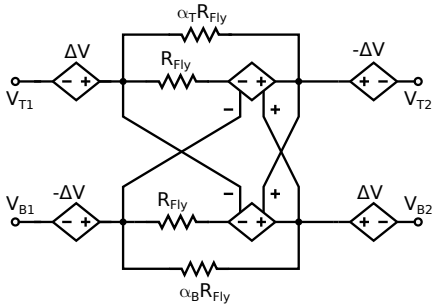


Fig. 5: Four terminal device model incorporating switch resistance.

where

$$\Delta V = \frac{A(V_{B1} - V_{T1} - V_{B2} + V_{T2})}{2(A + 1)}. \tag{17}$$

This can then be used to generate the circuit model seen in Fig. 5, which will incorporate the effects of incomplete charge transfer.

B. Leakage Effects

The leakage effects associated with the transistors are modelled using theory from the [] transistor models. The testing is performed in pspice, using the PTM to simulate the transistors used.