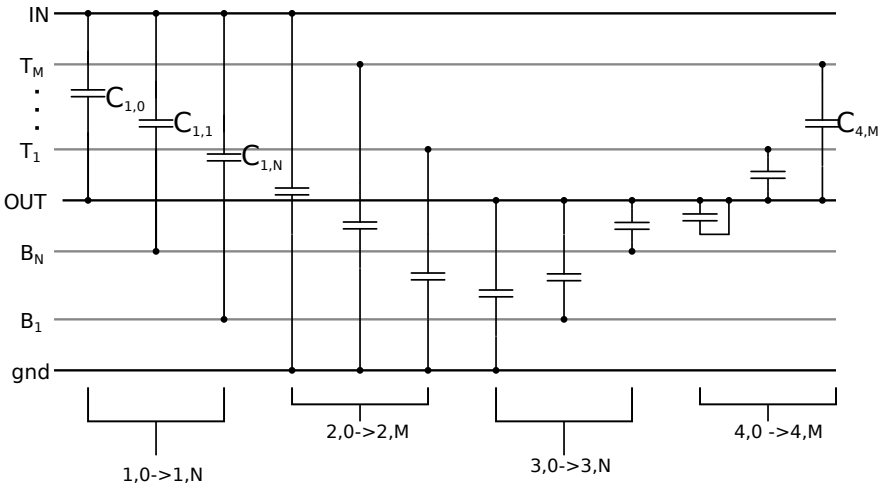


Figure 1: Circuit diagram illustrating the various connections made by the flying capacitors for the continuous ratio.

1 Steady State Model

The circuit to be analyzed is the continuous conversion ratio circuit as seen in [1], which can be seen in Fig. 1. The various steps are numbered along with their associated capacitors in Fig. 1, and will be used further in the analysis. The circuit diagram corresponding to a single flying capacitor and its switches (also referred to as a "core") can be seen in Fig. 2. The initial analysis and modeling is performed under the following assumptions,

- All the capacitors are linear.
- The top and bottom plate parasitic capacitance's have minimal impact on the transient and steady state characteristics of the converter, and are neglected from the analysis.
- All the flying capacitors are equally sized with capacitance C_{Fly}, where $C_{Fly} = C_{1,0} = C_{1,1} = C_{2,0} = C_{2,M}...$
- The switches for the intermediary nodes, $S_{T1}, S_{T2}, S_{TM}, S_{B1}, S_{BN}, etc$, all have an equivalent resistance R_{ON}. The resistance of the switches which connect to the positive and negative rails is 0 ($S_{T+}, S_{T-}, S_{B+}, S_{B-}$).

1.1 Charge Transfer Analysis

The operation of the converter is as follows, each capacitor iterates from steps (1,0)→(4,M) sequentially. There is always a connection to either 0, V_{IN} or V_{OUT} through one of the large interconnection switches, which act as shorts due to their 0Ω resistance. The other connection to the intermediary voltage domains occurs through a switch with a resistance R_{ON}, where the core voltage begins to equalize with the new voltage domain. An example circuit can be seen in Fig. 3a, which is electrically equivalent to Fig. 3b.

The circuit diagram in Fig. 3b, can be used to calculate the transient response of the circuit over each time step. As both the flying capacitance and resistance of each core is identical, the voltage at the intermediary node (B_N) is constant over the time step. This is a result of the symmetry in impedance on either side of the node. The resulting RC time constant will be referred to as τ, where

$$\tau = R_{ON} C_{Fly}. \tag{1}$$

This time constant can be used to describe the change in voltage with respect to time, as the capacitors connect to different voltage domains. Take the existing example as in Fig. 3b, the top plate voltages are

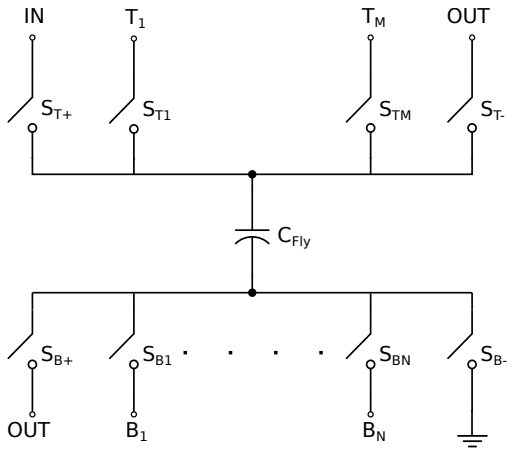
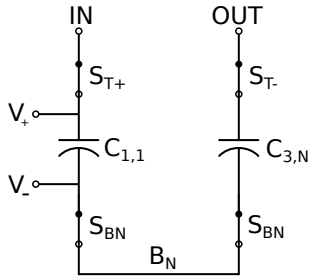
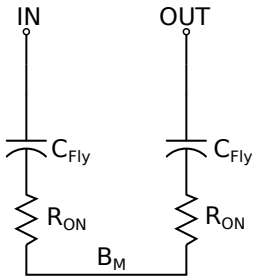


Figure 2: Circuit diagram illustrating the top and bottom connections of a single flying capacitor.



(a) Circuit configuration including switches and flying capacitors.



(b) Equivalent circuit with values.

Figure 3: Example circuit diagrams showing the connection to B_1.

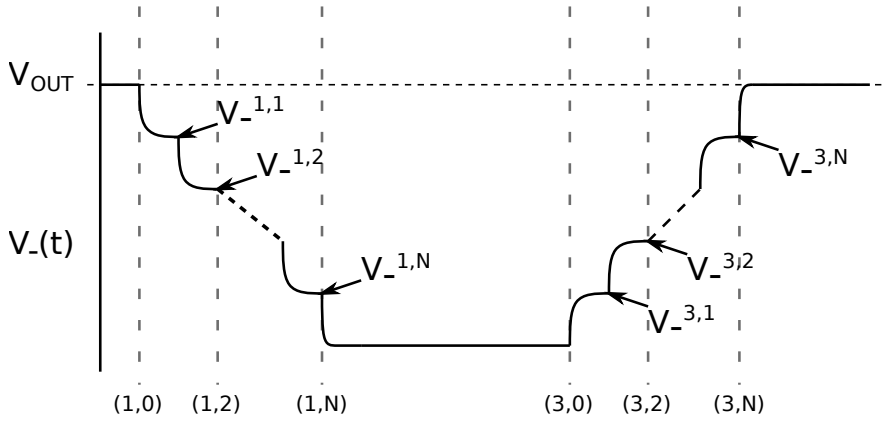


Figure 4: Illustration of $V_{-}(t)$ for various time steps over the period, where V_{-} is the bottom plate of the capacitor, as in 3a.

known, while the bottom plate voltage of $C_{1,1}$ ($V_{1,1}^{-}$) can be calculated as,

$$V_{-}^{1,1}(t) = V_{OUT} \exp\left(\frac{-t}{\tau}\right) + V_{BN}\left(1 - \exp\left(\frac{-t}{\tau}\right)\right), \tag{2}$$

where t is the time after the start of the step. More generally, the top and bottom plate voltages can be described as,

$$V_C[n] = V_C[n-1] \exp\left(\frac{-t}{\tau}\right) + V_{int}\left(1 - \exp\left(\frac{-t}{\tau}\right)\right), \tag{3}$$

where the voltage at $V_C[n-1]$ is the voltage at the end of previous step, while V_{int} is the voltage of the intermediary node (V_{T1}, V_{TM}, V_{B1}, etc) which the capacitor is connected to. Next, the duration of each time step can be incorporated into the analysis, using the switching frequency (f_{SW}). A substitution can then be made to simplify the analysis, where

$$A = 1 - \exp\left(\frac{-1}{\tau f_{SW}}\right), \tag{4}$$

which can be substituted into (3) for example

$$V_C[n] = V_C[n-1]A + V_{int}(1-A), \tag{5}$$

which can then be used to express the bottom plate voltage as a series of multiplications. The bottom plate voltage for steps (1,1)→(1,N) is illustrated in Fig. 4, and can be described as a sequence of transitions, where

$$\begin{aligned} V_{-}^{1,1} &= V_{OUT}(1-A) + AV_{BN}, \\ V_{-}^{1,2} &= V_{-}^{1,1}(1-A) + AV_{BN-1}, \\ &\vdots \\ V_{-}^{1,N} &= V_{-}^{1,N-1}(1-A) + AV_{B1}. \end{aligned} \tag{6}$$

Using this, a matrix can be constructed to describe the bottom plate voltages,

$$\begin{aligned} \begin{bmatrix} V_{-}^{1,1} \\ V_{-}^{1,2} \\ \vdots \\ V_{-}^{1,N-1} \\ V_{-}^{1,N} \end{bmatrix} = &\begin{bmatrix} A & 0 & \dots & 0 & 0 \\ A(1-A) & A & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A(1-A)^{N-2} & A(1-A)^{N-3} & \dots & A & 0 \\ A(1-A)^{N-1} & A(1-A)^{N-2} & \dots & A(1-A) & A \end{bmatrix} \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix} \\ &+ V_{OUT} \begin{bmatrix} (1-A) \\ (1-A)^2 \\ \vdots \\ (1-A)^{N-1} \\ (1-A)^N \end{bmatrix}. \end{aligned} \tag{7}$$

Using a similar method, a matrix can be constructed for the bottom plate voltages in steps (3,N)→(3,1),

$$\begin{bmatrix} V_{-}^{3,N} \\ V_{-}^{3,N-1} \\ \vdots \\ V_{-}^{3,2} \\ V_{-}^{3,1} \end{bmatrix} = \begin{bmatrix} A & A(1-A) & \dots & A(1-A)^{N-2} & A(1-A)^{N-1} \\ 0 & A & \dots & A(1-A)^{N-3} & A(1-A)^{N-2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & A & A(1-A) \\ 0 & 0 & \dots & 0 & A \end{bmatrix} \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix}. \tag{8}$$

Next, a charge balance analysis can be used to calculate the current moving into and out of nodes $B_1 \rightarrow B_N$ on each time step. In both cases, the charge into the node can be calculated using the change in voltage on the capacitor,

$$Q_{Bx} = C_{Fly}(V_{-}^{1,x} - V_{-}^{1,x-1}), \tag{9}$$

where x is the index from 1 to N. This can be used to construct matrices for both steps $(1,1) \rightarrow (1,N)$.

$$\begin{bmatrix} Q_{BN} \\ Q_{BN-1} \\ \vdots \\ Q_{B2} \\ Q_{B1} \end{bmatrix} = \begin{bmatrix} -A & 0 & \dots & 0 & 0 \\ A^2 & -A & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A^2(1-A)^{N-3} & A^2(1-A)^{N-4} & \dots & -A & 0 \\ A^2(1-A)^{N-2} & A^2(1-A)^{N-3} & \dots & A^2 & -A \end{bmatrix} \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix} C + CV_{DD} \begin{bmatrix} A \\ A(1-A) \\ \vdots \\ A(1-A)^{N-2} \\ A(1-A)^{N-1} \end{bmatrix}, \quad (10)$$

and $(3,1) \rightarrow (3,N)$

$$\begin{bmatrix} Q_{BN} \\ Q_{BN-1} \\ \vdots \\ Q_{B2} \\ Q_{B1} \end{bmatrix} = \begin{bmatrix} -A & A^2 & \dots & A^2(1-A)^{N-3} & A^2(1-A)^{N-2} \\ 0 & -A & \dots & A^2(1-A)^{N-4} & A^2(1-A)^{N-3} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & -A & A^2 \\ 0 & 0 & \dots & 0 & -A \end{bmatrix} \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix}. \quad (11)$$

The charge out of the nodes can then be added, and summed to zero, as the voltage at the nodes does not change at steady state. The resulting matrix is,

$$\begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} = CM \begin{bmatrix} V_{B1} \\ V_{B2} \\ \vdots \\ V_{BM-1} \\ V_{BM} \end{bmatrix} + CV_{DD} \begin{bmatrix} A \\ A(1-A) \\ \vdots \\ A(1-A)^{N-2} \\ A(1-A)^{N-1} \end{bmatrix}. \quad (12)$$

where

$$M = \begin{bmatrix} -2A & A^2 & \dots & A^2(1-A)^{N-3} & A^2(1-A)^{N-2} \\ A^2 & -2A & \dots & A^2(1-A)^{N-4} & A^2(1-A)^{N-3} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A^2(1-A)^{N-3} & A^2(1-A)^{N-4} & \dots & -2A & A^2 \\ A^2(1-A)^{N-2} & A^2(1-A)^{N-3} & \dots & A^2 & -2A \end{bmatrix}. \quad (13)$$

The solved expression for voltage levels $V_{B1} \rightarrow V_{BN}$ is,

$$V_{Bx} = V_{OUT} \frac{A(x-1)+1}{A(N-1)+2}, \quad (14)$$

a similar procedure can be followed to acquire the voltage levels for $V_{T1} \rightarrow V_{TN}$,

$$V_{Tx} = V_{OUT} + (V_{IN} - V_{OUT}) \frac{A(x-1)+1}{A(N-1)+2}. \quad (15)$$

These can now be substituted into (7) for example to acquire the solved expressions for V_{-} for steps (1,1) $\rightarrow$ (1,N). The solved expressions for the top and bottom plate voltages are:

$$V_{-}^{1,x} = \frac{((N-x-1)A+2)V_{OUT}}{A(N-1)+2}, \quad (16)$$

$$V_{+}^{2,x} = V_{OUT} + (V_{IN} - V_{OUT}) \frac{(M-x-1)A+2}{A(M-1)+2}, \quad (17)$$

$$V_{-}^{3,x} = \frac{xAV_{OUT}}{A(N-1)+2}, \quad (18)$$

$$V_{+}^{4,x} = V_{OUT} + \frac{xA(V_{IN} - V_{OUT})}{A(N-1)+2}. \quad (19)$$

In order to calculate the input and output currents of the converter, a charge balance method will be used. The charge delivered to the output can be observed from Fig. 1, where it occurs on steps (1,0), (3,0)→(3,N) and (4,1)→(4,M). The charge transferred on the steps is as follows,

$$Q_{3,0} = C_{Fly}(V_+^{2,M} - V_{OUT}), \tag{20}$$

$$Q_{3,1} \rightarrow Q_{3,N} = C_{Fly}V_{3,N}, \tag{21}$$

and

$$Q_{4,1} \rightarrow Q_{1,0} = C_{Fly}(V_{IN} - V_{OUT}), \tag{22}$$

resulting in a total output charge of

$$\begin{aligned} Q_{OUT} &= Q_{3,0} + Q_{3,1} + Q_{4,1} \\ Q_{OUT} &= C_{Fly}\frac{(2-A)(V_{IN} - V_{OUT})}{A(M-1)+2} + C_{Fly}\frac{NAV_{OUT}}{A(N-1)+2} + C_{Fly}(V_{IN} - V_{OUT}) \\ Q_{OUT} &= C_{Fly}\left(\frac{(A(M-2)+4)(V_{IN} - V_{OUT})}{A(M-1)+2} + \frac{NAV_{OUT}}{A(N-1)+2}\right). \end{aligned} \tag{23}$$

A similar method can be used to acquire the input charge, occurring over steps (1,0) → (2,0),

$$\begin{aligned} Q_{IN} &= C_{Fly}\left(V_{IN} - V_+^{4,M} + V_{OUT}\right) \\ Q_{IN} &= C_{Fly}\left(V_{IN} - V_{OUT} - \frac{MA(V_{IN} - V_{OUT})}{A(M-1)+2} + V_{OUT}\right) \\ Q_{IN} &= C_{Fly}\frac{MAV_{OUT} + (2-A)V_{IN}}{A(M-1)+2} \end{aligned} \tag{24}$$

The input and output charge can then be used in combination with the switching frequency to acquire the input and output power,

$$P_{IN} = V_{IN}f_{SW}C_{Fly}\frac{MAV_{OUT} + (2-A)V_{IN}}{A(M-1)+2}, \tag{25}$$

$$P_{OUT} = V_{OUT}f_{SW}C_{Fly}\left(\frac{(2-A)(V_{IN} - V_{OUT})}{A(M-1)+2} + \frac{NAV_{OUT}}{A(N-1)+2} + (V_{IN} - V_{OUT})\right), \tag{26}$$

finally, an expression for the conversion efficiency (η) can be constructed,

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}}{V_{IN}}\frac{(A(N-1)+2)(A(M-2)+4)(V_{IN} - V_{OUT}) + (A(M-1)+2)NAV_{OUT}}{(A(N-1)+2)(MAV_{OUT} + (2-A)V_{IN})}. \tag{27}$$

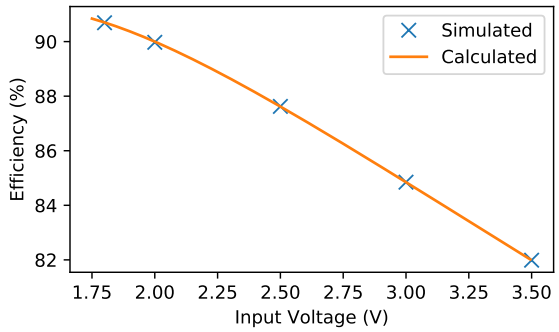
The resulting calculation for the efficiency is then graphed and compared to some simulation results with ideal components, which can be seen in Fig. 5a and 5b. Fig 5a plots the efficiency in comparison to input voltage, while Fig. 5b plots efficiency in comparison to A.

2 Steady State Model Usefulness

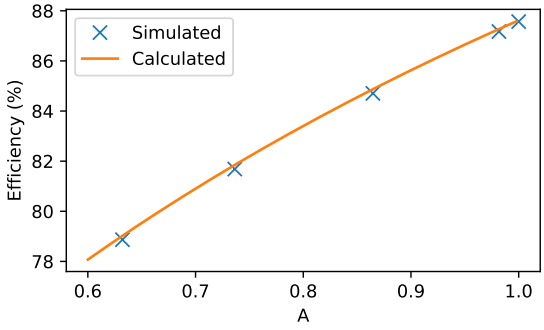
The usefulness of the model is going to be dependent on how accurate the underlying assumptions are, these will now be discussed.

2.1 Flying Capacitor Linearity

Provided the flying capacitors are made from MIM (Metal Insulator Metal) or MOM (Metal Oxide Metal) capacitors, the assumption of linearity should hold. Alternately, if the capacitors are MOS based, then there is likely some non-linearity which will impact the accuracy of the design. It should be noted that many of the techniques used to reduce parasitic capacitance have the additional impact of improving capacitor



(a) Comparison with constant $A = 1$ and $V_{OUT} = 1$.



(b) Comparison with constant $V_{IN} = 2.5$ and $V_{OUT} = 1$.

Figure 5: Verification of the calculated efficiency. The simulations were setup to conform to the model assumptions.

linearity [], []. Regardless, there is a need to do additional analysis to assess the impact of non-linearity on the model, and to incorporate that into the model.

A simple first order approximation would be to assess the total amount of charge required to drive the capacitor from $0 \rightarrow V_{IN}$, as this dictates the total change in charge on the capacitor. This can then be used to approximate how the value of C_{Fly} changes as a function of V_{IN}, which will impact the power density.

2.2 Top and Bottom Plate Parasitic Capacitance

Top and bottom plate parasitic capacitances can be expressed as C_{α_T}, and $C_{\alpha B}$, as seen in Fig. **??**. They are related to the flying capacitance by the factor αT and αB, where,

$$C_{\alpha T} = C_{Fly}\alpha_T, \tag{28}$$

and

$$C_{\alpha B} = C_{Fly}\alpha_B. \tag{29}$$

The effect of $C_{\alpha T}$ is increased current flowing from the input to output. It delivers charge to the output on step (3,0), as $C_{\alpha T}$ discharges from $V_+^{2,M} \rightarrow V_{OUT}$. This results in a total amount of charge,

$$Q_{\alpha T} = C_{\alpha T}(V_+^{2,M} - V_{OUT}) = C_{Fly}\alpha_T \frac{(2-A)(V_{IN} - V_{OUT})}{A(M-1)+2}, \tag{30}$$

being delivered to the output. Similarly, on step (1,0) $C_{\alpha T}$ draws charge from the input as it is charged from $(V_+^{4,M})$ to V_{IN},

$$Q_{\alpha_T} = C_{\alpha T}(V_{IN} - V_+^{4,M}) = C_{Fly}\alpha_T \frac{(2-A)(V_{IN} - V_{OUT})}{A(M-1)+2}. \tag{31}$$

The effect of $C_{\alpha B}$ is a decrease in total output current. Consider step (4,0), where the bottom plate is charged from $V_-^{3,N}$ to V_{OUT}, requiring charge,

$$Q_{\alpha B} = C_{\alpha B}(V_{OUT} - V_-^{3,N}) = C_{Fly}\alpha_B \frac{V_{OUT}(2-A)}{A(N-1)+2}. \tag{32}$$

The new expressions for the input and output charge are,

$$\begin{aligned} Q_{IN} &= C_{Fly}\frac{MAV_{OUT} + (2-A)V_{IN}}{A(M-1)+2} - C_{Fly}\alpha_T\frac{(2-A)(V_{IN}-V_{OUT})}{A(M-1)+2} \\ &= C_{Fly}\frac{(MA + \alpha_T(2-A))\,V_{OUT} + (1-\alpha_T)(2-A)V_{IN}}{A(M-1)+2}, \end{aligned} \tag{33}$$

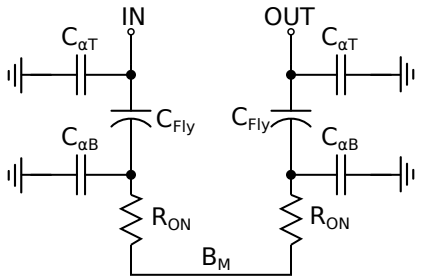


Figure 6: Equivalent circuit including parasitic capacitances.

and

$$\begin{aligned} Q_{OUT} &= C_{Fly}\left(\frac{(A(M-2)+4)(V_{IN}-V_{OUT})}{A(M-1)+2}+\frac{NAV_{OUT}}{A(N-1)+2}\right) \\ &+ C_{Fly}\alpha_T\frac{(2-A)(V_{IN}-V_{OUT})}{A(M-1)+2} - C_{Fly}\alpha_B\frac{V_{OUT}(2-A)}{A(N-1)+2} \\ &= C_{Fly}\left(\frac{(A(M-2)+4+\alpha_T(2-A))(V_{IN}-V_{OUT})}{A(M-1)+2}+\frac{(NA-\alpha_B(2-A))\,V_{OUT}}{A(N-1)+2}\right). \end{aligned} \tag{34}$$

2.2.1 Impact on Time Constant

The impact of $C_{\alpha T}$ and $C_{\alpha B}$ is negligible for values of $\alpha_B \,\&\, \alpha_T < 0.1$, and should be ignored in these cases. Otherwise the following analysis is relevant.

An additional impact of the top and bottom plate parasitic capacitances is a change in the time constant of the circuit. Consider the circuit in Fig. 6, as previous, the voltages at the intermediary nodes are constant with respect to time over a single step. However, the equivalent capacitance is now the result of C_{Fly} in parallel with $C_{Fly}\alpha_T$, resulting in a new calculation for A,

$$A = 1 - \exp\left(\frac{T_{EQ}}{R_{ON}C_{Fly}(1+\alpha_T)}\right). \tag{35}$$

This may result in different time constant steps when stepping the top plate voltage and the bottom plate voltage, if α_B != α_T. If α_B != α_T, then an equation for A which averages the difference between top and bottom plate equalization times,

$$A = 1 - \exp\left(\frac{2T_{EQ}}{R_{ON}C_{Fly}(2+\alpha_T+\alpha_B)}\right). \tag{36}$$

2.3 Flying Capacitor Mismatch

Given that the designer is choosing to equally size the flying capacitors, the only probable reason for mismatch is a result of process variation. This is going to be highly dependent on the technology node and a number of factors, however most of these should be negligible, given the sheer size of the flying capacitors.

2.4 Switch Resistance

The model used assumes constant switch resistance, however the switches are implemented using real transistors. The resistance model for long channel NMOS transistors is,

$$R_{ON} = \frac{L}{WC_{OX}\mu_N V_{GS}}, \tag{37}$$

where L and W are the channel length and width respectively, C_{OX} is the capacitance density of the oxide layer, μ_N is the carrier mobility, and V_{GS} is the gate voltage relative to the source. This would make the

R_{ON} dependent on the bottom plate voltage of C_{Fly} (provided V_G is a constant digital voltage) as V_S is going to be determined by the bottom plate voltage. However, if the relative voltage rail configuration is used, as proposed in [1], this can be avoided, and the switches can be modeled as having constant resistance R_{SW}. This techniques is used for the PMOS as well again, resulting in a near constant R_{SW}.

The next portion of this assumption is that switches S_{B+}, S_{B-}, S_{T+} and S_{T-} have a resistance of $0\,\Omega$. Clearly, this is not possible, as transistors always have some finite resistance. However, for maximal power density and performance, these transistors should be sized far larger than the other transistors. The motivation behind this design choice is that these transistors switch off and on at a far lower frequency than the other transistors. For example S_{B+} is on for $M+1$ cycles, meaning that it should be sized a factor $\sqrt{M+1}$ larger than the other PMOS transistors.

This will result in it having a resistance of, $R_{SB+} = \frac{R_{SW}}{\sqrt{M+1}}$, which will change the time constant of the circuit. Additionally, consider steps $(1,0)$, $(2,0)$, $(3,0)$, $(4,0)$, in these cases, it was previously assumed that there was full equalization occurring, as a result of the short circuits. The resulting time constant over these periods will be,

$$\tau = \frac{T_{EQ}\sqrt{N+1}\sqrt{M+1}}{(\sqrt{N+1}+\sqrt{M+1})R_{ON}C_{Ffly}}, \tag{38}$$

however, depending on how large N and M this assumption should remain a reasonable approximation. The only change required is that,

$$A = 1 - \frac{2T_{EQ}}{\left(2+\frac{1}{\sqrt{M+1}}+\frac{1}{\sqrt{N+1}}\right)R_{ON}C_{Fly}}, \tag{39}$$

will substitute the prior value of A.

References

[1] N. Butzen and M. Steyaert, "Design of single-topology continuously scalable-conversion-ratio switched-capacitor dcdc converters," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 4, pp. 1039–1047, 2019.