

# A Four Terminal Charge Pump Model Incorporating Device Leakage Effects

Mark Lipski

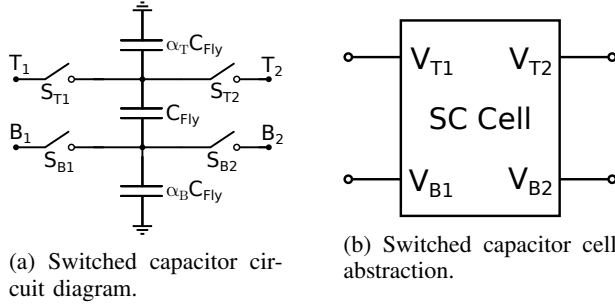


Fig. 1: Four terminal circuit, and equivalent block level abstraction.

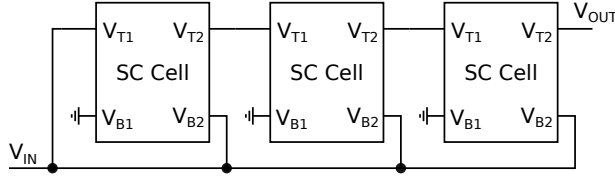


Fig. 2: Three Stage Dickson configuration using four terminal devices.

## I. ABSTRACT

This paper constructs a steady state model of the continuous conversion ratio charge pump architecture from first principles, incorporating incomplete charge transfer and finite switch resistance. The model is then verified using a pspice model of the circuit, and the limitations of the assumptions are discussed.

## II. INTRODUCTION

### III. STEADY STATE MODEL

The foundational building block of most Switched Capacitor Power Converter (SCPC) architectures is the circuit in Fig. 1a, where the flying capacitor connects to 4 unique voltage domains. This flying capacitor cell can then be abstracted as the four terminal device seen in Fig. 1b. The SC cell can then be used to construct various dc-dc converter configurations, such as the three stage Dickson in Fig. 2 or the series parallel converter in Fig. 3.

A steady state circuit representation of the four terminal model can be seen in Fig. 4, where  $R_{Fly} = \frac{1}{f_{sw} C_{Fly}}$ .

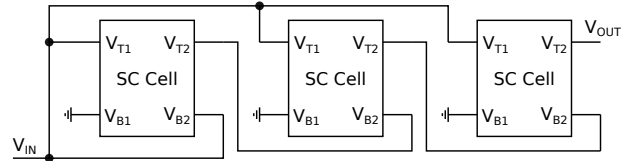


Fig. 3: Three Stage Series Parallel configuration using four terminal devices.

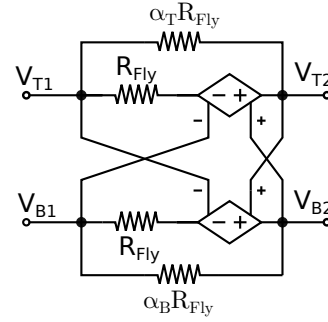


Fig. 4: Equivalent circuit model of the four terminal device operating under SSL conditions.

However, this model neglects the impact switch resistance has on the equivalent resistance of the cell.

The effect of incomplete charge transfer on the output and input charge characteristics of a dc-dc converter has been studied [1]. However, the model studied assumed ideal clock generation. The following analysis incorporates the resistance of clock drivers into the equations for input and output current.

#### A. Incomplete Charge Transfer

The associated analysis occurs at steady state with some assumptions:

- All the capacitors and resistors used in the analysis are linear and time invariant.
- The value of  $\alpha_T + \alpha_B < 0.1$ .

The circuit in Fig. 1a, can be represented as Fig. 5a in its first phase, with Fig. 5b representing its second phase. The voltage at the top and bottom plates of the capacitor are labeled  $V_{TP}$  and  $V_{BP}$ ,  $V_{TP1}$  for example, would specify top plate voltage in the first phase.

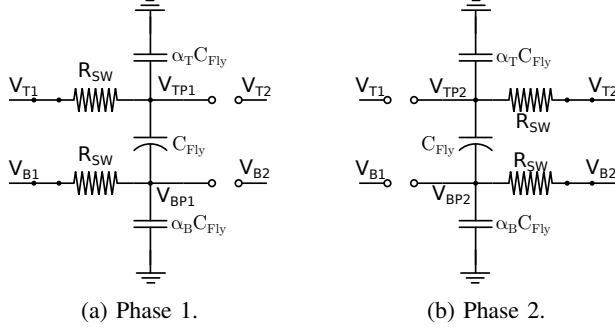


Fig. 5: Equivalent representation of 1a, with switch resistance  $R_{SW}$ , for both of its phases.

The first order approximation of  $V_{TP1}$  is,

$$V_{TP1}(t) = \exp\left(\frac{-t}{\tau}\right) V_{TP1}^i + \left(1 - \exp\left(\frac{-t}{\tau}\right)\right) V_{T1}, \quad (1)$$

where  $\tau$  is the first order time constant of the circuit, and  $V_{TP1}^i$  is the initial value of  $V_{TP1}$  at the start of the first phase.

In order to acquire the value of  $\tau$ , a frequency domain analysis of the structure in Fig. 5a can be performed. To simplify the analysis, the value of  $V_{B1} = 0$ , and the initial conditions on the capacitors are ignored, and the structure is analyzed with respect to  $V_{T1}$ , the resulting nodal equation at  $V_{TP1}$  is

$$\frac{V_{TP1} - V_{T1}}{R_{SW}} + s\alpha_T C V_{TP1} + sC(V_{TP1} - V_{BP1}) = 0, \quad (2)$$

similarly, a nodal analysis at  $V_{BP1}$  yields,

$$\frac{V_{BP1}}{R_{SW}} + s\alpha_B C V_{BP1} + sC(V_{BP1} - V_{TP1}) = 0. \quad (3)$$

These two nodal equations can then be used to solve for the dominant pole of the circuit, yielding

$$V_{TP1} = \frac{V_{T1}(sC(\alpha_B + 1))}{s^2 C^2 R^2 (\alpha_B + \alpha_T + \alpha_B \alpha_T) + sRC(2 + \alpha_B + \alpha_T) + 1}, \quad (4)$$

however, if it is assumed that  $\alpha_T = \alpha_B$  then the simplified expression is,

$$V_{TP1} = \frac{V_{T1}(sC(\alpha_B + 1))}{(s\alpha_B CR + 1)(sCR(2 + \alpha_B) + 1)}. \quad (5)$$

The resulting first order time constant is then,

$$\tau = R_{ON} C_{Fly} (2 + \alpha_B), \quad (6)$$

The final value of  $V_{TP1}$  can be evaluated at  $t = \frac{T_{SW}}{2}$ , as phase 1 occupies approximately half the period,

$$V_{TP1}^f = \exp\left(\frac{-T_{SW}}{2\tau}\right) V_{TP1}^i + \left(1 - \exp\left(\frac{-T_{SW}}{2\tau}\right)\right) V_{T1}. \quad (7)$$

Finally, a substitution can be made, relating to the exponential decay at the end of the time step,

$$A = \exp\left(-\frac{T_{SW}}{2\tau}\right) = \exp\left(\frac{-T_{SW}}{2R_{ON} C_{Fly} (2 + \alpha_B)}\right), \quad (8)$$

which can be used to create a simplified expression for  $V_{TP1}^f$ ,

$$V_{TP1}^f = AV_{TP1}^i + (1 - A)V_{T1}. \quad (9)$$

A similar procedure can then be repeated for the other nodal voltages,

$$V_{BP1}^f = AV_{TP1}^i + (1 - A)V_{B1}, \quad (10)$$

$$V_{TP2}^f = AV_{TP2}^i + (1 - A)V_{T2}, \quad (11)$$

$$V_{BP2}^f = AV_{BP2}^i + (1 - A)V_{B2}. \quad (12)$$

The initial conditions of  $C_{Fly}$  at the start of each phase can be acquired using the voltage stored on the capacitor. The voltage stored on the capacitor at the end of any phase is  $V_{TPx} - V_{BPx}$ , where  $x$  is the phase. Using the voltage on the capacitor, the initial conditions can be constructed,

$$V_{TP1}^i = \frac{V_{TP2}^f - V_{BP2}^f + V_{T1} + V_{B1}}{2}, \quad (13)$$

$$V_{BP1}^i = \frac{V_{BP2}^f - V_{TP2}^f + V_{B1} + V_{T1}}{2}, \quad (14)$$

$$V_{TP2}^i = \frac{V_{TP1}^f - V_{BP1}^f + V_{T2} + V_{B2}}{2}, \quad (15)$$

$$V_{BP2}^i = \frac{V_{BP1}^f - V_{TP1}^f + V_{T2} + V_{B2}}{2}. \quad (16)$$

Using the equations for the initial conditions and the final voltages, the final voltages can be solved,

$$V_{TP1}^f = V_{T1} + \Delta V, \quad (17)$$

$$V_{BP1}^f = V_{B1} - \Delta V, \quad (18)$$

$$V_{TP2}^f = V_{T2} - \Delta V, \quad (19)$$

and

$$V_{BP2}^f = V_{B2} + \Delta V \quad (20)$$

where

$$\Delta V = \frac{A(V_{B1} - V_{T1} - V_{B2} + V_{T2})}{2(A + 1)}. \quad (21)$$

This can then be used to generate the circuit model seen in Fig. 6, which will incorporate the effects of incomplete charge transfer.

This can then be verified using an ideal model of the circuit, using both a single SC cell, and in more complex configurations, such as the Dickson and series parallel. The resulting comparison can be seen in Fig. ??, where the resistance and voltage are held constant, and the frequency is varied.

A second set of tests was run to verify that the impact of  $\alpha_B$  and  $\alpha_T$  was as predicted, which can be seen in Fig. ??.

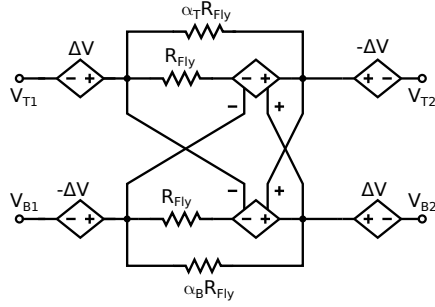


Fig. 6: Four terminal device model incorporating switch resistance.

### B. Leakage Effects

The leakage effects associated with the transistors are modelled using theory from the [] transistor models. The testing is performed in pspice, using the PTM to simulate the transistors used.

### REFERENCES

- [1] T. Tanzawa, "A switch-resistance-aware dickson charge pump model for optimizing clock frequency," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 6, pp. 336–340, 2011.