A Steady State Model for the Continuous Conversion Ratio Charge Pump

Mark Lipski

I. Abstract

This paper constructs a steady state model of the continuous conversion ratio charge pump architecture from first principles, incorporating incomplete charge transfer and finite switch resistance. The model is then verified using a pspice model of the circuit, and the limitations of the assumptions are discussed.

II. Introduction

The rise of IoT has driven the development of various ultra low power, low cost mobile systems. This results in a need for high efficiency, low cost power electronics.

One candidate for addressing many of the needs of industry is the continuous conversion charge pump proposed in [1]. The proposed structure has the benefit of providing a completely variable conversion ratio while maintaining high efficiencies.

While analytical models have been developed for charge pumps which incorporate switch resistance, [2], the structure in [1] requires separate analysis. The following work proposes a steady state model that will incorporate the effects of incomplete charge transfer.

The structure of the paper is as follows, first, a model of the charge pump will be generated. Next, the results of the model are compared to simulations performed using pspice. The results are then discussed, along with the validity of the assumptions.

III. Steady State Model

The circuit to be analyzed is the continuous conversion ratio circuit proposed in [1], seen in Fig. 1.

A. Circuit Operation

The continuous conversion ratio charge pump functions substantially differently from the traditional switched capacitor power converter in its operation. Conceptually, the flying capacitors are charged by connecting the top plate to V_{IN}, then discharge by connecting to V_{OUT}, delivering current to the output.

This process is made efficient using adiabatic charging methods similar to those in [3], [4], in which capacitors are gradually charged and discharged. The charging occurs over numerous steps, where the top plate connects to intermediary voltages between V_{OUT} and V_{IN}, labeled ($T_1 \rightarrow T_M$), with M indicating the number of intermediary levels. The bottom plate intermediary nodes are labeled B_1 to B_N.

The various steps are numbered along with their associated capacitors in Fig. 1, in steps (1,0 $\rightarrow$ 1,N) the bottom plate voltage is decreased, supplying nodes ($B_1 \rightarrow B_N$) with current. This current is then used to increase the bottom plate voltage over steps (3,1 $\rightarrow$ 3,N), simultaneously delivering current to the output. A similar process occurs with the top plate on steps (2,1 $\rightarrow$ 2,M) and (4,1 $\rightarrow$ 4,M) where current is drawn from the input.

The circuit diagram corresponding to a single flying capacitor and its switches (also referred to as a "core") can be seen in Fig. 2. The analysis and modeling is performed under the following assumptions,

- All the capacitors are linear.
- The top and bottom plate parasitic capacitance's have minimal impact on the transient and steady state characteristics of the converter, and are neglected from the analysis.
- All the flying capacitors are equally sized with capacitance C_{Fly}, where $C_{Fly} = C_{1,0} = C_{1,1} = C_{2,0} = C_{2,M}...$
- The input and output voltages V_{IN}, and V_{OUT} are constant and ideal.
- The switches for the intermediary nodes, S_{T1}, S_{T2}, $S_{TM}, S_{B1}, S_{BN}, etc$, all have an equivalent resistance R_{ON}. The resistance of the switches which connect to the positive and negative rails ($S_{T+}, S_{T-}, S_{B+}, S_{B-}$) is 0 Ω.

B. Charge Transfer Analysis

The operation of the converter involves each capacitor iterating from steps (1,0)$\rightarrow$(4,M) sequentially. There is always a connection on the top or bottom plate to either 0 V, V_{IN} or V_{OUT}. Connections to the intermediary voltage domains (those being $B_1 \rightarrow B_N$ and $T_1 \rightarrow T_M$) occur through a switch with a resistance R_{ON}. An example circuit can be seen in Fig. 3a, which is electrically equivalent to Fig. 3b.

The circuit diagram in Fig. 3b can be used to calculate the transient response of the circuit over each time step. Consider node B_N, the impedance of the branches to IN and OUT are identical, this symmetry results in B_N being constant over a single time step. The top and bottom plate voltages of the capacitors can then be

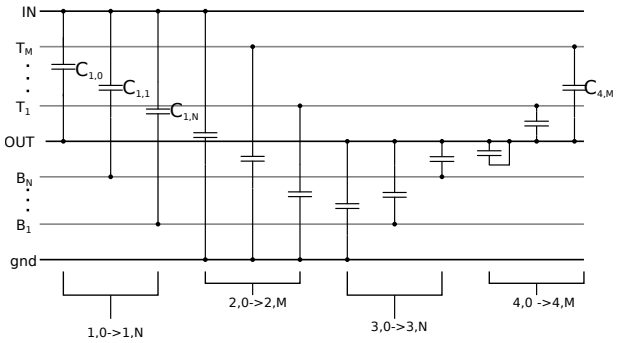


Fig. 1: Circuit diagram illustrating the various connections made by the flying capacitors for the continuous ratio.

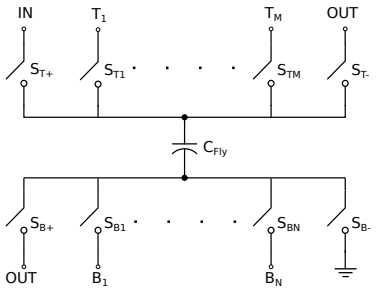
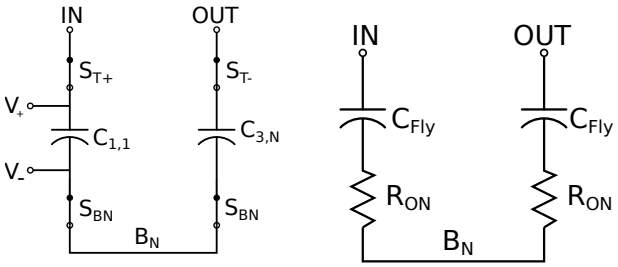


Fig. 2: Circuit diagram illustrating the top and bottom connections of a single flying capacitor.



(a) Circuit configuration including switches and flying capacitors.

(b) Equivalent circuit with values.

Fig. 3: Example circuit diagrams showing the connection to B_N.

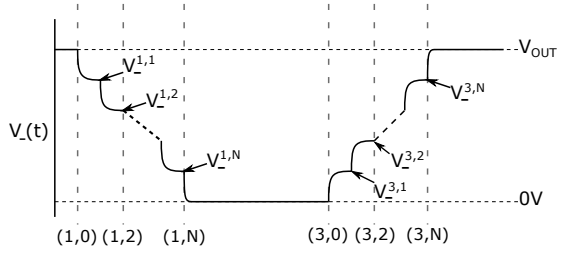


Fig. 4: Illustration of $V_{-}(t)$ for various time steps over the period, where V_{-} is the bottom plate of the capacitor, as in 3a.

described using a single RC time constant (τ), where $\tau = R_{ON}C_{Fly}$. Using Fig. 3b as an example, the top plate voltage of $C_{1,1}$ is known, while the bottom plate voltage ($V_{-}^{1,1}$) can be calculated as,

$$V_{-}^{1,1}(t) = V_{OUT}\exp\left(\frac{-t}{\tau}\right) + V_{BN}\left(1-\exp\left(\frac{-t}{\tau}\right)\right), \tag{1}$$

where t is the time after the start of the step. More generally, the top and bottom plate voltages can be described as,

$$V_C[n] = V_C[n-1]\exp\left(\tfrac{-1}{\tau f_{SW}}\right) + V_{int}\left(1-\exp\left(\tfrac{-t}{\tau f_{SW}}\right)\right), \tag{2}$$

where $V_C[n-1]$ is the voltage at the end of previous step, while V_{int} is the voltage of the intermediary node (V_{T1}, V_{TM}, V_{B1}, etc) which the capacitor is connected to. Next, the duration of each time step can be incorporated into the analysis using the switching frequency (f_{SW}). A substitution can then be made to simplify the analysis, where

$$A = 1-\exp\left(\tfrac{-1}{\tau f_{SW}}\right), \tag{3}$$

which can be substituted into (2) resulting in

$$V_C[n] = V_C[n-1](1-A) + AV_{int}. \tag{4}$$

This can be used to express the bottom plate voltage for steps (1,1)→(1,N), where

$$\begin{aligned} V_{-}^{1,1} &= V_{OUT}(1-A) + AV_{BN}, \\ V_{-}^{1,2} &= V_{-}^{1,1}(1-A) + AV_{BN-1}, \\ &\vdots \\ V_{-}^{1,N} &= V_{-}^{1,N-1}(1-A) + AV_{B1}. \end{aligned} \tag{5}$$

Using this, a matrix can be constructed to describe the bottom plate voltages,

$$\begin{bmatrix} V_{-}^{1,1} \\ V_{-}^{1,2} \\ \vdots \\ V_{-}^{1,N-1} \\ V_{-}^{1,N} \end{bmatrix} = H\begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix} + V_{OUT}\begin{bmatrix} (1-A) \\ (1-A)^2 \\ \vdots \\ (1-A)^{N-1} \\ (1-A)^N \end{bmatrix}, \tag{6}$$

where,

$$H = \begin{bmatrix} A & 0 & \dots & 0 & 0 \\ A(1-A) & A & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A(1-A)^{N-2} & A(1-A)^{N-3} & \dots & A & 0 \\ A(1-A)^{N-1} & A(1-A)^{N-2} & \dots & A(1-A) & A \end{bmatrix}. \tag{7}$$

Using a similar method, a matrix can be constructed for the bottom plate voltages in steps (3,N)→(3,1).

$$\begin{bmatrix} V_{-}^{3,N} \\ V_{-}^{3,N-1} \\ \vdots \\ V_{-}^{3,2} \\ V_{-}^{3,1} \end{bmatrix} = H^T \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix}. \tag{8}$$

To calculate the values of $V_{B1} \rightarrow V_{BN}$, the amount of charge delivered to these nodes on each time step must be known. For steps, (1,1)→(1,N), the charge delivered to Bx is,

$$Q_{Bx} = C_{Fly}(V_{-}^{1,x} - V_{-}^{1,x-1}), \tag{9}$$

where x ranges from 1 to N. A matrix for the charge delivered on steps $(1,1) \rightarrow (1,N)$ can then be constructed using (6) and (9)

$$\begin{bmatrix} Q_{BN} \\ Q_{BN-1} \\ \vdots \\ Q_{B2} \\ Q_{B1} \end{bmatrix} = CG \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix} + CV_{DD} \begin{bmatrix} A \\ A(1-A) \\ \vdots \\ A(1-A)^{N-2} \\ A(1-A)^{N-1} \end{bmatrix}, \tag{10}$$

where

$$G = \begin{bmatrix} -A & 0 & \dots & 0 & 0 \\ A^2 & -A & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A^2(1-A)^{N-3} & A^2(1-A)^{N-4} & \dots & -A & 0 \\ A^2(1-A)^{N-2} & A^2(1-A)^{N-3} & \dots & A^2 & -A \end{bmatrix}. \tag{11}$$

Using a similar procedure, the charge delivered on steps $(3,1) \rightarrow (3,N)$ is,

$$\begin{bmatrix} Q_{BN} \\ Q_{BN-1} \\ \vdots \\ Q_{B2} \\ Q_{B1} \end{bmatrix} = CG^T \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix}. \tag{12}$$

The steady state condition occurs when the net charge into the intermediary nodes is 0. This can be acquired by adding (10) and (12), then equating to zero,

$$\begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} = (G+G^T) \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix} + V_{DD} \begin{bmatrix} A \\ A(1-A) \\ \vdots \\ A(1-A)^{N-2} \\ A(1-A)^{N-1} \end{bmatrix}, \tag{13}$$

solving this expression for $V_{B1} \rightarrow V_{BN}$ yields,

$$V_{Bx} = V_{OUT} \frac{A(x-1)+1}{A(N-1)+2}. \tag{14}$$

A similar procedure can be followed to acquire the voltage levels for $V_{T1} \rightarrow V_{TM}$,

$$V_{Ty} = V_{OUT} + (V_{IN} - V_{OUT}) \frac{A(y-1)+1}{A(M-1)+2}, \tag{15}$$

where y ranges from 1 to M. These can now be substituted into (6) for example to acquire the solved expressions for V_{-} for steps (1,1) → (1,N). The solved expressions for the top and bottom plate voltages are:

$$V_{-}^{1,x} = \frac{((N-x-1)A+2)V_{OUT}}{A(N-1)+2}, \tag{16}$$

$$V_{+}^{2,y} = V_{OUT} + (V_{IN} - V_{OUT}) \frac{(M-y-1)A+2}{A(M-1)+2}, \tag{17}$$

$$V_{-}^{3,x} = \frac{xAV_{OUT}}{A(N-1)+2}, \tag{18}$$

$$V_{+}^{4,y} = V_{OUT} + \frac{yA(V_{IN}-V_{OUT})}{A(M-1)+2}. \tag{19}$$

The charge delivered to the output can be observed from Fig. 1, where it occurs on steps (1,0), (3,0)→(3,N) and (4,1)→(4,M). The charge transferred on the steps is as follows,

$$Q_{3,0} = C_{Fly}(V_{+}^{2,M} - V_{OUT}), \tag{20}$$

$$Q_{3,1} \rightarrow Q_{3,N} = C_{Fly} V_{3,N}, \tag{21}$$

and

$$Q_{4,1} \rightarrow Q_{1,0} = C_{Fly}(V_{IN} - V_{OUT}), \tag{22}$$

resulting in a total output charge of

$$\begin{aligned} Q_{OUT} &= Q_{3,0} + Q_{3,1} + Q_{4,1} \\ Q_{OUT} &= C_{Fly}\left(\frac{(A(M-2)+4)(V_{IN}-V_{OUT})}{A(M-1)+2} + \frac{NAV_{OUT}}{A(N-1)+2} \right). \end{aligned} \tag{23}$$

A similar method can be used to acquire the input charge, occurring over steps (1,0) → (2,0),

$$\begin{aligned} Q_{IN} &= C_{Fly}\left(V_{IN} - V_{+}^{4,M} + V_{OUT} \right) \\ Q_{IN} &= C_{Fly}\left(V_{IN} - V_{OUT} - \frac{MA(V_{IN}-V_{OUT})}{A(M-1)+2} + V_{OUT} \right) \\ Q_{IN} &= C_{Fly} \frac{MAV_{OUT} + (2-A)V_{IN}}{A(M-1)+2}. \end{aligned} \tag{24}$$

The input and output charge can then be used in combination with the switching frequency to acquire the input and output power,

$$P_{IN} = V_{IN} f_{SW} C_{Fly} \frac{MAV_{OUT} + (2-A)V_{IN}}{A(M-1)+2}, \tag{25}$$

$$\begin{aligned} P_{OUT} = V_{OUT} f_{SW} C_{Fly} \Big(& \frac{(2-A)(V_{IN}-V_{OUT})}{A(M-1)+2} \\ & + \frac{NAV_{OUT}}{A(N-1)+2} + (V_{IN} - V_{OUT}) \Big). \end{aligned} \tag{26}$$

In order to verify (25) and (26), the calculations are compared to simulation data which corresponded to the

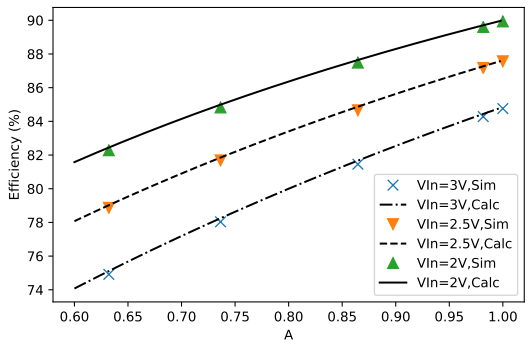


Fig. 5: Comparison between calculated and simulated efficiency results for various values of A and V_{IN}.

prior assumptions. The simulation results were acquired using pspice, in which 36 of the cores in Fig. 2 were used to simulate an N = M = 8 use case. Additional variables used in the simulations were V_{OUT} = 2.5 V, f_{SW} = 250 MHz, C_{Fly} = 1 nF, and R_{ON} was swept between 0.1Ω and 4Ω. The resulting comparison is graphed in Fig. 5, with an average error of <0.3% in both P_{IN} and P_{OUT}.

C. Incorporating Transistor Switching Losses

The power lost switching the gates of the transistors on and off can either be added to P_{IN}, or subtracted from P_{OUT}, depending on the bootstrapping and control method used. The power can be calculated using f_{SW}, along with the total gate capacitance of all the switches (C_G), and the switching voltage (V_{SW}),

$$P_{SW} = f_{SW} V_{SW}^2 C_G. \tag{27}$$

This will allow the designer to fully calculate the design trade-off associated with transistor sizing.

IV. Steady State Model Usefulness

The usefulness of the model is going to be dependent on how accurate the underlying assumptions are, these will now be discussed.

A. Switch Resistance

The fixed, time invariant on-resistance of the transistors is an approximation, however the relative bias structure used in [1] should eliminate the variation in R_{ON} based on the top and bottom plate voltages.

The next portion of this assumption is that switches S_{B+}, S_{B-}, S_{T+} and S_{T-} have a resistance of 0 Ω. The reality is that these switches should be sized a factor $\sqrt{M+1}$ or $\sqrt{N+1}$ larger than the other transistors in order to minimize both capacitive and resistive losses. The designer then only needs to incorporate this resistance into (3),

$$A = 1 - \exp\left(\frac{-1}{C_{Fly} R_{ON} (1+\sqrt{M+1}) f_{SW}}\right), \tag{28}$$

which will approximate the resulting impact on performance.

B. Constant V_{IN} and V_{OUT}

This assumption is going to depend entirely on the filtering capacitors used at the input and output. Realistically, there is going to be a reduction in the efficiency resulting from ripple in the input and output. This can be reduced by adapting the out-phasing technique used in [5] to the circuit.

V. Discussion

The proposed model is useful for giving an approximation of the efficiency, and predicting its relationship with the switch resistance. This can be used to optimize transistor sizing, along with selecting N and M. There exists a further need to incorporate additional effects into the model, such as transistor leakage effects, and exploring the exact impact of non-linearities on the performance of the configuration.

Finally, the model would benefit from further verification by incorporating post layout transistor models, as well as verifying the model using a fabricated device.

VI. Conclusion

In this paper, a steady state model of the continuous ratio charge pump architecture is presented. The model is then verified using pspice simulations, which results in a prediction of the input and output power to <0.3% average error. The results and limitations of the model are then discussed.

References

[1] N. Butzen and M. Steyaert, "Design of single-topology continuously scalable-conversion-ratio switched-capacitor DC-DC converters," *IEEE J. of Solid-State Circuits*, vol. 54, no. 4, pp. 1039–1047, 2019.

[2] T. Tanzawa, "A switch-resistance-aware dickson charge pump model for optimizing clock frequency," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 6, pp. 336–340, 2011.

[3] L. J. Svensson and J. G. Koller, "Driving a capacitive load without dissipating fCV^2," in *Proceedings of 1994 IEEE Symposium on Low Power Electronics*, 1994, pp. 100–101.

[4] N. Butzen and M. S. J. Steyaert, "Scalable parasitic charge redistribution: Design of high-efficiency fully integrated switched-capacitor dcdc converters," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2843–2853, 2016.

[5] H. Le, M. Seeman, S. R. Sanders, V. Sathe, S. Naffziger, and E. Alon, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm^2 at 81% efficiency," in *2010 IEEE Int. Solid-State Circuits Conf. - (ISSCC)*, 2010, pp. 210–211.