# A Steady State Model for the Continuous Conversion Ratio Charge Pump

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## I. Abstract

This paper constructs a steady state model of the continuous conversion ratio charge pump architecture from first principles, incorporating incomplete charge transfer and finite switch resistance. The model is then verified using a pspice model of the circuit, and the limitations of the assumptions are discussed.

## II. Introduction

The rise of IoT has driven the development of various ultra low power, low cost mobile systems. This results in a need for high efficiency, low cost power electronics.

One candidate for addressing many of the needs of industry is the continuous conversion charge pump proposed in [1]. The proposed structure has the benefit of providing a completely variable conversion ratio while maintaining high efficiencies.

The development of models for the structure will facilitate reduced design times, and a more streamlined design flow. One of the important aspects of the continuous ratio converter is the resulting impact of incomplete charge transfer on the efficiency and performance of the converter. The following work proposes a steady state model that will incorporate the effects of incomplete charge transfer into the existing equations for input and output current.

The structure of the paper is as follows, first, a model of the charge pump will be generated. Next, the results of the model are then compared to simulations performed using pspice. The results are then discussed, along with the validity of the assumptions.

## III. Steady State Model

The circuit to be analyzed is the continuous conversion ratio circuit as seen in [1], which can be seen in Fig. 1. The various steps are numbered along with their associated capacitors in Fig. 1, and will be used further in the analysis. The circuit diagram corresponding to a single flying capacitor and its switches (also referred to as a "core") can be seen in Fig. 2. The analysis and modeling is performed under the following assumptions,

- All the capacitors are linear.
- The top and bottom plate parasitic capacitance's have minimal impact on the transient and steady state characteristics of the converter, and are neglected from the analysis.
- All the flying capacitors are equally sized with capacitance $C_{Fly}$, where $C_{Fly} = C_{1,0} = C_{1,1} = C_{2,0} = C_{2,M} ...$
- The input and output voltages $V_{IN}$, and $V_{OUT}$ are constant and ideal.
- The switches for the intermediary nodes, $S_{T1}, S_{T2}, S_{TM}, S_{B1}, S_{BN}, etc$, all have an equivalent resistance $R_{ON}$. The resistance of the switches which connect to the positive and negative rails ($S_{T+}, S_{T-}, S_{B+}, S_{B-}$) is $0\Omega$ .

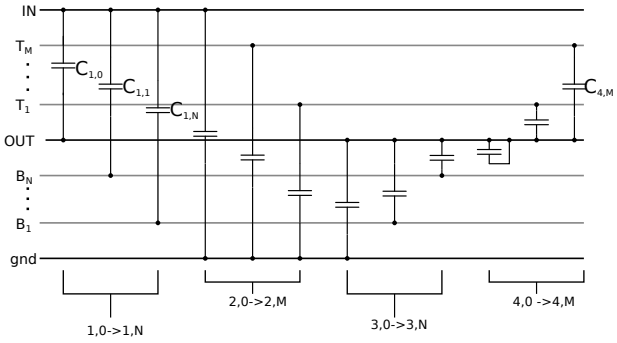



Fig. 1: Circuit diagram illustrating the various connections made by the flying capacitors for the continuous ratio.

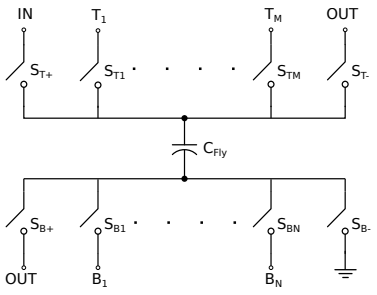
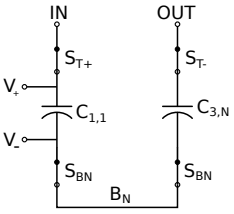


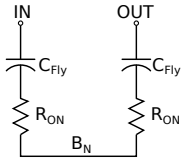

Fig. 2: Circuit diagram illustrating the top and bottom connections of a single flying capacitor.

### A. Charge Transfer Analysis

The operation of the converter is as follows, each capacitor iterates from steps (1,0)→(4,M) sequentially. There is always a connection on the top or bottom plate




(a) Circuit configuration including switches and flying capacitors.




(b) Equivalent circuit with values.

Fig. 3: Example circuit diagrams showing the connection to $B_N$.

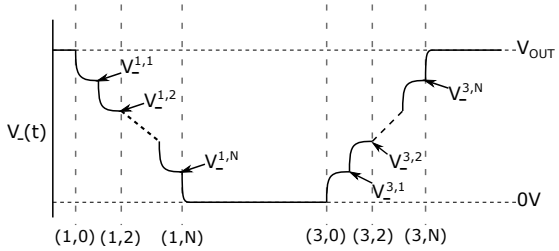



Fig. 4: Illustration of $V_{-}(t)$ for various time steps over the period, where $V_{-}$ is the bottom plate of the capacitor, as in 3a.

to either 0 V, $V_{IN}$ or $V_{OUT}$. The other connection to the intermediary voltage domains (those being $B_1 \rightarrow B_N$ and $T_1 \rightarrow T_M$) occurs through a switch with a resistance $R_{ON}$, where the core voltage begins to equalize with the new voltage domain. An example circuit can be seen in Fig. 3a, which is electrically equivalent to Fig. 3b.

The circuit diagram in Fig. 3b, can be used to calculate the transient response of the circuit over each time step. Consider node ($B_N$), the impedance of both branches to IN and OUT is identical, this symmetry results in $B_N$ being constant over a single time step. The top and bottom plate voltages of the capacitors can then be described using a single $RC$ time constant ($\tau$), where $\tau = R_{ON}C_{Fly}$. Using Fig. 3b as an example, the top plate voltage of $C_{1,1}$ is known, while the bottom plate voltage ($V_{-}^{1,1}$) can be calculated as,

$$V_{-}^{1,1}(t) = V_{OUT}\exp\left(\frac{-t}{\tau}\right) + V_{BN}\left(1-\exp\left(\frac{-t}{\tau}\right)\right), \tag{1}$$

where $t$ is the time after the start of the step. More generally, the top and bottom plate voltages can be described as,

$$V_C[n] = V_C[n\text{–}1]\exp\left(\frac{-1}{\tau f_{SW}}\right) + V_{int}\left(1-\exp\left(\frac{-t}{\tau f_{SW}}\right)\right), \tag{2}$$

where $V_C[n-1]$ is the voltage at the end of previous step, while $V_{int}$ is the voltage of the intermediary node ($V_{T1}$, $V_{TM}$, $V_{B1}$, etc) which the capacitor is connected to. Next, the duration of each time step can be incorporated into the analysis using the switching frequency ($f_{SW}$). A substitution can then be made to simplify the analysis, where

$$A = 1-\exp\left(\frac{-1}{\tau f_{SW}}\right), \tag{3}$$

which can be substituted into (2) for example

$$V_C[n] = V_C[n-1]A + V_{int}(1-A), \tag{4}$$

which can then be used to express the bottom plate voltage as a series of multiplications. The bottom plate voltage for steps (1,1)→(1,N) is illustrated in Fig. 4, and can be described as a sequence of transitions, where

$$\begin{aligned} V_{-}^{1,1} &= V_{OUT}(1-A) + AV_{BN}, \\ V_{-}^{1,2} &= V_{-}^{1,1}(1-A) + AV_{BN-1}, \\ &\vdots \\ V_{-}^{1,N} &= V_{-}^{1,N-1}(1-A) + AV_{B1}. \end{aligned} \tag{5}$$

Using this, the matrix in equation (6) can be constructed to describe the bottom plate voltages. Using a similar method, the matrix in equation (7) can be constructed for the bottom plate voltages in steps (3,N)→(3,1).

Next, a charge balance analysis can be used to calculate the current moving into and out of nodes $B_1 \rightarrow B_N$ on each time step. In both cases, the charge into the node can be calculated using the change in voltage on the capacitor,

$$Q_{Bx} = C_{Fly}(V_{-}^{1,x} - V_{-}^{1,x-1}), \tag{8}$$

where $x$ is the index from 1 to $N$. This can be used to construct matrices for both steps $(1,1) \rightarrow (1,N)$

and $(3,1) \rightarrow (3,N)$ as in (9) and (10) respectively. The charge out of the nodes can then be added, and summed to zero, as the voltage at the nodes does not change at steady state. The solved expression for voltage levels $V_{B1} \rightarrow V_{BN}$ is,

$$V_{Bx} = V_{OUT}\frac{A(x-1)+1}{A(N-1)+2}, \tag{11}$$

a similar procedure can be followed to acquire the voltage levels for $V_{T1} \rightarrow V_{TN}$,

$$V_{Tx} = V_{OUT} + (V_{IN}-V_{OUT})\frac{A(x-1)+1}{A(N-1)+2}. \tag{12}$$

These can now be substituted into (6) for example to acquire the solved expressions for $V_{-}$ for steps (1,1) →

$$\begin{bmatrix} V_-^{1,1} \\ V_-^{1,2} \\ \vdots \\ V_-^{1,N-1} \\ V_-^{1,N} \end{bmatrix} = \begin{bmatrix} A & 0 & \dots & 0 & 0 \\ A(1-A) & A & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A(1-A)^{N-2} & A(1-A)^{N-3} & \dots & A & 0 \\ A(1-A)^{N-1} & A(1-A)^{N-2} & \dots & A(1-A) & A \end{bmatrix} \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix} + V_{OUT} \begin{bmatrix} (1-A) \\ (1-A)^2 \\ \vdots \\ (1-A)^{N-1} \\ (1-A)^N \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} V_-^{3,N} \\ V_-^{3,N-1} \\ \vdots \\ V_-^{3,2} \\ V_-^{3,1} \end{bmatrix} = \begin{bmatrix} A & A(1-A) & \dots & A(1-A)^{N-2} & A(1-A)^{N-1} \\ 0 & A & \dots & A(1-A)^{N-3} & A(1-A)^{N-2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & A & A(1-A) \\ 0 & 0 & \dots & 0 & A \end{bmatrix} \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix} \tag{7}$$

$$\begin{bmatrix} Q_{BN} \\ Q_{BN-1} \\ \vdots \\ Q_{B2} \\ Q_{B1} \end{bmatrix} = C_{Fly} \begin{bmatrix} -A & 0 & \dots & 0 & 0 \\ A^2 & -A & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A^2(1-A)^{N-3} & A^2(1-A)^{N-4} & \dots & -A & 0 \\ A^2(1-A)^{N-2} & A^2(1-A)^{N-3} & \dots & A^2 & -A \end{bmatrix} \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix} + C_{Fly} V_{DD} \begin{bmatrix} A \\ A(1-A) \\ \vdots \\ A(1-A)^{N-2} \\ A(1-A)^{N-1} \end{bmatrix} \tag{9}$$

$$\begin{bmatrix} Q_{BN} \\ Q_{BN-1} \\ \vdots \\ Q_{B2} \\ Q_{B1} \end{bmatrix} = C_{Fly} \begin{bmatrix} -A & A^2 & \dots & A^2(1-A)^{N-3} & A^2(1-A)^{N-2} \\ 0 & -A & \dots & A^2(1-A)^{N-4} & A^2(1-A)^{N-3} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & -A & A^2 \\ 0 & 0 & \dots & 0 & -A \end{bmatrix} \begin{bmatrix} V_{BN} \\ V_{BN-1} \\ \vdots \\ V_{B2} \\ V_{B1} \end{bmatrix} \tag{10}$$

(1,N). The solved expressions for the top and bottom plate voltages are:

$$V_-^{1,x} = \frac{((N-x-1)A+2)V_{OUT}}{A(N-1)+2}, \tag{13}$$

$$V_+^{2,x} = V_{OUT} + (V_{IN} - V_{OUT})\frac{(M-x-1)A+2}{A(M-1)+2}, \tag{14}$$

$$V_-^{3,x} = \frac{xAV_{OUT}}{A(N-1)+2}, \tag{15}$$

$$V_+^{4,x} = V_{OUT} + \frac{xA(V_{IN}-V_{OUT})}{A(N-1)+2}. \tag{16}$$

In order to calculate the input and output currents of the converter, a charge balance method will be used. The charge delivered to the output can be observed from Fig. 1, where it occurs on steps (1,0), (3,0)→(3,N) and (4,1)→(4,M). The charge transferred on the steps is as follows,

$$Q_{3,0} = C_{Fly}(V_+^{2,M} - V_{OUT}), \tag{17}$$

$$Q_{3,1} \rightarrow Q_{3,N} = C_{Fly}V_{3,N}, \tag{18}$$

and

$$Q_{4,1} \rightarrow Q_{1,0} = C_{Fly}(V_{IN} - V_{OUT}), \tag{19}$$

resulting in a total output charge of

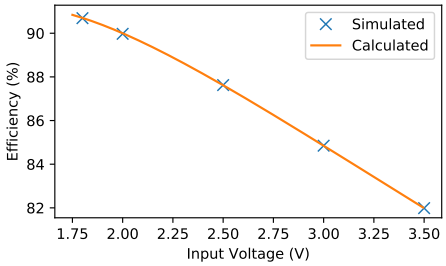
$$\begin{aligned} Q_{OUT} &= Q_{3,0} + Q_{3,1} + Q_{4,1} \\ Q_{OUT} &= C_{Fly}\left(\tfrac{(A(M-2)+4)(V_{IN}-V_{OUT})}{A(M-1)+2} + \tfrac{NAV_{OUT}}{A(N-1)+2}\right). \end{aligned} \tag{20}$$

A similar method can be used to acquire the input charge, occurring over steps (1,0) → (2,0),

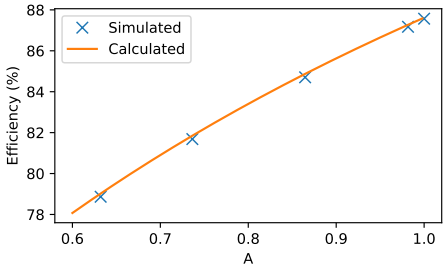
$$\begin{aligned} Q_{IN} &= C_{Fly}\left(V_{IN} - V_+^{4,M} + V_{OUT}\right) \\ Q_{IN} &= C_{Fly}\left(V_{IN} - V_{OUT} - \tfrac{MA(V_{IN}-V_{OUT})}{A(M-1)+2} + V_{OUT}\right) \\ Q_{IN} &= C_{Fly}\tfrac{MAV_{OUT}+(2-A)V_{IN}}{A(M-1)+2} \end{aligned} \tag{21}$$

The input and output charge can then be used in combination with the switching frequency to acquire the input and output power,

$$P_{IN} = V_{IN}f_{SW}C_{Fly}\frac{MAV_{OUT} + (2-A)V_{IN}}{A(M-1)+2}, \tag{22}$$




(a) Comparison using $A = 1$ and $V_{OUT} = 1$.




(b) Comparison using $V_{IN} = 2.5$ and $V_{OUT} = 1$.

Fig. 5: Verification of the calculated efficiency. The simulations were setup to conform to the model assumptions.

$$P_{OUT} = V_{OUT} f_{SW} C_{Fly} \Big( \tfrac{(2-A)(V_{IN}-V_{OUT})}{A(M-1)+2} + \tfrac{NAV_{OUT}}{A(N-1)+2} + (V_{IN} - V_{OUT}) \Big). \quad (23)$$

The efficiency can then be calculated using the input and output power, and is then graphed and compared to some simulation results with ideal components. Fig. 5a plots the efficiency in comparison to input voltage, while Fig. 5b plots efficiency in comparison to $A$.

### B. Incorporating Transistor Switching Losses

The power lost switching the gates of the transistors on and off can either be added to $P_{IN}$, or subtracted from $P_{OUT}$, depending on the bootstrapping and control method used. The power can be calculated using $f_{SW}$, along with the total gate capacitance of all the switches ($C_G$), and the switching voltage $V_{SW}$,

$$P_{SW} = f_{SW} V_{SW}^2 C_G. \quad (24)$$

This will allow the designer to fully calculate the design trade-off associated with transistor sizing.

## IV. Steady State Model Usefulness

The usefulness of the model is going to be dependent on how accurate the underlying assumptions are, these will now be discussed.

### A. Switch Resistance

The fixed, time invariant on-resistance of the transistors is an approximation, however the relative bias structure used in [1] should eliminate the variation in $R_{ON}$ based on the top and bottom plate voltages.

The next portion of this assumption is that switches $S_{B+}$, $S_{B-}$, $S_{T+}$ and $S_{T-}$ have a resistance of $0\,\Omega$. The reality is that these switches should be sized a factor $\sqrt{M+1}$ or $\sqrt{N+1}$ larger than the other transistors in order to minimize both capacitive and resistive losses. The designer then only needs to incorporate this resistance into (3),

$$A = 1 - \exp\left( \frac{-1}{C_{Fly} R_{ON} (1+\sqrt{M+1}) f_{SW}} \right), \quad (25)$$

which will approximate the resulting impact on performance.

### B. Constant $V_{IN}$ and $V_{OUT}$

This assumption is going to depend entirely on the filtering capacitors used at the input and output. Realistically, there is going to be a reduction in the efficiency resulting from ripple in the input and output. This can be reduced by adapting the out-phasing technique used in [2], to the circuit.

## V. Discussion

The proposed model is sufficiently useful for giving an approximation of the efficiency, and predicting its relationship with the transistor sizing. This can be used to quickly explore the design space, and optimize transistor sizing, along with selecting $N$ and $M$ with regards to the architecture. There exists a further need to incorporate additional effects into the model, such as transistor leakage effects, and exploring the exact impact of non-linearities on the performance of the configuration.

Finally, the model would benefit from further verification by incorporating post layout transistor models, as well as verifying the model using a fabricated device.

## VI. Conclusion

In this paper, a steady state model of the continuous ratio charge pump architecture is presented. The model is then verified using pspice simulations, and the results are discussed.

## References

[1] N. Butzen and M. Steyaert, "Design of single-topology continuously scalable-conversion-ratio switched-capacitor DC-DC converters," *IEEE J. of Solid-State Circuits*, vol. 54, no. 4, pp. 1039–1047, 2019.

[2] H. Le, M. Seeman, S. R. Sanders, V. Sathe, S. Naffziger, and E. Alon, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm$^2$ at 81% efficiency," in *2010 IEEE Int. Solid-State Circuits Conf. - (ISSCC)*, 2010, pp. 210–211.