

FR. Conceicao Rodrigues College of Engineering
Department of Computer Engineering

10 .Direct Mapped Cache, Fully Associative Cache, Set associative cache

1. Course, Subject & Experiment Details

| Academic Year | 2023-24 | Estimated Time | Experiment No. 11– 02 Hours |
|-------------------|-----------------------------|----------------|--|
| Course & Semester | S.E. (Computers) – Sem. III | Subject Name | Digital Logic & Computer Organization and Architecture |
| Chapter No. | 5 | Chapter Title | Memory Organization |
| Experiment Type | Software | Subject Code | CSC304 |

Rubrics

| Timeline (2) | Practical Skill & Applied Knowledge (4) | Output (4) | Total (10) |
|--------------|---|------------|------------|
| | | | |

2. Aim & Objective of Experiment

1. Understanding behaviour of Direct, associative and set associative cache from working module
2. Designing a Direct, associative and set associative cache for given parameters

3. Problem Statement

Show the memory address representation for the main memory and Ram in bits and Solve for tag size,search time for the following configuration using Direct, associative and 2 way set associative mapping: a) MM=128words , RAM=16words ,Block size= 4words

4. Software Required

Cache Simulator

<https://www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/dmc.html>

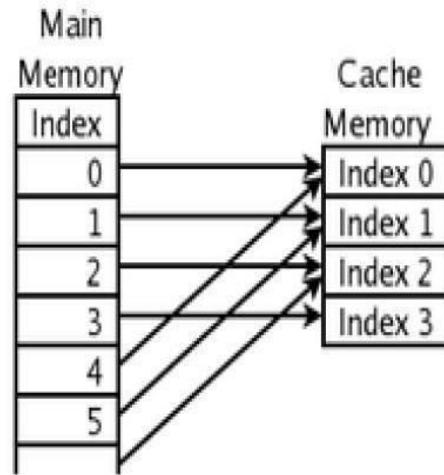
5. Brief Theoretical Description

DIRECT MAPPED CACHE



DEFINITIONS

- **TAG** – distinguishes one cache memory block with another
- **INDEX** – identifies the cache block
- **OFFSET** – points to desired data in cache block



INSTRUCTION BREAKDOWN

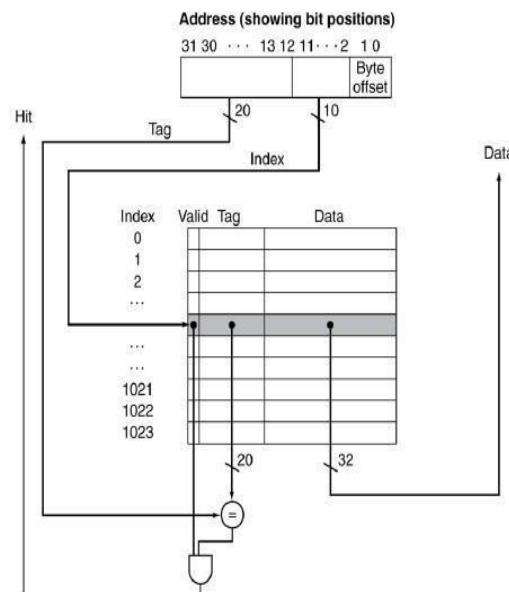
Each of the address of load instruction is broken into three parts: tag, index and offset.
Main memory size = M , cache size = C and offset bits = Z results in the following (right figure).

| | | |
|----------------------------|---------------------------|--------|
| Length of load instruction | $\log_2(M)$ | bits |
| OFFSET | $: z$ | bits |
| INDEX | $: \log_2(C) - z$ | bits |
| TAG | $: \log_2(M) - \log_2(C)$ | bits |
| CACHE BLOCKS | $: \log_2(C)$ | blocks |

DIRECT MAPPED CACHE

HOW IT WORKS

- The requested address is broken down into **tag**, **index**, and **offset**.
- Cache table with corresponding **index** will be examined.
 - If valid bit of the index is equals to 0, **cache miss** is obtained
 - Else tag bit of the requested address will be compared with tag bit in cache table
 - If tag is matched, **cache hit** is obtained
 - Else **cache miss** is obtained
- When **cache hit** is obtained, data from cache table will be returned. Else, data will be retrieved from main memory.



PRO / CONS

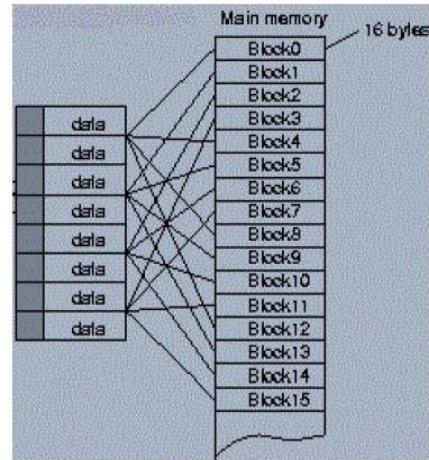
Direct mapping is simple and inexpensive to implement, but if a program accesses 2 blocks that map to the same line repeatedly, the cache begins to thrash back and forth reloading the line over and over again leads to high miss rate.

FULLY ASSOCIATIVE CACHE



DEFINITIONS

- **TAG** – distinguishes one cache memory block with another
- **OFFSET** – points to desired data in cache block



INSTRUCTION BREAKDOWN

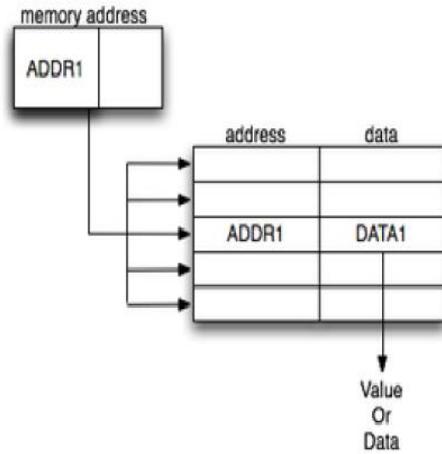
Each of the address of load instruction is broken into three parts: tag and offset.
Main memory size = M , cache size = C and offset bits = Z results in the following (right figure).

| | | |
|----------------------------|-------------------------|--------|
| Length of load instruction | $\log_2(M)$ | bits |
| OFFSET | : z | bits |
| TAG | $\log_2(M) - \log_2(C)$ | bits |
| CACHE BLOCKS | $\log_2(C)$ | blocks |

FULLY ASSOCIATIVE CACHE

HOW IT WORKS

- The requested address is broken down into **tag** and **offset**.
- Requested **tag** will be searched through cache with valid bit
 - If there is **tag** matched with one of the index in the cache table, **cache hit** is obtained
 - Else, **cache miss** is obtained
- When **cache hit** is obtained, data from cache table will be returned. Else, data will be retrieved from main memory.



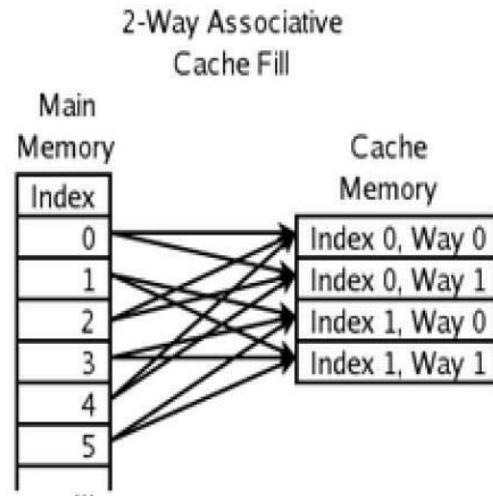
PRO / CONS

Fully Associative is the most efficient utilisation of cache blocks, yet it is expensive to transverse through the cache to find each requested tag. Since there is no specified slot for each instruction, an algorithm of replacement policy must be designed along with implementation of fully associative cache.

[N-WAY] SET ASSOCIATIVE CACHE



N-way set associative cache combines the idea of direct mapped cache and fully associative cache. It has direct mapped principle to an index, yet fully associative concept within the index. An **index** contains N blocks of way.



INSTRUCTION BREAKDOWN

Each of the address of load instruction is broken into three parts: tag, index and offset.

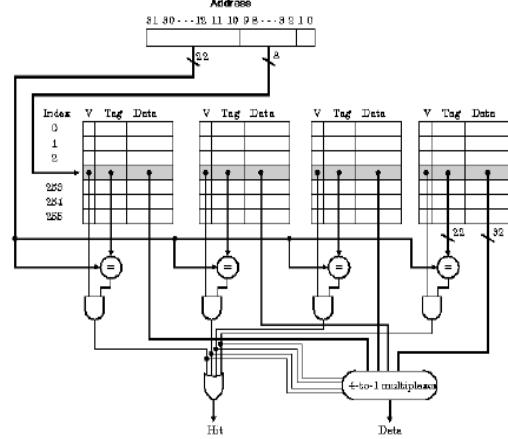
N-way set associative, Main memory size = M , cache size = C and offset bits = Z results in the following (right figure).

| | | |
|----------------------------|---------------------------------------|--------|
| Length of load instruction | : $\log_2(M)$ | bits |
| OFFSET | : z | bits |
| INDEX | : $\log_2(C) - z - \log_2(N)$ | bits |
| TAG | : $\log_2(M) - \log_2(C) + \log_2(N)$ | bits |
| CACHE BLOCKS | : $\log_2(C)$ | blocks |

[N-WAY] SET ASSOCIATIVE CACHE

HOW IT WORKS

- The requested address is broken down into **tag**, **index** and **offset**.
- Cache table with corresponding **index** will be examined. **N-ways** of cache blocks will be transversed.
 - If one of the **way** has the requested index, a **cache hit** will be obtained
 - Else **cache miss** is obtained
- When **cache hit** is obtained, data from cache table will be returned. Else, data will be retrieved from main memory.



PRO / CONS

Combining direct mapped and fully associative principle is seen as the most balanced way to obtain high hit rate meanwhile maintaining the resources cost. However, N-Way associative could be hard for initial implementation as various concepts is involved.

6. Attach the screenshot:

ParaCache

Write Policies

- Write Back
- Write Through
- Write On Allocate
- Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 2048
Offset Bits: 2

Instruction
 Load (in hex#): 4fc
 80,3bb,66a,448,2f,2df,2f7,59b,785

Information
 Valid bit is 0, therefore CACHE MISS is obtained. Cache is updated with the new dataset.

Statistics
 Hit Rate :
 Miss Rate :
 List of Previous Instructions :

DIRECT MAPPED CACHE

Instruction Breakdown

| | | |
|---------|-------|-------|
| 1001111 | 11 | 00 |
| 7 bit | 2 bit | 2 bit |

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|---------|------------|-----------|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |
| 2 | 0 | - | 0 | 0 |
| 3 | 1 | 1001111 | 0 | 0 |

Memory Block

| | | | |
|-----------|-----------|-----------|-----------|
| B. 0 W. 0 | B. 0 W. 1 | B. 0 W. 2 | B. 0 W. 3 |
| B. 1 W. 0 | B. 1 W. 1 | B. 1 W. 2 | B. 1 W. 3 |
| B. 2 W. 0 | B. 2 W. 1 | B. 2 W. 2 | B. 2 W. 3 |
| B. 3 W. 0 | B. 3 W. 1 | B. 3 W. 2 | B. 3 W. 3 |
| B. 4 W. 0 | B. 4 W. 1 | B. 4 W. 2 | B. 4 W. 3 |
| B. 5 W. 0 | B. 5 W. 1 | B. 5 W. 2 | B. 5 W. 3 |

MISS

ParaCache

Write Policies

- Write Back
- Write Through
- Write On Allocate
- Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 2048
Offset Bits: 2

Instruction
 Load (in hex#): 4fc
 80,3bb,66a,448,2f,2df,2f7,59b,785

Information
 Cache table is updated accordingly.
 Block 13F with offset 0 to 3 is transferred to cache.

Statistics
 Hit Rate :
 Miss Rate :
 List of Previous Instructions :

DIRECT MAPPED CACHE

Instruction Breakdown

| | | |
|---------|-------|-------|
| 1001111 | 11 | 00 |
| 7 bit | 2 bit | 2 bit |

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|---------|----------------------|-----------|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |
| 2 | 0 | - | 0 | 0 |
| 3 | 1 | 1001111 | BLOCK 13F WORD 0 - 3 | 0 |

Memory Block

| | | | |
|-------------|-------------|-------------|-------------|
| B. 13F W. 0 | B. 13F W. 1 | B. 13F W. 2 | B. 13F W. 3 |
| B. 140 W. 0 | B. 140 W. 1 | B. 140 W. 2 | B. 140 W. 3 |
| B. 141 W. 0 | B. 141 W. 1 | B. 141 W. 2 | B. 141 W. 3 |
| B. 142 W. 0 | B. 142 W. 1 | B. 142 W. 2 | B. 142 W. 3 |
| B. 143 W. 0 | B. 143 W. 1 | B. 143 W. 2 | B. 143 W. 3 |
| B. 144 W. 0 | B. 144 W. 1 | B. 144 W. 2 | B. 144 W. 3 |

DS_2023_24 | **EXPT-10** | **NTU Direct Mapped Cache Simulator**

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/dmc.html

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ParaCache

Write Policies

- Write Back
- Write Through
- Write On Allocate
- Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Reset Submit

Instruction

Load (in hex#)

3bb,66a,448,2f,2df,2f7,59b,785

Gen. Random Submit

Information

The cycle has been completed.
Please submit another instructions

Next Fast Forward

Statistics

| | |
|-------------|------|
| Hit Rate : | 0% |
| Miss Rate : | 100% |

List of Previous Instructions :

DIRECT MAPPED CACHE

Instruction Breakdown

| | | |
|---------|-------|-------|
| 1001111 | 11 | 00 |
| 7 bit | 2 bit | 2 bit |

Memory Block

| | | | |
|-------------|-------------|-------------|-------------|
| B 13F W. 0 | B. 13F W. 1 | B. 13F W. 2 | B. 13F W. 3 |
| B. 140 W. 0 | B. 140 W. 1 | B. 140 W. 2 | B. 140 W. 3 |
| B. 141 W. 0 | B. 141 W. 1 | B. 141 W. 2 | B. 141 W. 3 |
| B. 142 W. 0 | B. 142 W. 1 | B. 142 W. 2 | B. 142 W. 3 |
| B. 143 W. 0 | B. 143 W. 1 | B. 143 W. 2 | B. 143 W. 3 |
| B. 144 W. 0 | B. 144 W. 1 | B. 144 W. 2 | B. 144 W. 3 |

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|---------|----------------------|-----------|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |
| 2 | 0 | - | 0 | 0 |
| 3 | 1 | 1001111 | BLOCK 13F WORD 0 - 3 | 0 |

DS_2023_24 | **EXPT-10** | **NTU Fully Associative Cache**

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/fa.html

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ParaCache

Replacement Policies

- FIFO
- LRU
- Random

Write Policies

- Write Back
- Write Through
- Write On Allocate
- Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Reset Submit

Instruction

Load (in hex#)

224,495,6b2,403,510,7b9,19e,5ca,39c

Gen. Random Submit

Information

Index requested will be searched in whole cache

Next Fast Forward

Statistics

| | |
|------------|--|
| Hit Rate : | |
|------------|--|

FULLY ASSOCIATIVE CACHE

Instruction Breakdown

| | |
|-----------|-------|
| 111110011 | 10 |
| 9 bit | 2 bit |

Memory Block

| | | | |
|-----------|-----------|-----------|-----------|
| B. 0 W. 0 | B. 0 W. 1 | B. 0 W. 2 | B. 0 W. 3 |
| B. 1 W. 0 | B. 1 W. 1 | B. 1 W. 2 | B. 1 W. 3 |
| B. 2 W. 0 | B. 2 W. 1 | B. 2 W. 2 | B. 2 W. 3 |
| B. 3 W. 0 | B. 3 W. 1 | B. 3 W. 2 | B. 3 W. 3 |
| B. 4 W. 0 | B. 4 W. 1 | B. 4 W. 2 | B. 4 W. 3 |
| B. 5 W. 0 | B. 5 W. 1 | B. 5 W. 2 | B. 5 W. 3 |

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|------------|-----------|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |
| 2 | 0 | - | 0 | 0 |
| 3 | 0 | - | 0 | 0 |

DS_2023_24 | EXPT-10 | NTU Fully Associative Cache

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/fa.html

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ParaCache

Replacement Policies

- FIFO
- LRU
- Random

Write Policies

- Write Back
- Write Through

- Write On Allocate
- Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 2048
Offset Bits: 2

Instruction
 Load (in hex): 7ce
 224,495,6b2,403,510,7b9,19e,5ca,39c
 Gen. Random Submit

Information
 No cache contains 111110011 as value, therefore cache MISS is obtained.

Next **Fast Forward**

FULLY ASSOCIATIVE CACHE

Instruction Breakdown
 111110011 10
 9 bit 2 bit

Memory Block

| | | | |
|-----------|-----------|-----------|-----------|
| B. 0 W. 0 | B. 0 W. 1 | B. 0 W. 2 | B. 0 W. 3 |
| B. 1 W. 0 | B. 1 W. 1 | B. 1 W. 2 | B. 1 W. 3 |
| B. 2 W. 0 | B. 2 W. 1 | B. 2 W. 2 | B. 2 W. 3 |
| B. 3 W. 0 | B. 3 W. 1 | B. 3 W. 2 | B. 3 W. 3 |
| B. 4 W. 0 | B. 4 W. 1 | B. 4 W. 2 | B. 4 W. 3 |
| B. 5 W. 0 | B. 5 W. 1 | B. 5 W. 2 | B. 5 W. 3 |

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|------------|-----------|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |
| 2 | 0 | - | 0 | 0 |
| 3 | 0 | - | 0 | 0 |

Statistics
 Hit Rate :
 Miss Rate :
 List of Previous Instructions :
 Next Index: 0
 Last Index: 3

DS_2023_24 | EXPT-10 | NTU Fully Associative Cache

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/fa.html

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ParaCache

Write Policies

- Write On Allocate
- Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 2048
Offset Bits: 2

Instruction
 Load (in hex): 7ce
 224,495,6b2,403,510,7b9,19e,5ca,39c
 Gen. Random Submit

Information
 The new cache data is imported to cache.

Next **Fast Forward**

FULLY ASSOCIATIVE CACHE

Instruction Breakdown
 111110011 10
 9 bit 2 bit

Memory Block

| | | | |
|--------------|-------------|-------------|-------------|
| B. 0 W. 0 | B. 0 W. 1 | B. 0 W. 2 | B. 0 W. 3 |
| B. 1 F4 W. 0 | B. 1F4 W. 1 | B. 1F4 W. 2 | B. 1F4 W. 3 |
| B. 1F5 W. 0 | B. 1F5 W. 1 | B. 1F5 W. 2 | B. 1F5 W. 3 |
| B. 1F6 W. 0 | B. 1F6 W. 1 | B. 1F6 W. 2 | B. 1F6 W. 3 |
| B. 1F7 W. 0 | B. 1F7 W. 1 | B. 1F7 W. 2 | B. 1F7 W. 3 |
| B. 1F8 W. 0 | B. 1F8 W. 1 | B. 1F8 W. 2 | B. 1F8 W. 3 |

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----------|----------------------|-----------|
| 0 | 1 | 111110011 | BLOCK 1F3 WORD 0 - 3 | 0 |
| 1 | 0 | - | 0 | 0 |
| 2 | 0 | - | 0 | 0 |
| 3 | 0 | - | 0 | 0 |

Statistics
 Hit Rate :
 Miss Rate :
 List of Previous Instructions :
 Next Index: 0
 Last Index: 3

FIFO Fully Associative Cache

Instruction Breakdown

| | |
|-----------|-------|
| 111110011 | 10 |
| 9 bit | 2 bit |

Memory Block

| | | | |
|-----------|-----------|-----------|-----------|
| B.1F3.W.0 | B.1F3.W.1 | B.1F3.W.2 | B.1F3.W.3 |
| B.1F4.W.0 | B.1F4.W.1 | B.1F4.W.2 | B.1F4.W.3 |
| B.1F5.W.0 | B.1F5.W.1 | B.1F5.W.2 | B.1F5.W.3 |
| B.1F6.W.0 | B.1F6.W.1 | B.1F6.W.2 | B.1F6.W.3 |
| B.1F7.W.0 | B.1F7.W.1 | B.1F7.W.2 | B.1F7.W.3 |
| B.1F8.W.0 | B.1F8.W.1 | B.1F8.W.2 | B.1F8.W.3 |

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----------|----------------------|-----------|
| 0 | 1 | 111110011 | BLOCK 1F3 WORD 0 - 3 | 0 |
| 1 | 0 | - | 0 | 0 |
| 2 | 0 | - | 0 | 0 |
| 3 | 0 | - | 0 | 0 |

Information
The cycle has been completed.
Please submit another instructions

Statistics
Hit Rate : 0%

Next **Fast Forward**

2-Way Set Associative Cache

Instruction Breakdown

| | | |
|----------|-------|-------|
| 11111010 | 0 | 01 |
| 8 bit | 1 bit | 2 bit |

Memory Block

| | | | |
|---------|---------|---------|---------|
| B.0.W.0 | B.0.W.1 | B.0.W.2 | B.0.W.3 |
| B.1.W.0 | B.1.W.1 | B.1.W.2 | B.1.W.3 |
| B.2.W.0 | B.2.W.1 | B.2.W.2 | B.2.W.3 |
| B.3.W.0 | B.3.W.1 | B.3.W.2 | B.3.W.3 |
| B.4.W.0 | B.4.W.1 | B.4.W.2 | B.4.W.3 |
| B.5.W.0 | B.5.W.1 | B.5.W.2 | B.5.W.3 |

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|------------|-----------|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |

Information
Index requested will be searched in cache as highlighted in yellow

Statistics
Hit Rate : 0%

Next **Fast Forward**

DS_2023_24 | EXPT-10 | NTU 2-Way Set Associative Cache

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/sa2.html

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ParaCache

Replacement Policies: FIFO LRU Random

Write Policies: Write Back Write Through Write On Allocate Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 2048
Offset Bits: 2

Reset Submit

Instruction: Load (in hex) # 7d1
44,263,441,316,7e8,124,716,52b,42
Gen. Random Submit

Information: Following is the analysis diagram.

Statistics: Hit Rate :

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown: 11111010 | 0 | 01
8 bit | 1 bit | 2 bit

Memory Block:

| | | | |
|---------|---------|---------|---------|
| B.0 W.0 | B.0 W.1 | B.0 W.2 | B.0 W.3 |
| B.1 W.0 | B.1 W.1 | B.1 W.2 | B.1 W.3 |
| B.2 W.0 | B.2 W.1 | B.2 W.2 | B.2 W.3 |
| B.3 W.0 | B.3 W.1 | B.3 W.2 | B.3 W.3 |
| B.4 W.0 | B.4 W.1 | B.4 W.2 | B.4 W.3 |
| B.5 W.0 | B.5 W.1 | B.5 W.2 | B.5 W.3 |

Cache Table:

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|------------|-----------|
| 0 | 1 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|------------|-----------|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |

DS_2023_24 | EXPT-10 | NTU 2-Way Set Associative Cache

[www3.ntu.edu.sg/home/smitha/Paracache/Paracache/sa2.html](http://www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/sa2.html)

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ParaCache

Replacement Policies: FIFO LRU Random

Write Policies: Write Back Write Through Write On Allocate Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 2048
Offset Bits: 2

Reset Submit

Instruction: Load (in hex) # 7d1
44,263,441,316,7e8,124,716,52b,42
Gen. Random Submit

Information: Following is the analysis diagram.

Statistics: Hit Rate :
Miss Rate :
List of Previous Instructions :

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown: 11111010 | 0 | 01
8 bit | 1 bit | 2 bit

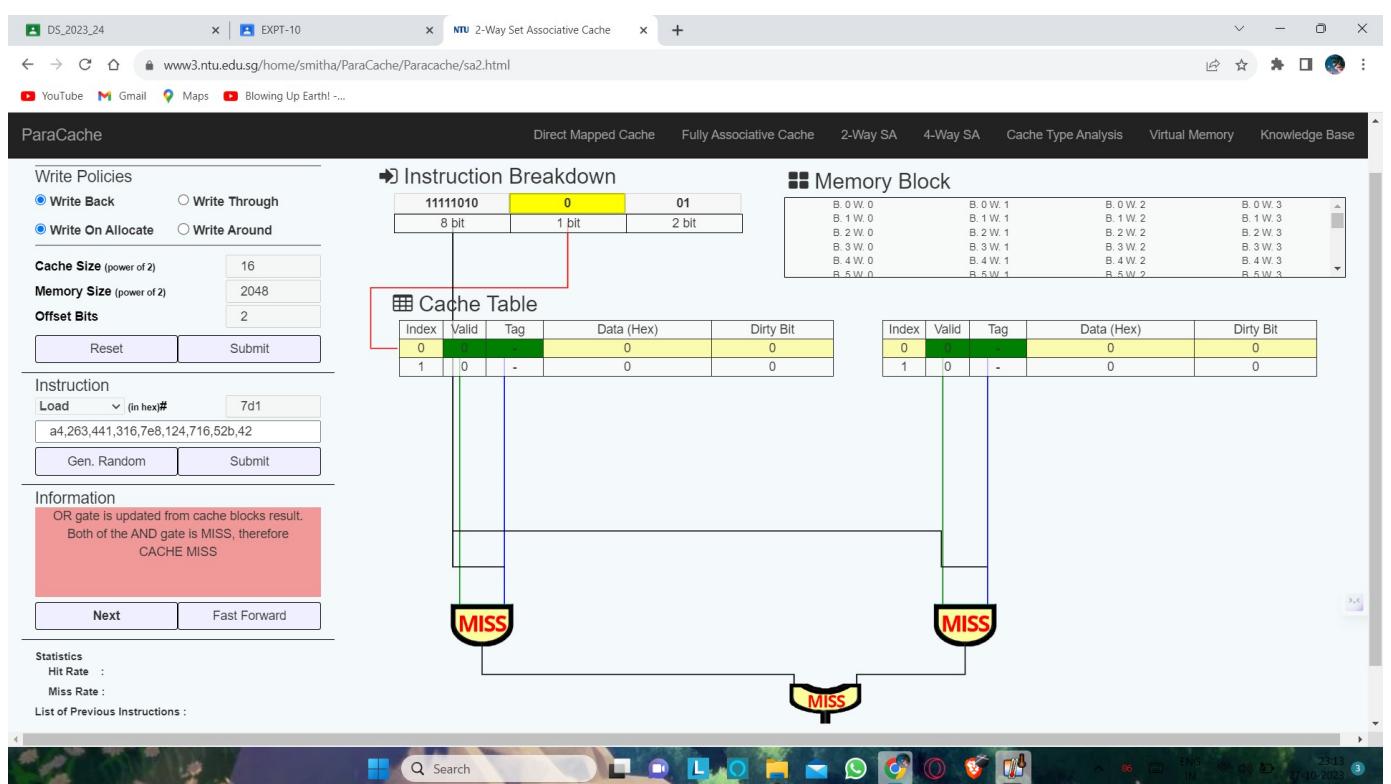
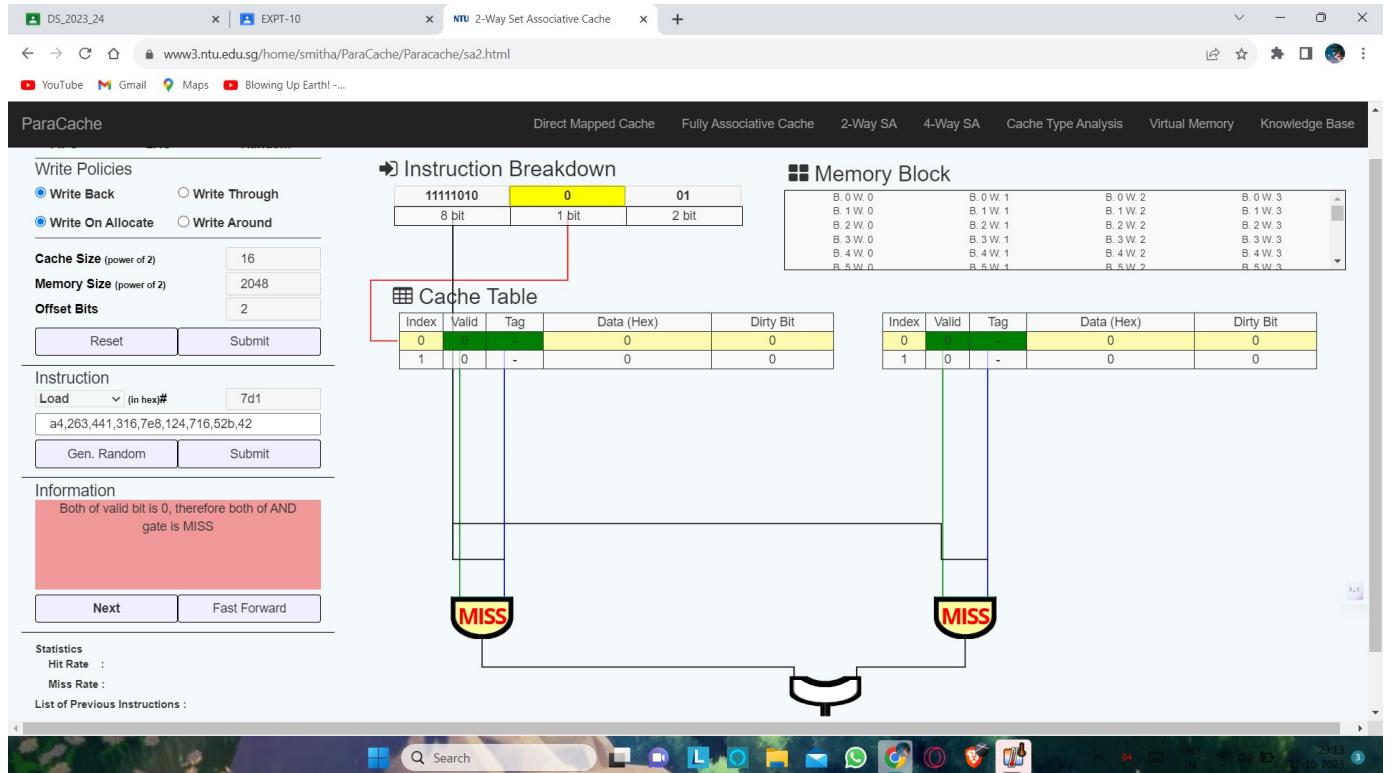
Memory Block:

| | | | |
|---------|---------|---------|---------|
| B.0 W.0 | B.0 W.1 | B.0 W.2 | B.0 W.3 |
| B.1 W.0 | B.1 W.1 | B.1 W.2 | B.1 W.3 |
| B.2 W.0 | B.2 W.1 | B.2 W.2 | B.2 W.3 |
| B.3 W.0 | B.3 W.1 | B.3 W.2 | B.3 W.3 |
| B.4 W.0 | B.4 W.1 | B.4 W.2 | B.4 W.3 |
| B.5 W.0 | B.5 W.1 | B.5 W.2 | B.5 W.3 |

Cache Table:

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|------------|-----------|
| 0 | 1 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|------------|-----------|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |



DS_2023_24 | EXPT-10 | NTU 2-Way Set Associative Cache

ParaCache

Replacement Policies: FIFO LRU Random

Write Policies: Write Back Write Through Write On Allocate Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 2048
Offset Bits: 2

Instruction Breakdown: **1111010** 0 01

| | | |
|-------|-------|-------|
| 8 bit | 1 bit | 2 bit |
|-------|-------|-------|

Memory Block:

| | | | |
|-----------|-----------|-----------|-----------|
| B.1F4.W.0 | B.1F4.W.1 | B.1F4.W.2 | B.1F4.W.3 |
| B.1F5.W.0 | B.1F5.W.1 | B.1F5.W.2 | B.1F5.W.3 |
| B.1F6.W.0 | B.1F6.W.1 | B.1F6.W.2 | B.1F6.W.3 |
| B.1F7.W.0 | B.1F7.W.1 | B.1F7.W.2 | B.1F7.W.3 |
| B.1F8.W.0 | B.1F8.W.1 | B.1F8.W.2 | B.1F8.W.3 |
| B.1F9.W.0 | B.1F9.W.1 | B.1F9.W.2 | B.1F9.W.3 |

Cache Table:

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|---------------|-----------|
| 0 | 1 | fa | B.1F4.W.0 - 3 | 0 |
| 1 | 0 | - | 0 | 0 |

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|------------|-----------|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |

Information: The cycle has been completed. Please submit another instructions.

Statistics: Hit Rate: 0%

DS_2023_24 | EXPT-10 | NTU 2-Way Set Associative Cache

ParaCache

Replacement Policies: FIFO LRU Random

Write Policies: Write Back Write Through Write On Allocate Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 2048
Offset Bits: 2

Instruction Breakdown: **1111010** 0 01

| | | |
|-------|-------|-------|
| 8 bit | 1 bit | 2 bit |
|-------|-------|-------|

Memory Block:

| | | | |
|-----------|-----------|-----------|-----------|
| B.1F4.W.0 | B.1F4.W.1 | B.1F4.W.2 | B.1F4.W.3 |
| B.1F5.W.0 | B.1F5.W.1 | B.1F5.W.2 | B.1F5.W.3 |
| B.1F6.W.0 | B.1F6.W.1 | B.1F6.W.2 | B.1F6.W.3 |
| B.1F7.W.0 | B.1F7.W.1 | B.1F7.W.2 | B.1F7.W.3 |
| B.1F8.W.0 | B.1F8.W.1 | B.1F8.W.2 | B.1F8.W.3 |
| B.1F9.W.0 | B.1F9.W.1 | B.1F9.W.2 | B.1F9.W.3 |

Cache Table:

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|---------------|-----------|
| 0 | 1 | fa | B.1F4.W.0 - 3 | 0 |
| 1 | 0 | - | 0 | 0 |

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|-------|-------|-----|------------|-----------|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |

Information: The cycle has been completed. Please submit another instructions.

Statistics: Hit Rate: 0%

7. Conclusion:

Hence, the memory address representation for the main memory and RAM in the bits is shown and a Direct associative, Fully associative and N-way associative cache is designed using the cache simulator.