33.1 Basic configuration

The DAC is configured using the following registers:

1. Power: The DAC is always connected to V_{DDA}. Register access is determined by IOCON register settings (see below).
2. Peripheral clock: The DAC operates from the common PCLK that clocks both the bus interface and functional portion of most APB peripherals. See Section 3.3.3.5.
3. Pins: Enable the DAC pin and select the pin mode for DACOUT through the relevant IOCON register (Section 7.4.1). This must be done before accessing any DAC registers.
4. DMA: The DAC can be connected to the GPDMA controller (see Section 33.5.2). For GPDMA connections, see Table 692.

33.2 Features

- 10-bit digital to analog converter
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable speed vs. power
- Maximum update rate of 1 MHz.

33.3 Architecture

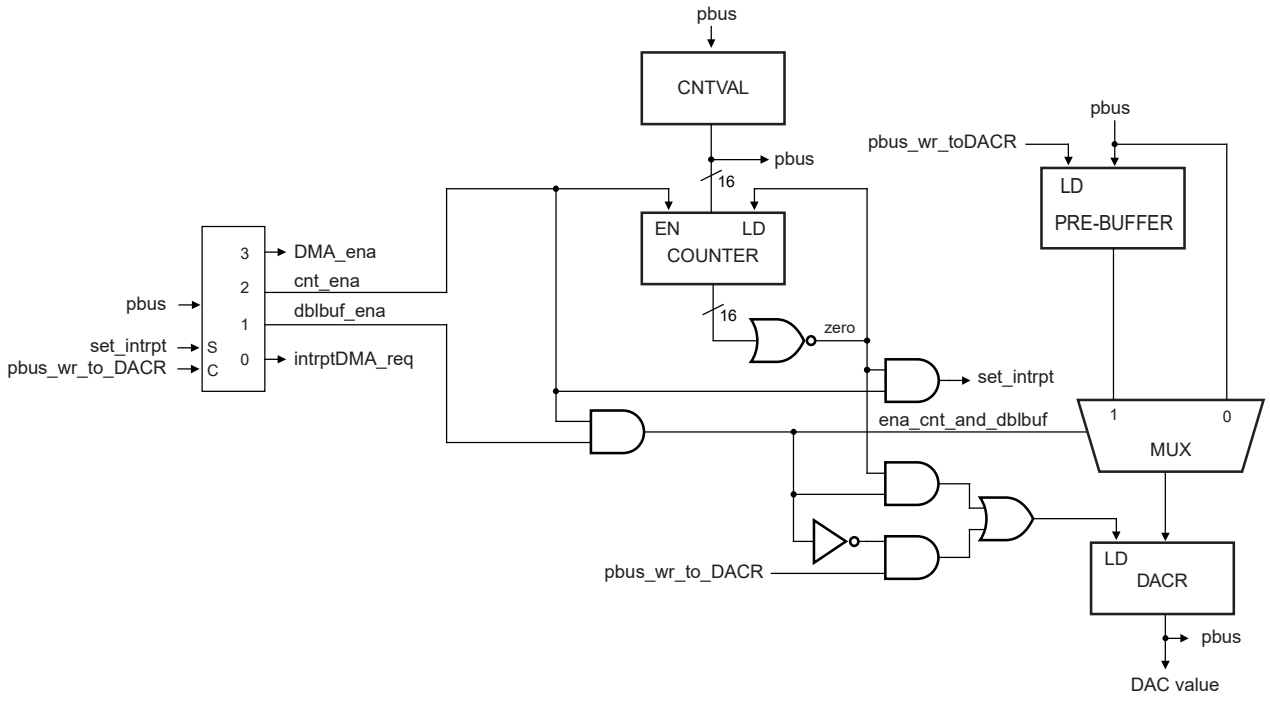

Fig 162. DAC control with DMA interrupt and timer

33.4 Pin description

Table 680 gives a brief summary of each of DAC related pins.

Table 680. D/A Pin Description

Pin	Type	Description
DAC_OUT	Output	**Analog Output.** After the selected settling time after the DACR is written with a new value, the voltage on this pin (with respect to V_{SSA}) is VALUE × ((V_{REFP} - V_{REFN})/1024) + V_{REFN}. Note that DAC_OUT is disabled when the CPU is in Deep-sleep, Power-down, or Deep Power-down modes.
V_{REFP}	Reference	**Voltage Reference.** This pin provides a voltage reference level for the ADC and DAC. **Note: V_{REFP} should be tied to VDD(3V3) if the ADC and DAC are not used.**
V_{DDA}, V_{SSA}	Power	**Analog Power and Ground.** These should typically be the same voltages as V_{DD} and V_{SS}, but should be isolated to minimize noise and error. **Note: VDDA should be tied to VDD(3V3) and VSSA should be tied to VSS if the ADC and DAC are not used.**

33.5 Register description

Note that the DAC does not have a control bit in the PCONP register. To enable the DAC, its output must be selected to appear on the related pin, P0[26], by configuring the relevant IOCON register (Section 7.4.1). See Section 7.4.1 “I/O configuration register contents (IOCON)”. the DAC must be enabled in this manner prior to accessing any DAC registers.

Table 681. Register overview: DAC (base address 0x4008 C000)

Name	Access	Address offset	Description	Reset value[1]	Table
CR	R/W	0x000	D/A Converter Register. This register contains the digital value to be converted to analog and a power control bit.	0	682
CTRL	R/W	0x004	DAC Control register. This register controls DMA and timer operation.	0	683
CNTVAL	R/W	0x008	DAC Counter Value register. This register contains the reload value for the DAC DMA/Interrupt timer.	0	684

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

33.5.1 D/A Converter Register

This read/write register includes the digital value to be converted to analog, and a bit that trades off performance vs. power. Bits 5:0 are reserved for future, higher-resolution D/A converters.

Table 682: D/A Converter Register (CR - address 0x4008 C000) bit description

Bit	Symbol	Value	Description	Reset Value
5:0	-		Reserved. Read value is undefined, only zero should be written.	NA
15:6	VALUE		After the selected settling time after this field is written with a new VALUE, the voltage on the DAC_OUT pin (with respect to V_{SSA}) is VALUE × ((V_{REFP} - V_{REFN})/1024) + V_{REFN}.	0
16	BIAS		Settling time The settling times noted in the description of the BIAS bit are valid for a capacitance load on the DAC_OUT pin not exceeding 100 pF. A load impedance value greater than that value will cause settling time longer than the specified time. One or more graphs of load impedance vs. settling time will be included in the final data sheet.	0
		0	The settling time of the DAC is 1 μs max, and the maximum current is 700 μA. This allows a maximum update rate of 1 MHz.	
		1	The settling time of the DAC is 2.5 μs and the maximum current is 350 μA. This allows a maximum update rate of 400 kHz.	
31:17	-		Reserved. Read value is undefined, only zero should be written.	NA

33.5.2 D/A Converter Control register

This read/write register enables the DMA operation and controls the DMA timer.

Table 683. D/A Control register (CTRL - address 0x4008 C004) bit description

Bit	Symbol	Value	Description	Reset Value
0	INT_DMA_REQ		DMA interrupt request	0
		0	Clear on any write to the DACR register.	
		1	Set by hardware when the timer times out.	
1	DBLBUF_ENA		Double buffering	0
		0	Disable	
		1	Enable. When this bit and the CNT_ENA bit are both set, the double-buffering feature in the DACR register will be enabled. Writes to the DACR register are written to a pre-buffer and then transferred to the DACR on the next time-out of the counter.	
2	CNT_ENA		Time-out counter operation	0
		0	Disable	
		1	Enable	
3	DMA_ENA		DMA access	0
		0	Disable	
		1	Enable. DMA Burst Request Input 7 is enabled for the DAC (see Table 692).	
31:4	-		Reserved. Read value is undefined, only zero should be written.	NA

33.5.3 D/A Converter Counter Value register

This read/write register contains the reload value for the Interrupt/DMA counter.

Table 684: D/A Converter Counter Value register (CNTVAL - address 0x4008 C008) bit description

Bit	Symbol	Description	Reset Value
15:0	VALUE	16-bit reload value for the DAC interrupt/DMA timer.	0
31:16	-	Reserved	-

33.6 Operation

33.6.1 DMA counter

When the counter enable bit CNT_ENA in DACCTRL is set, a 16-bit counter will begin counting down, at the rate selected by PCLK (see Section 3.3.3.5), from the value programmed into the DACCNTVAL register. The counter is decremented Each time the counter reaches zero, the counter will be reloaded by the value of DACCNTVAL and the DMA request bit INT_DMA_REQ will be set in hardware.

Note that the contents of the DACCTRL and DACCNTVAL registers are read and write accessible, but the timer itself is not accessible for either read or write.

If the DMA_ENA bit is set in the DACCTRL register, the DAC DMA request will be routed to the GPDMA. When the DMA_ENA bit is cleared, the default state after a reset, DAC DMA requests are blocked.

33.6.2 Double buffering

Double-buffering is enabled only if both, the CNT_ENA and the DBLBUF_ENA bits are set in DACCTRL. In this case, any write to the DACR register will only load the pre-buffer, which shares its register address with the DACR register. The DACR itself will be loaded from the pre-buffer whenever the counter reaches zero and the DMA request is set. At the same time the counter is reloaded with the COUNTVAL register value.

Reading the DACR register will only return the contents of the DACR register itself, not the contents of the pre-buffer register.

If either the CNT_ENA or the DBLBUF_ENA bits are 0, any writes to the DACR address will go directly to the DACR register.