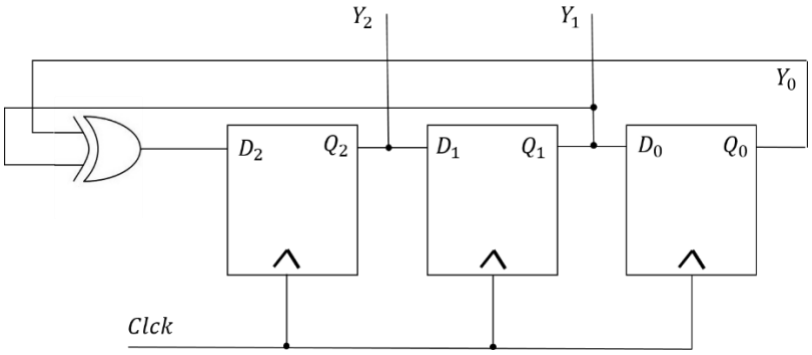
1. he following figure shows a sequential circuit with two D Flip Flops with a common input clock. Assume that the flip flops are initialized at '1'. That is, $Q_0 = Q_1 = Q_2 = 1$ during Cycle 0. This means the output of this circuit is initially $Q_2Q_1Q_0$ = '1 1 1'.

   a. Compute the value of each output signal (Q_2, Q_1 and Q_0) for 8 cycles using the table below.

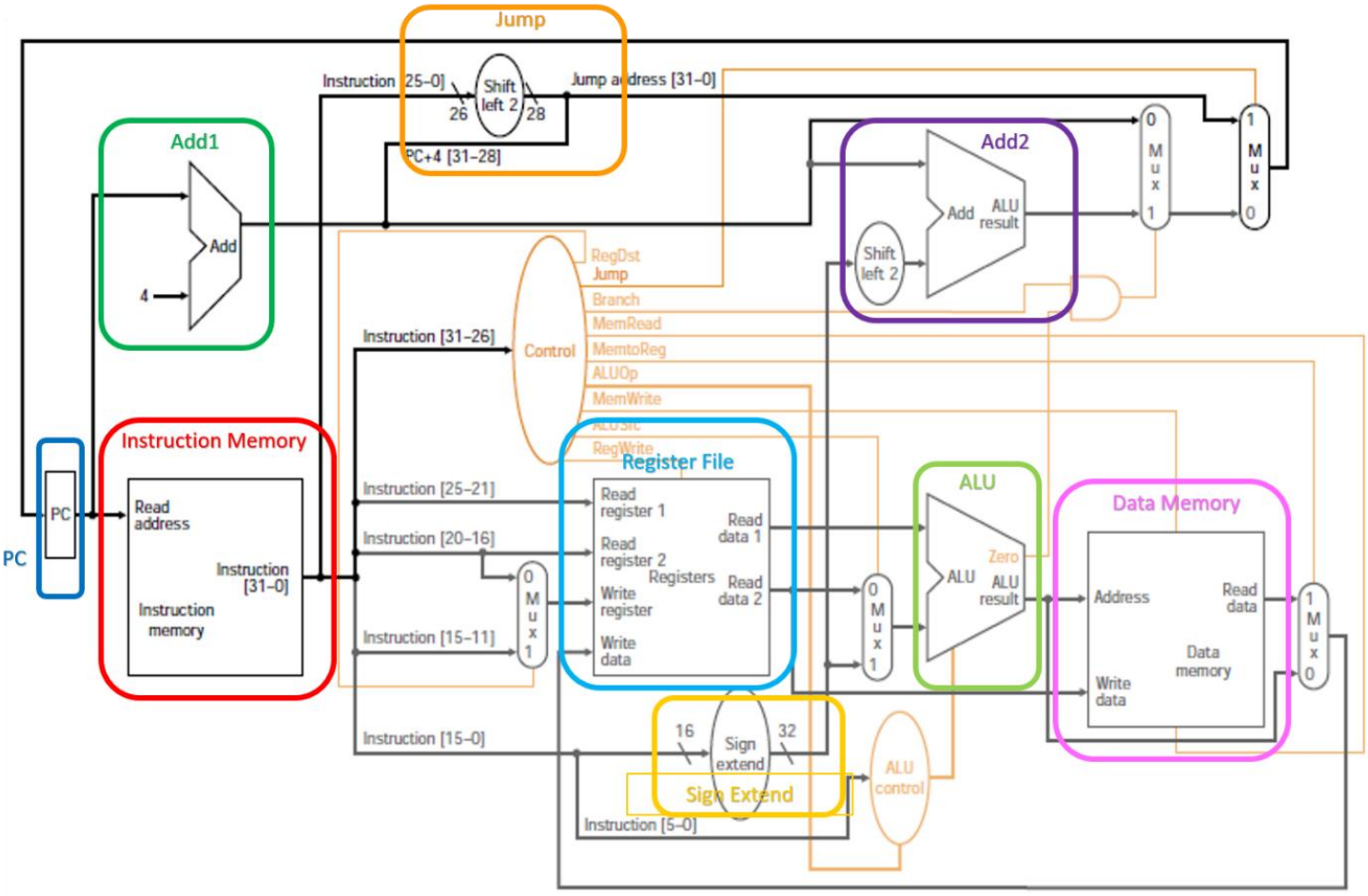
   b. Convert the 3-bit binary $Q_2Q_1Q_0$ to its equivalent decimal in the table. How many unique output states (i.e., $Q_2Q_1Q_0$) does this circuit produce?



Clock Cycle	D_2 D_1 D_0	Q_2 Q_1 Q_0	Decimal ($Q = Q_2Q_1Q_0$)
0		1 1 1	7
1			
2			
3			
4			
5			
6			
7			
8			

2. Consider the following 3 instructions are to be executed though the MIPS architecture shown below. Assume that the branch instruction is taken.

```
lw      $t1, 12($t0)
and     $s0, $t2, $t1
beq     $0, $s0, 1048d
```



a. Fill out the table below to show which of the hardware blocks are used (i.e., are active) during execution of each instruction. Each hardware block is shown by a box in the next figure.

	PC	Instruction Memory	Register File	Sing Extend	ALU	Data Memory	ADD1	ADD2	Jump
lw									
and									
beq									

b. Fill out the table below to show which of the control signals in the figure should be activated (set to 1) during execution of each instruction. You do not need to specify inactive or unknown (i.e. '0' and 'x' values) signals in this part.

	RegDst	Jump	Branch	MemRead	MemtoReg	MemWrite	RegWrite
lw							
and							
beq							

c. Assume the program starts from address 1032d (i.e., address 1032 decimal) in the instruction memory and branch is taken. Compute the value of PC after each instruction is executed.

	Program Counter (PC) Content
lw	
and	
beq	

3. Consider the following instruction sequence executing on the 5-stage MIPS pipeline of form IF, ID, EX, MEM, WB.

```
li      $t1, 8
lw      $t2, 4($t0)
add     $t3, $t1, $t2
sw      $t3, 12($t0)
```

a. Assume that the pipeline does not use any forwarding. Complete the following pipeline execution diagram for the above instruction sequence, showing the flow of instructions through the pipeline during each clock cycle. Indicate any necessary stalls on the pipeline diagram. How many cycles does it take to complete execution of the instruction sequence? What is the overall CPI?

Instruction / Cycle	1	2	3	4	5	6	7	8	9	10	11	12
li $t1, 8	IF	ID	EX	MEM	WB							
lw $t2, 4($t0)												
add $t3, $t1, $t2												
sw $t3, 12($t0)												

b. Now, assume that all possible forwarding paths have been added to the pipeline. Redraw the pipeline execution diagram below. In the diagram show forwarding by arrows. How many cycles does it take to finish the instruction sequence? What is the overall CPI?

Instruction / Cycle	1	2	3	4	5	6	7	8	9	10	11	12
li $t1, 8	IF	ID	EX	MEM	WB							
lw $t2, 4($t0)												
add $t3, $t1, $t2												
sw $t3, 12($t0)												