CPT_S 260 Intro to Computer Architecture
Lecture 26

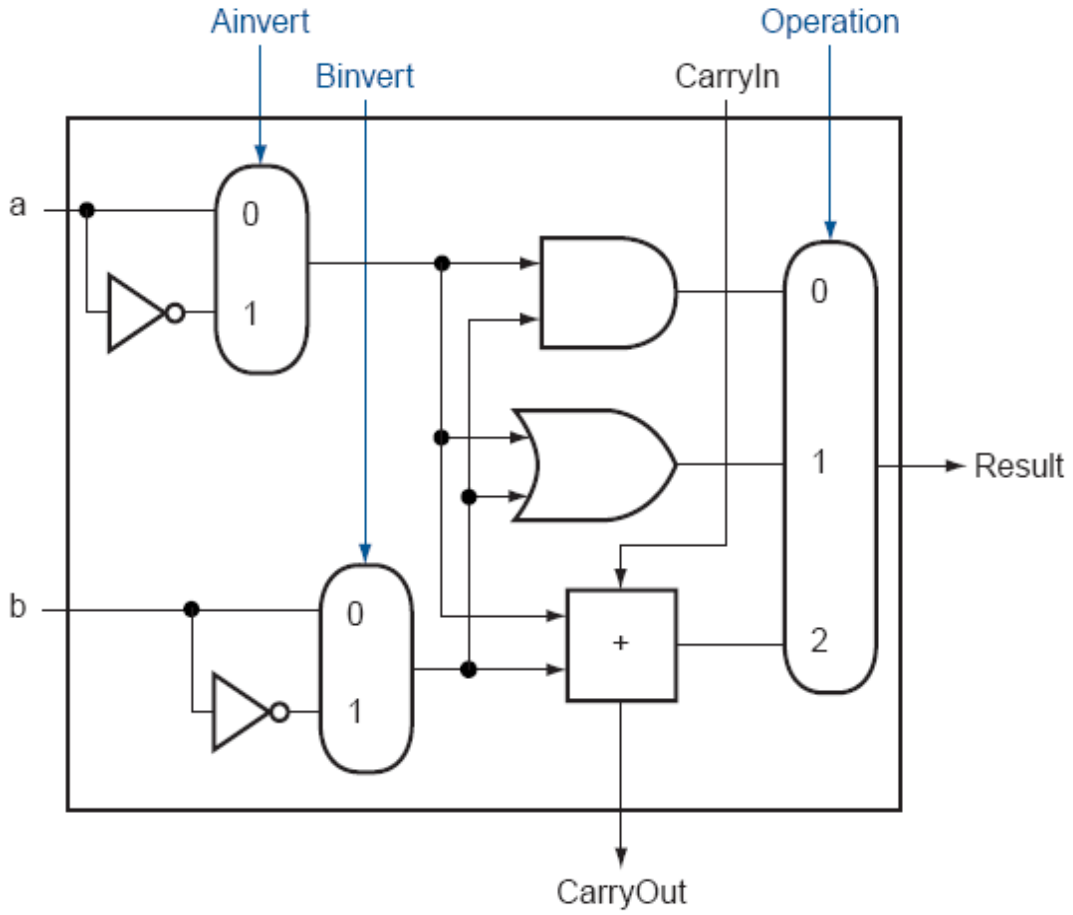
Digital Design: Sequential Logic
March 21, 2022

Ganapati Bhat
School of Electrical Engineering and Computer Science
Washington State University

Announcements

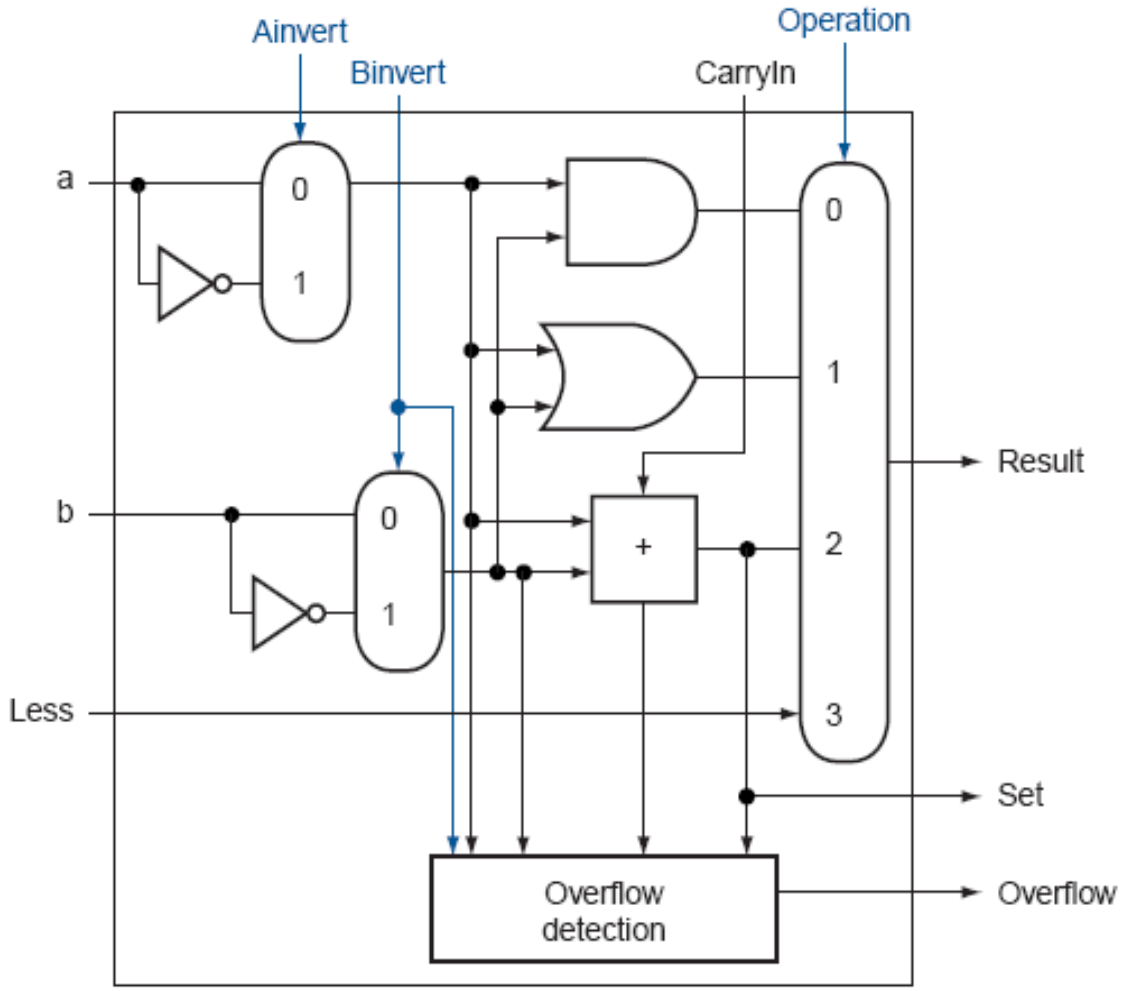
- **Mid term exam 2**
  - Friday, April 1, 2022
  - Format will be similar to exam 1
  - Tentative topics: MIPS, digital logic, single cycle MIPS implementation

Recap: Incorporating NOR

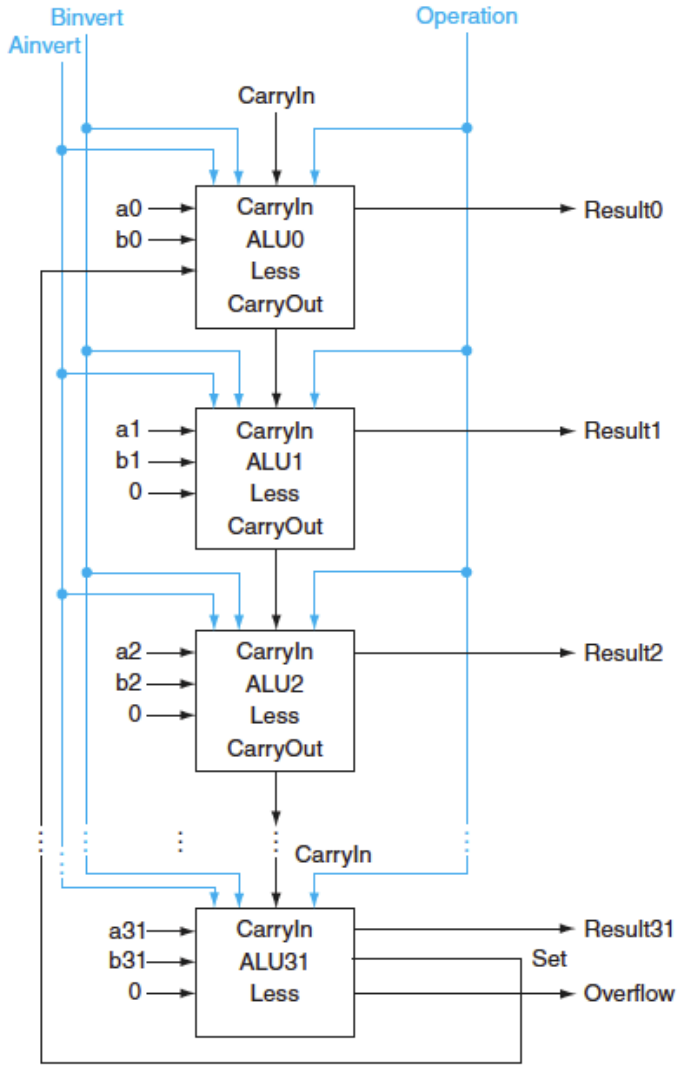


Recap: Incorporating slt

- Perform a – b and check the sign
- New signal (Less) that is zero for ALU boxes 1-31
- The 31st box has a unit to detect overflow and sign – the sign bit serves as the Less signal for the 0th box



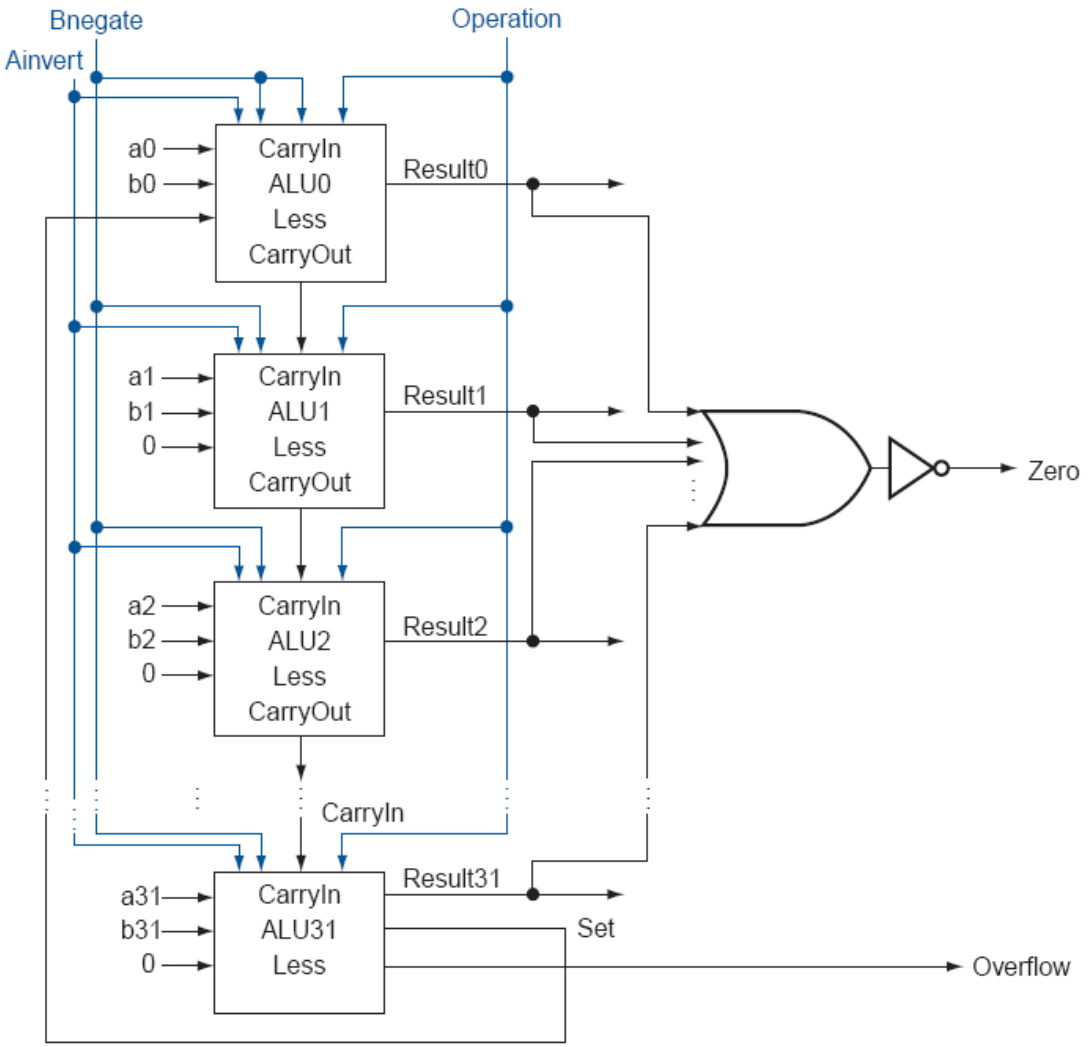
Incorporating slt



Recap: Incorporating beq

- **Perform a – b and**
  - Confirm that the
  - Result is all zero's

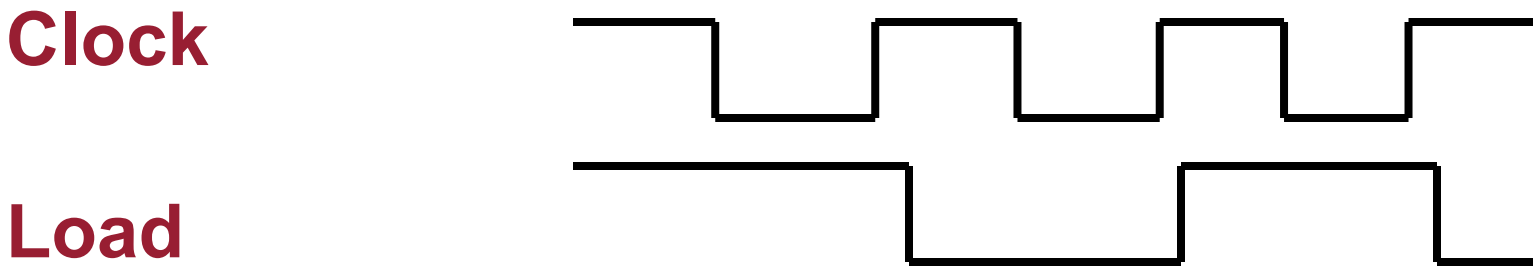
ALU control lines	Function
0000	AND
0001	OR
0010	add
0110	subtract
0111	set on less than
1100	NOR



Sequential Logic

Registers

- Register – a collection of binary storage elements
- In theory, a register is sequential logic which can be defined by a state table
- More often think of a register as storing a vector of binary values
- Frequently used to perform simple data storage and data movement and processing operations



Example: 4-bit Register

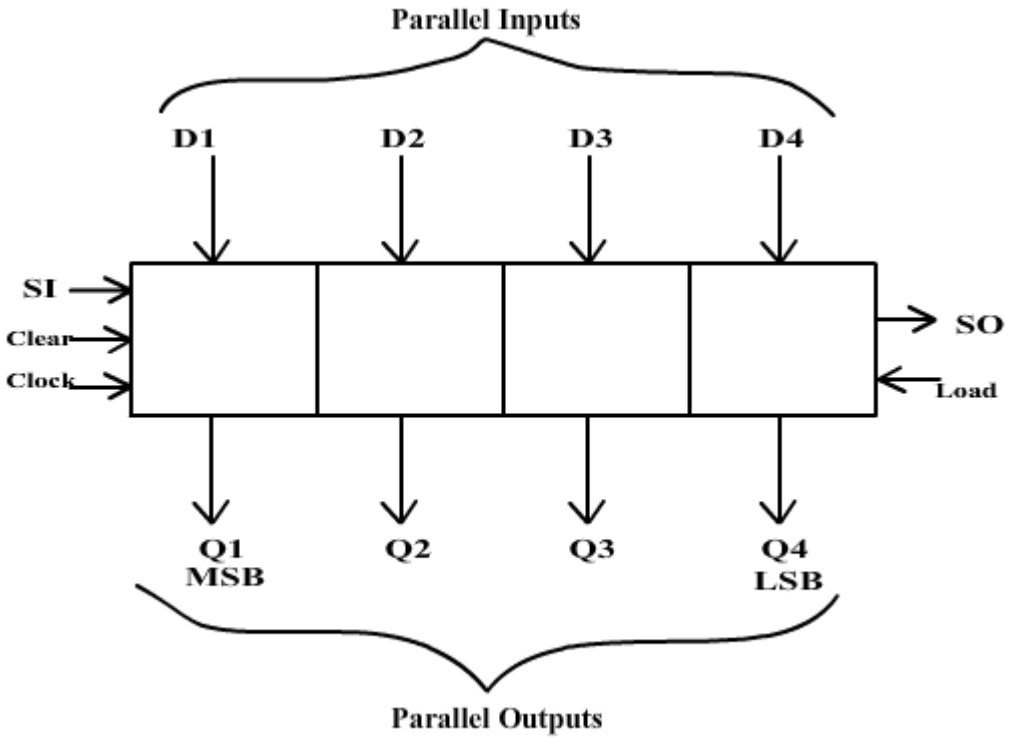
SI -> Shift In

SO -> Shift Out

Clear -> Clears the bits in register

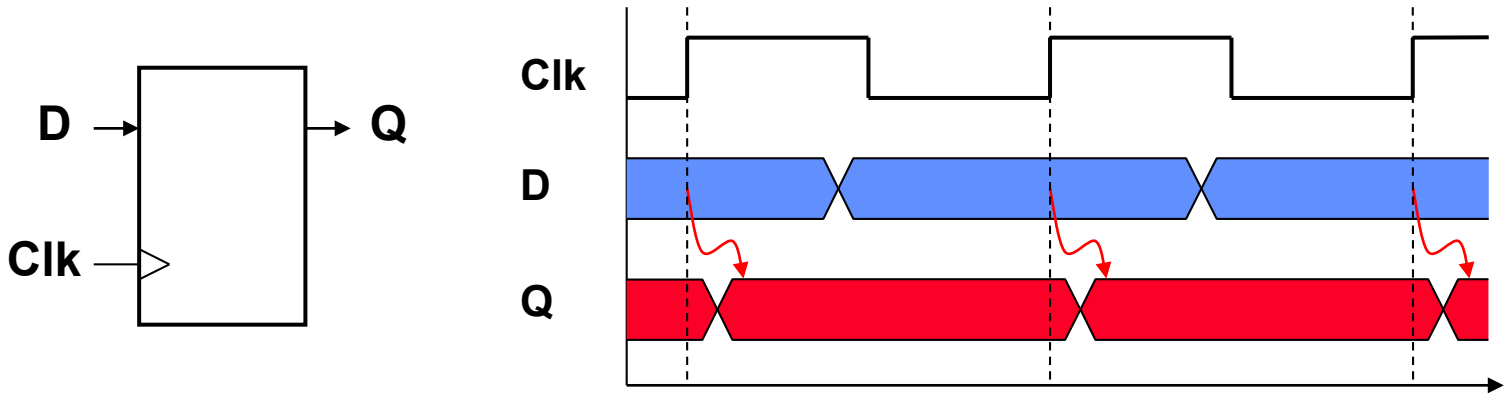
Load -> Reads the inputs into register

Clock -> Provides timing for read/writes



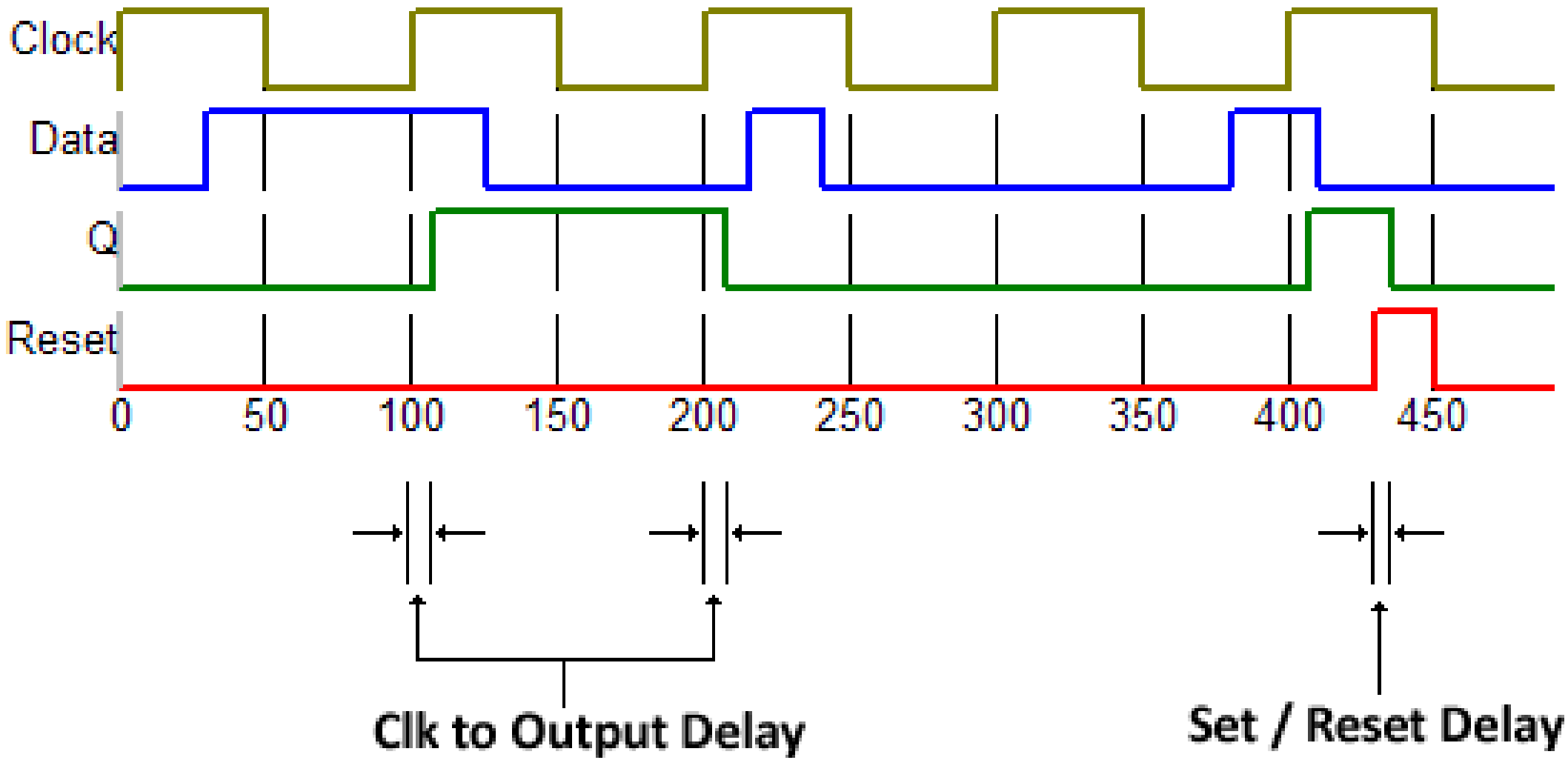
Sequential Elements

- **Flip flops: stores data in a circuit**
  - Uses a clock signal to determine when to update the stored value
  - Edge-triggered: update when Clk changes from 0 to 1



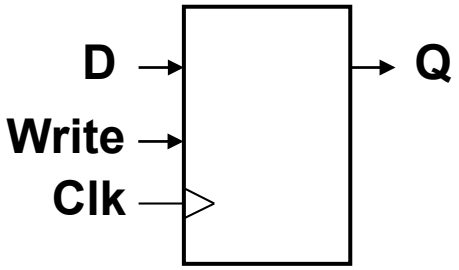
10

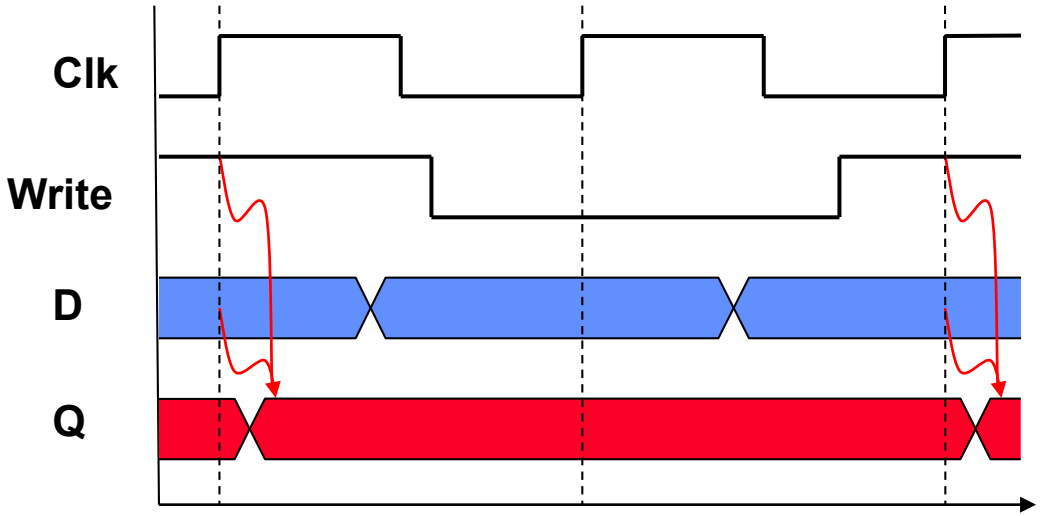
Clocking Sequence



Sequential Elements

- **Flip flop with write control**
  - Only updates on clock edge when write control input is ‘1’
  - Used when stored value is required later

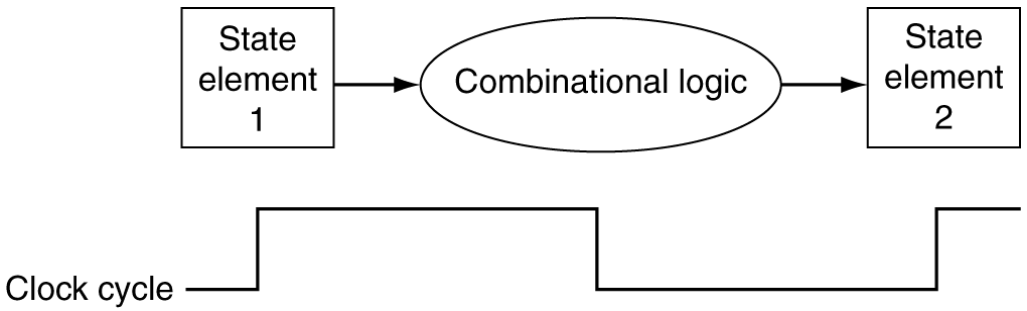


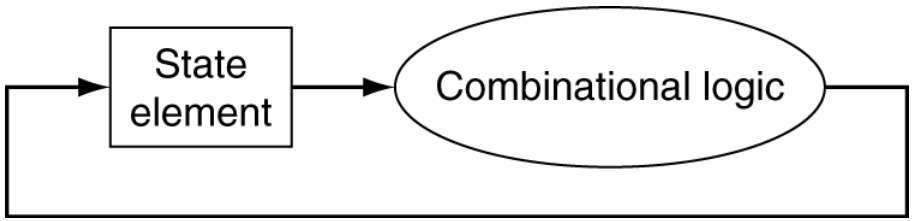


12

Clocking Methodology

- **Combinational logic transforms data during clock cycles**
  - Between clock edges
  - Input from state elements, output to state element
  - Longest delay determines clock period





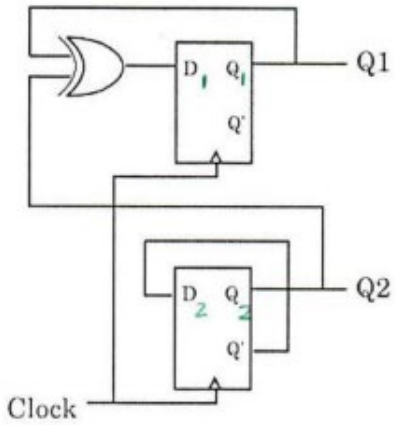
Example

5. **Sequential Logic (10 points).** The following figure shows a sequential circuit with two D Flip Flops with a common input clock. Assume that the flip flops are initialized at '0'. That is, $Q_1 = Q_2 = 0$ during Cycle 0. This means the output of this circuit is initially Q_2Q_1 = '00'.

   a. *(5 points)* Compute the value of each output signal (Q_2 and Q_1) for 8 cycles using the table below.

   b. *(5 points)* Convert the 3-bit binary Q_2Q_1 to its equivalent decimal in the table. How many unique output states (i.e., Q_2Q_1) does this circuit produce?

$$\begin{cases} D_1 = Q_1 \oplus Q_2 \\ D_2 = \overline{Q_2} \end{cases}$$



$Q_1 \times (2)^0 + Q_2 \times (2)^1$

Clock Cycle	Q_2	Q_1	Decimal ($Q = Q_2Q_1$)
0	0	0	0
1	1	0	2
2	0	1	1
3	1	1	3
4	0	0	0
5	1	0	2
6	0	1	1
7	1	1	3
8	0	0	0

Example

3. Consider the following Boolean expression:

$$F = (\bar{A} + AB)\,[(A + A)B + A\bar{B}]$$

Assume that you are allowed to use only these three gate types: NOT, 2-input AND, 2-input OR to design the digital circuit for '*F*' although you are not required to use all the three types. Furthermore, assume that the latency of each gate is 500 ps (i.e., 500 picoseconds).

a. Simplify function '*F*' as much as possible. What is the final simplified expression of '*F*'?
b. Draw equivalent digital circuit for the simplified function.
c. What is the overall latency of the simplified circuit?

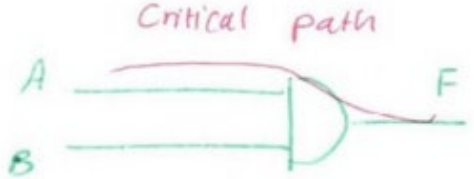
a. $F = (\bar{A} + AB)[(A + A)B + A\bar{B}] = (\bar{A} + AB)(AB + A\bar{B})$

rule $A + A = A$; rule $B + \bar{B} = 1$; $A(B + \bar{B}) = A \cdot 1$

$F = (\bar{A} + AB)(A) = A\bar{A} + AAB = AB$

rule $A\bar{A} = 0$; rule $AA = A$

b.



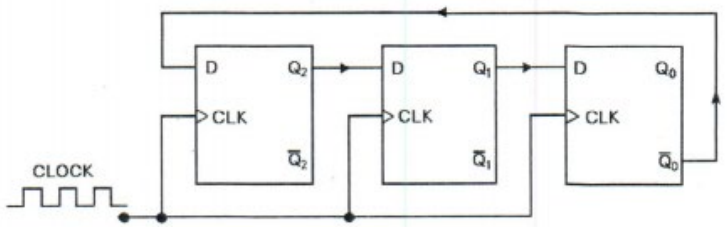
c. latency = 1 × 500 ps = 500 ps

one gate

Example

5. **Basics of Digital Design (10 points).** The following figure shows a sequential circuit with three D Flip Flops with a common input clock. Not that the inverted output of the last flip-flop ($\bar{Q}_0$) is connected to the input of the first flip-flop (D input of the far left flip flop). Assume that the flip flops are initialized at '0'. That is, $Q_2 = Q_1 = Q_0 = 0$ during Cycle 0. This means the output of this circuit is initially $Q_2Q_1Q_0$ = '000'.

   a. *(5 points)* Compute the value of each output signal (Q_2, Q_1, and Q_0) for 10 cycles using the table below.
   b. *(5 points)* Convert the 3-bit binary $Q_2Q_1Q_0$ to its equivalent decimal in the table. How many unique output states (i.e., $Q_2Q_1Q_0$) does this circuit produce?



Clock Cycle	Q_2	Q_1	Q_0	Decimal ($Q = Q_2Q_1Q_0$)
0	0	0	0	0
1	1	0	0	4
2	1	1	0	6
3	1	1	1	7
4	0	1	1	3
5	0	0	1	1
6	0	0	0	0
7	1	0	0	4
8	1	1	0	6
9	1	1	1	7
10	0	1	1	3

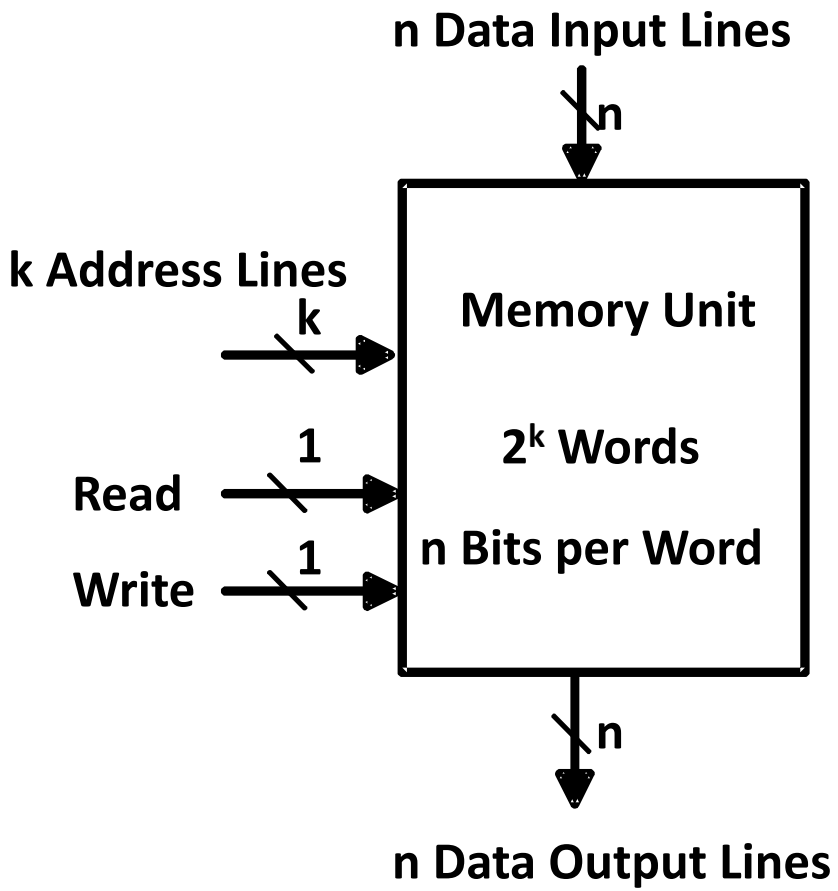
these are 6 distinct states: 0, 4, 6, 7, 3, 1

Memory Definitions

- Memory – A collection of storage cells together with the necessary circuits to transfer information to and from them.
- Memory Organization – the basic architectural structure of a memory in terms of how data is accessed.
- Random Access Memory (RAM) – a memory organized such that data can be transferred to or from any cell (or collection of cells) in a time that is not dependent upon the particular cell selected.
- Memory Address – A vector of bits that identifies a particular memory element (or collection of elements).

Memory Block Diagram

- A basic memory system is shown here:
- k address lines are decoded to address 2^k words of memory.
- Each word is n bits.
- Read and Write are single control lines defining the simplest of memory operations.



Memory Organization Example

- **Example memory contents:**
  - A memory with 3 address bits & 8 data bits has:
  - k = 3 and n = 8 so $2^3 = 8$ addresses labeled 0 to 7.
  - $2^3 = 8$ words of 8-bit data

Memory Address Binary	Decimal	Memory Content
0 0 0	0	1 0 0 0 1 1 1 1
0 0 1	1	1 1 1 1 1 1 1 1
0 1 0	2	1 0 1 1 0 0 0 1
0 1 1	3	0 0 0 0 0 0 0 0
1 0 0	4	1 0 1 1 1 0 0 1
1 0 1	5	1 0 0 0 0 1 1 0
1 1 0	6	0 0 1 1 0 0 1 1
1 1 1	7	1 1 0 0 1 1 0 0