WASHINGTON STATE UNIVERSITY

CptS260: Introduction to Computer Architecture

Homework 7

School of Electrical and Computer Engineering
Spring 2022

Pipeline

1. Consider the processor with a five stage pipeline with delays listed in Table 1.

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

Table 1. Delay of each stage in the pipeline

And assume that instructions percentage for each type is as follows:

ALU	BEQ	LW	SW
45%	20%	20%	15%

Table 2. Instructions' percentage

a. What is the clock cycle for this processor with five stage pipeline? If use this stages in a non-pipeline design, what is the clock cycle?(ignore the delay of registers between different stages)

The minimum clock cycle is the maximum delay of different stages. Therefore, the clock cycle is 350ps.

b. Latency for an instruction is defined as the time that is needed for a single instruction to be executed. Calculate the latency for lw instruction in both pipeline and no-pipeline processor. Which one has a lower latency?

The latency for non-pipeline design is the summation of execution time of different stages.

$$Latency_{non-pipeline} = 250 + 350 + 150 + 300 + 200 = 1250ps$$

On the other hand, for pipeline processor, the latency is as follows:

$$Latency_{pipeline} = Num_{stages} \times Clock_{cycle} = 5 \times 350 = 1750ps$$

c. Assume that you are allowed to split a stage into two equal stages. Which one do you prefer? Why? What is the new clock cycle for this design?

To maximize the performance, the stage with the highest delay should be split. In this case, the ID stage has the highest delay, and the clock cycle would be 350ps.

2. Assume that the following code is executed on a five stage pipeline data path:

```
add     $5, $2, $1
lw      $3, 4($5)
lw      $2, 0($2)
or      $3, $5, $3
sw      $3, 0($5)
and     $7, $8, $2
```

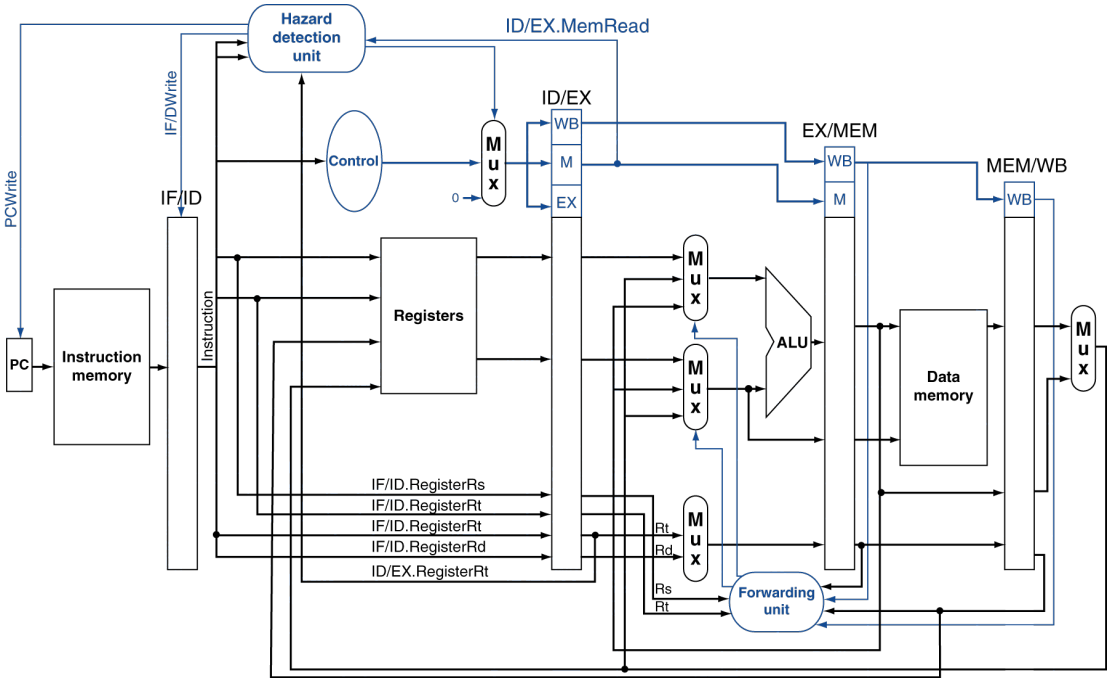

Figure 1. Pipelined MIPS with forwarding and hazard detection unit

a. If there is no forwarding and hazard detection unit, insert NOPs in the code to ensure correct operation. How many clock cycles are needed to finish this set of instructions?

We need a total of 15 cycles to finish the program.

Inst/Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ADD	IF	ID	EX	M	WB										
NOP	LW1 is waiting for register $5(WB should happen before LW1 execution)														
NOP	2 NOP is needed														
LW1				IF	ID	EX	M	WB							
LW2					IF	ID	EX	M	WB						
NOP	OR is waiting for LW1(register $3)														
OR							IF	ID	EX	M	WB				
NOP	SW is waiting for OR (register $3)														
NOP	2 NOP is needed														
SW										IF	ID	EX	M	WB	

AND											IF	ID	EX	M	WB

b. Repeat part (a) with this assumption that you can change or rearrange the instructions, and the only register that you can use in addition to the above registers is $6. How many clock cycles you will need in this case? What is the speed up compare to part (a).

Now assume that we have the forwarding unit in the design, but we don't have the hazard detection unit. What happens when this code is being executed? Explain your answer.

If we have forwarding unit, the only unresolved issue would relate to the case where an instruction is waiting for a load instruction. The hazard detection unit is still needed because it must insert a one-cycle stall whenever the load supplies a value to the instruction that immediately follows that load. Here, the code will execute correctly, as there is no dependency between load instructions and their next instructions.

3. Assume that you have a pipelined MIPS processor with 5 stage pipeline, full forwarding, and a branch prediction unit which always predicts as 'taken'. Draw the pipeline execution (multi-cycle) diagram for the following code:

```
        lw r2,0(r1)
label1: beq r2,r0,label2 # not taken once, then taken
        lw r3,0(r2)
        beq r3,r0,label1 # taken
        add r1,r3,r1
label2: sw r1,0(r2)
```

assume that there is no delay slots, and branches execute in EX stage. How many clock cycles does it take to complete the above set of instructions?

Take a reference to Exercise 4.14 (page 365) in the textbook.

Inst/Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LW1	IF	ID	EX	M	WB										
BEQ1	X	X	IF	ID	EX	M	WB								
SW				IF	ID	EX	M	WB							
LW2						IF	ID	EX	M	WB					
BEQ2						X	X	IF	ID	EX	M	WB			
BEQ1									IF	ID	EX	M	WB		
SW										IF	ID	EX	M	WB	