WASHINGTON STATE UNIVERSITY

School of Electrical Engineering and Computer Science
Introduction to Computer Architecture, Fall 2016

Midterm #2
November 9, 2016
Duration: 60 minutes

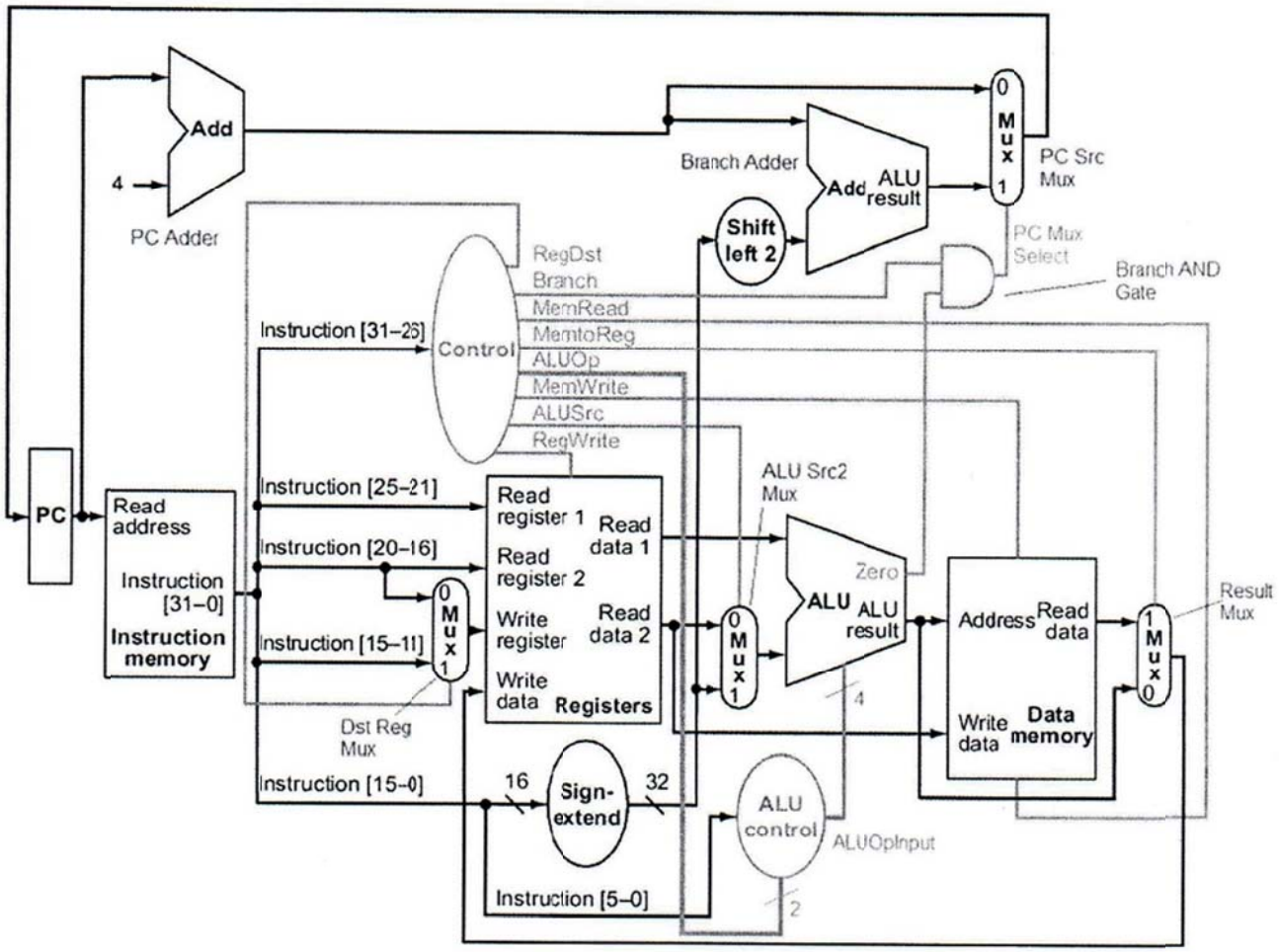
NAME: ID:

	Points	Earned
Problem 1	40	
Problem 2	30	
Problem 3	30	
Problem 4 (Bonus)	10	
Total	110	

Notes:

- You may bring a double-sided letter-size cheat-sheet and a calculator to the test. No other resources are allowed! In particular, NO textbook, lecture notes, internet access, smartphone usage, etc. are allowed!
- Make sure to write your name and WSU ID down on all pages.
- You may use both sides of each page if needed!
- Show your work for each question. Even if you do not know exact answer to a question, show your work to get partial credit.
- MIPS reference data is provided on the last page of this test.

1. Consider the following simple single cycle MIPS architecture, which is the same architecture discussed in the class.



a. What is the value (i.e., '0', '1', 'x') of each one of the following control signals during execution of 'ADD' instruction?

RegDst = 1
Branch = 0
MemtoReg = 0
AluSrc = 0

Jump = 0
MemRead = 0
MemWrite = 0
RegWrite = 1

b. What is the value (i.e., '0', '1', 'x') of each one of the following control signals during execution of 'J' instruction?

RegDst = 0
Branch = X
MemtoReg = 0
AluSrc = 0

Jump = 1
MemRead = 0
MemWrite = 0
RegWrite = 0

c. What is the value (i.e., '0', '1', 'x') of each one of the following control signals during execution of 'BEQ' instruction?

RegDst = X
Branch = 1
MemtoReg = X
AluSrc = 0
Jump = 0
MemRead = 0
MemWrite = 0
RegWrite = 0

d. What is the value (i.e., '0', '1', 'x') of each one of the following control signals during execution of 'SW' instruction?

RegDst = X
Branch = 0
MemtoReg = X
AluSrc = 1
Jump = 0
MemRead = 0
MemWrite = 1
RegWrite = 0

e. Assume instruction "J 1012d" is located in address 1000d (i.e., address 1000 decimal) in the instruction memory. What is the value of PC in decimal after this instruction is executed.

J address (Instruction[25-0]) : (26 bits)

J 1012d → 1012d = 00...0 1111110100 (16 bits)

We shift left the above number by 2:

16 bits: 00...0 1111110100 00

Finally, we should concatenate the four most significant bit of this value:

PC+4 = 1004d = 00...0 1111101100 (22 bits) → four most significant bits are '0000'

PC new = 000000...0 1111110100 00 = 4048d (20 bits)

f. Assume instruction "BEQ $t1, $t2, 10d" is located in address 1000d (i.e., address 1000 decimal) in the instruction memory. We also know that $t1 = 10d, and $t2 = 10d. What is the value of PC in decimal after this instruction is executed.

For BEQ, we should check the condition; if it is true (as it here), we should calculate the new value for PC using the relative PC addressing:

PC new = Sign-extend (branch address (Instruction(15-0))) << 2 + (PC old + 4) (next instruction)

branch address = 10d = 00...0 1010 (12 bits) → sign-extend → 00...0 1010 (28 bits)

shif left by 2 → 00...0 101000 (26 bits)

PC + 4 = 1004d = 00...0 1111101100 (22 bits)

PC new = 00...0 1010 + 00...0 1111101100

0 00...0 1000 0010100 = 1044d

3. Consider the following Boolean expression:

$$F = (\bar{A} + AB)\,[(A + A)B + A\bar{B}]$$

Assume that you are allowed to use only these three gate types: NOT, 2-input AND, 2-input OR to design the digital circuit for '*F*' although you are not required to use all the three types. Furthermore, assume that the latency of each gate is 500 ps (i.e., 500 picoseconds).

a. Simplify function '*F*' as much as possible. What is the final simplified expression of '*F*'?
b. Draw equivalent digital circuit for the simplified function.
c. What is the overall latency of the simplified circuit?

a. $F = (\bar{A} + AB)[(A + A)B + A\bar{B}] = (\bar{A} + AB)(AB + A\bar{B})$

rule $A + A = A$ → A

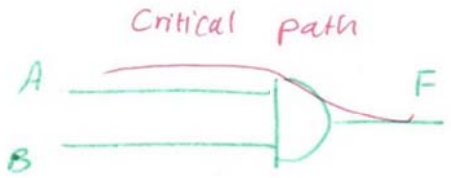
rule $B + \bar{B} = 1$ → 1

$A(B + \bar{B})$

$F = (\bar{A} + AB)(A) = A\bar{A} + AAB = AB$

rule $A\bar{A} = 0$ → 0 rule $AA = A$ → A

b.



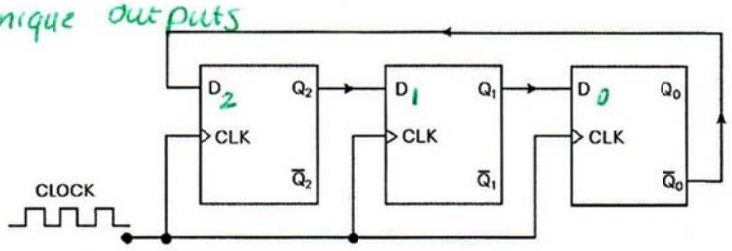
c. latency = 1 × 500 ps = 500 ps

one gate

4. **(Bonus Question)** The following figure shows a sequential circuit with three D Flip Flops with a common input clock. Note that the inverted output of the last flip-flop ($\bar{Q}_0$) is connected to the input of the first flip-flop (D input of the far left flip flop). Assume that the flip flops are initialized at '1'. That is, $Q_2 = Q_1 = Q_0 = 1$ during Cycle 0. This means the output of this circuit is initially $Q_2Q_1Q_0$ = '111'.

   a. Compute the value of each output signal (Q_2, Q_1, and Q_0) for 10 cycles using the table below.
   b. Convert the 3-bit binary $Q_2Q_1Q_0$ to its equivalent decimal in the table.
   c. How many unique output states (i.e., $Q_2Q_1Q_0$) does this circuit produce after the initial state?

6 unique outputs



$D_2 = \bar{Q}_0$

$D_1 = Q_2$

$D_0 = Q_1$

$\bar{Q}_0$ = Q_2 = Q_1

D_2	D_1	D_0	Clock Cycle	Q_2	Q_1	Q_0	Decimal ($Q = Q_2Q_1Q_0$)
0	1	1	0	1	1	1	7
0	0	1	1	0	1	1	3
0	0	0	2	0	0	1	1
1	0	0	3	0	0	0	0
1	1	0	4	1	0	0	4
1	1	1	5	1	1	0	6
0	1	1	6	1	1	1	7
0	0	1	7	0	1	1	3
0	0	0	8	0	0	1	1
1	0	0	9	0	0	0	0
1	1	0	10	1	0	0	4

* The output of each D flip flop is its input from the previous cycle *