WASHINGTON STATE UNIVERSITY

School of Electrical Engineering and Computer Science

CptS260: Introduction to Computer Architecture - Fall 2015

Midterm 2 (Duration: 60 Minutes)

November 13, 2015

NAME: Solution **ID:** (2)

Notes:

(A) This test includes 4 questions each with 25 points.
(B) You may bring a double-side letter-size cheat-sheet and a calculator to the test. No other resources are allowed! In particular, NO textbook, lecture notes, internet access, smartphone usage, …etc are allowed!
(C) Make sure to write your name and WSU ID down on all pages.
(D) You may use both sides of each page if needed!

1. The following MIPS assembly code is expected to implement the 'for' loop mentioned below. There are four mistakes in the assembly code that you need to find. Assume that the base address of array 'A' is in register $s0. Find the mistakes and write correct instruction with correct arguments for each.

```
for (i=0; i<100; i++)
{
  A[i] = 256;
}
```

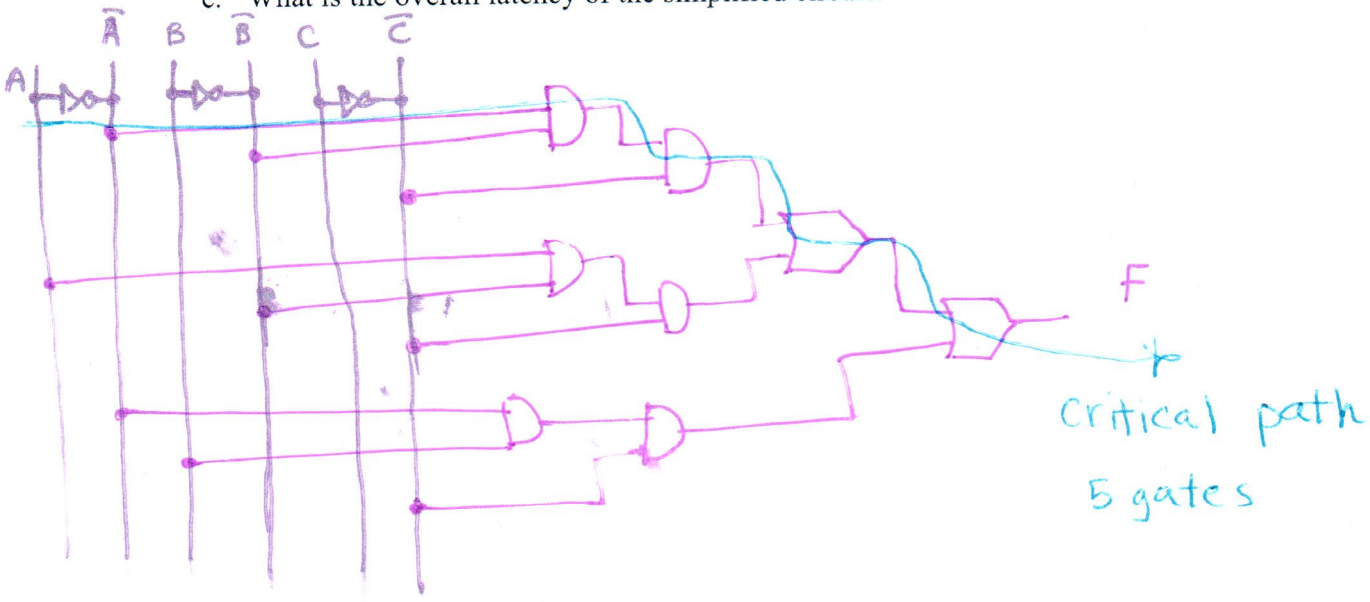
```
   li    $t0, $s0
   li    $t1, 100d
X  sll   $t1, $t1, 4      ⟶  sll  $t1, $t1, 2
   add   $t1, $t1, $s0
   ori   $t2, $zero, 256d
top:
X  sltu  $t3, $s0, $t1    ⟶  sltu  $t3, $t0, $t1
   beq   $t3, $zero, done
X  sw    $t2, 12($t0)     ⟶  sw  $t2, 0($t0)
X  addi  $t0, $t0, 1      ⟶  addi  $t0, $t0, 4
   j     top
done:
```

2. Consider the following Boolean expression:

$$F = \bar{A}\,\bar{B}\,\bar{C} + A\,\bar{B}\,\bar{C} + \bar{A}\,B\,\bar{C}$$

Assume that you are allowed to use only these gates: NOT, 2-input AND, 2-input OR to design the digital circuit for '*F*'. Furthermore, assume that the latency of each gate is 2 ns.

a. Draw equivalent digital circuit for non-simplified function '*F*'.
b. What is the overall latency of the circuit in part (a)?
c. Simplify function '*F*' as much as possible.
d. Draw equivalent digital circuit for the simplified function.
e. What is the overall latency of the simplified circuit?

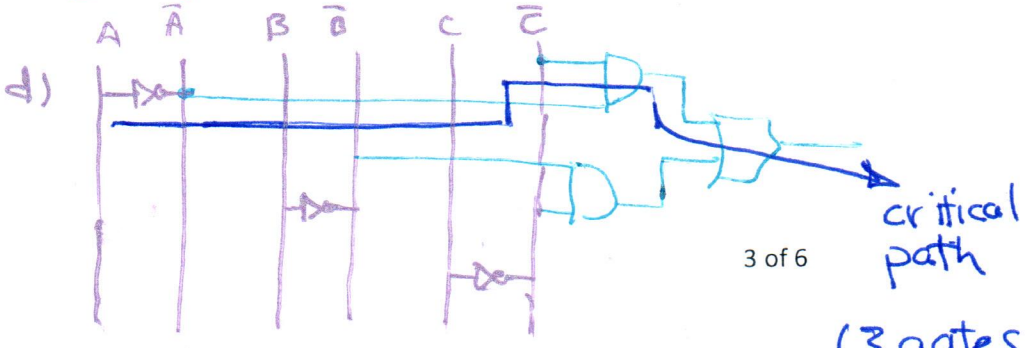


b) $5 \times 2\text{ns} = 10\text{ns}$

c) $F = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}B\bar{C} = \bar{C}(\bar{A}\bar{B} + A\bar{B} + \bar{A}B)$

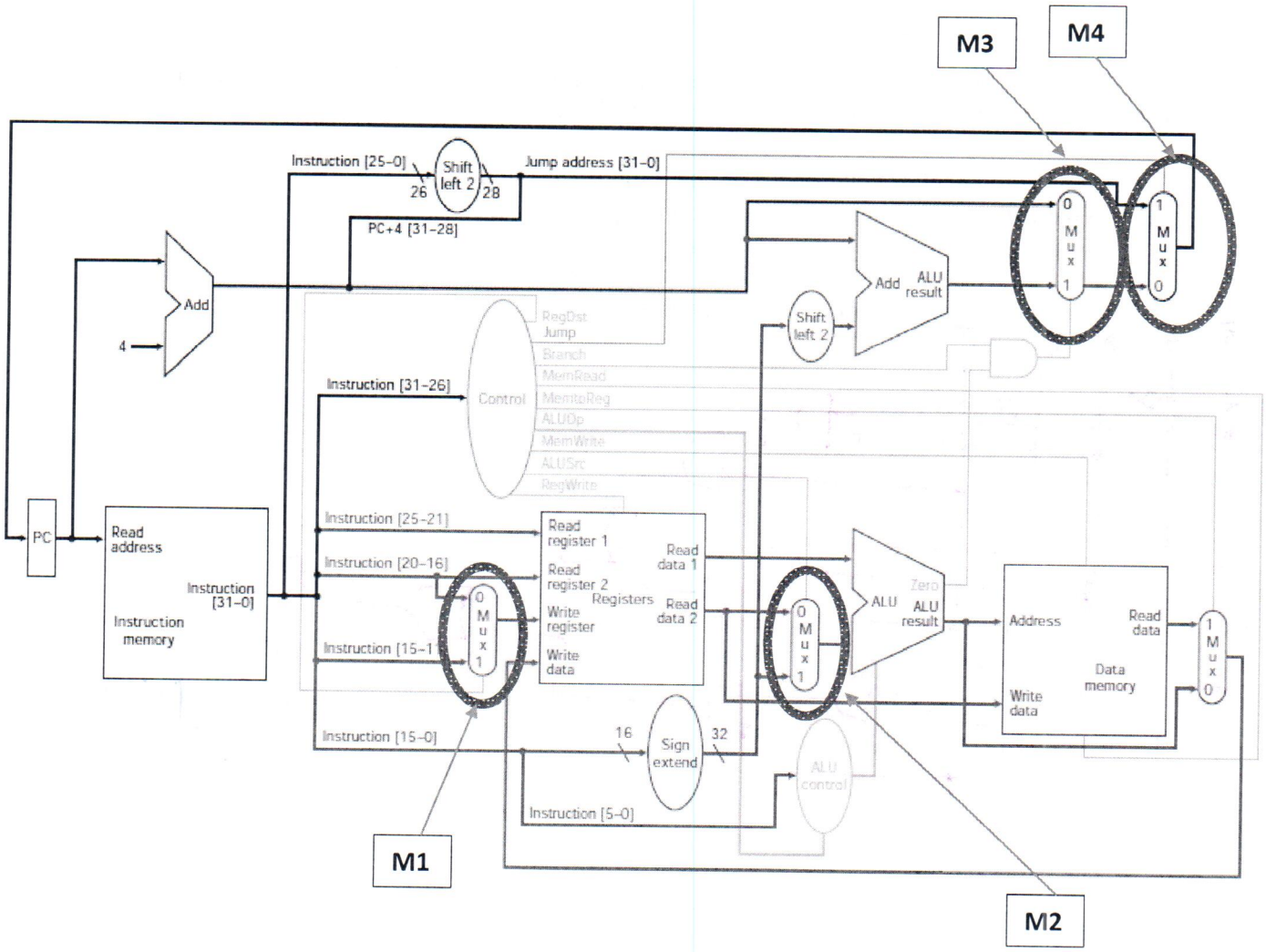
$= \bar{C}(\bar{A}(B+\bar{B}) + A\bar{B}) = \bar{C}(\bar{A} + A\bar{B}) = \bar{C}(\bar{A}+A)(\bar{A}+\bar{B})$

$= \bar{C}(\bar{A}+\bar{B}) = \bar{C}\bar{A} + \bar{C}\bar{B}$

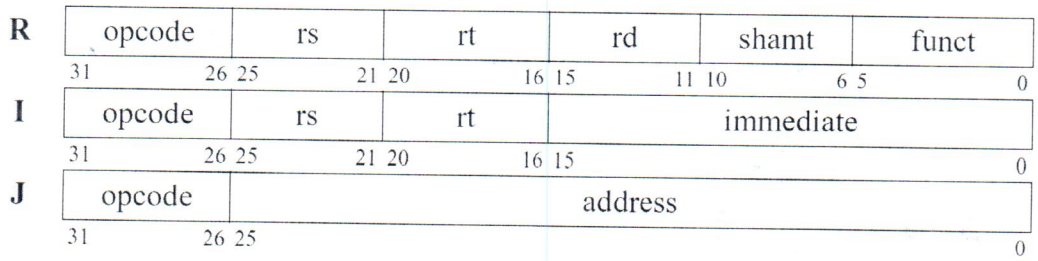


e) $3 \times 2\text{ns} = 6\text{ns}$

3. Consider the following simple single cycle MIPS architecture and instruction format, which is the same architecture discussed in the class.



Instruction Format for R-Type, I-Type, and Jump instructions



a. Assume that the following instruction is in the datapath to execute. The instruction is located in address 1000d (i.e., address 1000 decimal) in the instruction memory. We also know that $t1 = 10d, and $t2 = 24d.

BEQ $t1, $t2, 10

- What is the value of PC after this instruction is executed.
- What is the value of selection pin for each multiplexer in the datapath (0 or 1). The MUXs are labeled as M1, M2, M3, and M4.

Condition is not right ⇒ Branch is not taken ⇒

⇒ PC → PC + 4

1000d + 4d = 1004d = 1111101100 b

BEQ is an I-type Instruction

inst(25-20) = rs ⇒ M1 selection is 0

inst(20-16) = rt

ALU operation is substraction of $t1 and $t2 ⇒ M2 sel is 0

Branch is not taken ⇒ M3, M4 should take PC+4 as the next value of PC ⇒ M3, M4 sel's should be 0 (both)

b. Specify the value of each control signal listed in the following table during execution of each instruction listed in the first column.

Instruction	RegDst	Branch	MemRead	MemtoReg	MemWrite	AluSrc	RegWrite
add $9, $7, $8	1	0	0	0	0	0	1
lw $5, 10($8)	0	0	1	1	0	1	1
sw $4, 0($3)	X	0	0	X	1	1	0