WASHINGTON STATE UNIVERSITY

CptS260: Introduction to Computer Architecture

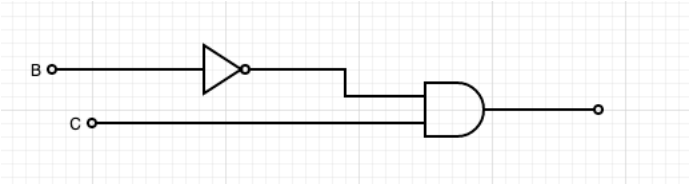
Homework 5 Solution

School of Electrical and Computer Engineering
Spring 2022

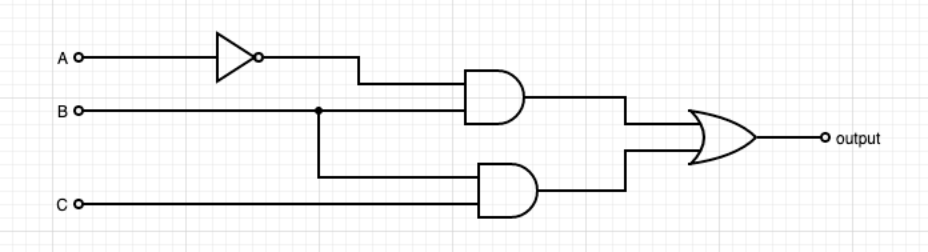
Digital Design

Answer 1:

a. $output = A'BC' + ABC' = BC'$



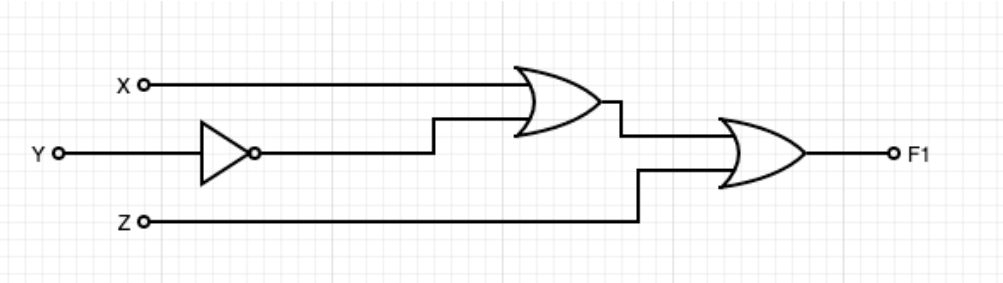
b. $output = A'BC' + A'BC + ABC = A'B + BC$



Answer 2:

a. F1 = $X + \bar{X}\bar{Y} + ZY = (X + \bar{X})(X + \bar{Y}) + ZY = X + \bar{Y} + ZY =$

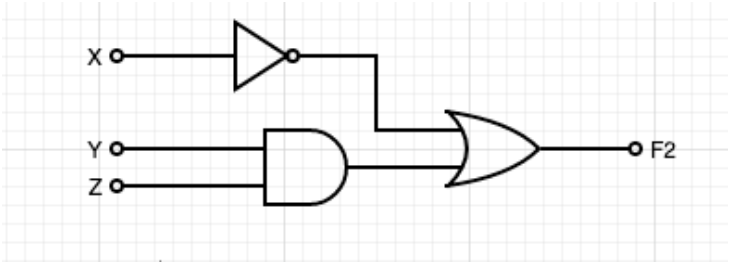
$X + (\bar{Y} + Z)(\bar{Y} + Y) = X + \bar{Y} + Z$



$$latency = 300 * 3 = 900\ ps$$

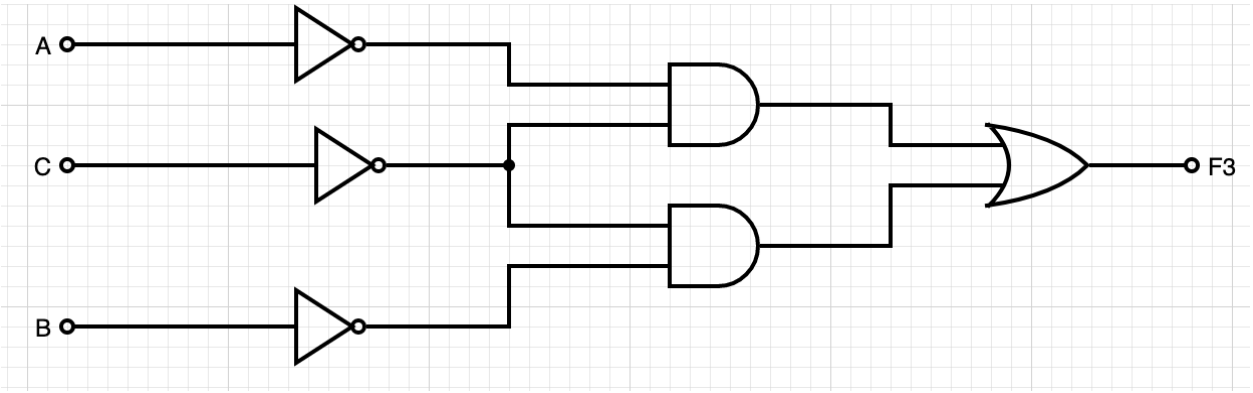
b. F2 = $\bar{X}\bar{Y} + \bar{X} + XYZ = \bar{X}(1+\bar{Y}) + XYZ = \bar{X} + XYZ =$

$(\bar{X} + X)(\bar{X} + YZ) = (\bar{X} + YZ)$



$$latency = 300 * 2 = 600\, ps$$

c. F2 = $\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}B\bar{C} = (\bar{A} + A)\bar{B}\bar{C} + \bar{A}B\bar{C} = \bar{B}\bar{C} + \bar{A}B\bar{C} = (\bar{B} + \bar{A}B)\bar{C} =$
$(\bar{B} + \bar{A})(\bar{B} + B)\bar{C} = (\bar{B} + \bar{A})\bar{C} = \bar{B}\bar{C} + \bar{A}\bar{C}$



$$latency = 300 * 3 = 900\, ps$$

Answer 3:

a1	a0	b1	b0	l	ge	eq	l(signed)	ge(signed)	eq(signed)
0	**0**	**0**	**0**	0	0	1	0	0	1
0	**0**	**0**	**1**	1	0	0	1	0	0
0	**0**	**1**	**0**	1	0	0	0	1	0
0	**0**	**1**	**1**	1	0	0	0	1	0
0	**1**	**0**	**0**	0	1	0	0	1	0
0	**1**	**0**	**1**	0	0	1	0	0	1
0	**1**	**1**	**0**	1	0	0	0	1	0
0	**1**	**1**	**1**	1	0	0	0	1	0
1	**0**	**0**	**0**	0	1	0	1	0	0
1	**0**	**0**	**1**	0	1	0	1	0	0
1	**0**	**1**	**0**	0	0	1	0	0	1
1	**0**	**1**	**1**	1	0	0	1	0	0

1	**1**	**0**	**0**	0	1	0	1	0	0
1	**1**	**0**	**1**	0	1	0	1	0	0
1	**1**	**1**	**0**	0	1	0	0	1	0
1	**1**	**1**	**1**	0	0	1	0	0	1

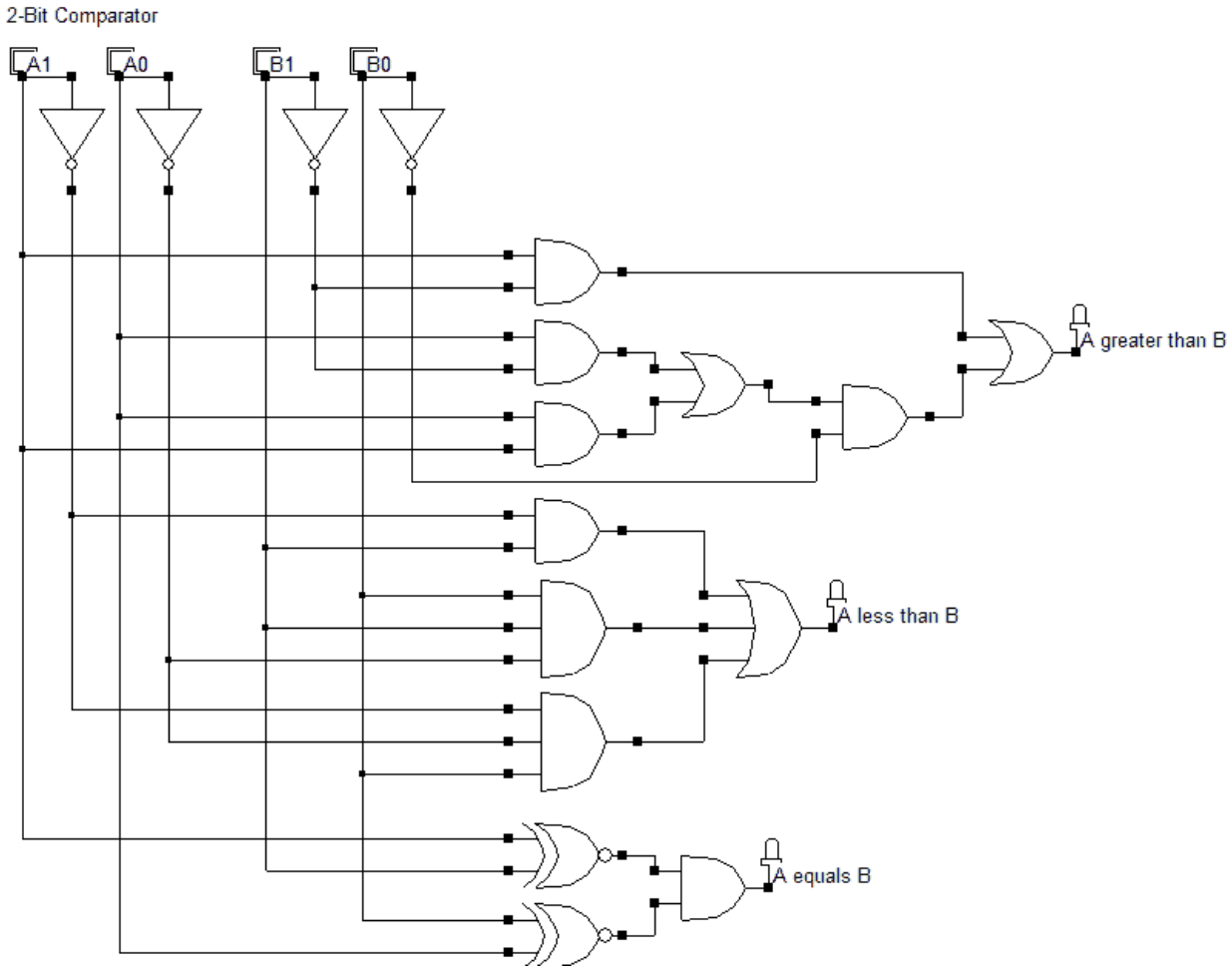
You should notice that for unsigned number, we have: 00 = 0d, 01=1d, 10=2d, 11=3d, and for signed numbers: 00 = 0d, 10 = -2d, 01= 1d, 11= -1d

The equation for l output is: $eq = \overline{a_1}\,\overline{a_0}\;\overline{b_1}\;\overline{b_0} + \overline{a_1}a_0\overline{b_1}b_0 + a_1\overline{a_0}b_1\overline{b_0} + a_1a_0b_1b_0$

We can simplify the output as: $eq = \overline{a_1}\,\overline{b_1}(\,\overline{a_0}\;\overline{b_0} + a_0b_0) + a_1b_1(\overline{a_0}\overline{b_0} + a_0b_0)$

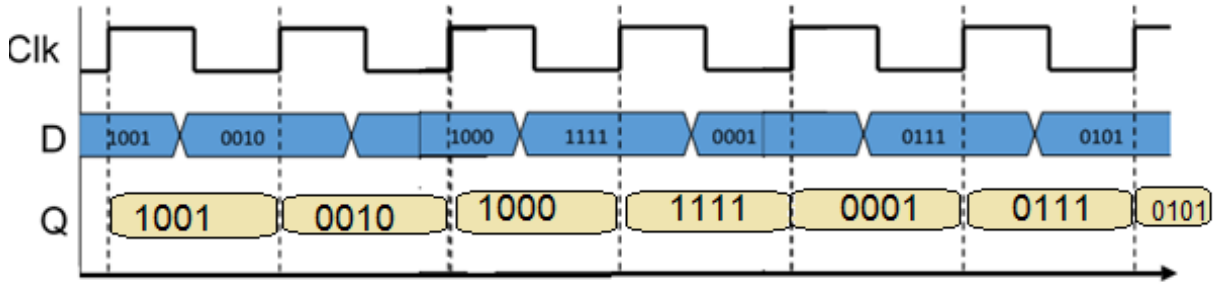
$= (\,\overline{a_0}\;\overline{b_0} + a_0b_0)\,(\overline{a_1}\;\overline{b_1} + a_1b_1)$

The two terms are XNOR gates. This is what you need to draw the circuit for outputs eq. The terms in the above equation are those that eq output is equal to one in the truth table.
You can get equation for other outputs using the same procedure. The circuit is:



Answer 4:

On each positive edge of clock output will change to the input at that moment, and it will hold the data until the next positive edge of clock even if the input changes.



Answer 5: