School of Electrical Engineering and Computer Science

CptS 260 - Introduction to Computer Architecture Fall 2019

Midterm #2 Fall 2019 **Duration:** 50 minutes

NAME: Solution

ID:

	Total Points	Earned
Problem 1	15	
Problem 2	28	
Problem 3	20	
Problem 4	15	
Problem 5	15	
Problem 6	15	5
Bonus	3	

Notes:

- You may bring a calculator to the test. No other resources are allowed! In particular, NO textbook, lecture notes, internet access, smartphone usage, etc. are allowed!
- Make sure to write your name and WSU ID down on the first page
- Show your work for each question.
- MIPS reference data is provided!

1. (15 points) Consider the following Boolean Expression:

$$F = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}B\bar{C}$$

Assume that you are allowed to use only these three gate types: NOT, 2-input AND, 2-input OR to design the digital circuit for F although you are not required to use all the three types. Furthermore, assume that the latency of each gate is 300 ps (i.e., 300 picoseconds).

Simplify function 'F' as much as possible. What is the final simplified expression of 'F'?

Draw equivalent digital circuit for the simplified function.

What is the overall latency of the simplified circuit?

a.
$$F = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C} = \overline{C}(\overline{A}\overline{B} + \overline{A}\overline{B} + \overline{A}\overline{B})$$

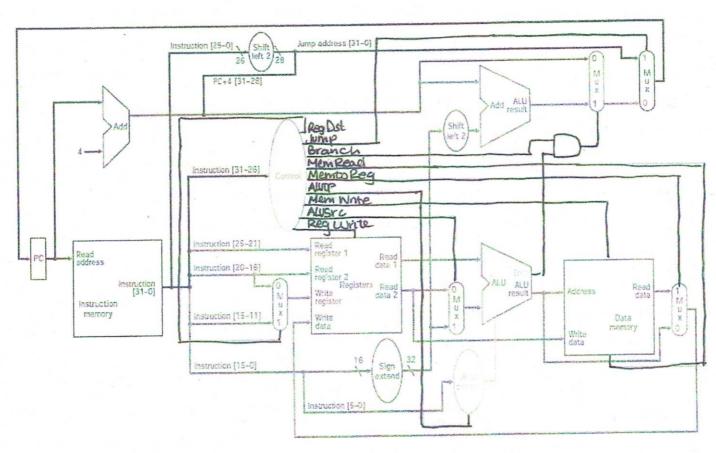
$$= \overline{C}(\overline{A}(B+B) + \overline{A}\overline{B}) = \overline{C}(\overline{A} + \overline{A}\overline{B}) = \overline{C}(\overline{A} + \overline{B})$$

$$= \overline{A}\overline{C} + \overline{B}\overline{C}$$

b) A DOTO F C DOTO F B DOTO Z

c) $3 \times 300 ps = 900 ps$

2. (20 Points) Consider the following simple single cycle MIPS architecture, which is the same architecture discussed in the class.



a. (8 pts) What is the value (i.e., '0', '1', 'x') of each one of the following control signals during execution of 'AND' instruction?

RegDst = 1
Branch =
$$O$$
MemtoReg = O
AluSrc = O

b. (8 pts) What is the value (i.e., '0', '1', 'x') of each one of the following control signals during execution of 'SW' instruction?

RegDst = X
Branch =
$$\bigcirc$$
MemtoReg = X
AluSrc = $|$

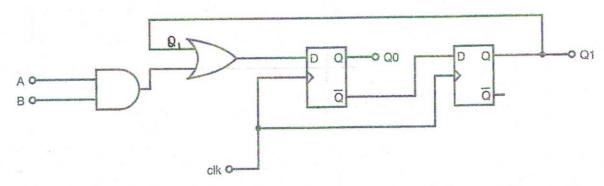
c. (8 pts) What is the value (i.e., '0', '1', 'x') of each one of the following control signals during execution of 'LW' instruction?

RegDst =
$$0$$

Branch = 0

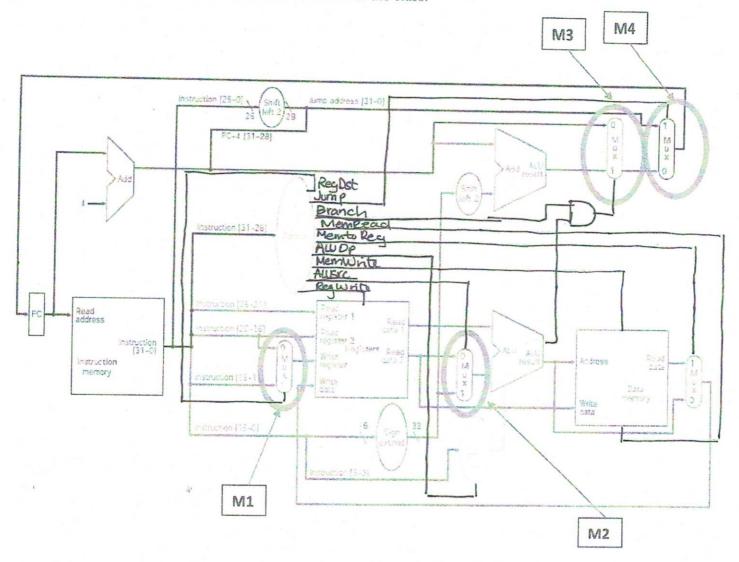
d. (4 pts) Assume instruction "AND \$t0, \$t1, \$t2" is located at address (1000)D (i.e., address 1000 in decimal) in the instruction memory. What is the value of PC in decimal after this instruction is executed?

- 3. (20 Points) The following figure shows a sequential circuit with three D Flip Flops with a common input clock. Note that the inverted output of the first flip-flop (\$\overline{Q}_0\$) is connected to the input of the second flip-flop (D input of the far right flip flop). Assume that the flip flops are initialized at '1'. That is, \$Q_1 = Q_0 = 1\$ during Cycle 0. This means the output of this circuit is initially \$Q_1Q_0 = '11'.
 - a. Compute the value of each output signal (Q1, and Q0) for 10 cycles using the table below.
 - b. Convert the 2-bit binary Q1Q0 to its equivalent decimal in the table.
 - c. How many unique output states (i.e., Q1Q0) does this circuit produce after the initial state?



Clock Cycle	A	В	Q1 Q0	Decimal (Q= Q1Q0)
0	0	1	1 1	3
1	1	1	0 1	
2	1	0	0 0	0
3	1	1	1 1	3
4	0	Q	0 1	-
5	0	0	0 0	0
6	0	1	1 0	2
7	0	1	1 1	3
8	1	1	0 1	1
9	1	1.	0 (-	1
10	0	0	0 0	O

4. (15 points) Consider the following single cycle MIPS architecture and instruction format, which is the same architecture discussed in the class.



Instruction Format for R-Type, I-Type, and Jump instructions

opcode			ΓS			rt			rd	shar	nt	funct	
31	26	25		21	20		16	15	1	1 10	6.5		0
opcode			rs			rt					ediate		
31	26	25		21	20		16	15		- 10° - 100 table (100° 10		~~~	0
opcode								a	ddress				
31	26	25		-					make past to do a su term			Application from the control and control of the con	0

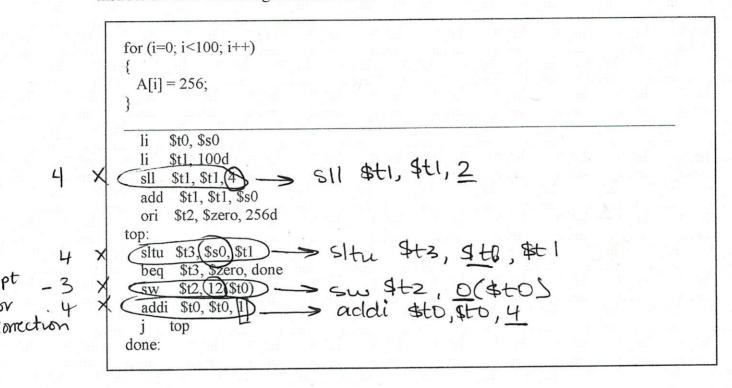
Assume that the following instruction is in the datapath to execute. The instruction is located in address (1000)p. (i.e., address 1000 decimal) in the instruction memory. We also know that t = (10)p, and t = (24)p.

BEQ \$t1, \$t2, 10.

(3)a. What is the value of PC after this instruction is executed?

b. What is the value of selection pin for each multiplexer in the datapath (0 or 1). The MUXs are labeled as M1, M2, M3, and M4.

5. (15 points) The following MIPS assembly code is expected to implement the 'for' loop mentioned below. There are four mistakes in the assembly code that you need to find. Assume that the base address of array 'A' is in register \$s0. Find the mistakes and write correct instruction with correct arguments for each.



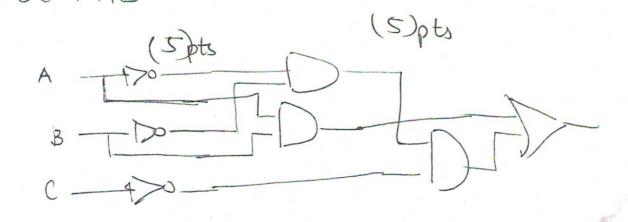
· 2 pts for emor 2 pts for correction (15 points) Write a Boolean Sum of Product (SOP) expression for this truth table, then simplify that expression as much as possible. Draw the circuits for simplified expressions.

A	B B	С	Output		
0	0	0			
0	0	1	0		
0	1	0	1		
0	1	1	. 0		
1	0	0	0		
1	0	1	0		
1	1	0			
1	1	1	1		

$$\overline{ABC} + ABC + ABC (\overline{AB+ABC}) = ABC$$

$$(S) \overline{ABC} + AB(\overline{C}+C)$$

$$\overline{ABC} + AB$$



OR 3 input AND gate for ABE.

Bonus Question: (3 points)

Mr Brown was killed on Sunday afternoon. The wife said she was reading a book. The butler said He was taking a shower. The chef said he was making breakfast. The maid said she was folding clothes, and the gardener said he was planting tomatoes. Who did it?

Boolean Expression Rules:

$$A + \bar{A} = 1$$

$$A \cdot \bar{A} = 0$$

$$\bar{\bar{A}} = A$$

$$A \cdot (A + B) = A$$

$$A + AB = A$$

$$A + \bar{A}B = A + B$$

$$A + A = A$$

$$A \cdot A = A$$

$$A \cdot 0 = 0$$

$$A + 1 = 1$$

$$A \cdot 1 = A$$

$$A + 0 = A$$