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RULES: (APPLIED WHEN POSSIBLE)

- 1.) MSB TO LSB IS TOP TO BOTTOM
- 2.) WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
- 3.) ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
- 4.) AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
- 5.) LANED SIGNALS ARE GROUPED ON SYMBOLS
- 6.) TRANSMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
- 7.) SUFFIX _V IS USED FOR VOLTAGE RAIL SIGNAL NAMES
- 8.) SUFFIX _DP AND _DN ARE USED FOR DIFFERENTIAL PAIRS
- 9.) UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
- 10.) SUFFIX _N FOR ACTIVE LOW OR N JUNCTION
- 11.) SUFFIX _P FOR P JUNCTION
- 12.) SUFFIX _EN FOR ENABLE
- 13.) 'CLK' FOR CLOCKS, 'RST' FOR RESETS
- 14.) PWRGD FOR POWER GOOD
- 15.) REV AND FAB ARE SET USING CUSTOM VARIABLES
TOOLS>OPTIONS>VARIABLES

[PAGE_TITLE=COVER PAGE]

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[56]	VREGS, V3P3
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[67]	CONN, SWITCHES
[68]	CONN, HDT
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[70]	DEBUG, CONNECTORS
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GREYBULL
REV 1.0
FAB M
RETAIL

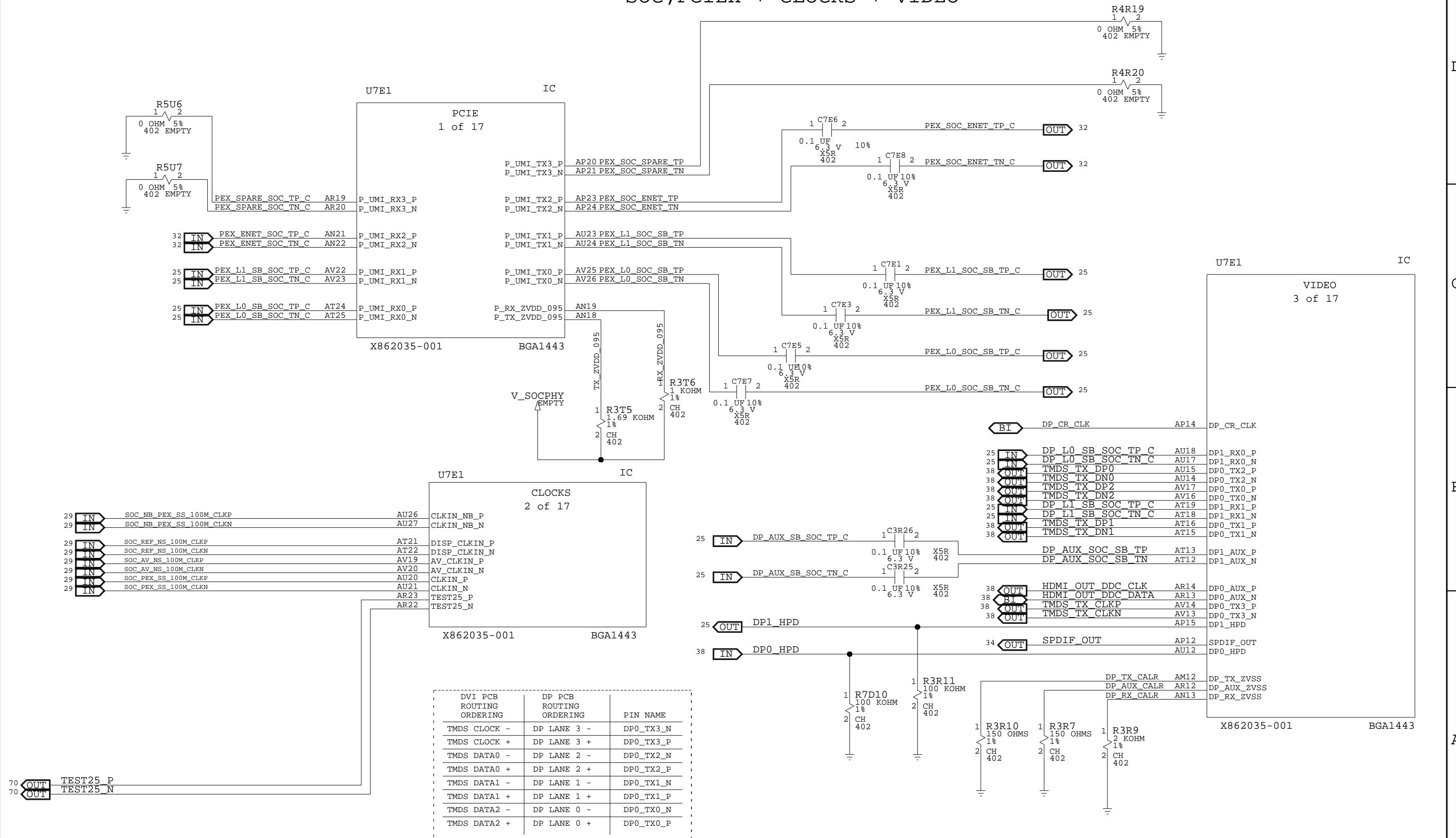
D

C

B

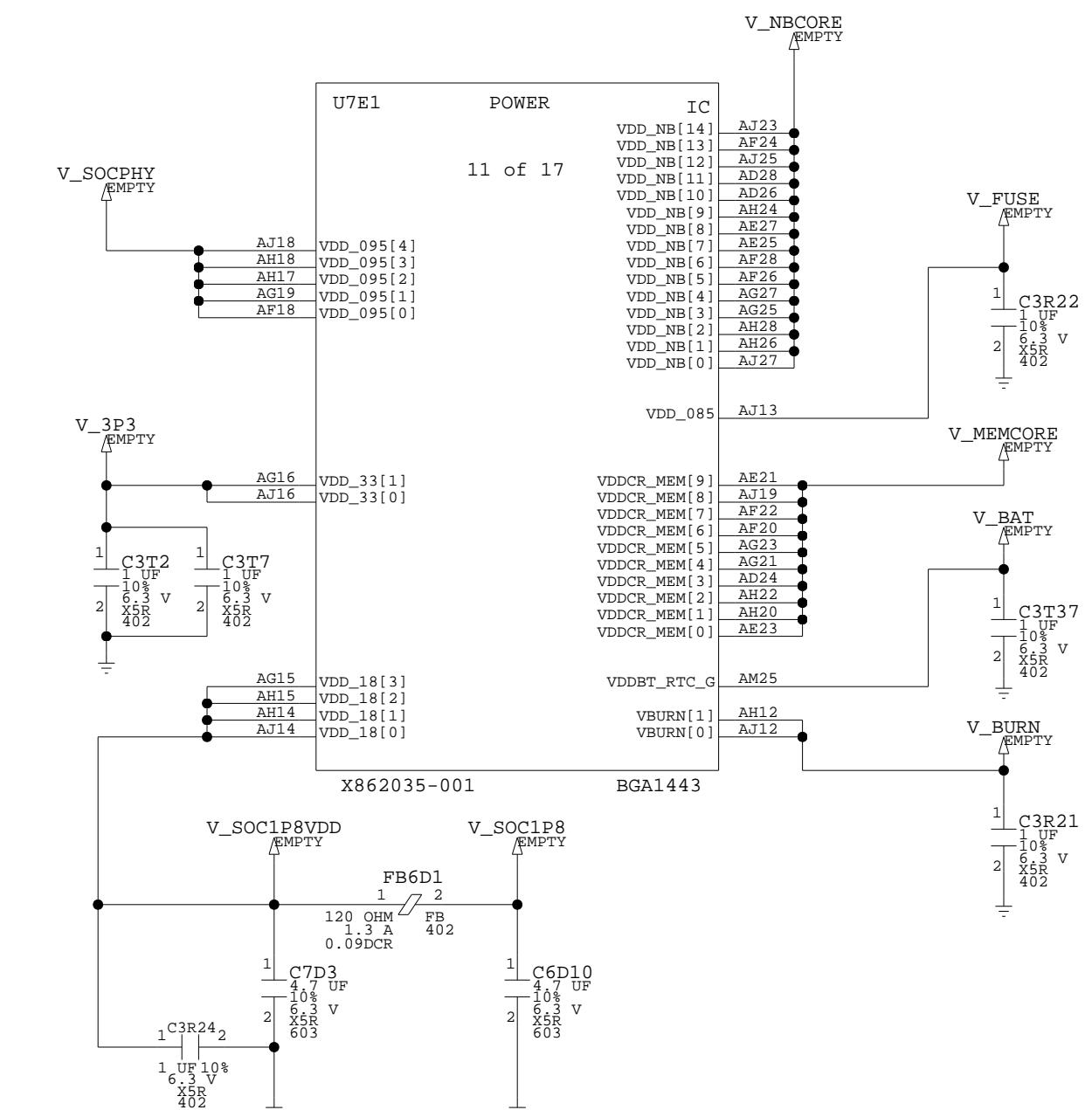
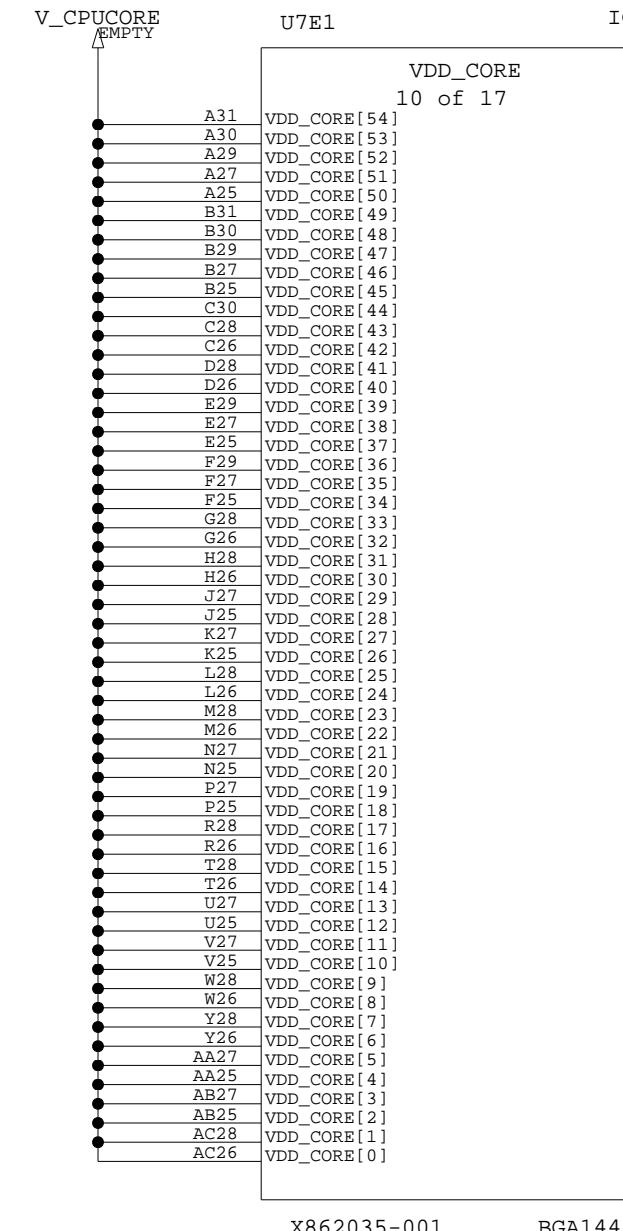
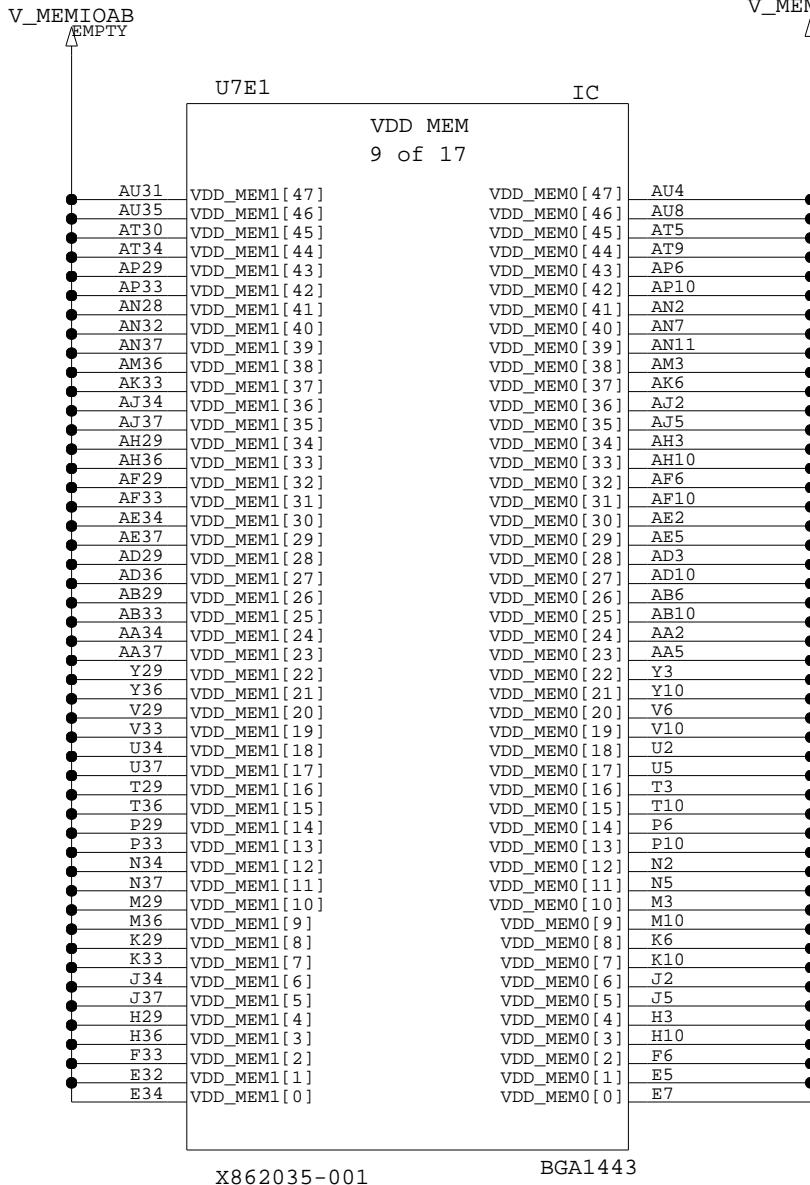
A

SOC, PCIE X + CLOCKS + VIDEO



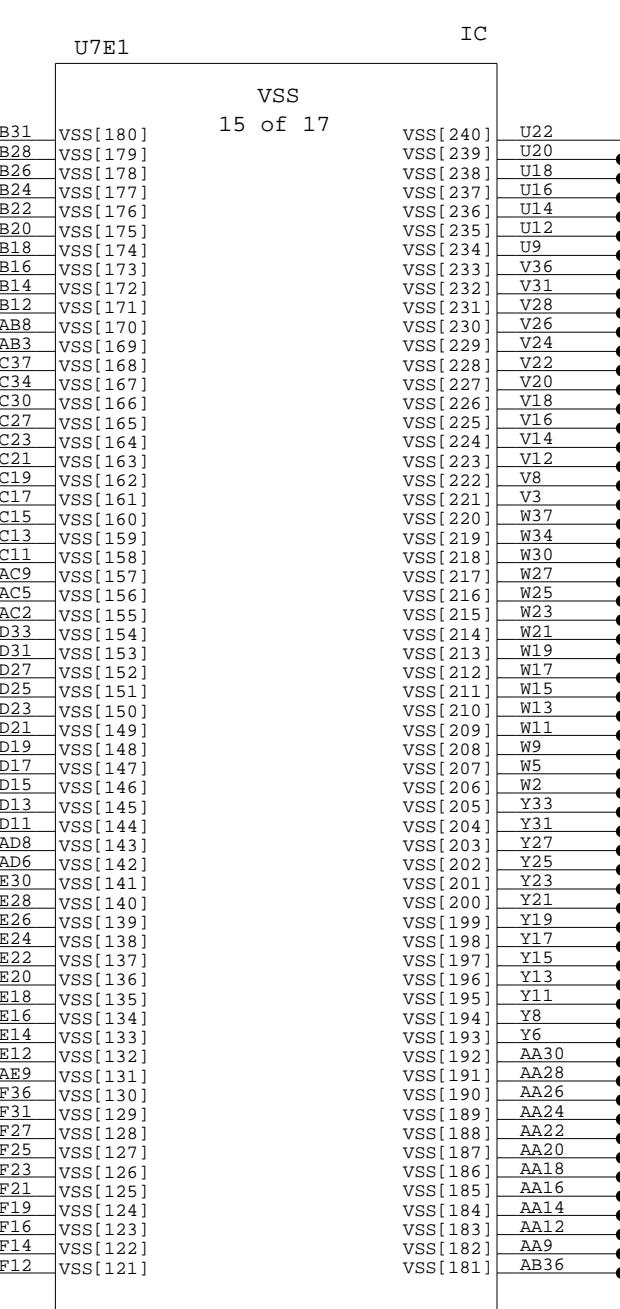
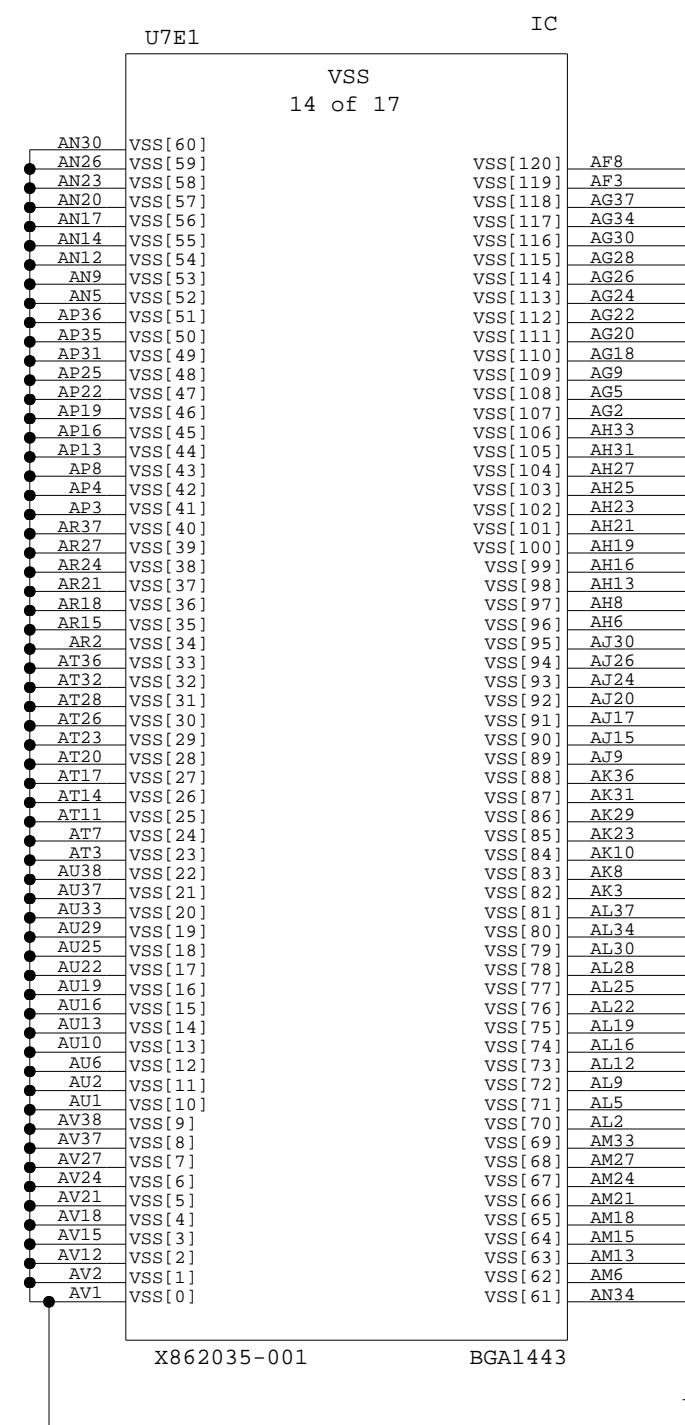
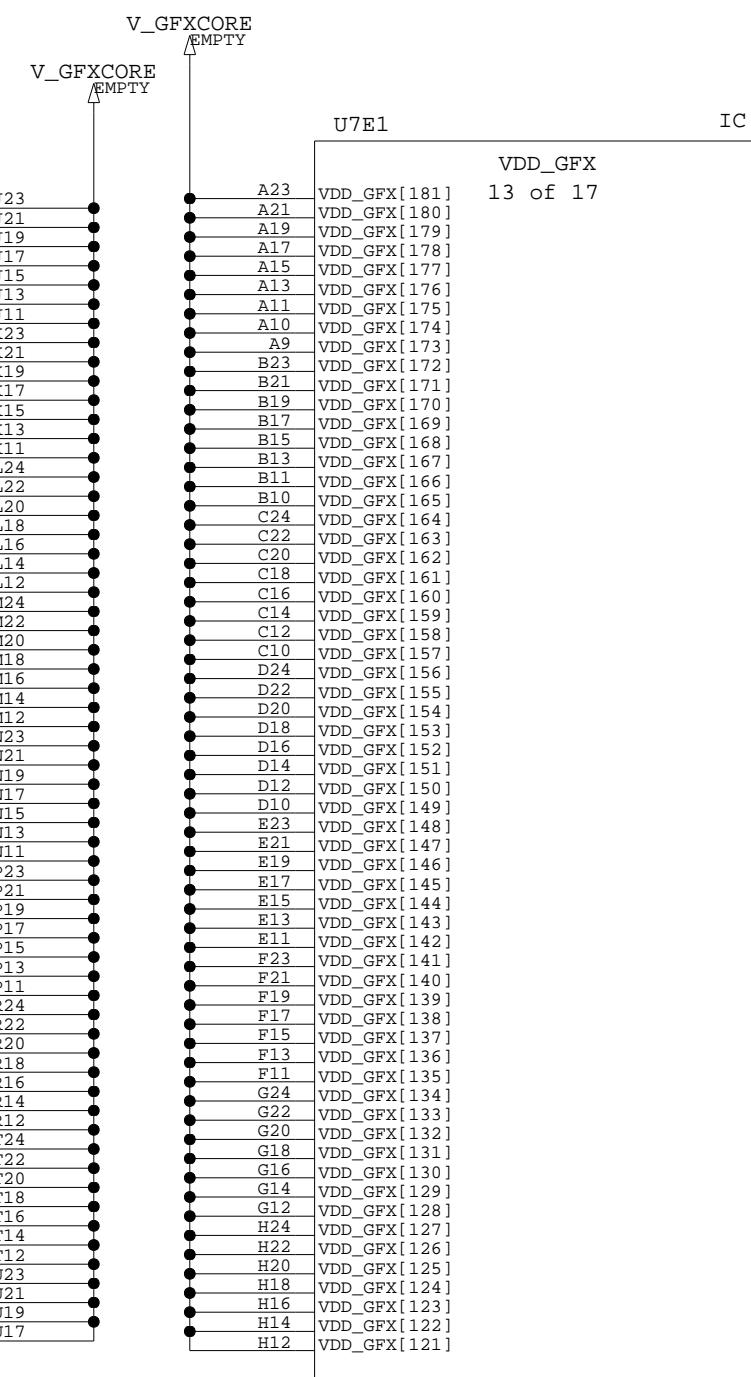
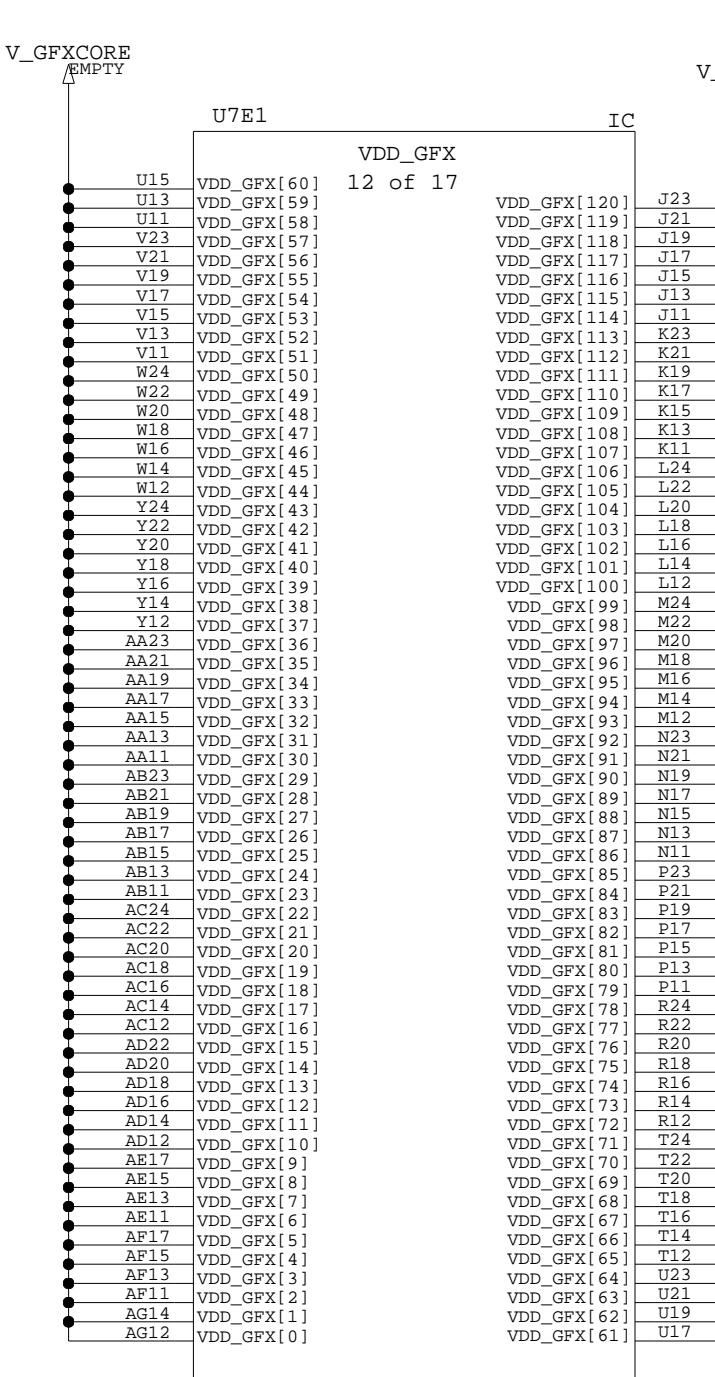
SOC POWER , MEM + CPUCORE + MEMCORE + NBCORE + MISC

D



SOC POWER , V_GFXCORE + VSS

D



SOC, MEMORY PARTITION C + D

D

C

B

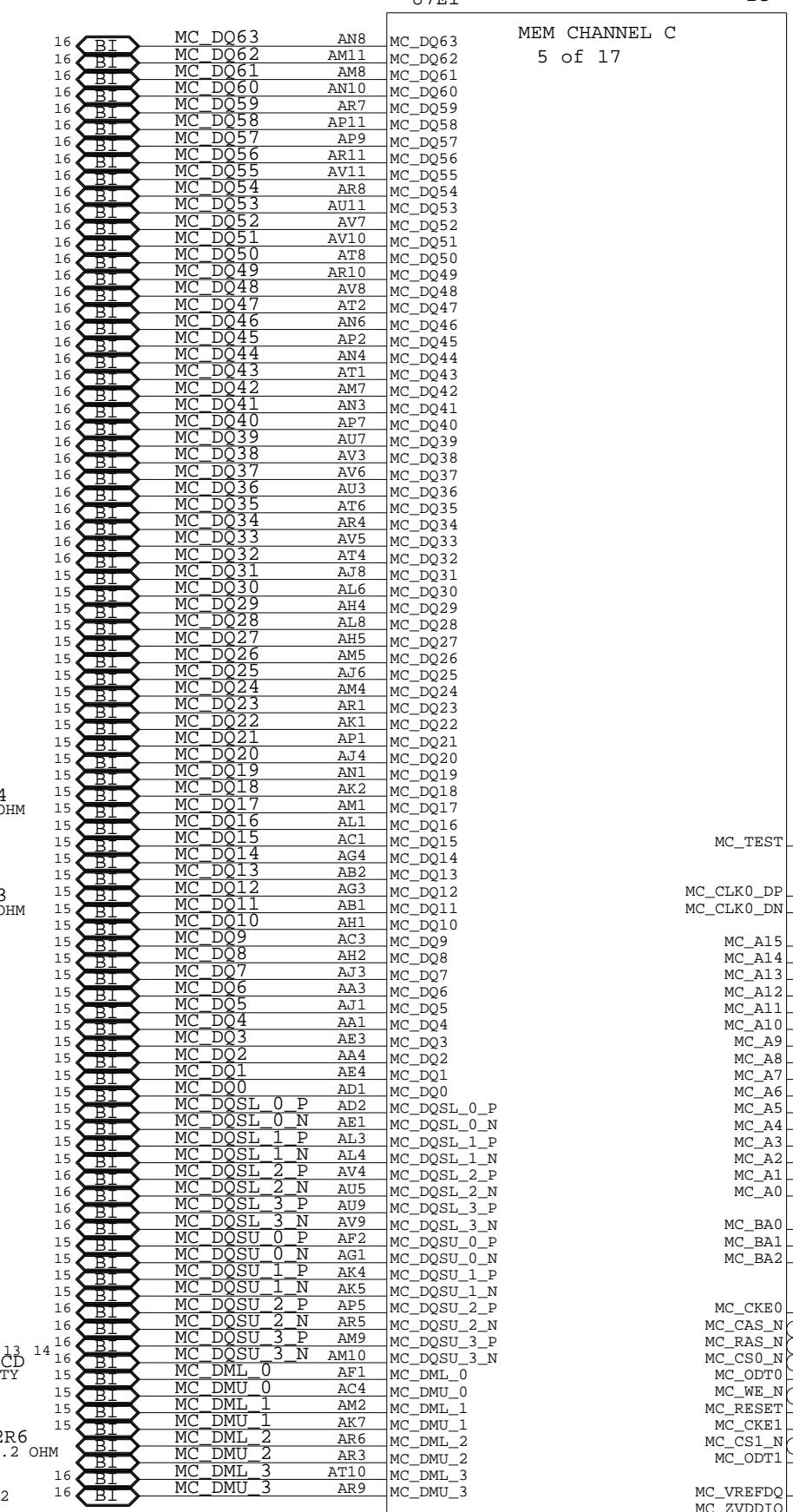
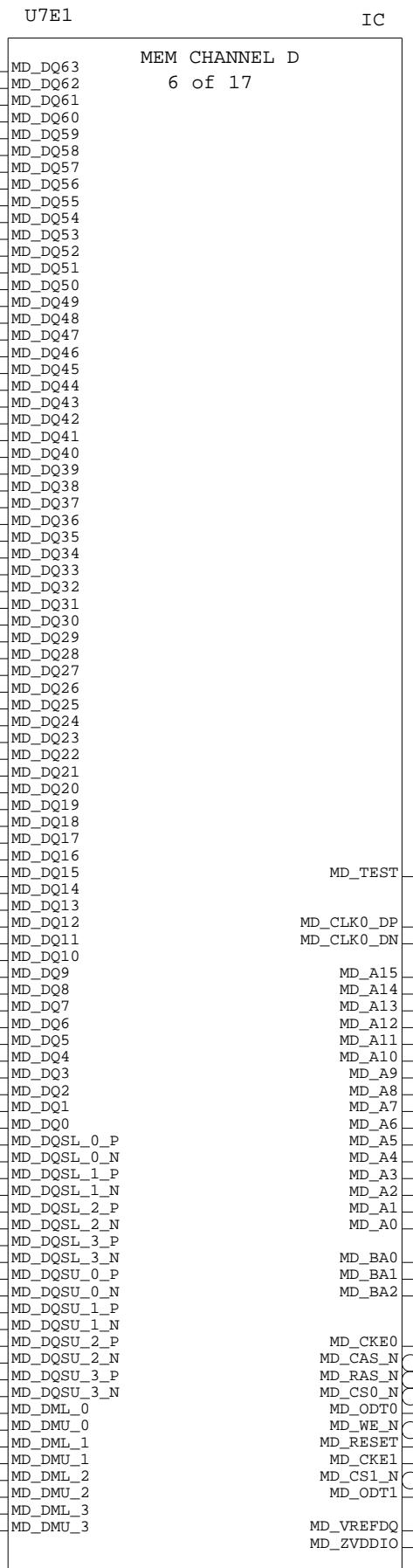
A

D

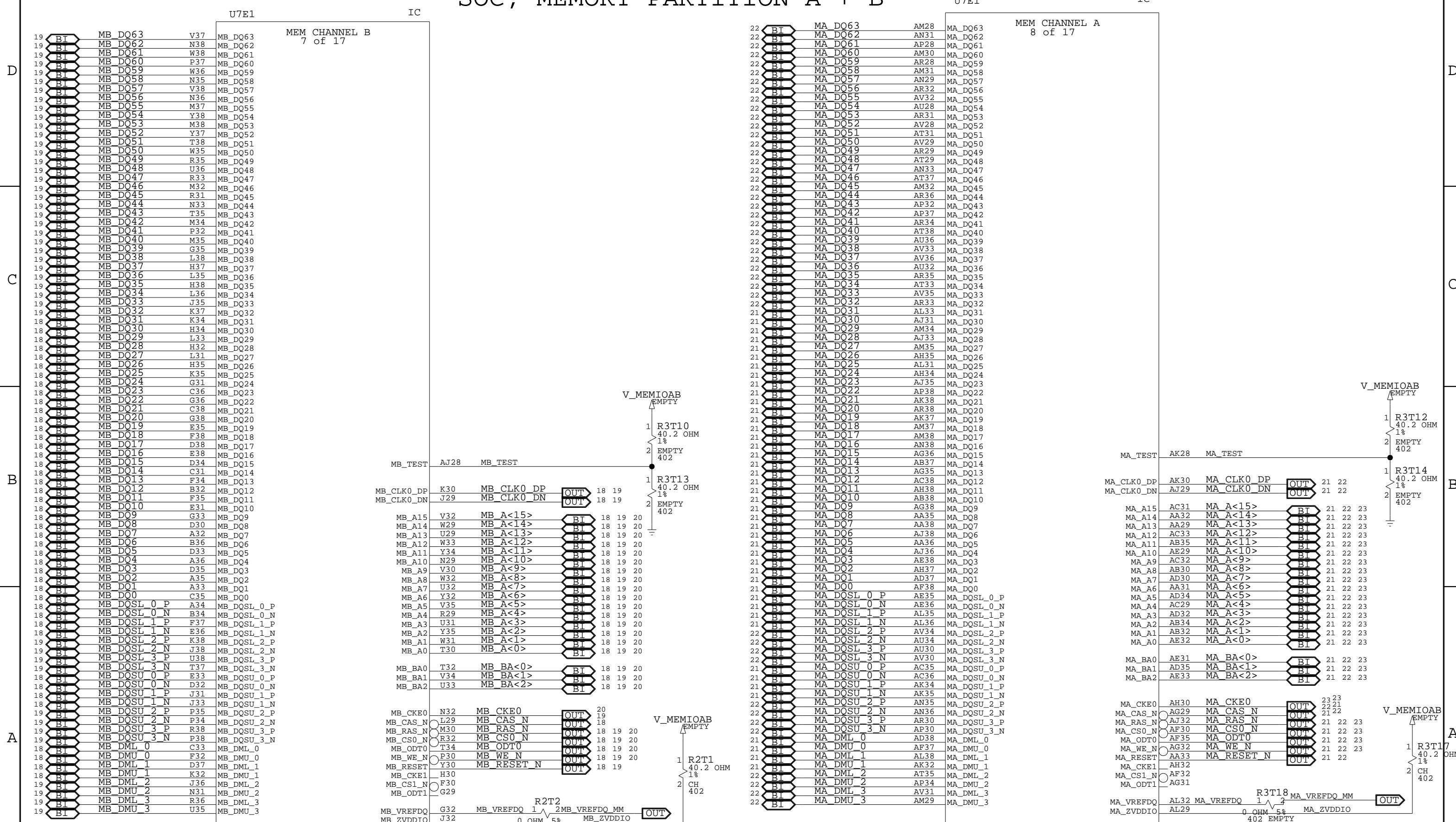
C

B

A



SOC, MEMORY PARTITION A + B



SOC VSS + SPARE

D

C

B

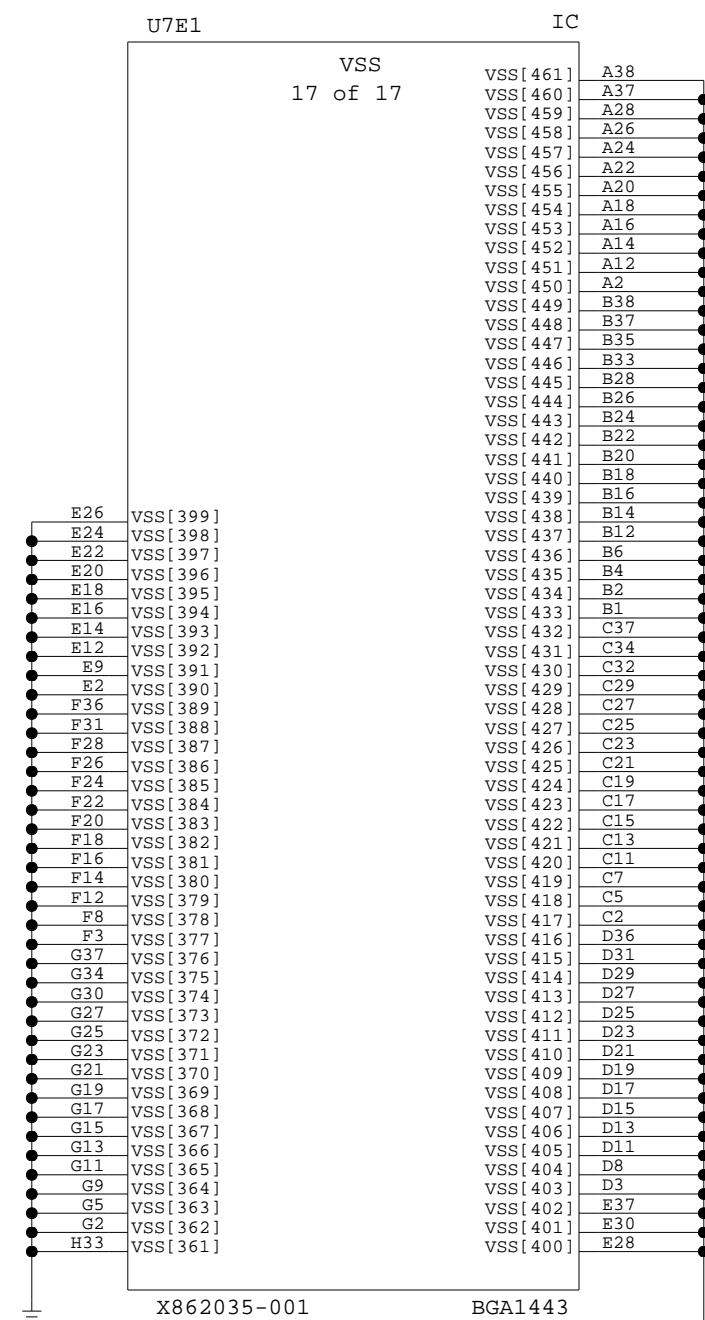
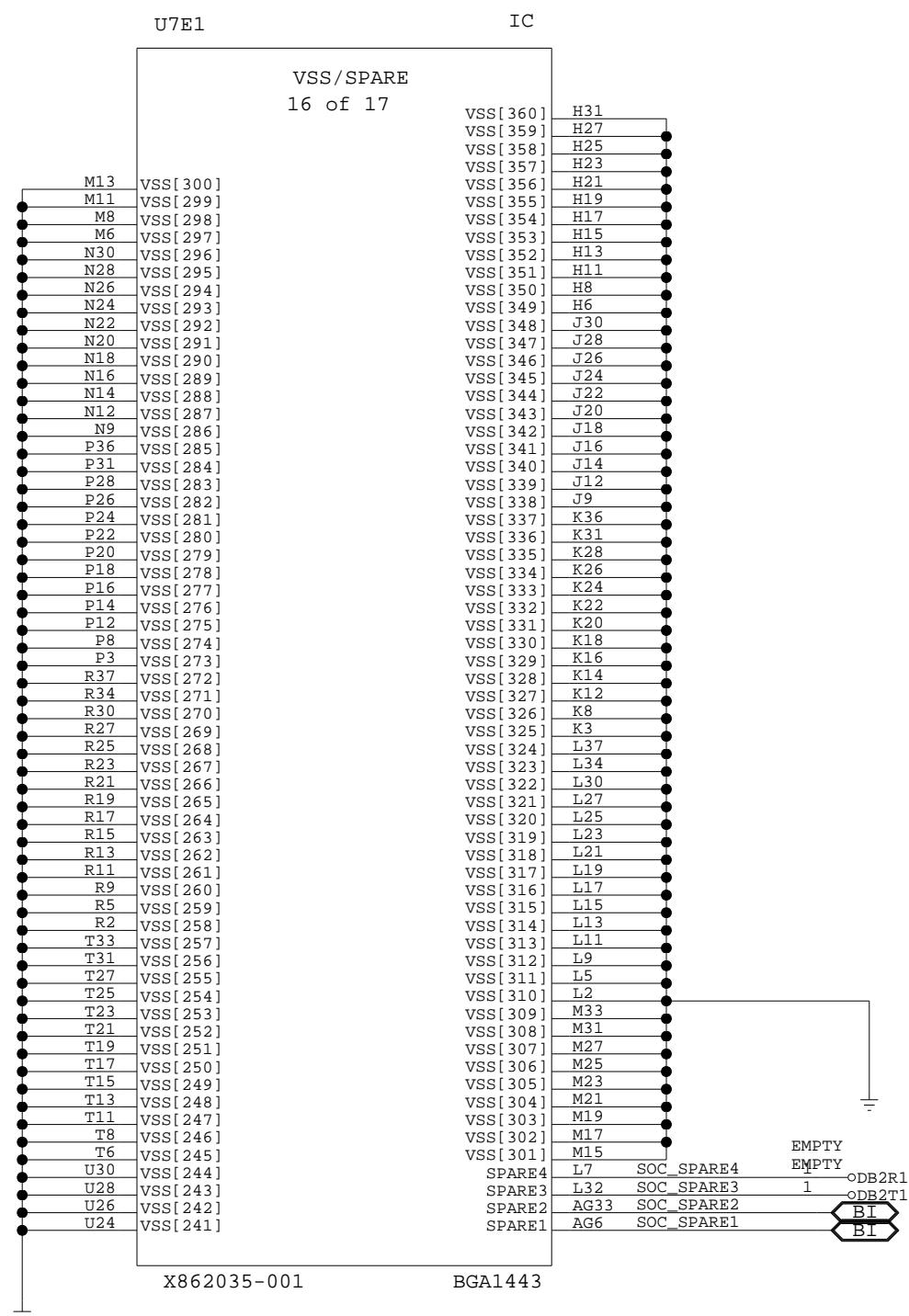
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D

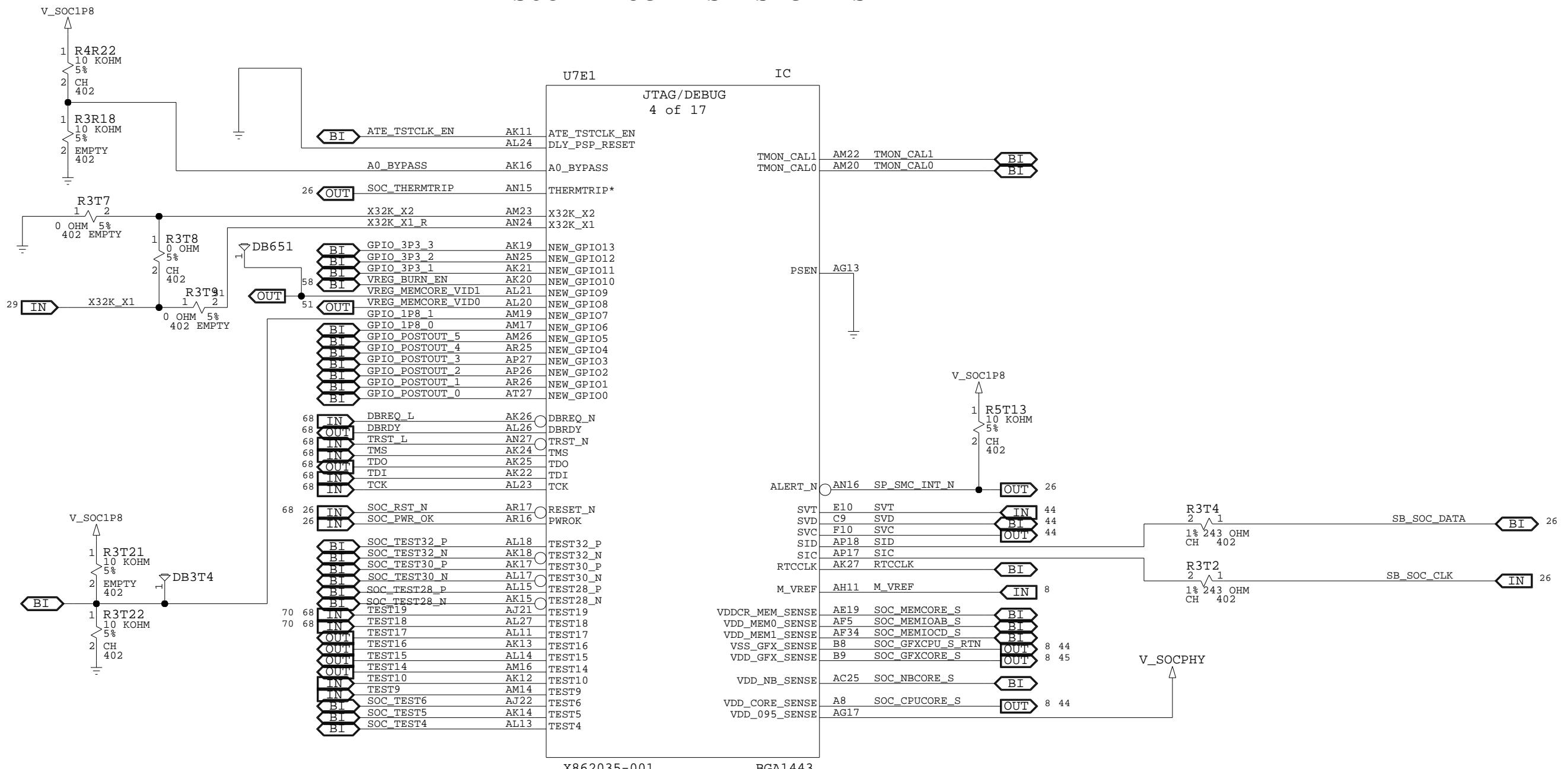
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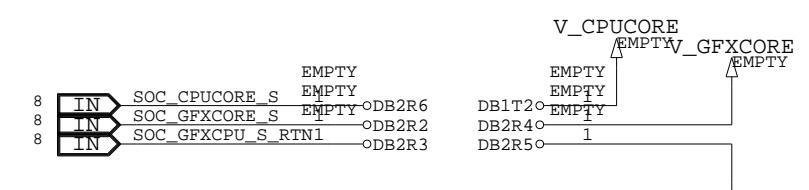
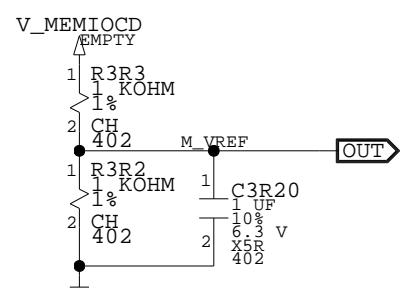
A



SOC DEBUG + SB SIGNALS



X862035-001 BGA1443

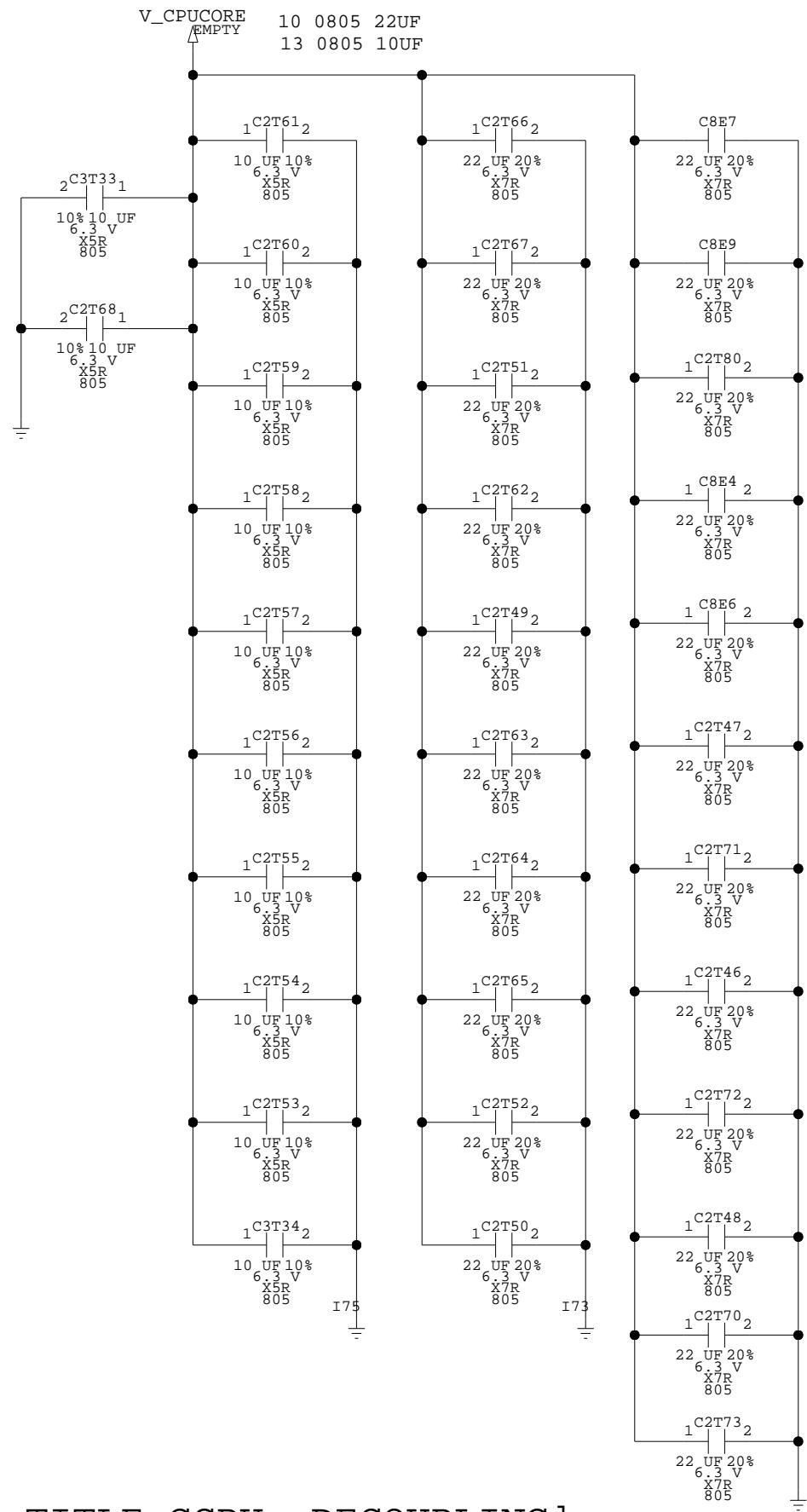


SOC, DECOUPLING

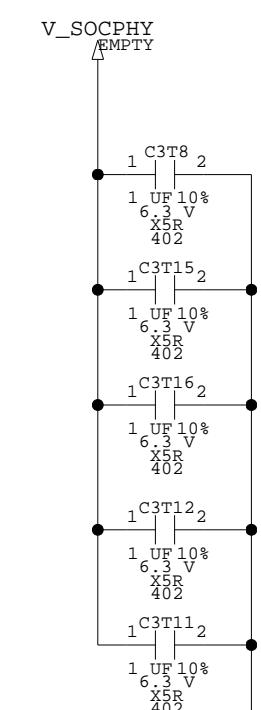


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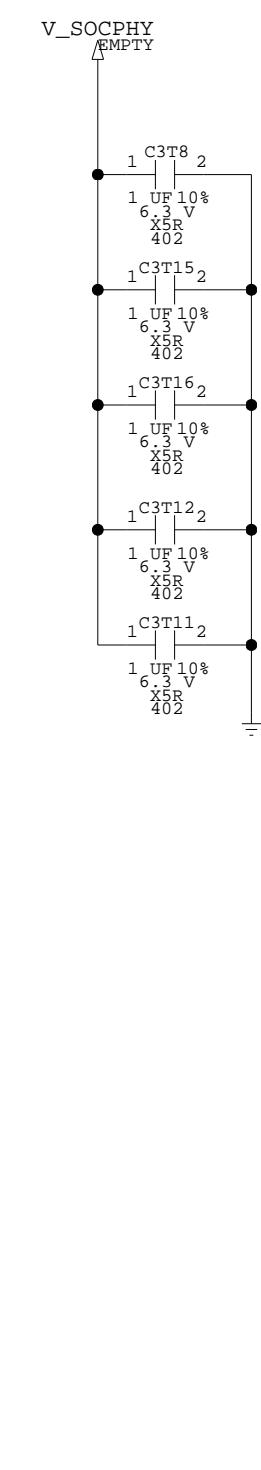
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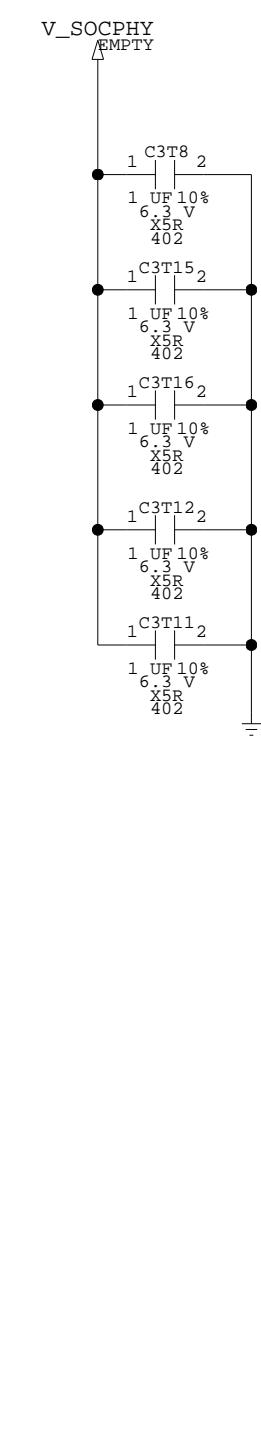
V_SOCPHY EMPTY



V_NBCCORE EMPTY



V_MEMCORE EMPTY



C

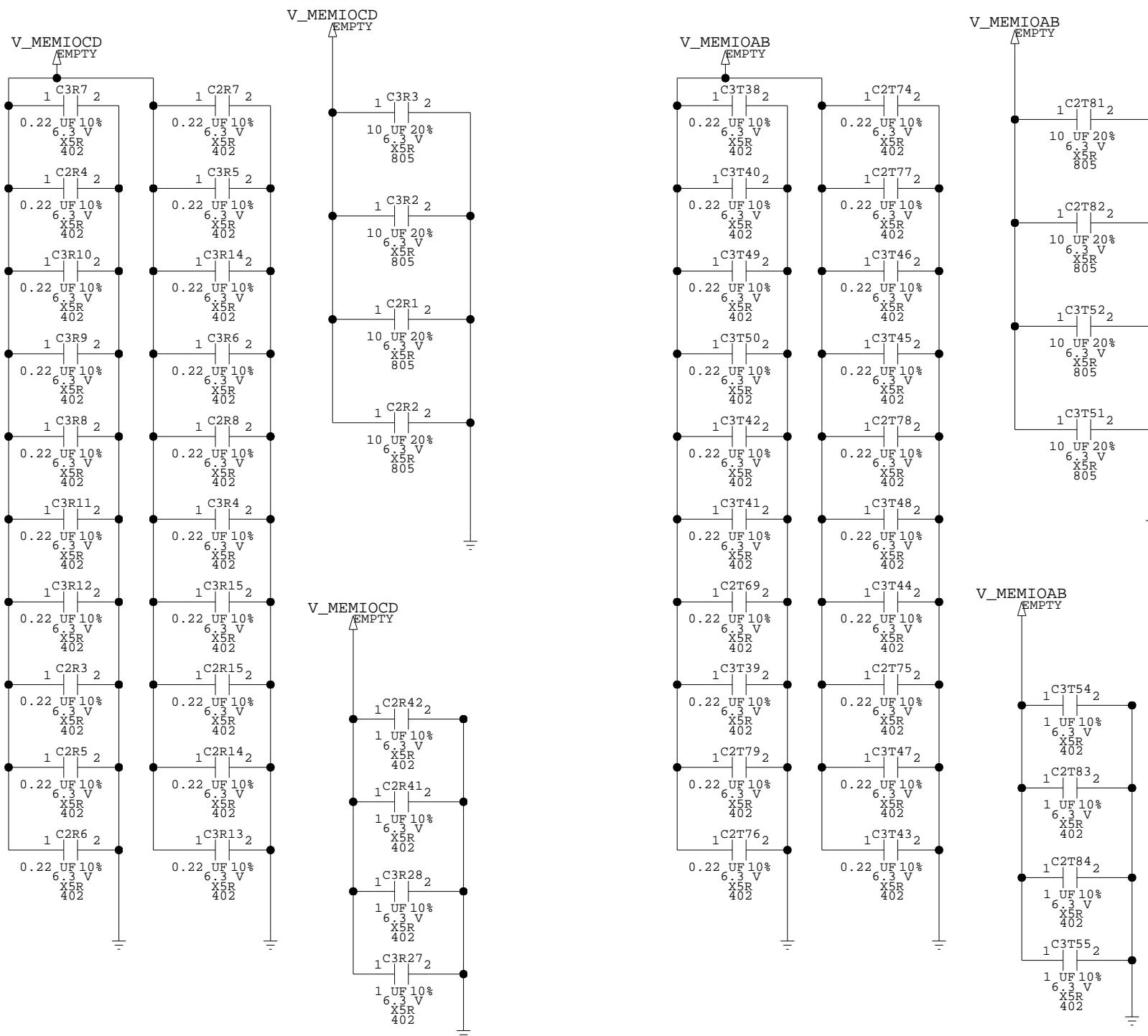
D

C

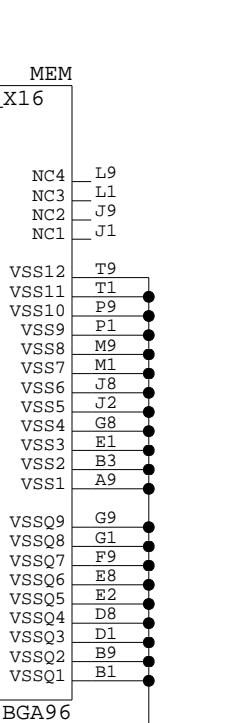
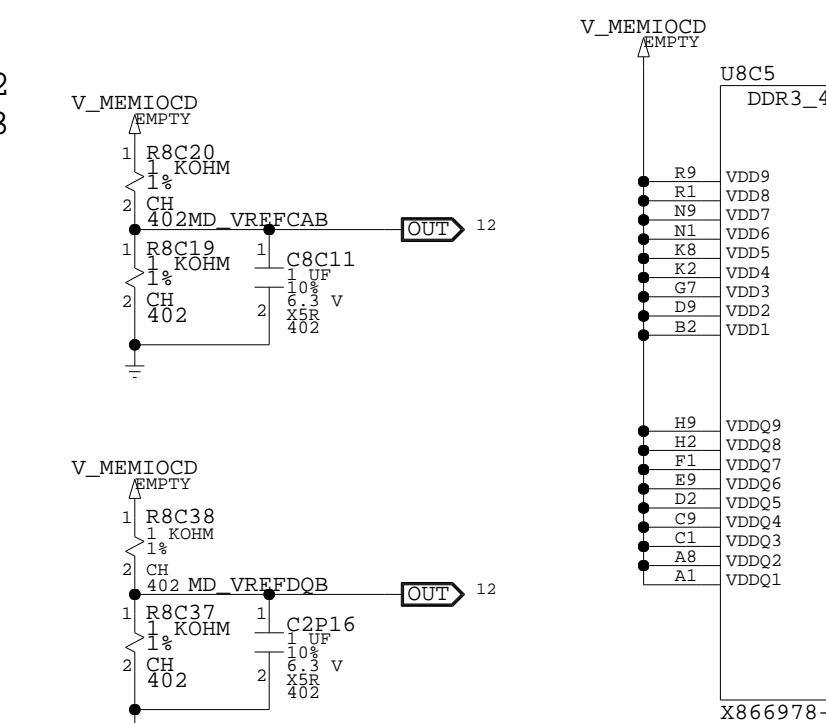
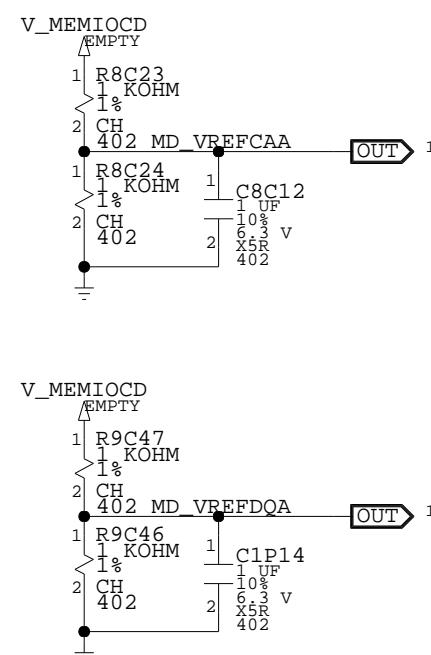
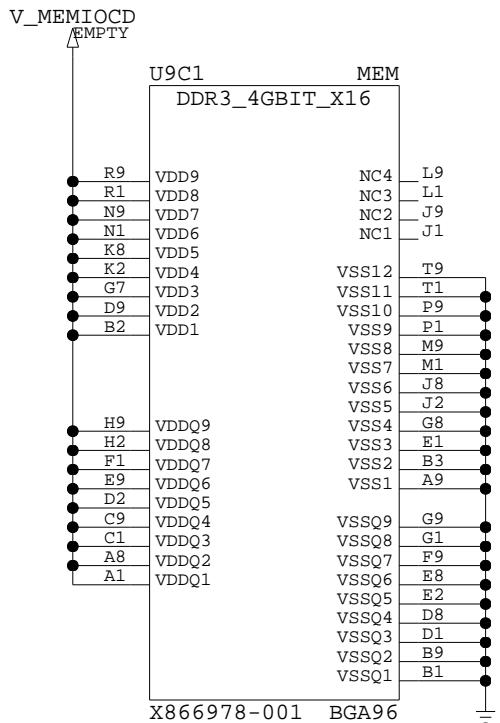
B

A

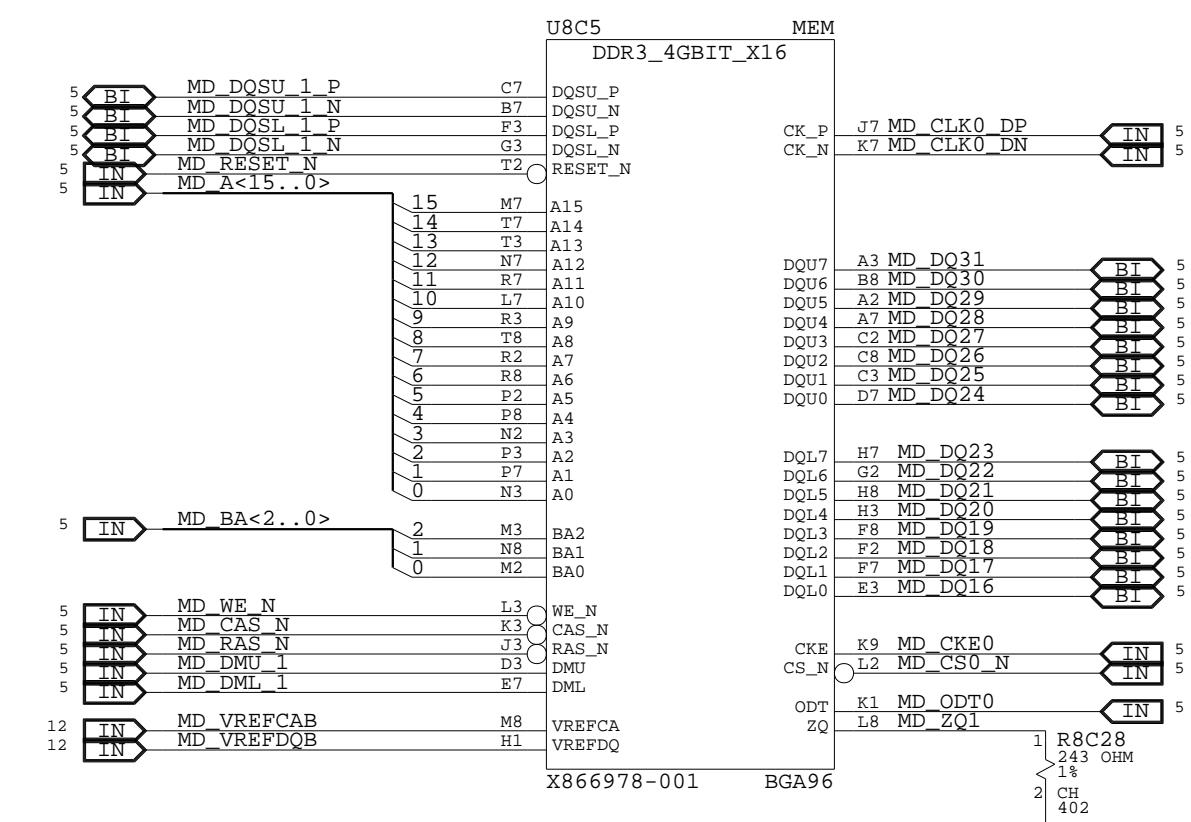
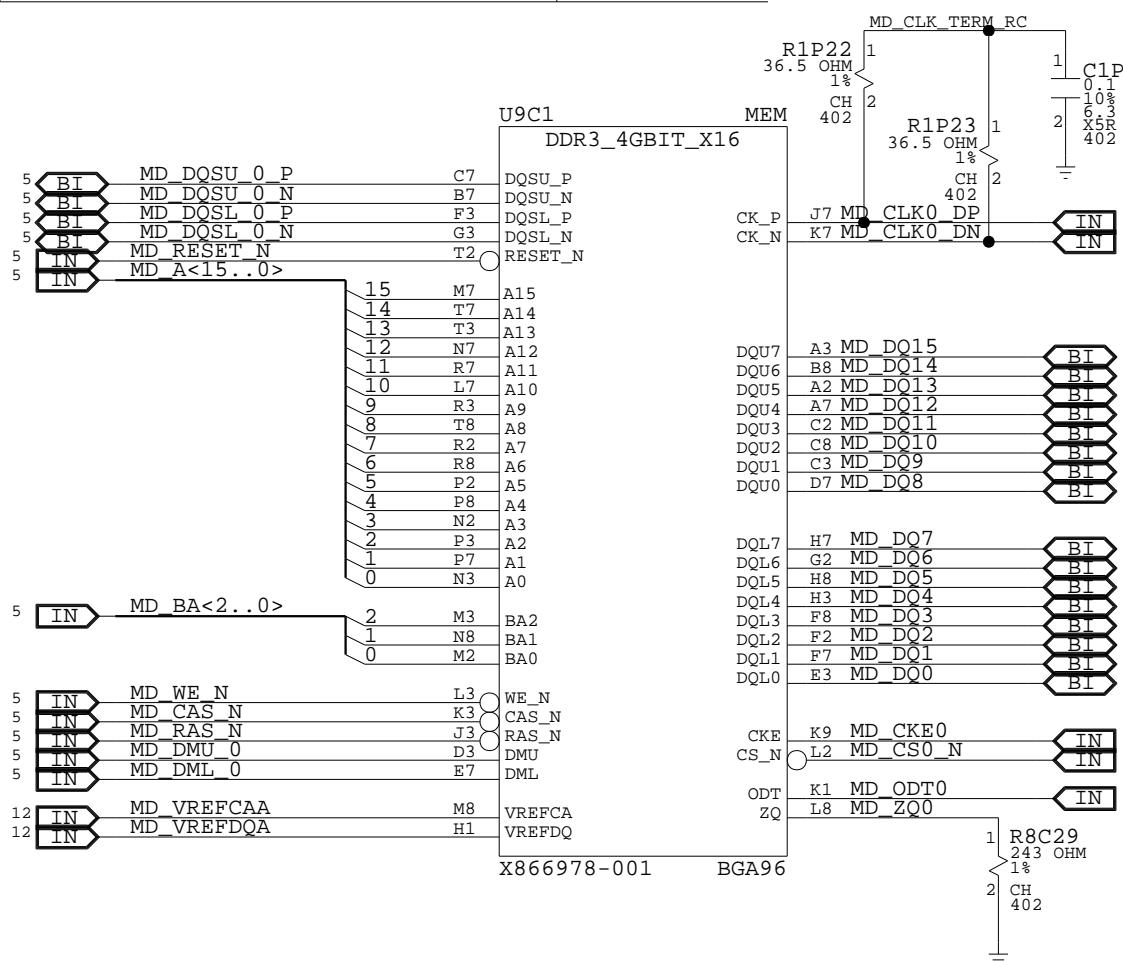
SOC, DECOUPLING



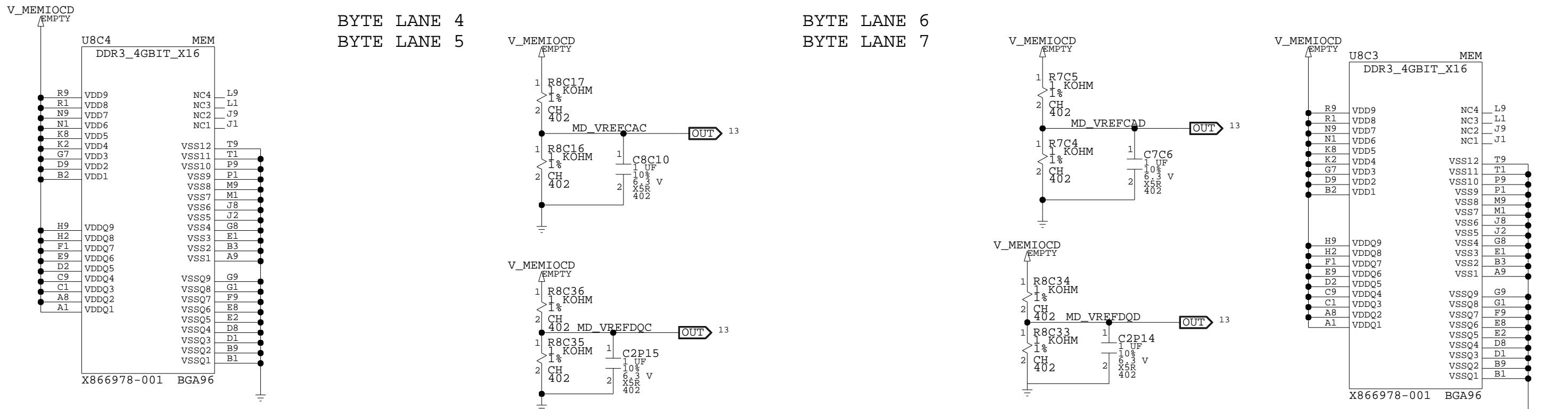
MEMORY CHANNEL D



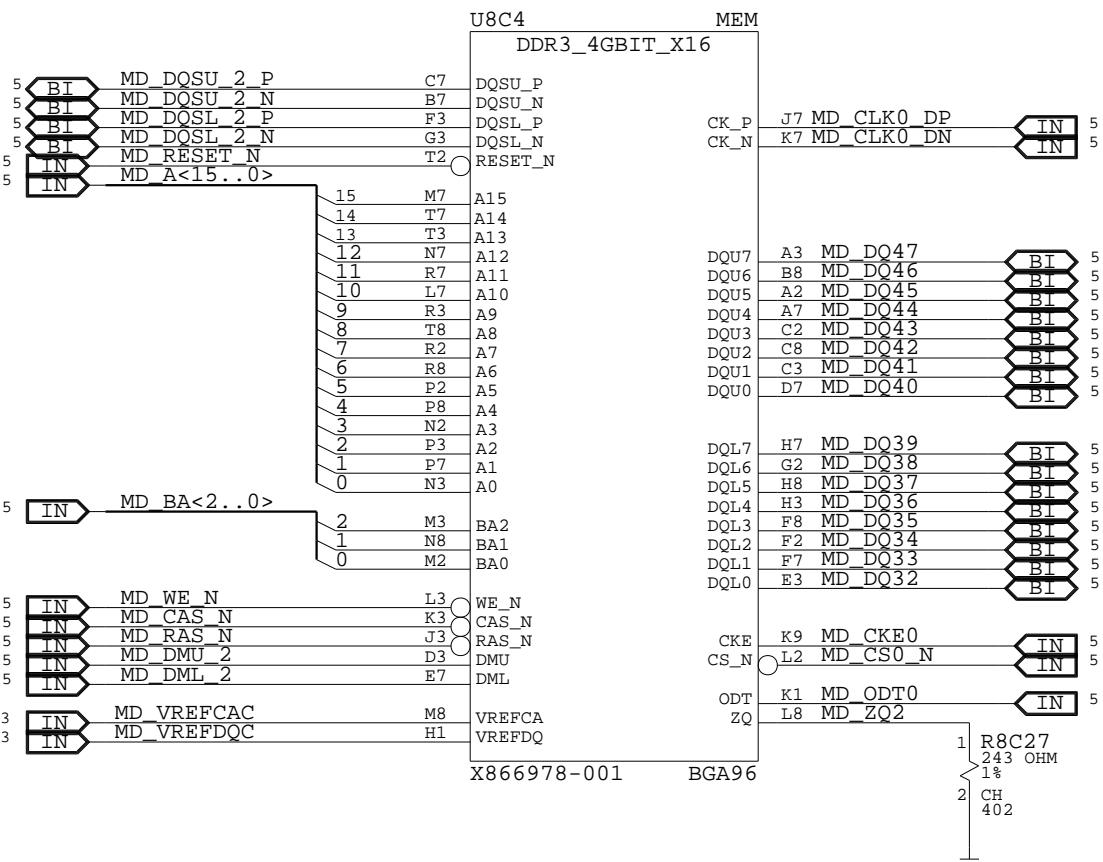
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U9C1, U8C5	EMPTY	EMPTY	MEMORY	DUMMY_BOM



MEMORY CHANNEL D

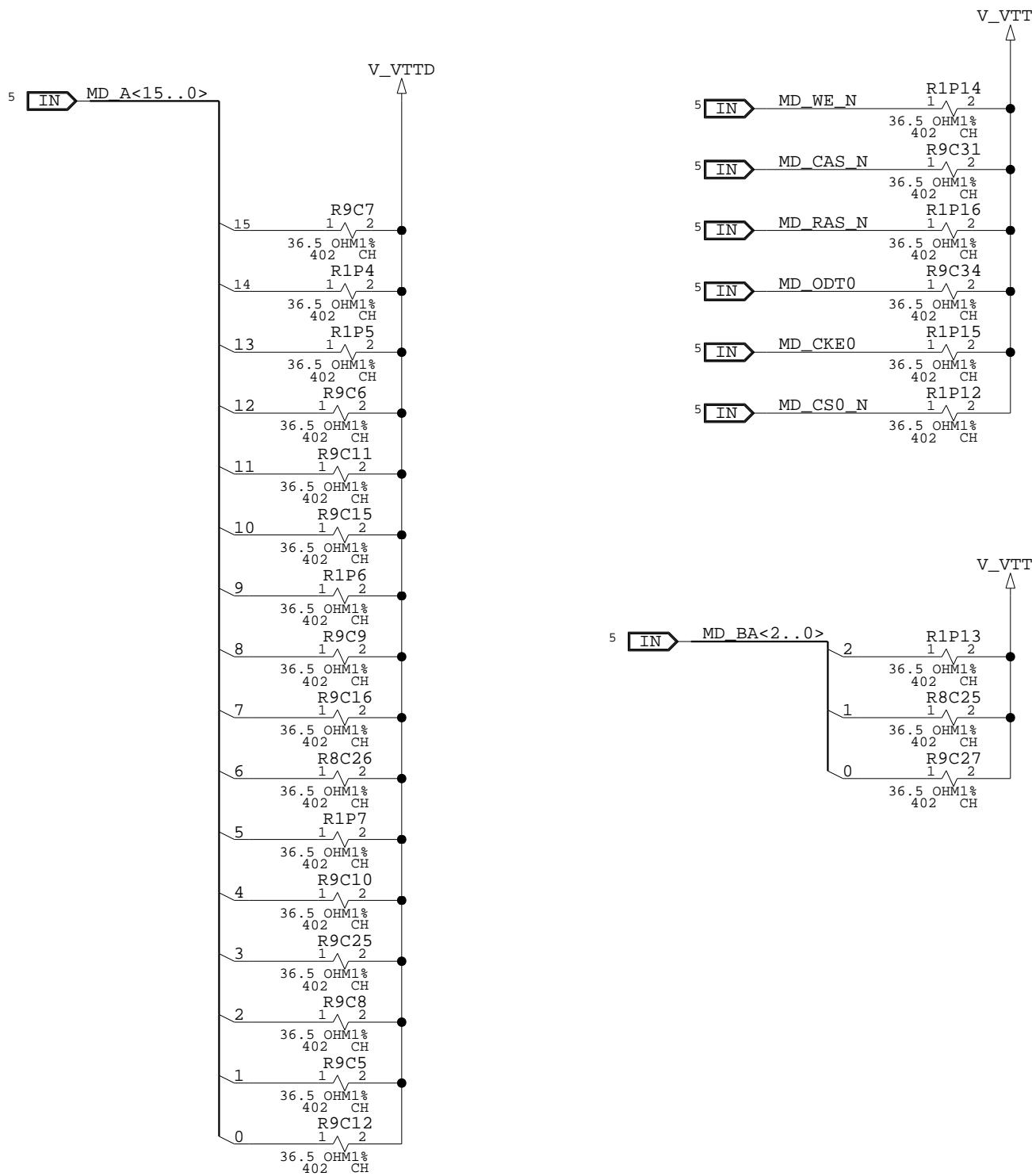


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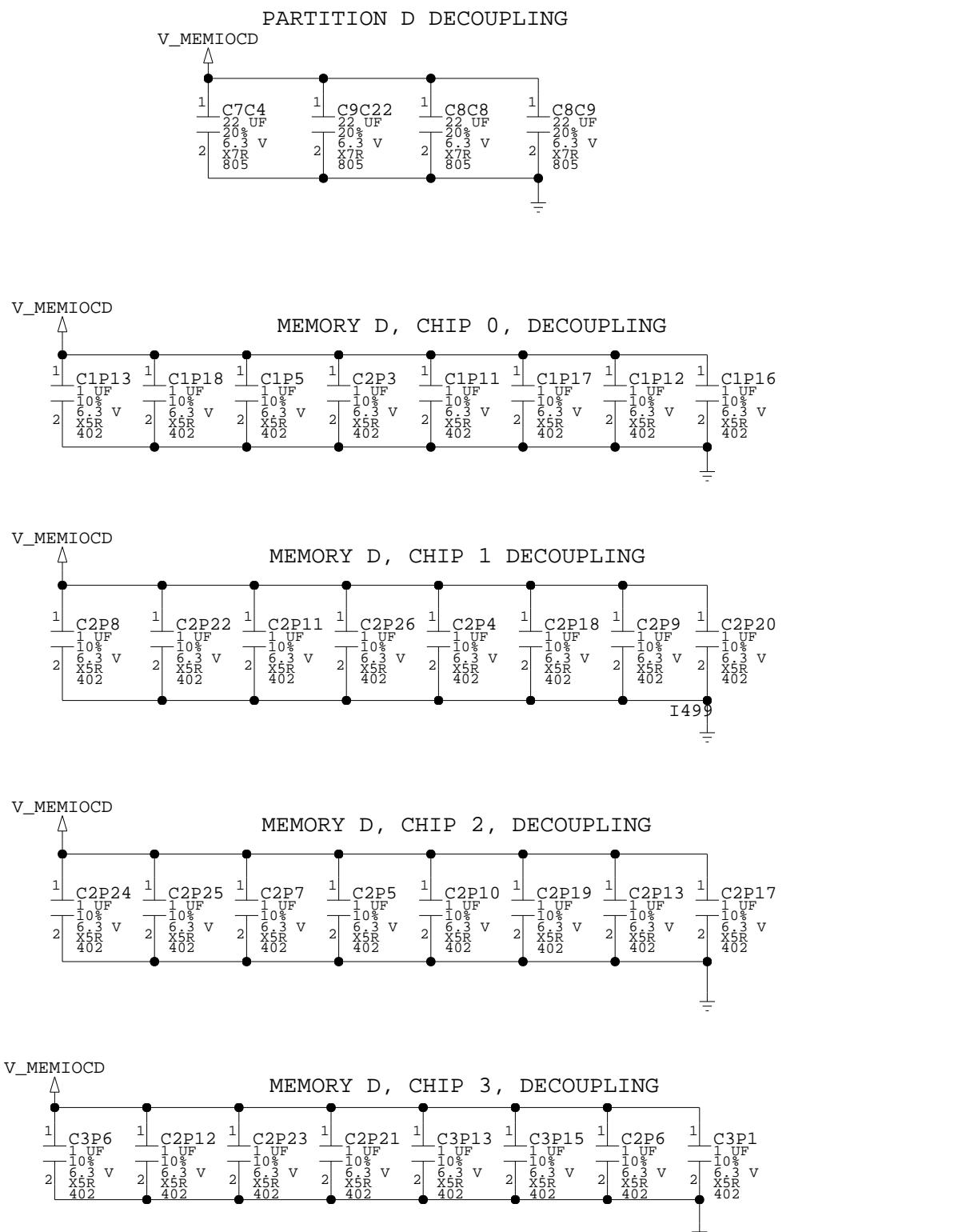


MEMORY CHANNEL D, DECOUPLING + TERMINATION

D

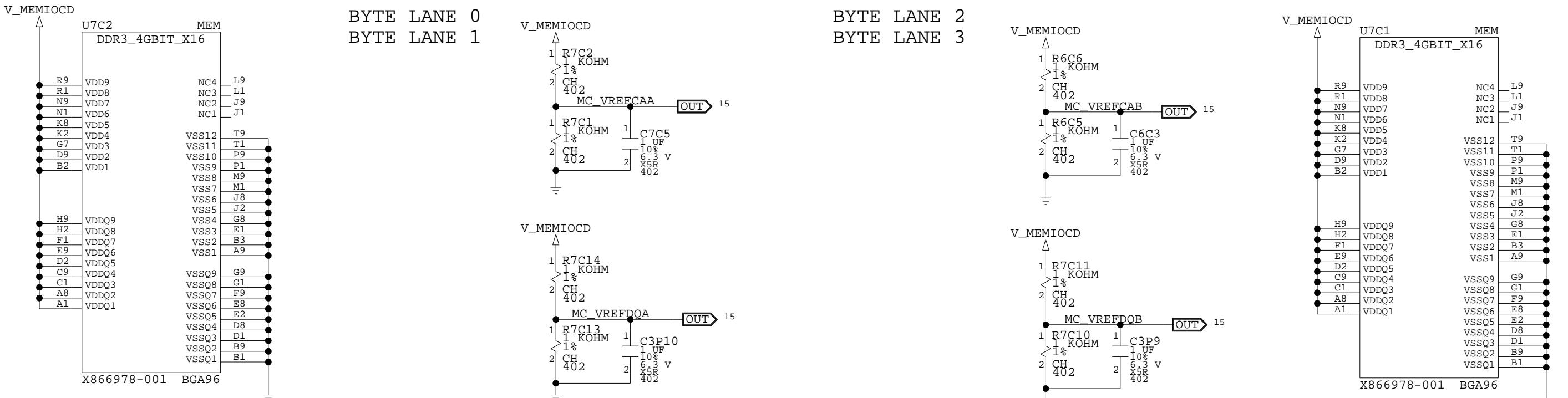


C

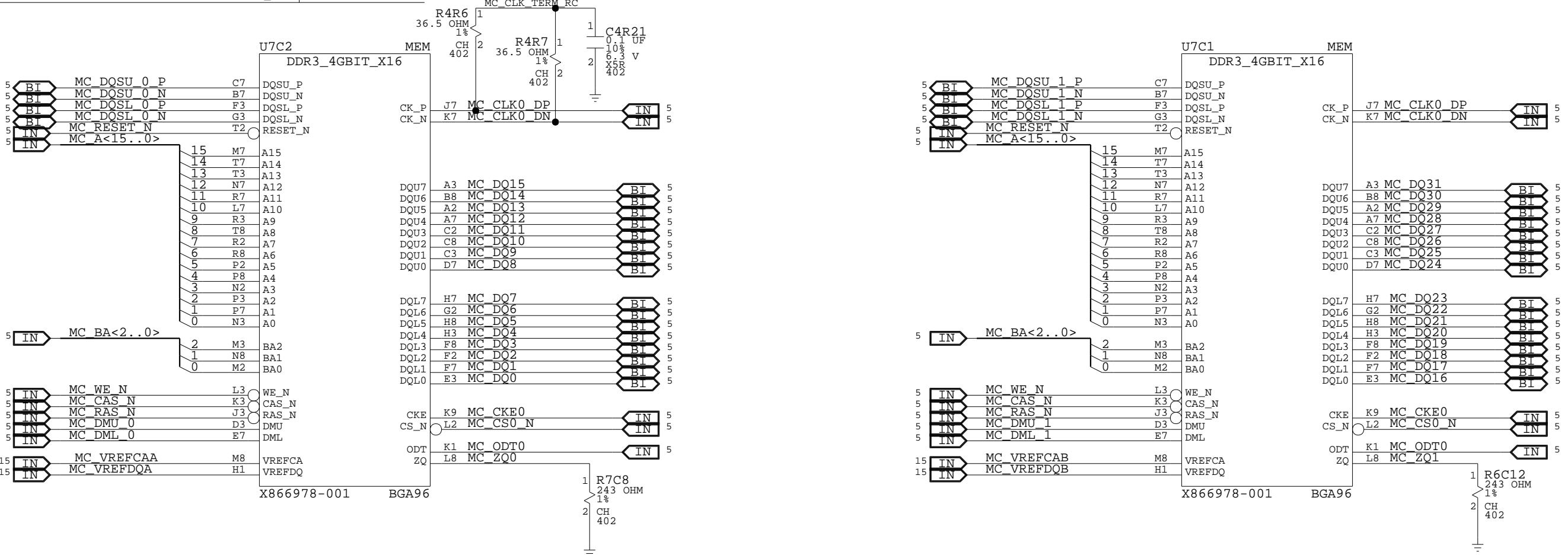


A

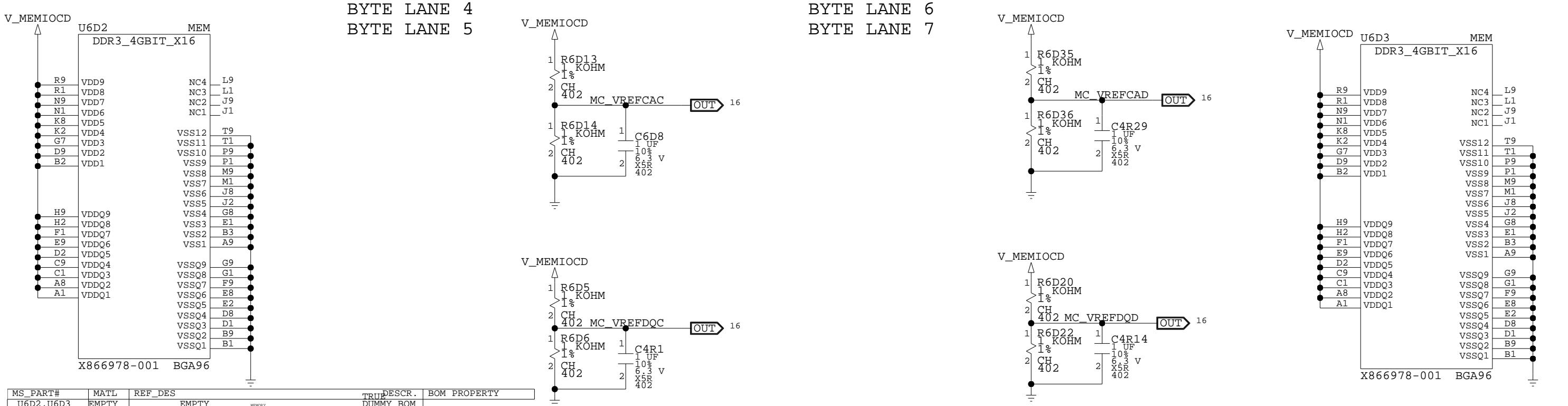
MEMORY CHANNEL C



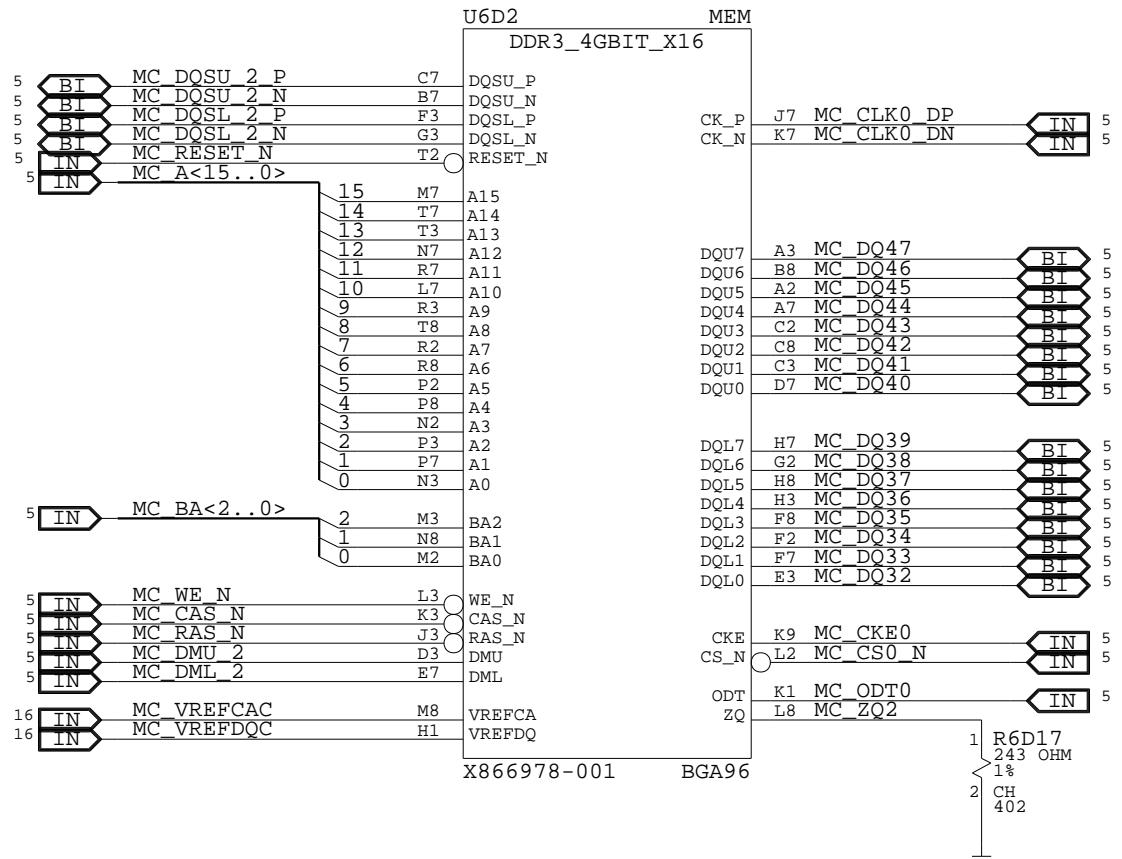
MS_PART#	MATL	REF_DES	TRUE DESCR.	BOM PROPERTY
U7C2, U7C1	EMPTY	MEMORY	DUMMY_BOM	



MEMORY CHANNEL C



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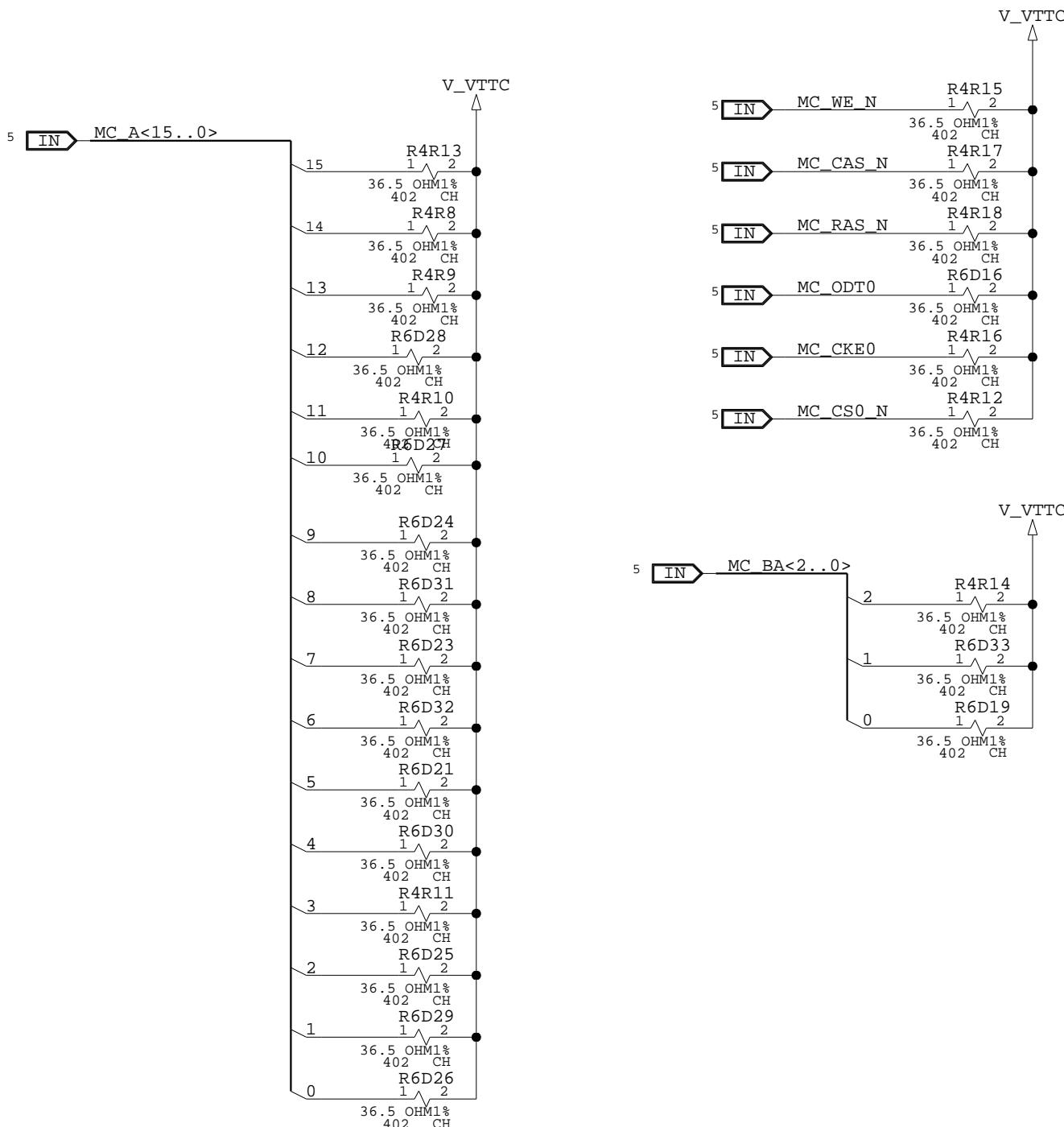


[PAGE_TITTLE=MEMORY PARTITION_B , HIGH]

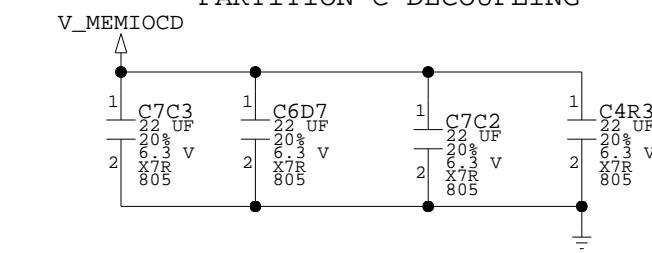
8 7 6 5 4 3 2 1

MEMORY CHANNEL C, DECOUPLING + TERMINATION

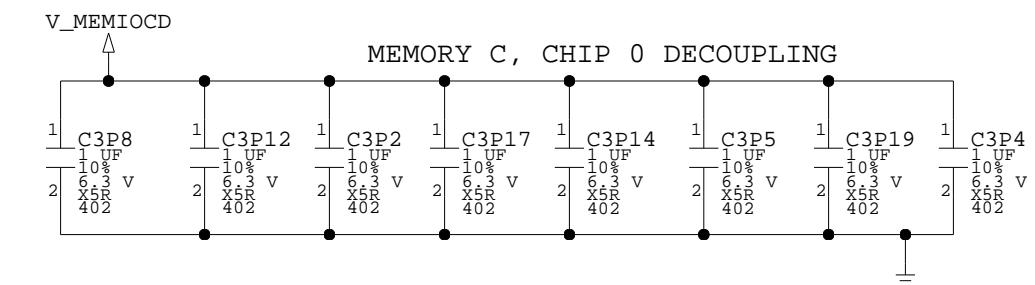
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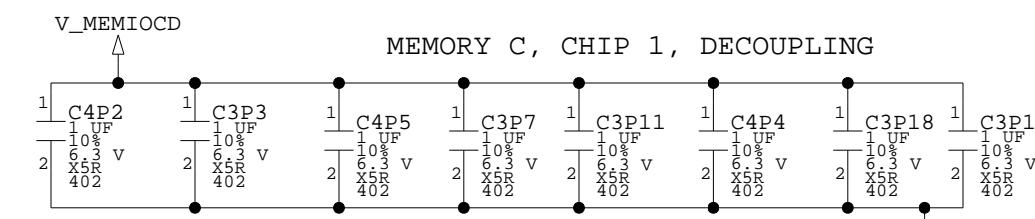
PARTITION C DECOUPLING



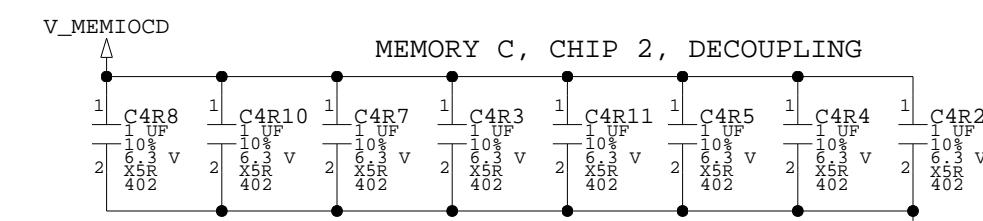
MEMORY C, CHIP 0 DECOUPLING



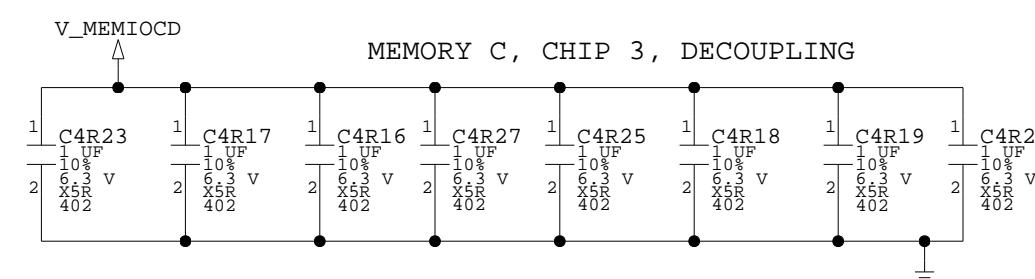
MEMORY C, CHIP 1, DECOUPLING



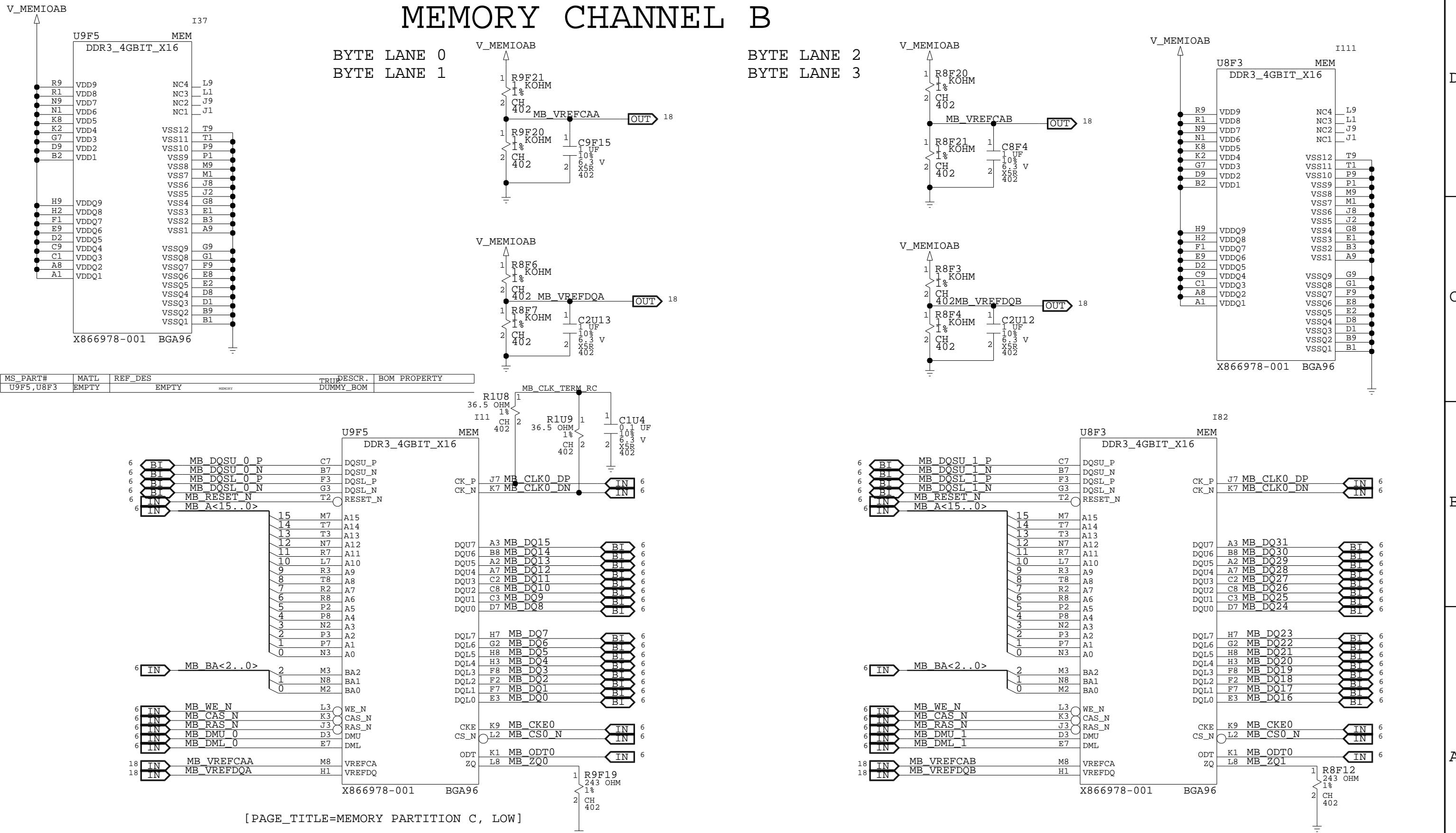
MEMORY C, CHIP 2, DECOUPLING



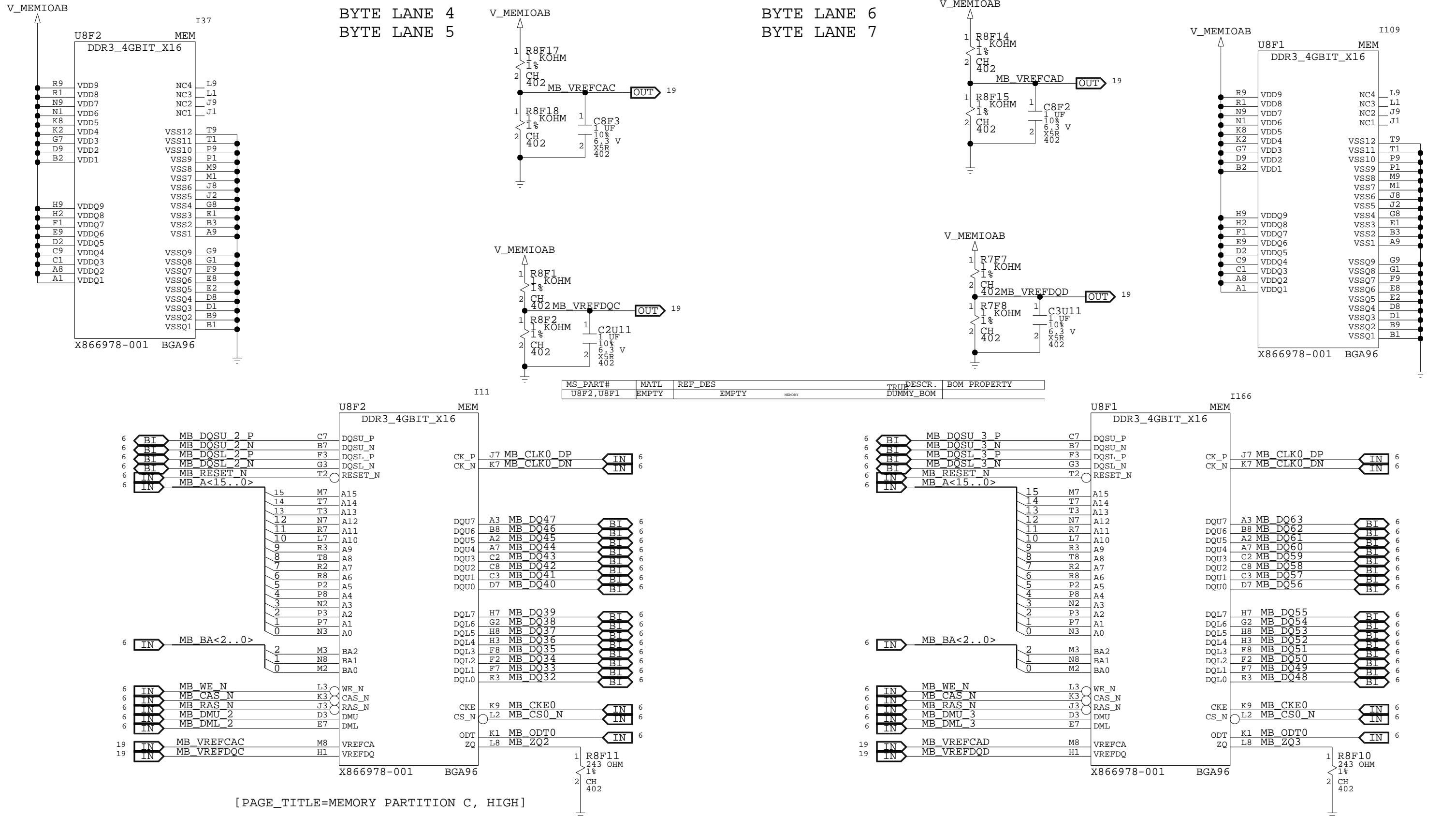
MEMORY C, CHIP 3, DECOUPLING



MEMORY CHANNEL B

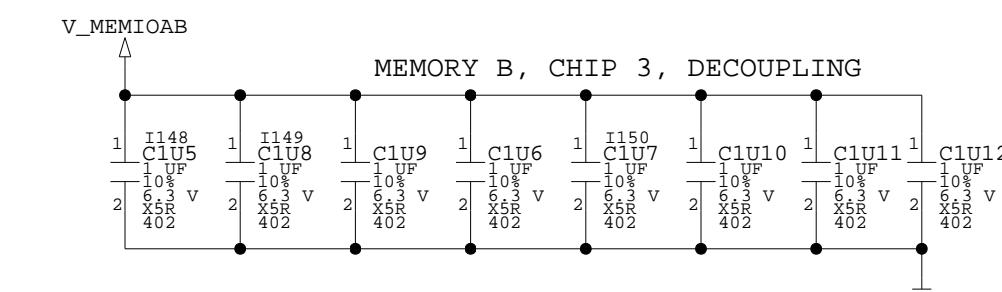
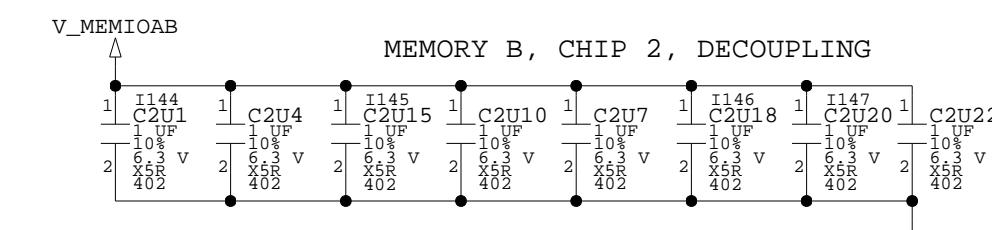
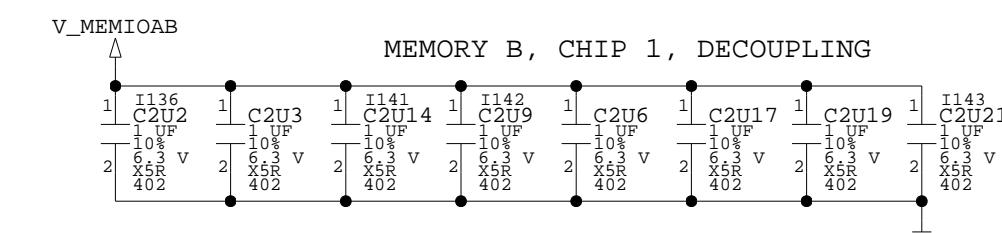
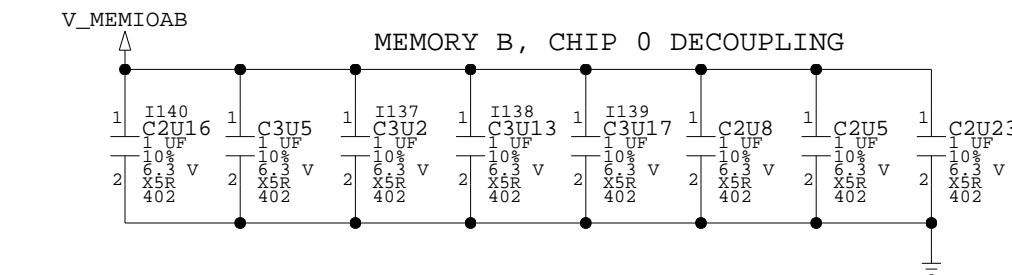
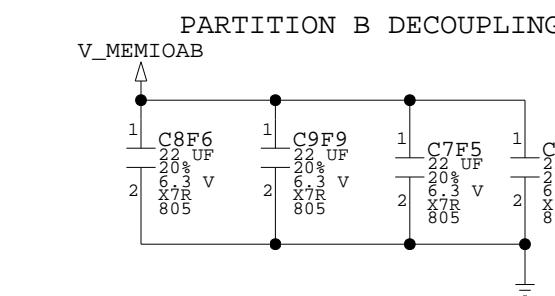
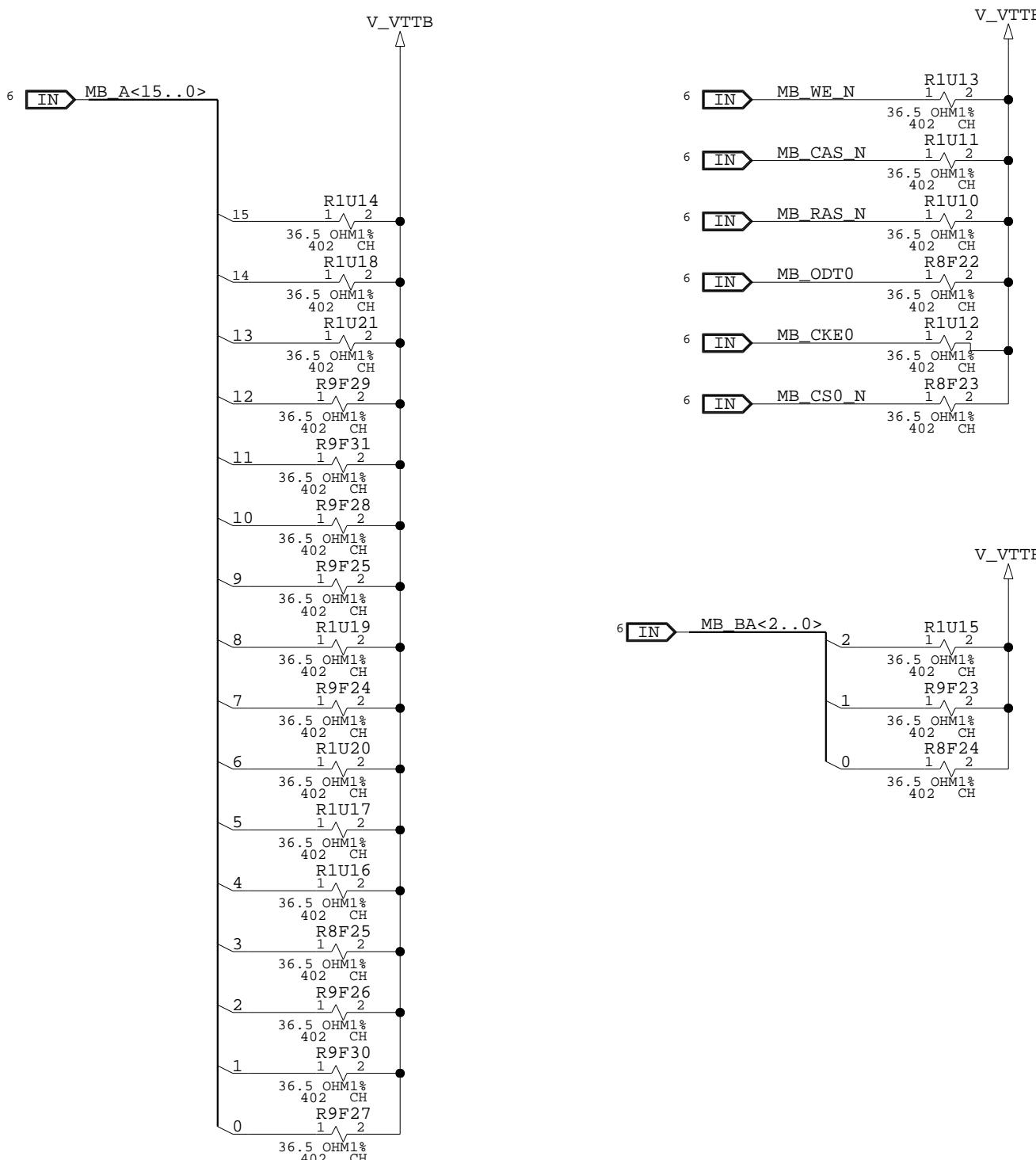


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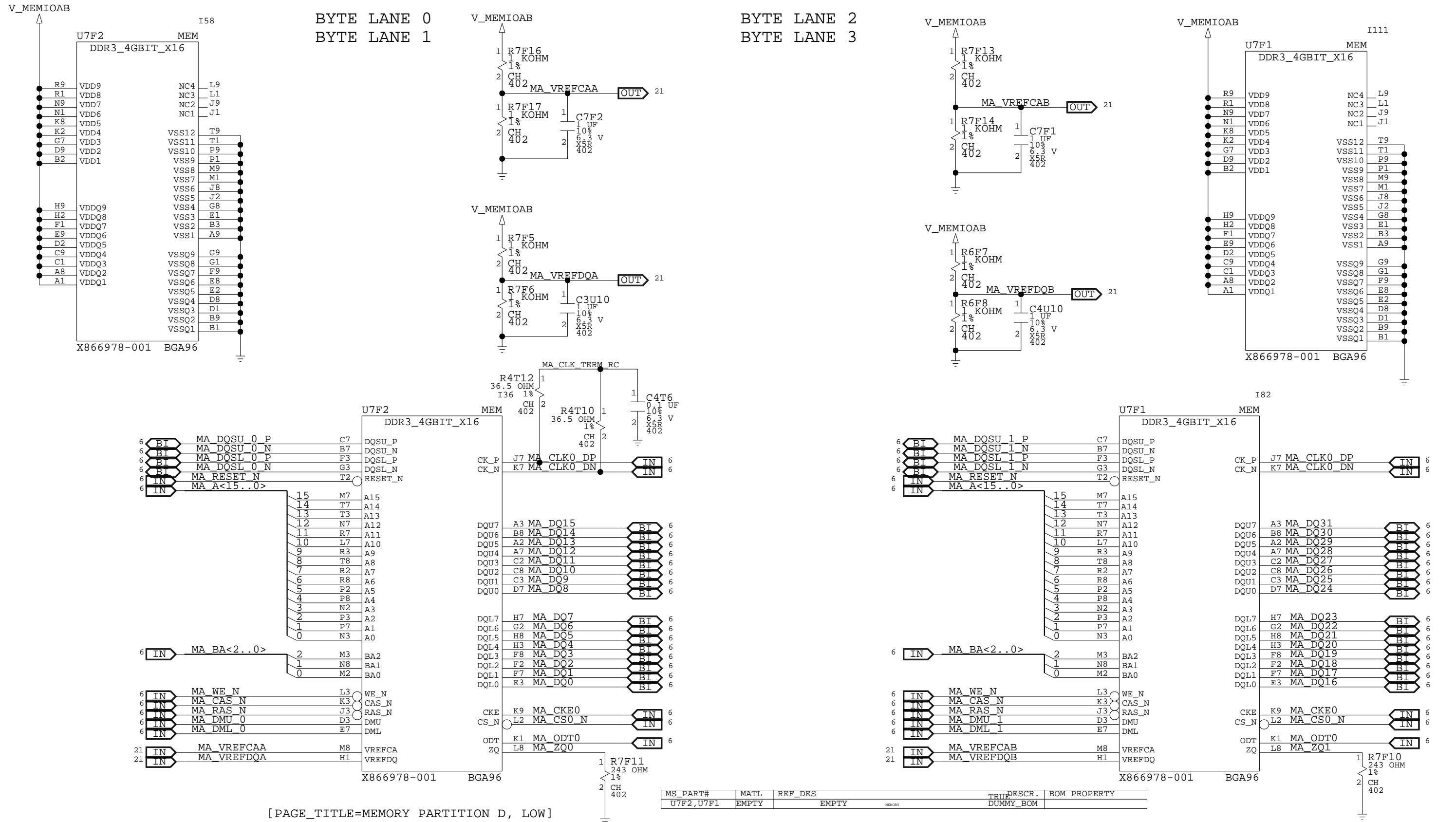


MEMORY CHANNEL B, DECOUPLING + TERMINATION

D



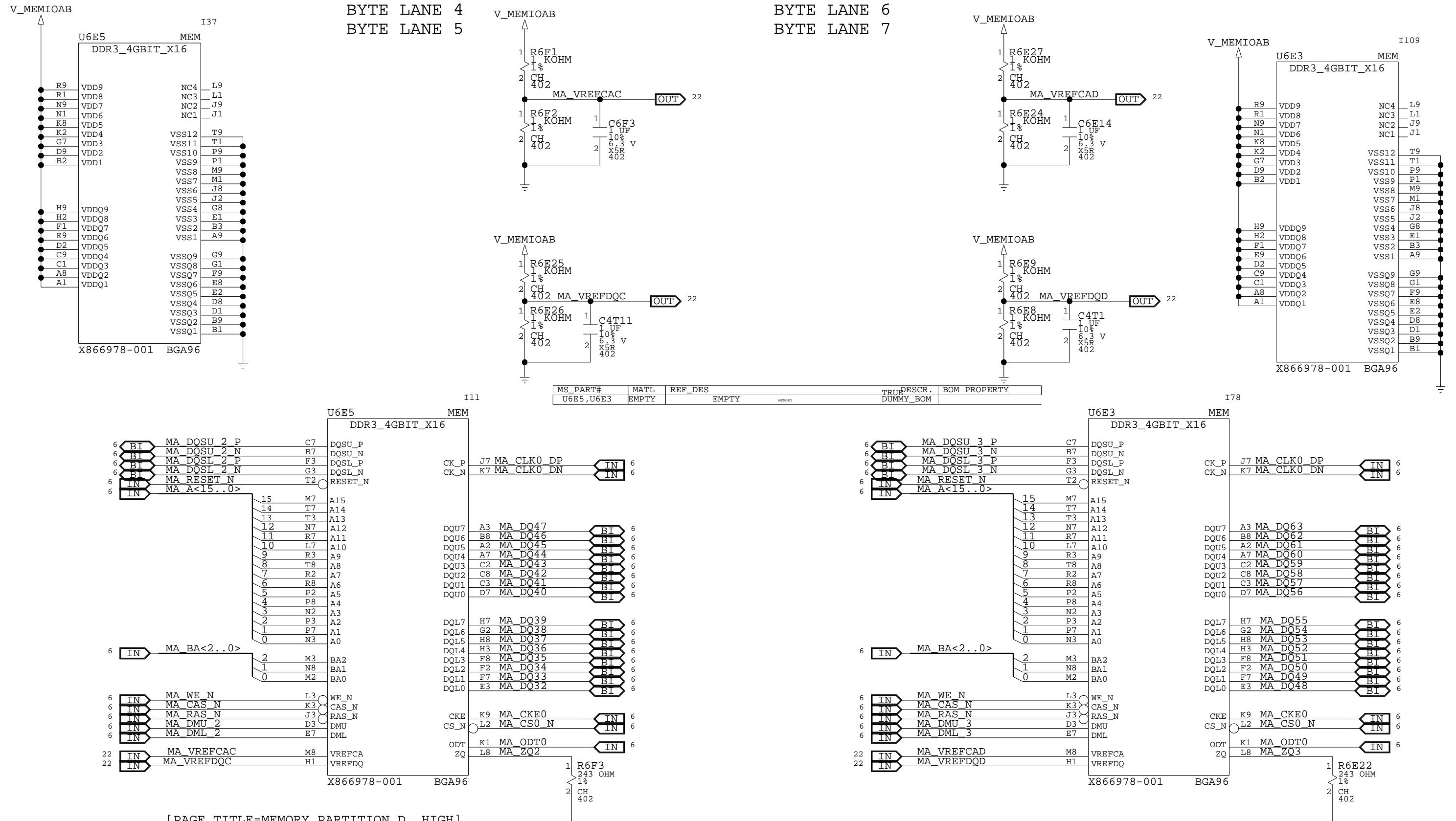
MEMORY CHANNEL A



[PAGE_TITLE=MEMORY PARTITION D, LOW]

MS_PART#	MATL	REF_DES	TRUE DESCRIPTOR	BOM PROPERTY
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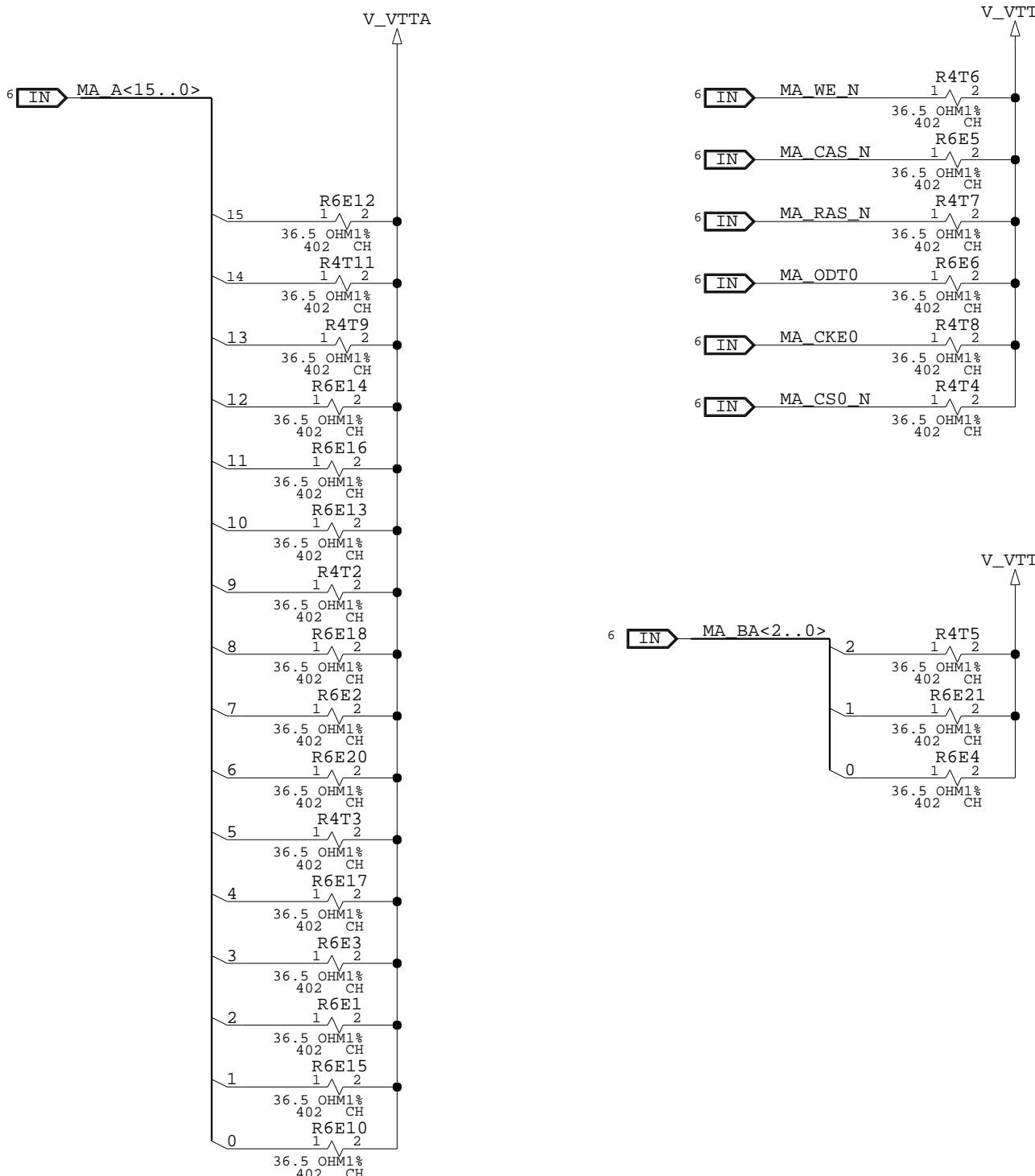
MEMORY CHANNEL A



[PAGE_TITLE=MEMORY PARTITION D, HIGH]

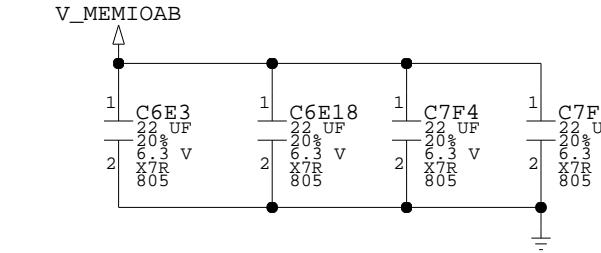
MEMORY CHANNEL A, DECOUPLING + TERMINATION

D



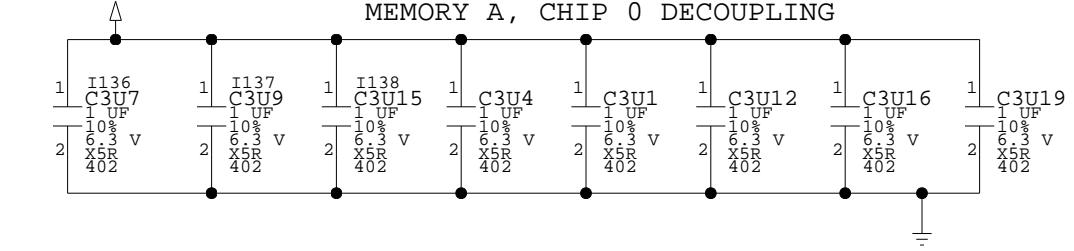
D

PARTITION A DECOUPLING



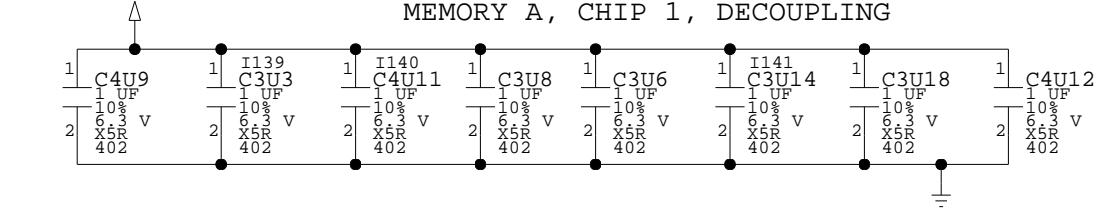
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MEMORY A, CHIP 0 DECOUPLING



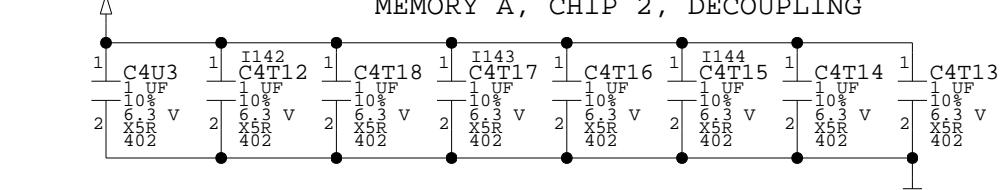
C

MEMORY A, CHIP 1, DECOUPLING



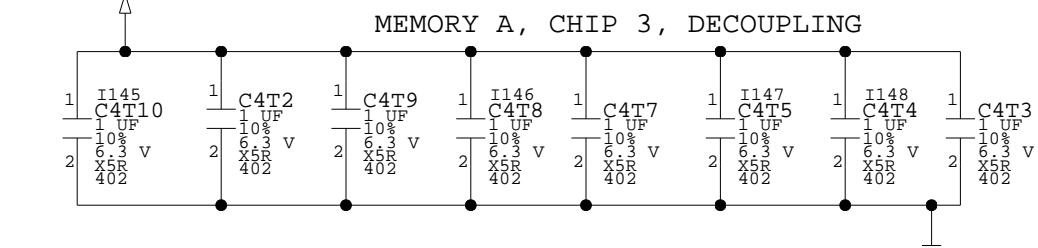
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MEMORY A, CHIP 2, DECOUPLING



A

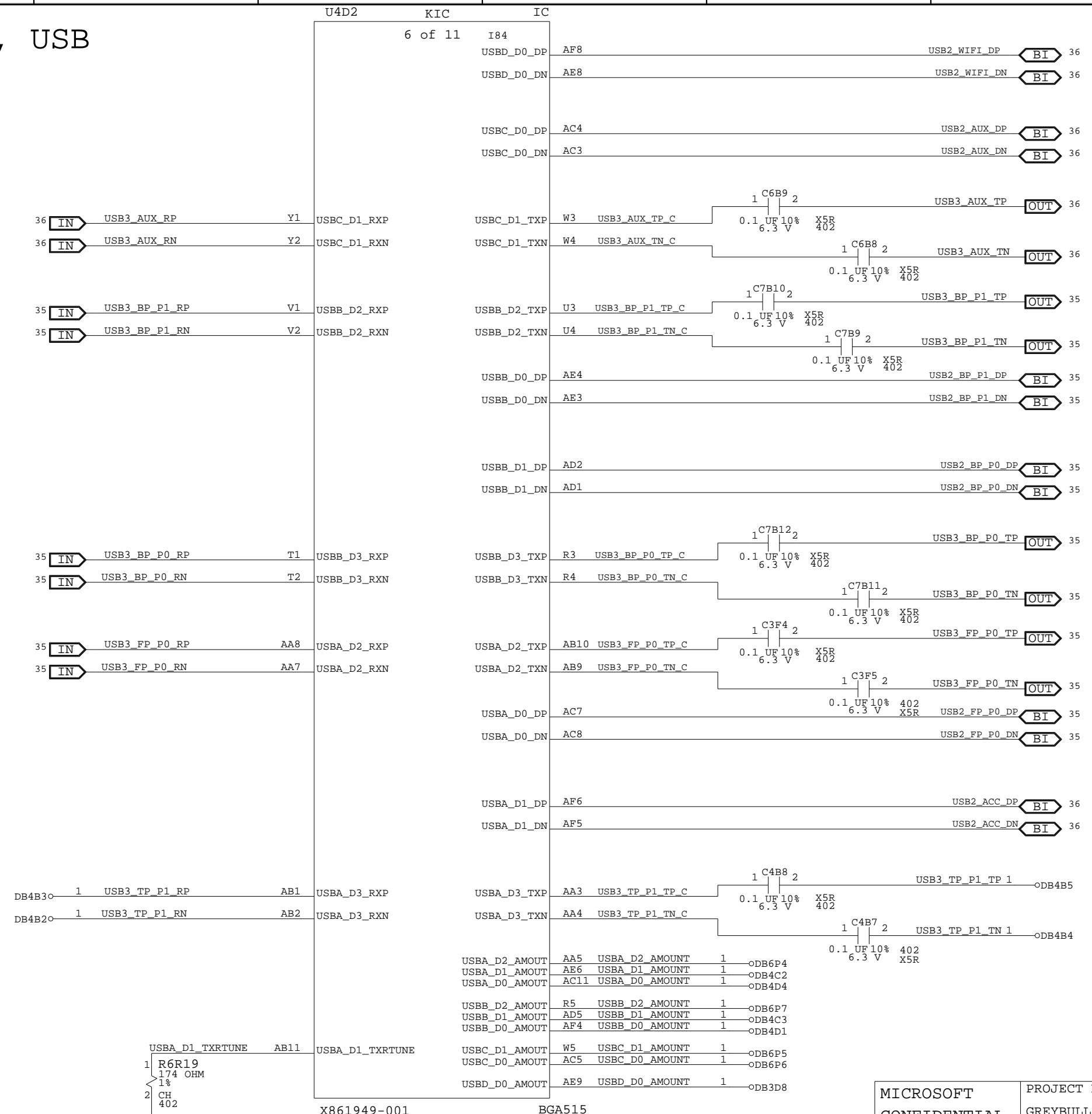
MEMORY A, CHIP 3, DECOUPLING



[PAGE_TITLE=MEMORY PARTITION D, DECOUPLING, TERMINATION]

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 23/72	CSA PAGE 23/72	FAB M	REV 1.0
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KIC, USB



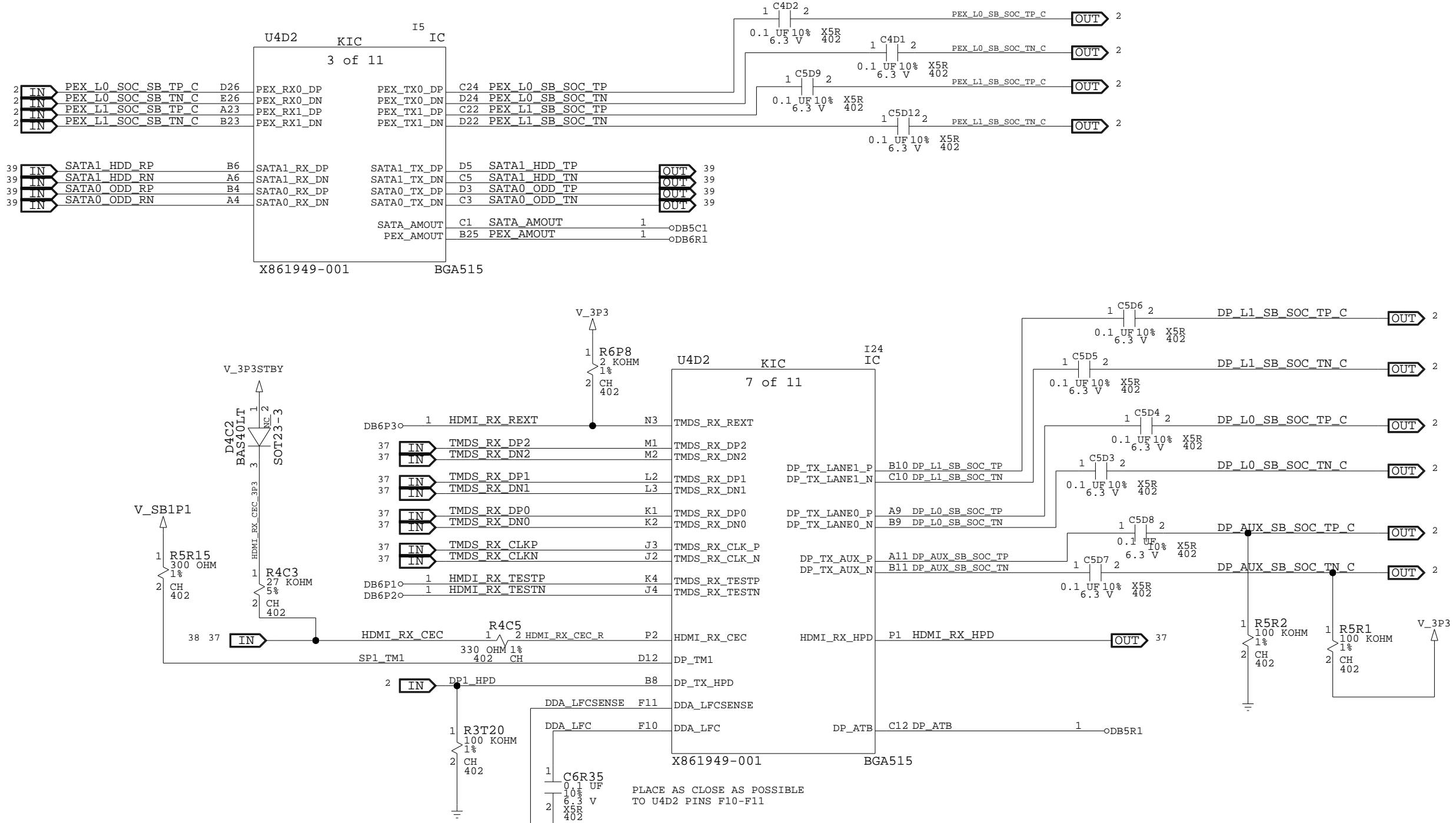
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			X861949-001

x861949-001

BGA515

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 24/72	CSA PAGE 24/72	FAB M	REV 1.0
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KIC, PCIE + SATA + VIDEO



MS_PART#	MATL	REF_DES	TRUE_DESCR.	BOM PROPERTY
U4D2	EMPTY	EMPTY	KIC	DUMMY_BOM

KIC, SMC

D

D

C

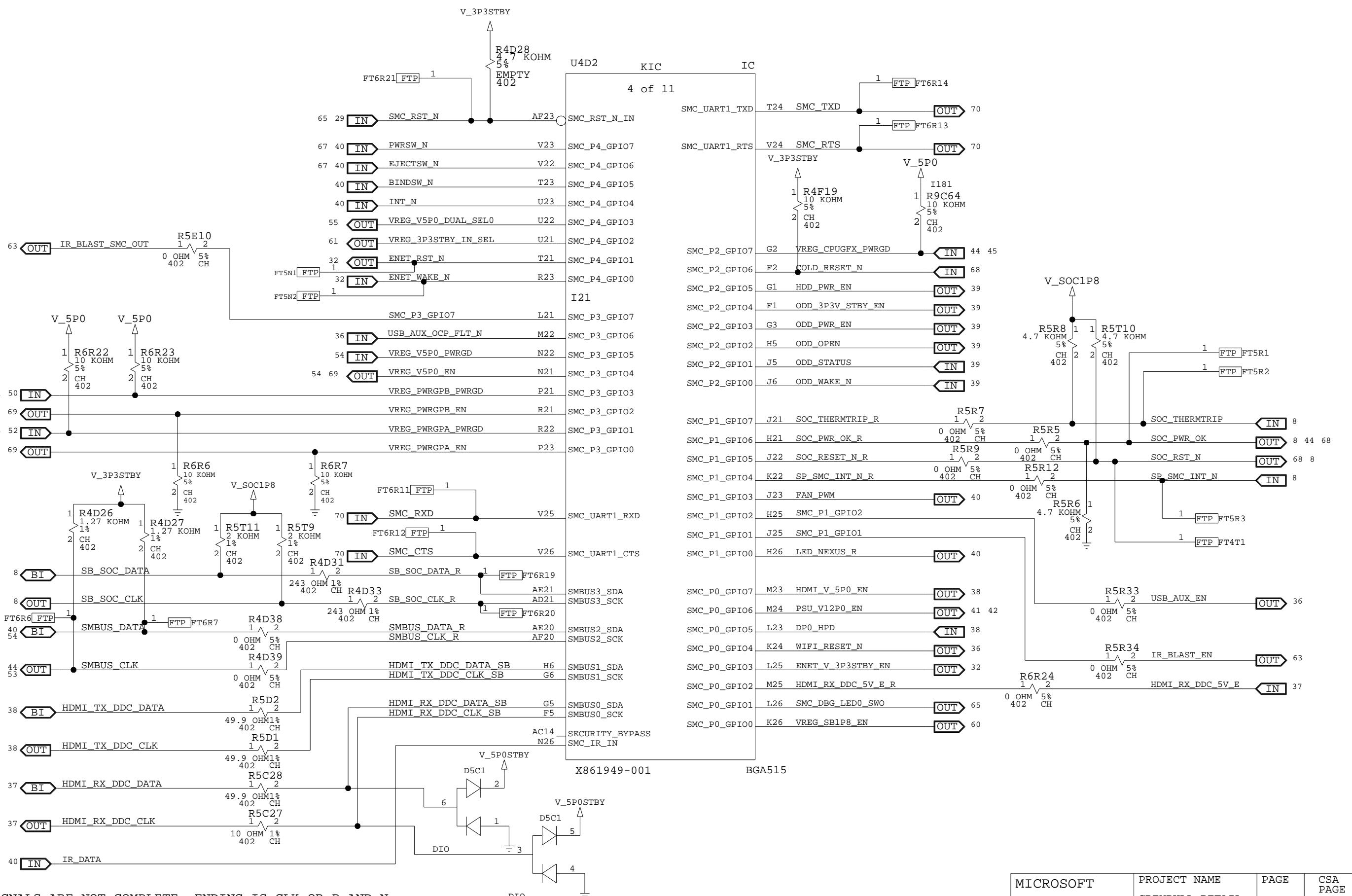
C

B

B

A

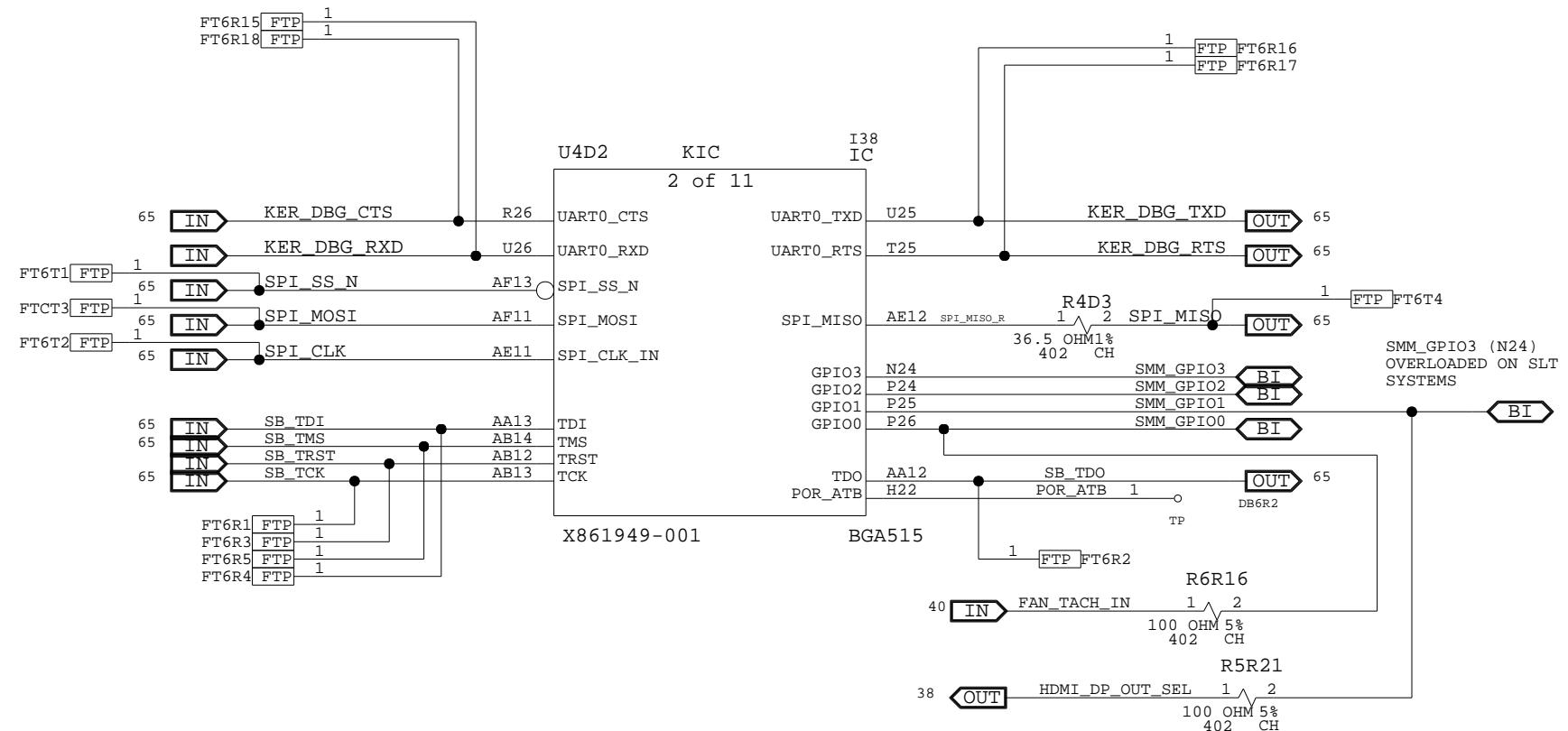
A



THESE SIGNALS ARE NOT COMPLETE- ENDING IS CLK OR P AND N

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 26/72	CSA PAGE 26/72	FAB M	REV 1.0
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KIC, FACET



D

D

C

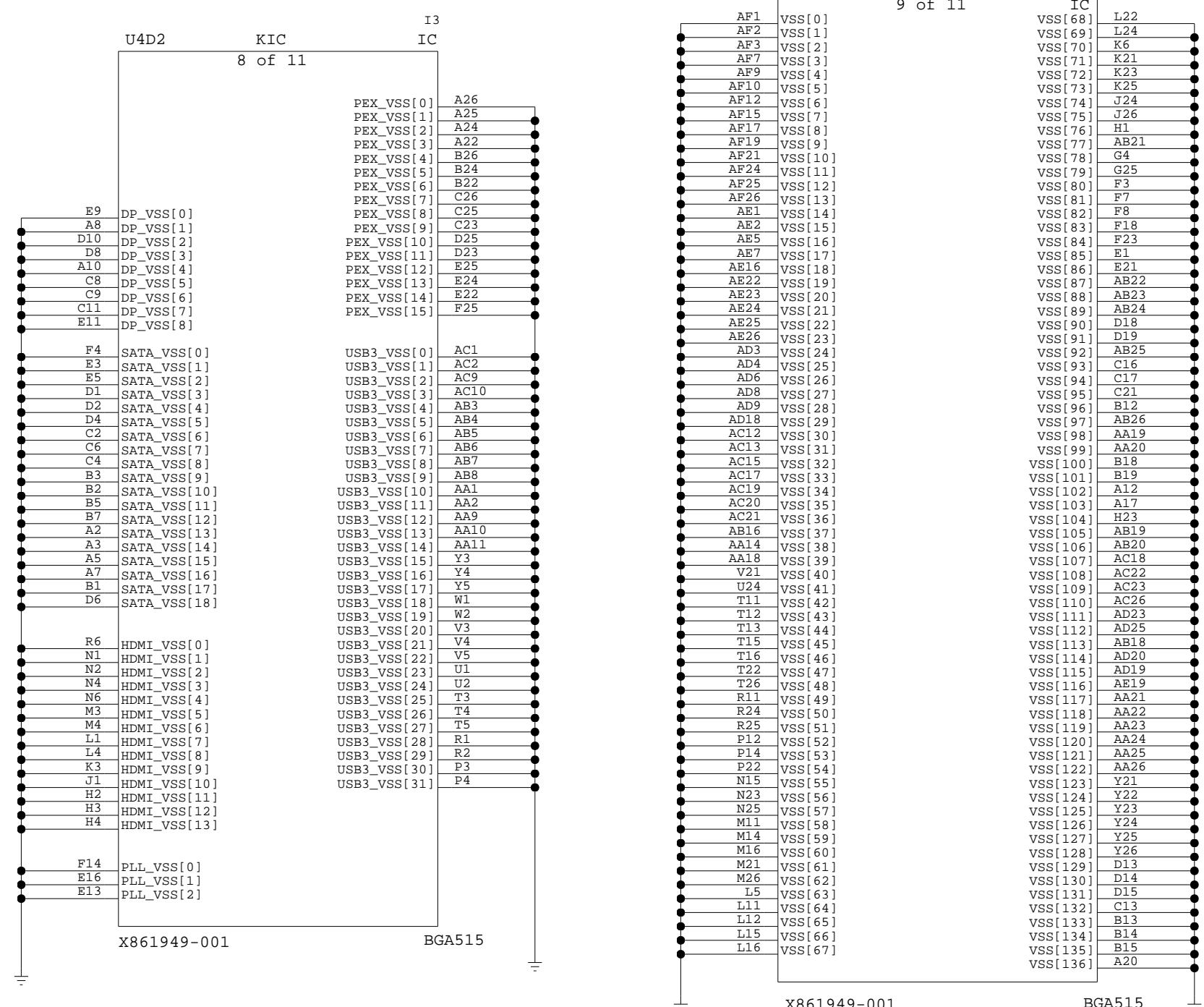
C

B

B

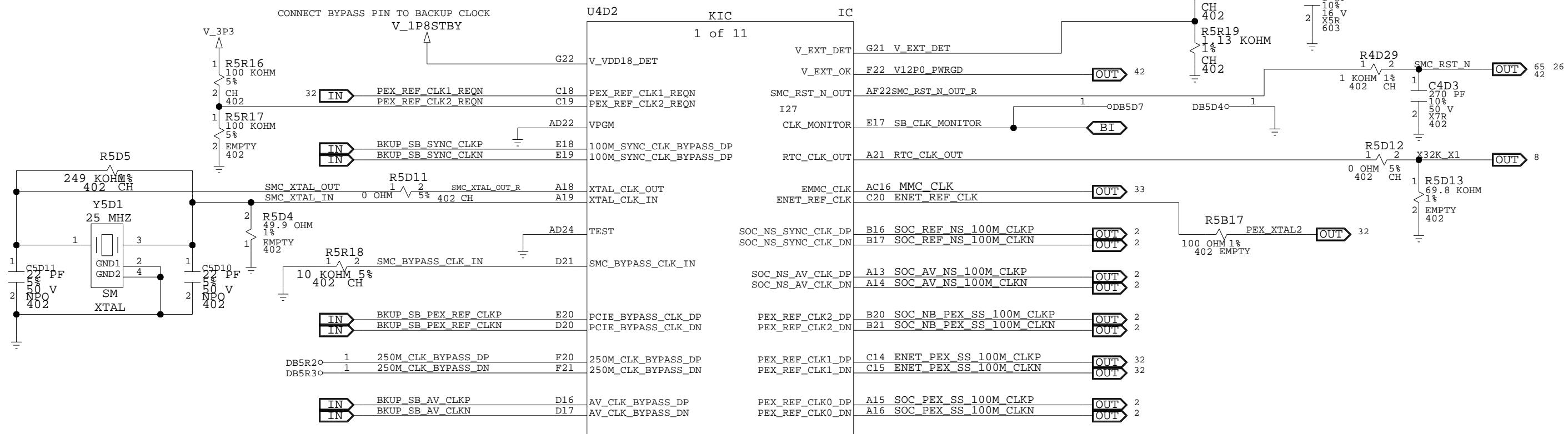
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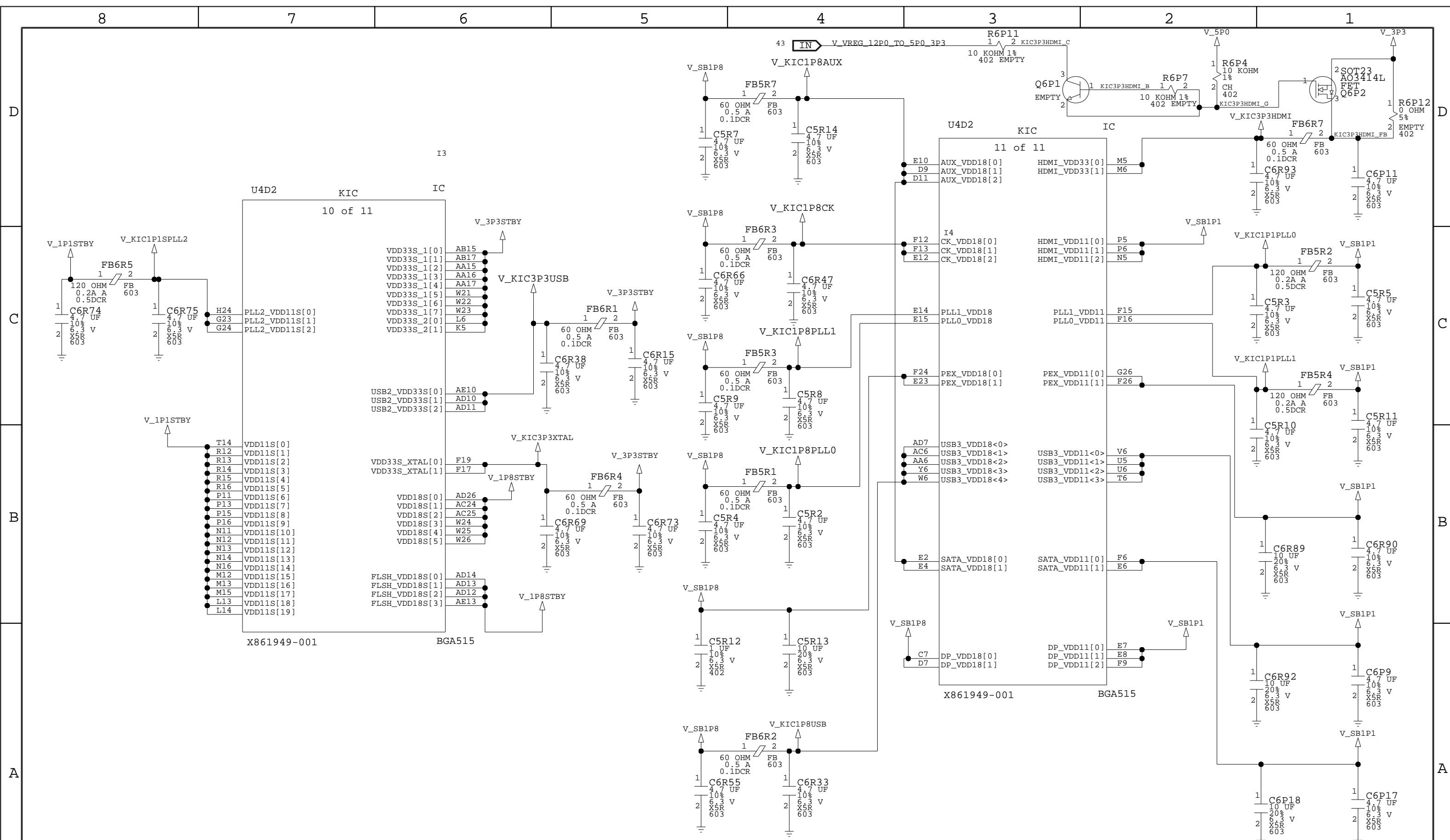
A



8 7 6 5 4 3 2 1

KIC, CLOCKS + STRAPPING + POR





KIC, DECOUPLING

D

D

C

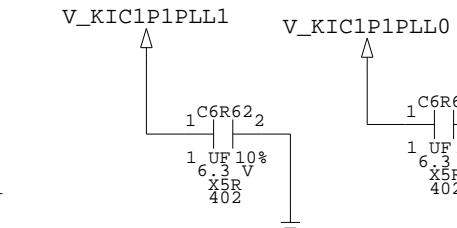
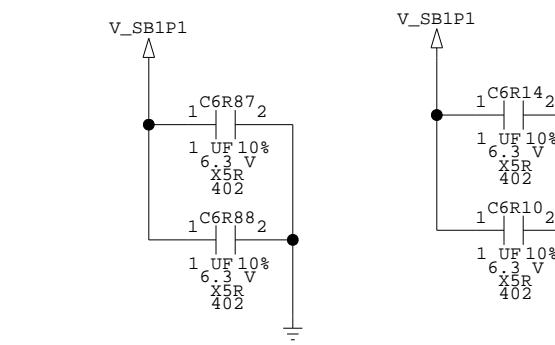
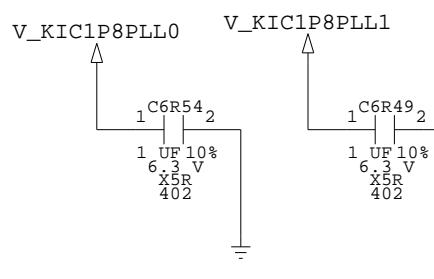
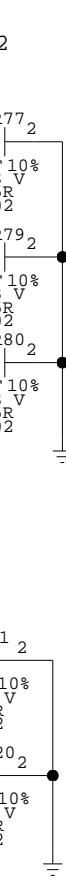
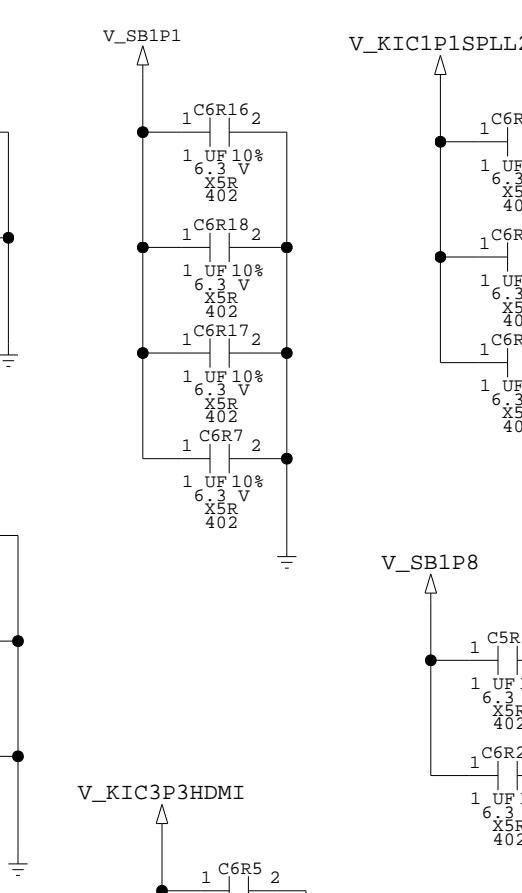
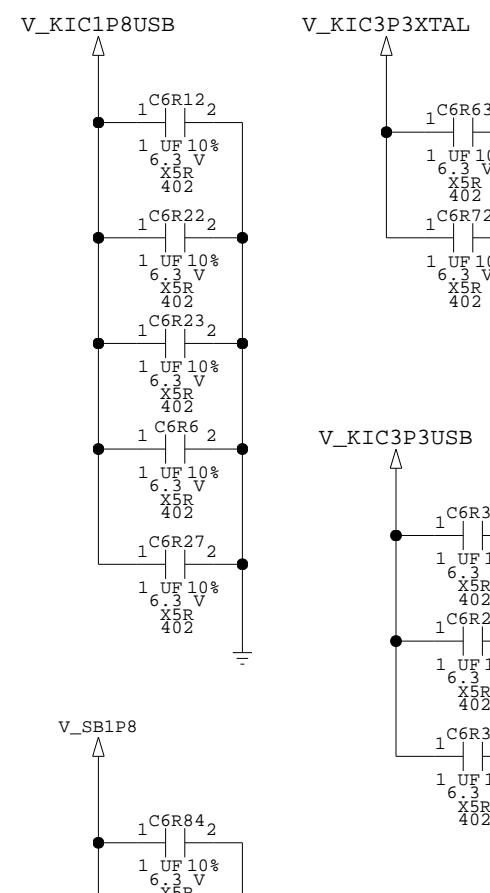
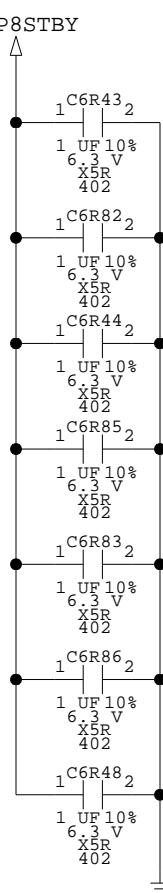
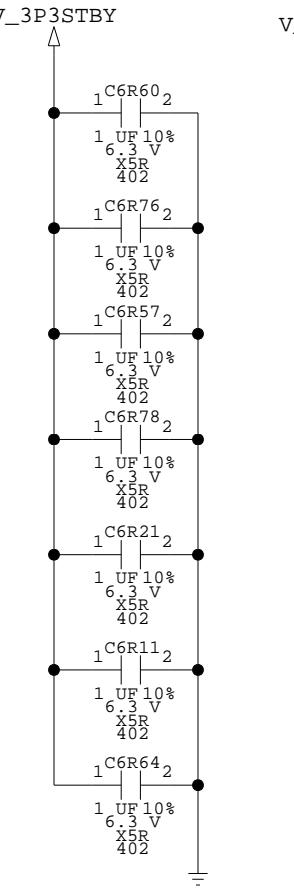
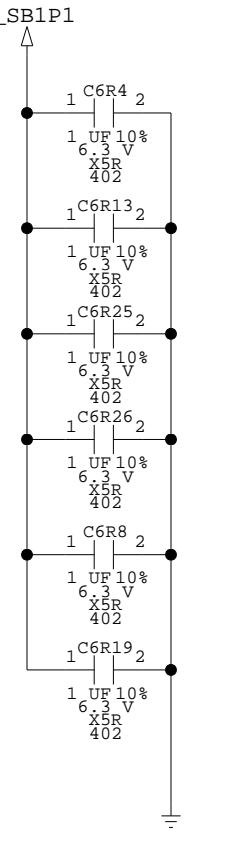
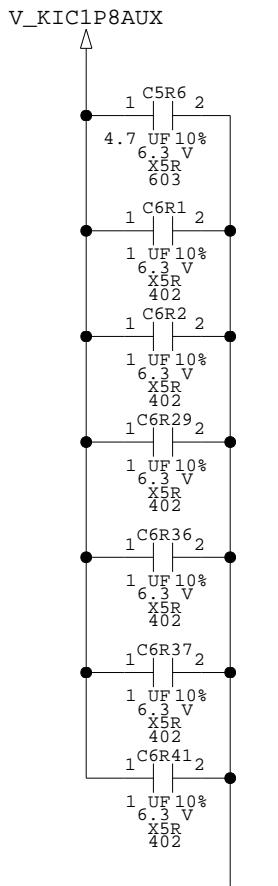
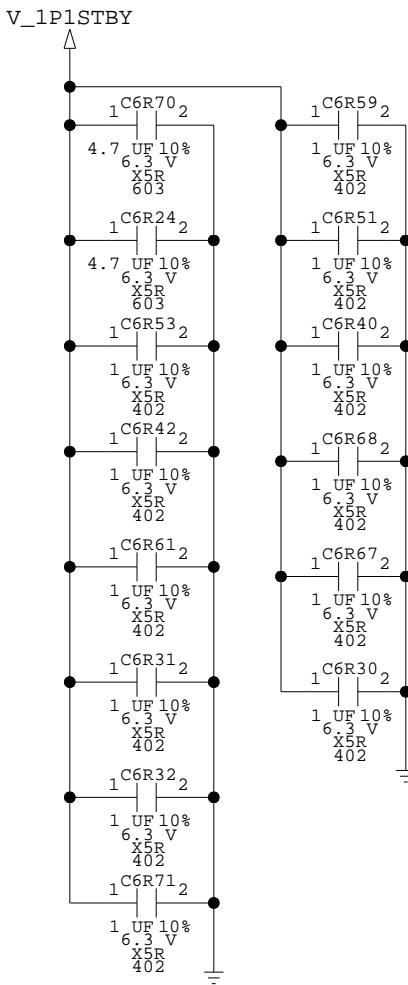
C

B

B

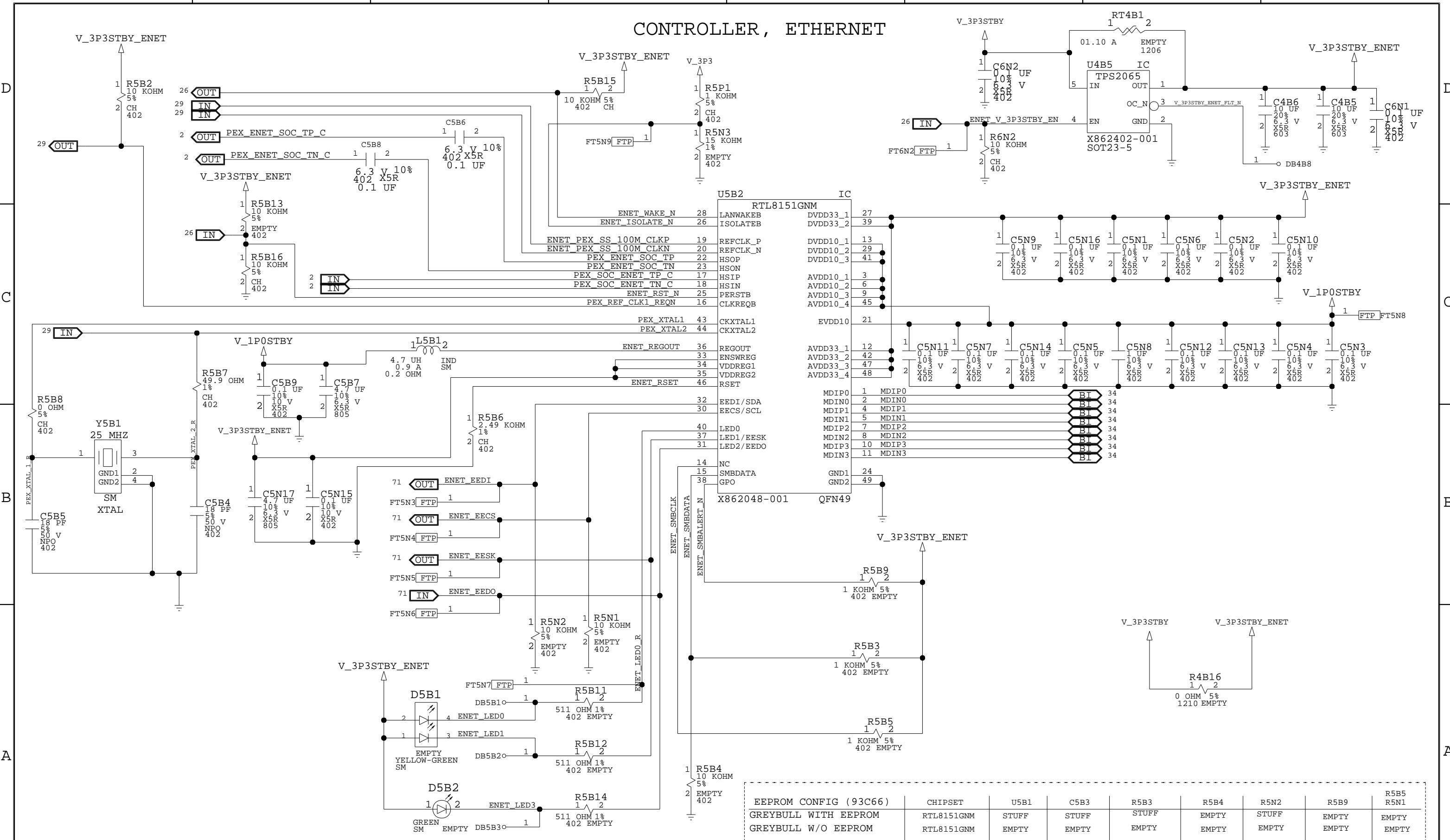
A

A

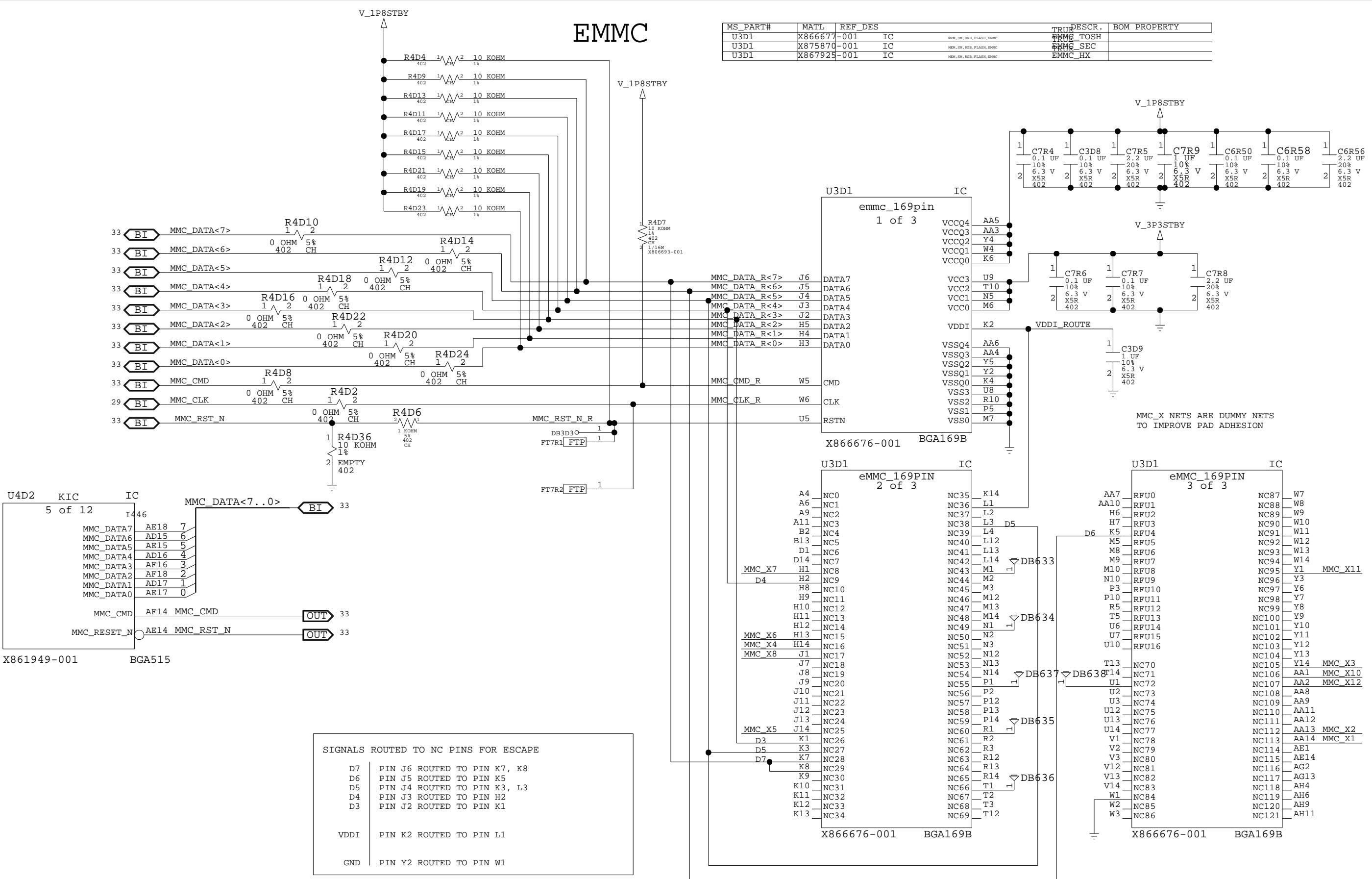


8 7 6 5 4 3 2 1

CONTROLLER, ETHERNET



EEPROM CONFIG (93C66)	CHIPSET	U5B1	C5B3	R5B3	R5B4	R5N2	R5B9	R5B5 R5N1
GREYBULL WITH EEPROM	RTL8151GNM	STUFF	STUFF	STUFF	EMPTY	STUFF	EMPTY	EMPTY
GREYBULL W/O EEPROM	RTL8151GNM	EMPTY						



CONN, RJ45 + TOSLINK

D

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C

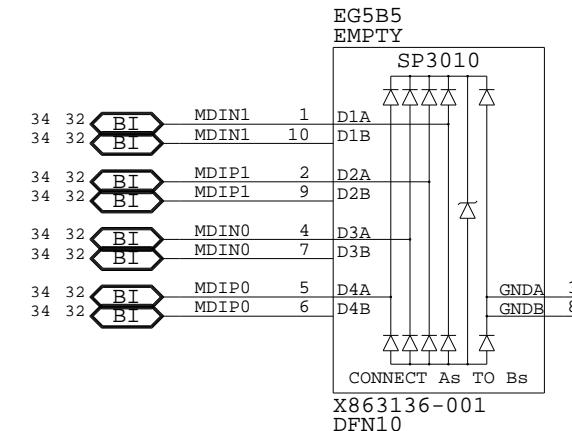
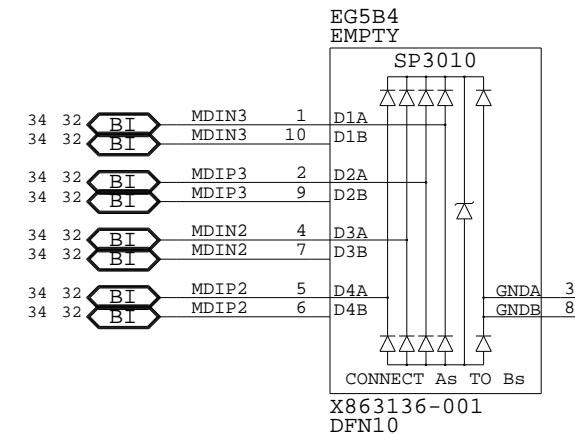
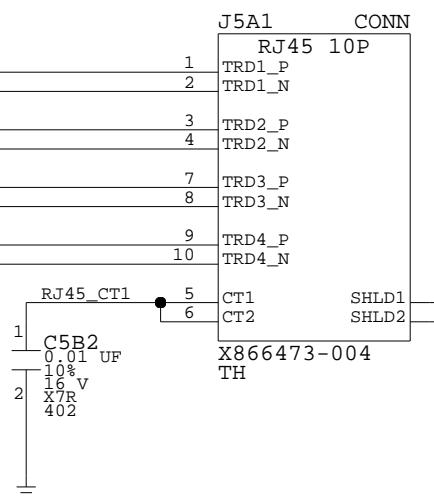
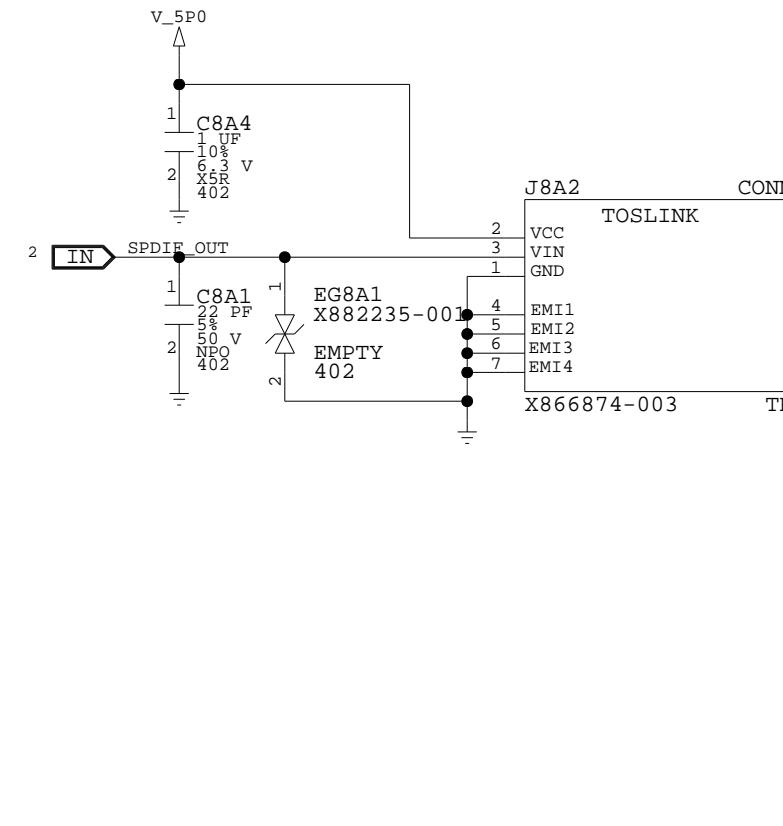
C

B

B

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A



CONN , USB

D

D

C

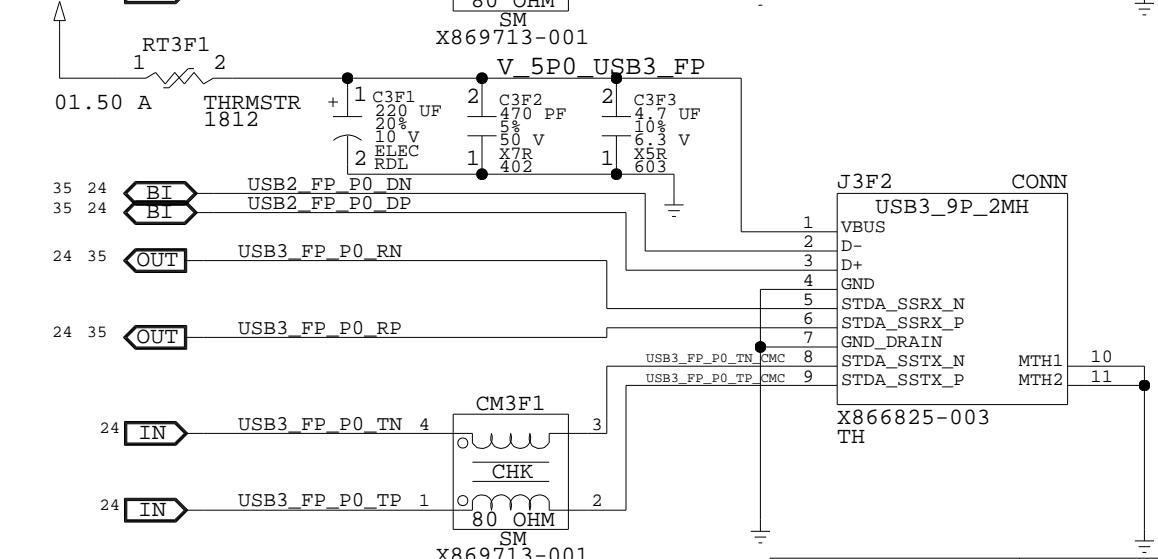
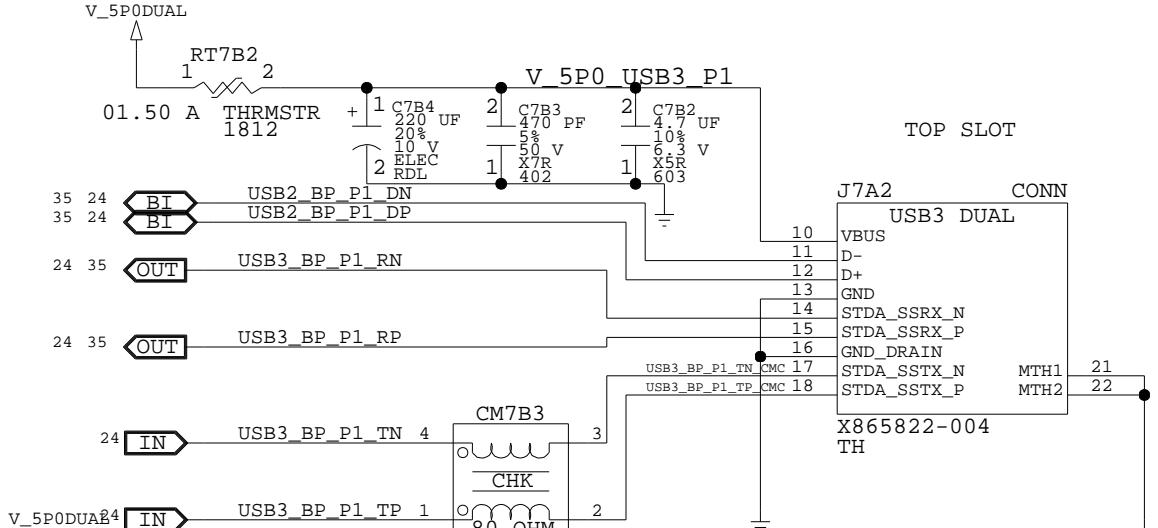
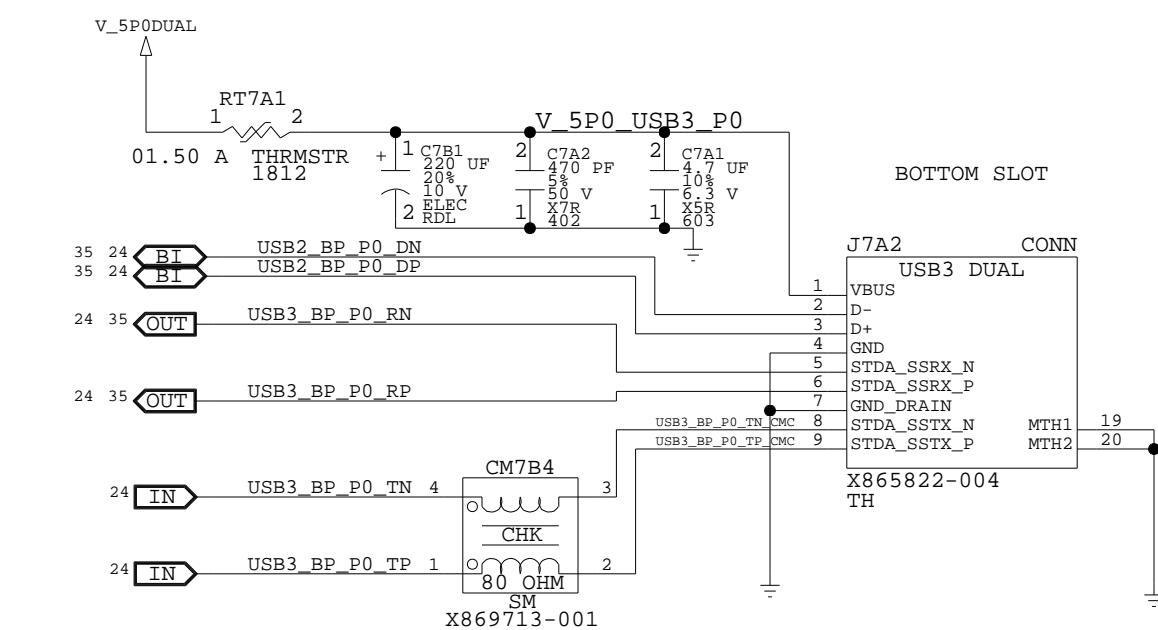
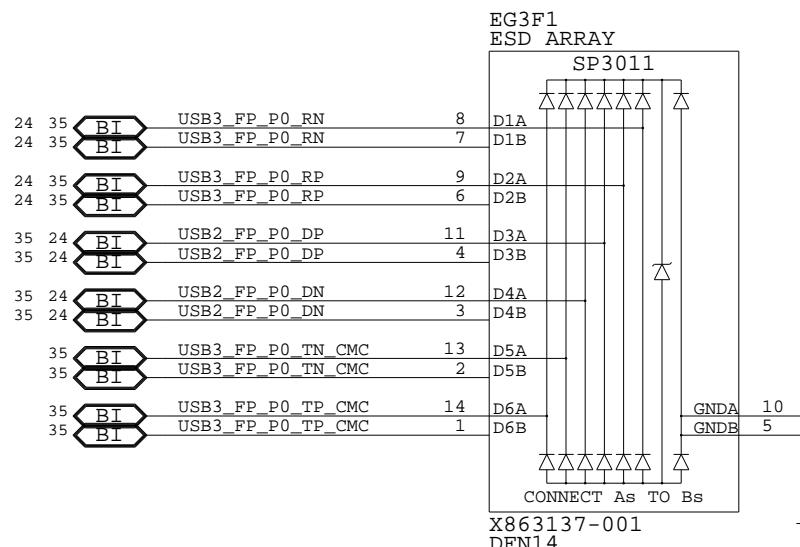
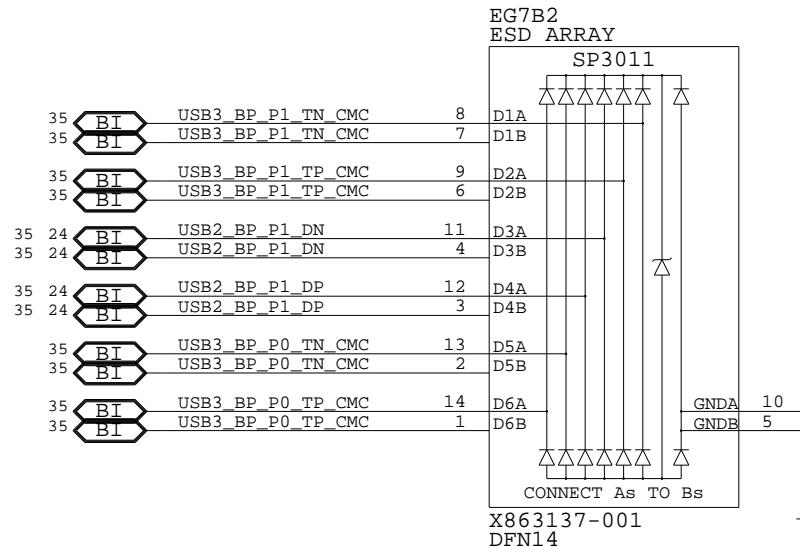
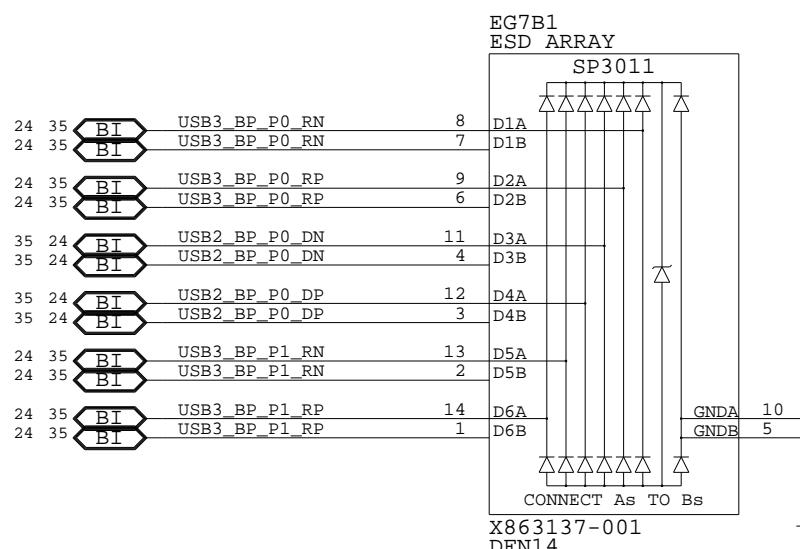
C

B

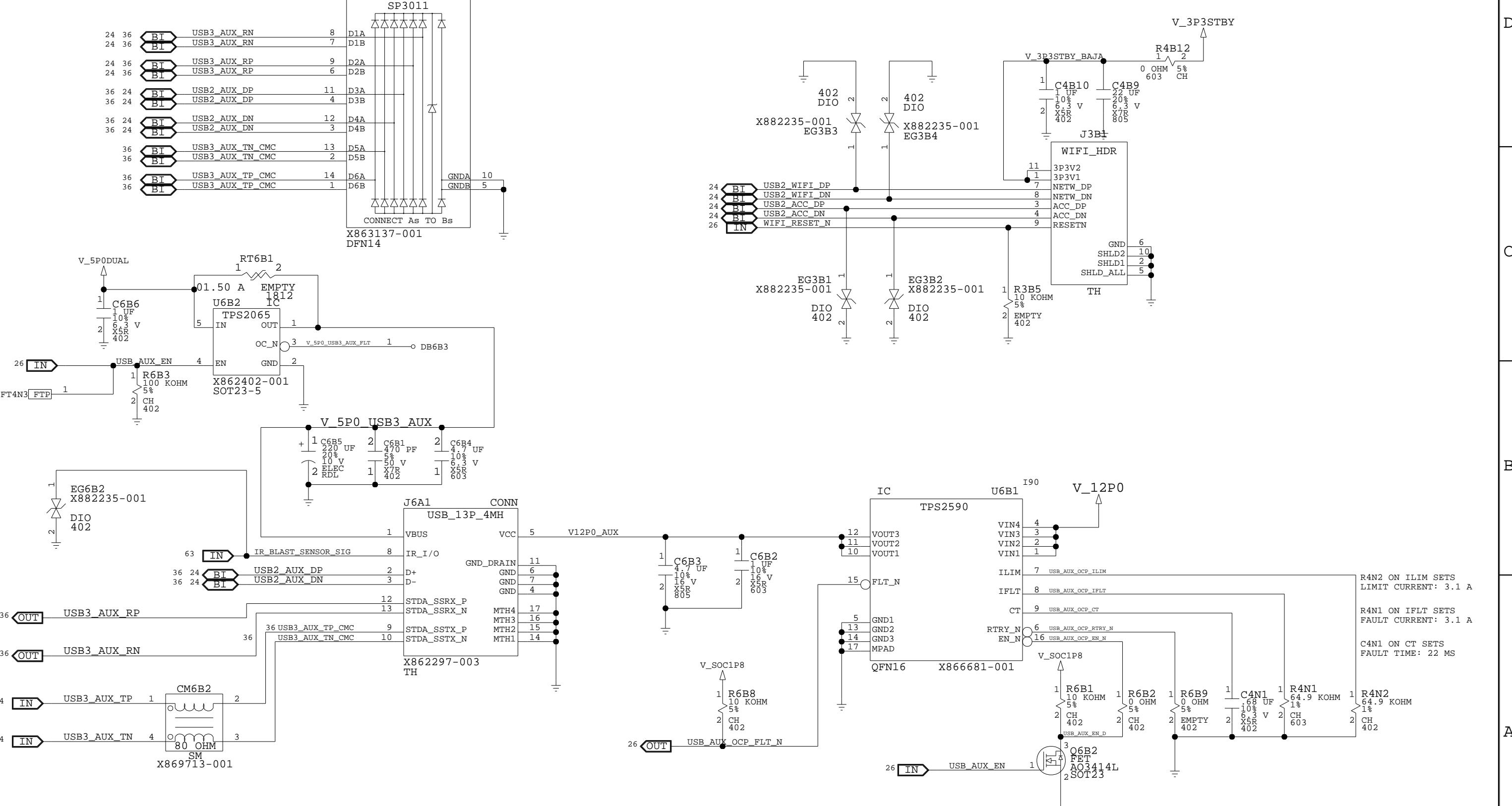
B

A

A



CONN, USB



CONN , HDMI IN

25 OUT TMDS_RX_DP2

25 OUT TMDS_RX_DN2

25 OUT TMDS_RX_DP1

25 OUT TMDS_RX_DN1

25 OUT TMDS_RX_DP0

25 OUT TMDS_RX_DN0

25 OUT TMDS_RX_CLKP

25 OUT TMDS_RX_CLKN

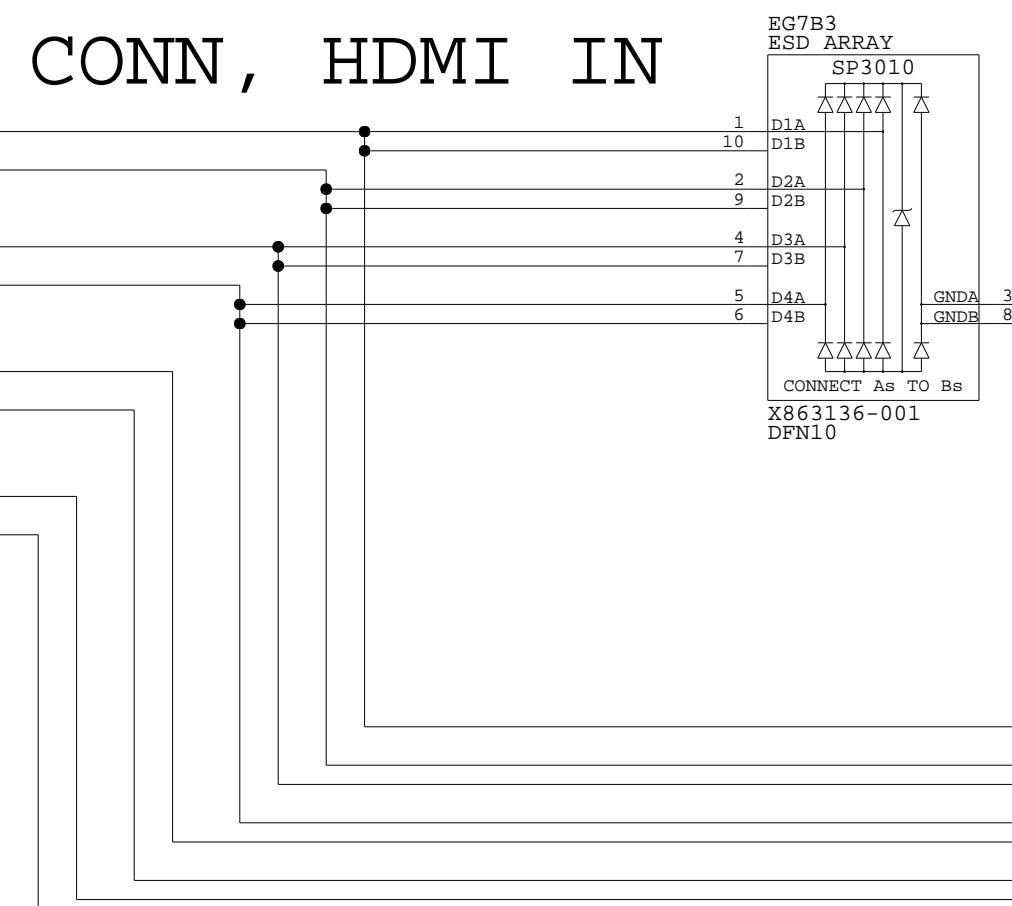
V_3P3STBY
1 R8B19 10 KOHM
2 CH 402

26 OUT HDMI_RX_DDC_5V_E

1 R8B20 0 OHM
2 CH 402
HDMI_RX_DDC_5V_D
SOT-523 EMPTY

1 R8B21 2 KOHM
2 EMPTY 402
U8B2 FET SOT23
1 HDMI_RX_DDC_5V_G 10 KOHM 1% CH
2 603

EG7B4 ESD ARRAY
SP3010 X863136-001 DFN10
1 D1A 10
2 D2A 2
3 D2B 9
4 D3A 4
5 D3B 7
6 D4A 5
7 D4B 6
8 GND
9 GND
CONNECT As TO Bs



EG7B3
ESD ARRAY
SP3010
1 D1A
2 D2A
3 D2B
4 D3A
5 D3B
6 D4A
7 D4B
8 GND
9 GND
CONNECT As TO Bs
X863136-001
DFN10

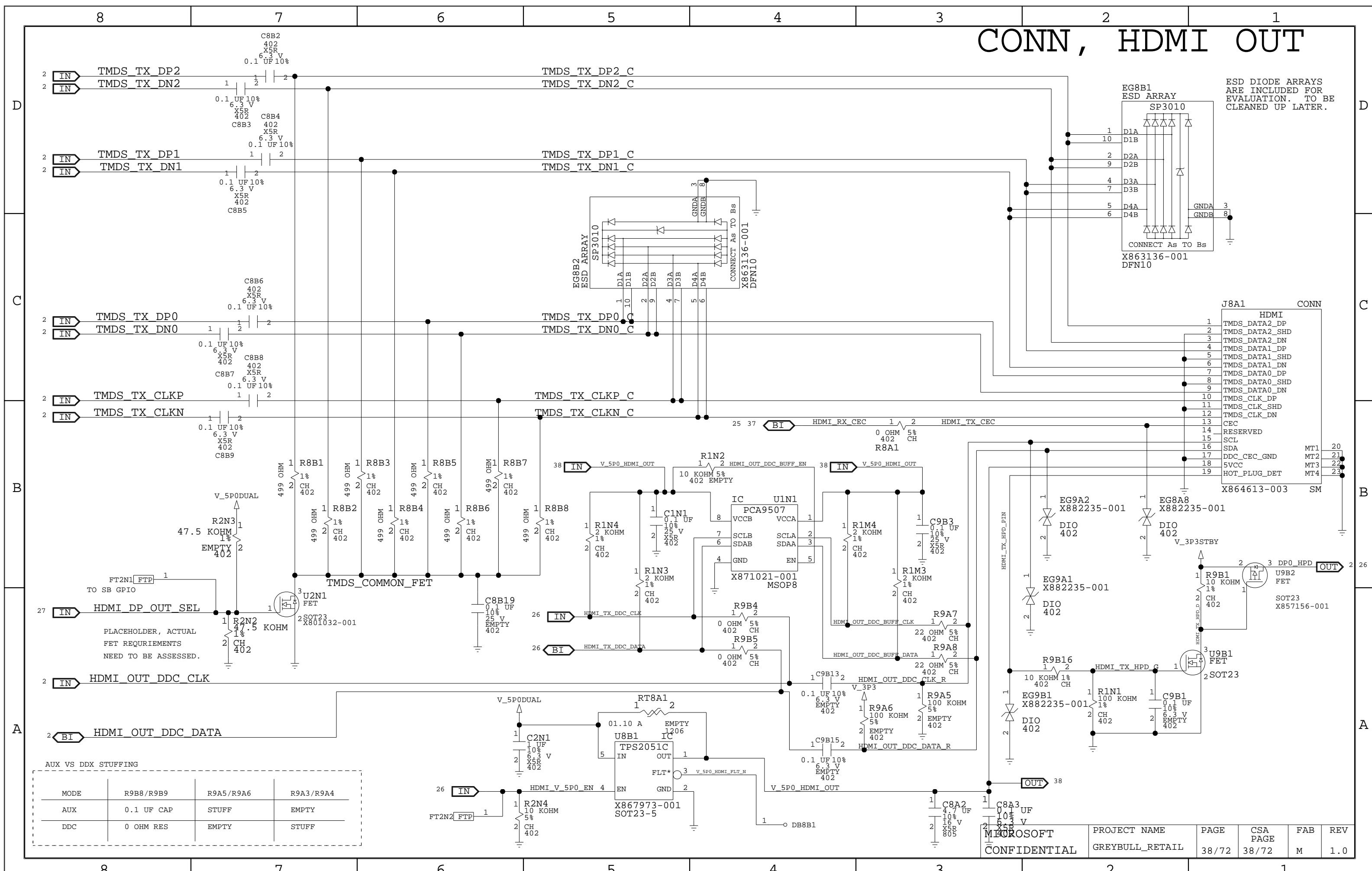
25 BI HDMI_RX_CEC

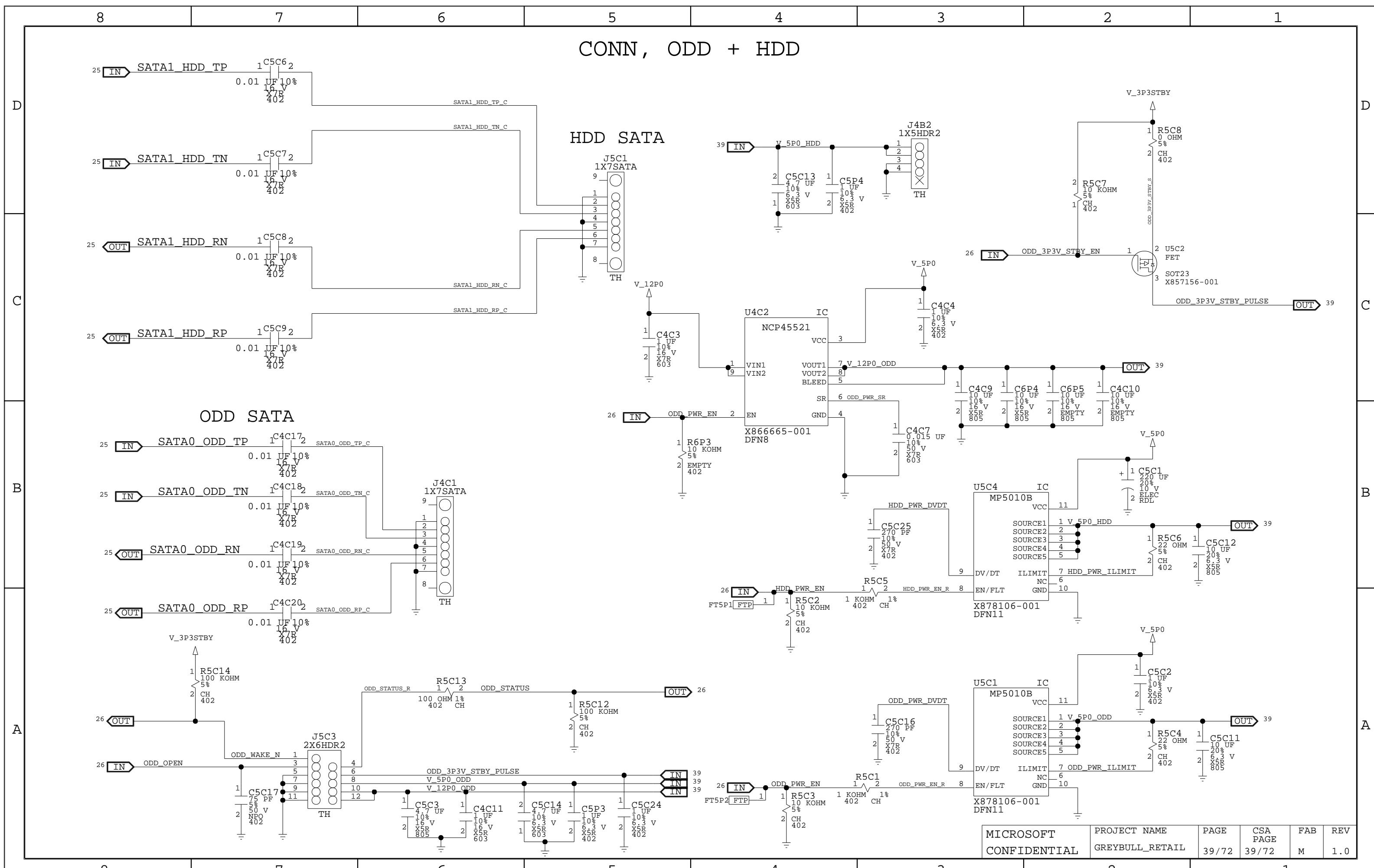
J7A1 CONN
1 TMDS_DATA2_DP
2 TMDS_DATA2_SHD
3 TMDS_DATA2_DN
4 TMDS_DATA1_DP
5 TMDS_DATA1_SHD
6 TMDS_DATA1_DN
7 TMDS_DATA0_DP
8 TMDS_DATA0_SHD
9 TMDS_DATA0_DN
10 TMDS_CLK_DP
11 TMDS_CLK_SHD
12 TMDS_CLK_DN
13 CEC
14 RESERVED
15 SCL
16 SDA
17 DDC_CEC_GND
18 5VCC
19 HOT_PLUG_DET
MT1 20
MT2 21
MT3 22
MT4 23
X864613-003 SM

EG7A9 X882235-001
DIO 402EG8A7 X882235-001
EMPTY 402EG8A7 X882235-001
R8A3 1 KOHM 5% CH
EMPTY 40226 BI HDMI_RX_DDC_CLK
26 BI HDMI_RX_DDC_DATA

EG7A3 X882235-001
DIO 402
EG7A4 X882235-001
DIO 402

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 37/72	CSA PAGE 37/72	FAB M	REV 1.0
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CONN , LITHIUM + FAN

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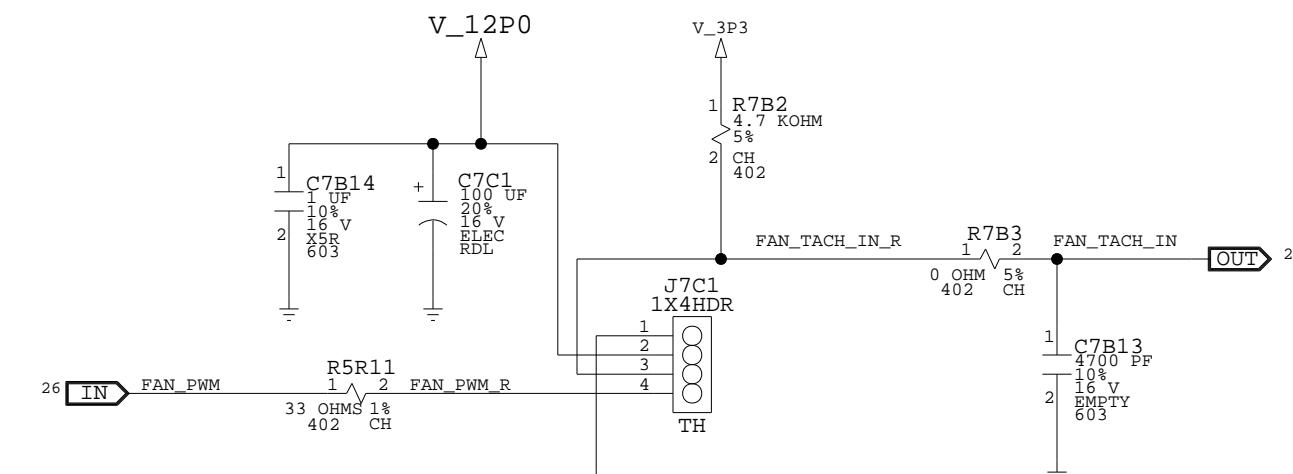
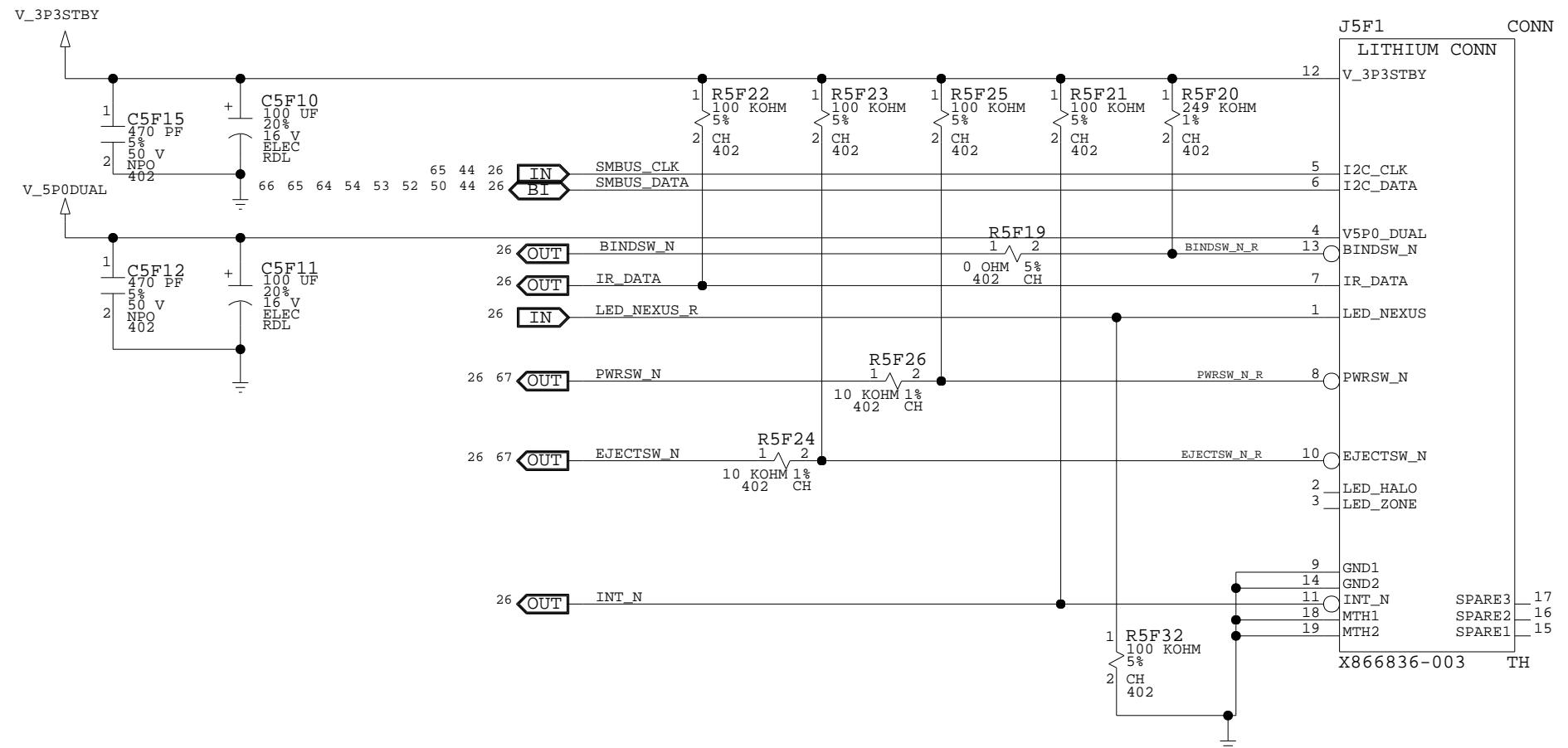
C

B

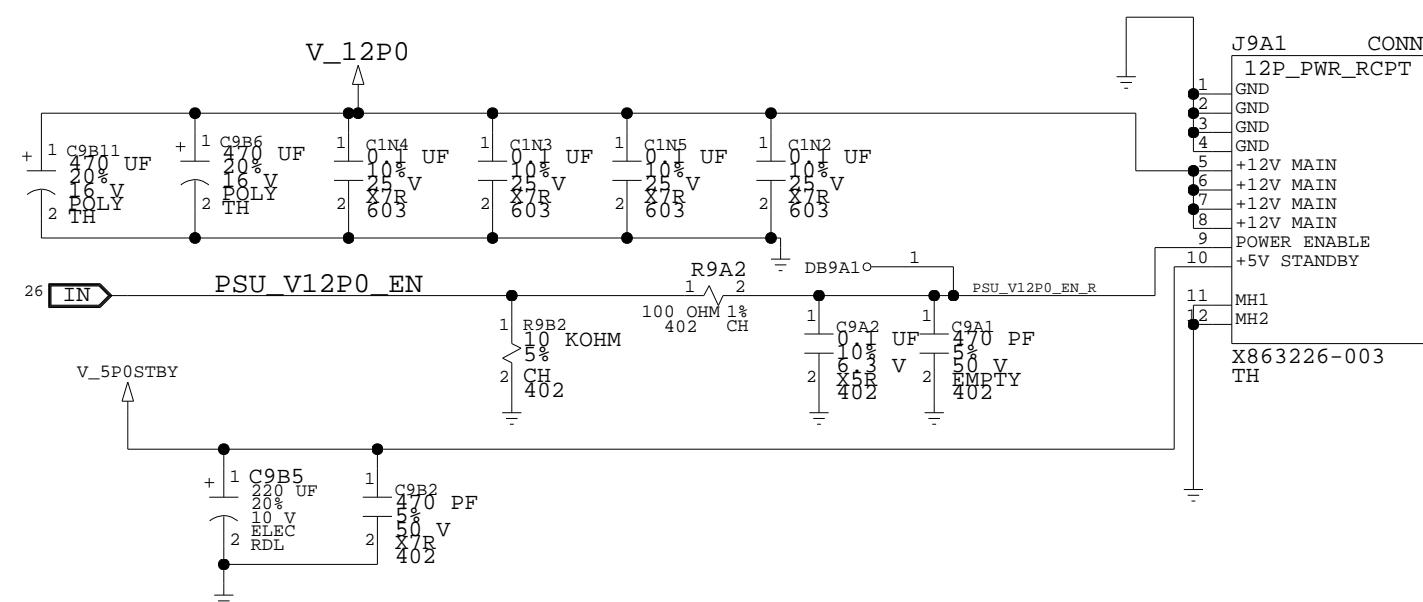
B

A

A



CONN, PWR



D

D

C

C

B

B

A

A

VREGS, BLEEDERS

D

D

C

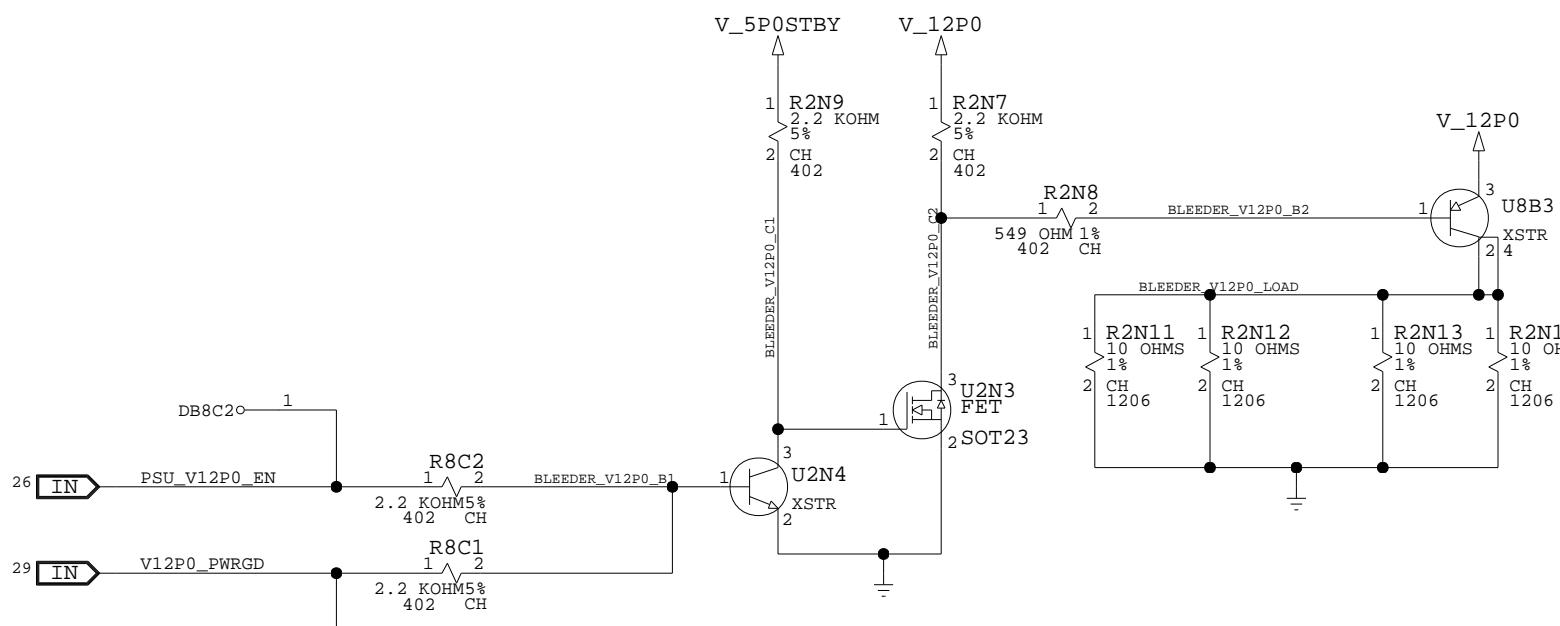
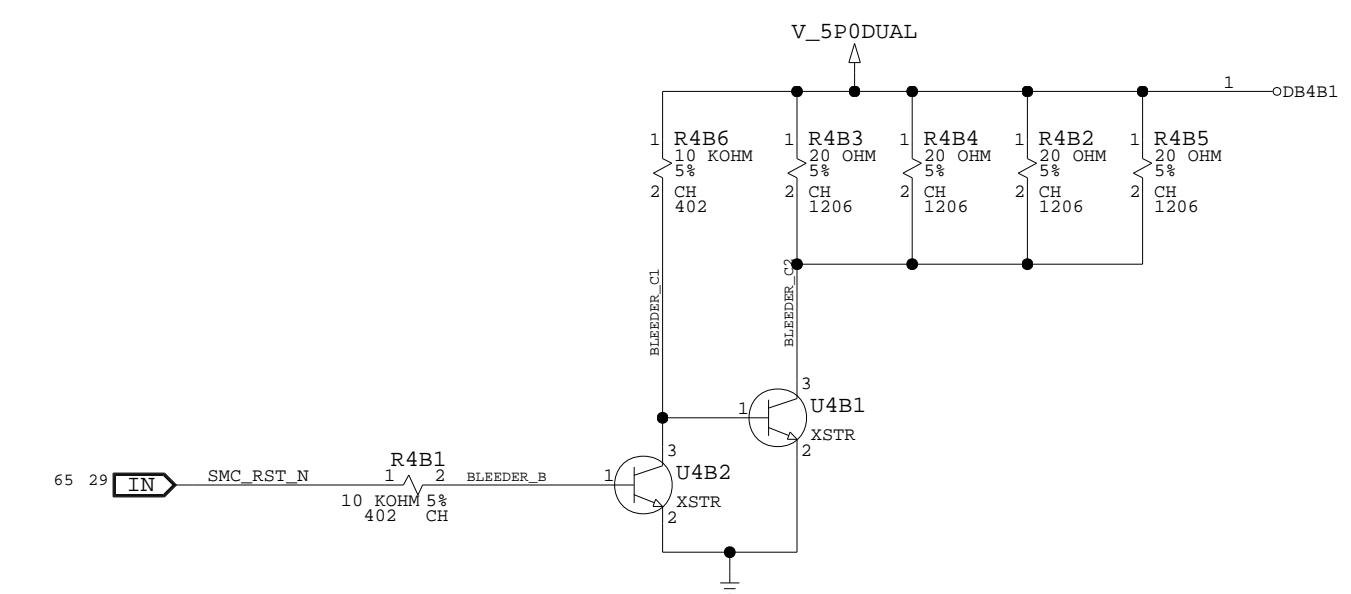
C

B

B

A

A

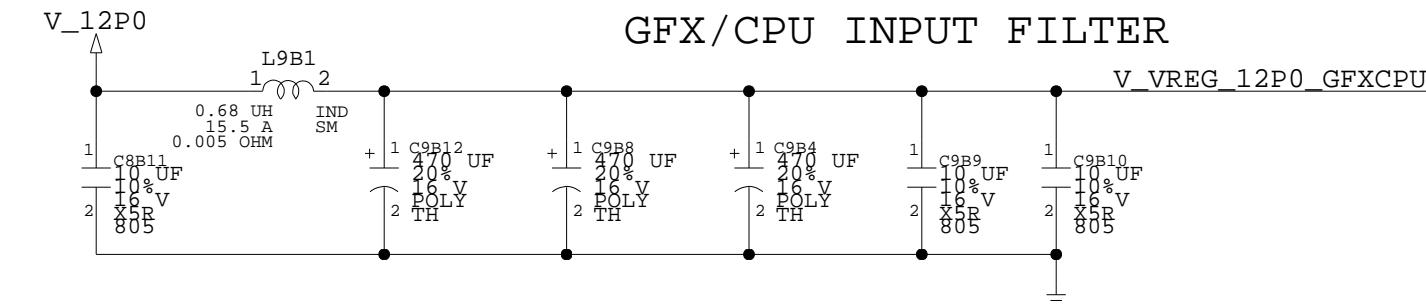
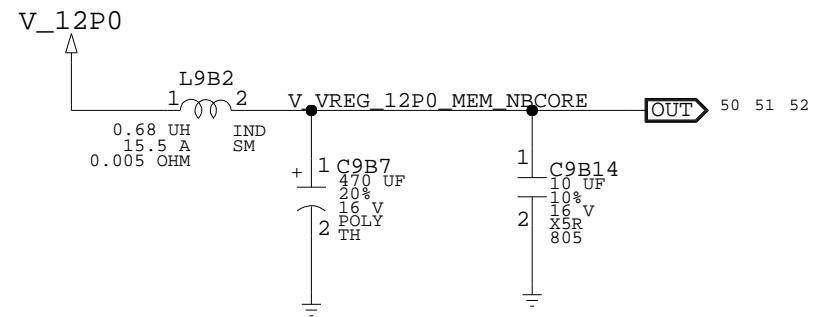
V_{12P0} BLEEDERV_{5P0DUAL} BLEEDER

VREGS, INPUT + OUTPUT FILTERS

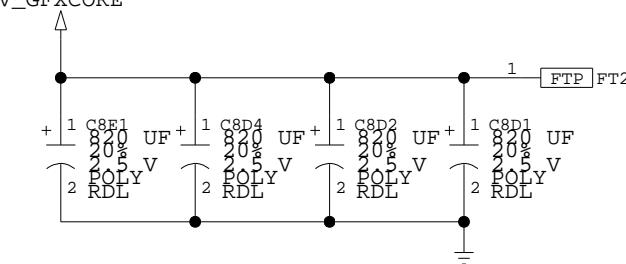
D

D

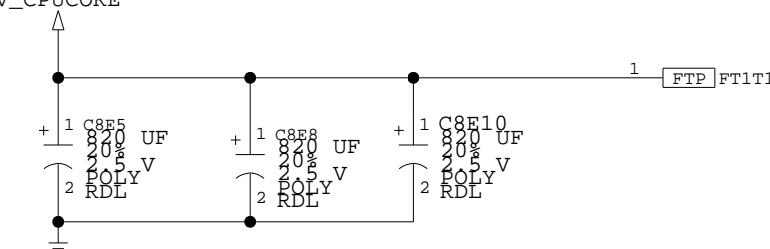
IO/NBCORE/MEMCORE INPUT FILTER



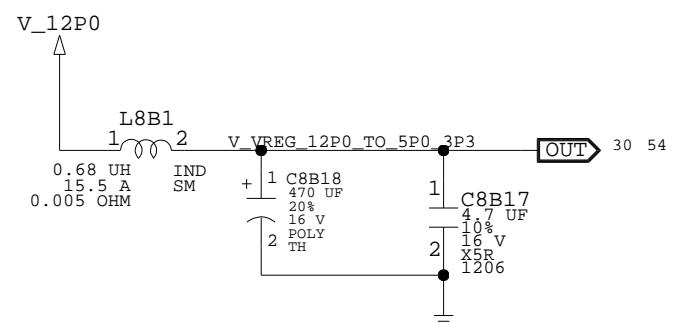
V_GFXCORE OUTPUT FILTER



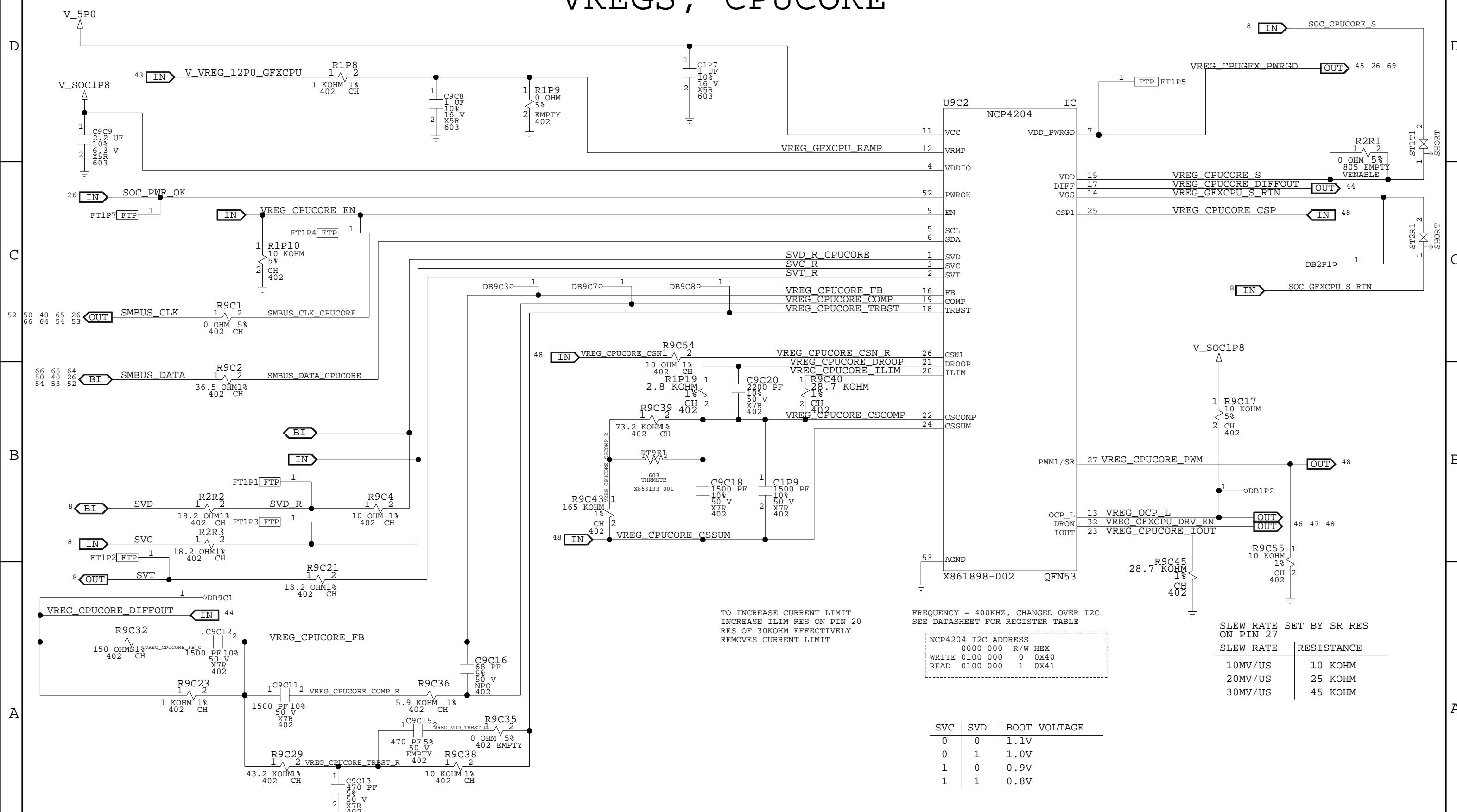
V_CPUUCORE OUTPUT FILTER



5P0/3P3 INPUT FILTER



VREGS, CPUCORE



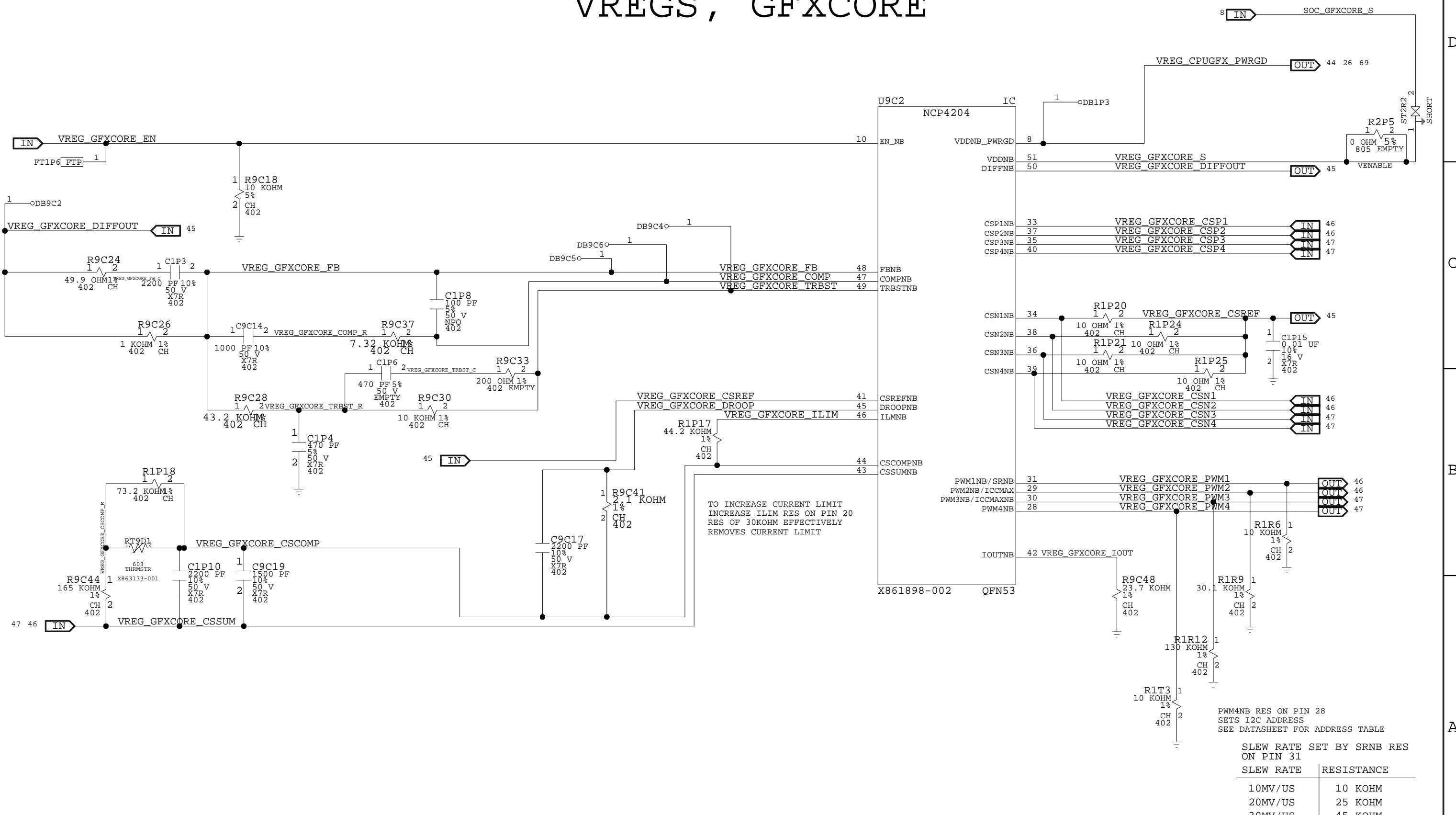
SVC	SVD	BOOT VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

NCP4204 I2C ADDRESS			
0000	000	R/W	HEX
WRITE	0100	000	0
READ	0100	000	1

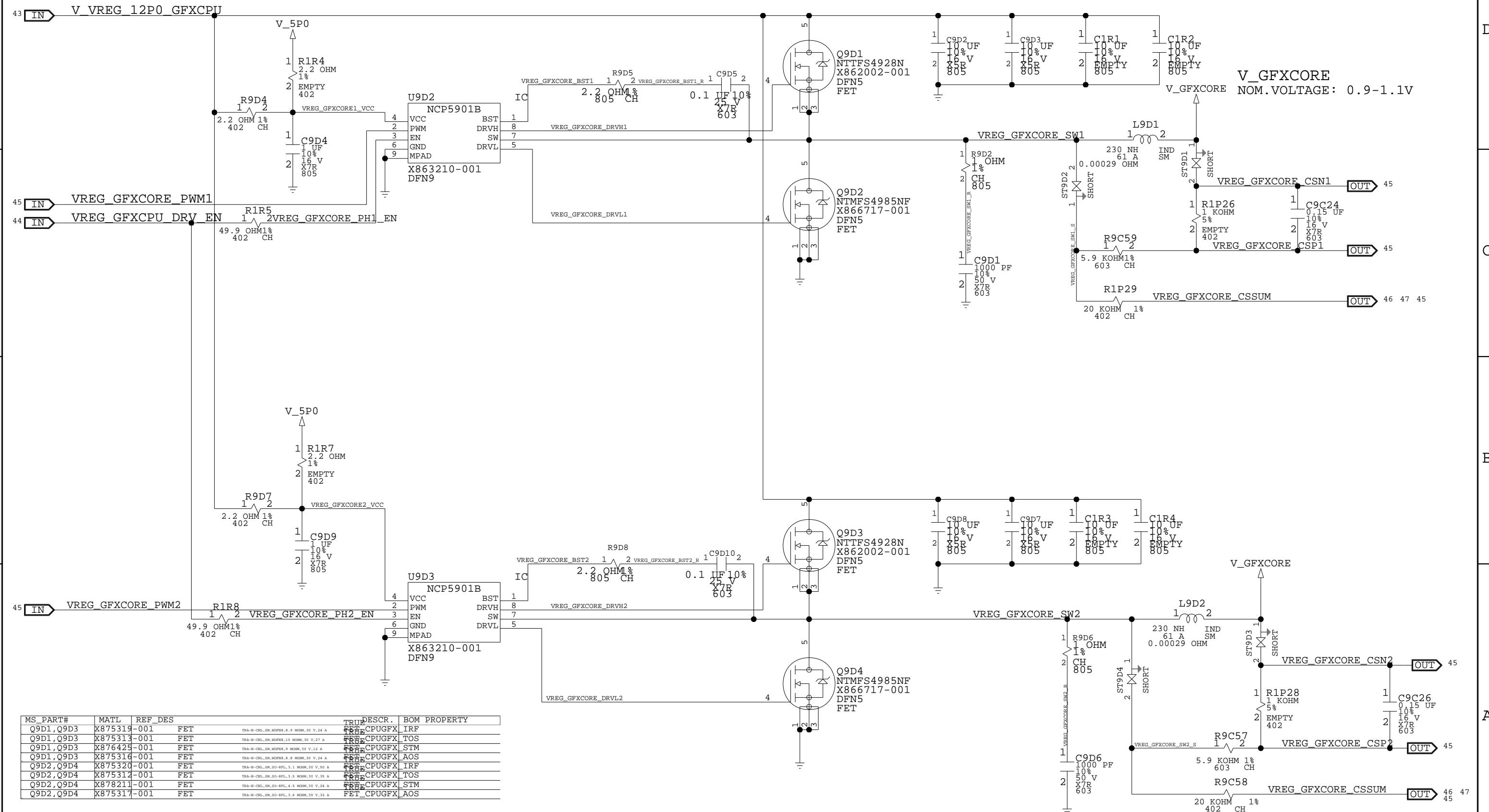
FREQUENCY = 400KHZ, CHANGED OVER I2C
SEE DATASHEET FOR REGISTER TABLE

SLEW RATE	SET BY SR RES ON PIN 27
SLEW RATE	RESISTANCE
10MV/US	10 KOHM
20MV/US	25 KOHM
30MV/US	45 KOHM

VREGS , GFXCORE

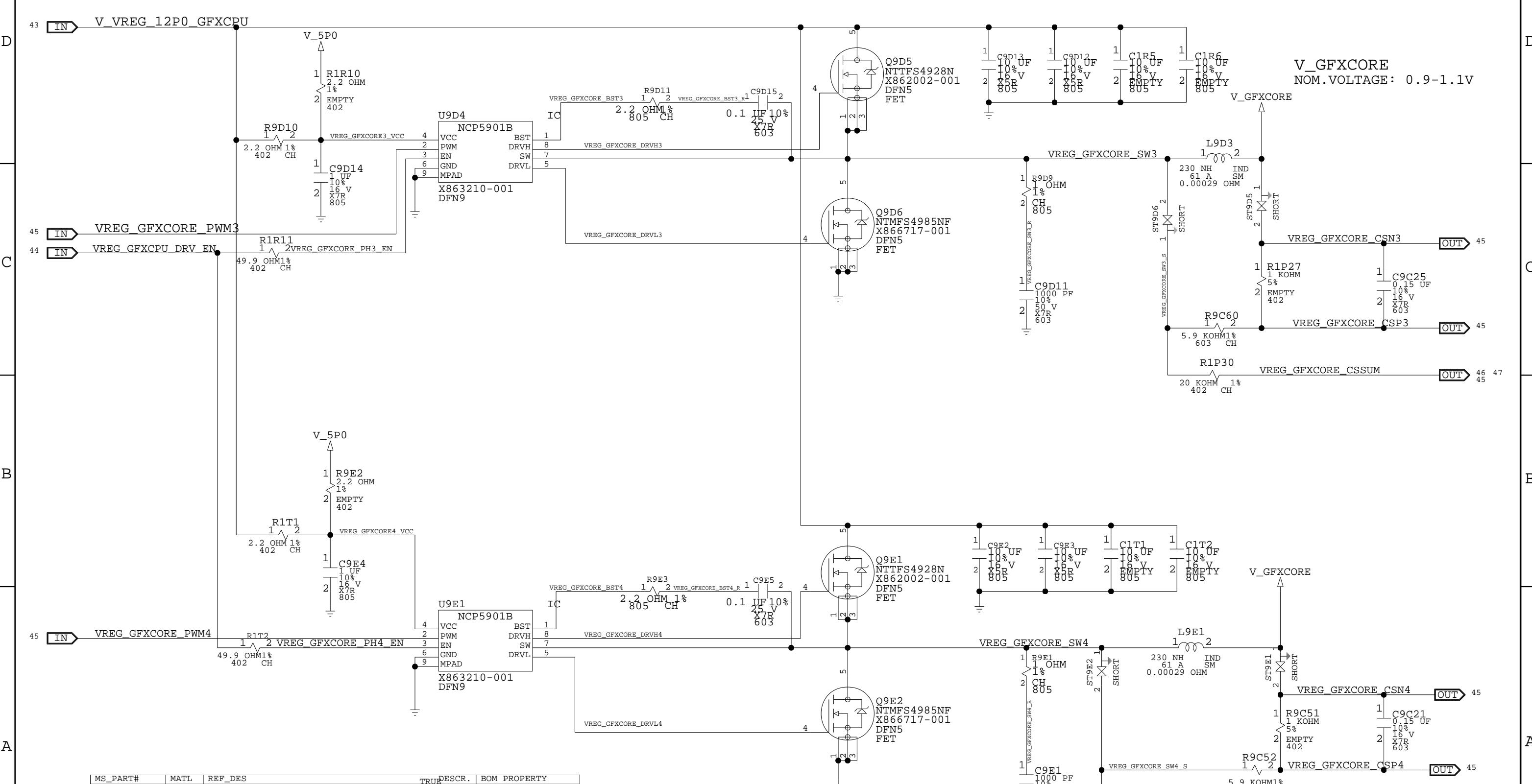


VREGS , GFXCORE OUTPUT PHASE 1 & 2



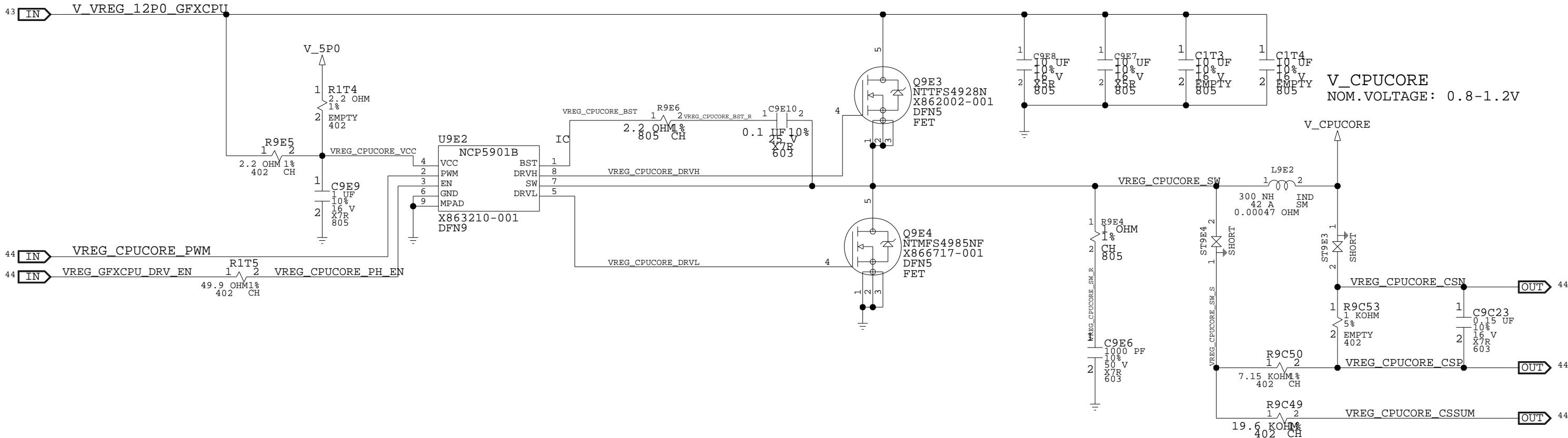
MS_PART#	MATL	REF_DES	TRU	DESCR.	BOM	PROPERTY
Q9D1,Q9D3	X875319-001	FET	TRA-N-CNL	SM_WDFN8_8.9 MOHN,30 V, 24 A	TRUE	CPUGFX
Q9D1_Q9D3	X875313-001	FET	TRA-N-CNL	SM_WDFN8_10 MOHN,30 V, 27 A	TRUE	CPUGFX
Q9D1_Q9D3	X876425-001	FET	TRA-N-CNL	SM_WDFN8_9 MOHN,30 V, 12 A	TRUE	CPUGFX
Q9D1_Q9D3	X875316-001	FET	TRA-N-CNL	SM_WDFN8_8.8 MOHN,30 V, 24 A	TRUE	CPUGFX
Q9D2_Q9D4	X875320-001	FET	TRA-N-CNL	SM_SF-8FL_3.1 MOHN,30 V,50 A	TRUE	CPUGFX
Q9D2_Q9D4	X875312-001	FET	TRA-N-CNL	SM_SF-8FL_3.5 MOHN,30 V, 35 A	TRUE	CPUGFX
Q9D2_Q9D4	X878211-001	FET	TRA-N-CNL	SM_SF-8FL_4.5 MOHN,30 V, 24 A	TRUE	CPUGFX
Q9D2_Q9D4	X875317-001	FET	TRA-N-CNL	SM_SF-8FL_3.6 MOHN,30 V, 32 A	TRUE	CPUGFX

VREGS , GFXCORE OUTPUT PHASE 3 & 4



MS_PART#	MATL	REF_DESC	TRUE_DESCR.	BOM	PROPERTY
Q9D5_Q9E1	X8753139-001	FET	TRA-N-CNL_SM_NDFN8_8.9 MOHM_30_V_24_A	TRUE	CPUGFX
Q9D5_Q9E1	X8753133-001	FET	TRA-N-CNL_SM_NDFN8_10 MOHM_30_V_27_A	TRUE	CPUGFX
Q9D5_Q9E1	X876425-001	FET	TRA-N-CNL_SM_NDFN8_9 MOHM_30_V_12_A	TRUE	CPUGFX
Q9D5_Q9E1	X8753136-001	FET	TRA-N-CNL_SM_NDFN8_8.8 MOHM_30_V_24_A	TRUE	CPUGFX
Q9D6_Q9E2	X875320-001	FET	TRA-N-CNL_SM_SO-BP12-3.1 MOHM_30_V_50_A	TRUE	CPUGFX
Q9D6_Q9E2	X875312-001	FET	TRA-N-CNL_SM_SO-BP12-3.5 MOHM_30_V_35_A	TRUE	CPUGFX
Q9D6_Q9E2	X878211-001	FET	TRA-N-CNL_SM_SO-BP12-4.5 MOHM_30_V_24_A	TRUE	CPUGFX
Q9D6_Q9E2	X8753137-001	FET	TRA-N-CNL_SM_SO-BP12-3.6 MOHM_30_V_32_A	TRUE	CPUGFX

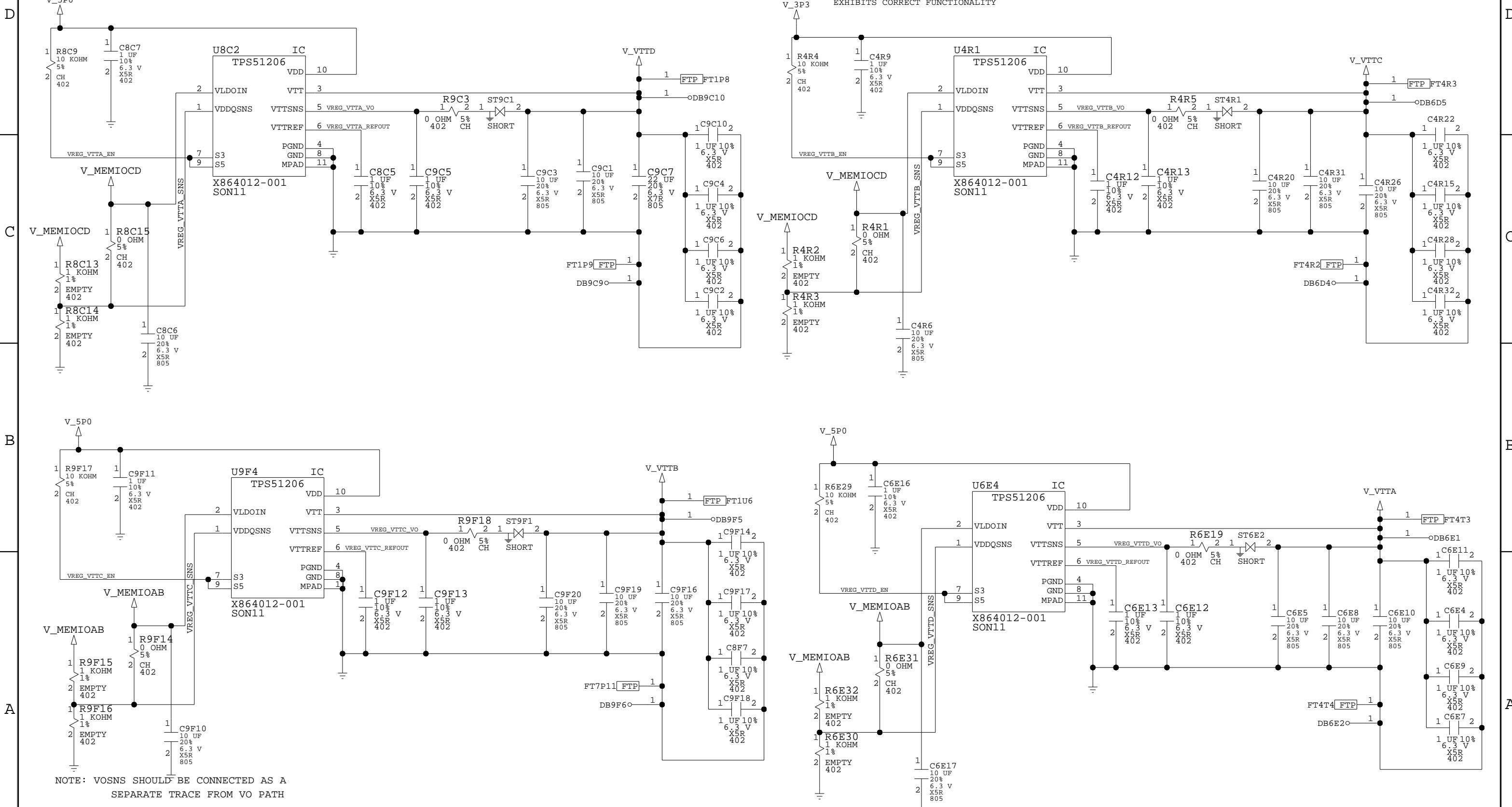
VREGS , CPUCORE OUTPUT PHASE



MS_PART#	MATL	REF_DES	TRUE DESCRI.	BOM PROPERTY
Q9E3	X875319-001	FET	TRA-N-CNL,SM,MDP88,1.9 MOHM,30 V,24 A	TRUE_CPUUGFX,IRF
Q9E3	X875313-001	FET	TRA-N-CNL,SM,MDP88,1.0 MOHM,30 V,27 A	TRUE_CPUUGFX,TOS
Q9E3	X876425-001	FET	TRA-N-CNL,SM,MDP88,9 MOHM,30 V,12 A	TRUE_CPUUGFX,STM
Q9E3	X875316-001	FET	TRA-N-CNL,SM,MDP88,1.8 MOHM,30 V,28 A	TRUE_CPUUGFX,AOS
Q9E4	X875320-001	FET	TRA-N-CNL,SM,SO-SFL,3.1 MOHM,30 V,50 A	TRUE_CPUUGFX,IRF
Q9E4	X875312-001	FET	TRA-N-CNL,SM,SO-SFL,3.5 MOHM,30 V,75 A	TRUE_CPUUGFX,TOS
Q9E4	X878211-001	FET	TRA-N-CNL,SM,SO-SFL,4.5 MOHM,30 V,24 A	TRUE_CPUUGFX,STM
Q9E4	X875317-001	FET	TRA-N-CNL,SM,SO-SFL,3.6 MOHM,30 V,32 A	TRUE_CPUUGFX,AOS

VREGS , VTT TERMINATION

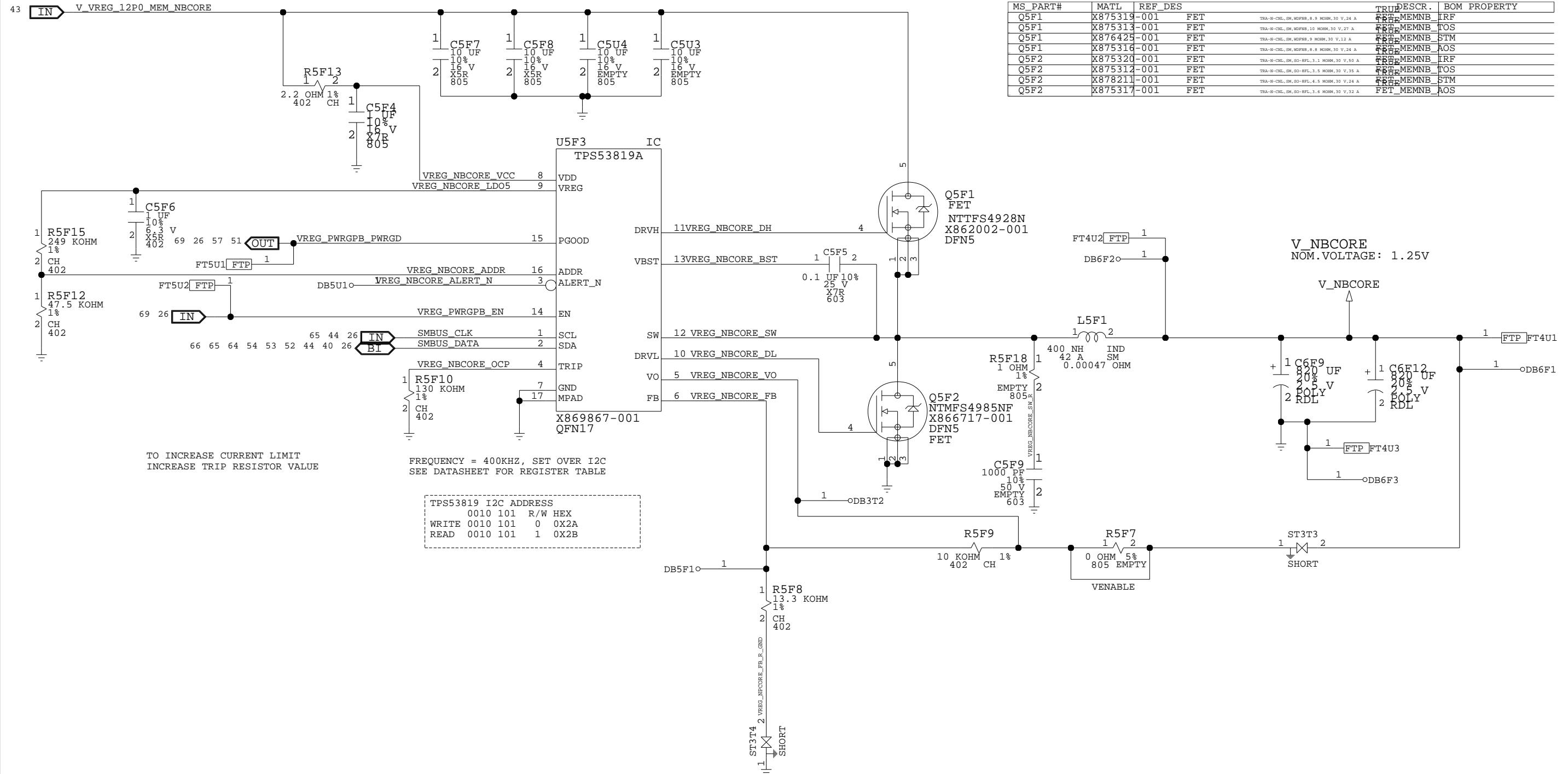
POWERED BY V3P3 DUE TO
PHYSICAL LAYOUT CONSTRAINTS
EXHIBITS CORRECT FUNCTIONALITY



VREGS , NBCORE

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D



VREGS , MEMCORE

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D

C

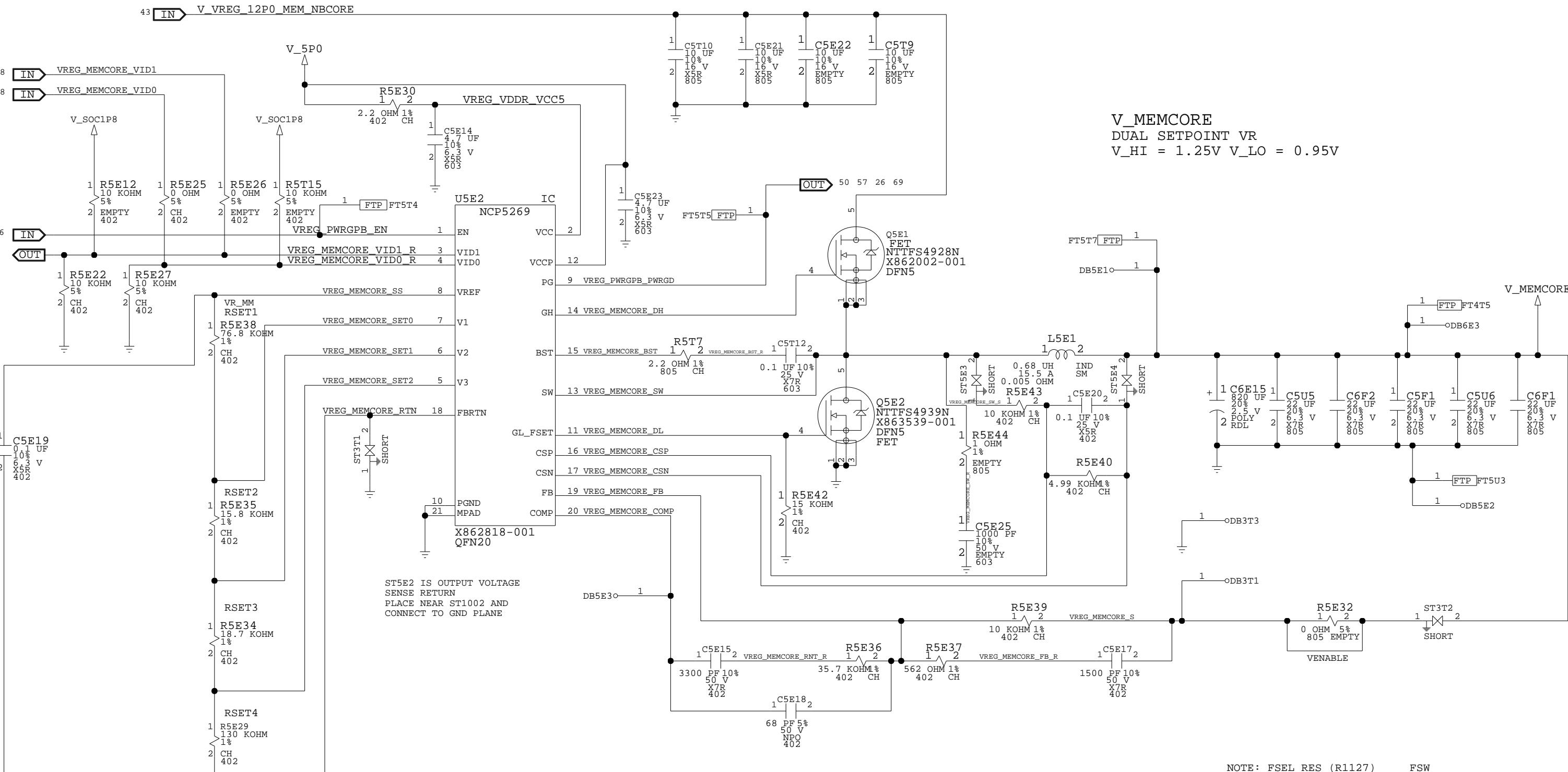
C

B

B

A

A



MS PART#	MATL	REF DES	TRUE DESCRIPT.	BOM	PROPERTY
Q5E1	X875319-001	FET	TRA-H-CNL,SM,MDFNS,8.9 MOHM,30 V,24 A	TRUE	MEMNB, IRF
Q5E1	X875313-001	FET	TRA-H-CNL,SM,MDFNS,10 MOHM,30 V,27 A	TRUE	MEMNB, TGS
Q5E1	X876425-001	FET	TRA-H-CNL,SM,MDFNS,9 MOHM,30 V,12 A	TRUE	MEMNB, STM
Q5E1	X875316-001	FET	TRA-H-CNL,SM,MDFNS,8.8 MOHM,30 V,24 A	TRUE	MEMNB, AOS
Q5E2	X875318-001	FET	TRA-H-CNL,SM,MDFNS,6.3 MOHM,30 V,24 A	TRUE	MEMNB, IRF
Q5E2	X875314-001	FET	TRA-H-CNL,SM,MDFNS,5.4 MOHM,30 V,27 A	TRUE	MEMNB, TGS
Q5E2	X876423-001	FET	TRA-H-CNL,SM,MDFNS,4.5 MOHM,30 V,17 A	TRUE	MEMNB, STM
Q5E2	X875315-001	FET	TRA-H-CNL,SM,MDFNS,5 MOHM,30 V,30 A	FET	MEMNB, AOS

NOTE: FSEL RES (R1127)

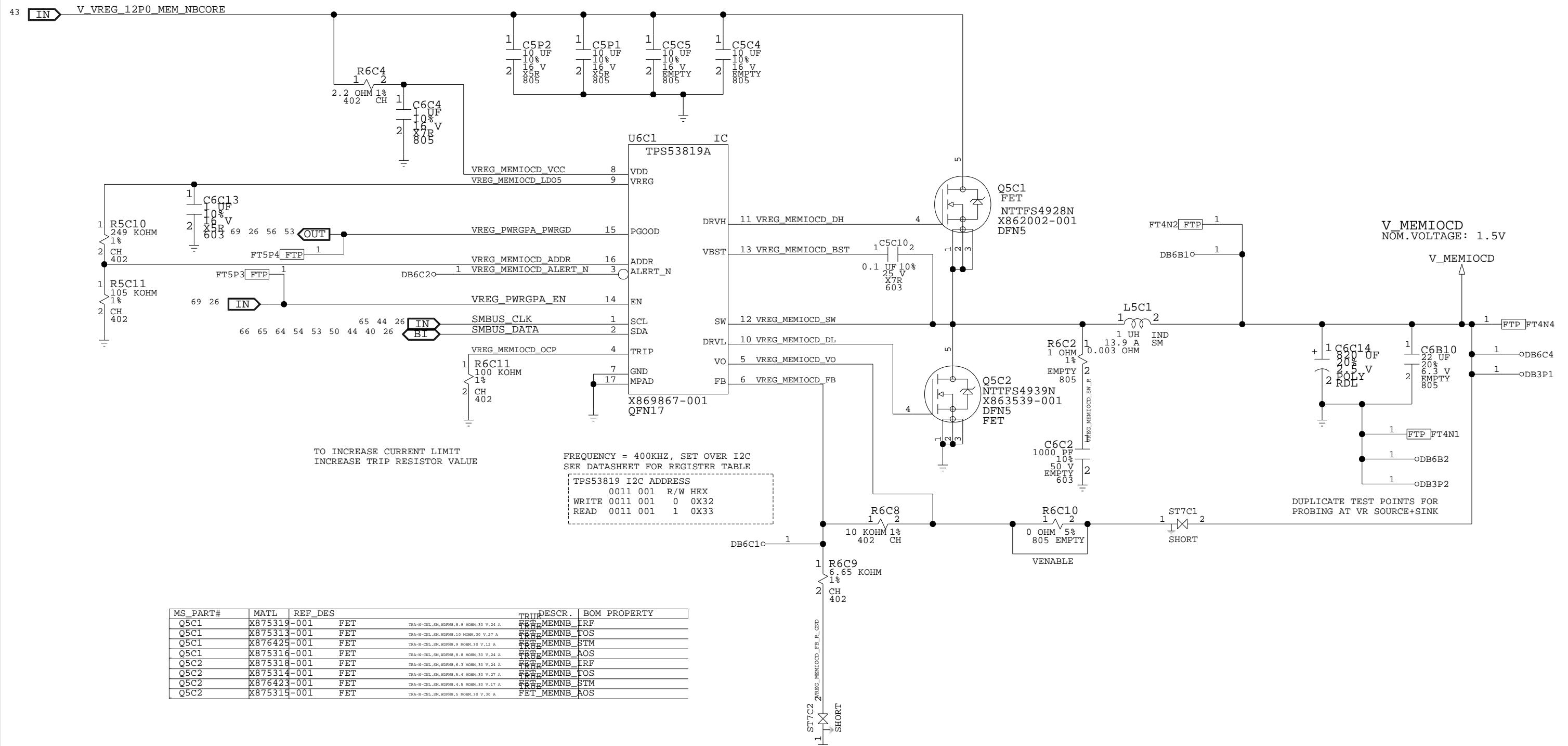
FSW	2K	300KHZ
	6K	400KHZ
	15K	600KHZ

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 51/72	CSA PAGE 51/72	FAB M	REV 1.0
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D

D

VREG, MEMIOCD

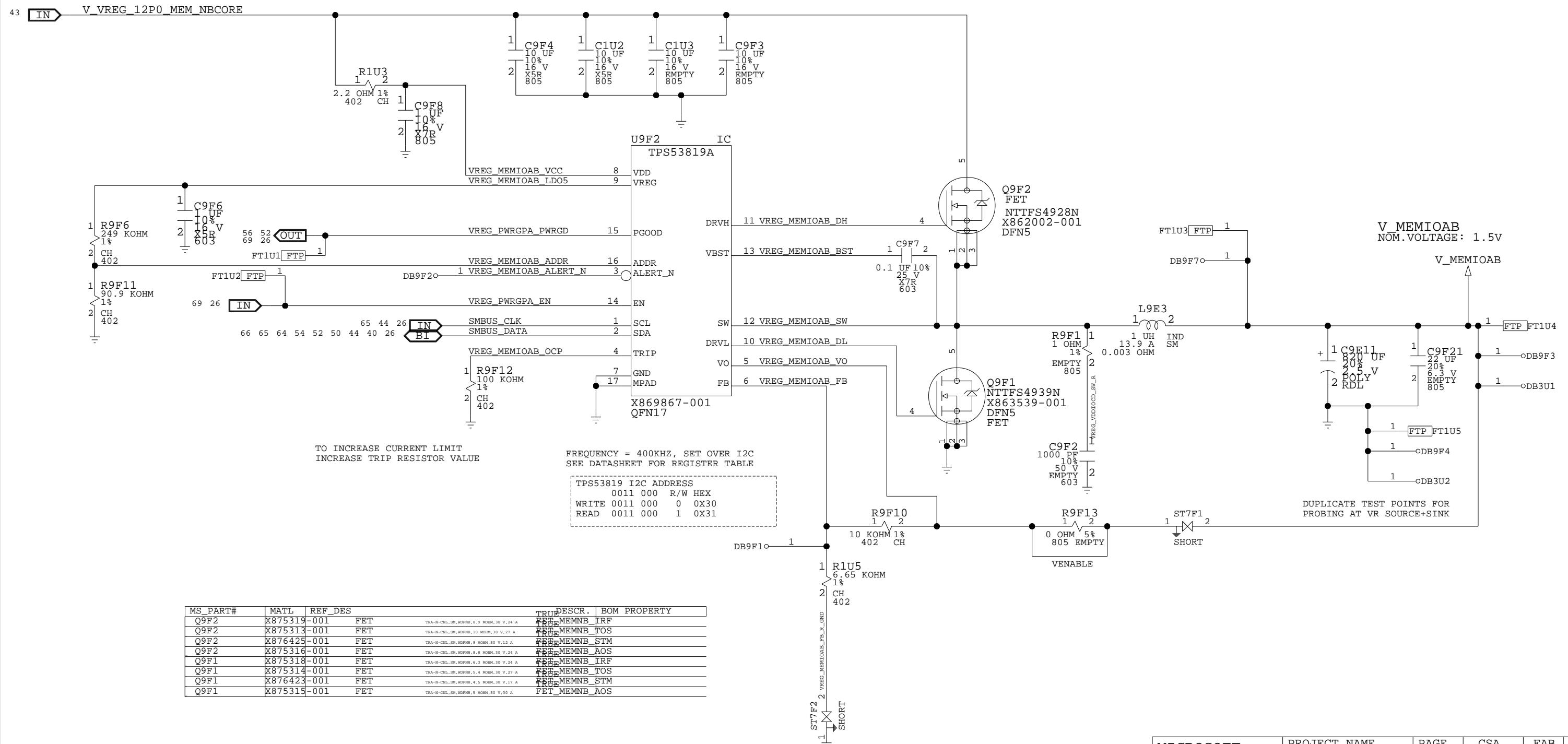


MS_PART#	MATL	REF_DES	TRIP	DESCR.	BOM PROPERTY
Q5C1	X875319-001	FET	TPS53819	FET_MEMNB_IRF	
Q5C1	X875313-001	FET	TPS53819	FET_MEMNB_TOS	
Q5C1	X876425-001	FET	TPS53819	FET_MEMNB_STM	
Q5C1	X875316-001	FET	TPS53819	FET_MEMNB_AOS	
Q5C2	X875318-001	FET	TPS53819	FET_MEMNB_IRF	
Q5C2	X875314-001	FET	TPS53819	FET_MEMNB_TOS	
Q5C2	X876423-001	FET	TPS53819	FET_MEMNB_STM	
Q5C2	X875315-001	FET	TPS53819	FET_MEMNB_AOS	

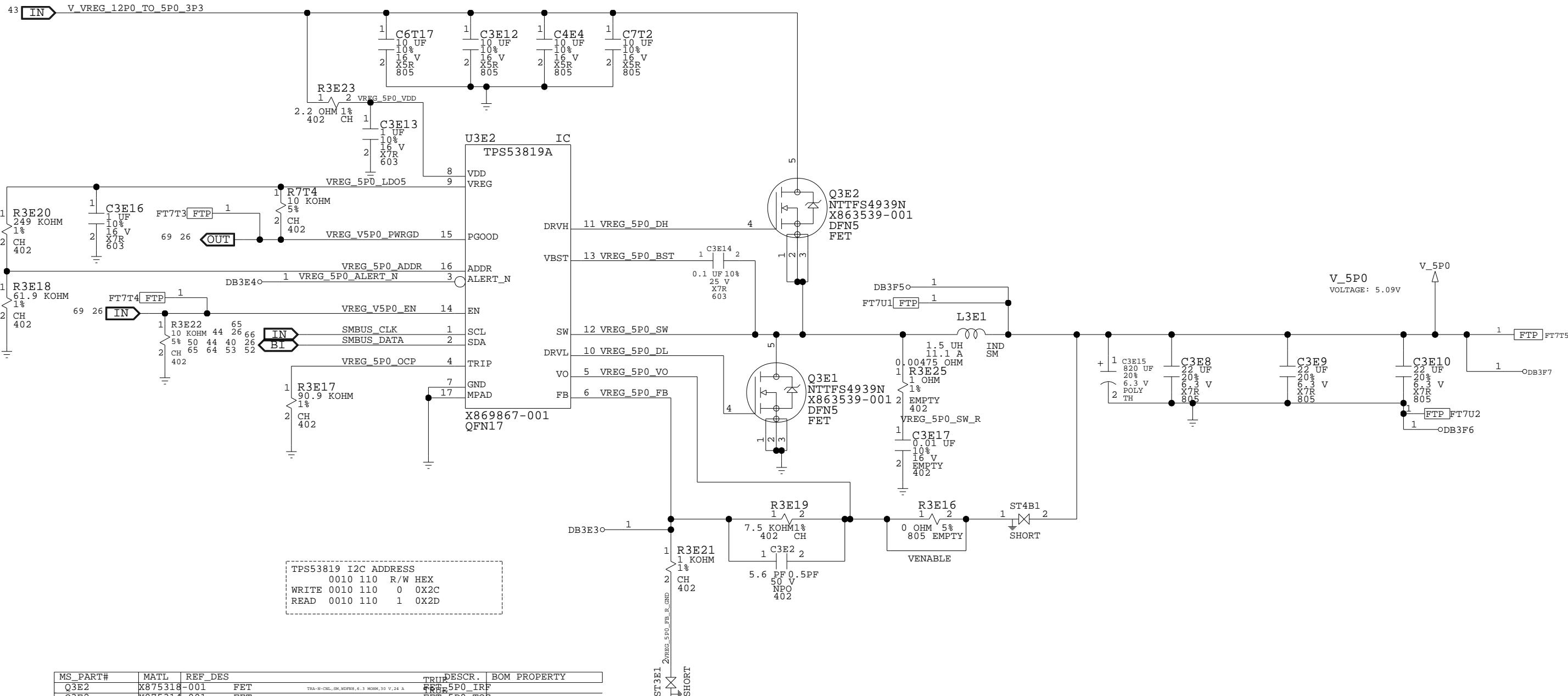
D

D

VREG , MEMIOAB



VREGS, V5P0

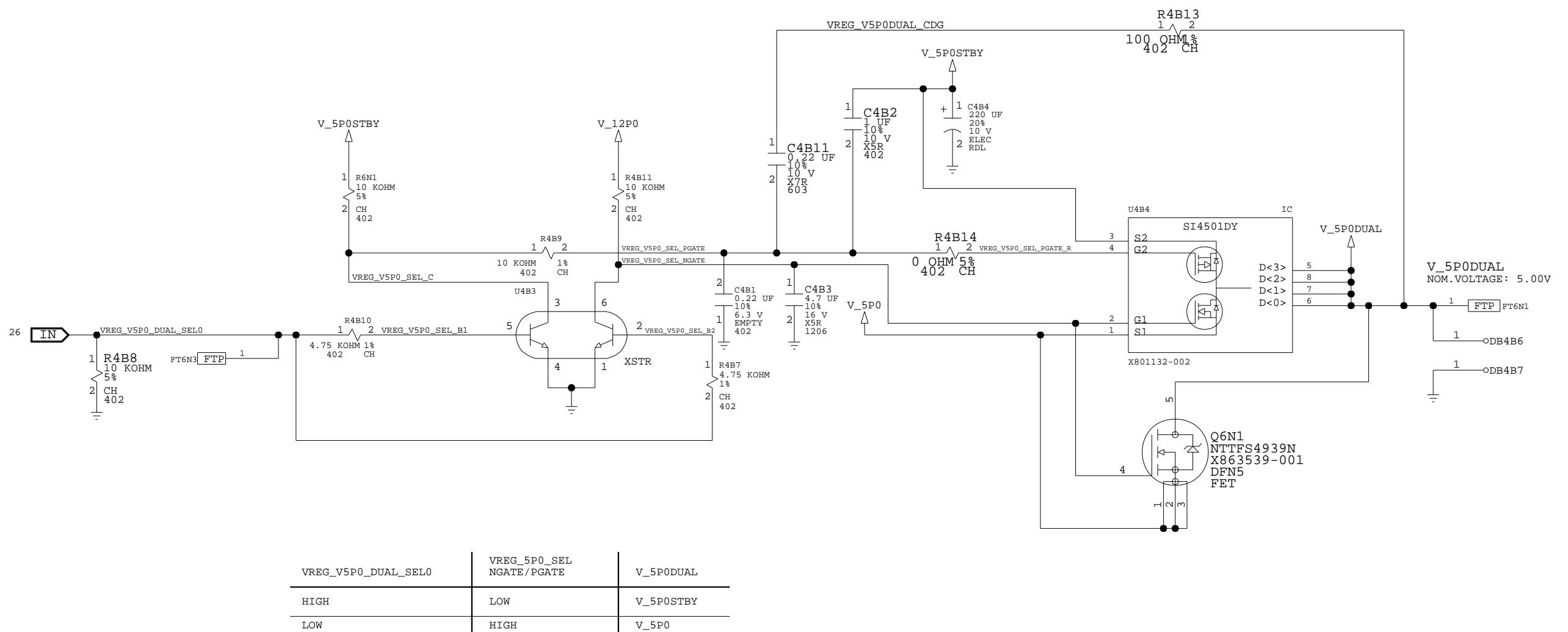


MS_PART#	MATL	REF_DESCR	TRIP	DESCR.	BOM PROPERTY
Q3E2	X875318-001	FET	TRA-N-CNL,SM,WDFN8,6.3	MCHM,30 V,24 A	FET 5P0_IRF
Q3E2	X875314-001	FET	TRA-N-CNL,SM,WDFN8,5.4	MCHM,30 V,27 A	FET 5P0_TOS
Q3E2	X876423-001	FET	TRA-N-CNL,SM,WDFN8,4.5	MCHM,30 V,17 A	FET 5P0_STM
Q3E2	X875315-001	FET	TRA-N-CNL,SM,WDFN8,5	MCHM,30 V,30 A	FET 5P0_AOS
Q3E1	X875318-001	FET	TRA-N-CNL,SM,WDFN8,6.3	MCHM,30 V,24 A	FET 5P0_IRF
Q3E1	X875314-001	FET	TRA-N-CNL,SM,WDFN8,5.4	MCHM,30 V,27 A	FET 5P0_TOS
Q3E1	X876423-001	FET	TRA-N-CNL,SM,WDFN8,4.5	MCHM,30 V,17 A	FET 5P0_STM
Q3E1	X875315-001	FET	TRA-N-CNL,SM,WDFN8,5	MCHM,30 V,30 A	FET 5P0_AOS

[PAGE_TITLE=VREGS , V5P0]

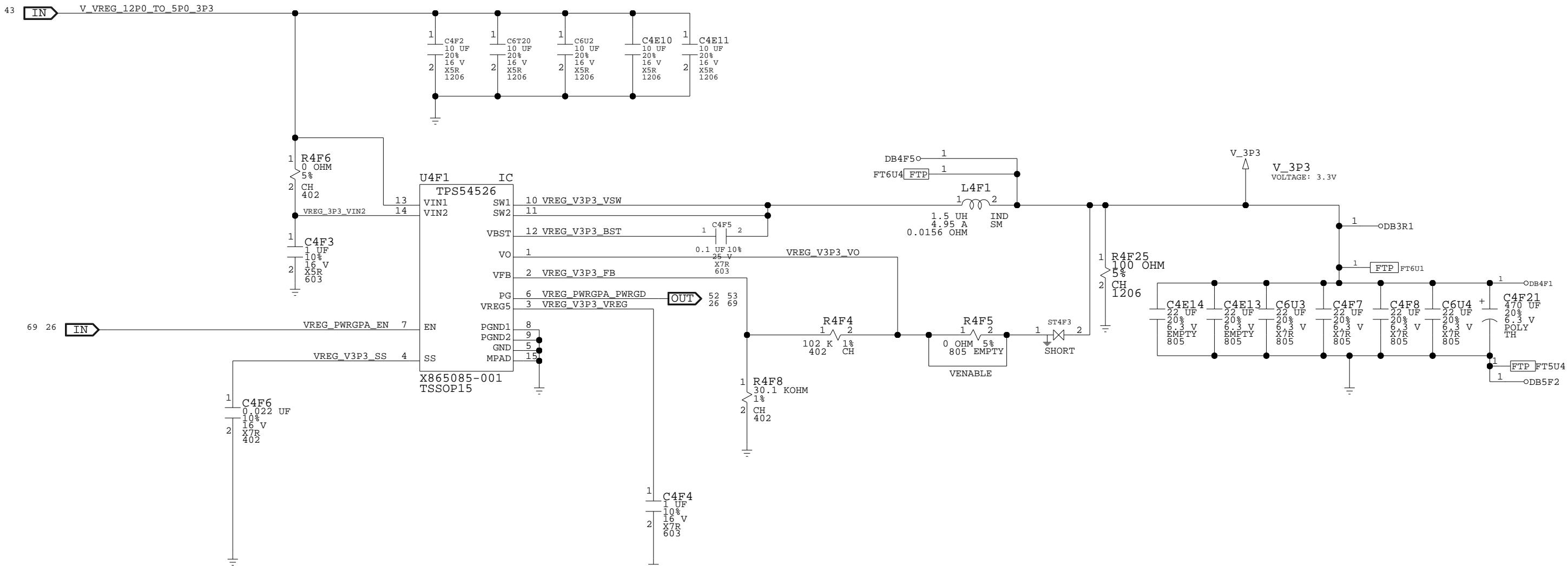
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	GREYBULL_RETAIL	54/72	54/72	M	1.0

VREGS , V5P0 DUAL

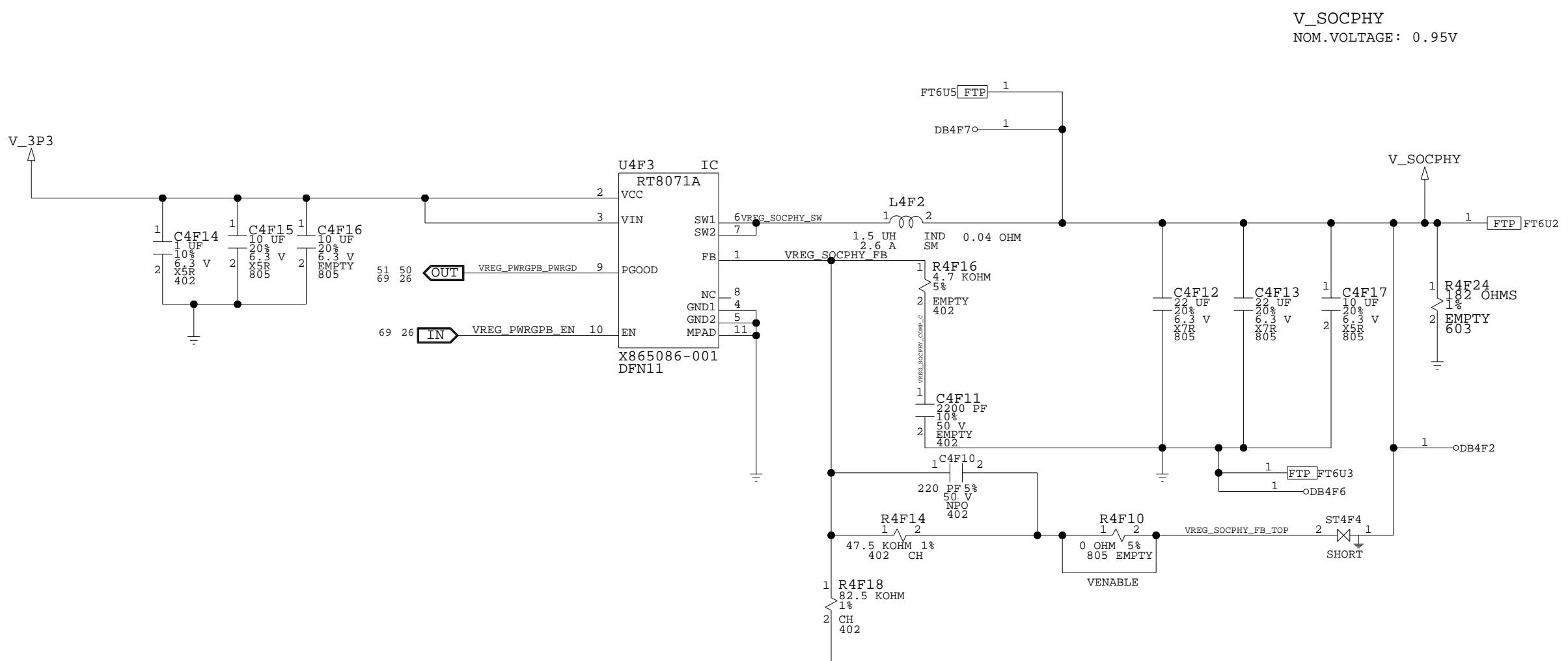


VREG_V5P0_DUAL_SEL0	VREG_5P0_SEL NGATE/PGATE	V_5P0DUAL
HIGH	LOW	V_5P0STBY
LOW	HIGH	V_5P0

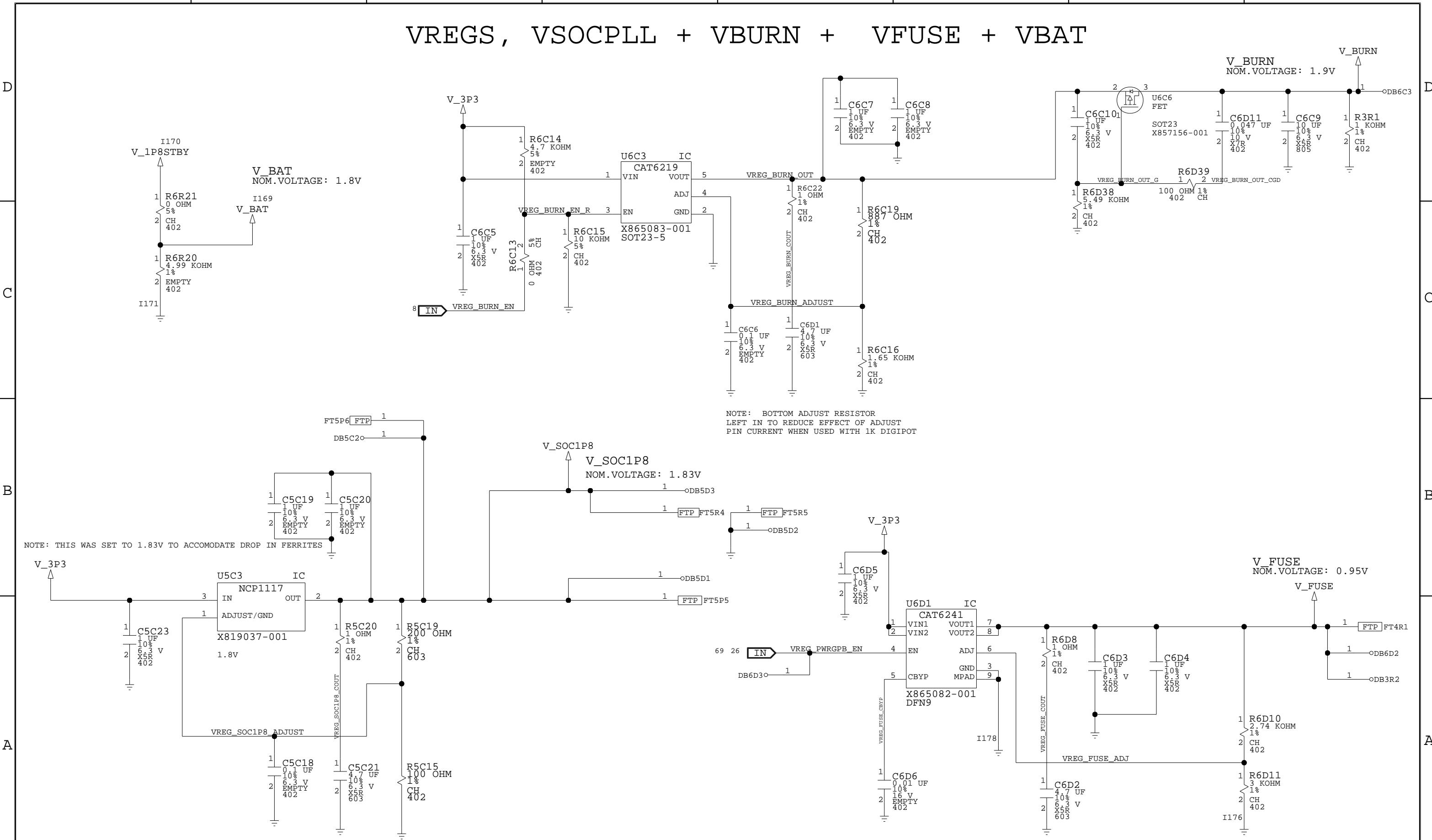
VREGS, V3P3



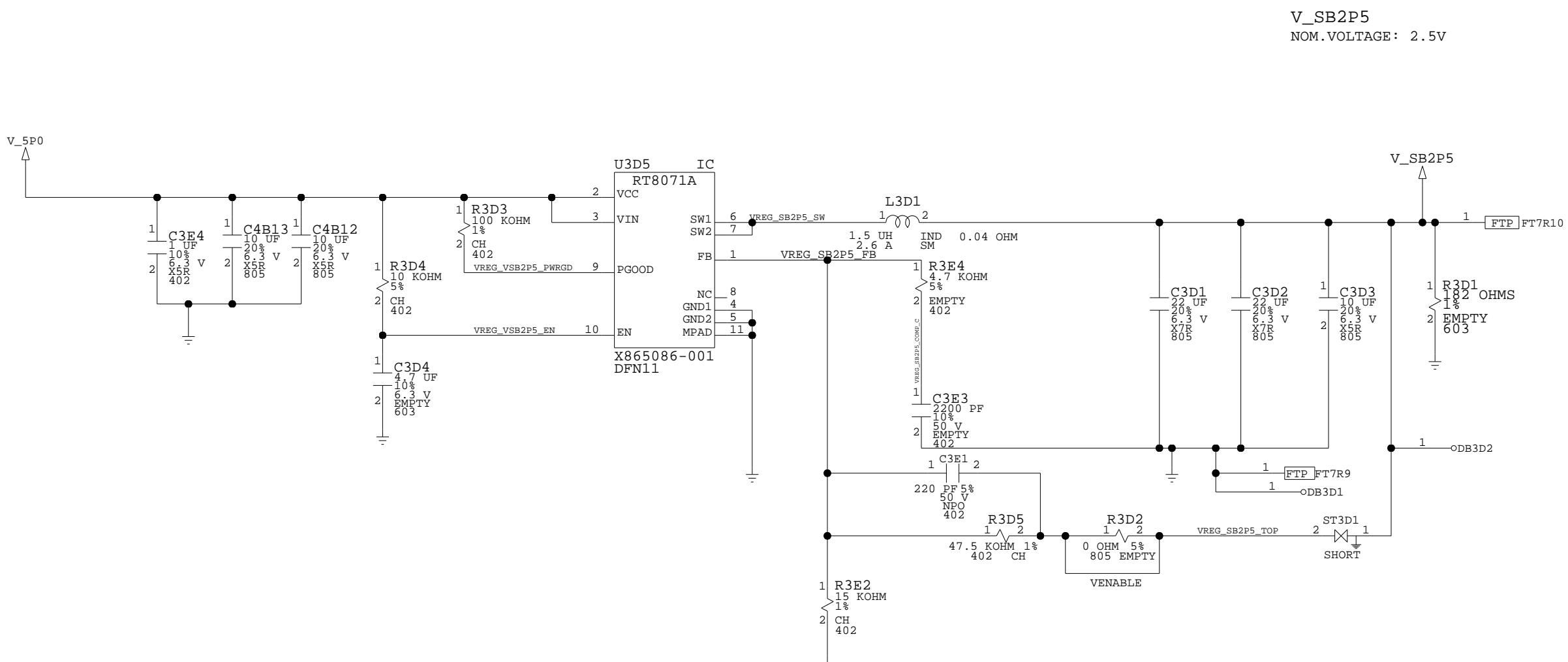
VREGS, VSOCPHY



VREGS, VSOCPLL + VBURN + VFUSE + VBAT



VREGS, VSB2P5



VREGS , VSB1P8PLL + VSB1P8IO + VSBCORE + VSB1P1PLL

D

D

C

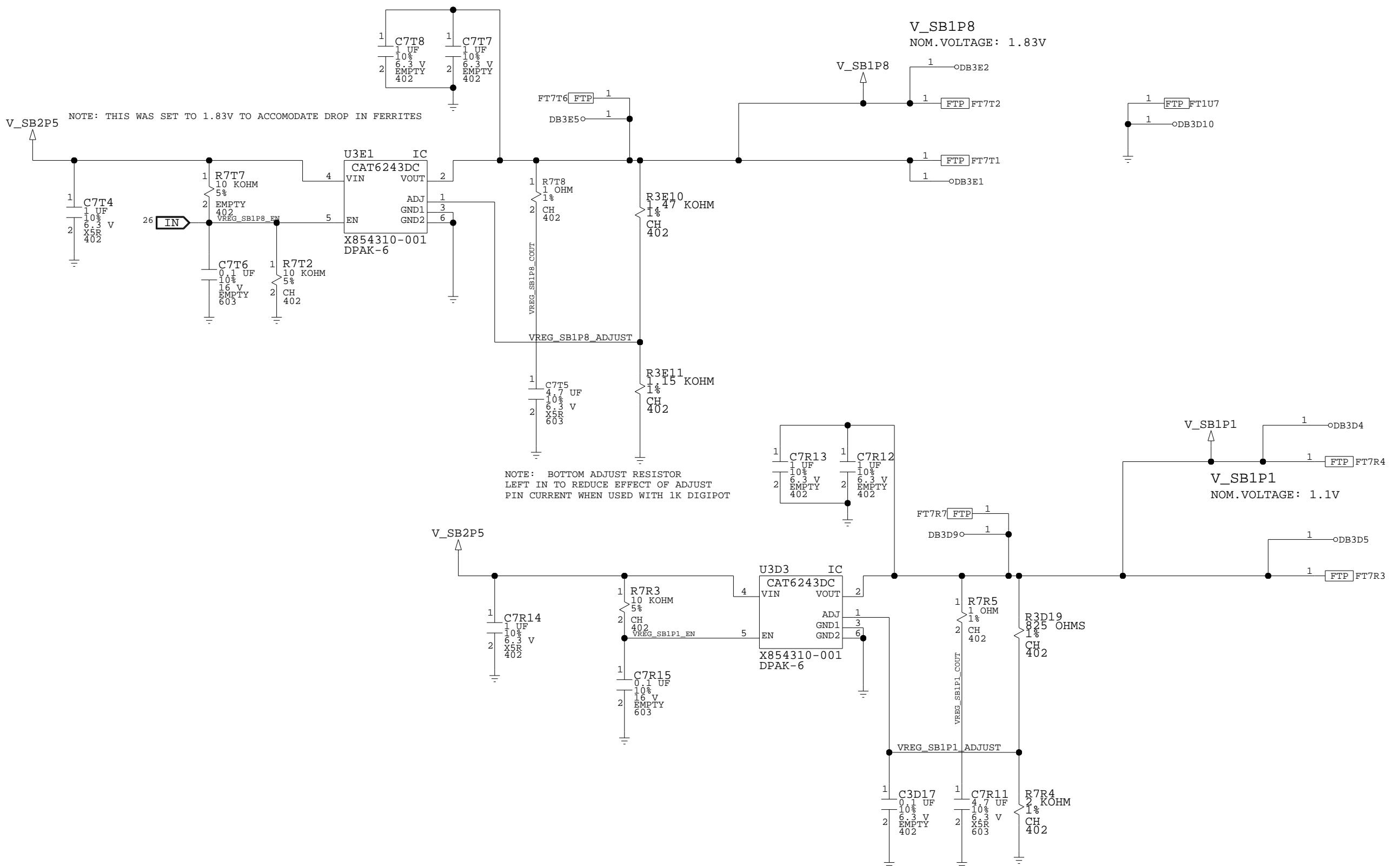
C

B

B

A

A



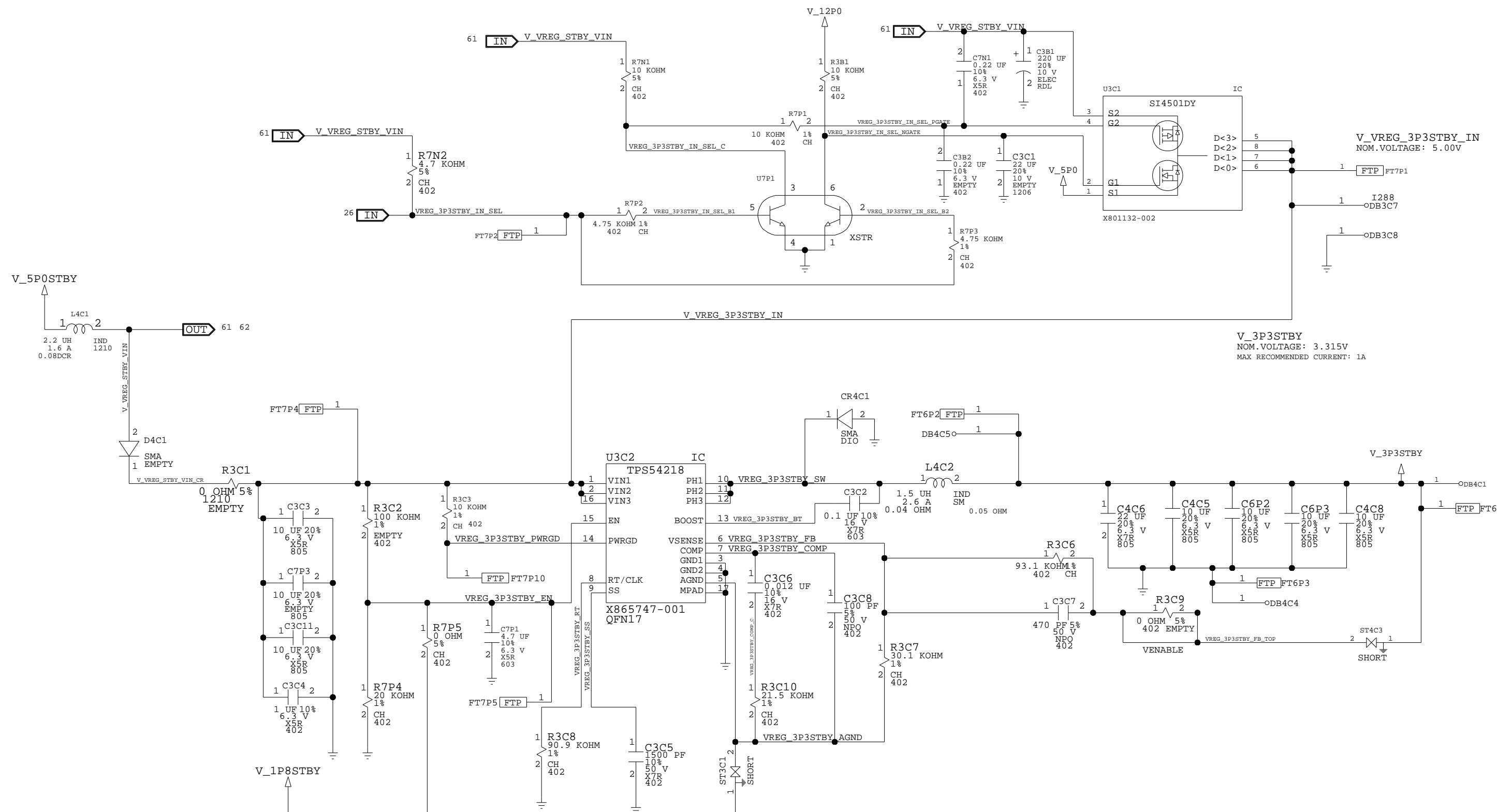
NOTE: BOTTOM ADJUST RESISTOR
LEFT IN TO REDUCE EFFECT OF ADJUST
PIN CURRENT WHEN USED WITH 1K DIGIPOT

MICROSOFT
CONFIDENTIALPROJECT NAME
GREYBULL_RETAIL

PAGE	60/72	CSA PAGE	60/72	FAB	M	REV	1.0
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VREGS, STANDBY SWITCHERS 3P3

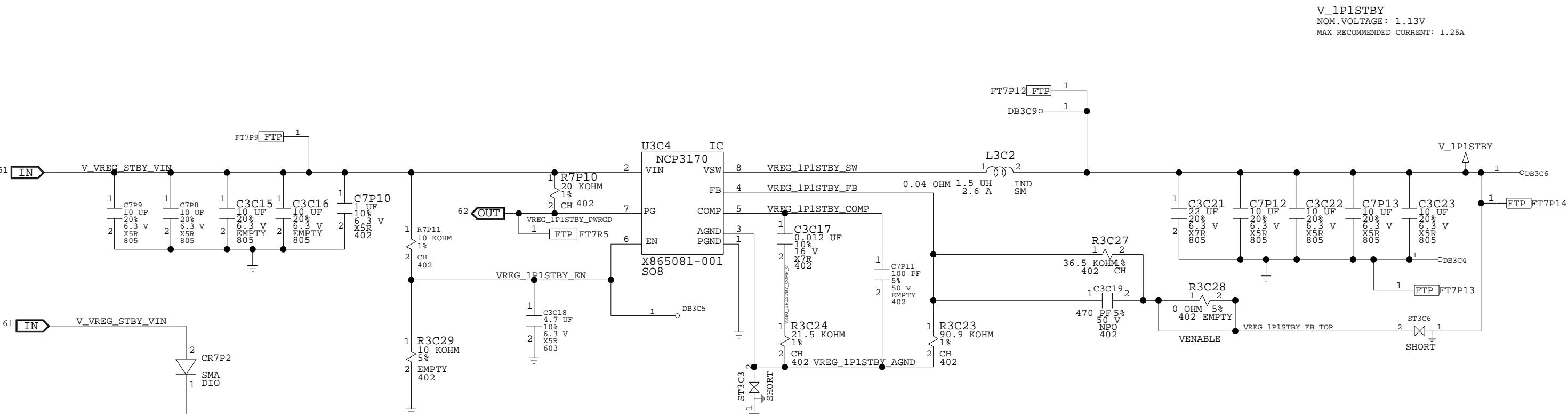
VREG_3P3STBY_IN_SEL	VREG_3P3STBY_IN_SEL_NGATE/PGATE	VREG_3P3STBY_VCC
HIGH	LOW	V_5P0STBY
LOW	HIGH	V_5P0



VREGS, STANDBY SWITCHERS 1P1 + 1P8

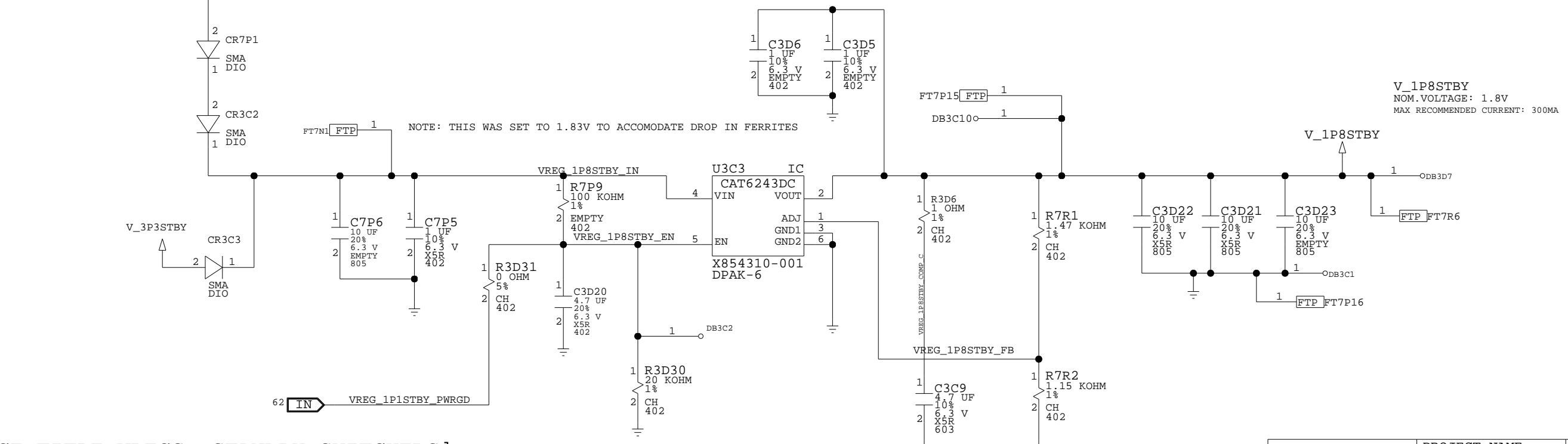
D

D



C

C



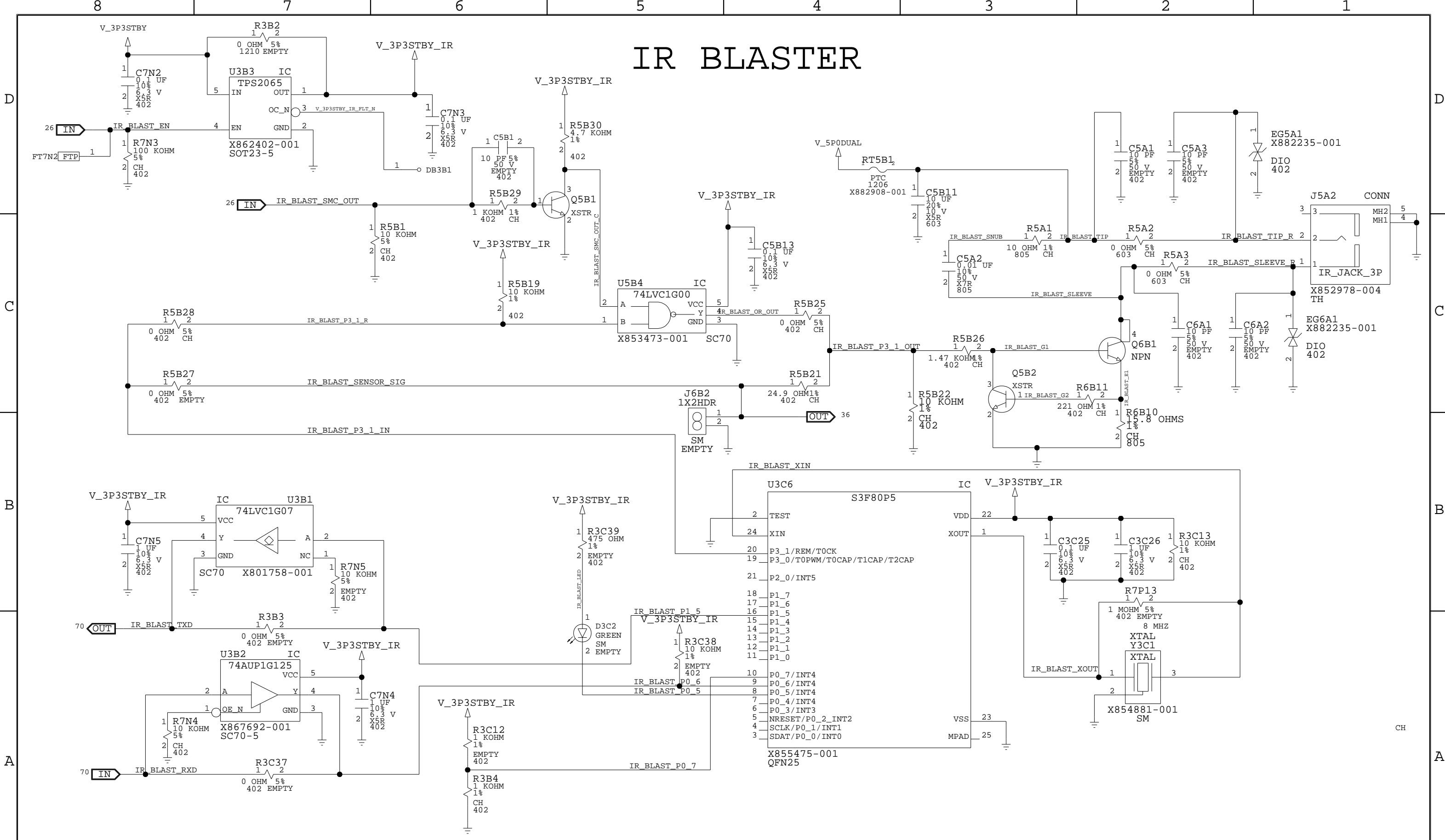
B

B

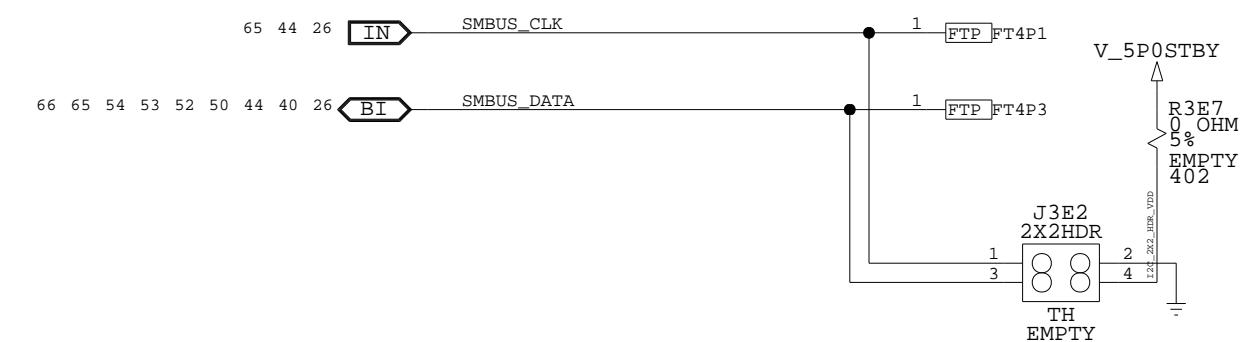
[PAGE_TITLE=VREGS, STANDBY SWITCHERS]

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 62/72	CSA PAGE 62/72	FAB M	REV 1.0
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IR BLASTER



I2C



FACET, FTDI

D

D

C

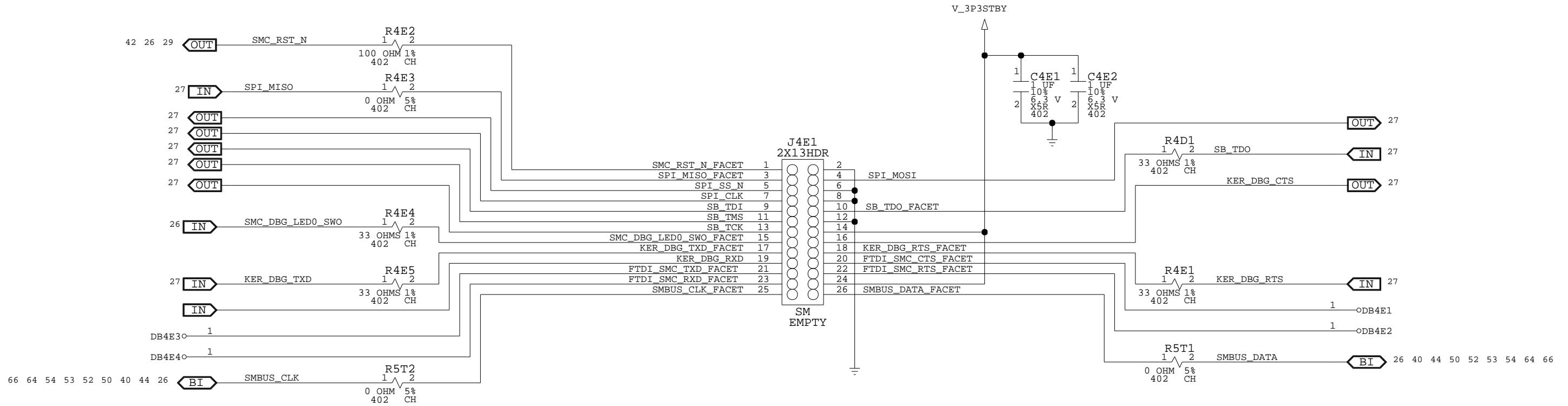
C

B

B

A

A



FACET, FTDI+MISC

D

D

C

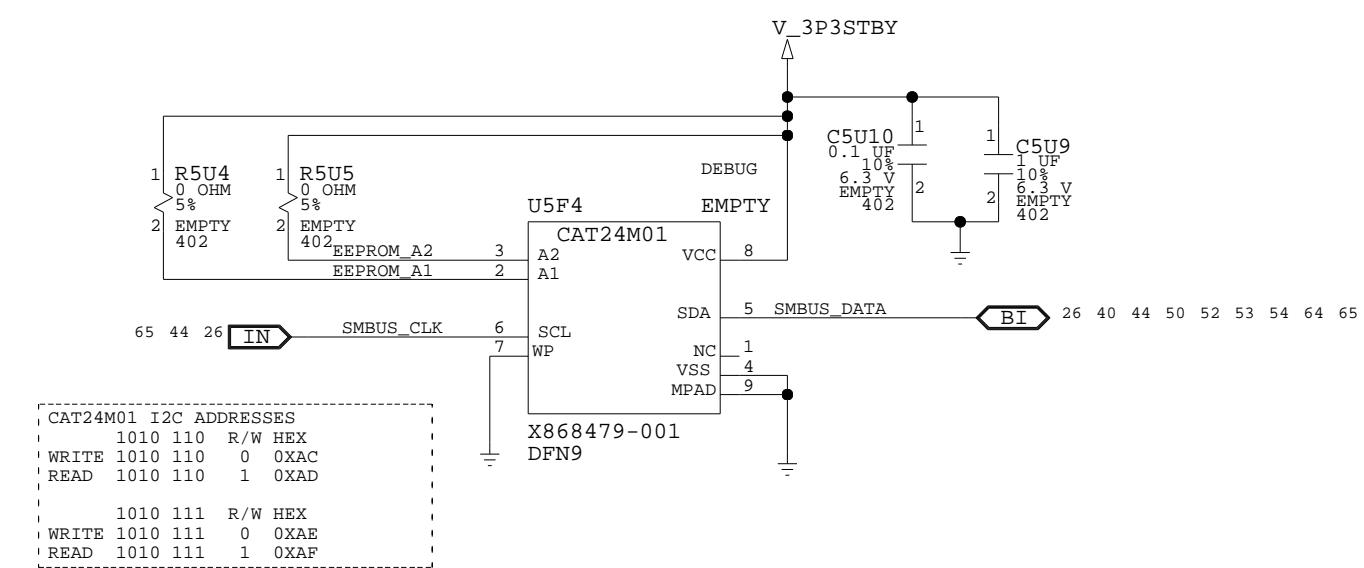
C

B

B

A

A



MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 66/72	CSA PAGE 66/72	FAB	REV
				M	1.0

CONN , SWITCHES

D

D

C

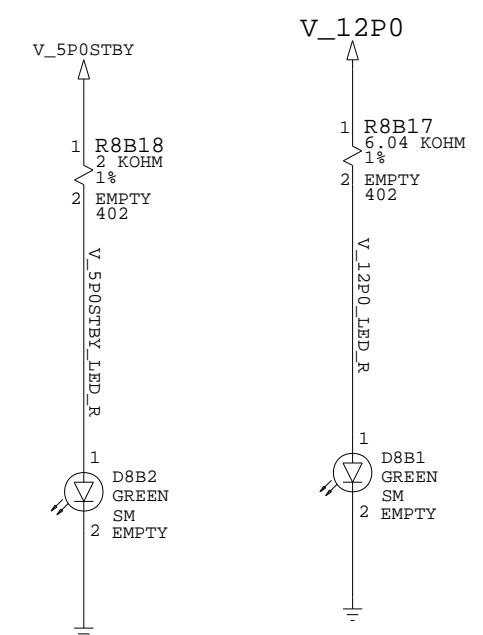
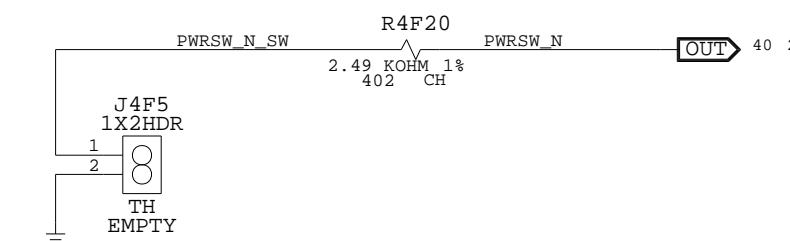
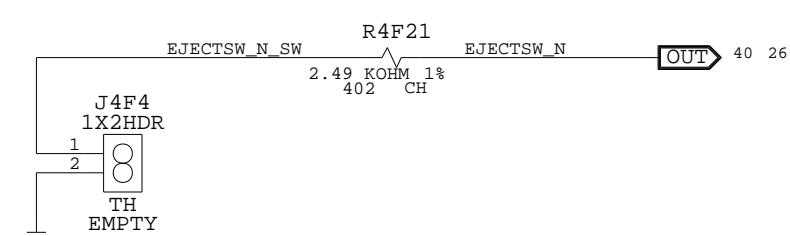
C

B

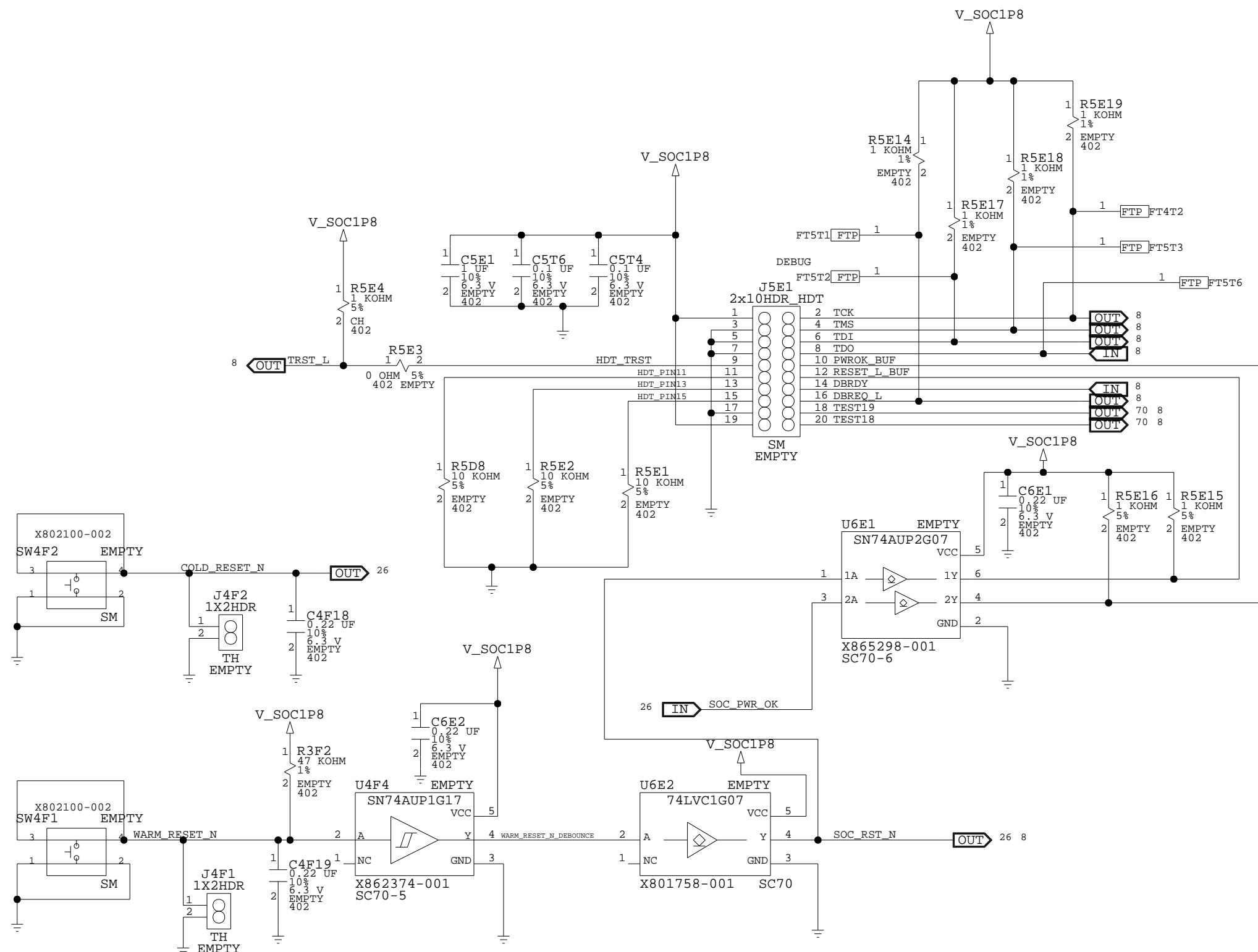
B

A

A



CONN , HDT



DEBUG, VR HEADERS AND TEST POINTS

D

D

C

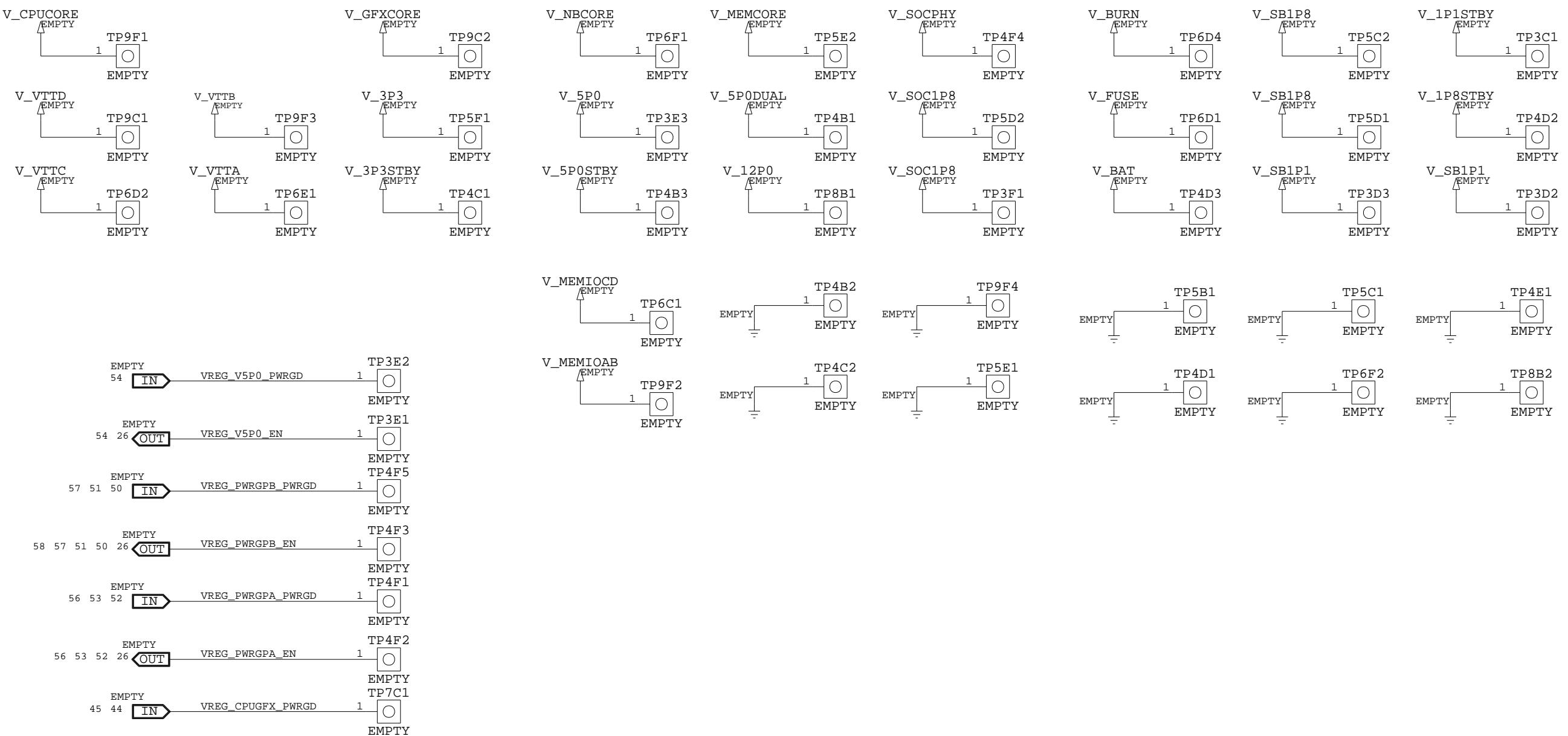
C

B

B

A

A



DEBUG , CONNECTORS

D

D

C

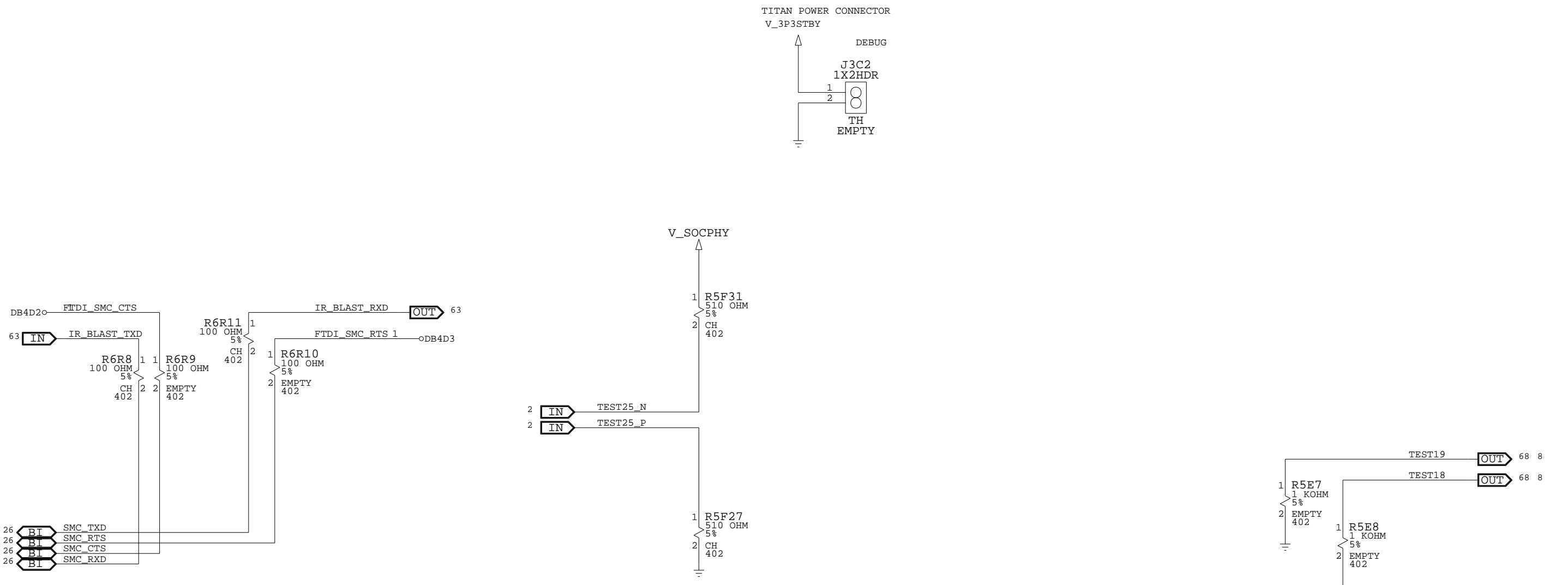
C

B

B

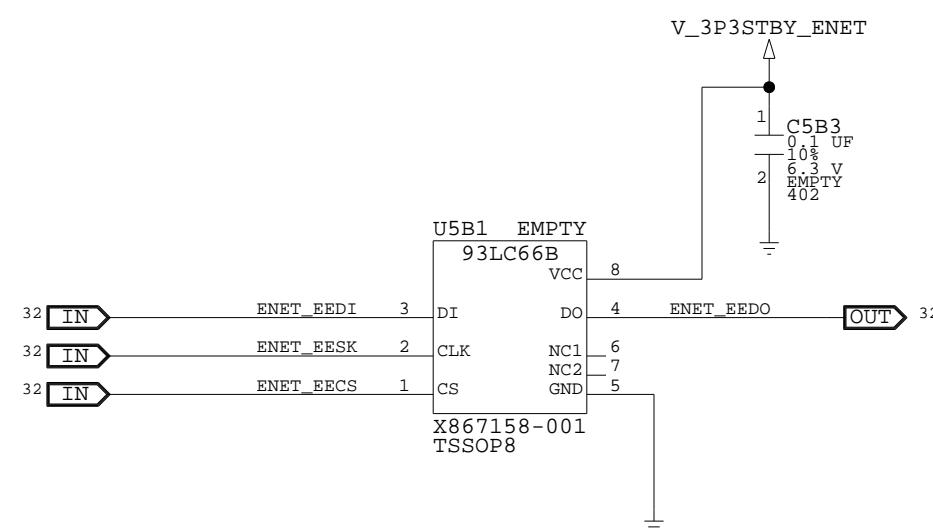
A

A



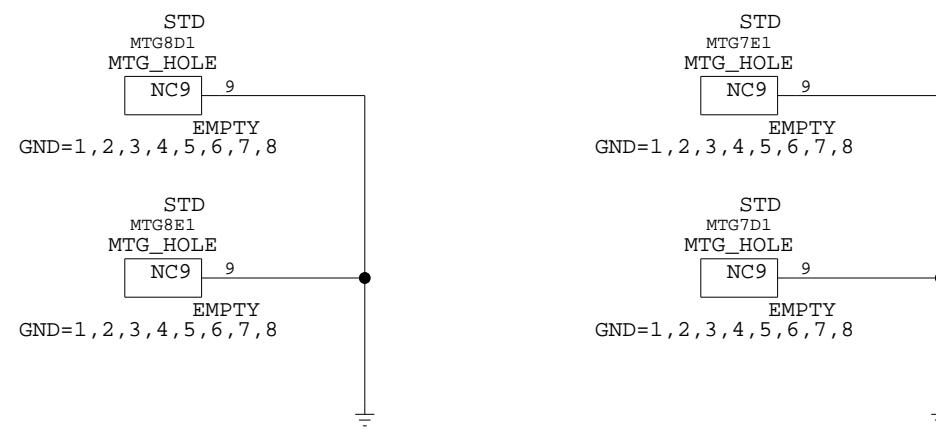
8 7 6 5 4 3 2 1

DEBUG , ENET EEPROM + MISC



LABELS AND MOUNTING

HEAT SINK MOUNTING HOLES



INTELLIGENT SERIAL NUMBER TARGET

