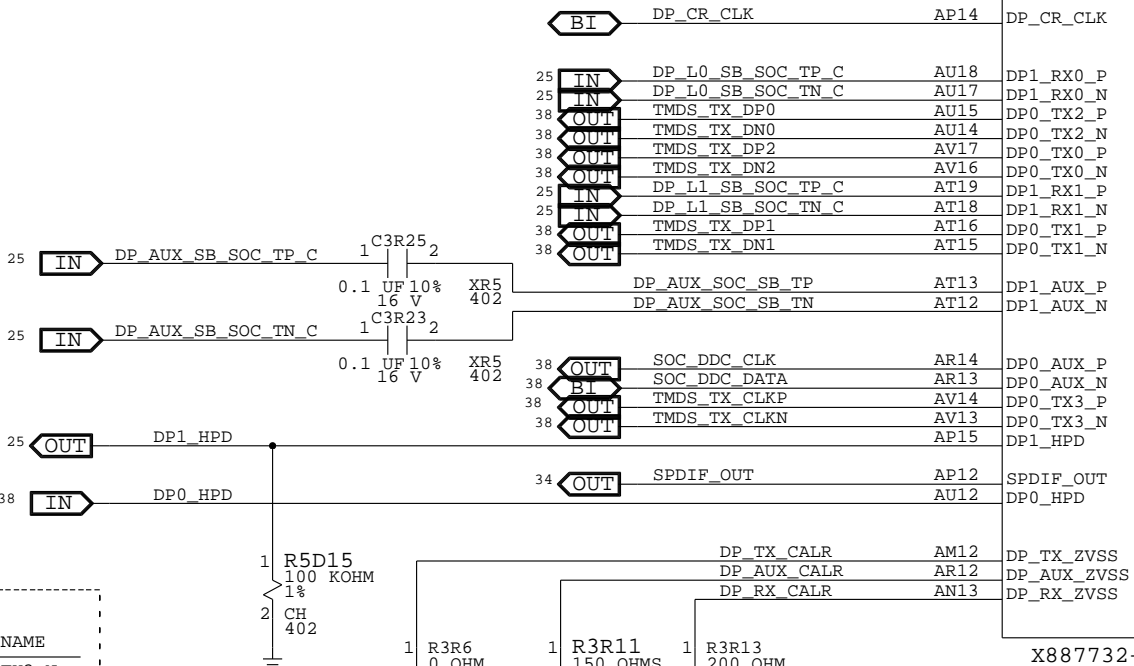
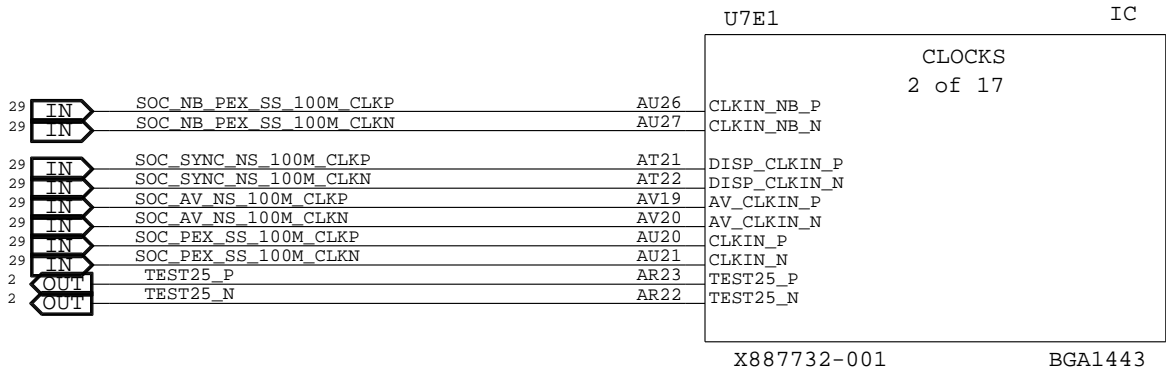
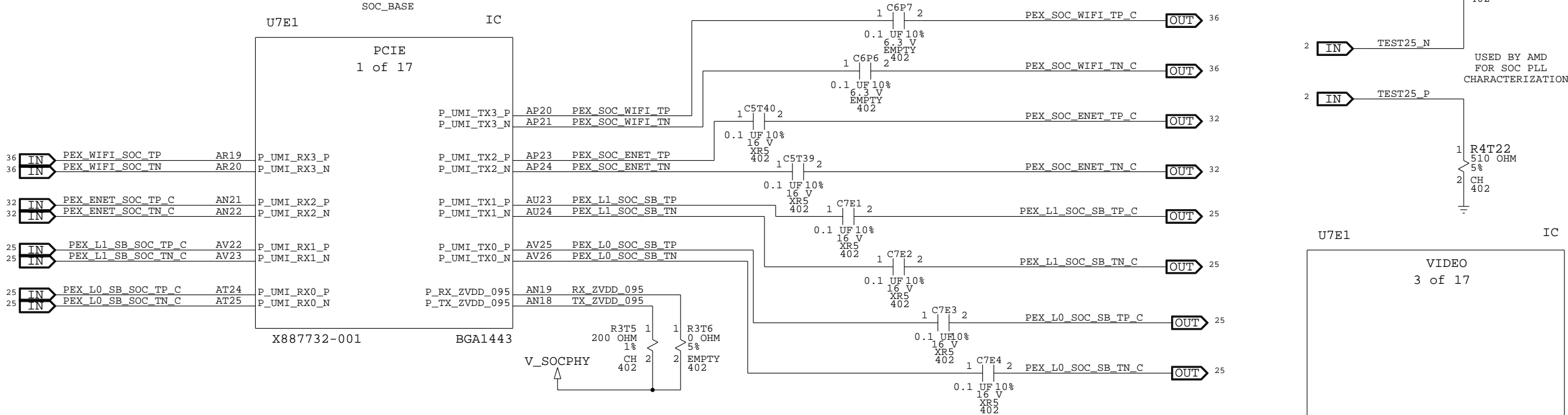


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| 8 | | 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | | |
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| | [33] | EMMC | | | | | | | | | | | | | | | |
| | [34] | CONN: RJ45,TOSLINK | | | | | | | | | | | | | | | |
| | [35] | CONN: USB (FRONT & REAR) | | | | | | | | | | | | | | | |
| | [36] | CONN: WIFI | | | | | | | | | | | | | | | |
| | [37] | CONN: HDMI IN | | | | | | | | | | | | | | | |
| | [38] | CONN: HDMI OUT | | | | | | | | | | | | | | | |
| | [39] | CONN: HDMI SUPPORT | | | | | | | | | | | | | | | |
| [40] | CONN: ODD & HDD | | | | | | | | | | | | | RULES: (APPLIED WHEN POSSIBLE) 1. MSB TO LSB IS TOP TO BOTTOM 2. WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT 3. ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING 4. AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS 5. LANED SIGNALS ARE GROUPED ON SYMBOLS 6. TRANSMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS 7. SUFFIX V IS USED FOR VOLTAGE RAIL SIGNAL NAMES 8. SUFFIX DP AND DN ARE USED FOR DIFFERENTIAL PAIRS 9. UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE 10.SUFFIX N FOR ACTIVE LOW OR N JUNCTION 12.SUFFIX P FOR P JUNCTION 13.SUFFIX EN FOR ENABLE 14.'CLK' FOR CLOCKS, 'RST' FOR RESETS 15.PWRGD FOR POWER GOOD 16.REV AND FAB ARE SET USING CUSTOM VARIABLES TOOLS>OPTIONS>VARIABLES | | | |
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| [42] | CONN: POWER | | | | | | | | | | | | | | | | |
| [43] | VREGS: INPUT & OUTPUT FILTERS | | | | | | | | | | | | | | | | |
| [44] | VREGS: CPUCORE | | | | | | | | | | | | | | | | |
| [45] | VREGS: GFXCORE | | | | | | | | | | | | | | | | |
| [46] | VREGS: GFXCORE OUTPUT PHASE 1 & 2 | | | | | | | | | | | | | | | | |
| [47] | VREGS: CPUCORE OUTPUT PHASE | | | | | | | | | | | | | | | | |
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SOC:PCIE, CLOCKS, VIDEO

- NOTES:
- 1.TO SUPPORT A PCIE WIFI INTERFACE (J3C1), POPULATE C6P6 AND C6P7
 - 2.SEE PAGE 32 FOR 100MHZ CLOCK ROUTING INFORMATION



| MS_PART# | MATL | REF_DES | DESCR. | BOM_PROPERTY |
|-------------|------|---------|--|---------------|
| X941293-001 | IC | U7E1 | ARLENE,TSMC,SHINKO,SPIL,AMD PENANG,TYPICAL,79W TDP+,AG,AKA ROUTE | ARLENE_SOC_R1 |
| X941294-001 | IC | U7E1 | ARLENE,TSMC,IRIDEN,SPIL,AMD PENANG,TYPICAL,79W TDP+,AG,AKA ROUTE | ARLENE_SOC_R2 |
| X941295-001 | IC | U7E1 | ARLENE,TSMC,UMTC,SPIL,AMD PENANG,TYPICAL,79W TDP+,AG,AKA ROUTE | ARLENE_SOC_R3 |
| X941296-001 | IC | U7E1 | ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,FF,79W TDP+,AG,AKA ROUTE | ARLENE_SOC_FF |
| X941297-001 | IC | U7E1 | ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,FS,79W TDP+,AG,AKA ROUTE | ARLENE_SOC_FS |
| X941298-001 | IC | U7E1 | ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,SF,79W TDP+,AG,AKA ROUTE | ARLENE_SOC_SF |
| X941299-001 | IC | U7E1 | ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,SS,79W TDP+,AG,AKA ROUTE | ARLENE_SOC_SS |

| DVI PCB ROUTING ORDERING | DP PCB ROUTING ORDERING | PIN NAME |
|--------------------------|-------------------------|-----------|
| TMDS CLOCK - | DP LANE 3 - | DP0_TX3_N |
| TMDS CLOCK + | DP LANE 3 + | DP0_TX3_P |
| TMDS DATA0 - | DP LANE 2 - | DP0_TX2_N |
| TMDS DATA0 + | DP LANE 2 + | DP0_TX2_P |
| TMDS DATA1 - | DP LANE 1 - | DP0_TX1_N |
| TMDS DATA1 + | DP LANE 1 + | DP0_TX1_P |
| TMDS DATA2 - | DP LANE 0 - | DP0_TX0_N |
| TMDS DATA2 + | DP LANE 0 + | DP0_TX0_P |

8 7 6 5 4 3 2 1

SOC: POWER: MEMIO, MEMCORE, CPUCORE, NBCORE, MISC

D C B A

The diagram illustrates the power management IC (U7E1) and its connections to various power planes and components. The IC is shown in two views: a top view (U7E1) and a bottom view (U7E1). The top view shows the IC connected to V_MEMIO, V_CPUCORE, and V_NBCORE. The bottom view shows the IC connected to V_SOCPHY, V_BAT, V_BURN, and V_SOC1P8. The IC is labeled with various pins and internal components, including capacitors (C3T3, C3T5, C3R26, C7D1, C6D9, C3R24, C3T23), resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100), and fuses (F1, F2, F3, F4, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F17, F18, F19, F20, F21, F22, F23, F24, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F35, F36, F37, F38, F39, F40, F41, F42, F43, F44, F45, F46, F47, F48, F49, F50, F51, F52, F53, F54, F55, F56, F57, F58, F59, F60, F61, F62, F63, F64, F65, F66, F67, F68, F69, F70, F71, F72, F73, F74, F75, F76, F77, F78, F79, F80, F81, F82, F83, F84, F85, F86, F87, F88, F89, F90, F91, F92, F93, F94, F95, F96, F97, F98, F99, F100). The diagram is divided into sections A, B, C, and D.

U7E1 IC

VDD CORE 10 of 17

VDD MEM 9 of 17

VDD NB 14 of 17

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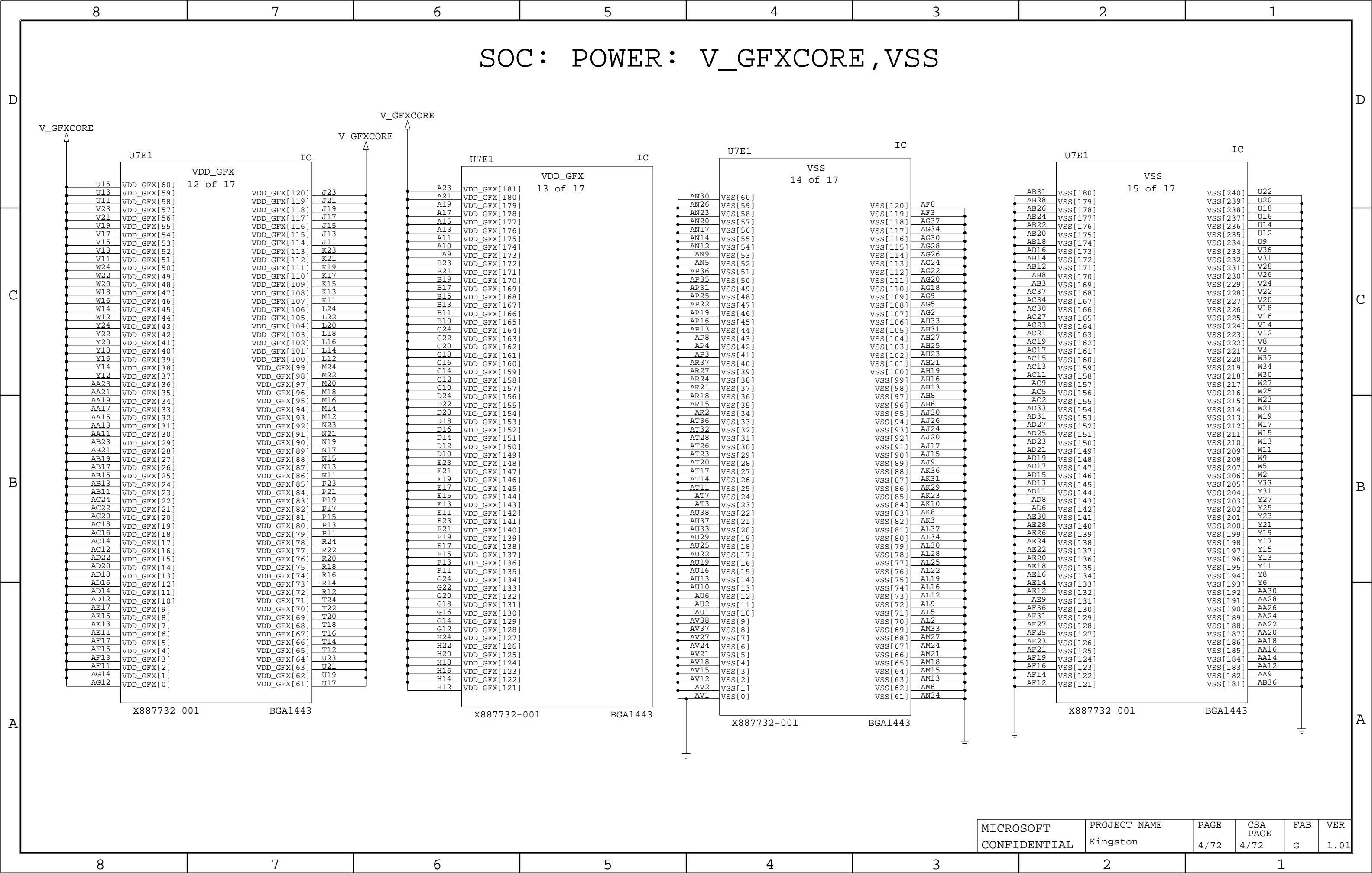
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VSS

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IC

AB31

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Y11

VSS[194]

Y8

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Y6

VSS[192]

AA30

VSS[191]

AA28

VSS[190]

AA26

VSS[189]

AA24

VSS[188]

AA22

VSS[187]

AA20

VSS[186]

AA18

VSS[185]

AA16

VSS[184]

AA14

VSS[183]

AA12

VSS[182]

AA9

VSS[181]

AB36

V_GFXCORE

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6

5

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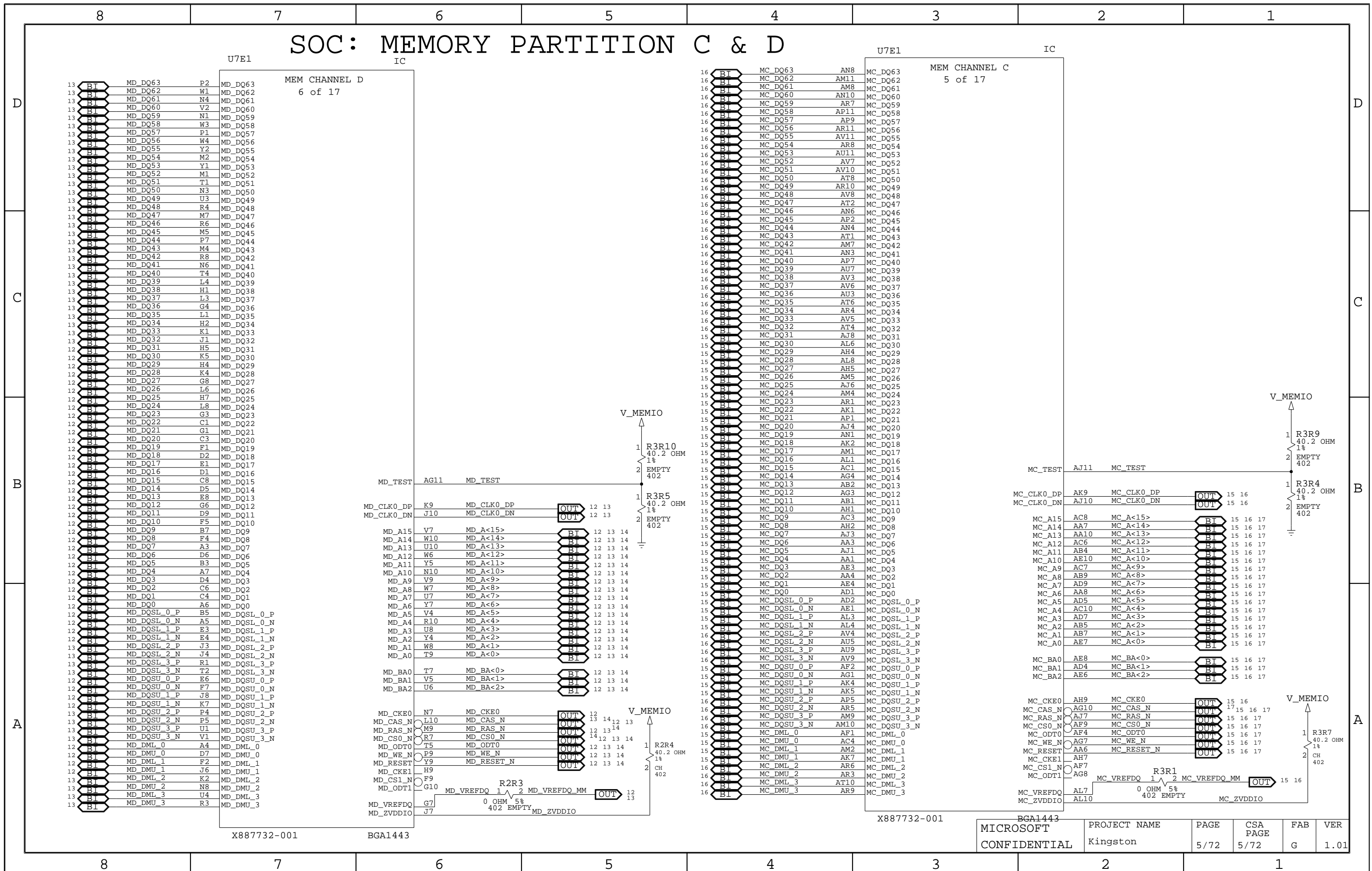
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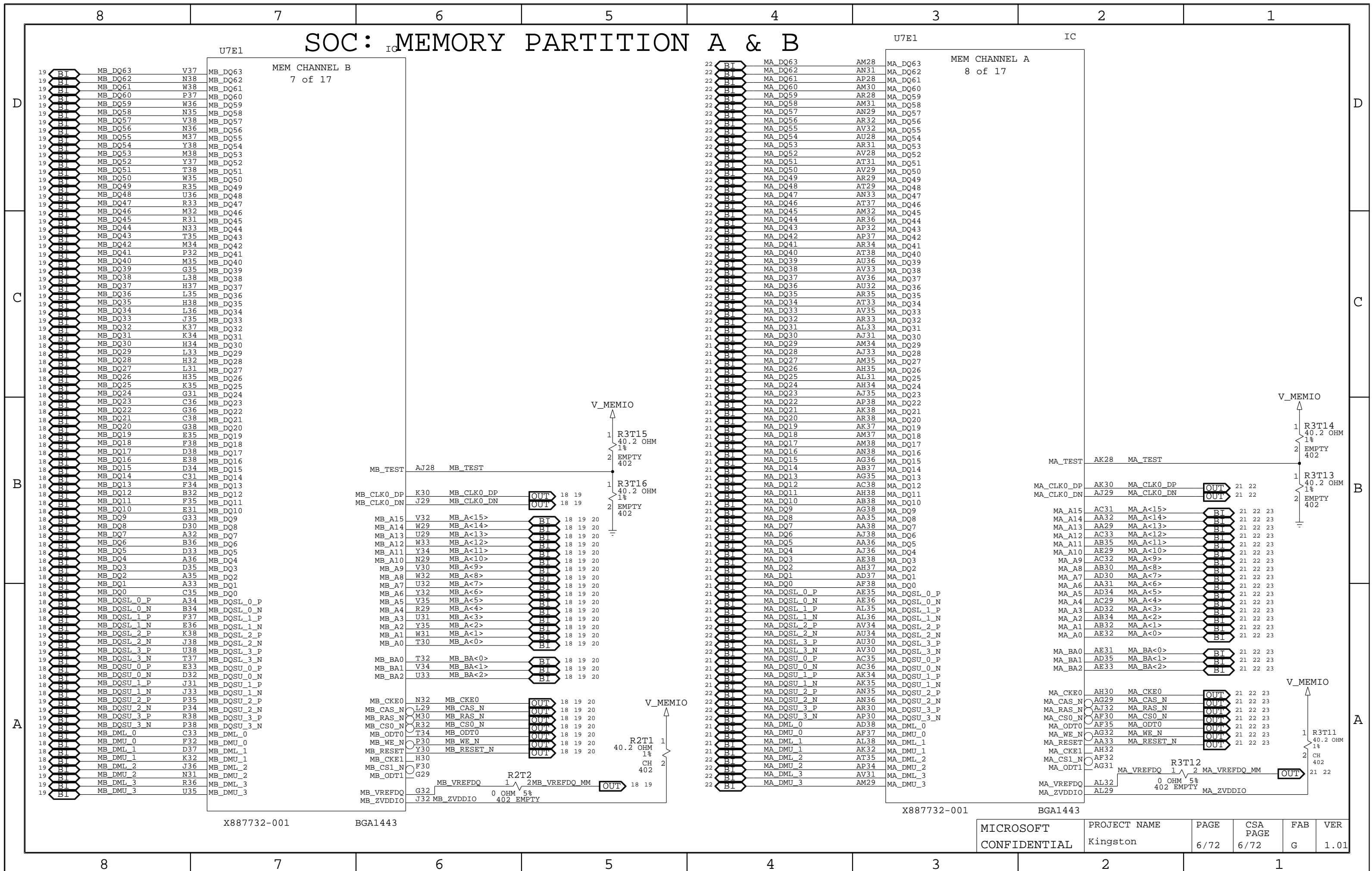
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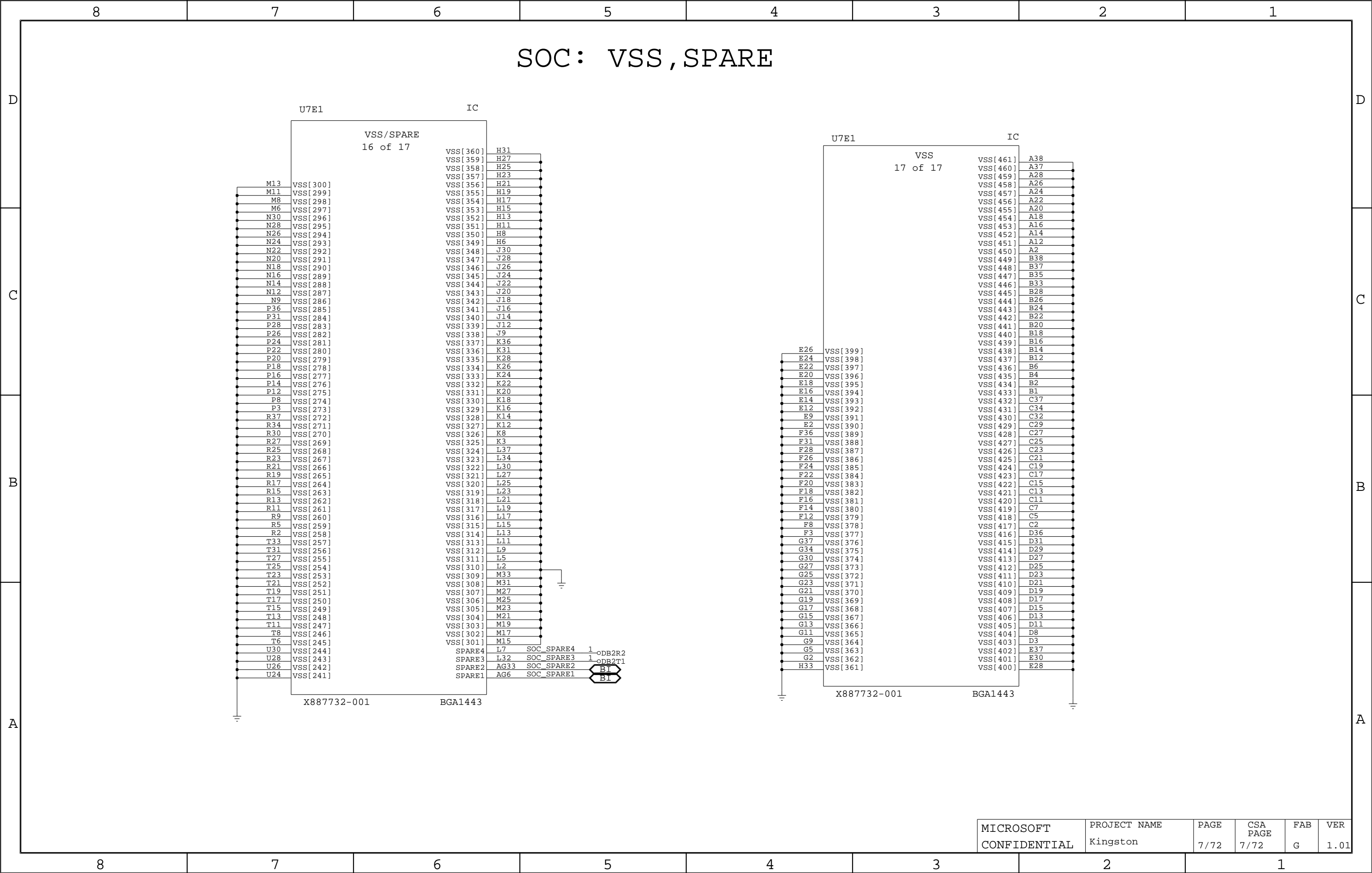
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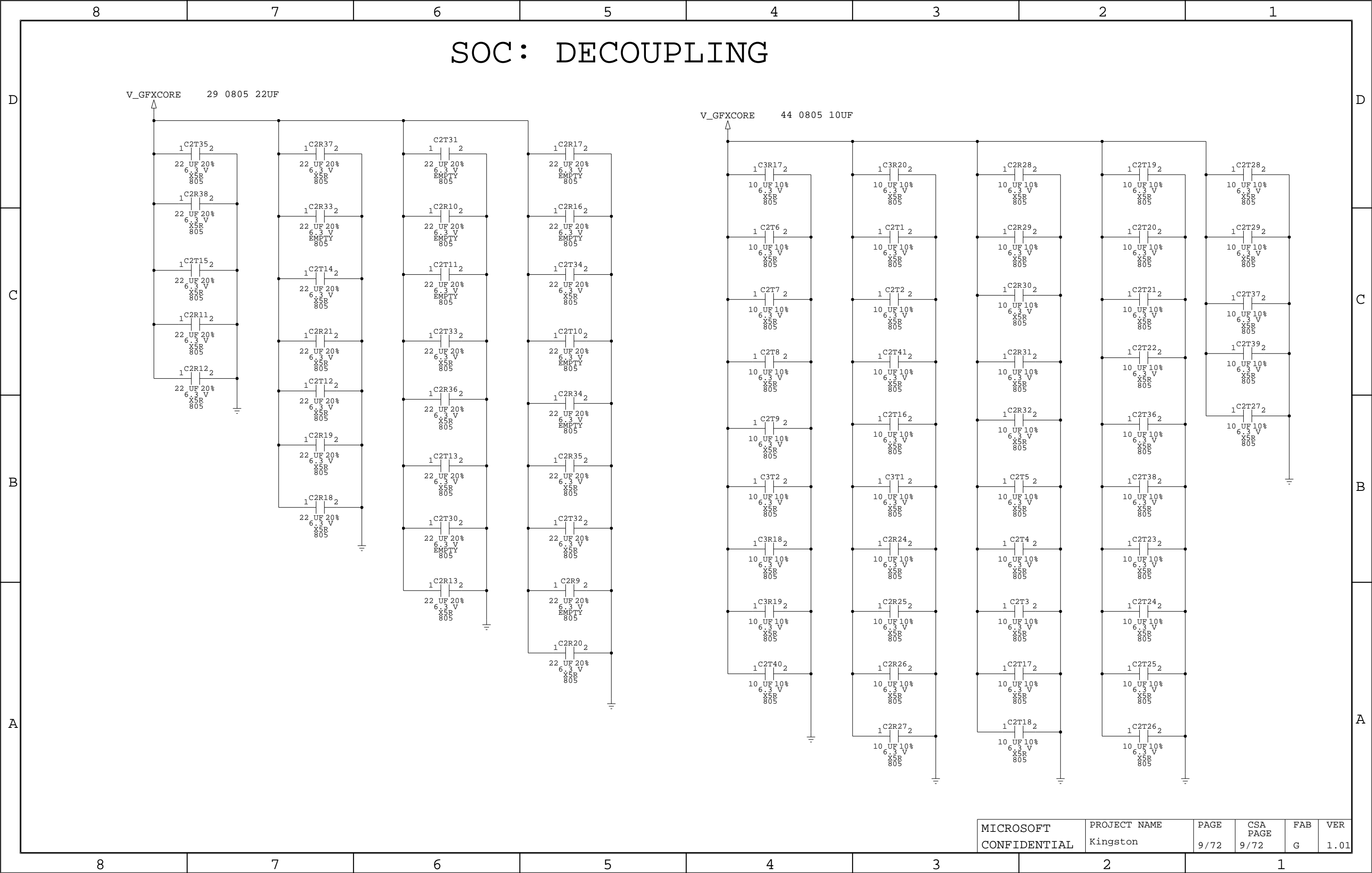
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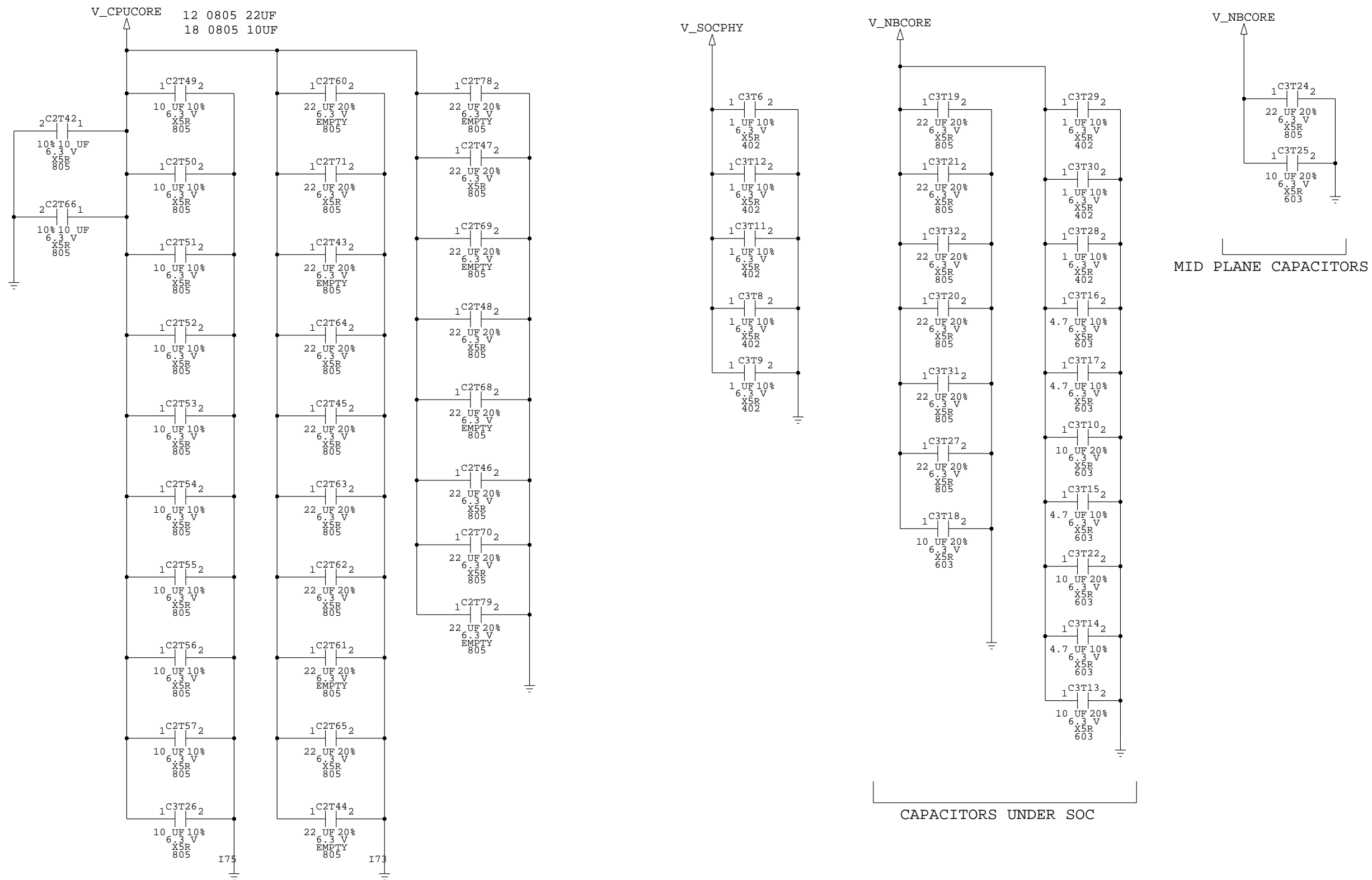




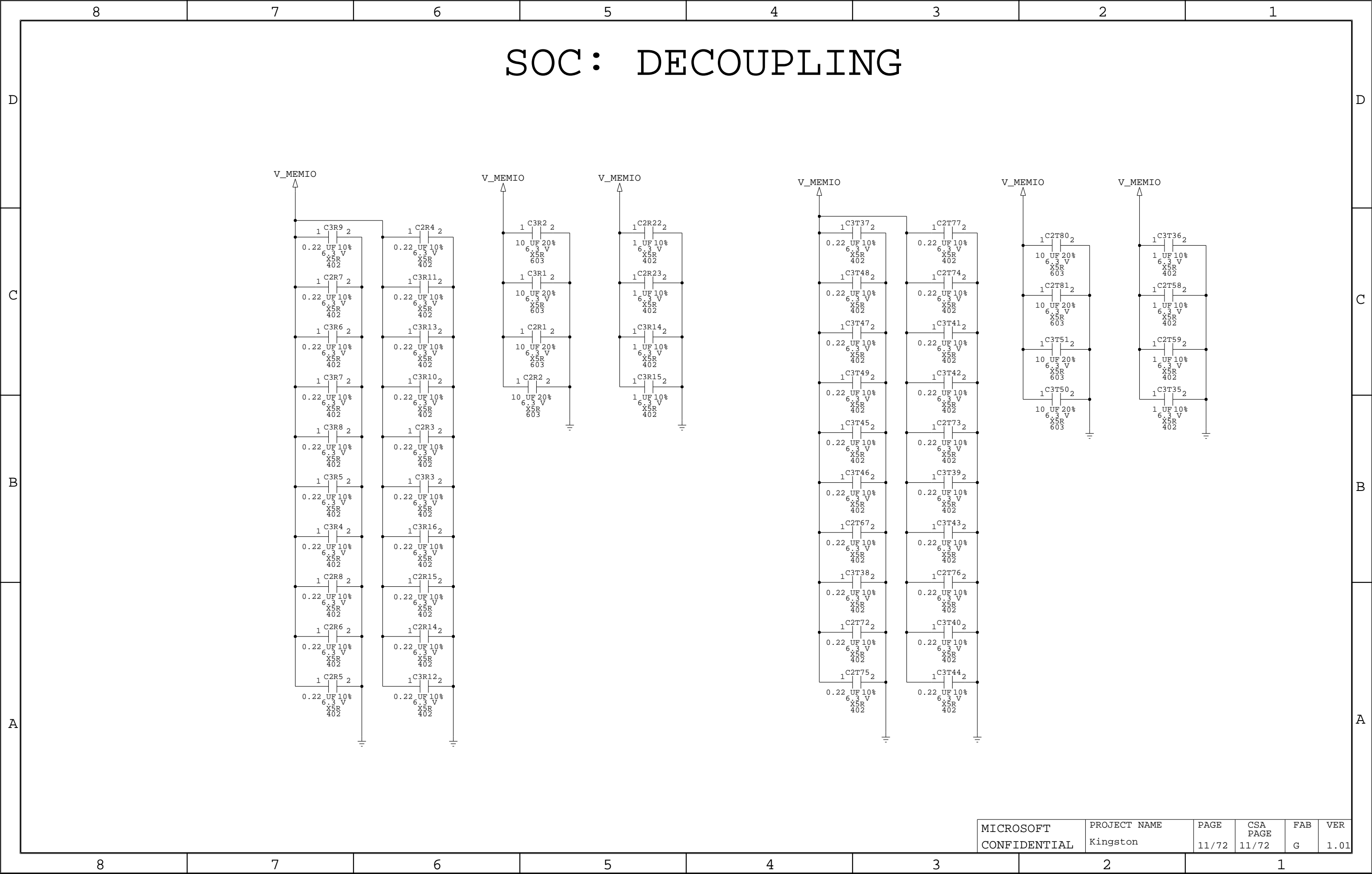




SOC: DECOUPLING



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MEMORY: CHANNEL D

D

C

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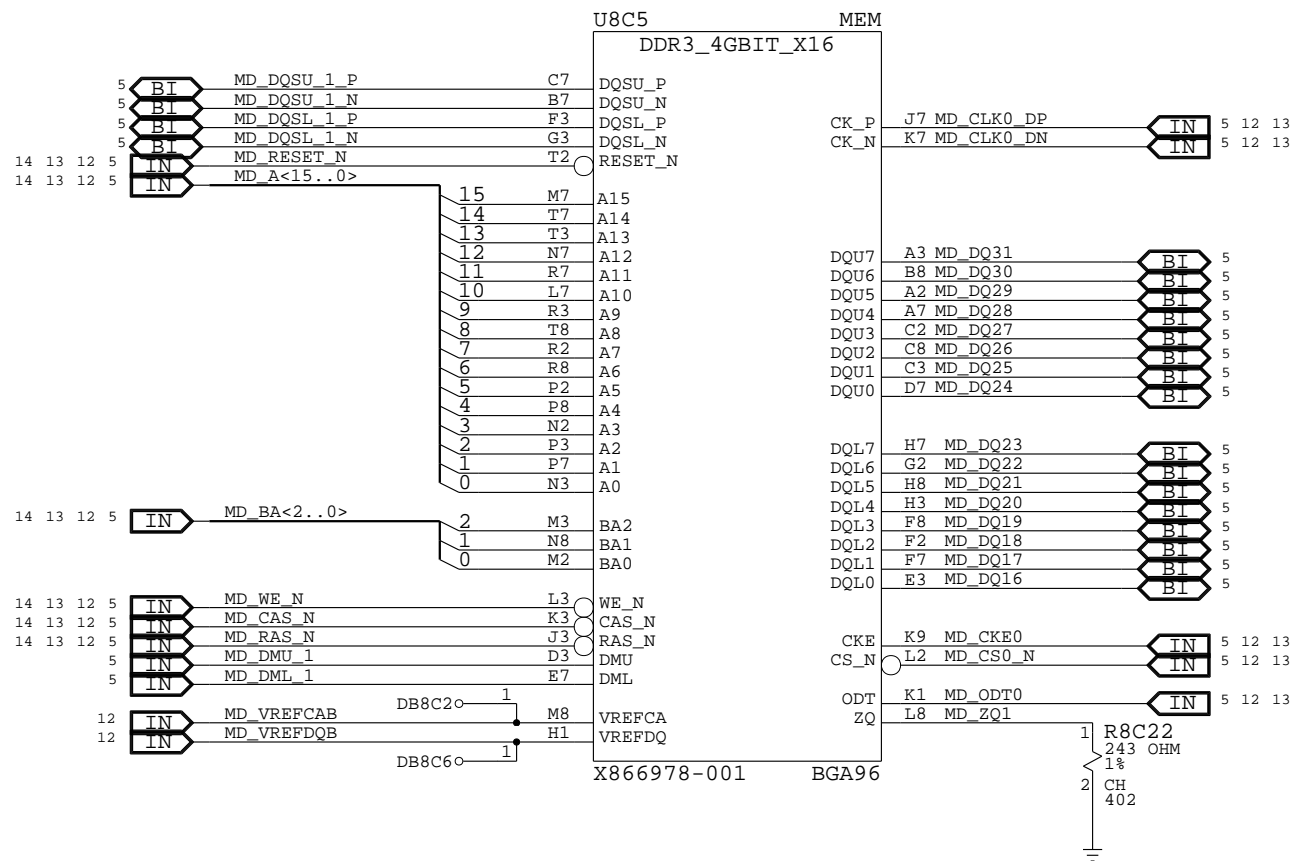
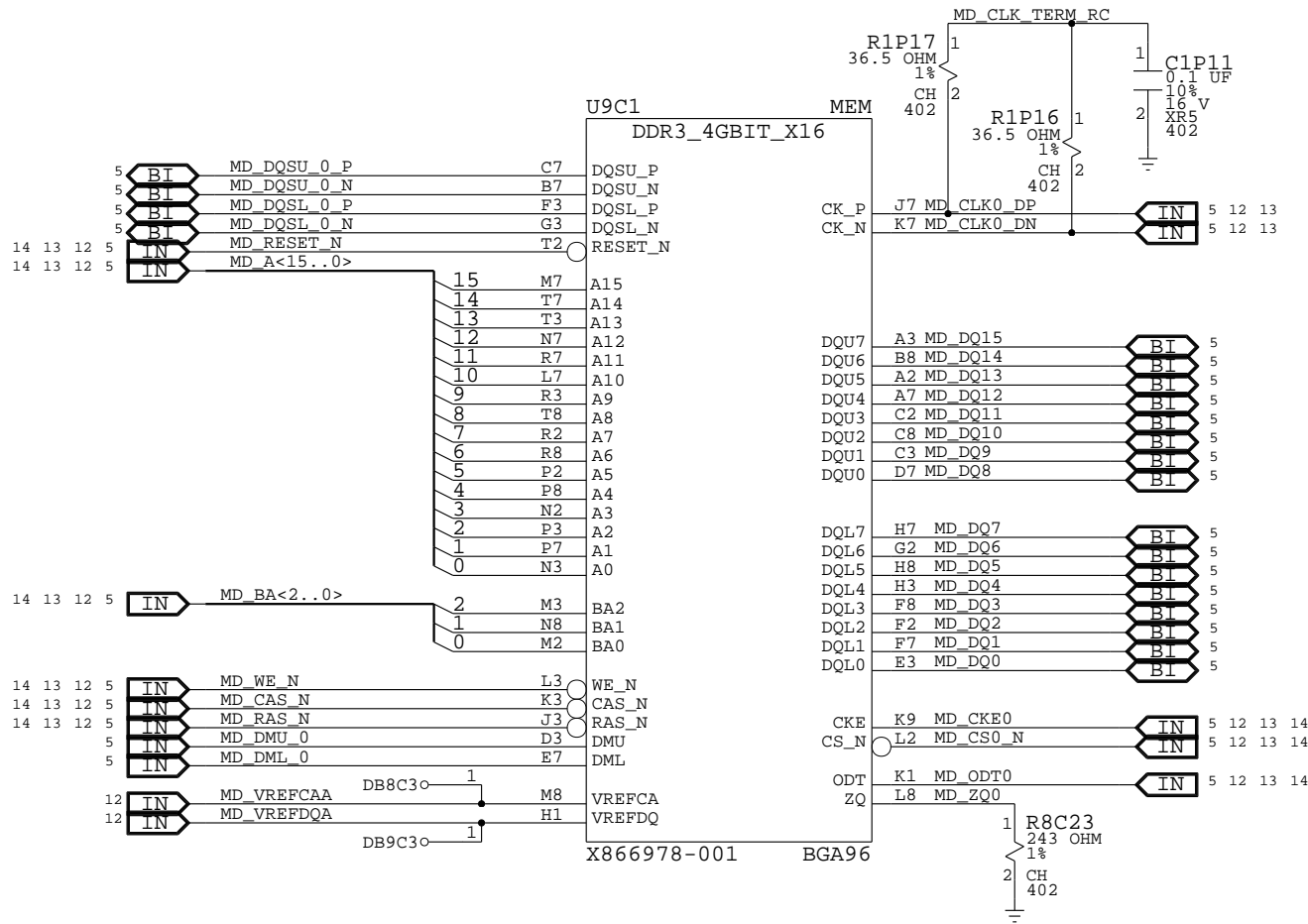
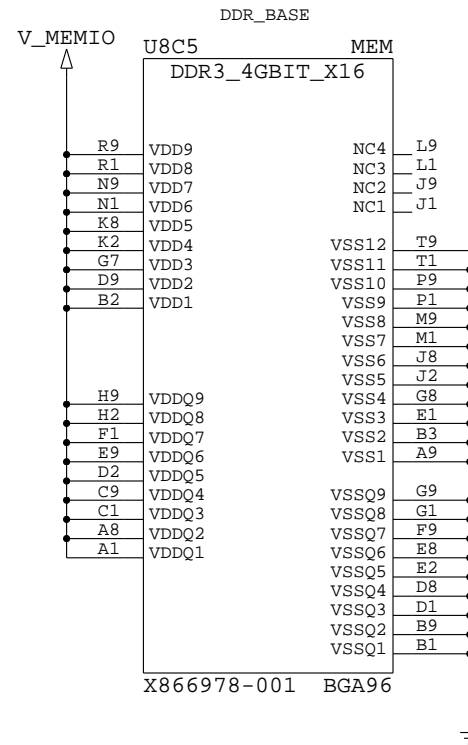
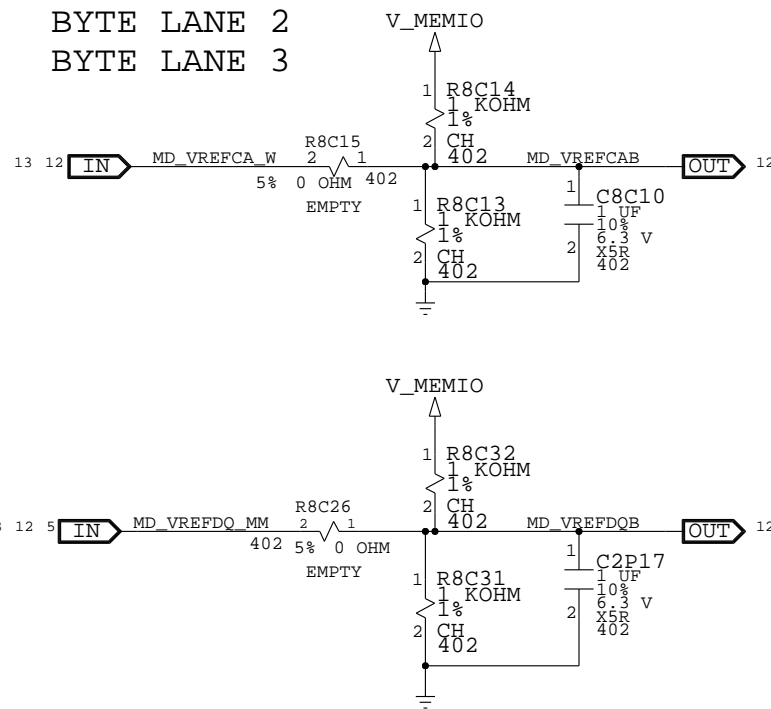
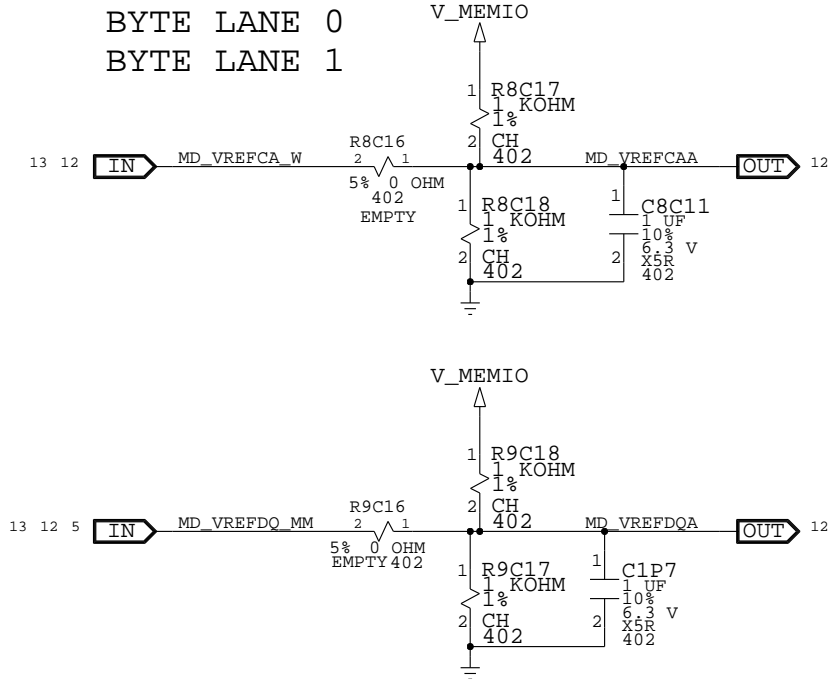
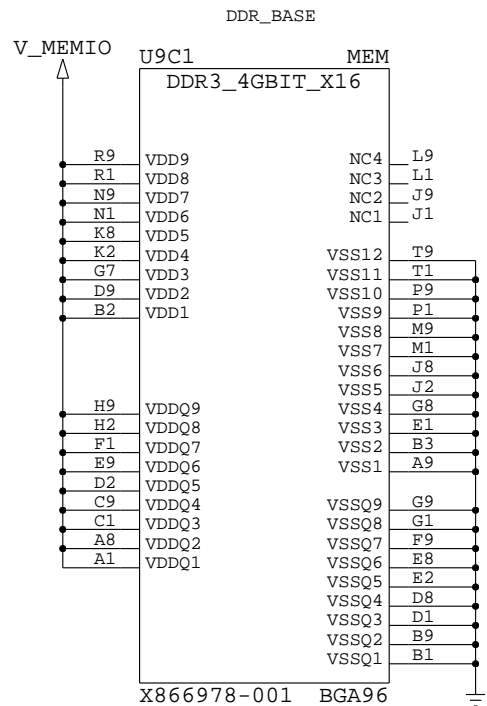
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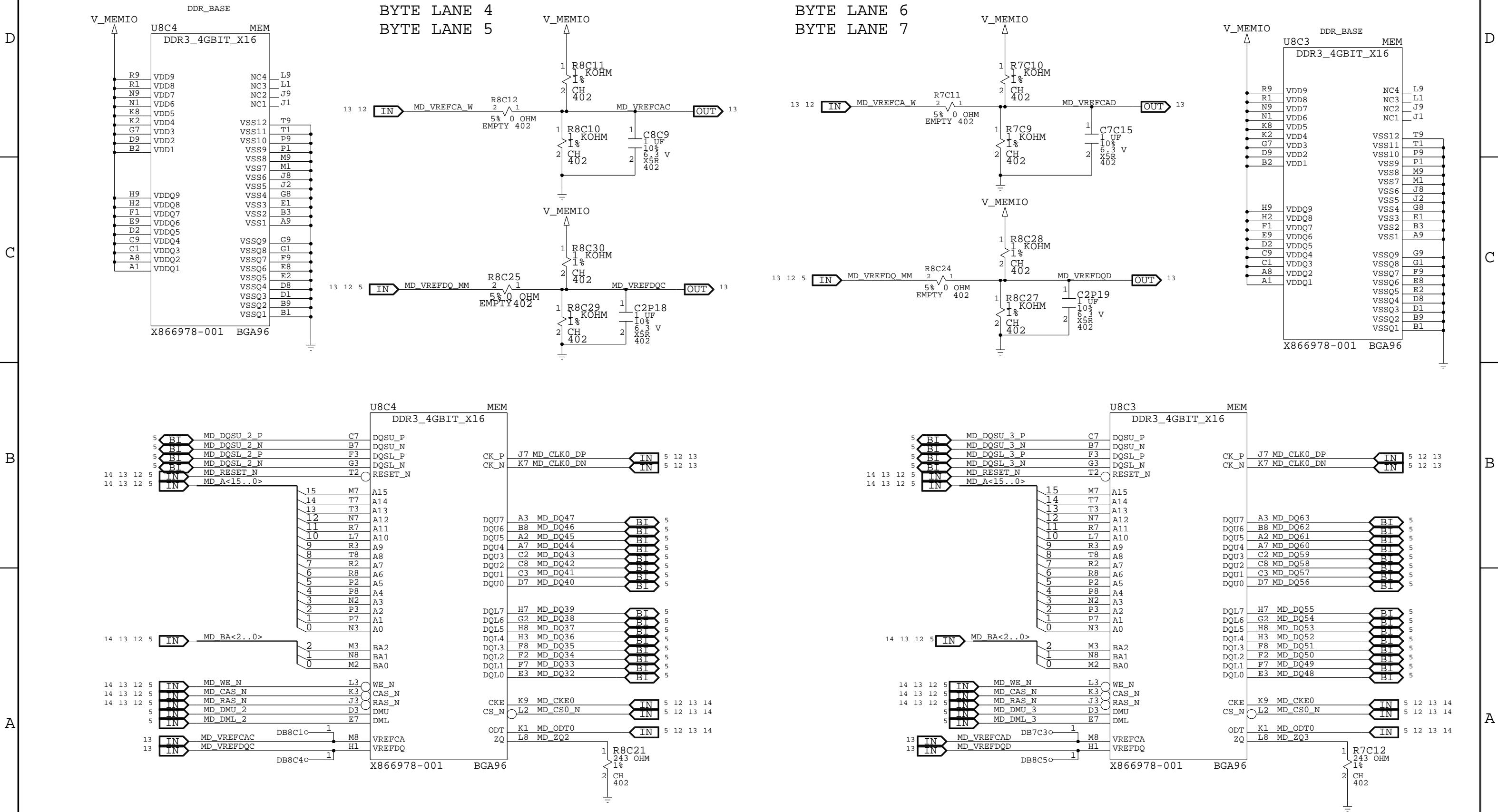
C

B

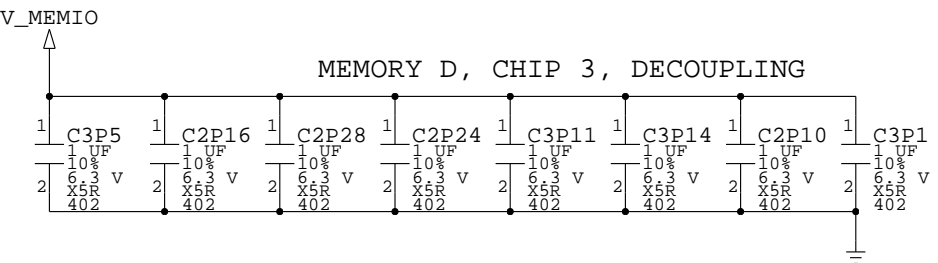
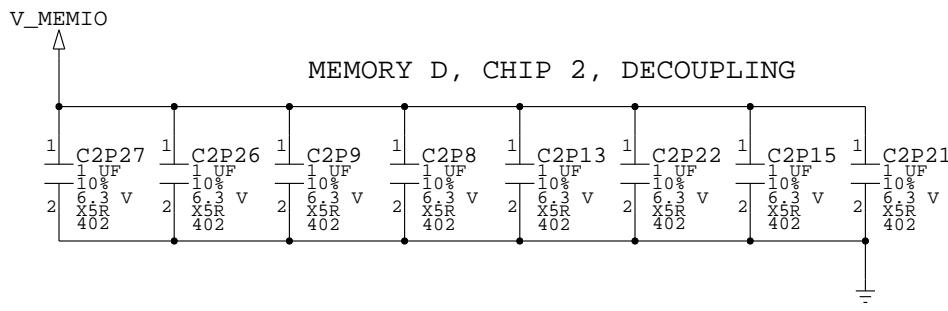
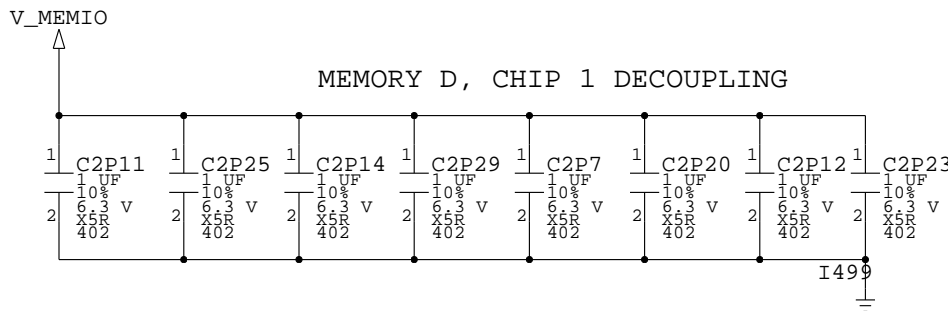
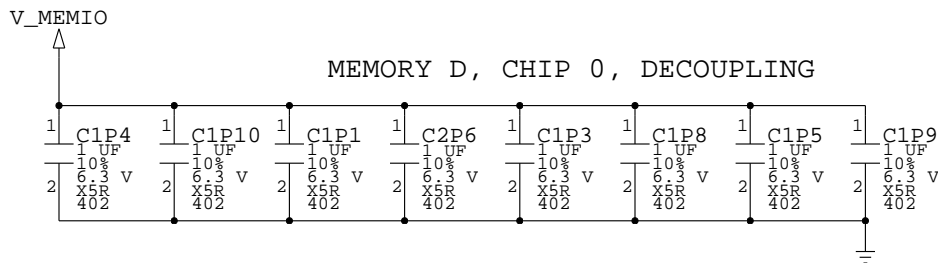
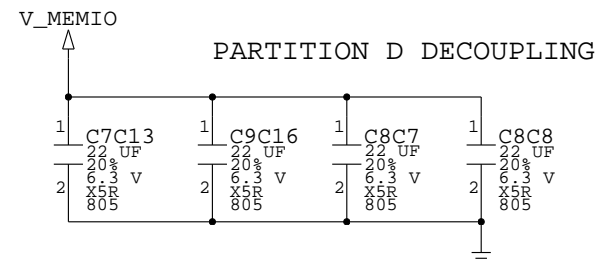
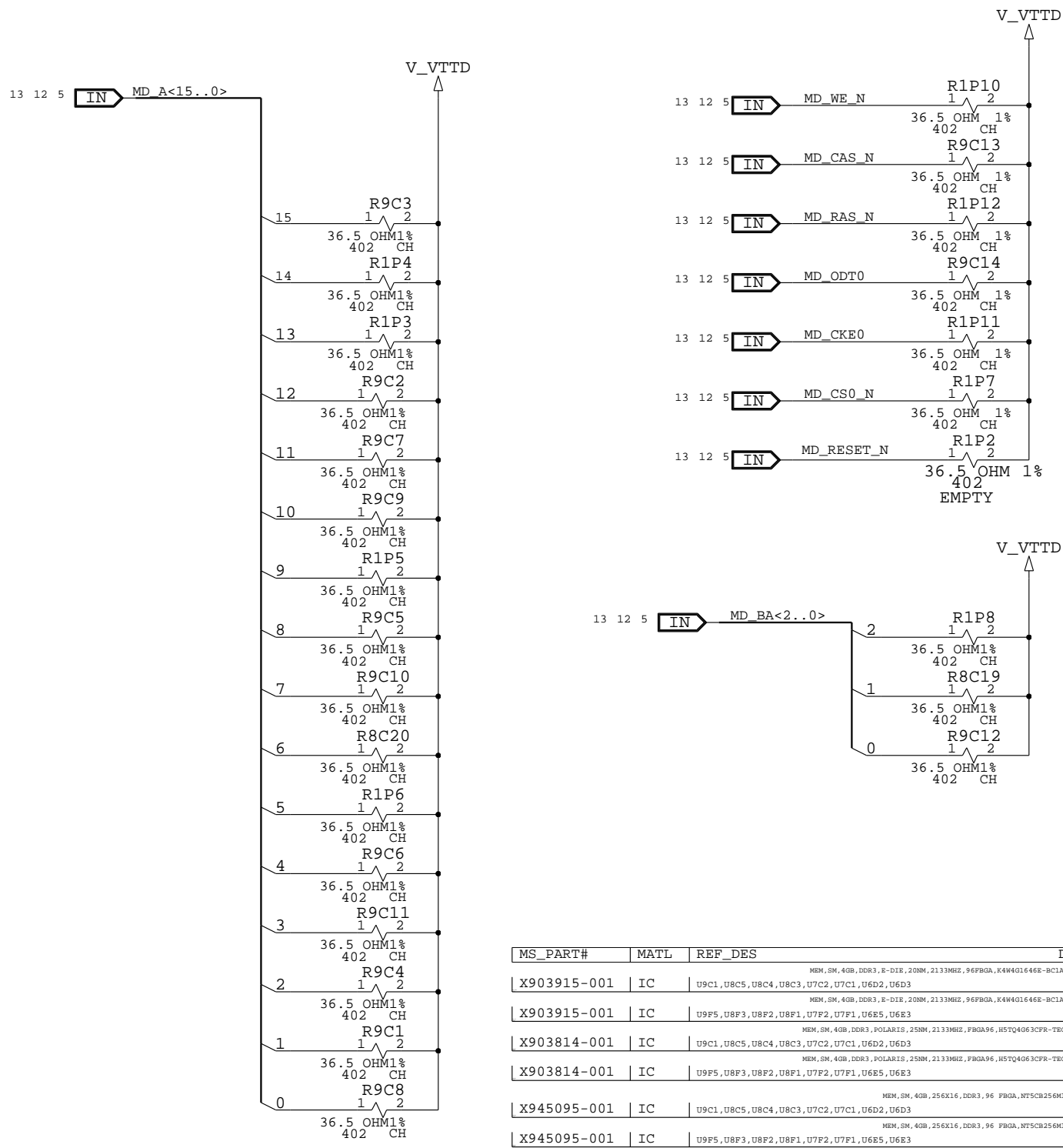
A



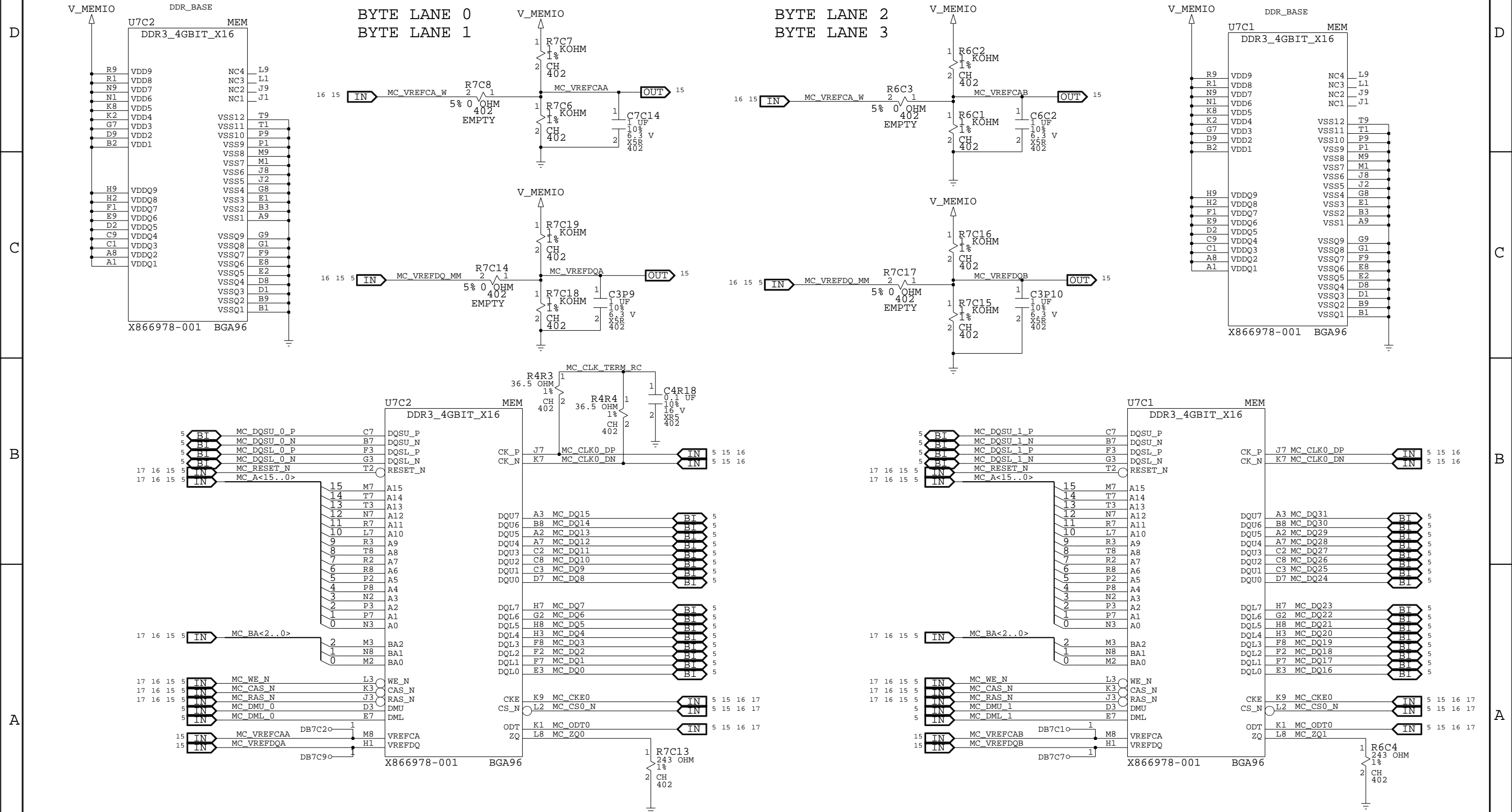
MEMORY: CHANNEL D



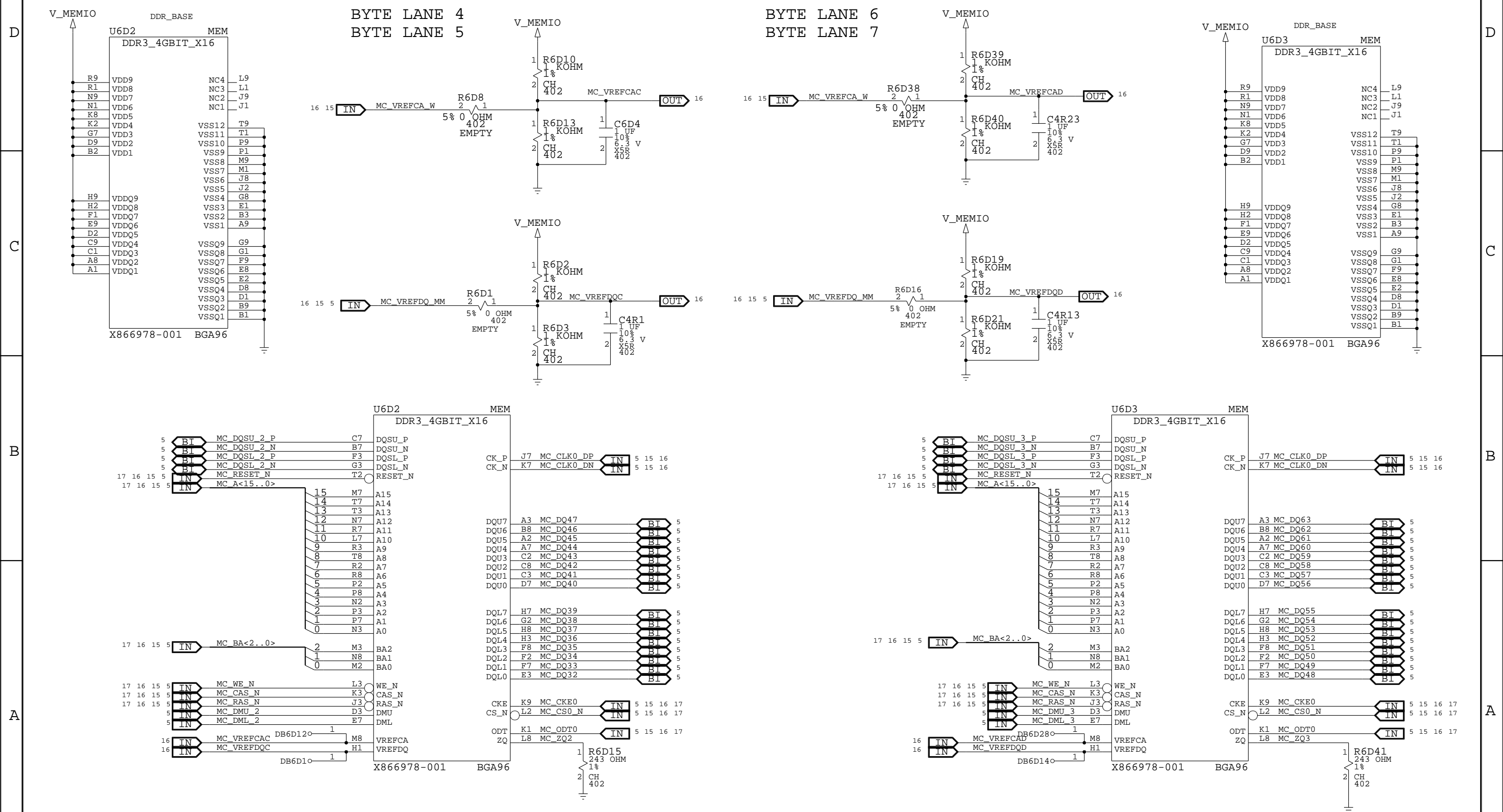
MEMORY: CHANNEL D, DECOUPLING & TERMINATION



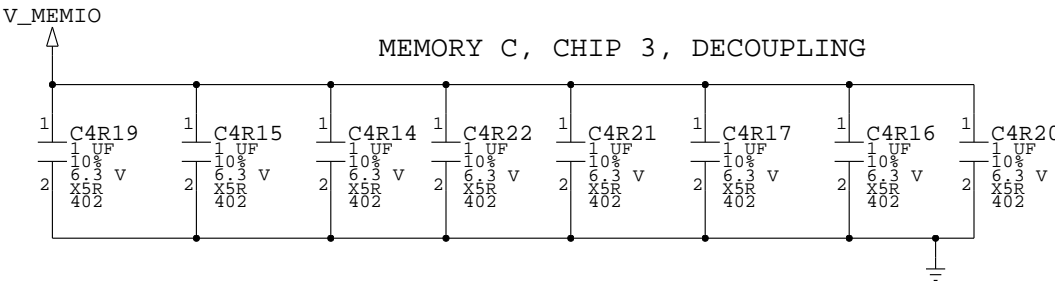
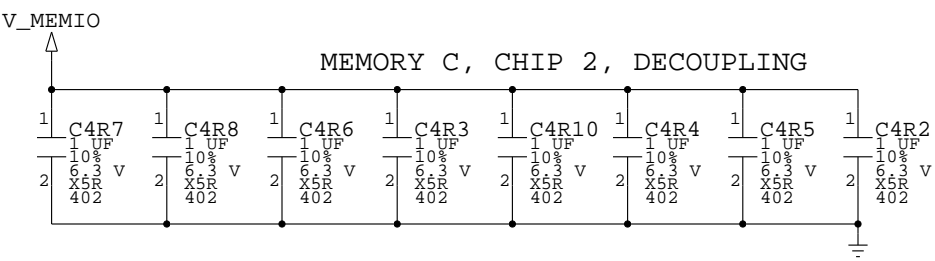
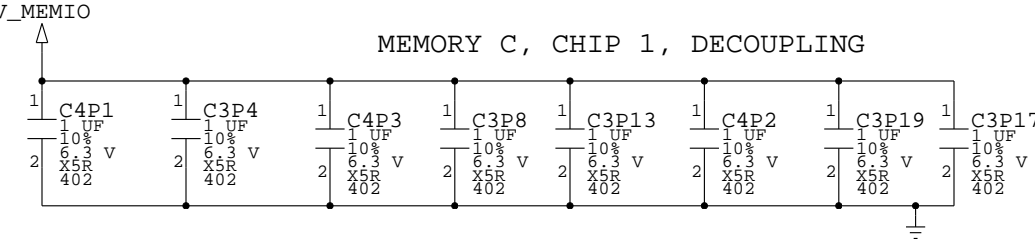
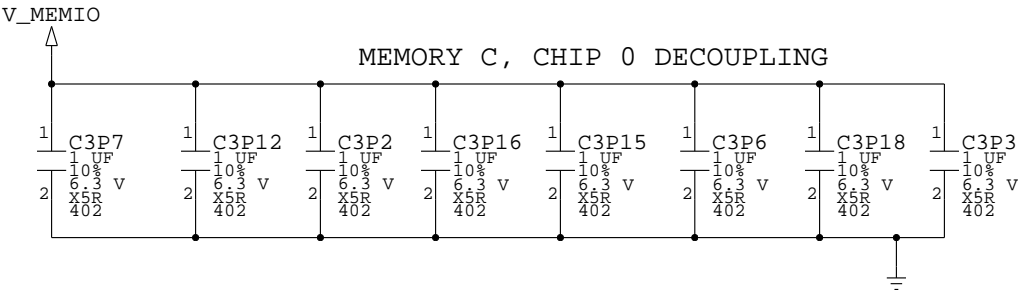
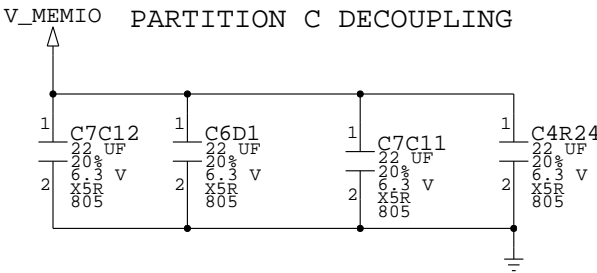
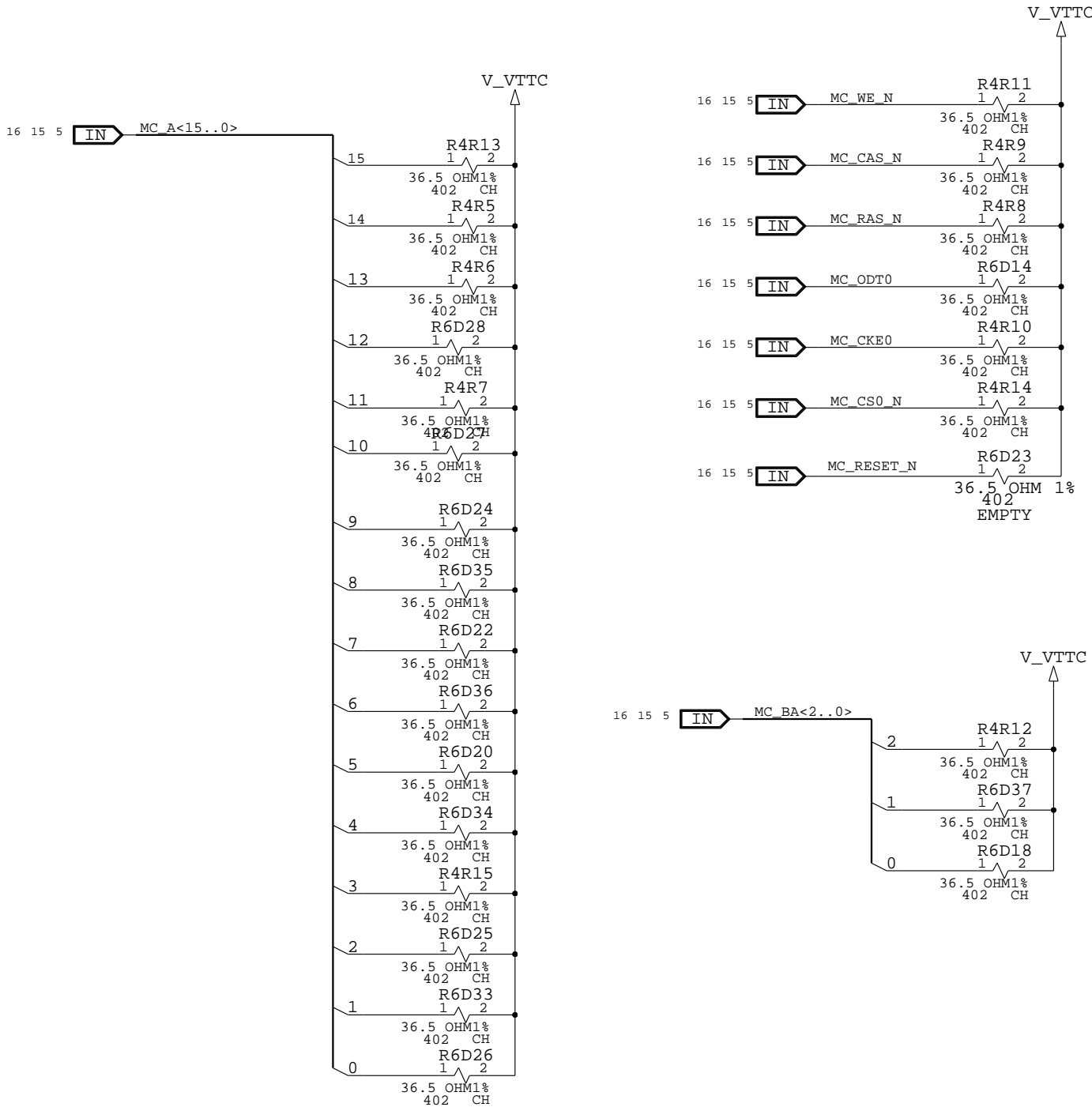
MEMORY: CHANNEL C



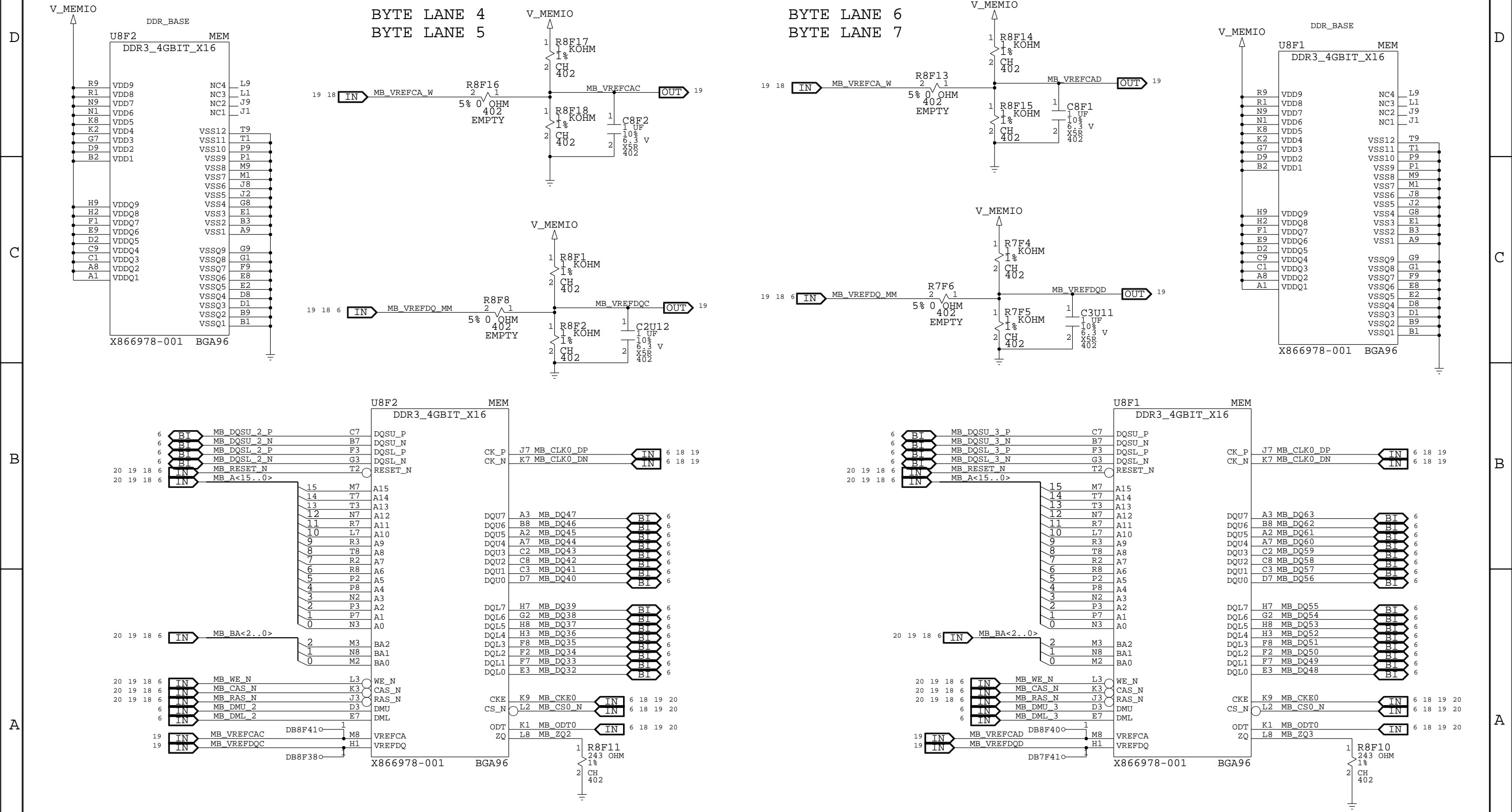
MEMORY: CHANNEL C



MEMORY: CHANNEL C, DECOUPLING & TERMINATION



MEMORY: CHANNEL B



MEMORY: CHANNEL B, DECOUPLING & TERMINATION

D

C

B

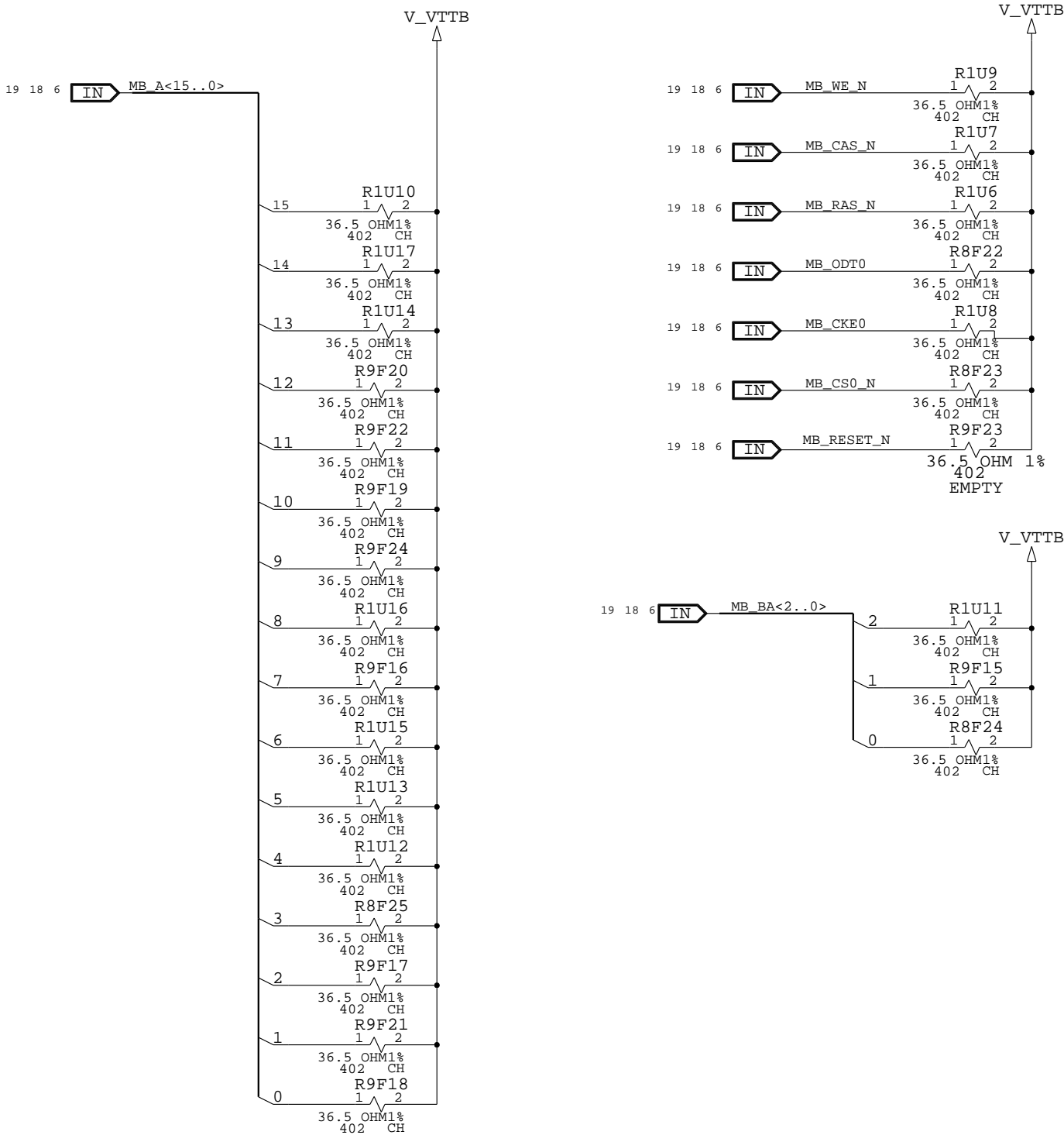
A

D

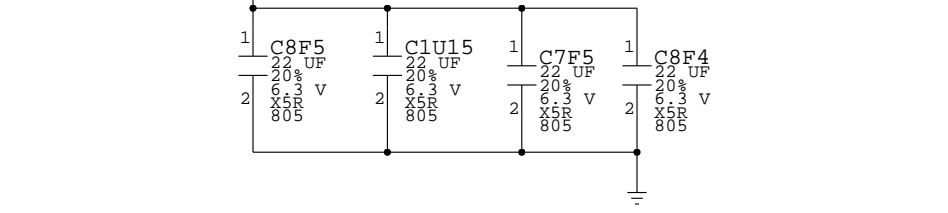
C

B

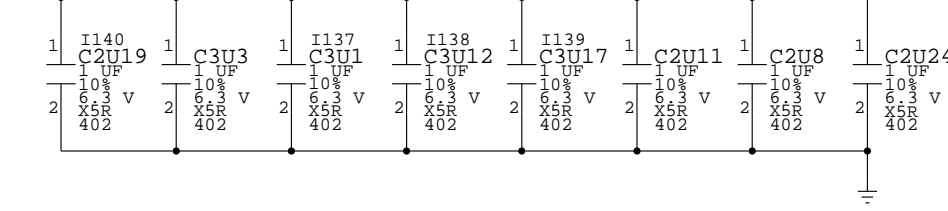
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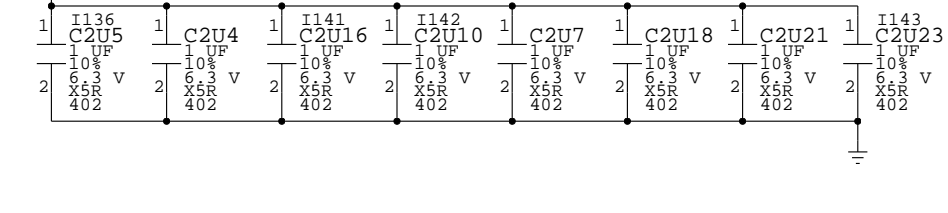
PARTITION B DECOUPLING



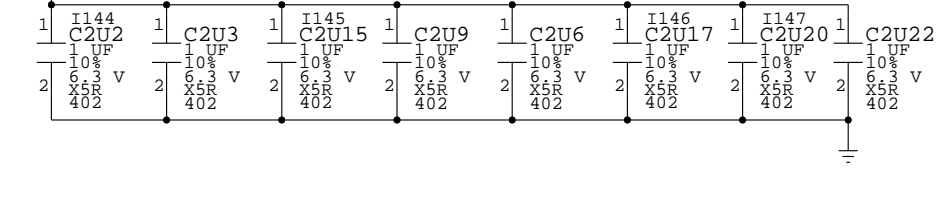
MEMORY B, CHIP 0 DECOUPLING



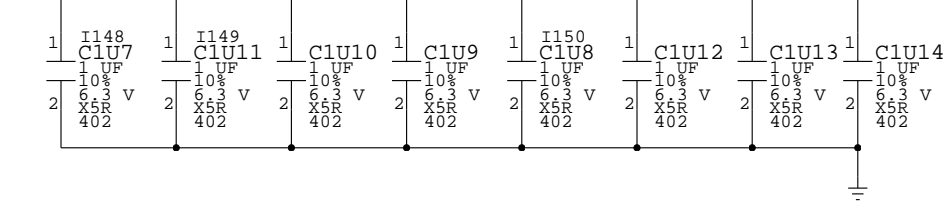
MEMORY B, CHIP 1, DECOUPLING



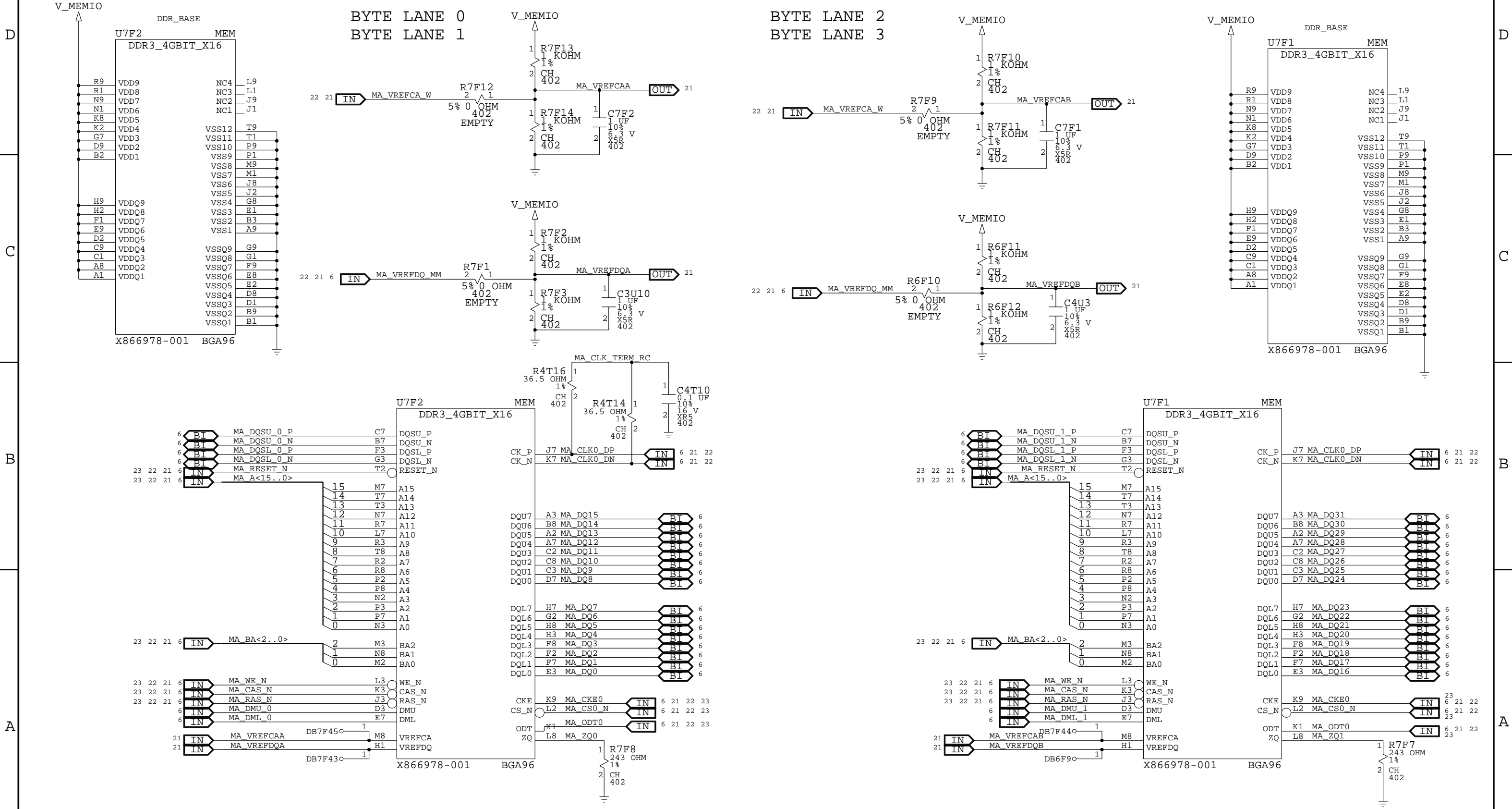
MEMORY B, CHIP 2, DECOUPLING



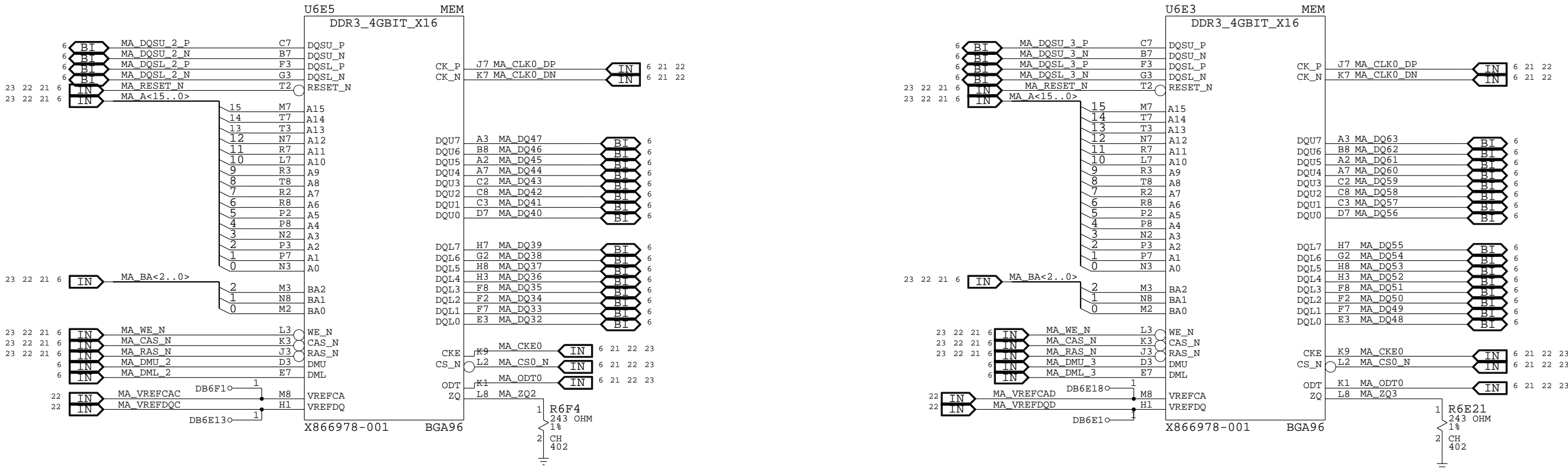
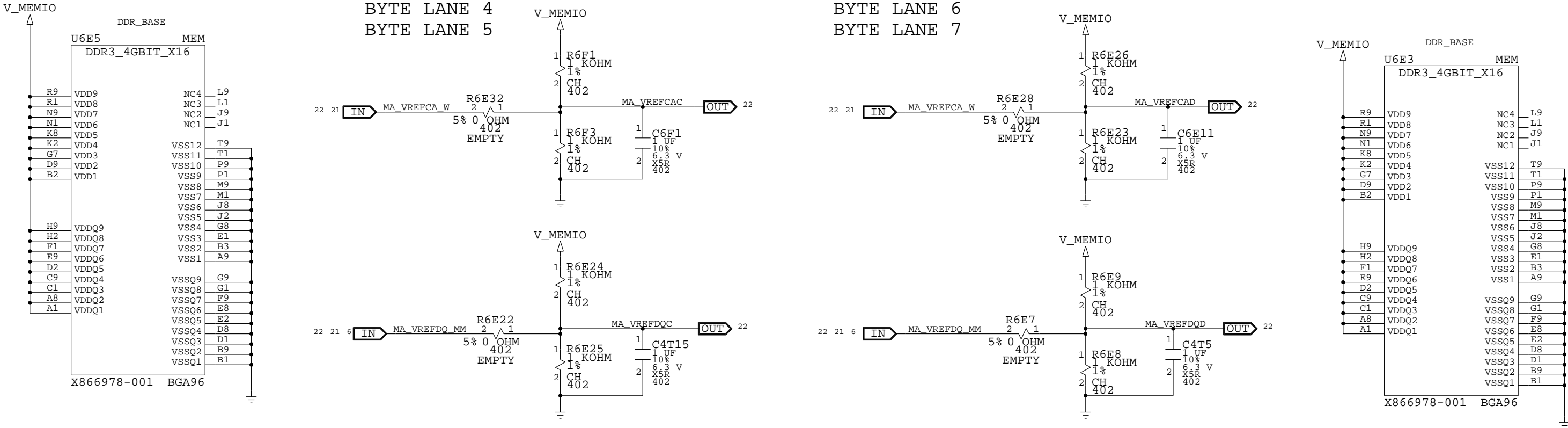
MEMORY B, CHIP 3, DECOUPLING

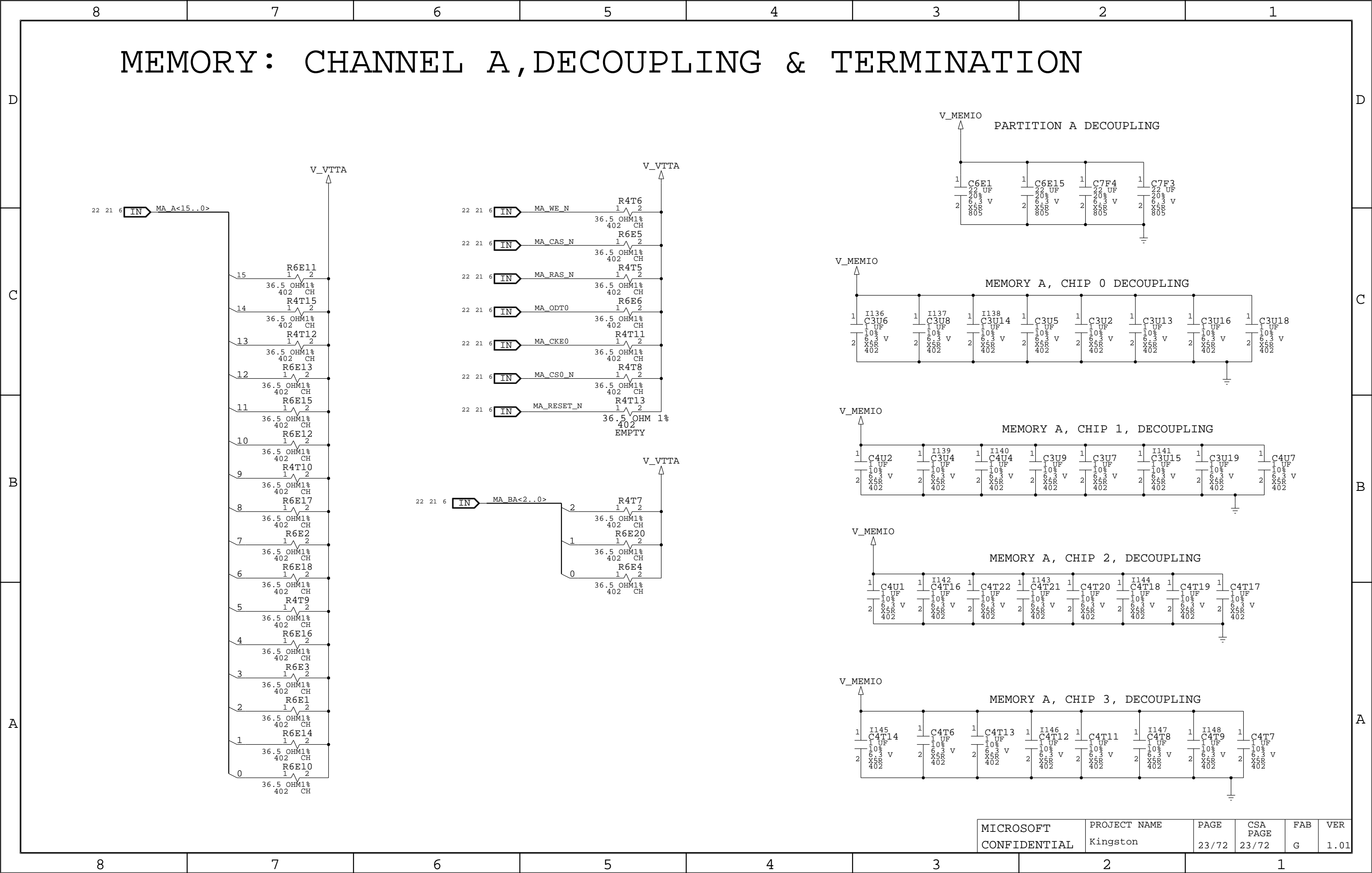


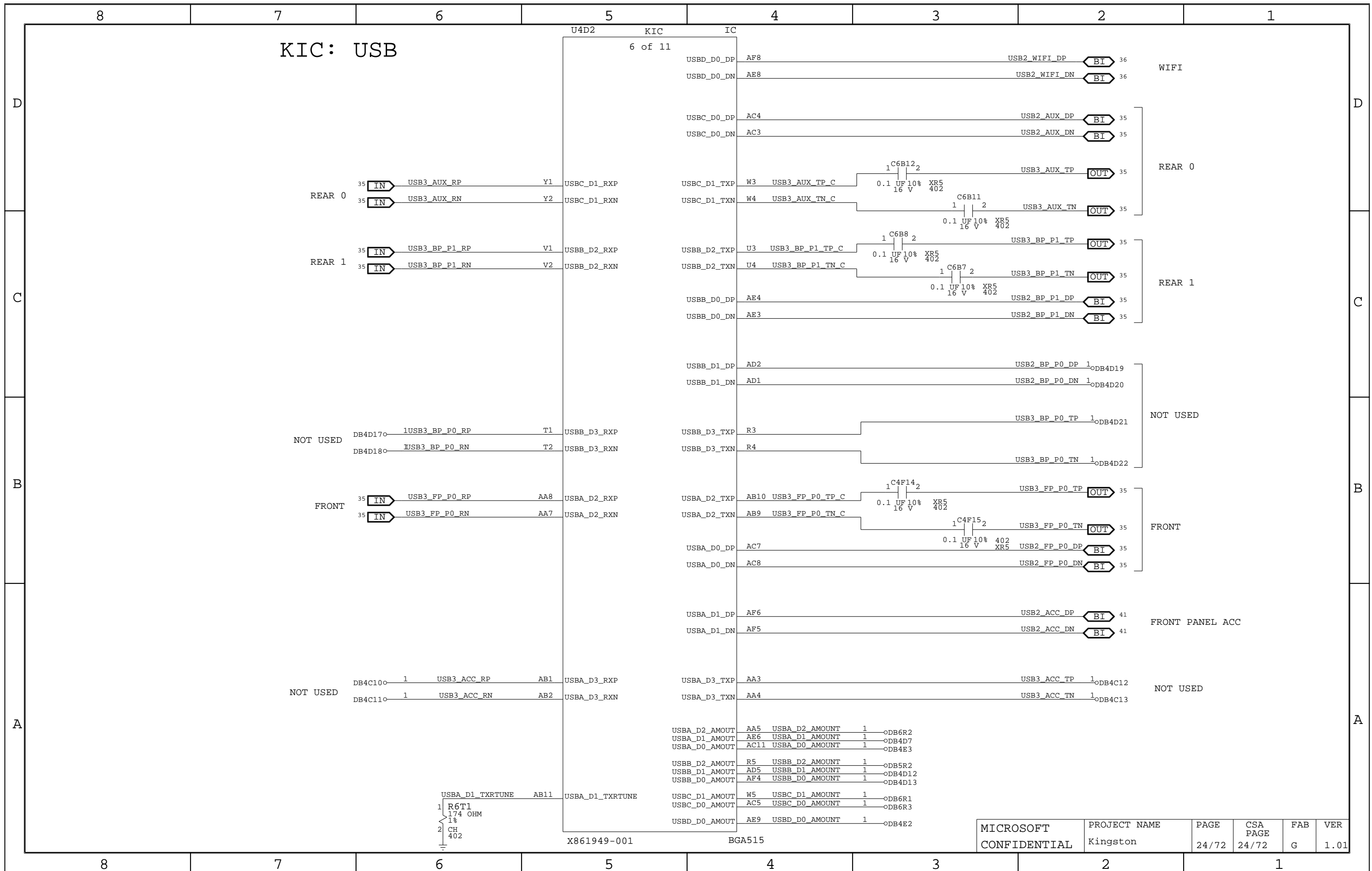
MEMORY: CHANNEL A



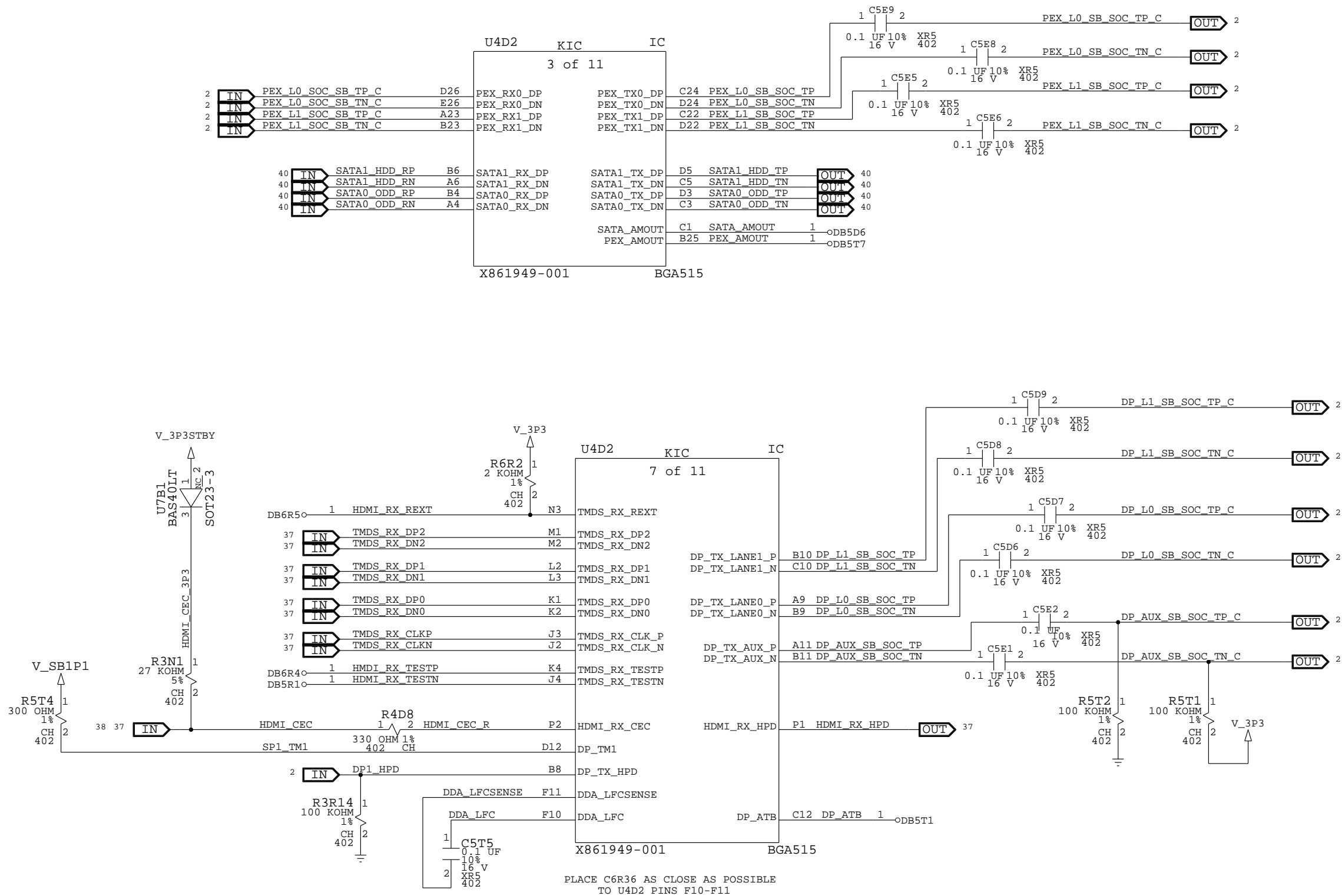
MEMORY: CHANNEL A



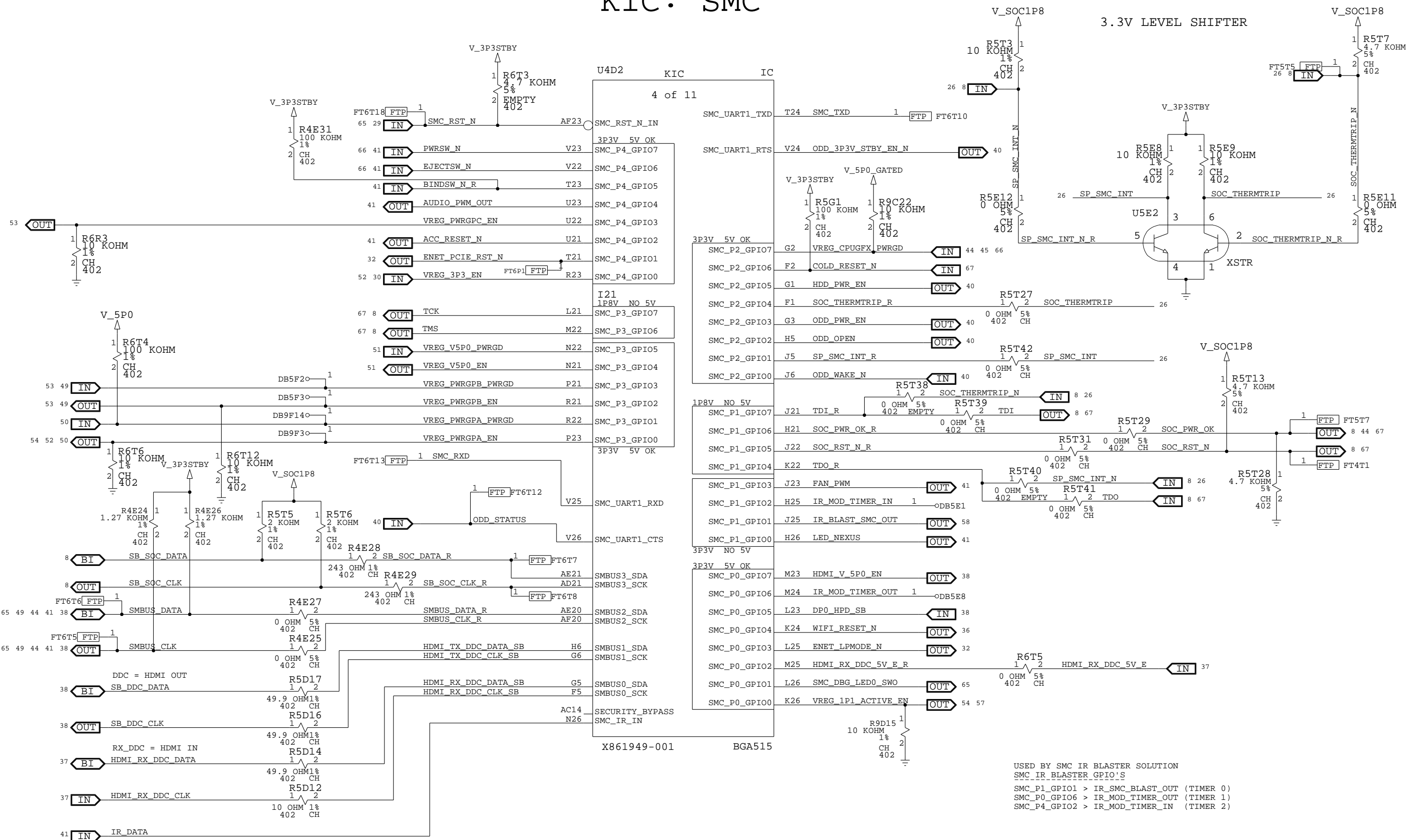




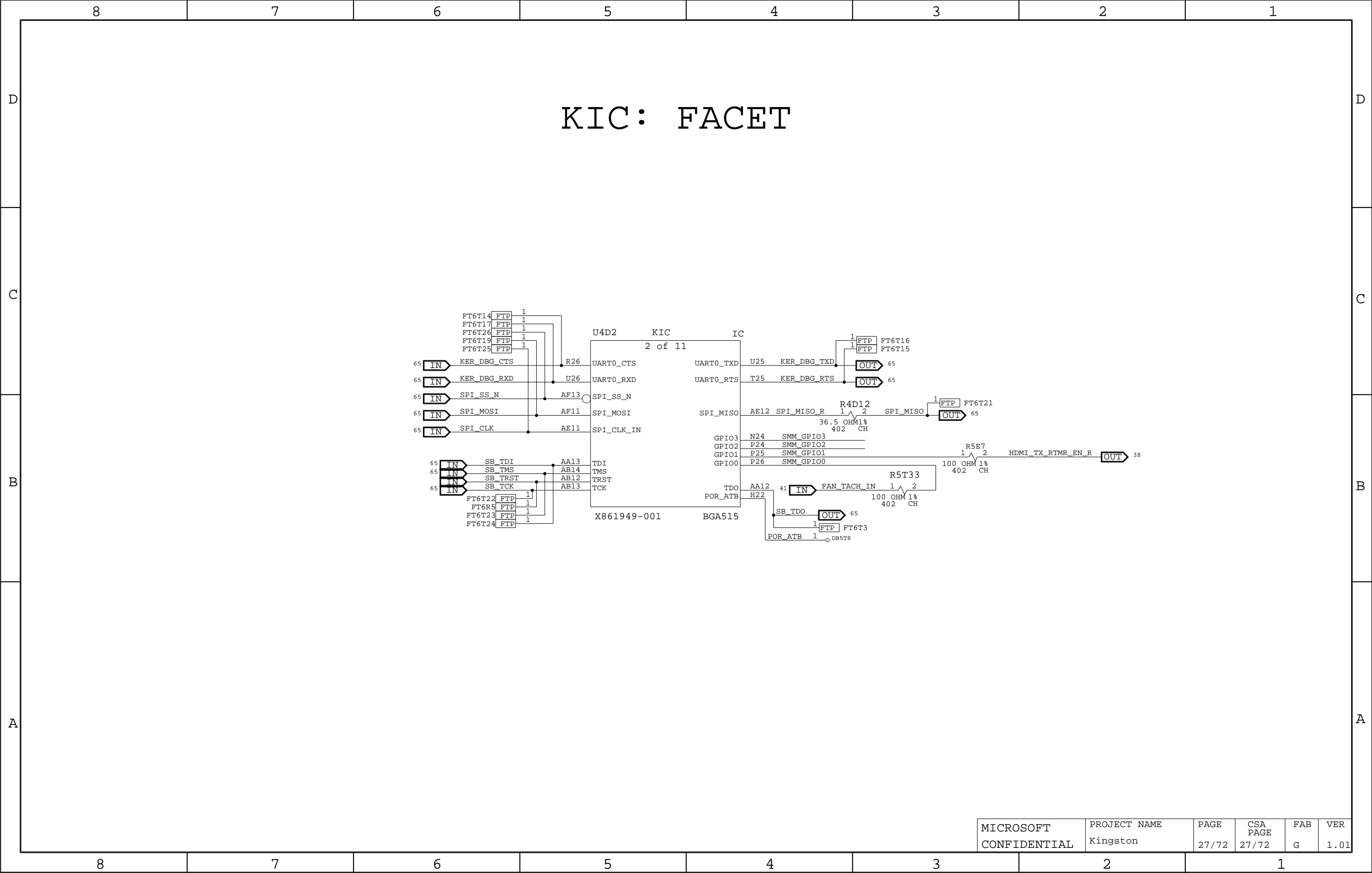
KIC: PCIEX, SATA, VIDEO

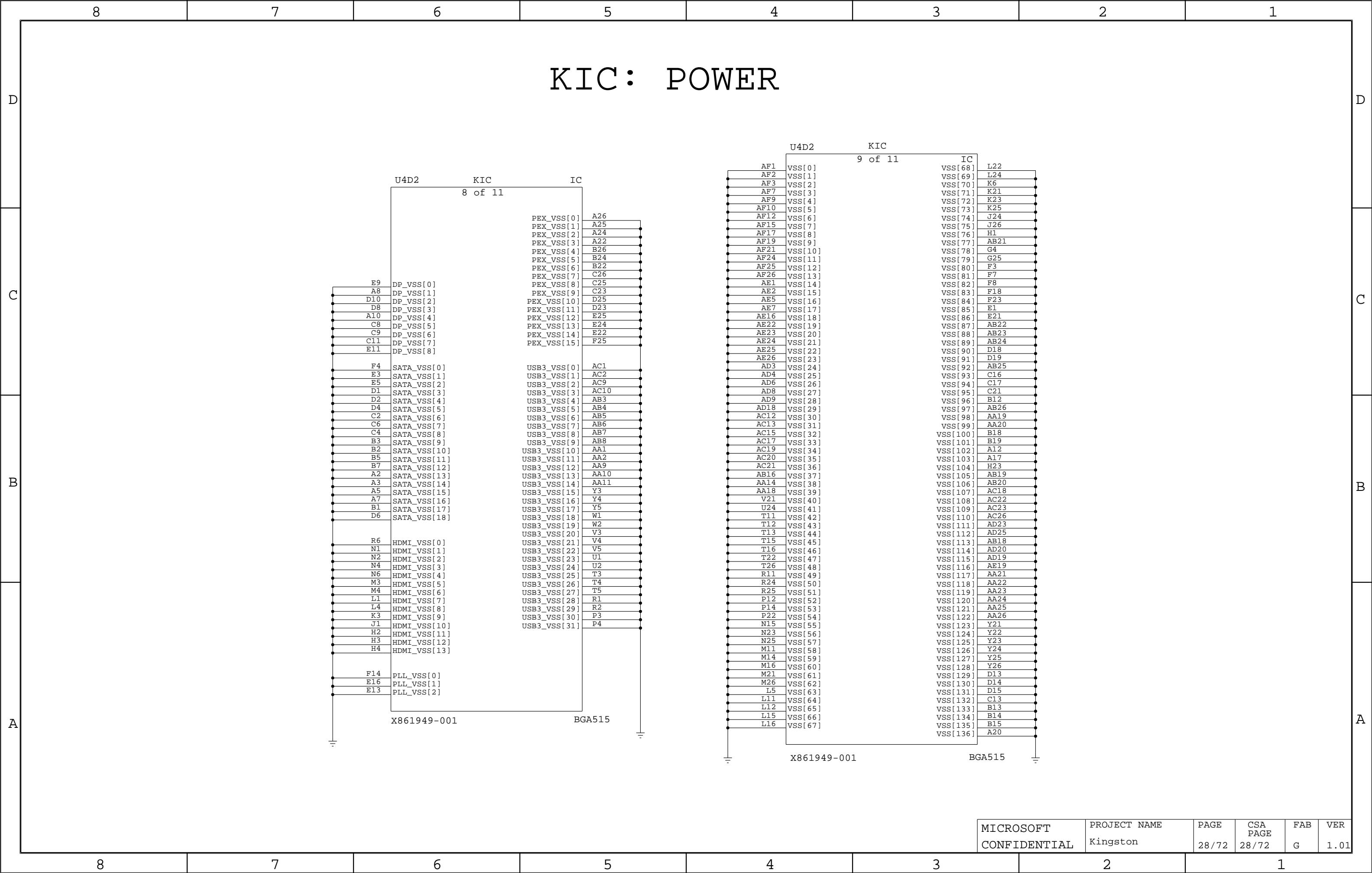


KIC: SMC

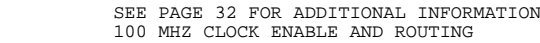


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| MICROSOFT | PROJECT NAME | PAGE | CSA PAGE | FAB | VER |
| CONFIDENTIAL | Kingston | 26/72 | 26/72 | G | 1.01 |





KIC: CLOCKS, STRAPPING, POR

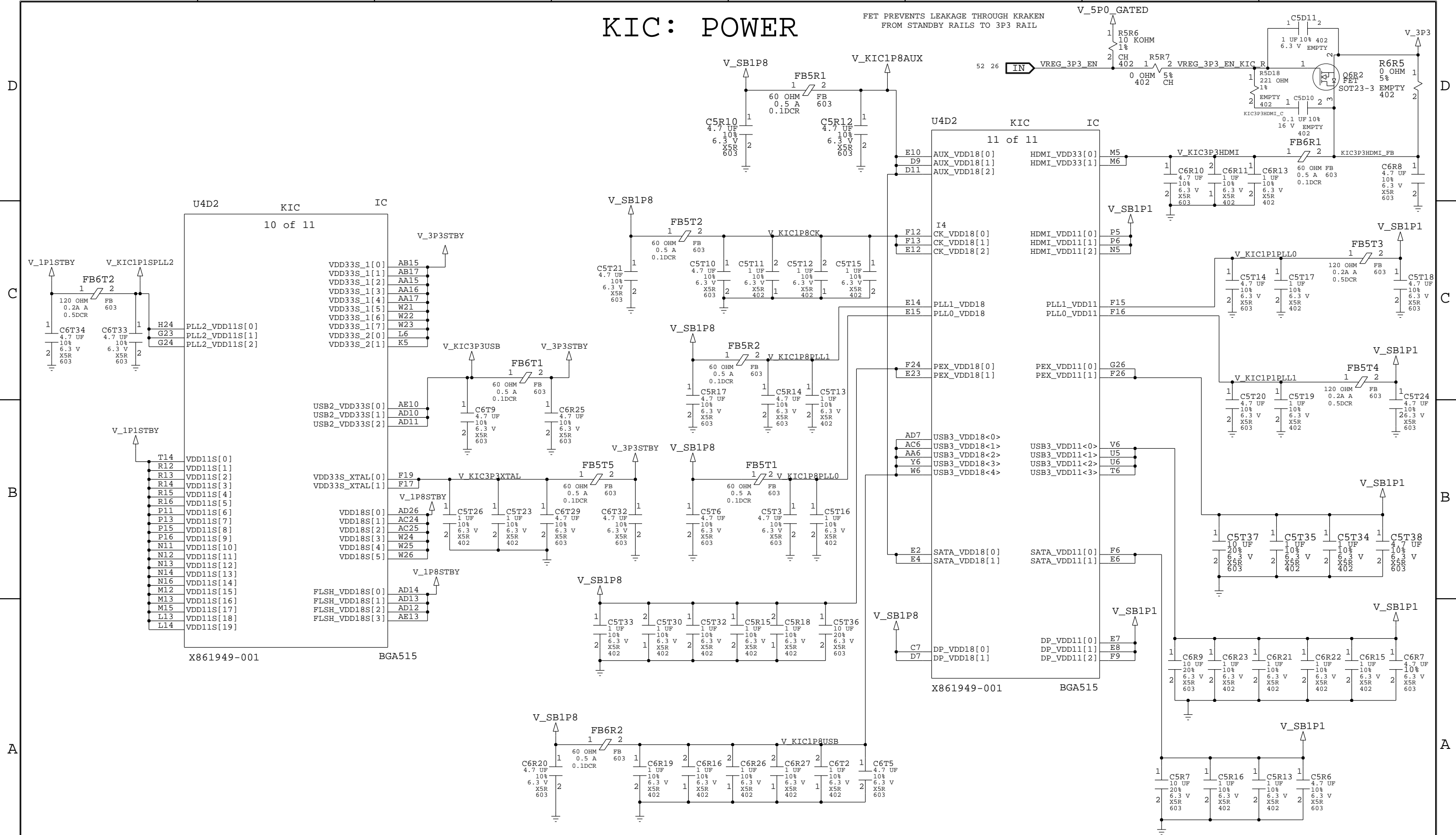


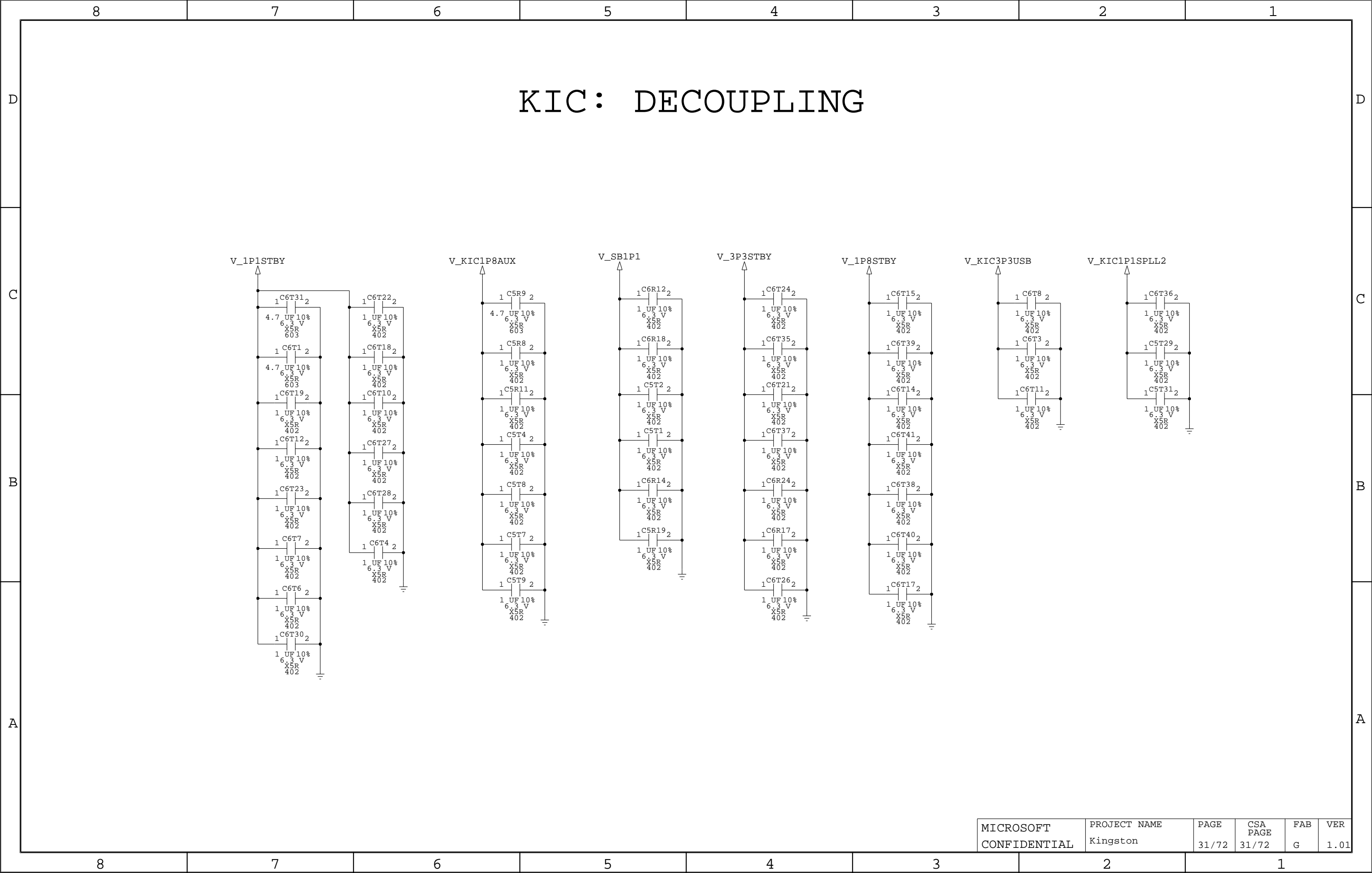
ULTRA MINIATURE COAX
TO SMA CABLE ASSEMBLY
DIGIKEY PN: 931-1098-ND

| MS_PART# | MATL | REF_DES | DESCR. | BOM_PROPERTY |
|-------------|------|---------|---------------------|--------------|
| X861949-005 | IC | U4D2 | IC,KRAKEN SB,BGA515 | KIC_RETAIL |
| X861949-003 | IC | U4D2 | IC,KRAKEN SB,BGA515 | KIC_DEV |

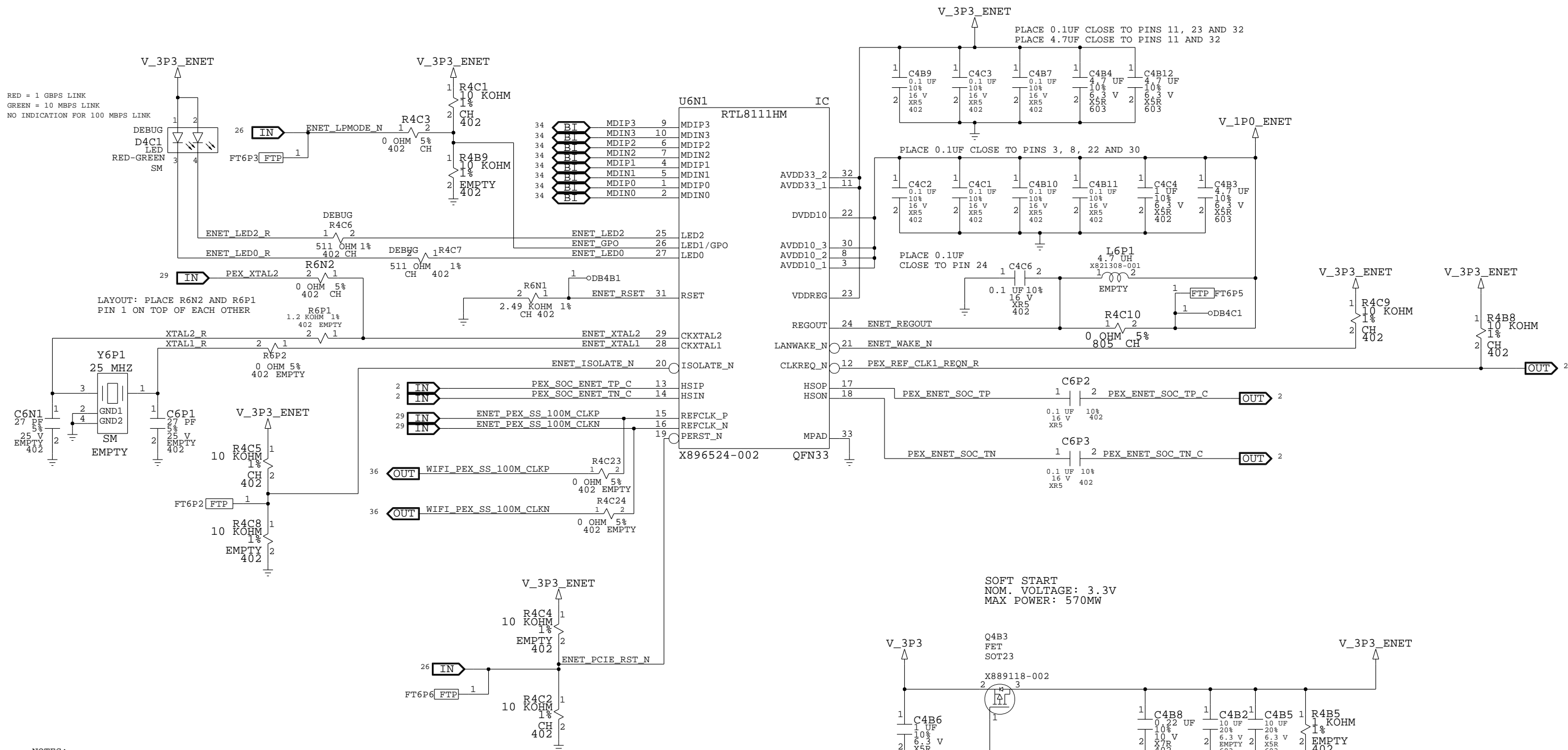
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|--------------|--------------|-------|-------------|-----|------|
| MICROSOFT | PROJECT NAME | PAGE | CSA PAGE | FAB | VER |
| CONFIDENTIAL | Kingston | 29/72 | 29/72 | G | 1.01 |

KIC: POWER





ETHERNET CONTROLLER



- NOTES:
- 1. THE RTL8111HM IS CONFIGURED FROM REALTEK WITH EFUSE "ENABLE LAN DISABLE" MODE SET, WHICH PROVIDES DEFAULT SUPPORT FOR SIGNAL ENET_LPMODE_N. THIS FEATURE CAN BE OVERRIDDEN BY SOFTWARE
 - 2. TO SUPPORT A PCIE WIFI INTERFACE (J3C1), THE FOLLOWING BOM CHANGES ARE NEEDED:
 - A: POPULATE R4C23 AND R4C24, WHICH WILL SEND THE 100 MHZ CLOCK TO THE WIFI INTERFACE. IN ADDITION, IT IS CRITICAL THAT EACH LEG OF THE CLOCK BE TERMINATED AT THE FAR END INTO 50 OHMS.
 - B: ON PAGE 2, POPULATE AC COUPLING CAPS C6P6 AND C6P7
 - C: FOR PRELIMINARY DEVELOPMENT TESTING, NO OTHER BOM CHANGES ARE REQUIRED. THE ETHERNET CONTROLLER WILL MANAGE THE ENABLING OF THE 100 MHZ CLOCK.
 - D: FOR PRODUCTION RETAIL, ON PAGE 29 REMOVE R4B3 AND POPULATE R4C26. THIS CHANGE WILL REQUIRE MODIFIED SMC FIRMWARE TO EXPLICITLY ENABLE THE 100 MHZ CLOCK.

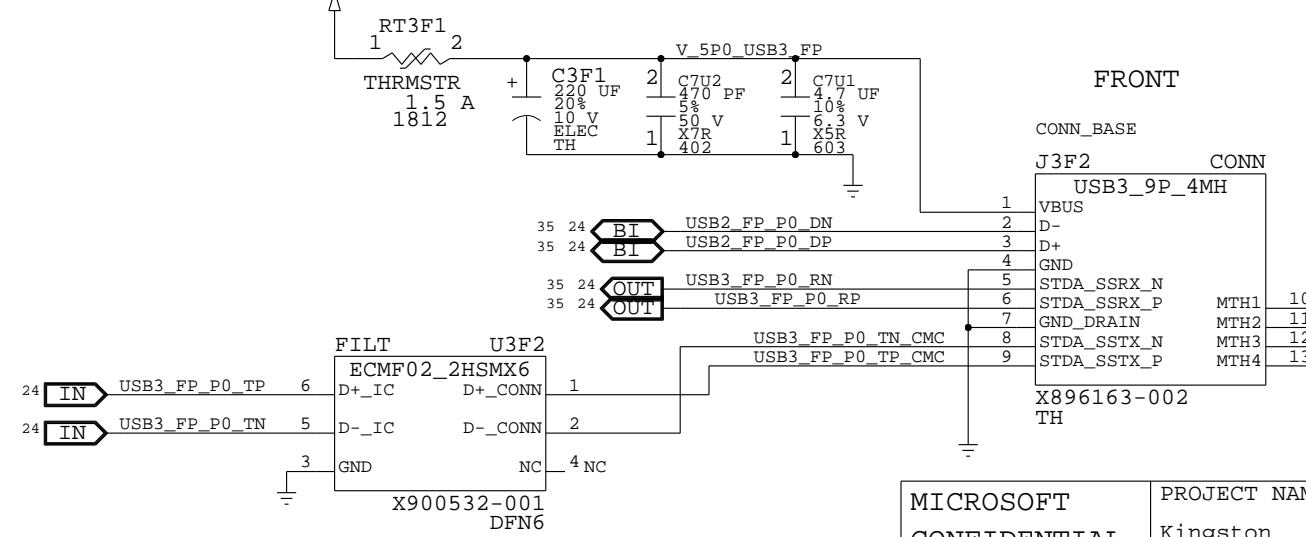
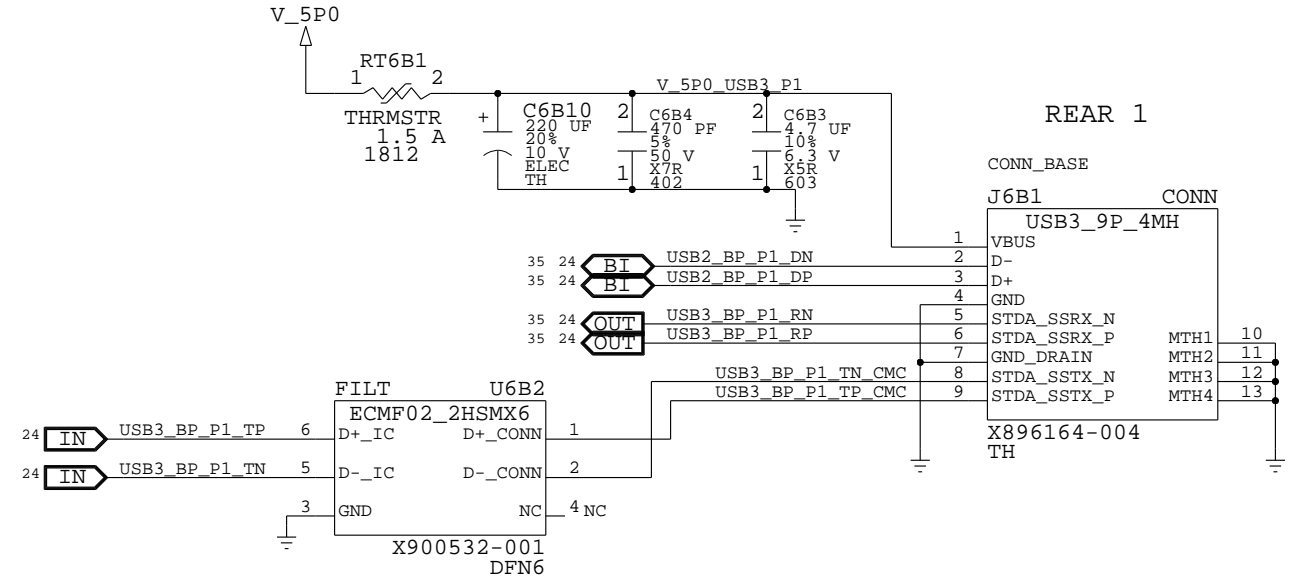
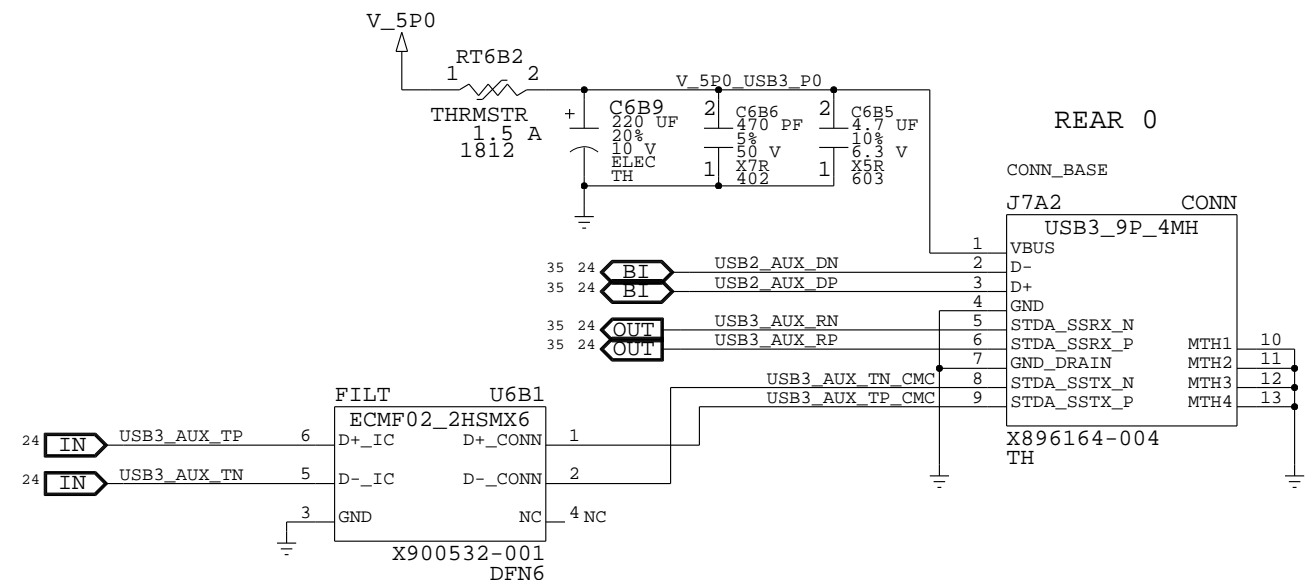
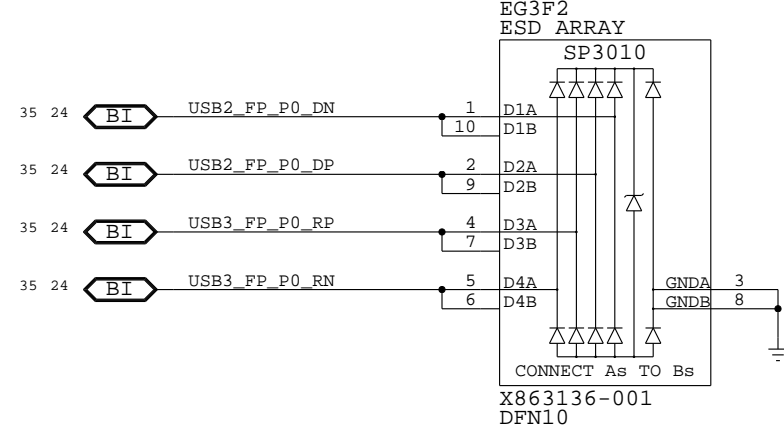
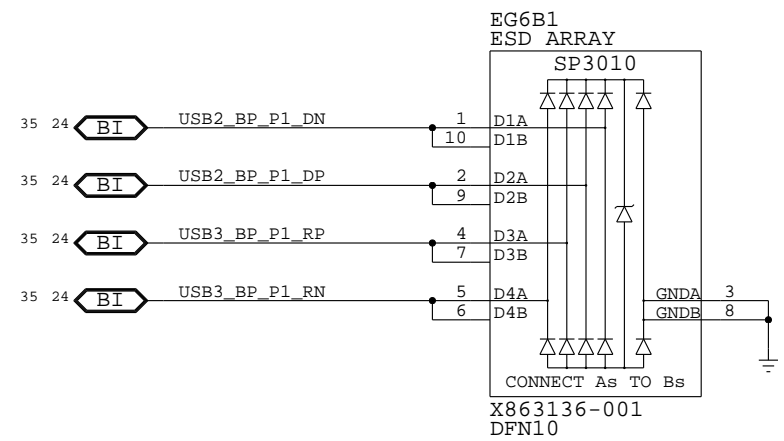
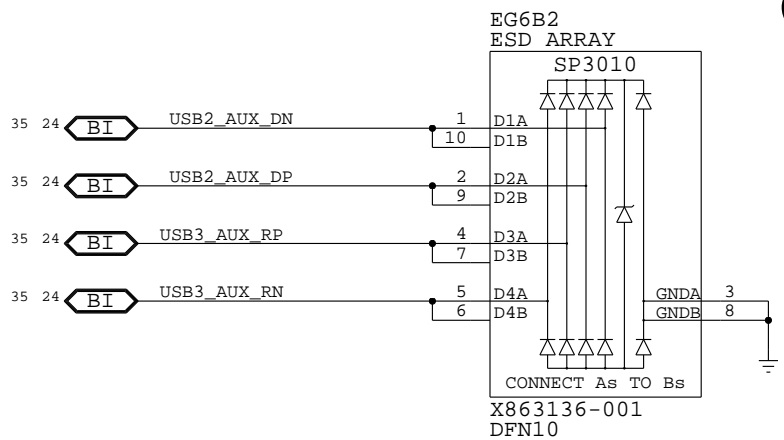
SOFT START
NOM. VOLTAGE: 3.3V
MAX POWER: 570MW

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|---------------------------|--------------------------|---------------|----------------------|----------|-------------|
| MICROSOFT CONFIDENTIAL | PROJECT NAME Kingston | PAGE 32/72 | CSA PAGE 32/72 | FAB G | VER 1.01 |
|---------------------------|--------------------------|---------------|----------------------|----------|-------------|

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|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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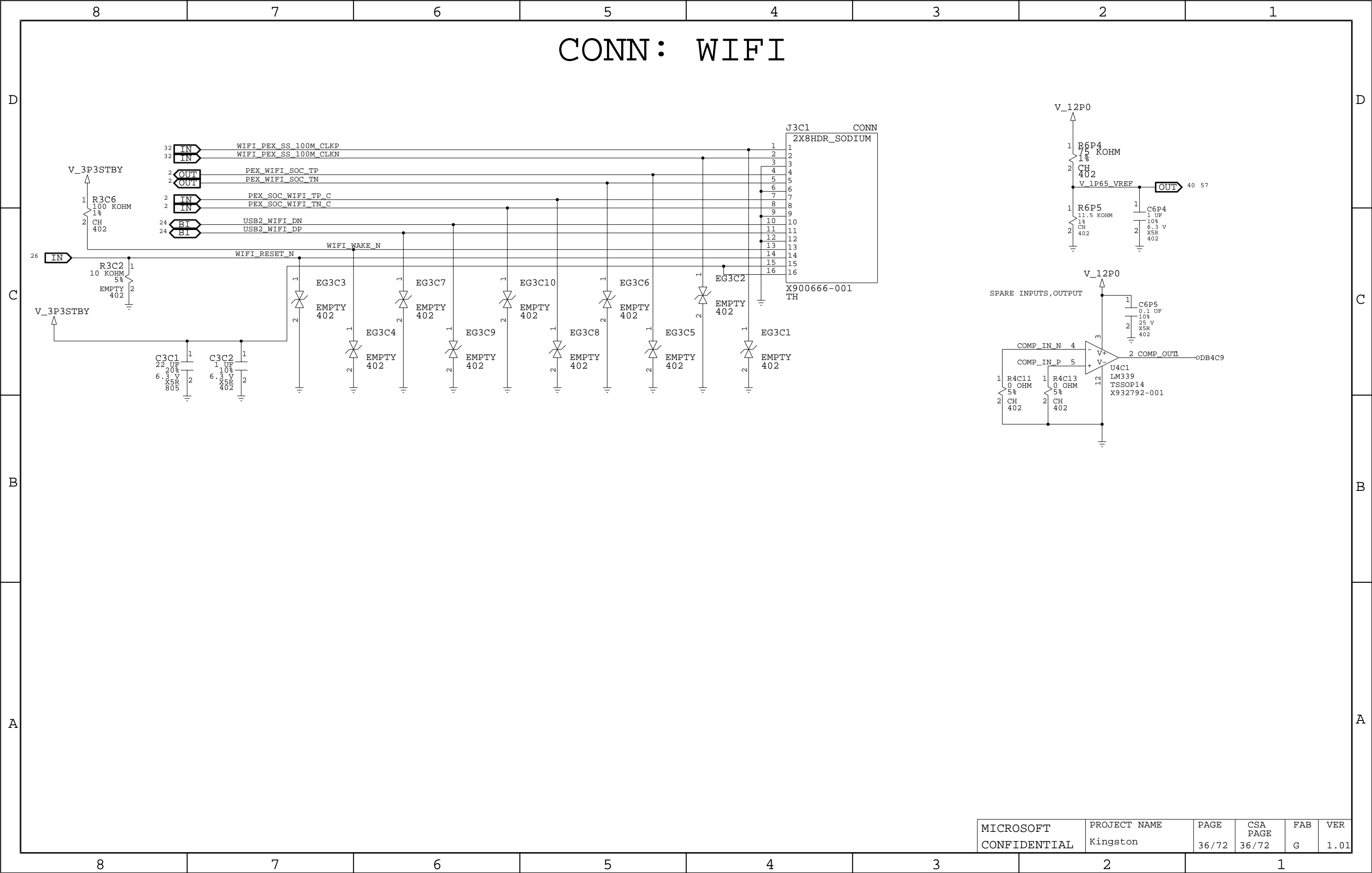


CONN: USB (FRONT & REAR)

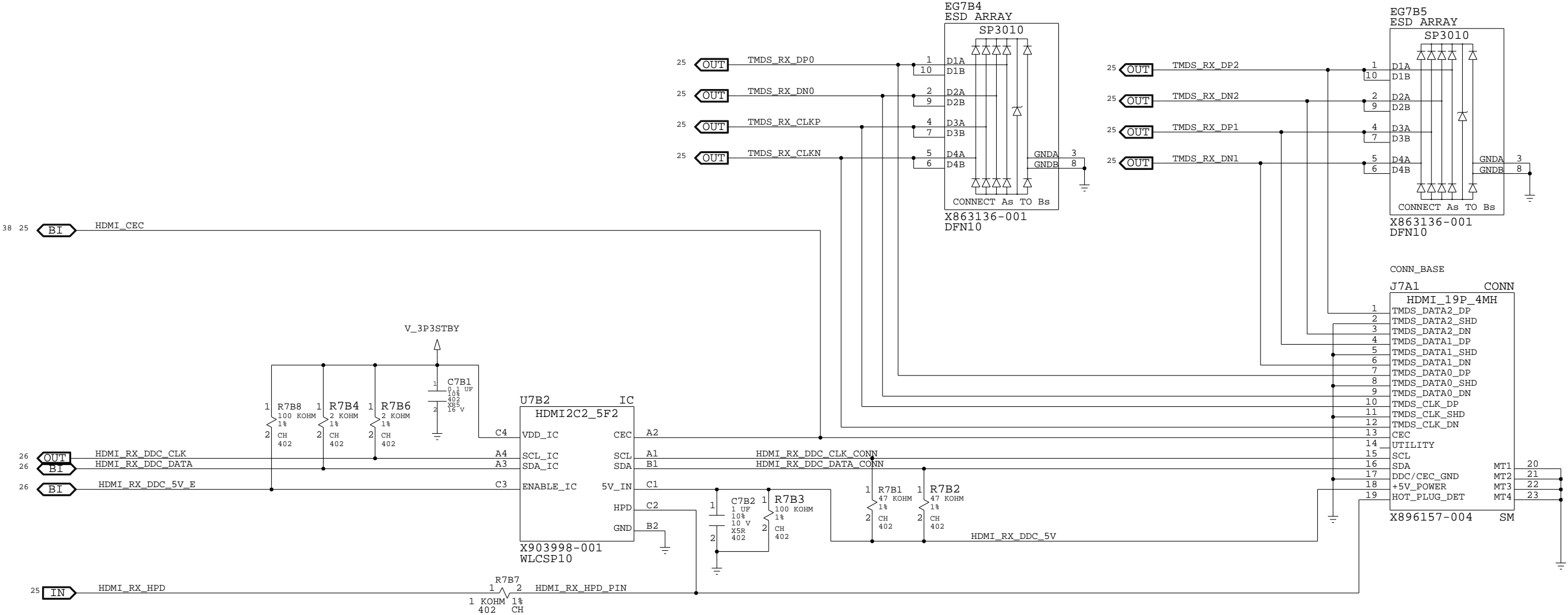


| MS_PART# | MATL | REF_DES | DESCR. | BOM PROPERTY |
|-------------|------|-----------|---|---------------------|
| X896164-004 | CONN | J7A2,J6B1 | CONN-USB,TH,009,FEMALE,USB3-A,BLACK NI, KGS | USB_REAR_FOXC_BLACK |
| X896164-003 | CONN | J7A2,J6B1 | CONN-USB,SM,009,FEMALE,USB3-A,PLAIN NI, KGS | USB_REAR_FOXC_PLAIN |

| MS_PART# | MATL | REF_DES | DESCR. | BOM PROPERTY |
|-------------|------|---------|---|----------------|
| X896163-004 | CONN | J3F2 | CONN-USB,TH,009,FEMALE,FRONT,USB3-A,BLACK NICKEL, KGS | USB_FRONT_FOXC |
| X907318-002 | CONN | J3F2 | CONN-USB,TH,009,FEMALE,FRONT,USB3-A,KGS,(QUAL-AMPHENOL) | USB_FRONT_AMPH |



CONN: HDMI IN



D



H

B

A

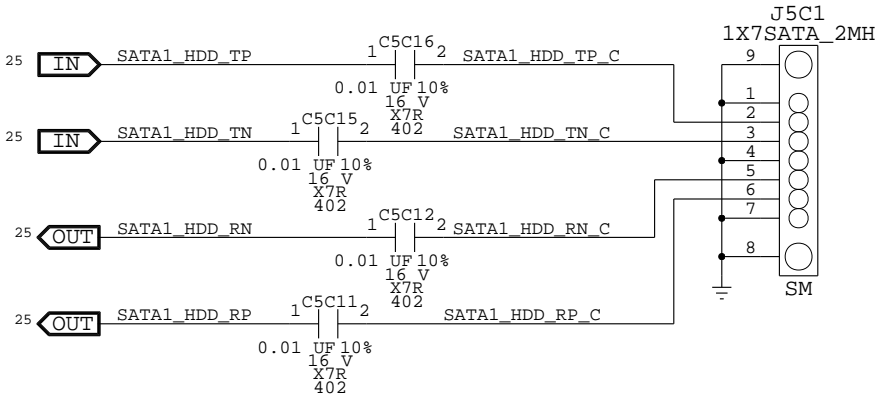
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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|

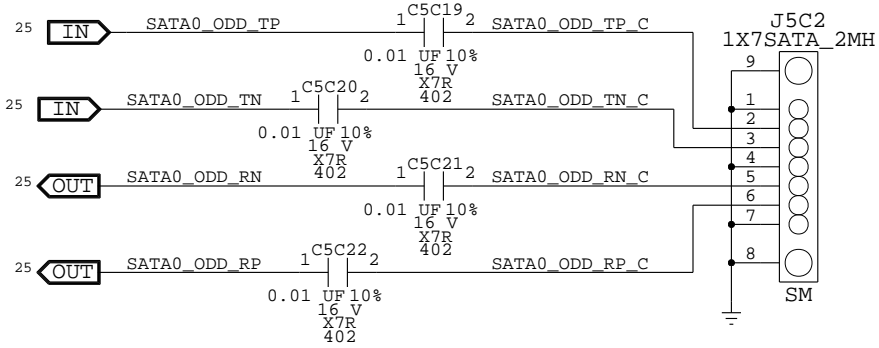
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|--------------------|--|-------|--|---|--|---|--|---|--|---|--|---|--|---|--|
| 8 | | 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | |
| CONN: HDMI SUPPORT | | | | | | | | | | | | | | | |
| D | | | | | | | | | | | | | | D | |
| C | | | | | | | | | | | | | | C | |
| B | | BLANK | | | | | | | | | | | | B | |
| A | | | | | | | | | | | | | | A | |
| 8 | | 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | |
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CONN: ODD & HDD

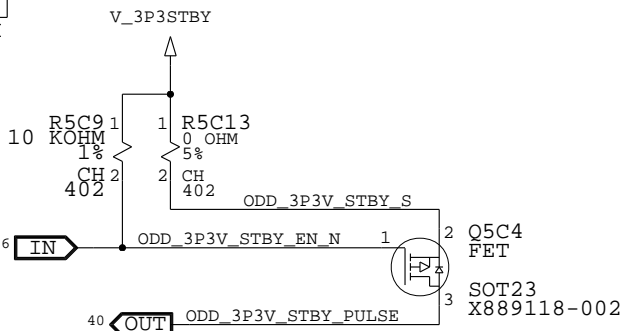
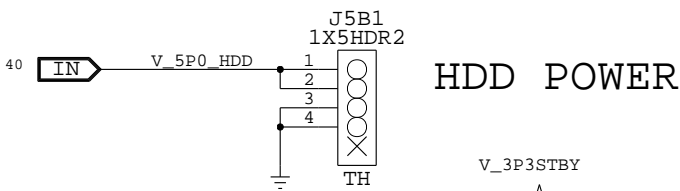
HDD SATA



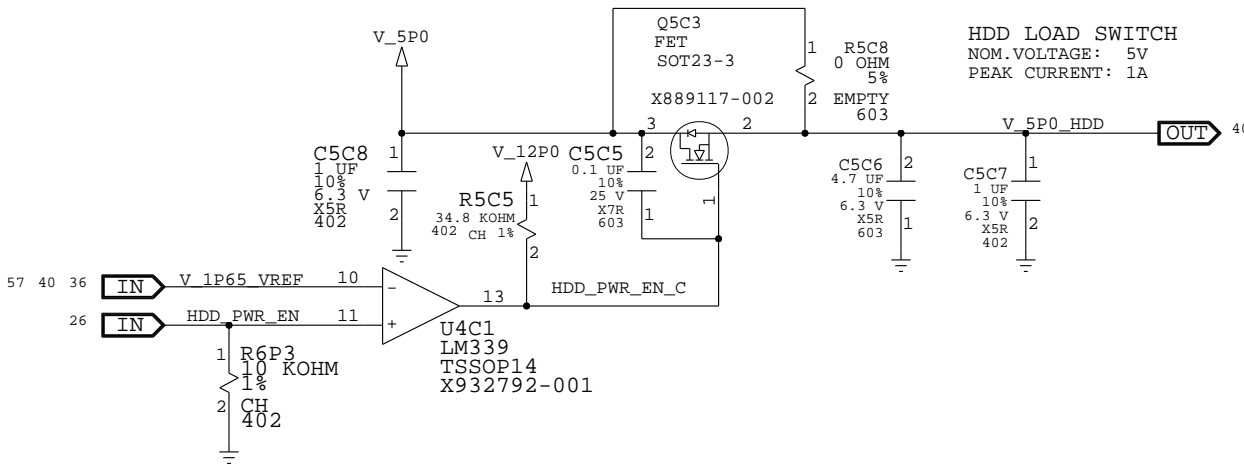
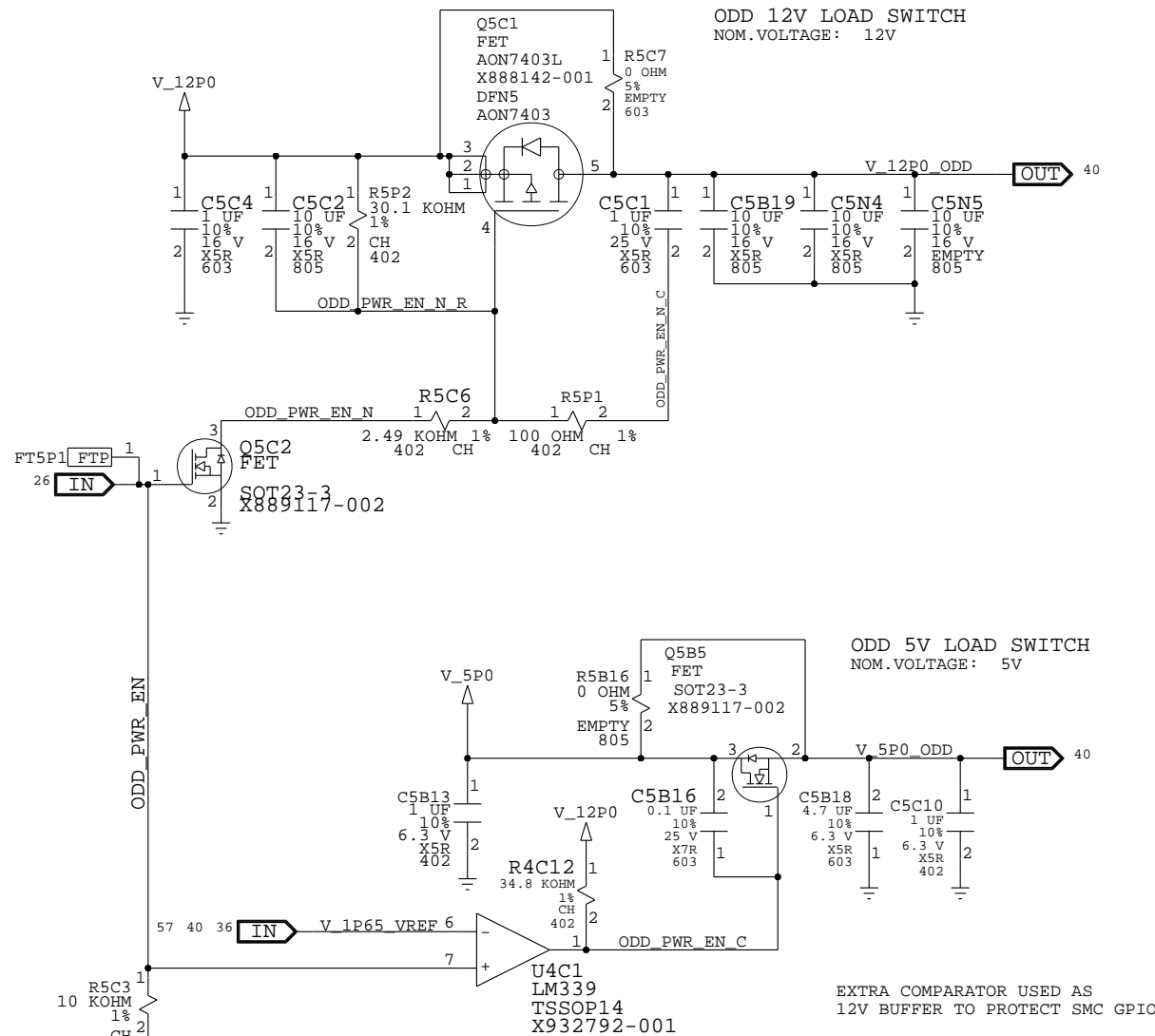
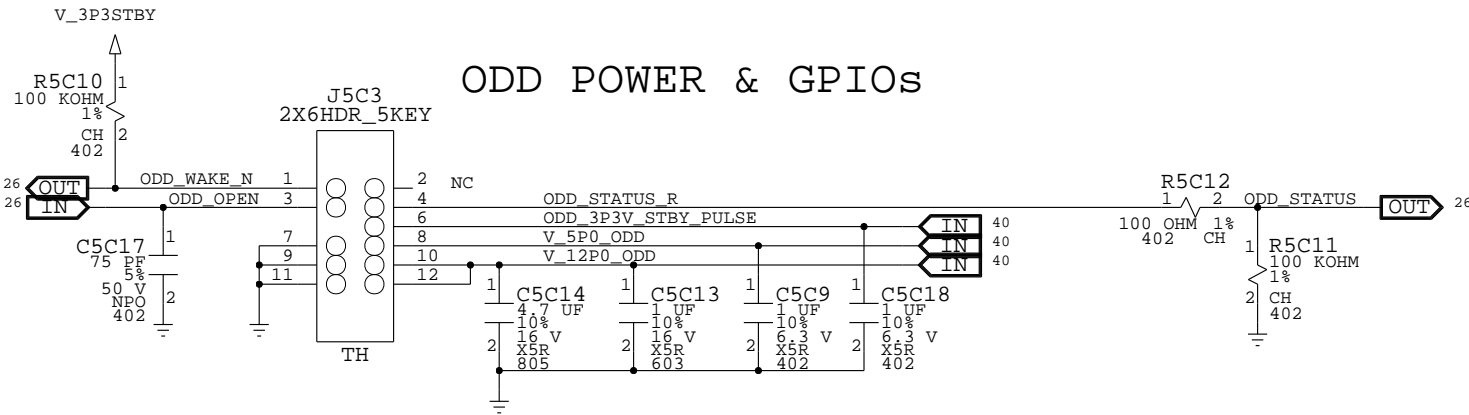
ODD SATA



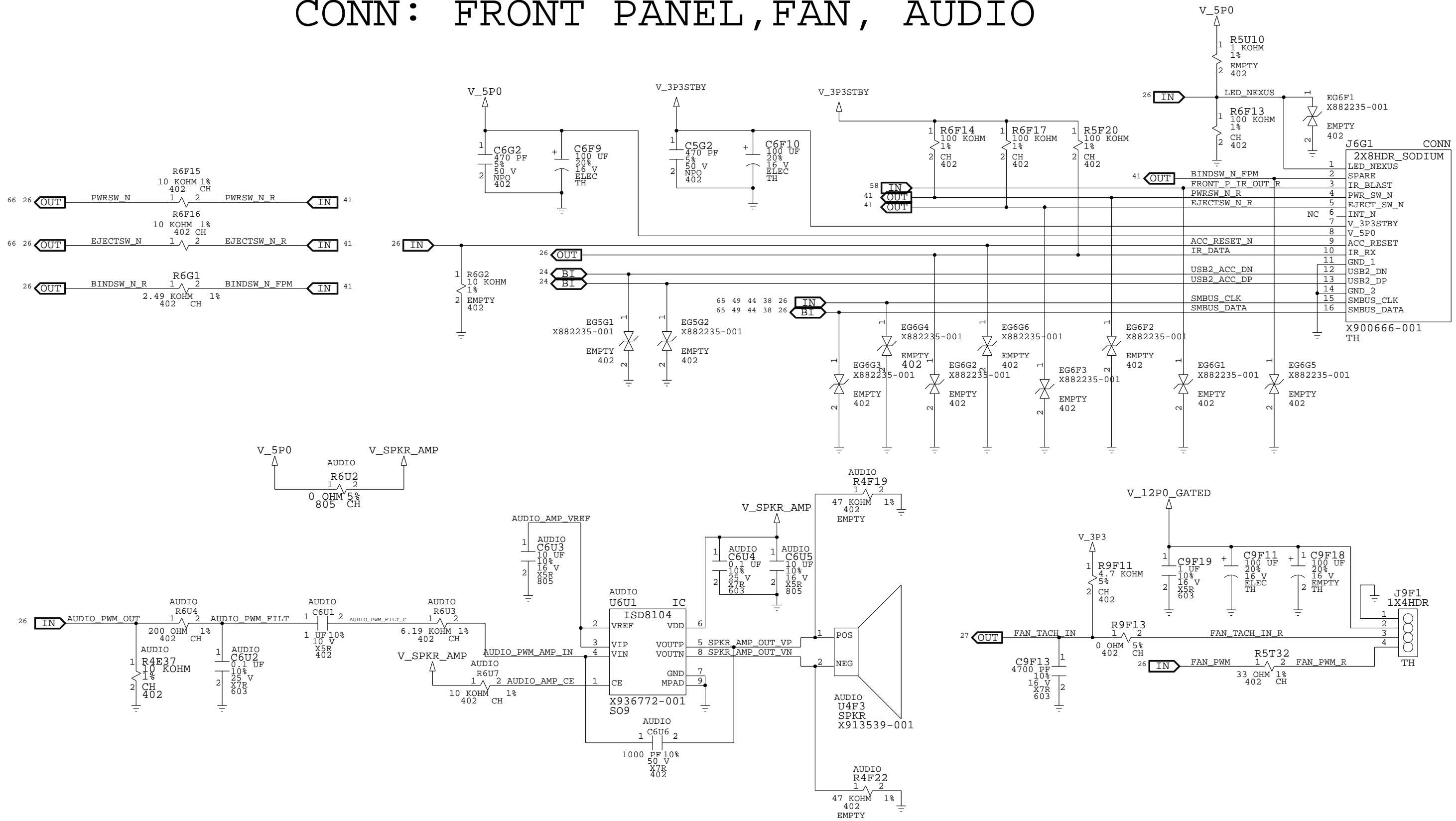
HDD POWER

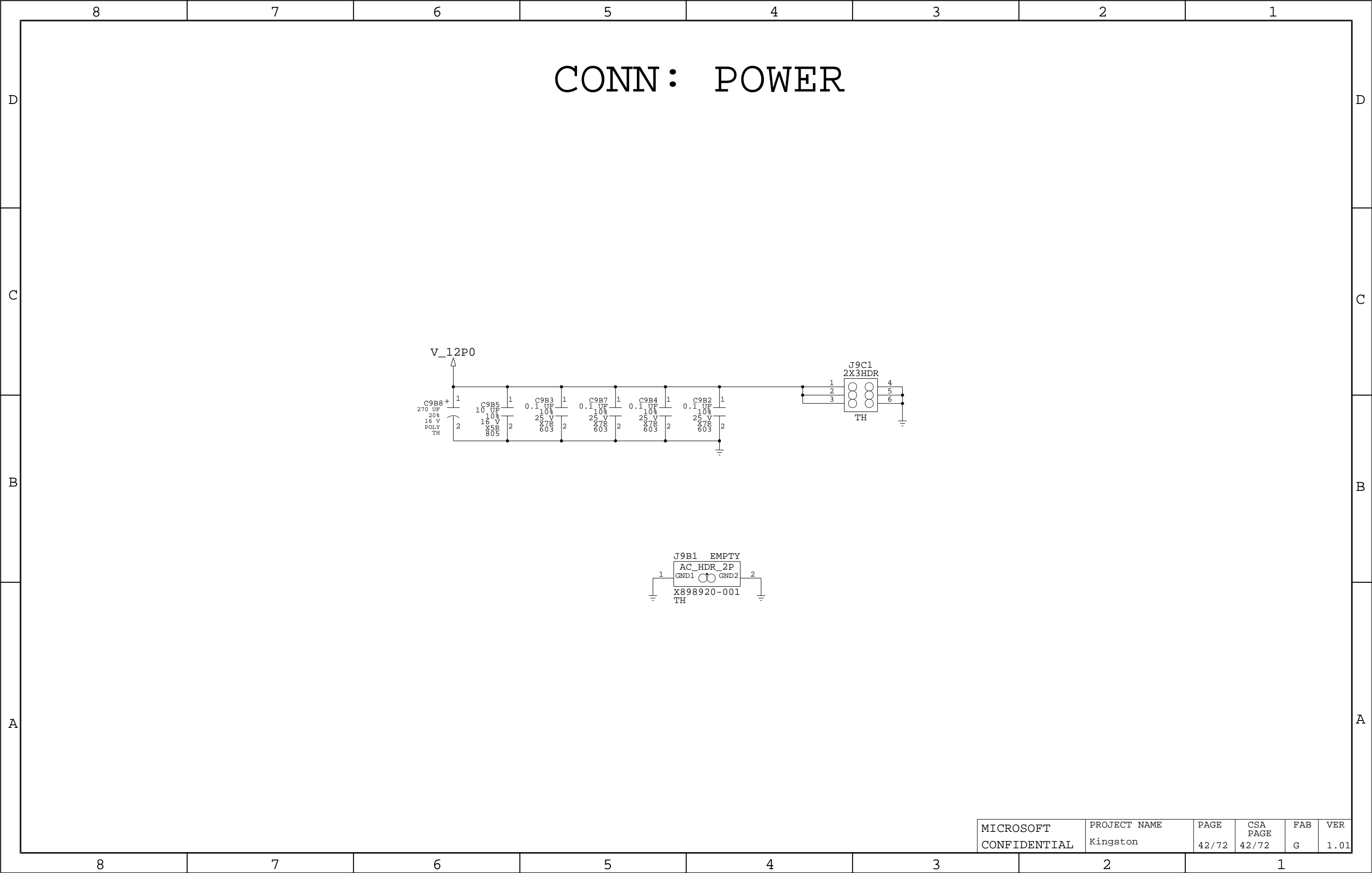


ODD POWER & GPIOs



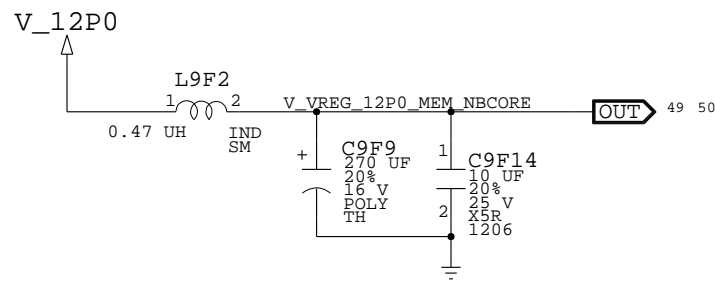
CONN: FRONT PANEL, FAN, AUDIO



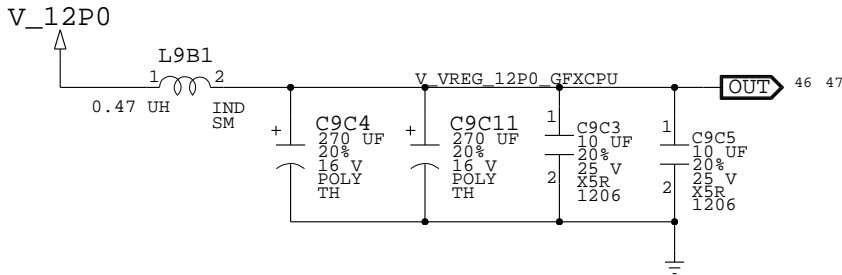


VREGS: INPUT & OUTPUT FILTERS

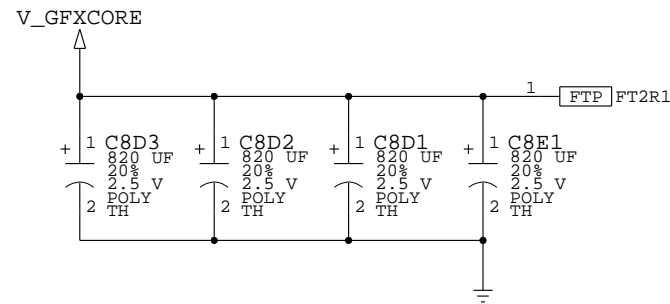
IO/NBCORE INPUT FILTER



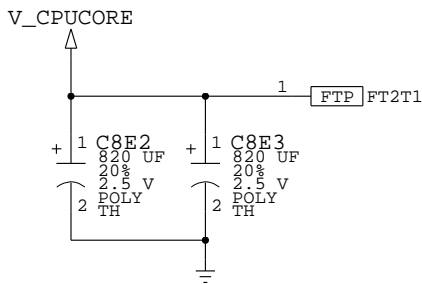
GFX/CPU INPUT FILTER



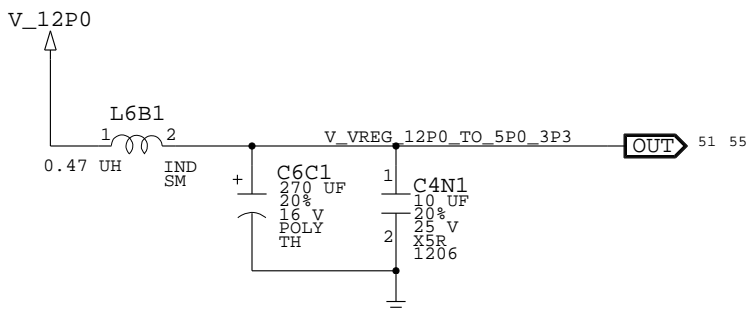
V_GFXCORE OUTPUT FILTER



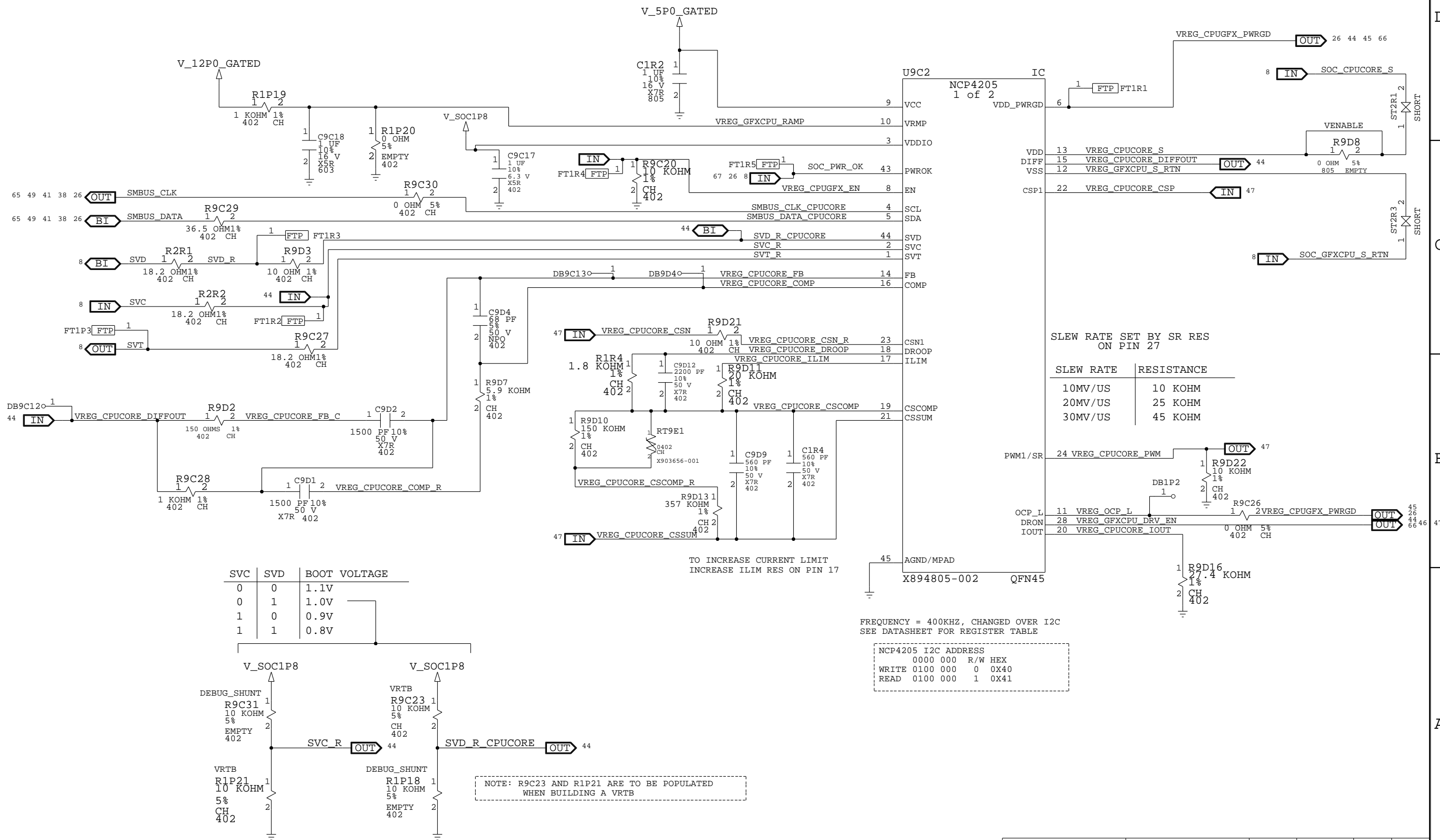
V_CPUCORE OUTPUT FILTER



V_5P0 AND V_3P3 INPUT FILTER

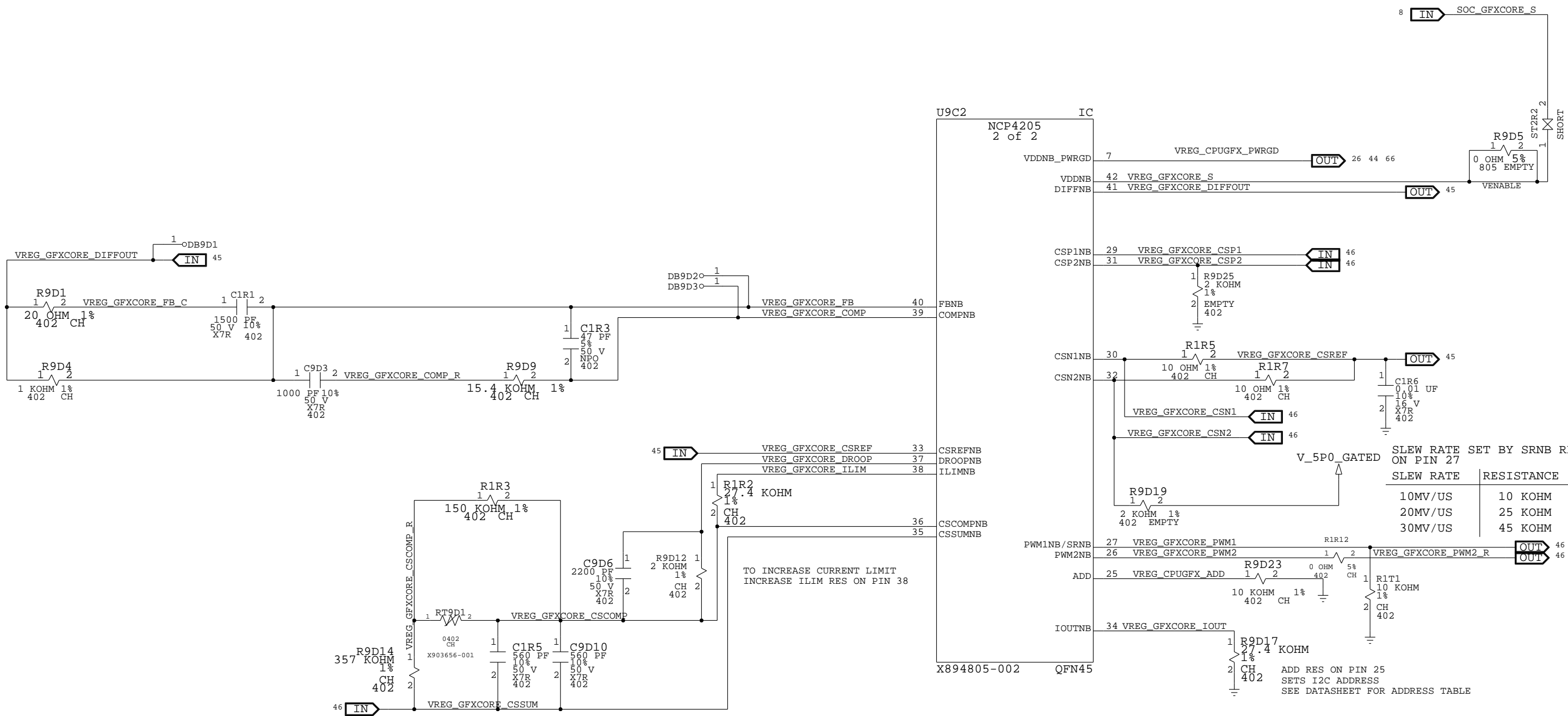


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VREGS:  CPUCORE
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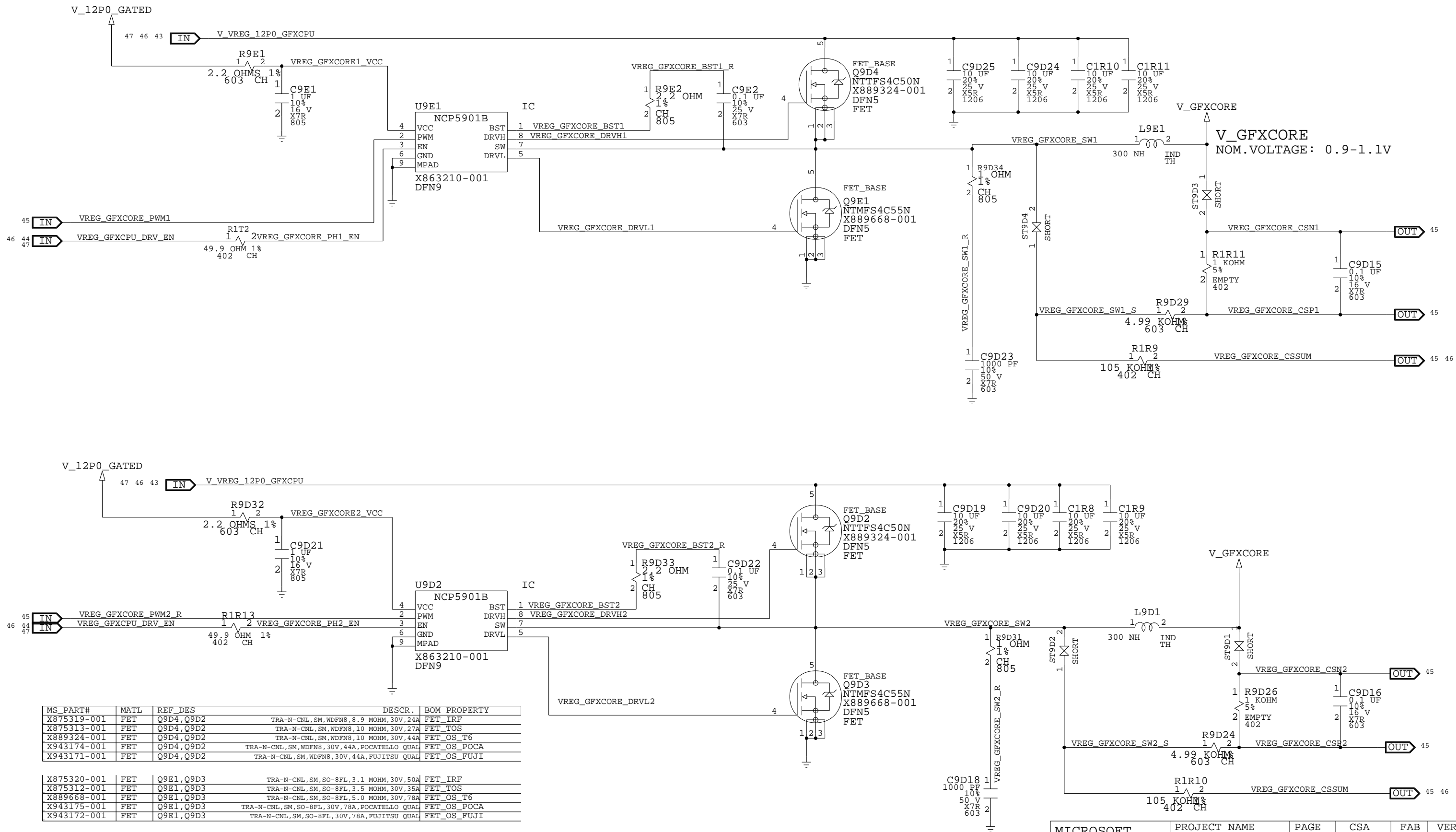


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| MICROSOFT | PROJECT NAME | PAGE | CSA PAGE | FAB | VER |
| CONFIDENTIAL | Kingston | 44/72 | 44/72 | G | 1.01 |

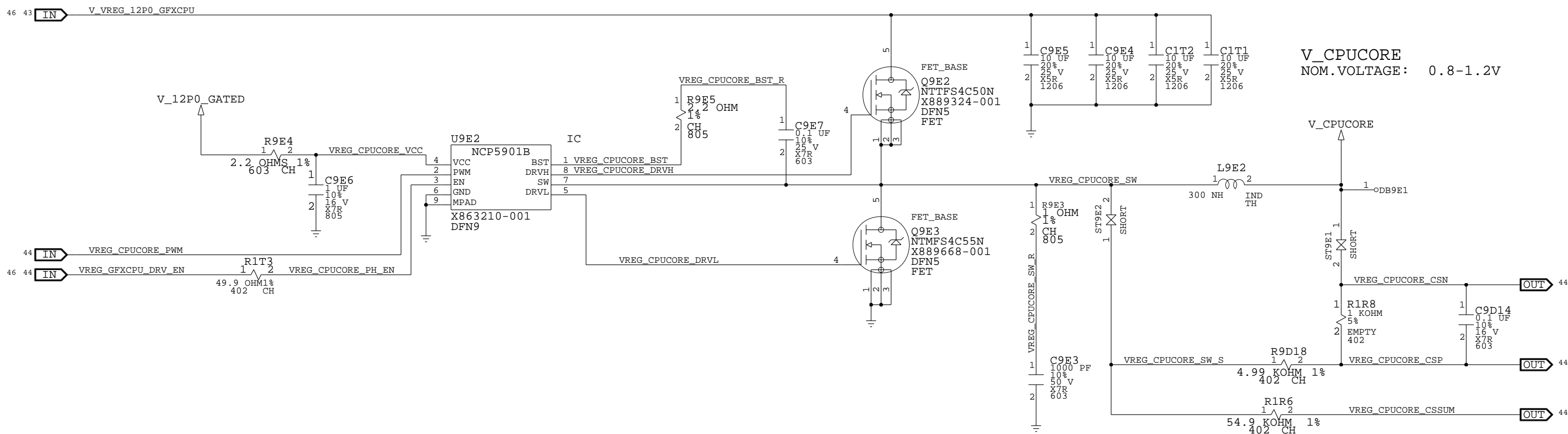
VREGS: GFXCORE



VREGS: GFXCORE OUTPUT PHASE 1 & 2



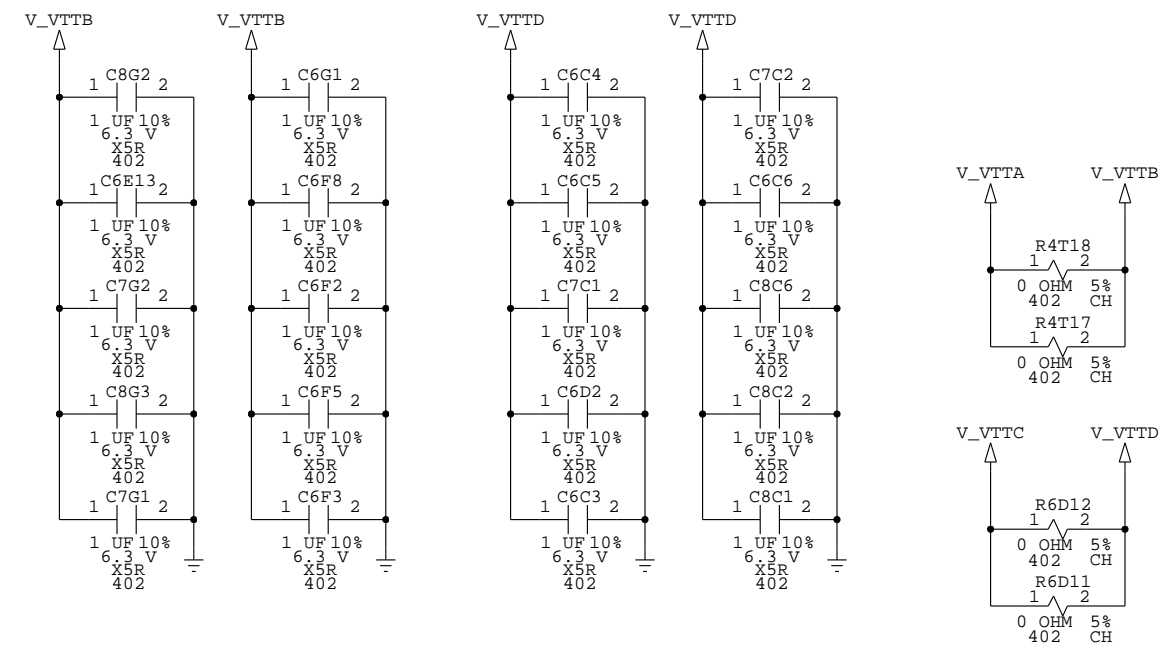
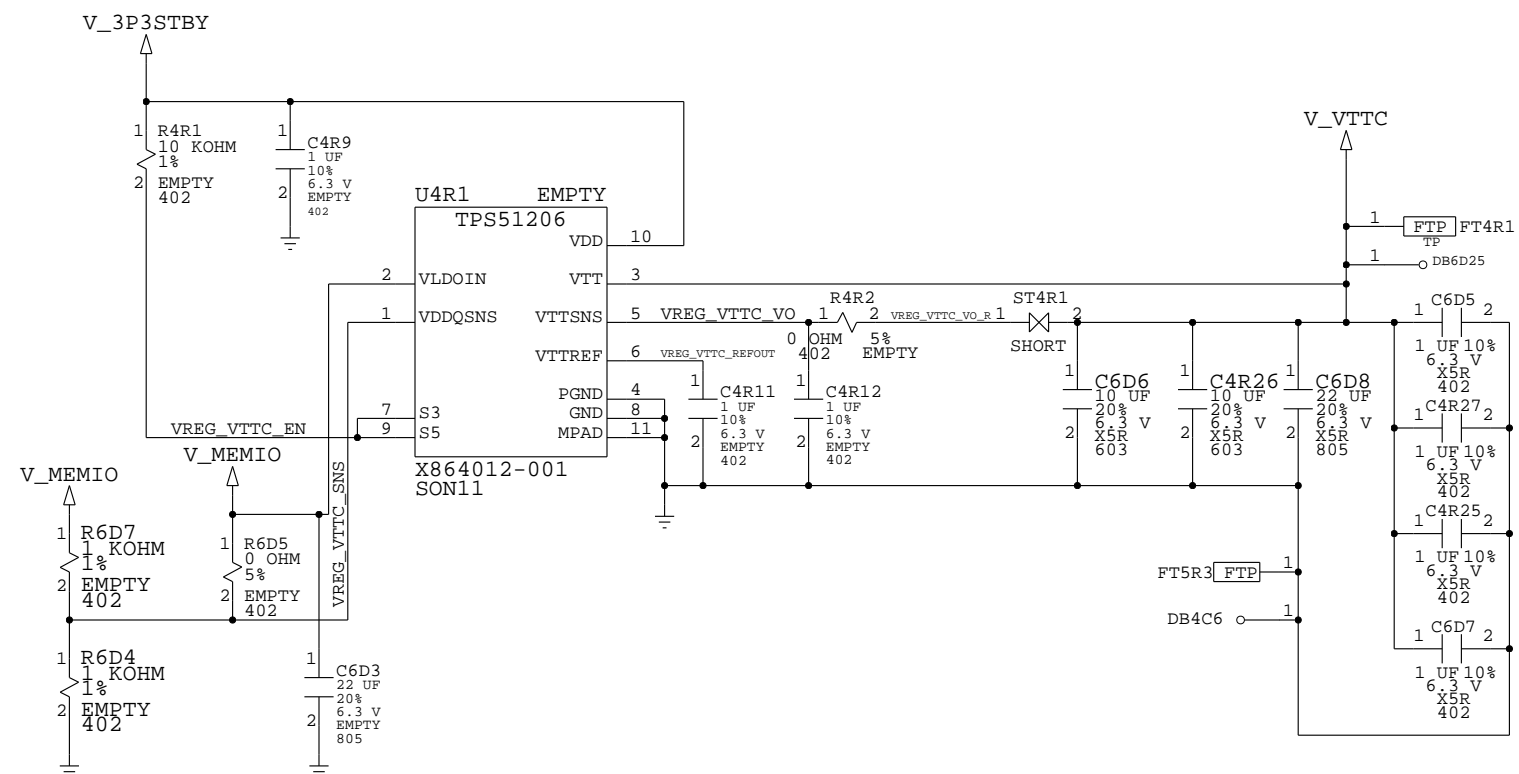
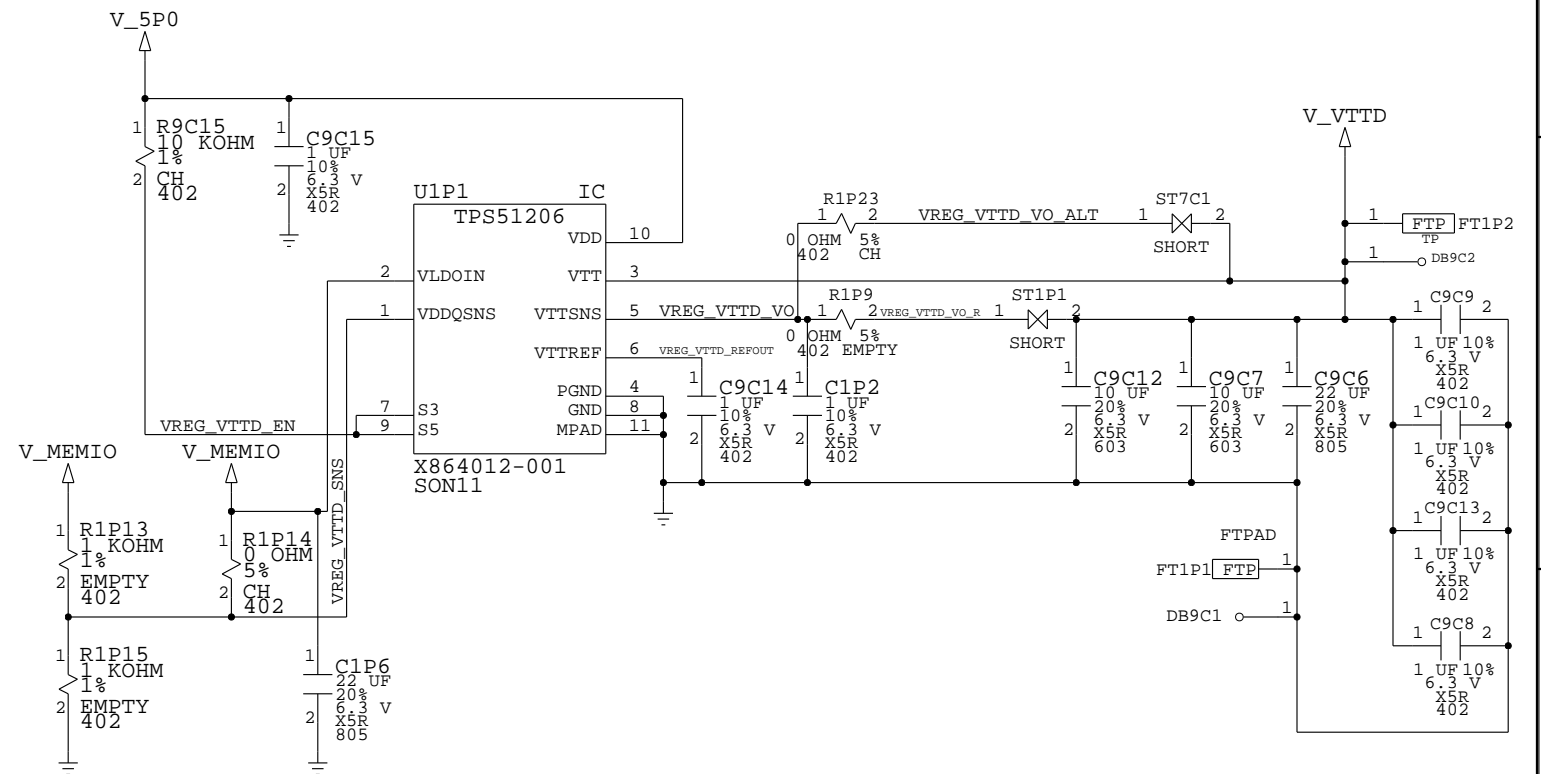
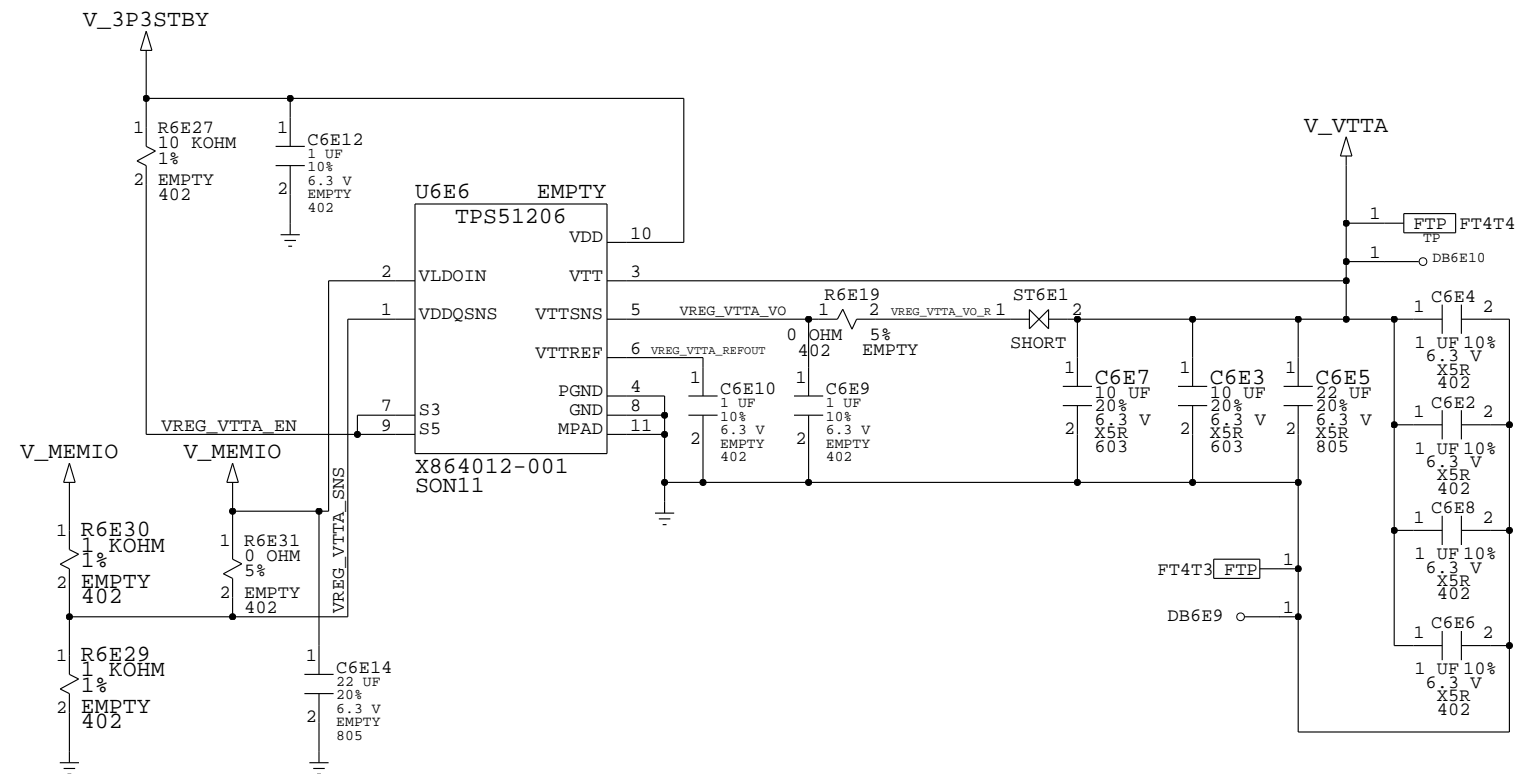
VREGS: CPUCORE OUTPUT PHASE



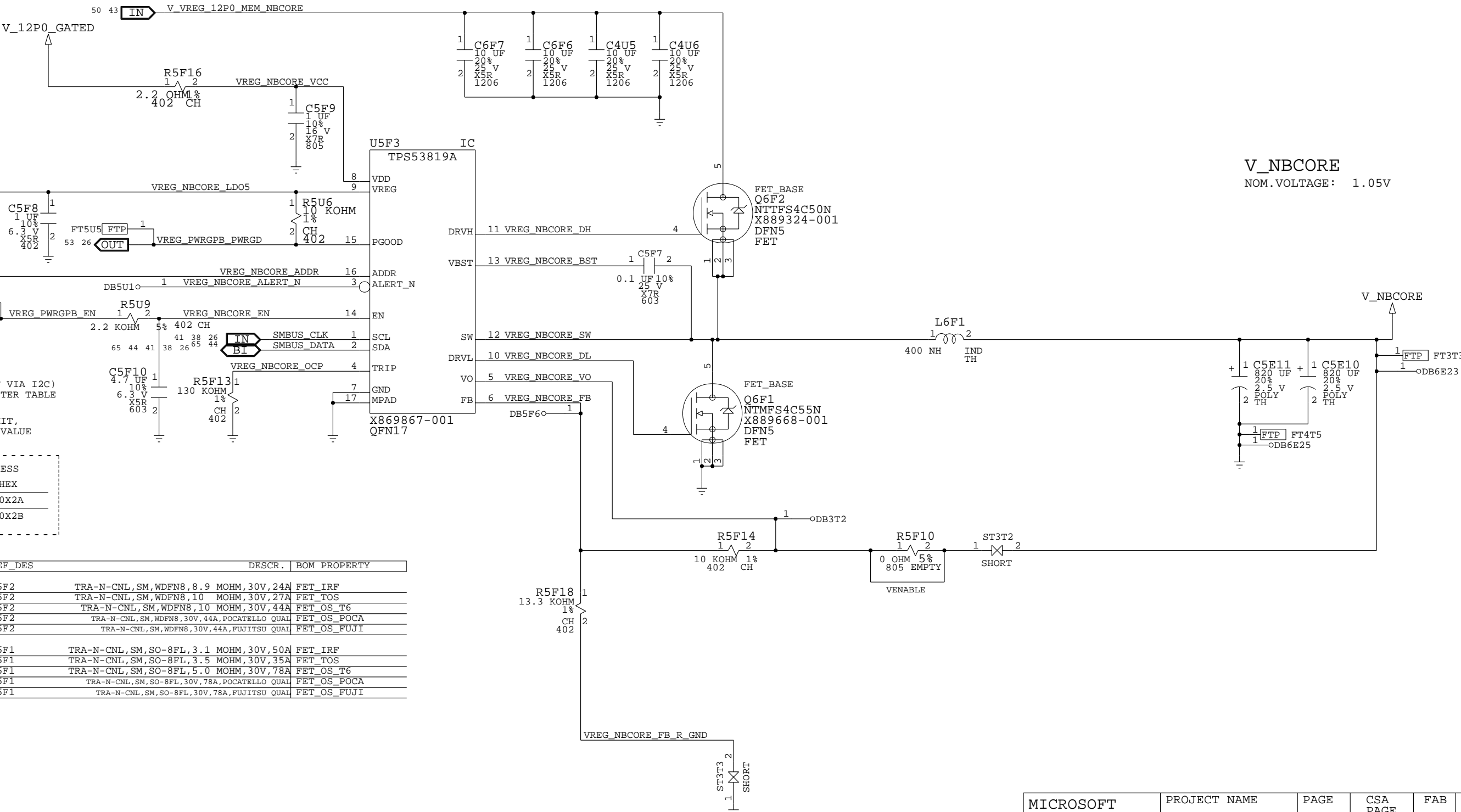
| MS_PART# | MATL | REF_DES | DESCR. | BOM_PROPERTY |
|-------------|------|---------|---|--------------|
| X875319-001 | FET | Q9E2 | TRA-N-CNL,SM,WDFN8,8.9 MOHM,30V,24A | FET_IRF |
| X875313-001 | FET | Q9E2 | TRA-N-CNL,SM,WDFN8,10 MOHM,30V,27A | FET_TOS |
| X889324-001 | FET | Q9E2 | TRA-N-CNL,SM,WDFN8,10 MOHM,30V,44A | FET_OS_T6 |
| X943174-001 | FET | Q9E2 | TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL | FET_OS_POCA |
| X943171-001 | FET | Q9E2 | TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL | FET_OS_FUJI |

| | | | | |
|-------------|-----|------|--|-------------|
| X875320-001 | FET | Q9E3 | TRA-N-CNL,SM,SO-8FL,3.1 MOHM,30V,50A | FET_IRF |
| X875312-001 | FET | Q9E3 | TRA-N-CNL,SM,SO-8FL,3.5 MOHM,30V,35A | FET_TOS |
| X889668-001 | FET | Q9E3 | TRA-N-CNL,SM,SO-8FL,5.0 MOHM,30V,78A | FET_OS_T6 |
| X943175-001 | FET | Q9E3 | TRA-N-CNL,SM,SO-8FL,30V,78A,POCATELLO QUAL | FET_OS_POCA |
| X943172-001 | FET | Q9E3 | TRA-N-CNL,SM,SO-8FL,30V,78A,FUJITSU QUAL | FET_OS_FUJI |

VREGS: VTT TERMINATION



VREGS: NBCORE

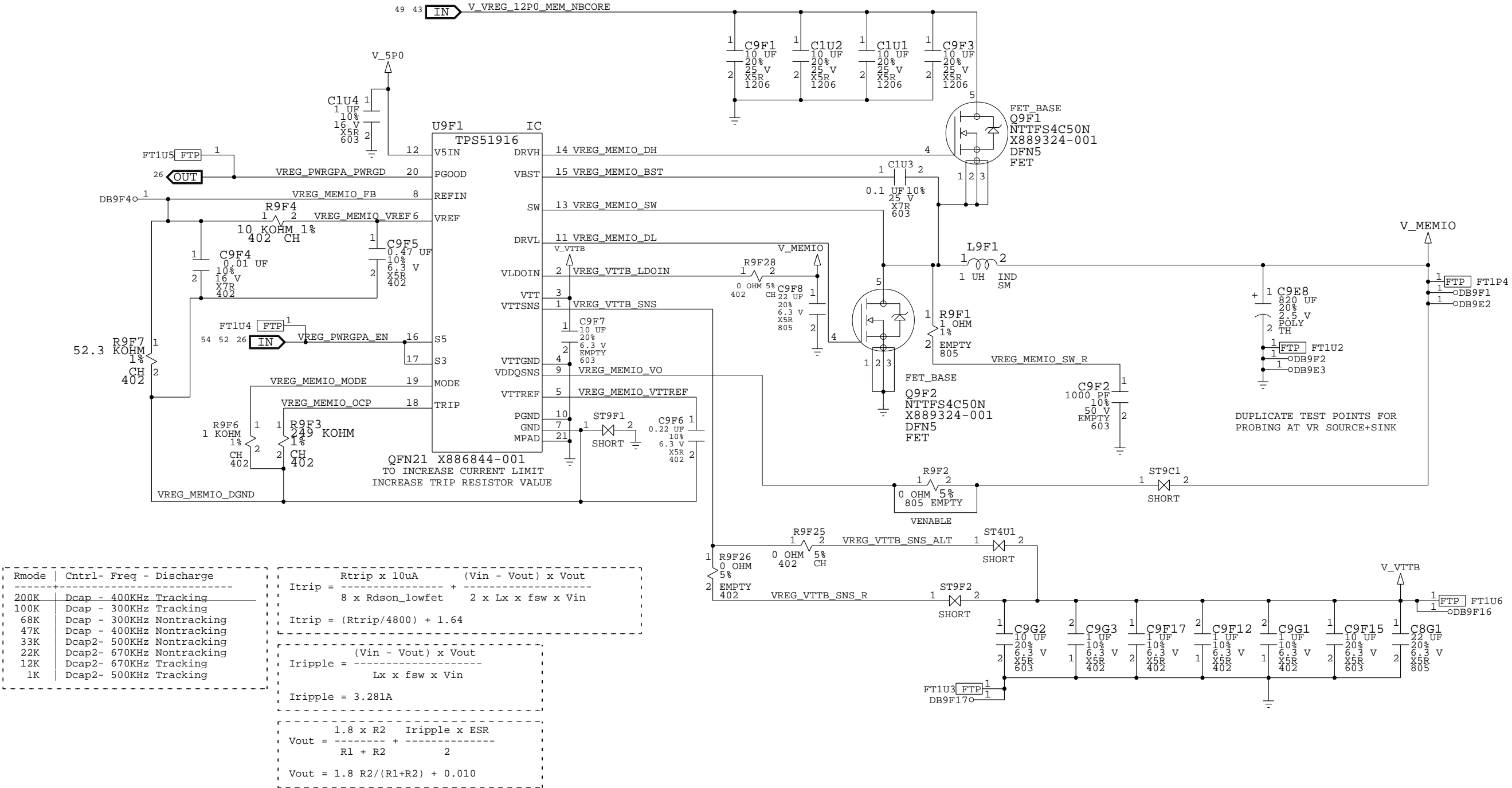


VREG: MEMIO

| MS_PART# | MATL | REF_DES | DESCR. | BOM PROPERTY |
|-------------|------|---------|---|--------------|
| X875319-001 | FET | Q9F1 | TRA-N-CNL,SM,WDFN8,8.9 MOHM,30 V,24 A | FET_IRF |
| X875313-001 | FET | Q9F1 | TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,27 A | FET_TOS |
| X889324-001 | FET | Q9F1 | TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,44 A | FET_OS_T6 |
| X943174-001 | FET | Q9F1 | TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL | FET_OS_POCA |
| X943171-001 | FET | Q9F1 | TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL | FET_OS_FUJI |
| X875319-001 | FET | Q9F2 | TRA-N-CNL,SM,WDFN8,8.9 MOHM,30 V,24 A | FET_IRF |
| X875313-001 | FET | Q9F2 | TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,27 A | FET_TOS |
| X889324-001 | FET | Q9F2 | TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,44 A | FET_OS_T6 |
| X943174-001 | FET | Q9F2 | TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL | FET_OS_POCA |
| X943171-001 | FET | Q9F2 | TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL | FET_OS_FUJI |

Q9F2 MATCHES Q9F1

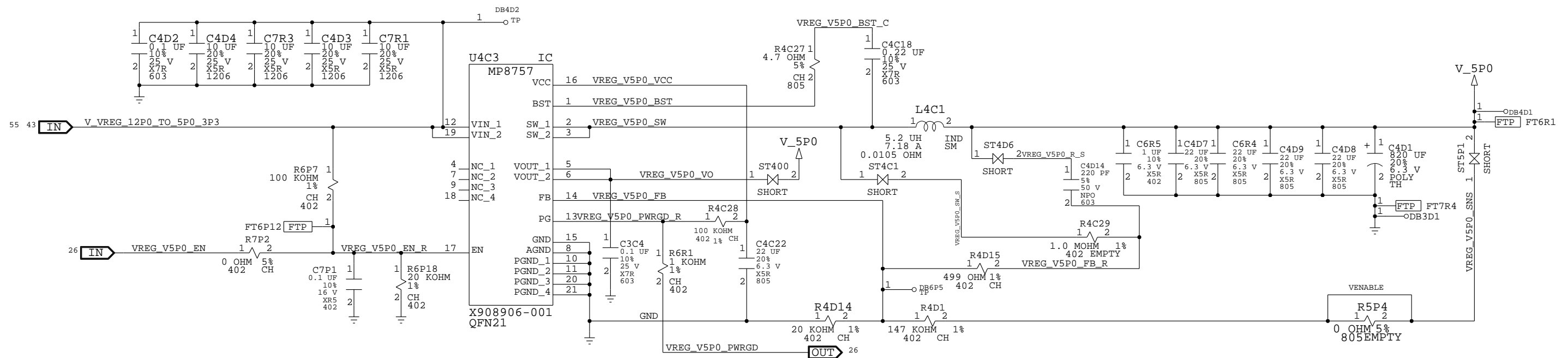
V_MEMIO
NOM. VOLTAGE: 1.50



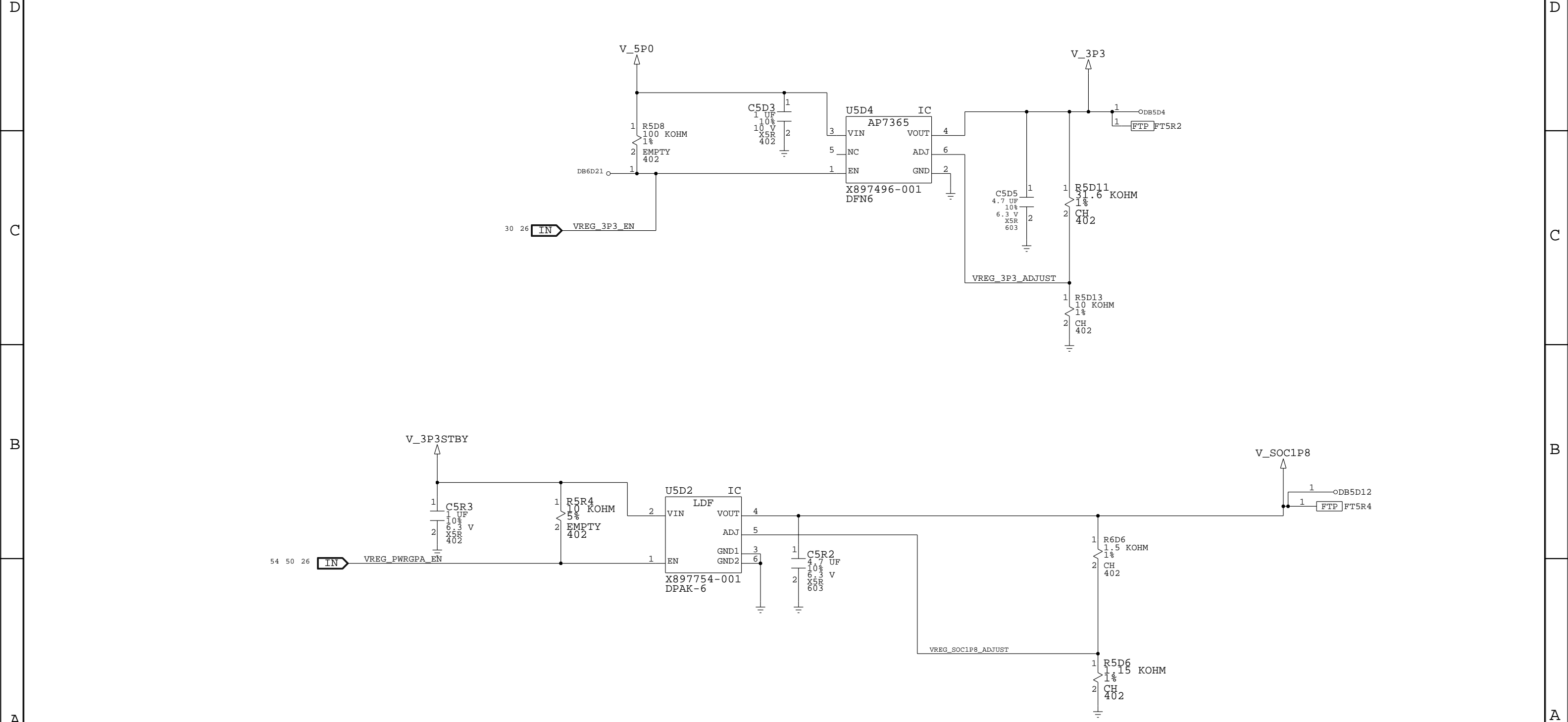
VREGS: V5P0

V_5P0

NOM. VOLTAGE: 5.09

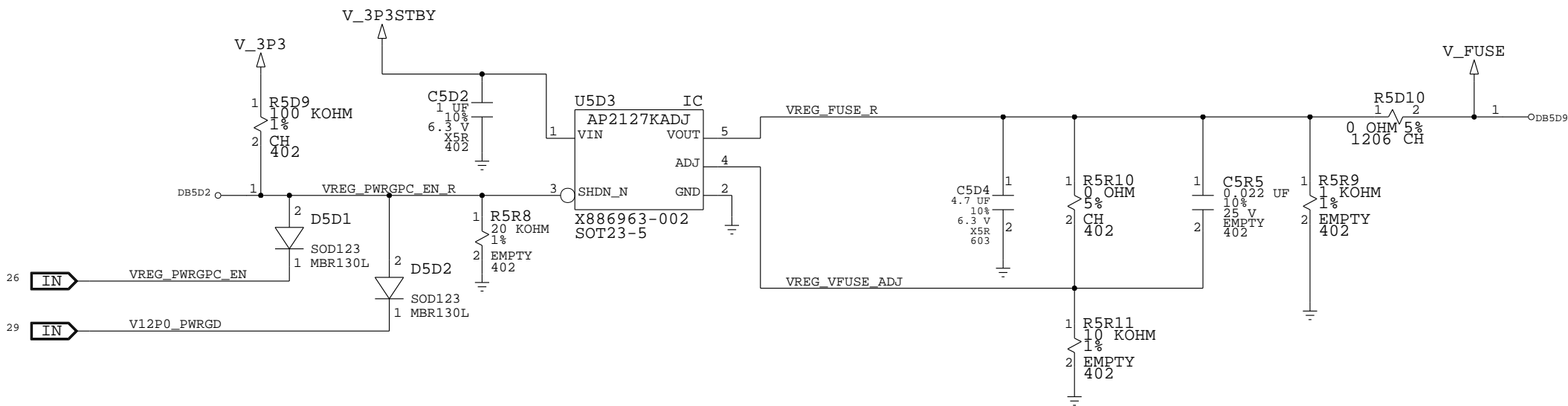
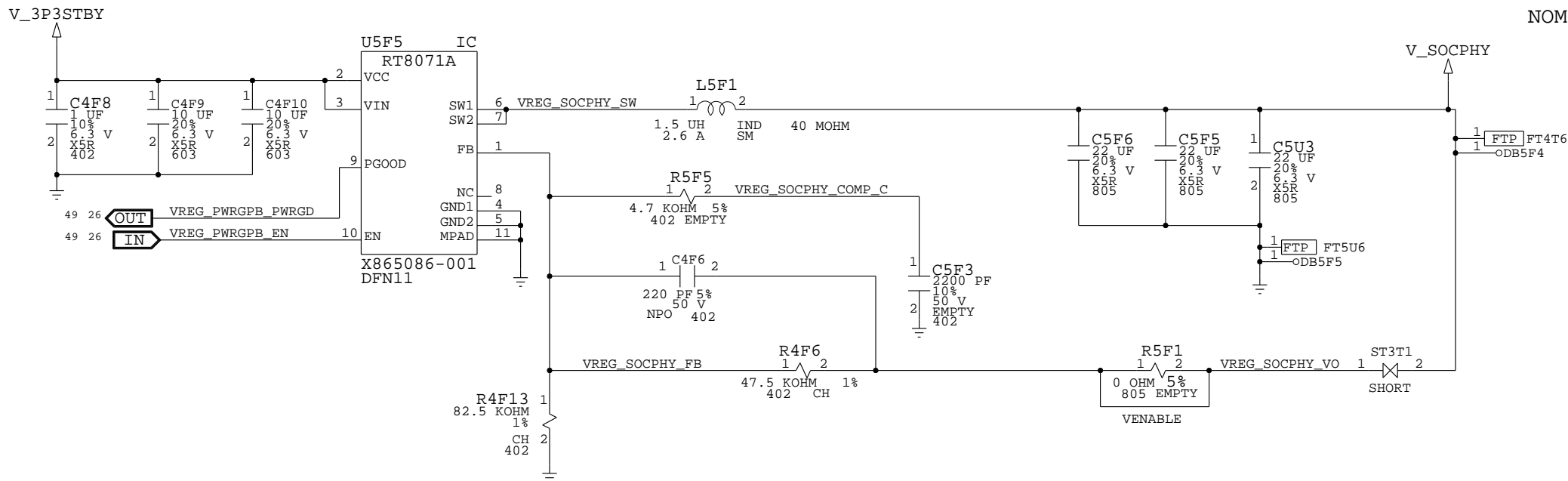


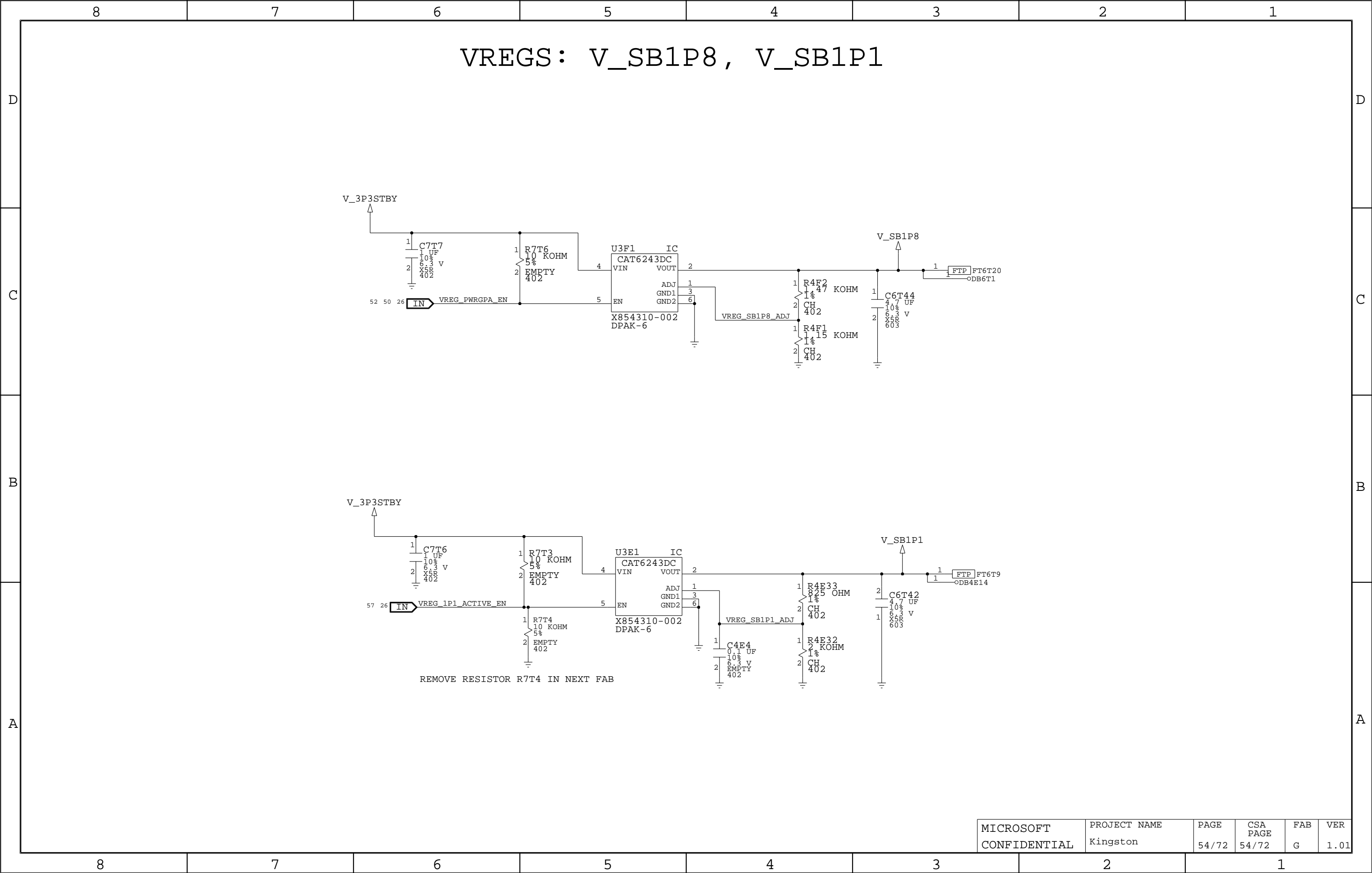
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VREGS: VSOCPHY/VFUSE

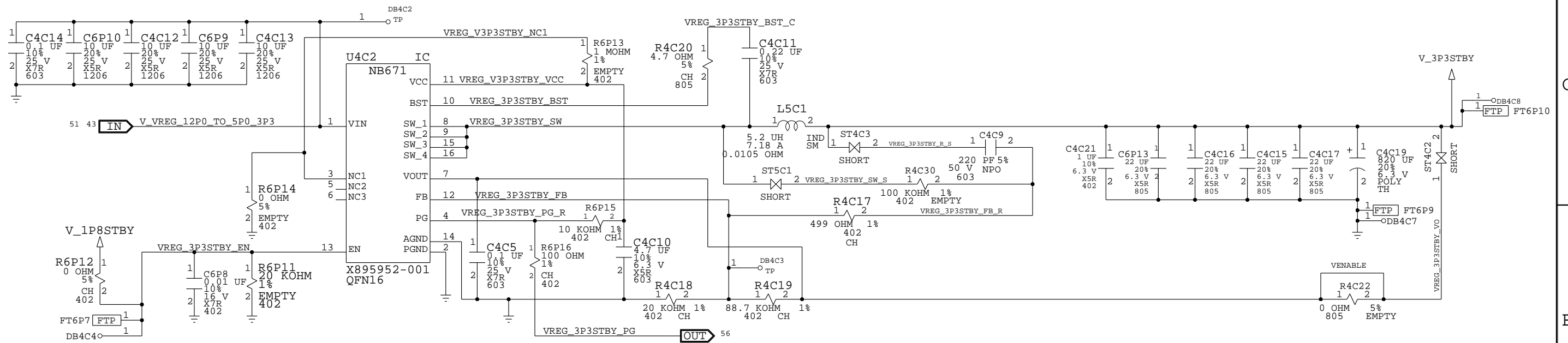
V_SOCPHY
NOM. VOLTAGE: 0.95





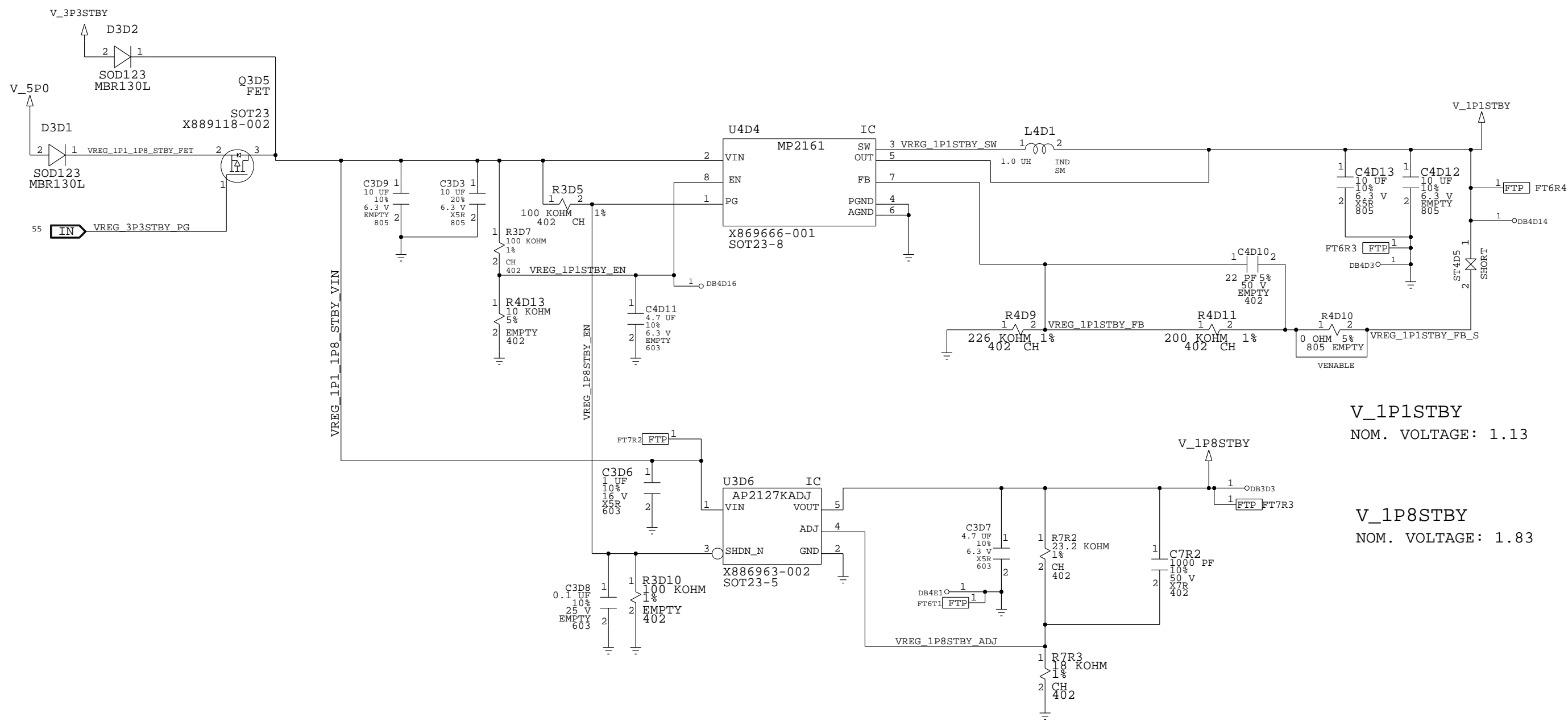
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VREGS:  V3P3  STANDBY
```

V_3P3STBY
NOM. VOLTAGE: 3.31



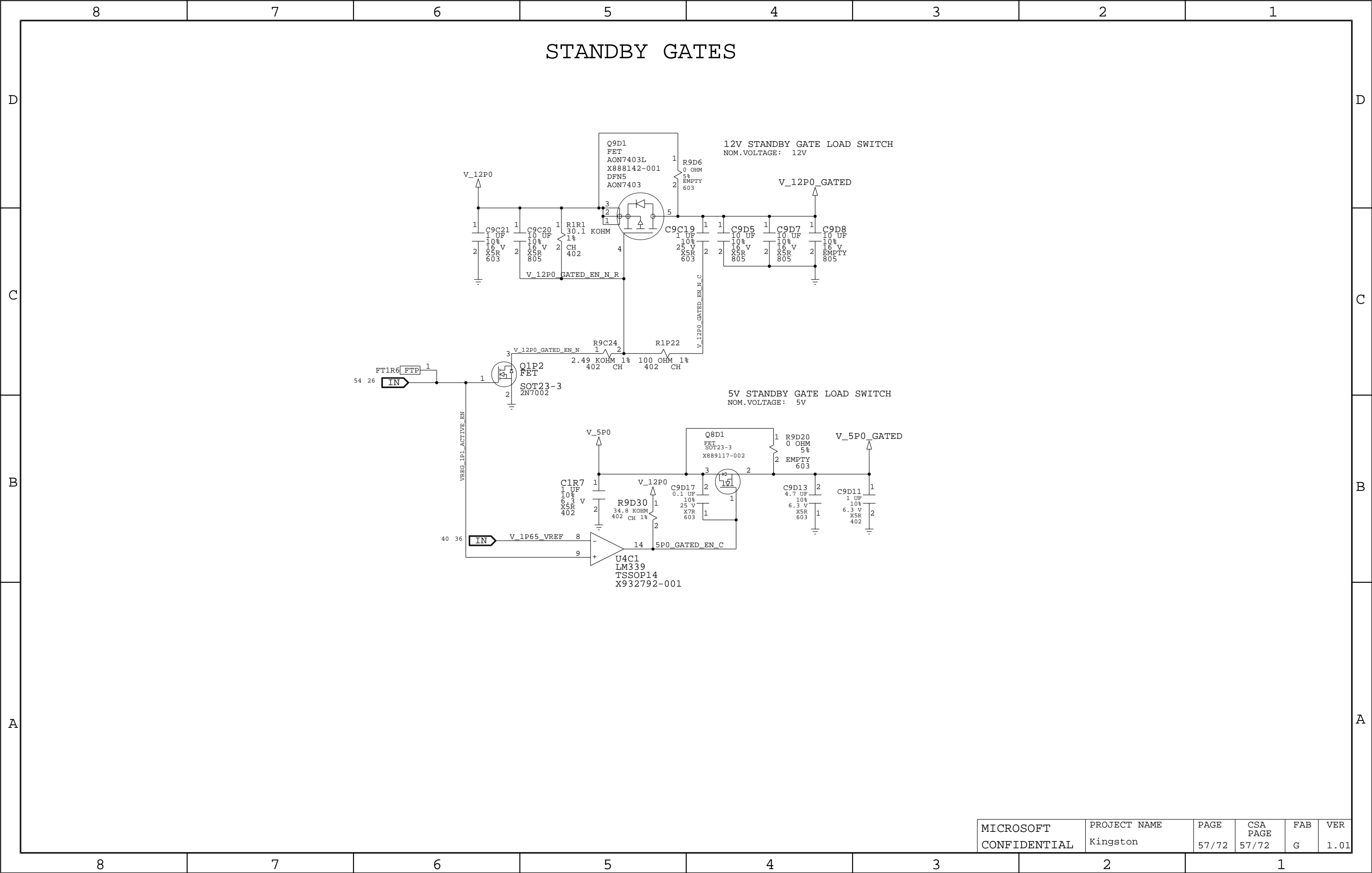
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VREGS: V1P1 STANDBY, V1P8 STANDBY

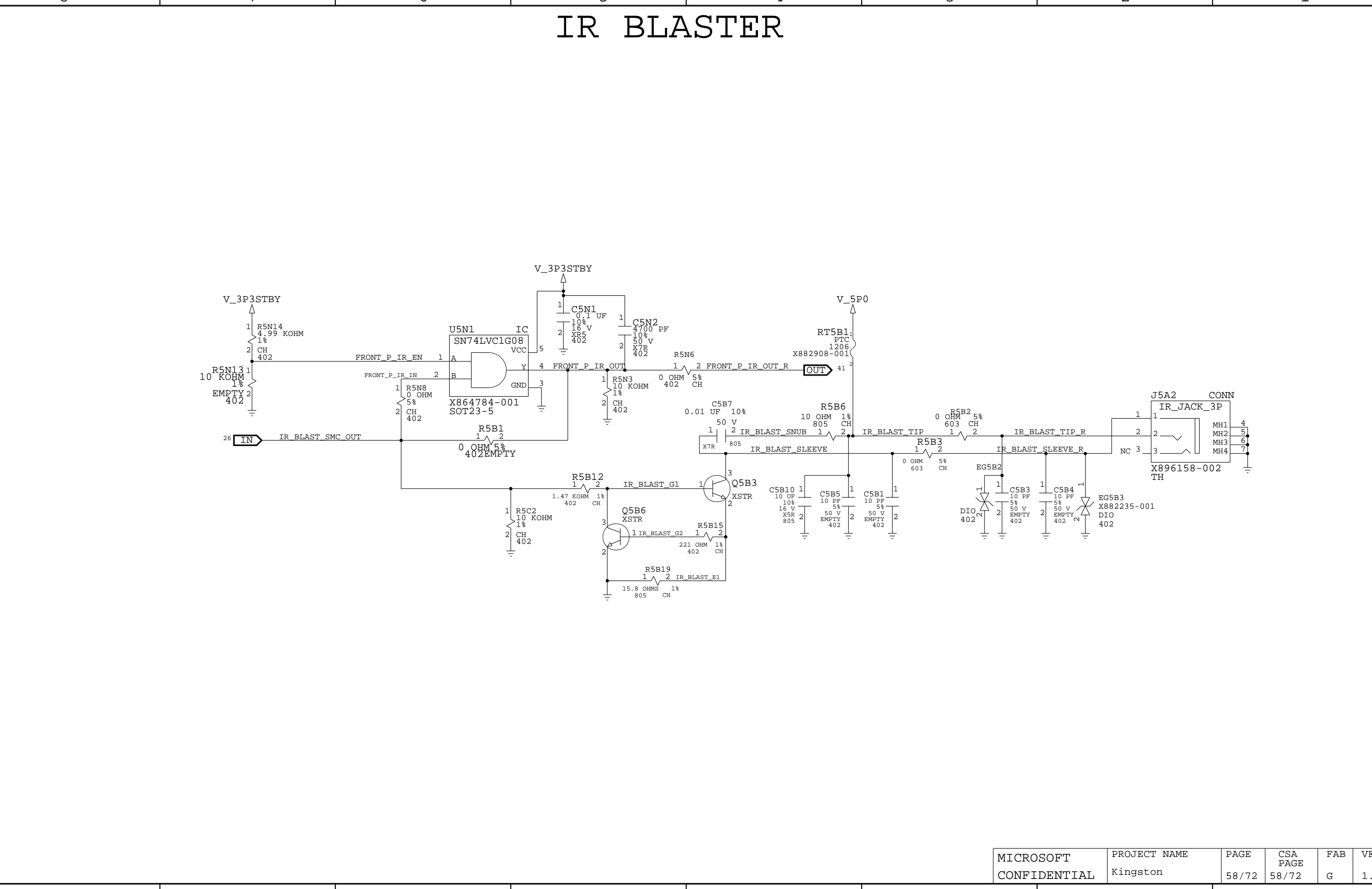


V_1P1STBY
NOM. VOLTAGE: 1.13

V_1P8STBY
NOM. VOLTAGE: 1.83

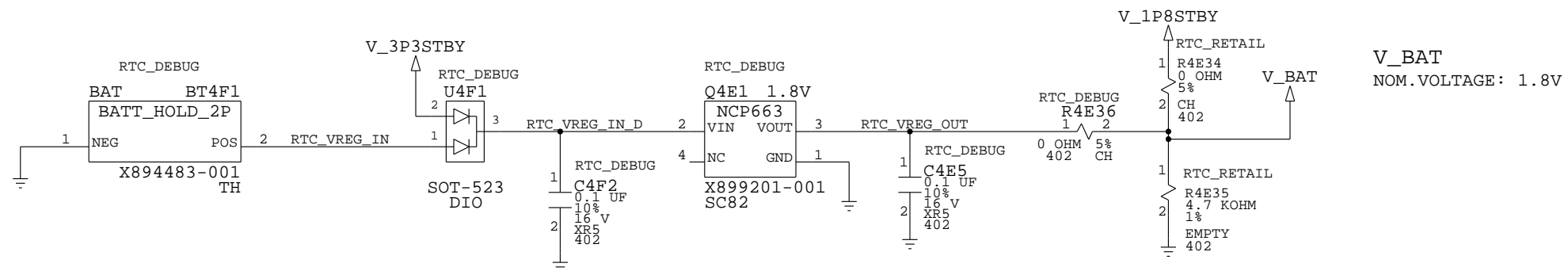


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| MARGIN: SOCPHY ,SOC1P8 ,MEMIO ,NBCORE | | | | | | | | | | | | | | | |
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V_BAT



| MS_PART# | MATL | REF_DES | DESCR. | BOM PROPERTY |
|-------------|------|------------|---|--------------|
| X895557-001 | BAT | COIN_CELL1 | BAT-COIN, OTH, 3 V, OTHER, OTH, 2032 (VARTA QUAL) | BAT VARTA |

VARTA MAXIMUM OPERATING TEMP 70C

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MONITOR: NBCORE, MEMIO

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MONITOR: VSOC1P8,VSOCPHY

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| 8 | | 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | |
| MONITOR: V12P0 | | | | | | | | | | | | | | | |
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| MICROSOFT CONFIDENTIAL | | PROJECT NAME Kingston | | PAGE 64/72 | | CSA PAGE 64/72 | | FAB G | | VER 1.01 | | | | | |

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| MICROSOFT CONFIDENTIAL | | PROJECT NAME Kingston | PAGE 64/72 | CSA PAGE 64/72 | FAB G | VER 1.01 |
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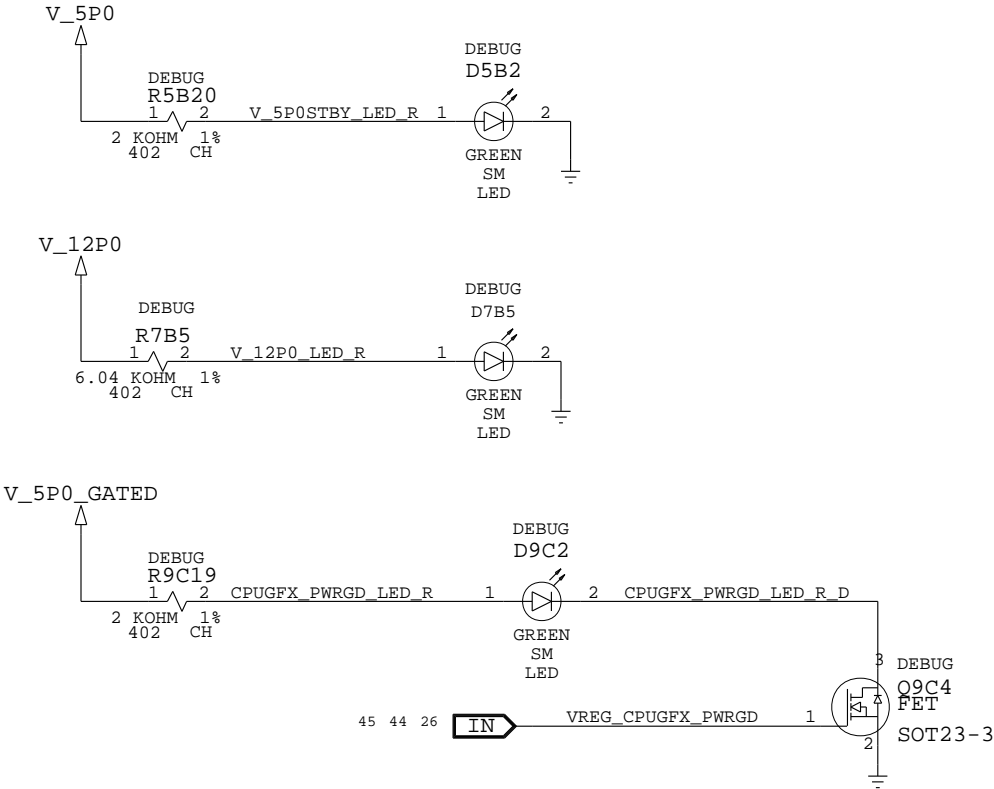
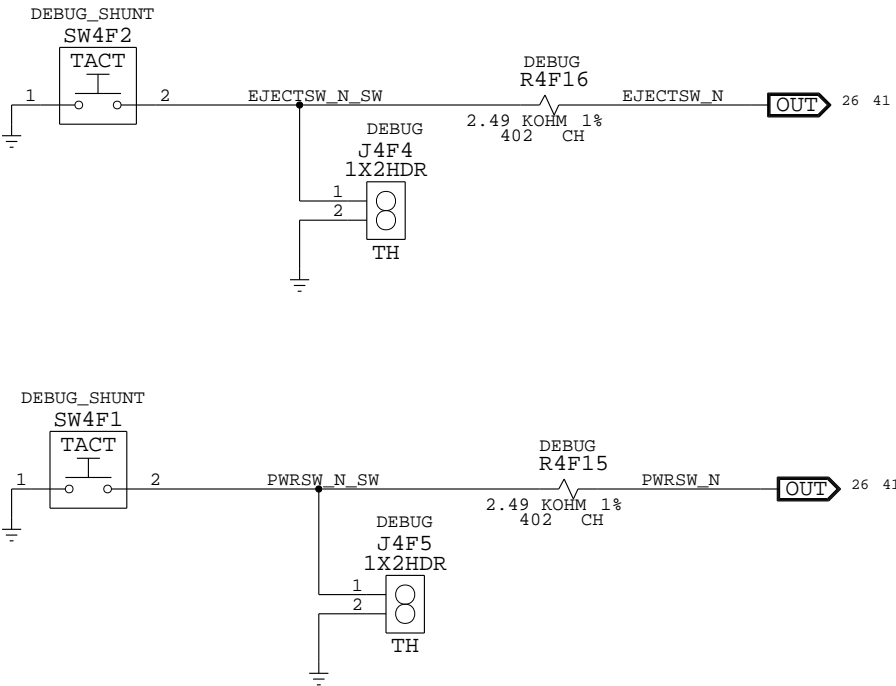
The schematic diagram illustrates the J4E1 2X13HDR connector and its associated signal lines. The connector is a 2x13 pin header with pins numbered 1 through 26. The signal lines are connected to various components and pins as follows:

- Pin 1:** SMC_RST_N (OUT) connected to R6T15 (100 OHM 1% CH) and R6T14 (0 OHM 5% CH).
- Pin 2:** SPI_MISO (IN) connected to R5T37 (33 OHM 1% CH) and R5T36 (33 OHM 1% CH).
- Pin 3:** SMC_DBG_LED0_SWO (IN) connected to R5T35 (0 OHM 5% CH).
- Pin 4:** KER_DBG_TXD (IN) connected to R5T34 (33 OHM 1% CH).
- Pin 5:** SMBUS_CLK (BI) connected to R5T33 (0 OHM 5% CH).
- Pin 6:** SMC_RST_N FACET (OUT) connected to R6T15.
- Pin 7:** SPI_MISO FACET (OUT) connected to R6T14.
- Pin 8:** SPI_SS_N (OUT) connected to R5T37.
- Pin 9:** SPI_CLK (OUT) connected to R5T36.
- Pin 10:** SB_TDI (OUT) connected to R5T35.
- Pin 11:** SB_TMS (OUT) connected to R5T34.
- Pin 12:** SB_TCK (OUT) connected to R5T33.
- Pin 13:** SMC_DBG_LED0_SWO FACET (OUT) connected to R5T35.
- Pin 14:** KER_DBG_TXD FACET (OUT) connected to R5T34.
- Pin 15:** KER_DBG_RXD (OUT) connected to R5T33.
- Pin 16:** FTDI_SMC_TXD FACET (OUT) connected to R5T34.
- Pin 17:** FTDI_SMC_RXD FACET (OUT) connected to R5T33.
- Pin 18:** SMBUS_CLK FACET (BI) connected to R5T33.
- Pin 19:** SMC_DBG_LED0_SWO (IN) connected to R5T37.
- Pin 20:** SPI_MISO (IN) connected to R5T36.
- Pin 21:** SPI_SS_N (IN) connected to R5T37.
- Pin 22:** SPI_CLK (IN) connected to R5T36.
- Pin 23:** SB_TDI (IN) connected to R5T35.
- Pin 24:** SB_TMS (IN) connected to R5T34.
- Pin 25:** SB_TCK (IN) connected to R5T33.
- Pin 26:** SMC_RST_N (OUT) connected to R6T15.

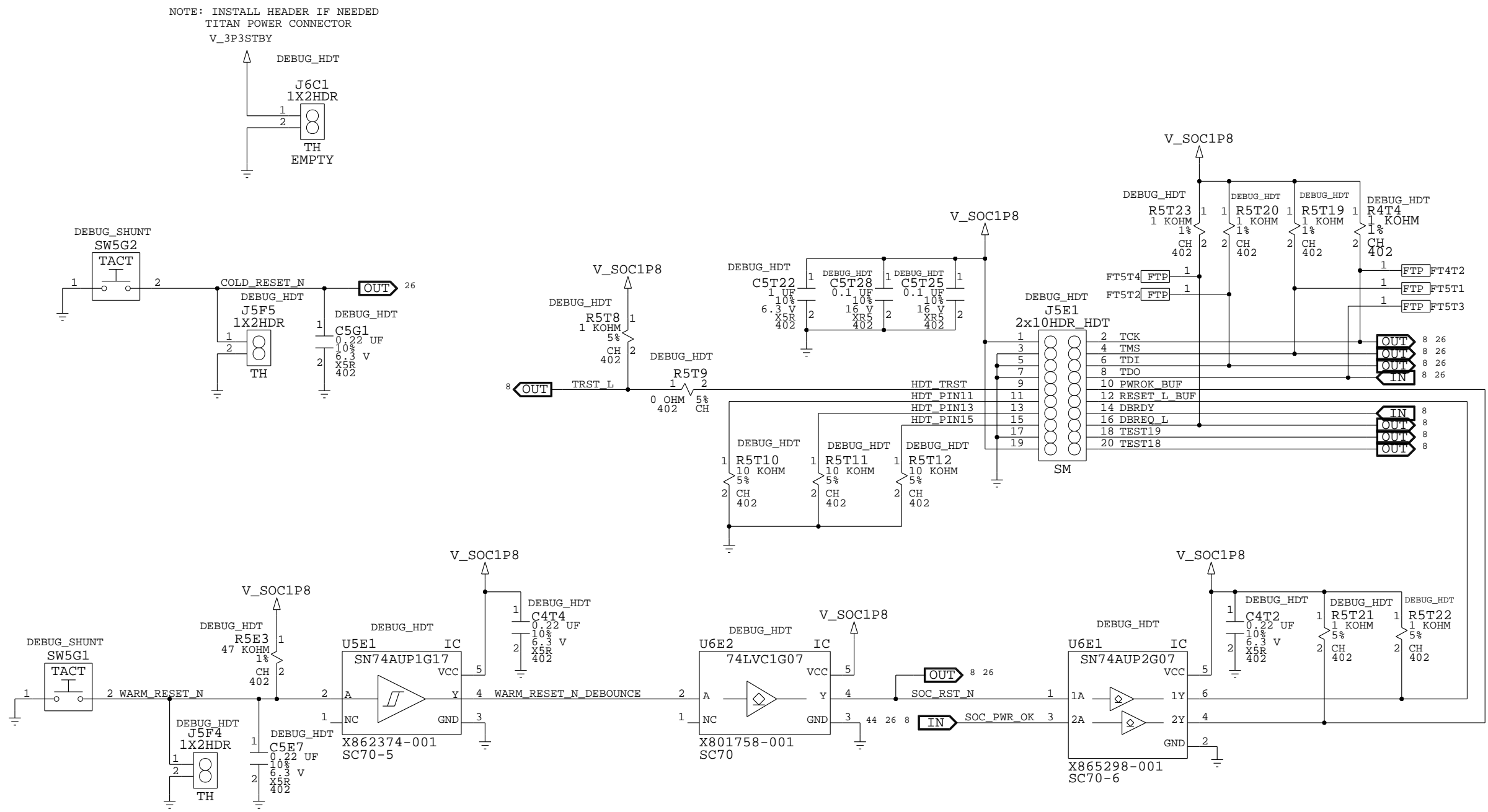
Additional components and connections include:

- DEBUG_FACET:** A 100 OHM 1% CH resistor connected to pins 1 and 2.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 3 and 4.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 5 and 6.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 7 and 8.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 9 and 10.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 11 and 12.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 13 and 14.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 15 and 16.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 17 and 18.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 19 and 20.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 21 and 22.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 23 and 24.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 25 and 26.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 27 and 28.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 29 and 30.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 31 and 32.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 33 and 34.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 35 and 36.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 37 and 38.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 39 and 40.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 41 and 42.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 43 and 44.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 45 and 46.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 47 and 48.
- DEBUG_FACET:** A 33 OHM 1% CH resistor connected to pins 49 and 50.

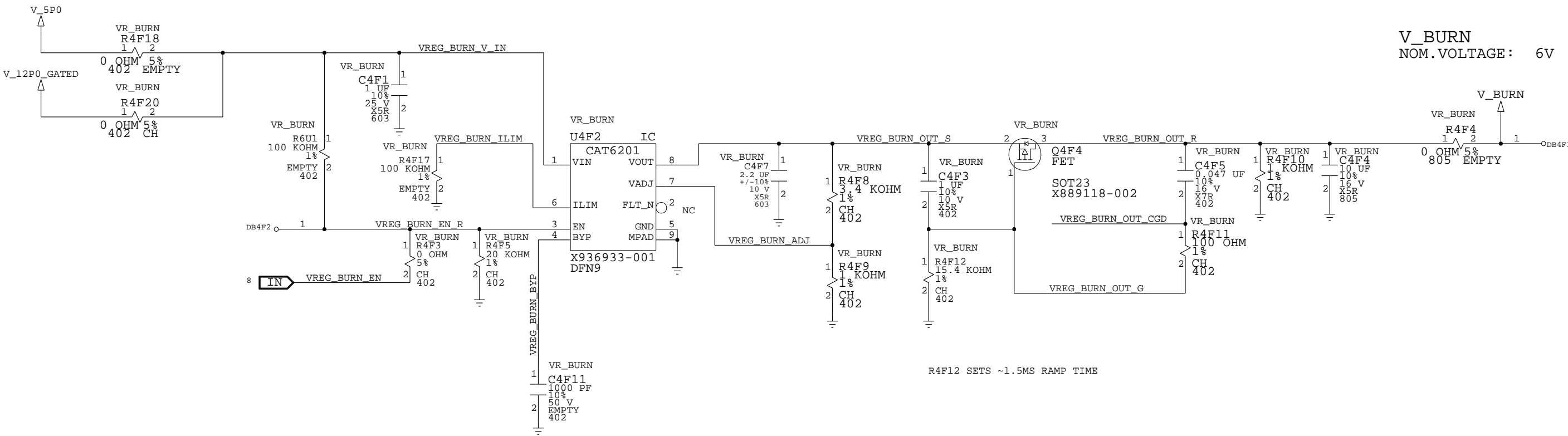
CONN: SWITCHES

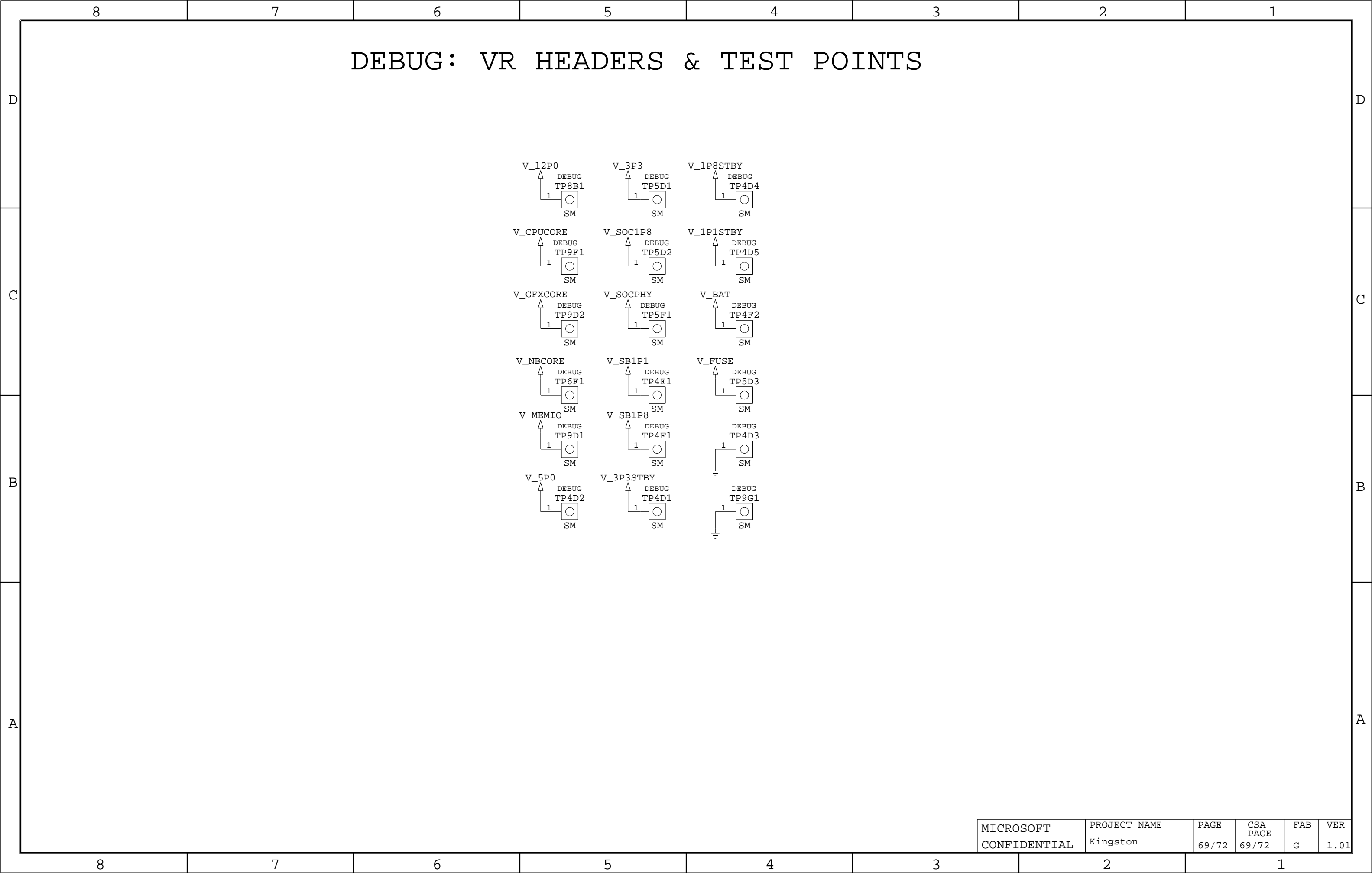


CONN: HDT



DEBUG: V_BURN





V_NBCORE

DEBUG

TP6F1

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SM

V_SB1P1

DEBUG

TP4E1

1

SM

V_FUSE

DEBUG

TP5D3

1

SM

V_MEMIO

DEBUG

TP9D1

1

SM

V_SB1P8

DEBUG

TP4F1

1

SM

DEBUG

TP4D3

1

SM

V_5P0

DEBUG

TP4D2

1

SM

V_3P3STBY

DEBUG

TP4D1

1

SM

DEBUG

TP9G1

1

SM

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| DEBUG : CONNECTORS | | | | | | | | | | | | | | | |
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8 7 6 5 4 3 2 1

LABELS AND MOUNTING

HEAT SINK MOUNTING HOLES

STD
MTG8D1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG8E1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG7E1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG7D1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

SCREW BOSS

J3C3 CONN
SCREW_BOSS_3P
NC 1 1
2 2
3 3
X900629-001
TH

J4G1 CONN
SCREW_BOSS_3P
NC 1 1
2 2
3 3
X900629-001
TH

MTG3P1
MTG_HOLE
PTH 1
EMPTY

MTG4R1
MTG_HOLE
PTH 1
EMPTY

INTELLIGENT SERIAL NUMBER TARGET

LB5G1
X801181-001
LABEL
1
1375X250_TARGET

| MS_PART# | MATL | REF_DES | DESCR. | BOM PROPERTY |
|-------------|------|---------|-----------------------------------|--------------|
| X947889-001 | FR4 | PCB1 | PCB-RIGID,RETAIL,FAB G,6L,FR4,OSP | PCB_OSP |

| MICROSOFT | PROJECT NAME | PAGE | CSA | FAB | VER |
|--------------|--------------|-------|---------------|-----|------|
| CONFIDENTIAL | Kingston | 71/72 | PAGE 71/72 | G | 1.01 |

| MS_PART# | MATL | REF_DES | DESCR. | BOM PROPERTY |
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| X947889-001 | FR4 | PCB1 | PCB-RIGID,RETAIL,FAB G,6L,FR4,OSP | PCB_OSP |

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| CONFIDENTIAL | Kingston | 71/72 | 71/72 | G | 1.01 |

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| C | AUX | HDMI STUFFING OPTION. NEVER USED IN PRODUCTION. REWORK PURPOSES ONLY | | | | | | | | | | | | | | C |
| | COMMON | ALL COMPONENTS WITH NO BOM PROPERTY | | | | | | | | | | | | | | |
| | DDC | HDMI STUFFING OPTION. ALWAYS USED IN PRODUCTION | | | | | | | | | | | | | | |
| | DDR_BASE | DUMMY PLACE HOLDER FOR DDR3 DEVICES. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE 3 INSTEAD: DDR_HYNIX, DDR_MICRON, DDR_SAMSUNG | | | | | | | | | | | | | | |
| | DDR_HYNIX | HYNIX DDR3 | | | | | | | | | | | | | | |
| | DDR_MICRON | MICRON DDR3 | | | | | | | | | | | | | | |
| | DDR_SAMSUNG | SAMSUNG DDR3 | | | | | | | | | | | | | | |
| | DEBUG | COMPONENTS REQUIRED FOR BRING UP & DEBUG | | | | | | | | | | | | | | |
| | DEBUG_HDT | HDT-RELATED DEBUG COMPONENTS | | | | | | | | | | | | | | |
| | DEBUG_HDMI | DEBUG HDMI CONNECTOR USED 8L DEBUG BOARDS | | | | | | | | | | | | | | |
| | DEBUG_SHUNT | COMPONENTS WHICH ARE ON DEBUG BOARDS, BUT ARE REMOVED/SHORTED ON RETAIL | | | | | | | | | | | | | | |
| | EMMC_BASE | DUMMY PLACE HOLDER FOR EMMC DEVICE & RESISTORS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_20NM, EMMC_HYNIX_5P0, EMMC_HYNIX_1XNM, EMMC_SAMSUNG AND EMMC_TOSHIBA | | | | | | | | | | | | | | |
| EMMC_HYNIX_5P0 | HYNIX EMMC V5.0 EMMC DEVICE | | | | | | | | | | | | | | | |
| FET_BASE | DUMMY PLACE HOLDER FOR HIGH AND LOW FETS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: FET_AOS, FET_OS_T6, FET_STM, OR FET_TOS | | | | | | | | | | | | | | | |
| FET_IRF | INTERNATIONAL RECTIFIER FETS USED FOR VOLTAGE REGUALTORS | | | | | | | | | | | | | | | |
| FET_OS_T6 | ON-SEMI T6 FETS USED FOR VOLTAGE REGULATORS | | | | | | | | | | | | | | | |
| FET_STM | STMICROELECTRONICS FETS USED FOR VOLTAGE REGULATORS | | | | | | | | | | | | | | | |
| FET_TOS | TOSHIBA FETS USED FOR VOLTAGE REGULATORS | | | | | | | | | | | | | | | |
| GARFIELD | CONTAINS GARFIELD (SOC) RELATED PASSIVE/ACTIVE COMPONENTS | | | | | | | | | | | | | | | |
| KIC_BASE | DUMMY PLACE HOLDER FOR KIC. NEVER USE THIS IN THE RECIPE FILE. USE ONE OF THESE INSTEAD: KIC_DEV OR KIC_RETAIL | | | | | | | | | | | | | | | |
| KIC_DEV | DEBUG VERSION OF KRAKEN | | | | | | | | | | | | | | | |
| KIC_RETAIL | RETAIL VERSION OF KRAKEN | | | | | | | | | | | | | | B | |
| MEM_FIXED | SETS V_MEMIO TO A FIXED VOLTAGE (NON-MARGINED). MUST BE USED IN CONJUNCTION WITH NOT MEM_MM | | | | | | | | | | | | | | | |
| MEM_MM | ALLOWS V_MEMIO TO BE MARGINED FOR M&M BOARDS. MUST BE USED IN CONJUNCTION WITH NOT MEM_FIXED | | | | | | | | | | | | | | | |
| PANTHER | CONTAINS PANTHER (SOC) RELATED PASSIVE/ACTIVE COMPONENTS | | | | | | | | | | | | | | | |
| PANTHER_SOC | PANTHER SYSTEM-ON-CHIP (SOC) | | | | | | | | | | | | | | | |
| PANTHER_SOC_LP | PANTHER SYSTEM-ON-CHIP (SOC) LOW POWER VERSION | | | | | | | | | | | | | | | |
| PCB_GI | FAB TYPE: GOLD | | | | | | | | | | | | | | | |
| PCB_OSP | FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE | | | | | | | | | | | | | | | |
| RTC_RETAIL | RTC CIRCUIT IMPLEMENTATION FOR RETAIL BOARDS | | | | | | | | | | | | | | | |
| RTC_DEBUG | RTC CIRCUIT IMPLEMENTATION FOR DEBUG BOARDS | | | | | | | | | | | | | | | |
| SOC_BASE | DUMMY PLACE HOLDER FOR SOC | | | | | | | | | | | | | | | A |
| VR_FIXED | SET ALL VRS TO FIXED VOLTAGES (NON-MARGINED). EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_MM | | | | | | | | | | | | | | | |
| VR_MM | ALLOWS MOST VRS TO BE MARGINED FOR M&M BOARDS. EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_FIXED | | | | | | | | | | | | | | | |
| VRTB | BOOT STRAPPING RESISTOR ONLY TO BE POPULATED WHEN BUILDING VOLTAGE REGULATOR TEST BOARD WHICH CONTAINS NO SOC | | | | | | | | | | | | | | | |
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