SHEET	SHEET NAME	SHEET	SHEET NAME
1	NONE	41	CONN: M.2
2	SOC: PCIEX,CLOCKS	42	CONN: ODD
3	SOC: VIDEO	43	CONN: FRONT PANEL, FAN, NEXUS
4	SOC POWER: MEMIO, CPUCORE, SOC	44	CONN: POWER
5	SOC: POWER: GFXCORE, MEMPHY, MISC	45	VREGS: V_12P0_GATED
6	SOC: POWER: VSS	46	VREGS: INPUT DECOUPLING
7	SOC: POWER: VSS	47	VREGS: V_CPUCORE, V_GFXCORE CONTROLLER
8	SOC: DEBUG, SB SIGNALS, V_BAT, VOLTAGE SENSE	48	VREGS: V_GFXCORE OUTPUT PHASE 1 & 2
9	SOC: V_GFXCORE DECOUPLING	49	VREGS: V_GFXCORE OUTPUT PHASE 3 & 4
10	SOC: V_SOC DECOUPLING	50	VREGS: V_CPUCORE OUTPUT
11	SOC: V_MEMIO/V_MEMPHY DECOUPLING	51	VREGS: V_MEMIO, V_MEMPHY, V_SOC CONTROLLER
12	SOC: V_CPUCORE DECOUPLING	52	VREGS: V_MEMIO, V_MEMPHY, V_SOC SENSE
13	SOC & Memory: CHA/PHY0	53	VREGS: V_MEMIO AND V_MEMPHY OUTPUT
14	MEMORY: PWR/VSS & DECAP, A	54	VREGS: V_SOC OUTPUT
15	SOC & Memory: CHB/PHY1	55	VREGS: V_5P0
16	MEMORY: PWR/VSS & DECAP, B	56	VREGS: V_SOC1P8, V_DRAM1P8
17	SOC & Memory: CHC/PHY2	57	VREGS: V_SOCPHY, V_FUSE
18	MEMORY: PWR/VSS & DECAP, C	58	VREGS: V_SB1P8, V_SB1P1
19	SOC & Memory: CHD/PHY3	59	VREGS: V_3P3STBY
20	MEMORY: PWR/VSS & DECAP, D	60	VREGS: V_3P3_GATED, V_3P3_CFX
21	SB: SMC	61	VREGS: V_1P1STBY, V_1P8STBY
22	SB: USB	62	I2C
23	SB: PCIEX, SATA, VIDEO	63	DEBUG: MARGIN V_SOCPHY,V_SOC1P8, V_DRAM1P8
24	SB: SMM UART, SPI, JTAG, GPIO	64	DEBUG: MONITOR V_SOC1P8, V_SOCPHY, V_12P0, V_DRAM1P8
25	SB: POWER (VSS)	65	DEBUG: MONITOR M.2. CFEXPRESS
26	SB: POWER	66	DEBUG: FACET HEADER
27	SB: DECOUPLING	67	DEBUG: FTDI BRIDGE
28	SB: CLOCKS, STRAPPING, POR	68	DEBUG: FTDI BUFF, USB, PWR
29	CLOCK: PCIE 100MHZ SS	69	DEBUG: SWITCHES, LEDS
30	CLOCK: PCIE 100MHZ NS	70	DEBUG: HDT
31	ETHERNET CONTROLLER	71	DEBUG: VR HEADERS, TEST POINTS, CONNECTORS
32	SB: EMMC (LEGACY)	72	LABELS AND MOUNTING
33	MEMORY: SPI FLASH SOC	73	BOM DEFINITIONS
34	MEMORY: SPI FLASH	74	STOCKTON_NEXUS
35	HDMI: VIDEO OUT	75	B2B CONN AND LABELS
36	HDMI: LOAD SWITCHES	76	NEXUS LED AND POWER SWITCH
37	AUDIO: PREMIUM AND RETAIL		
38	CONN: RJ45, SPDIF, CFEXPRESS		
39	CONN: USB (FRONT & REAR)		
40	CONN: WIFI		

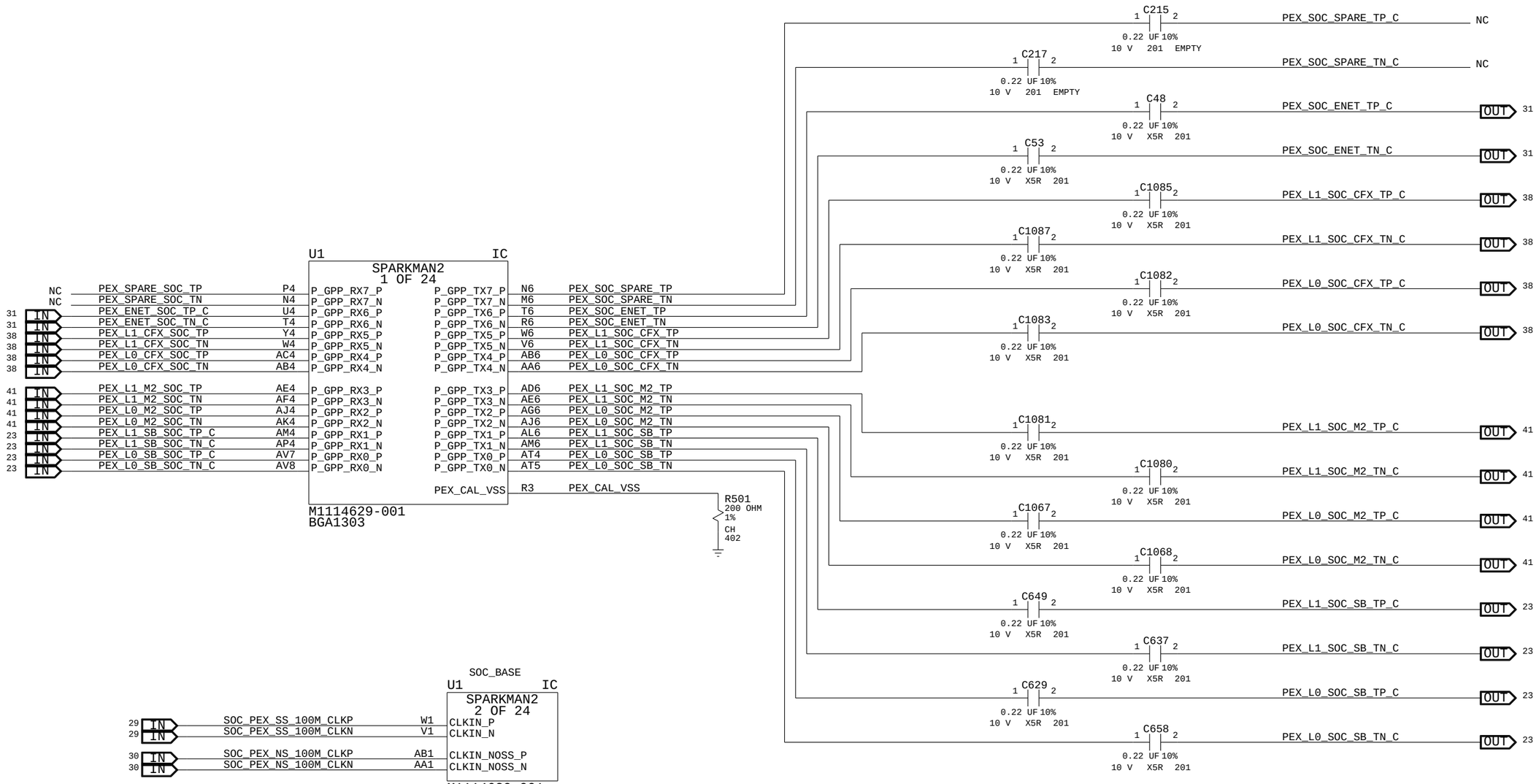
STOCKTON FAB C
REV 0.12

RULES: (APPLIED WHEN POSSIBLE)
1. MSB TO LSB IS TOP TO BOTTOM
2. WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
3. ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
4. AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
5. LANED SIGNALS ARE GROUPED ON SYMBOLS
6. TRANSIMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
7. SUFFIX V_ IS USED FOR VOLTAGE RAIL SIGNAL NAMES
8. SUFFIX _DP AND _DN ARE USED FOR DIFFERIENTAL PAIRS
9. UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
10. SUFFIX _N FOR ACTIVE LOW OR N JUNCTION
12. SUFFIX _P FOR P JUNCTION
13. SUFFIX _EN FOR ENABLE
14. 'CLK' FOR CLOCKS, 'RST' FOR RESETS
15. PWRGD FOR POWER GOOD
16. REV AND FAB ARE SET USING CUSTOM VARIABLES
    TOOLS>OPTIONS>VARIABLES

DRAWING
Tue Jun 25 13:39:30 2019

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	1/76	1/76	C	0.12

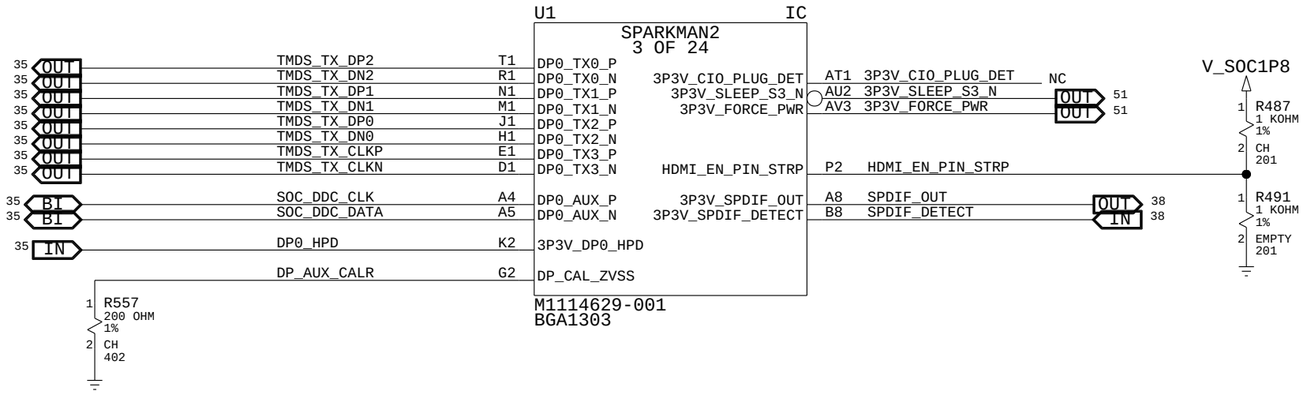
SOC: PCIEX,CLOCKS



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1114629-001	IC	U1	PROCSR,SOC,SM,1304-BGA,SPARKMAN35	SOC_INCLUDE
M1114629-001	EMPTY	U1	PROCSR,SOC,SM,1304-BGA,SPARKMAN35	SOC_EMPTY

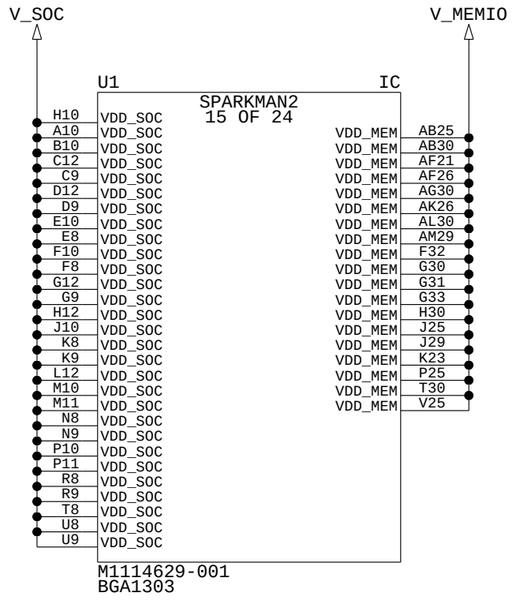
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	2/76	2/76	C	0.12

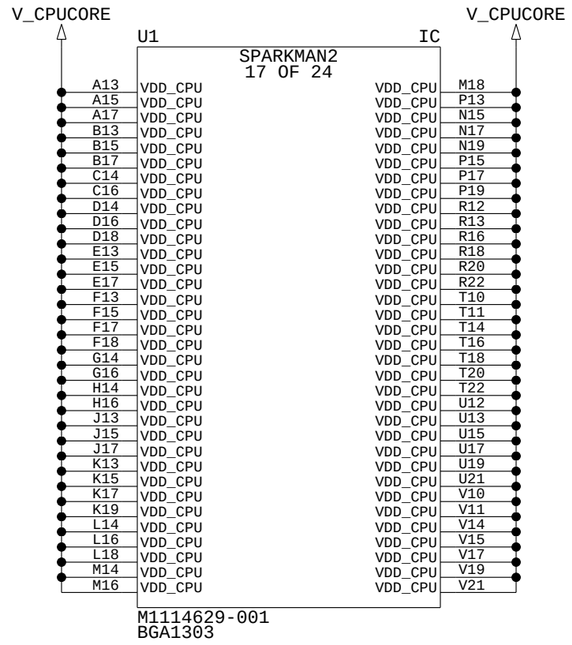
SOC: VIDEO



DVI PCB ROUTING ORDERING	DP PCB ROUTING ORDERING	PIN NAME
TMDS CLOCK -	DP LANE 3 -	DP0_TX3_N
TMDS CLOCK +	DP LANE 3 +	DP0_TX3_P
TMDS DATA0 -	DP LANE 2 -	DP0_TX2_N
TMDS DATA0 +	DP LANE 2 +	DP0_TX2_P
TMDS DATA1 -	DP LANE 1 -	DP0_TX1_N
TMDS DATA1 +	DP LANE 1 +	DP0_TX1_P
TMDS DATA2 -	DP LANE 0 -	DP0_TX0_N
TMDS DATA2 +	DP LANE 0 +	DP0_TX0_P

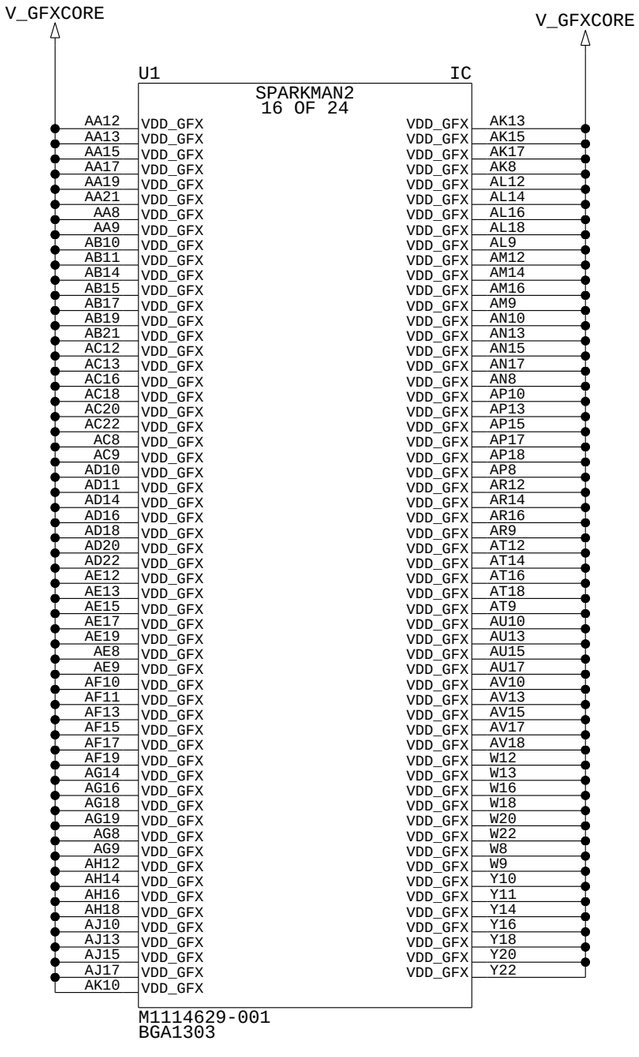
SOC POWER: MEMIO, CPUCORE, SOC

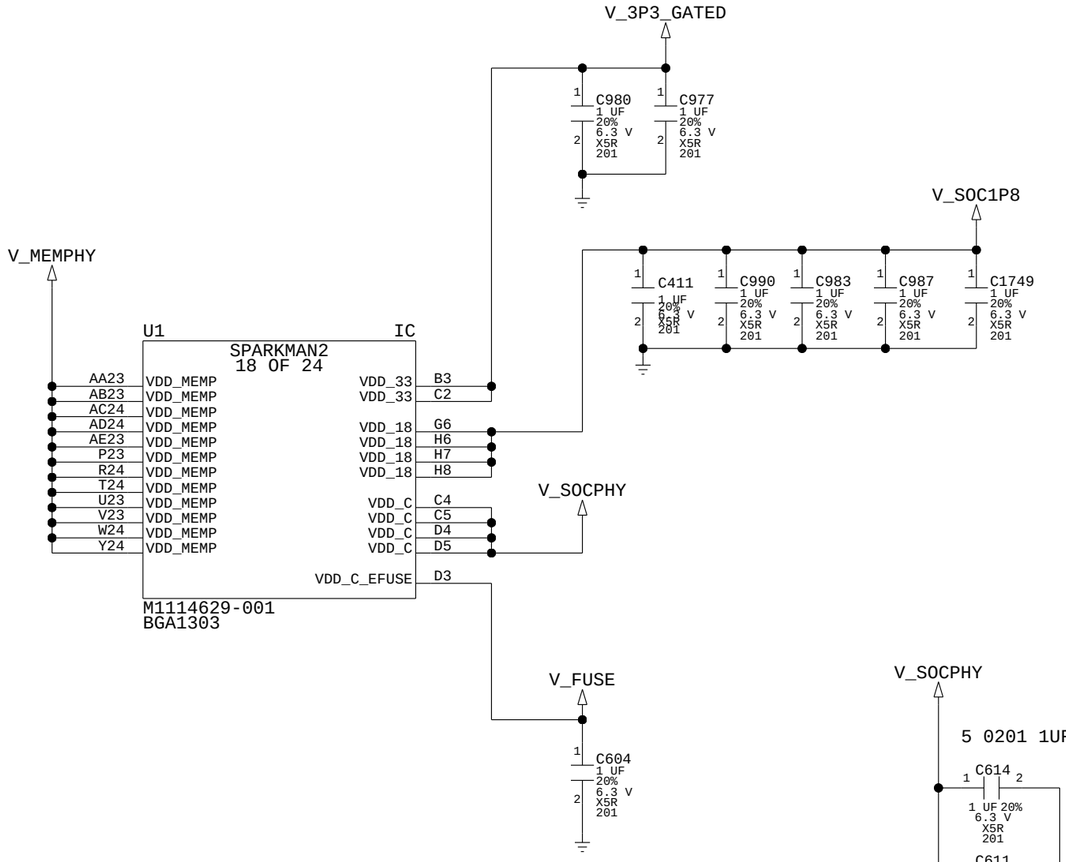




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	4/76	4/76	C	0.12

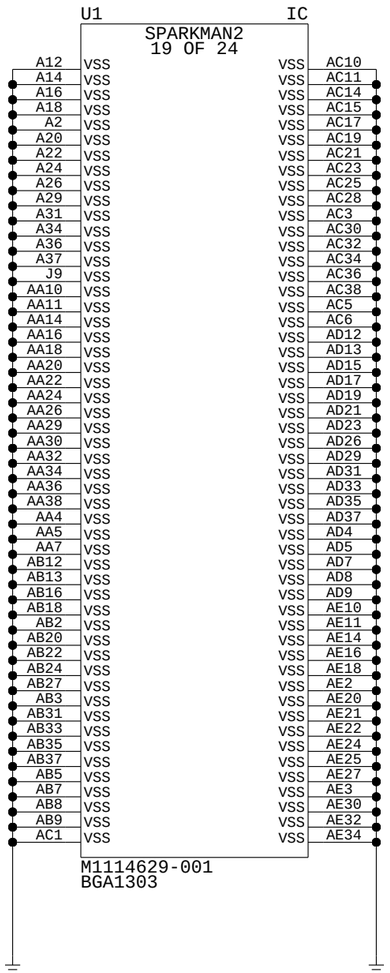
SOC: POWER: GFXCORE, MEMPHY, MISC

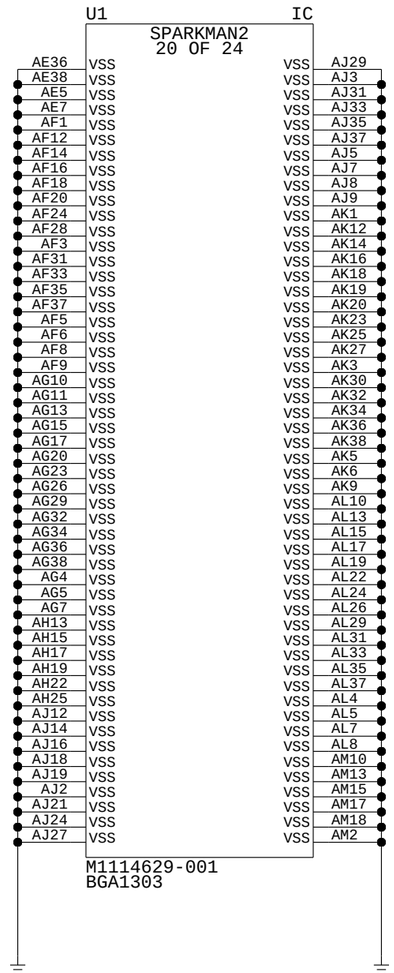


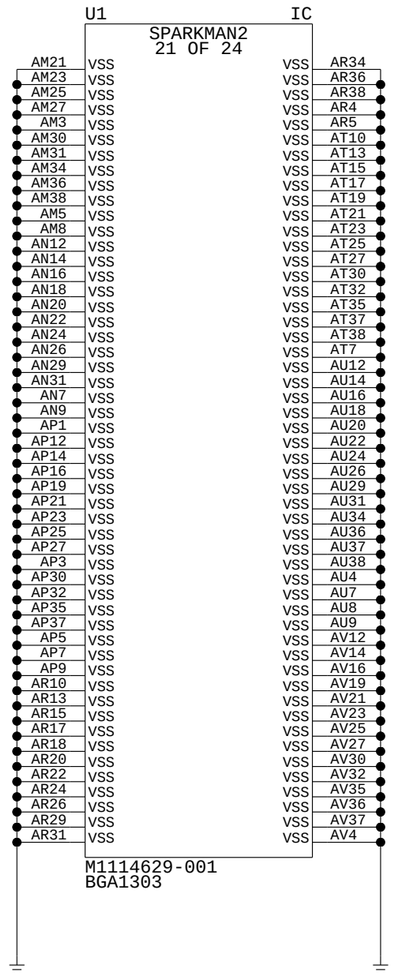


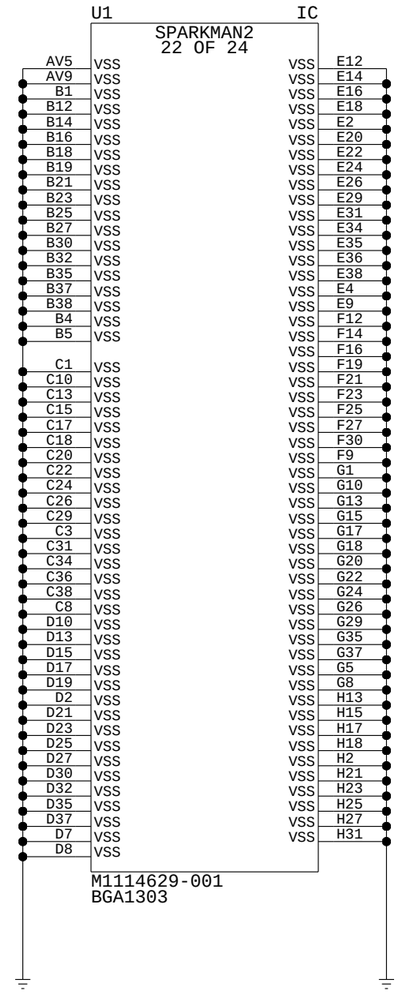
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	5/76	5/76	C	0.12

SOC: POWER: VSS



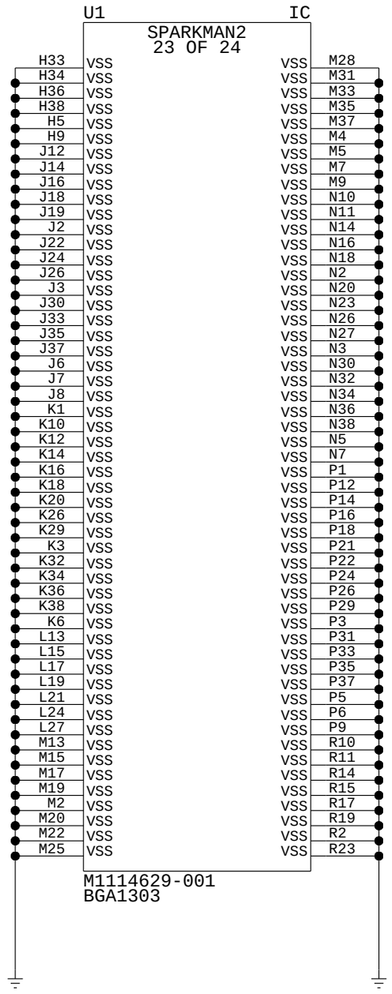


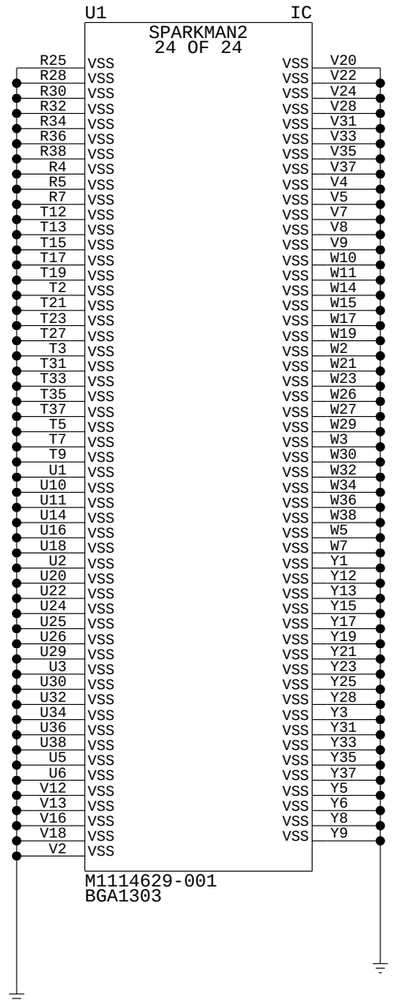




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	6/76	6/76	C	0.12

SOC: POWER: VSS





MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	7/76	7/76	C	0.12

SOC: DEBUG, SB SIGNALS, V_BAT, VOLTAGE SENSE

U1 IC
SPARKMAN2
4 OF 24

70 IN DBREQ_L AL3 DBREQ_N
70 21 IN TCK AG1 TCK
70 21 IN TDI AJ1 TDI
70 21 OUT TDO AG2 TDO
70 21 IN TMS AF2 TMS
70 IN TRST_L AG3 TRST_N

FLOATING IN FINAL DESIGN
ANATSTIN_N P8 ANATSTIN_P
ANATSTIN_P P7 ANATSTIN_N
ANATSTOUT_P K7 ANATSTOUT_P
ANATSTOUT_N M8 ANATSTOUT_N

AT3 PSEN
AU5 A0_BYPASS

TMON_CAL E3 TMON_CAL0 — 1 FTP FT78
TM_IO A3 TM_IO
THERMDA E7 THERMDA
THERMDC F7 THERMDC
ANALOGOUT0 H3 ANALOGOUT0
ANALOGOUT1 H4 ANALOGOUT1
BP_0 K4 BP_0
BP_1 J4 BP_1
BP_2 K5 BP_2
BP_3 J5 BP_3
DIECRACKMON G3 DIECRACKMON

NC FLOATING IN FINAL DESIGN

M1114629-001
BGA1303

V_SOC1P8
R821 1 KOHM 1% EMPTY 402
R822 10 KOHM 1% EMPTY 402
A0_BYPASS

47 OUT SVC
47 BI SVD
47 IN SVT
R628 0 OHM 5% CH 402
R627 0 OHM 5% CH 402
R626 0 OHM 5% CH 402

V_SOC1P8
R405 475 OHM 1% EMPTY 402 DEBUG
C553 47 PF 5% 50 V EMPTY 201 DEBUG
R406 475 OHM 1% EMPTY 402 DEBUG
C554 47 PF 5% 50 V EMPTY 201 DEBUG

21 BI SB_SOC_CLK
R430 243 OHM 1% CH 402
21 IN SB_SOC_DATA
R431 243 OHM 1% CH 402

V_SOC1P8
R810 100 KOHM 1% CH 201

SVC_R_SOC Y7
SVD_R_SOC AC7
SVT_R_SOC U7
SOC_SIC AR1
SOC_SID AP2
X32K_X1 AA2
X32K_X2 Y2
70 47 21 OUT SOC_PWR_OK AT2
21 OUT SOC_THERMTRIP_N AK7
21 OUT SP_SMC_INT_N AR2
PROCHOT_N AF7
V3
70 21 IN SOC_RST_N AR3
AU1
AV2

V_BAT
C645 1 UF 20% 6.3 V X5R 201

RTC_RETAIL
28 IN X32K_X2_R
R84 0 OHM 5% 402 CH

RTC_XDK
R97 20 MOHM 5% 402 CH

C144, C155 VALUE SELECTED
TO CENTER XTAL FREQ

Y1
32.768 KHZ
SM
XTAL
M1099527-001
RTC_XDK

RTC_XDK C144 2.2 PF 0.25PF 50 V NPO 402
RTC_XDK C155 2.2 PF 0.25PF 50 V NPO 402

U1 IC
SPARKMAN2
6 OF 24

SVC SVD SVT
SOC_SIC SOC_SID
X32K_X1 X32K_X2
PWROK
THERMTRIP_N ALERT_N PROCHOT_N VDD_RTC
RESET_N
CHK_PAD EQ_MAG

M1114629-001
BGA1303

NOTE: CHK_PAD AND EQ_MAG
MUST BE CONNECTED TO VSS
FOR BEST RESULTS

SVC1 B7 CAC_THROTTLE_DET — 1 DB16
SVD1 A7 CAC_COUNTER_SNAP_DET — 1 DB14
SVT1 C7 1P8V_GPIO2 — 1 DB489
PCC G4 PCC — 1 DB18
VR_MEMIO_CTL AR8 VR_MEMIO_CTL
QSS_N AA3 QSS_N — OUT 33
QSCLK AD1 QSCLK — OUT 33
QSIO0 AE1 QSIO0 — OUT 33
QSIO1 AD2 QSIO1 — IN 33
QSIO2 AD3 QSIO2 — OUT 33
QSIO3 AC2 QSIO3 — OUT 33
1P8V_GPIO0 E5 GPIO_SPARE0
1P8V_GPIO1 AU3 1P8V_GPIO1
MST_SIC0 AM1 MST_SIC0
MST_SID0 AL1 MST_SID0
MST_SIC1 AL2 MST_SIC1
MST_SID1 AK2 MST_SID1

1 DB4
1 DB6
1 DB8
1 DB10

U1 IC
SPARKMAN2
5 OF 24

47 OUT SOC_GFXCORE_S AT8 VDD_GFX_SENSE
47 OUT SOC_GFXCORE_S_RTN AR7 VSS_GFX_SENSE
47 OUT SOC_CPUCORE_S N12 VDD_CPU_SENSE
47 OUT SOC_CPUCORE_S_RTN N13 VSS_CPU_SENSE
52 OUT SOC_VSOC_S A9 VDD_SOC_SENSE
52 OUT SOC_VSOC_S_RTN B9 VSS_SOC_SENSE
52 OUT SOC_MEMIO_S E32 VDD_MEM_SENSE
52 OUT SOC_MEMIO_S_RTN F31 VSS_MEM_SENSE
52 OUT SOC_MEMPHY_S P20 VDD_MEMP_SENSE
52 OUT SOC_MEMPHY_S_RTN R21 VSS_MEMP_SENSE

M1114629-001
BGA1303

RTC_XDK
CONN BT1
BATT_HOLD_2P
2 NEG
POS 1 RTC_VREG_IN
M1083468-001
SM1
BATTERY CONNECTOR

V_3P3STBY
U77
SOT-523
DIO
RTC_XDK

RTC_VREG_IN_D
C512 0.1 UF 10% 16 V X5R 201 RTC_XDK

Q1 1.8V
NCP663
VIN VOUT
NC GND
X899201-001
SC82
RTC_XDK

RTC_VREG_OUT
C513 0.1 UF 10% 16 V X5R 201 RTC_XDK

R77 0 OHM 5% 402 CH RTC_XDK

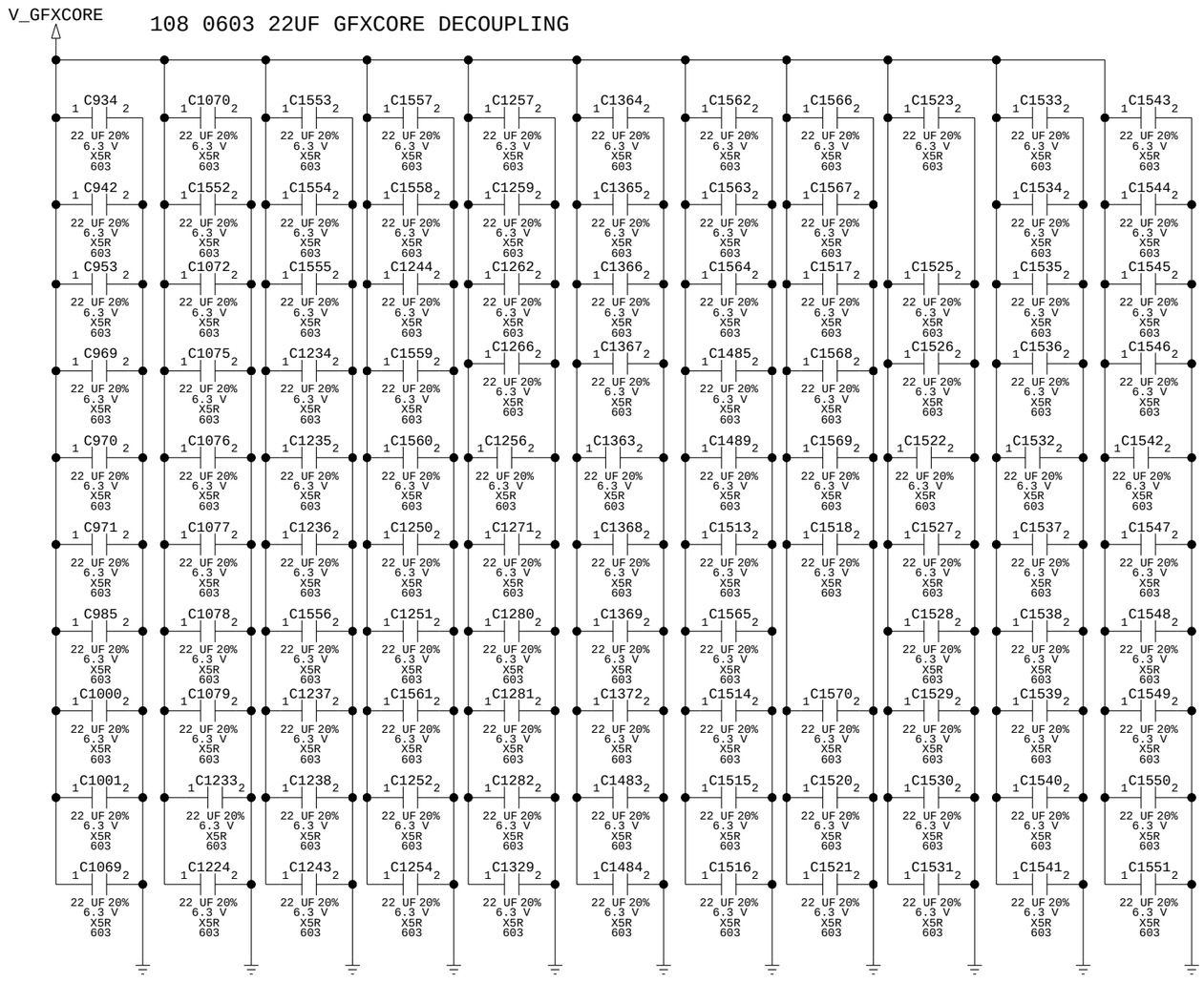
V_1P8STBY
R387 0 OHM 5% CH 402 RTC_RETAIL
R388 221 KOHM 1% CH 402 RTC_XDK

V_BAT
V_BAT
NOM.VOLTAGE: 1.8V

STUFF R388 IF SOC IS NOT STUFFED

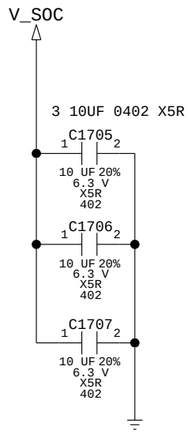
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	8/76	8/76	C	0.12

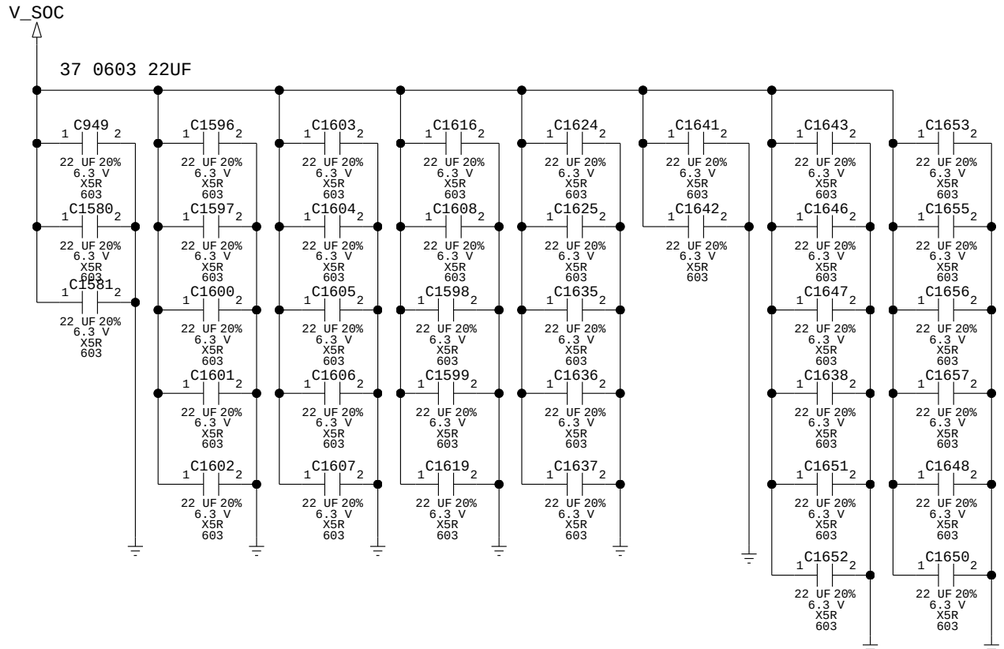
SOC: V_GFXCORE DECOUPLING



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	9/76	9/76	C	0.12

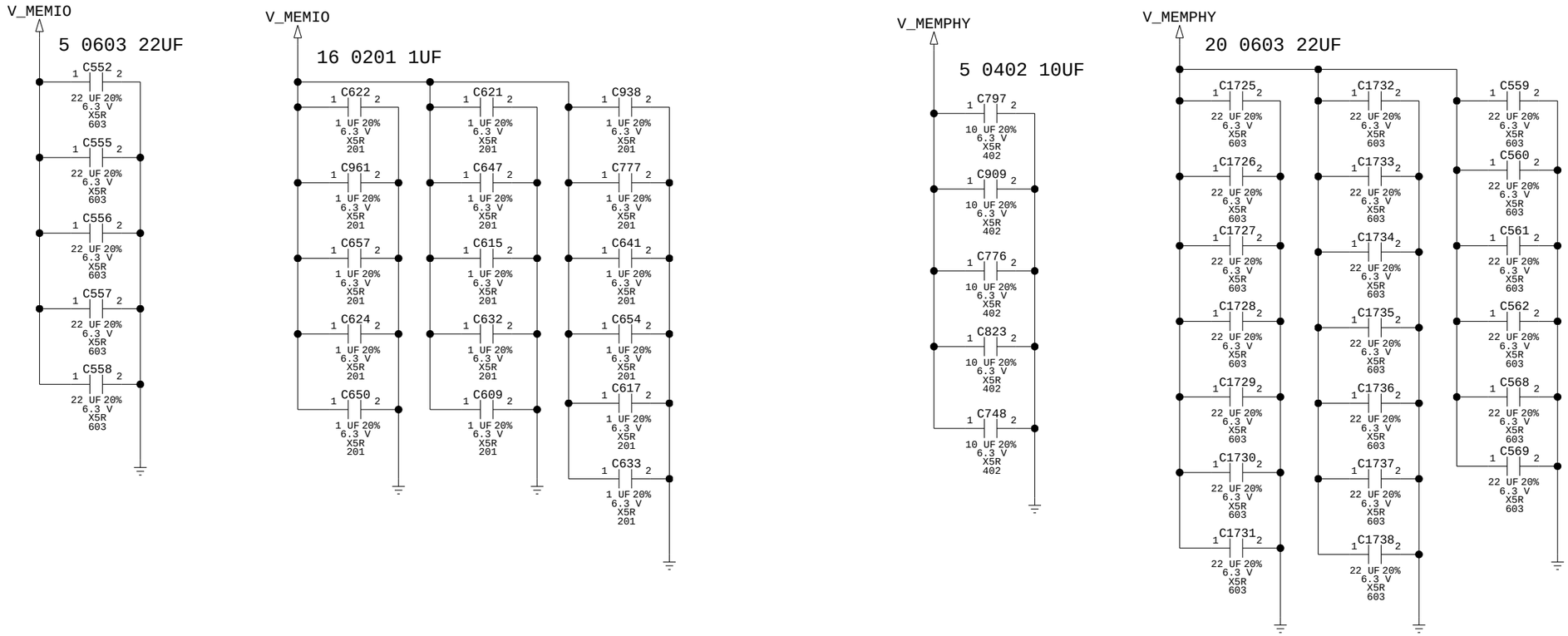
SOC: V_SOC DECOUPLING





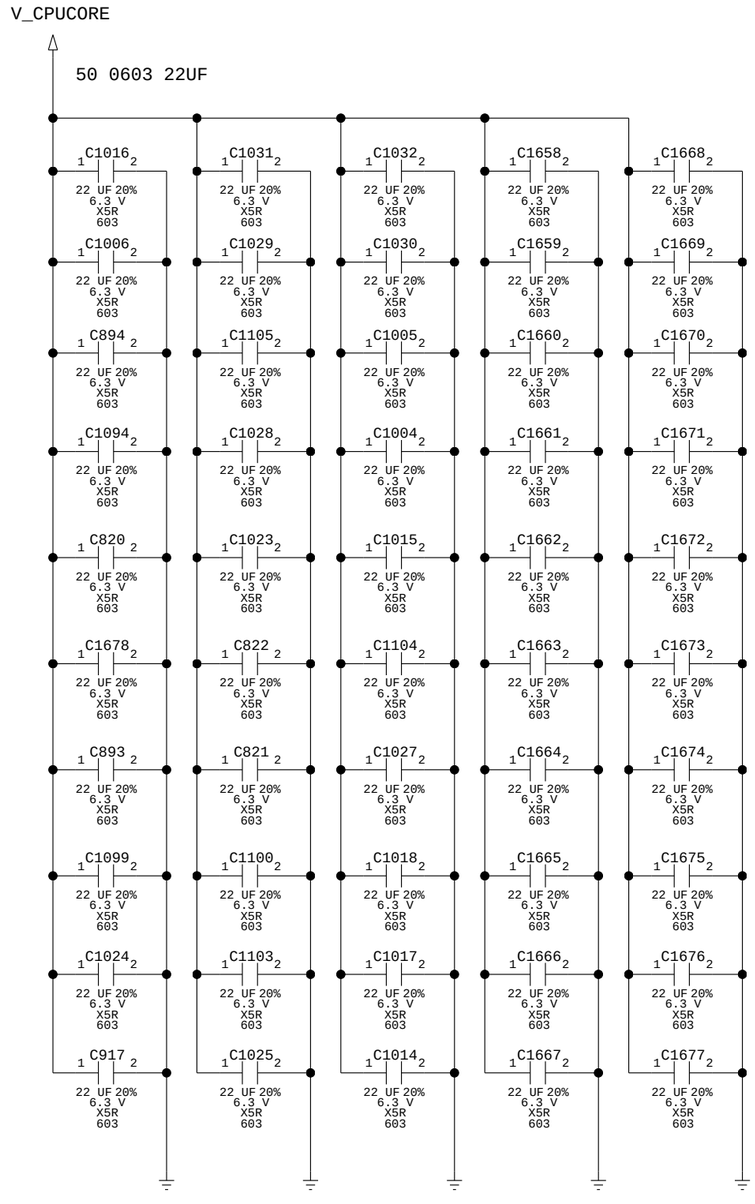
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	10/76	10/76	C	0.12

SOC: V_MEMIO/V_MEMPHY DECOUPLING



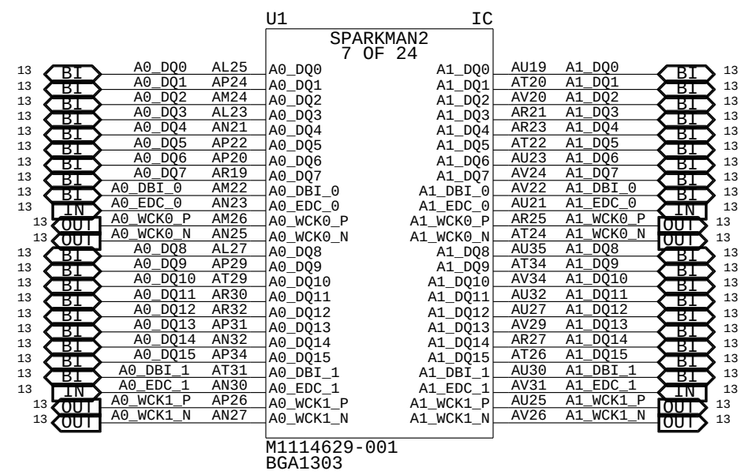
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	11/76	11/76	C	0.12

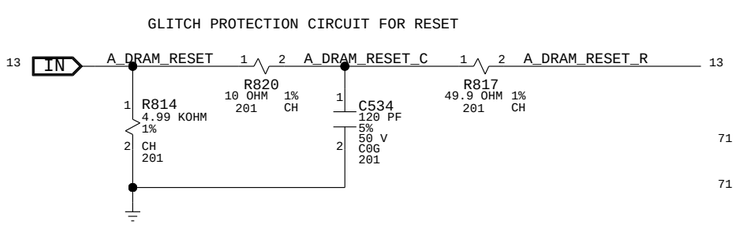
SOC: V_CPUCORE DECOUPLING

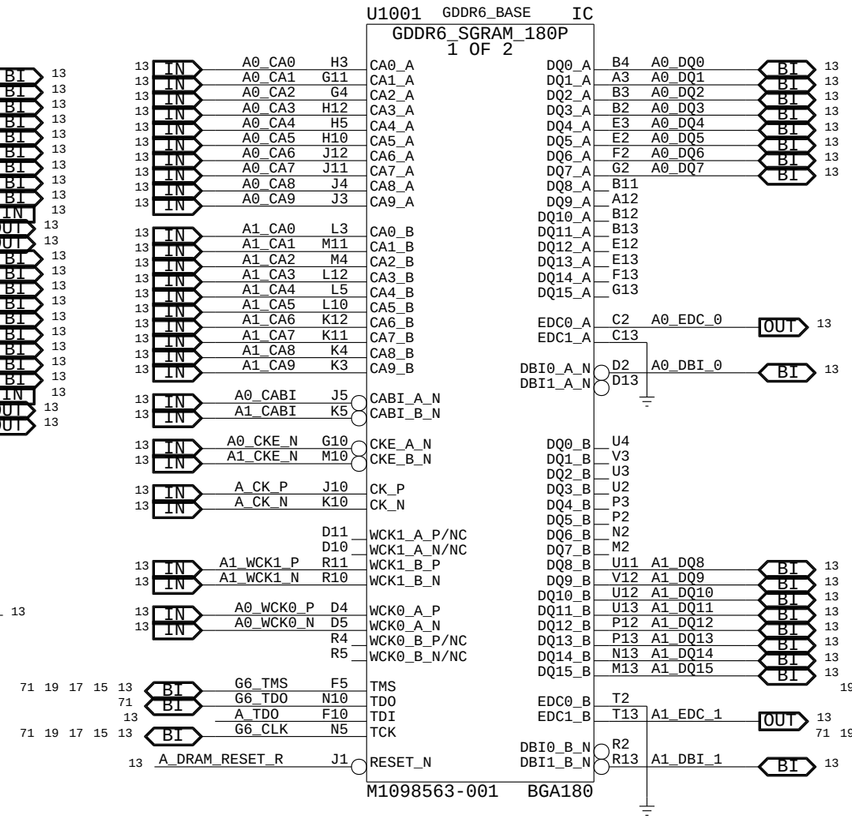


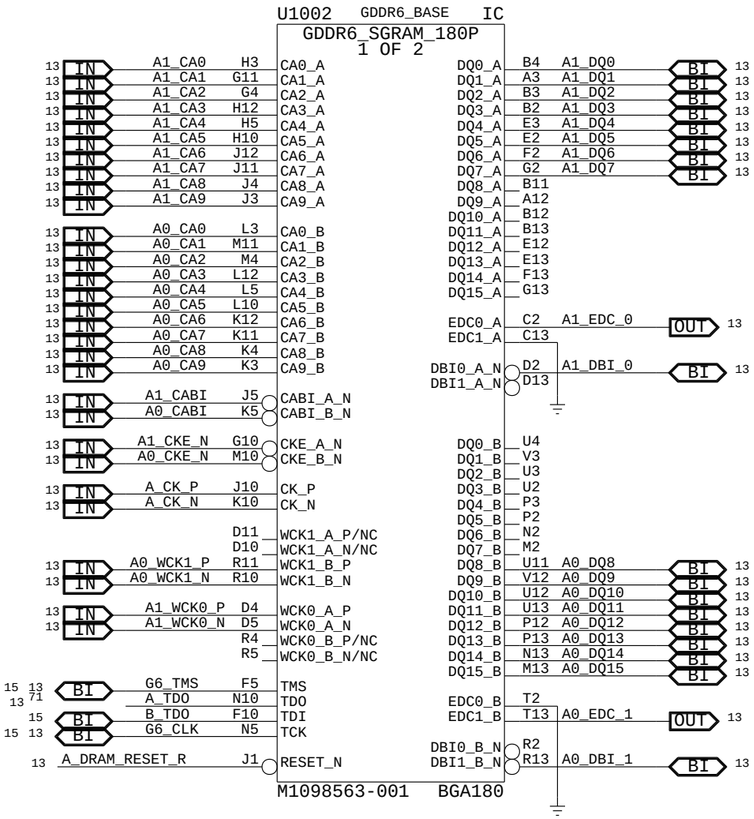
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	12/76	12/76	C	0.12

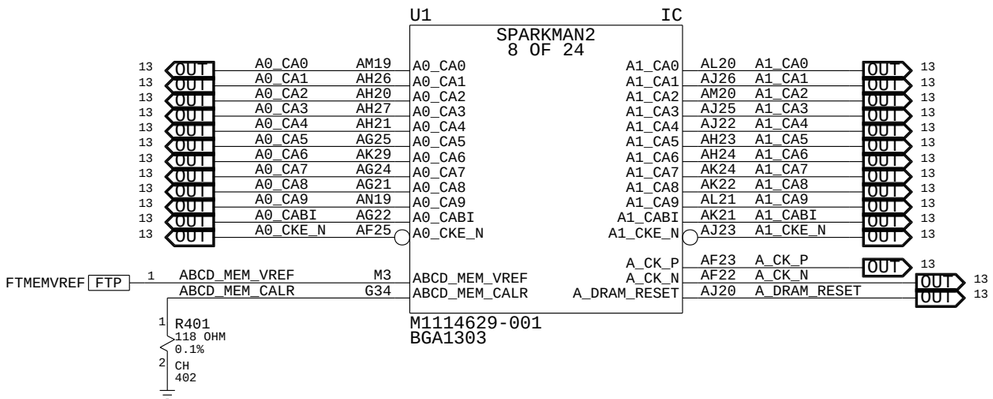
SOC & Memory: CHA/PHY0







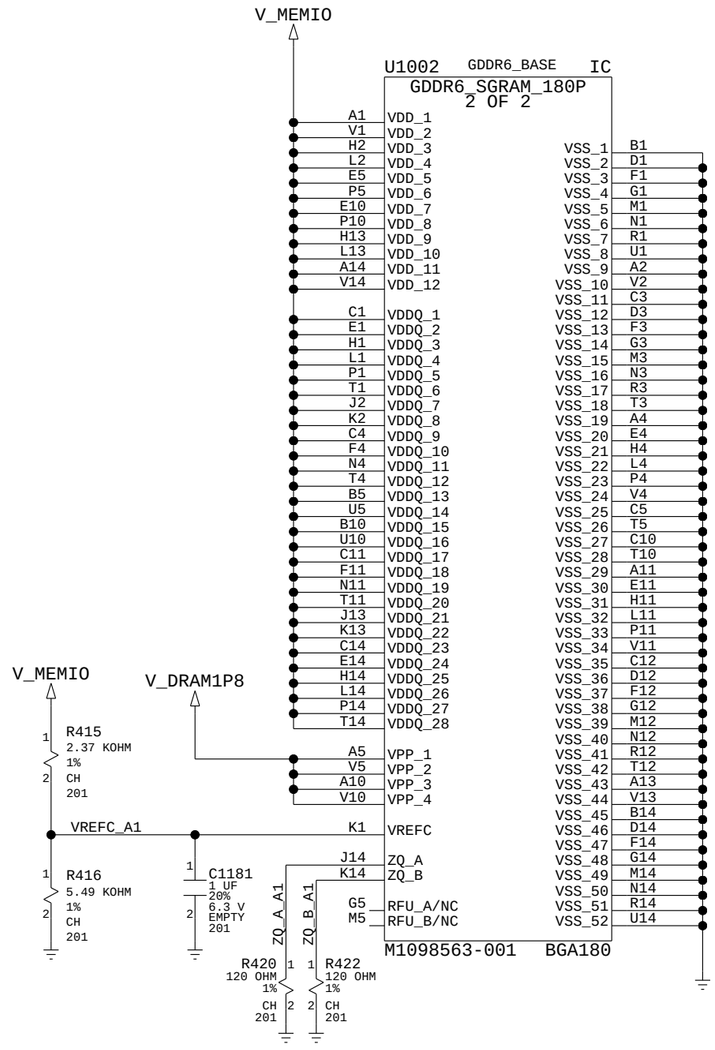


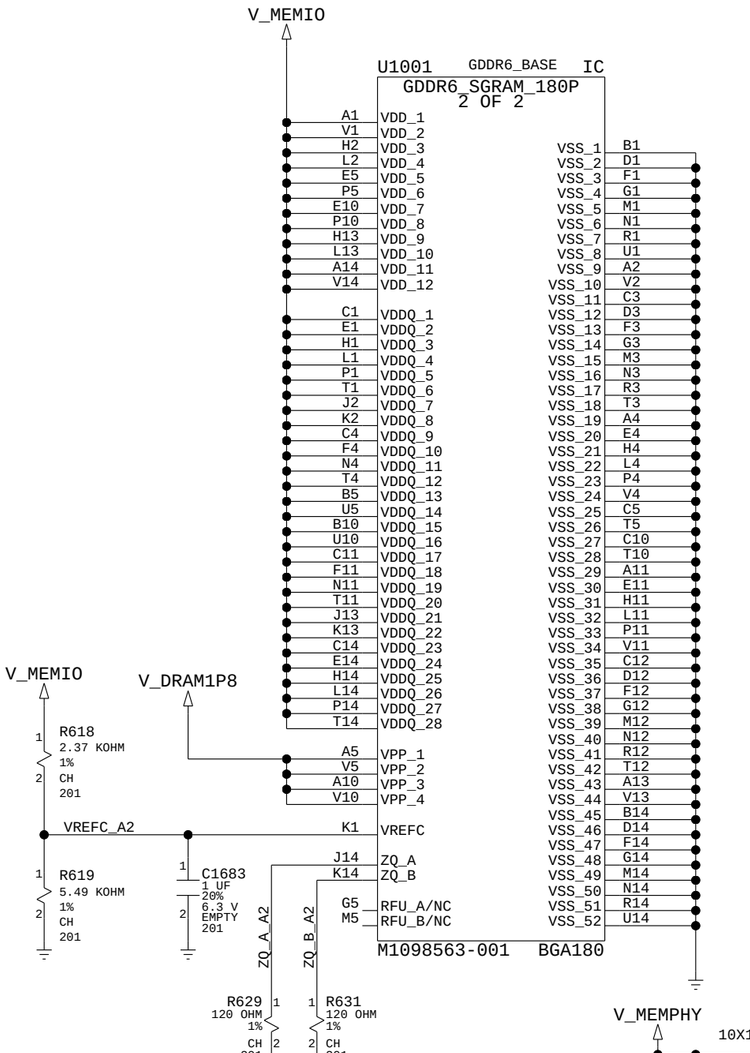


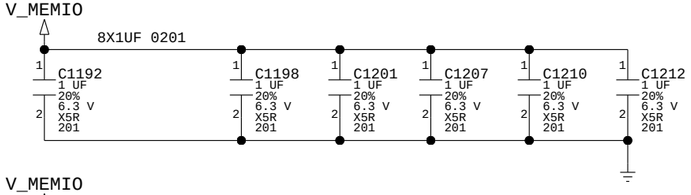
MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1098563-001	IC	U1002, U1001, U1005, U1006, U1011	GDDR6	GDDR6_SAMSUNG
M1107532-001	IC	U1002, U1001, U1005, U1006, U1011	GDDR6	GDDR6_HYNIX
M1107537-001	IC	U1002, U1001, U1005, U1006, U1011	GDDR6	GDDR6_MICRON

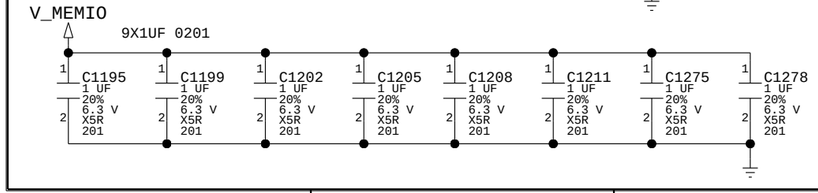
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	13/76	13/76	C	0.12

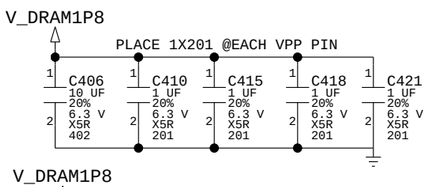
MEMORY: PWR/VSS & DECAP, A

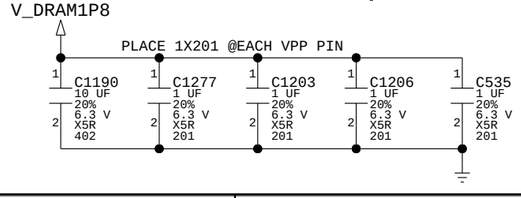


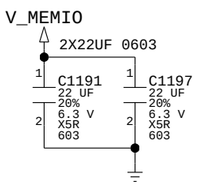


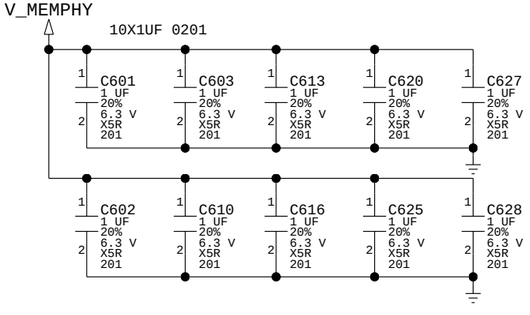






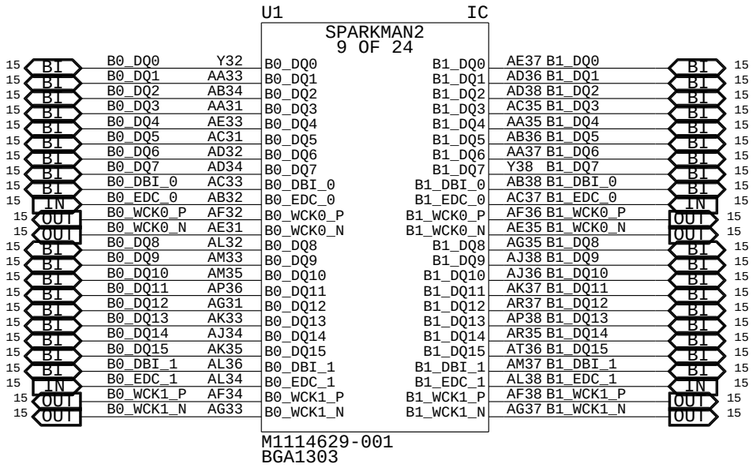


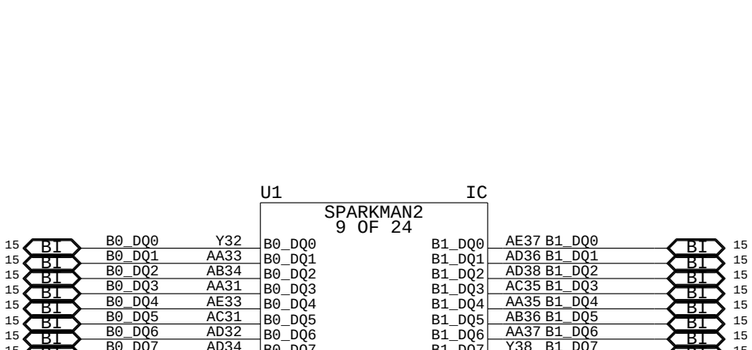


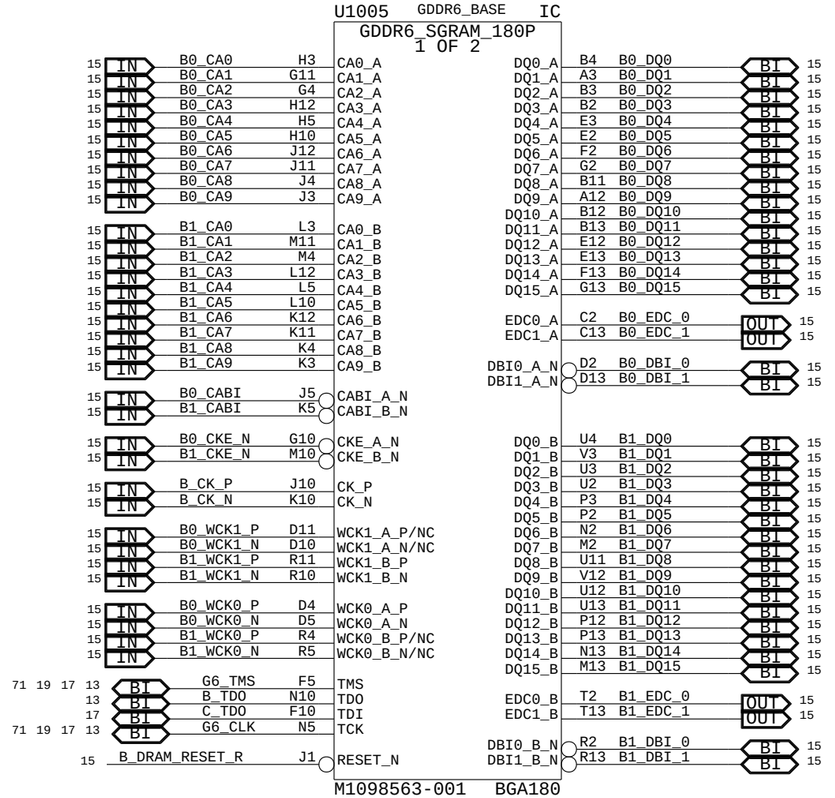


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	14/76	14/76	C	0.12

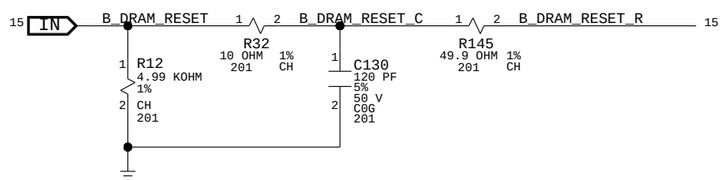
SOC & Memory: CHB/PHY1





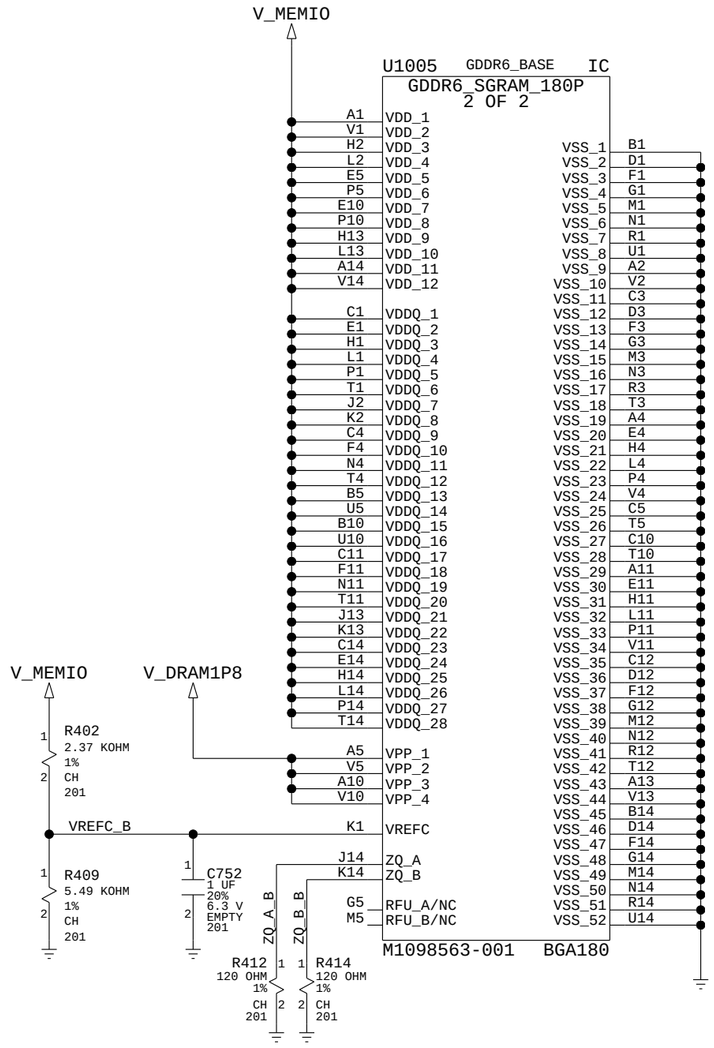


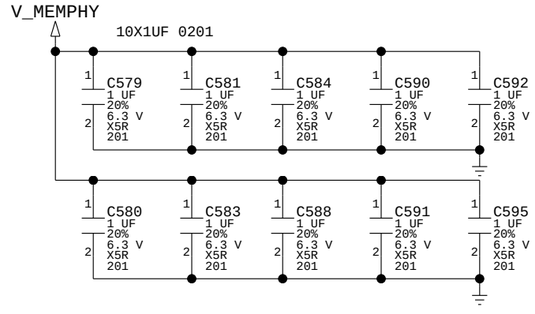
GLITCH PROTECTION CIRCUIT FOR RESET

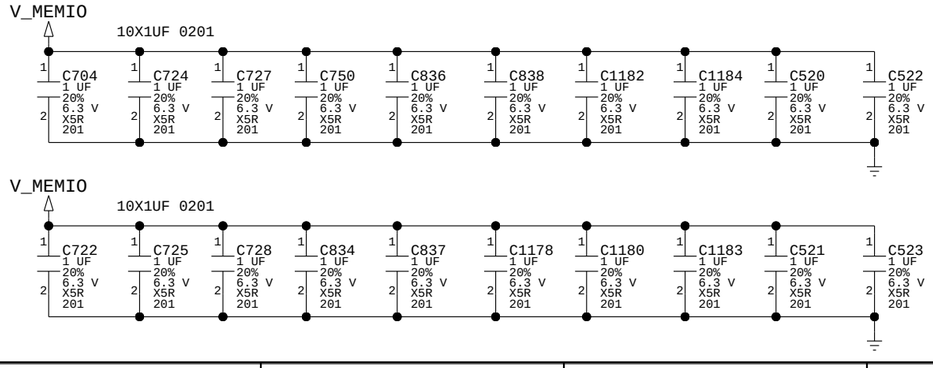


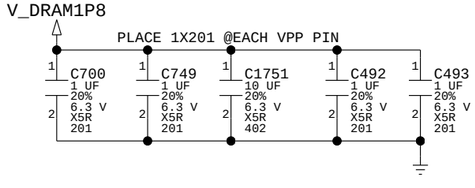
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	15/76	15/76	C	0.12

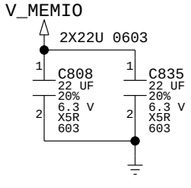
MEMORY: PWR/VSS & DECAP, B





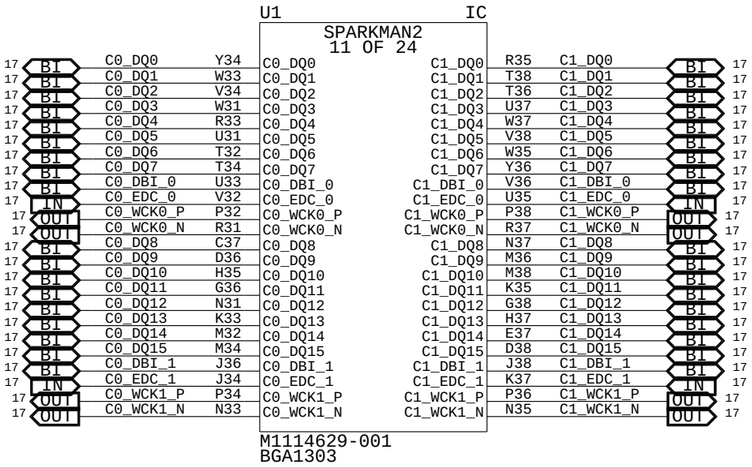


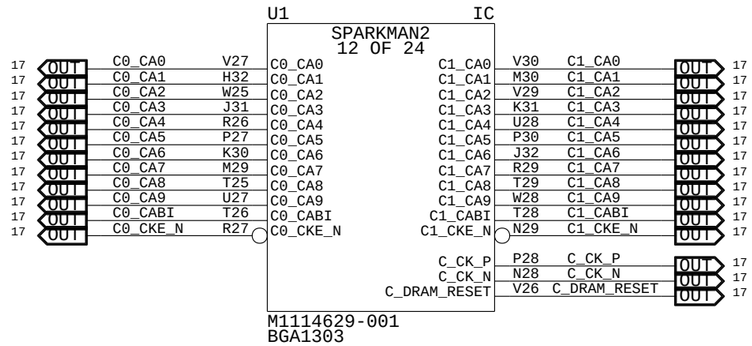


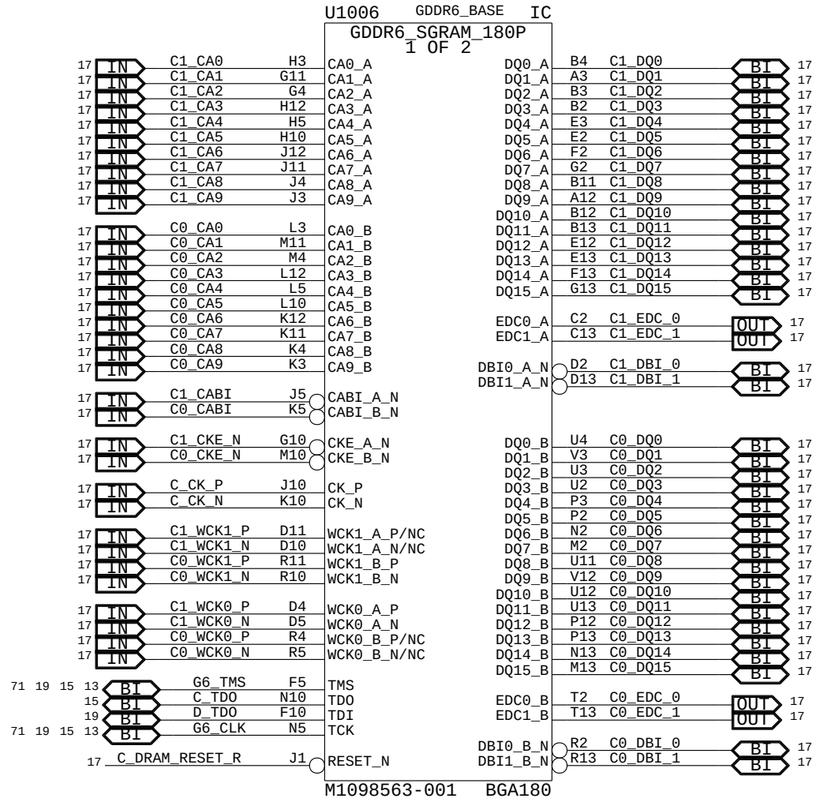


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	16/76	16/76	C	0.12

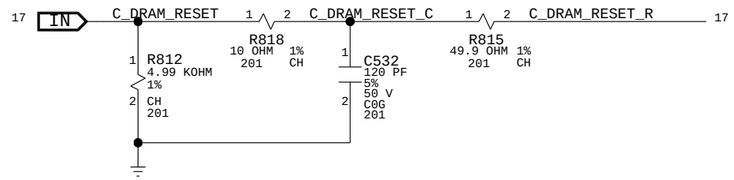
SOC & Memory: CHC/PHY2





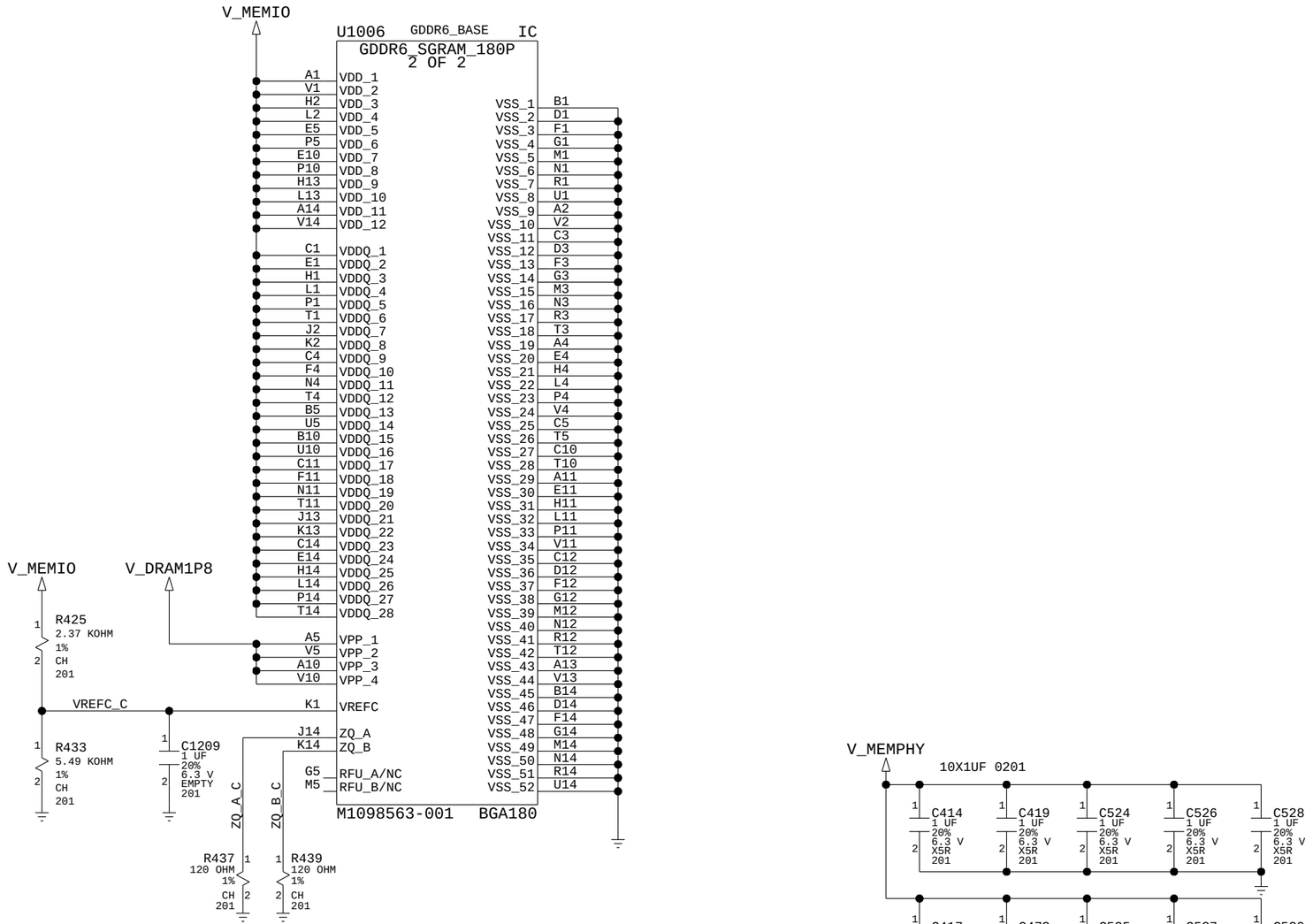


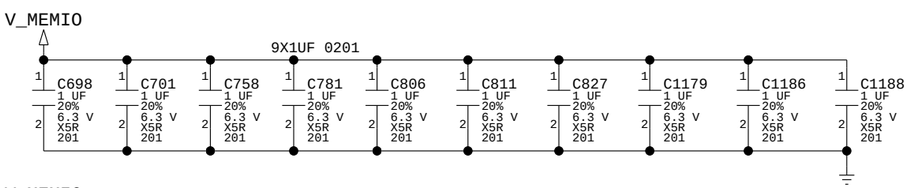
GLITCH PROTECTION CIRCUIT FOR RESET

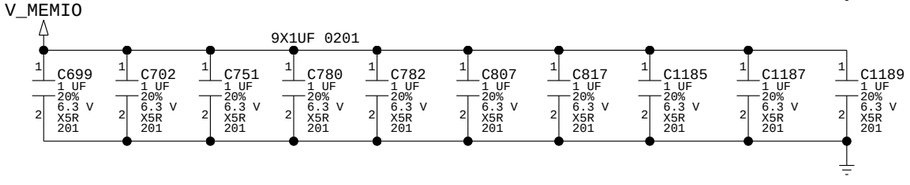


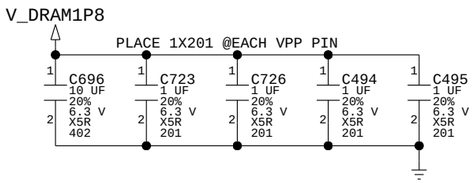
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	17/76	17/76	C	0.12

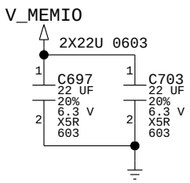
MEMORY: PWR/VSS & DECAP, C





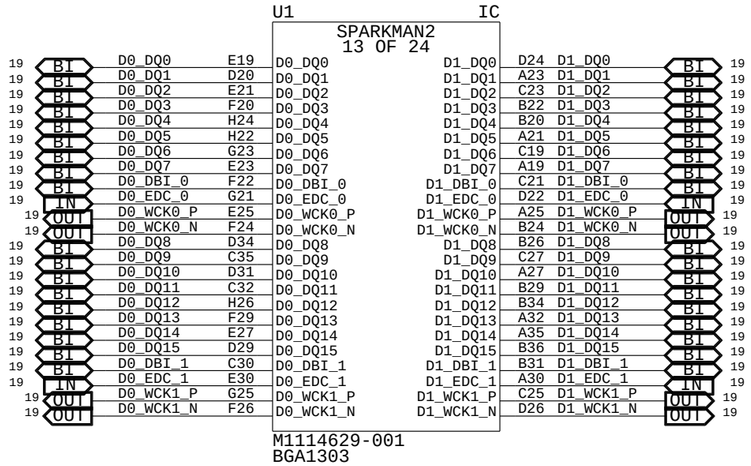


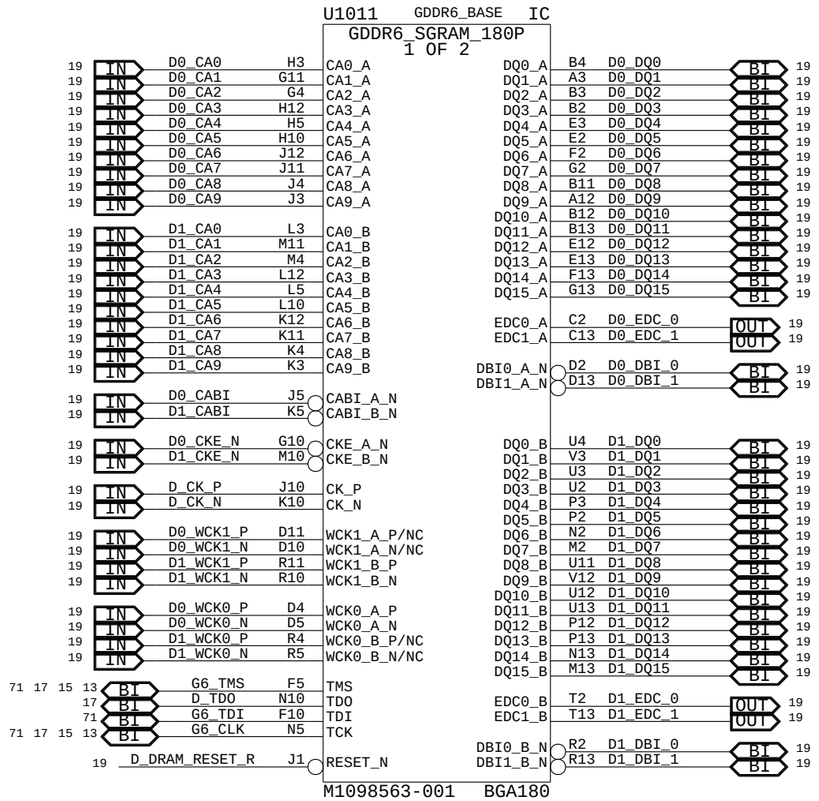


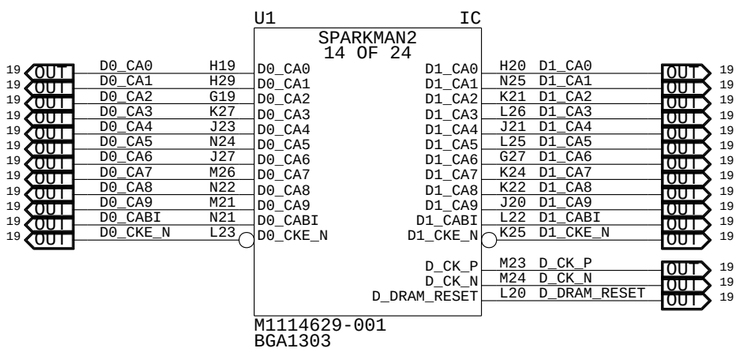


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	18/76	18/76	C	0.12

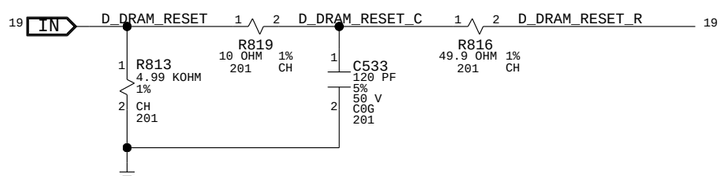
SOC & Memory: CHD/PHY3





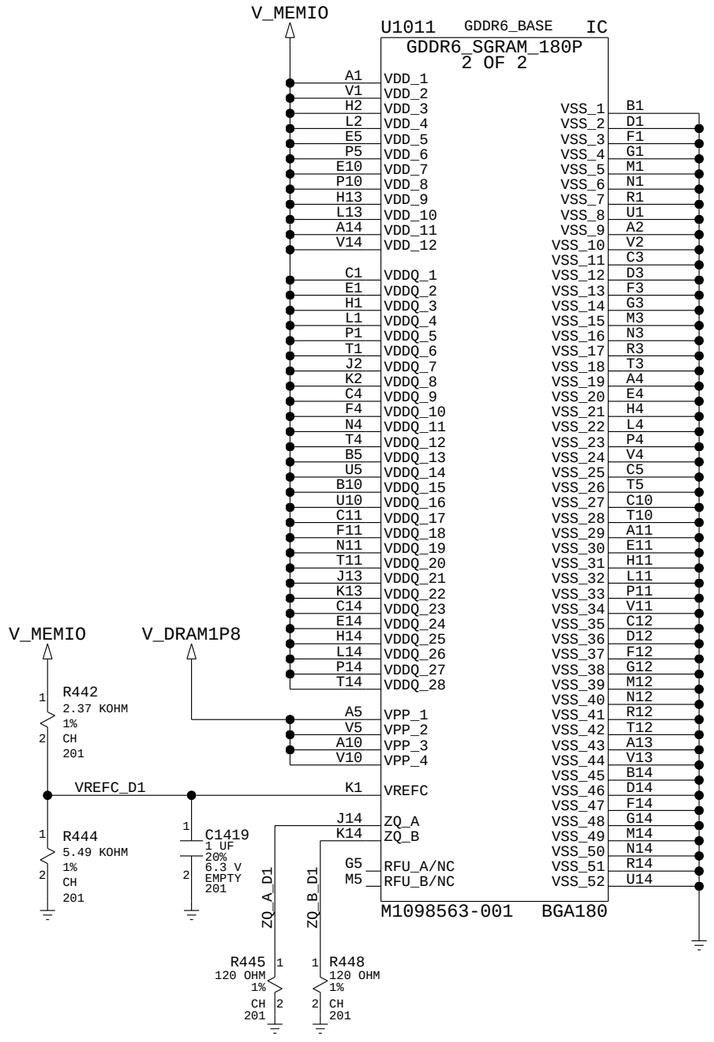


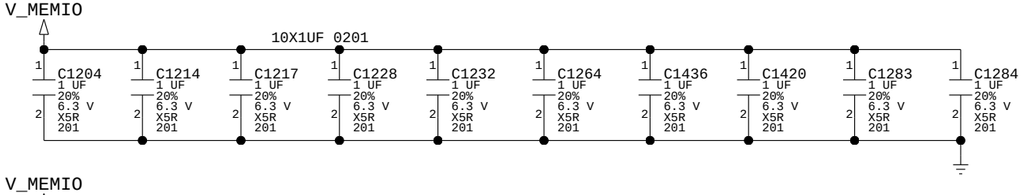
GLITCH PROTECTION CIRCUIT FOR RESET

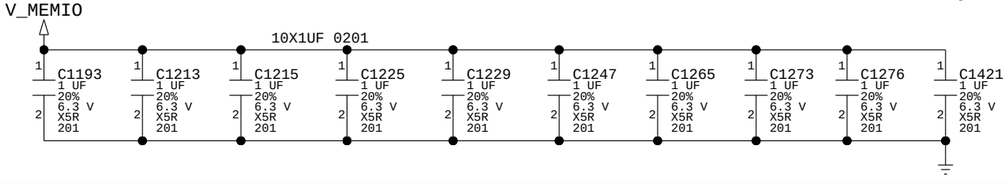


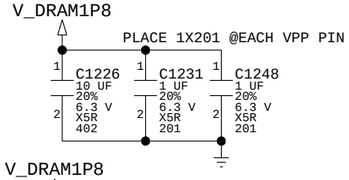
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	19/76	19/76	C	0.12

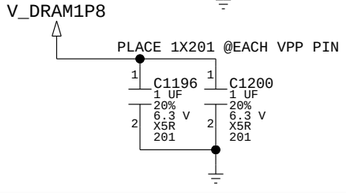
MEMORY: PWR/VSS & DECAP, D

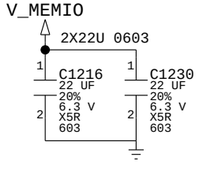


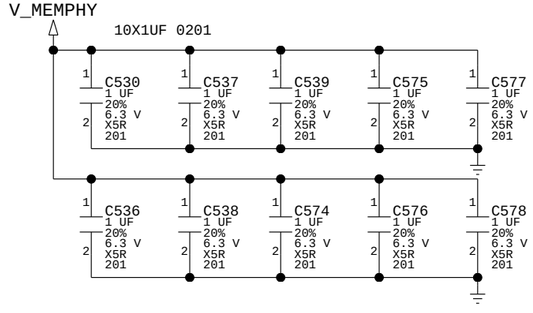






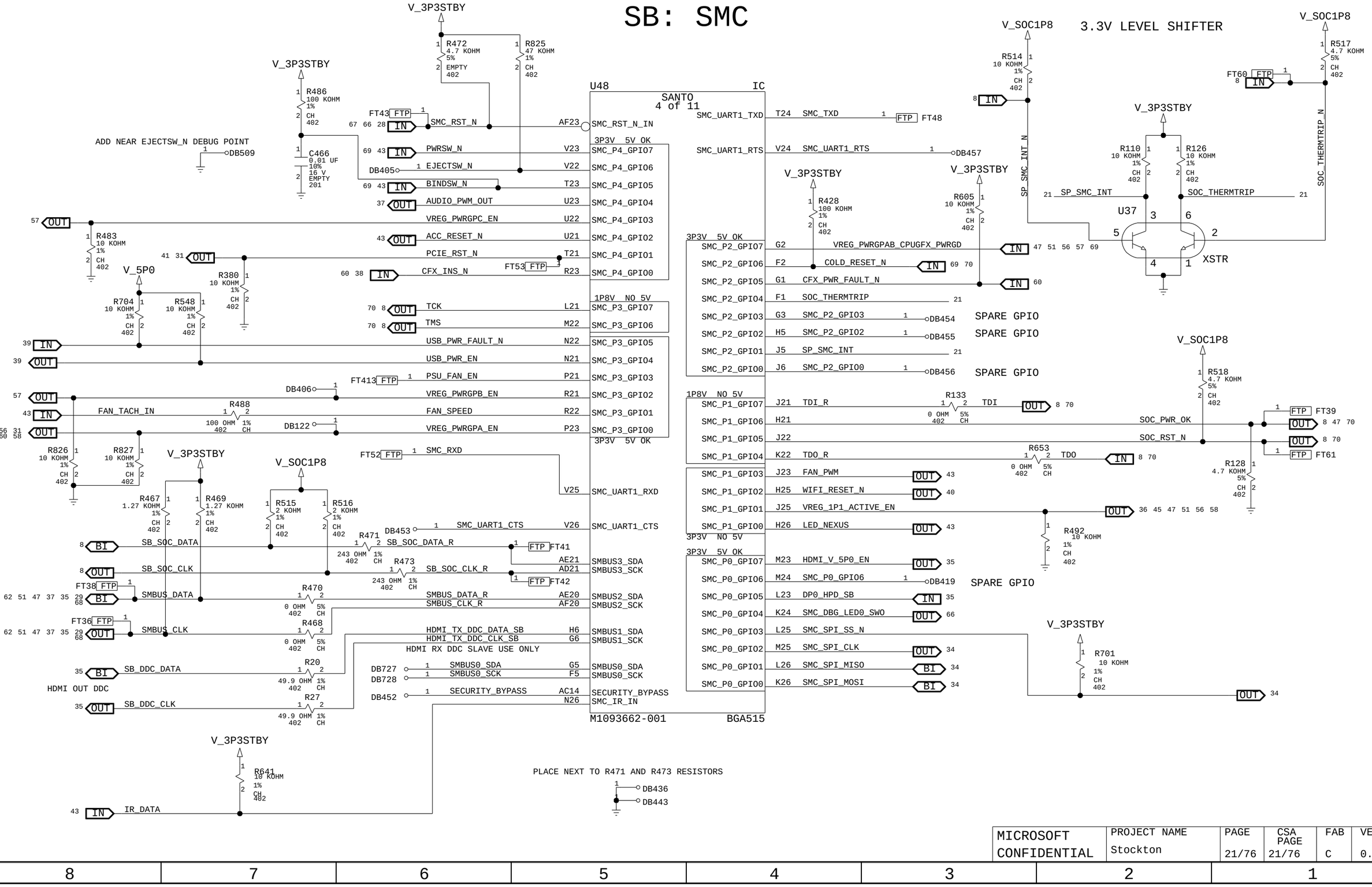






MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	20/76	20/76	C	0.12

SB: SMC



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	21/76	21/76	C	0.12

SB: USB

U48
SANTO
6 of 11
IC

				USBD_D0_DP	AF8	USB2_WIFI_DP	BI	40	WIFI
				USBD_D0_DN	AE8	USB2_WIFI_DN	BI	40	
				USBC_D0_DP	AC4	USB2_AUX_DP	BI	39	REAR 1
				USBC_D0_DN	AC3	USB2_AUX_DN	BI	39	
REAR 1	39 IN	USB3_AUX_RP	Y1 USBC_D1_RXP	USBC_D1_TXP	W3	USB3_AUX_TP_C	C501 1 2 0.1 UF10% 16 V 201 X5R	USB3_AUX_TP OUT 39	
	39 IN	USB3_AUX_RN	Y2 USBC_D1_RXN	USBC_D1_TXN	W4	USB3_AUX_TN_C	C500 1 2 0.1 UF 10% 16 V 201 X5R	USB3_AUX_TN OUT 39	
REAR 0	39 IN	USB3_BP_P1_RP	V1 USBB_D2_RXP	USBB_D2_TXP	U3	USB3_BP_P1_TP_C	C499 1 2 0.1 UF10% 16 V 201 X5R	USB3_BP_P1_TP OUT 39	REAR 0
	39 IN	USB3_BP_P1_RN	V2 USBB_D2_RXN	USBB_D2_TXN	U4	USB3_BP_P1_TN_C	C498 1 2 0.1 UF10% 16 V 201 X5R	USB3_BP_P1_TN OUT 39	
				USBB_D0_DP	AE4	USB2_BP_P1_DP	BI	68	
				USBB_D0_DN	AE3	USB2_BP_P1_DN	BI	68	
				USBB_D1_DP	AD2	USB2_BP_P0_DP	1 DB85		NOT USED
				USBB_D1_DN	AD1	USB2_BP_P0_DN	1 DB84		
NOT USED	DB90 1	USB3_BP_P0_RP	T1 USBB_D3_RXP	USBB_D3_TXP	R3			USB3_BP_P0_TP 1 DB408	
	DB91 1	USB3_BP_P0_RN	T2 USBB_D3_RXN	USBB_D3_TXN	R4			USB3_BP_P0_TN 1 DB15	
				USBA_D2_TXP	AB10	USB3_FP_P0_TP_C	C1097 1 2 0.1 UF10% 16 V 201 X5R	USB3_FP_P0_TP OUT 39	
FRONT	39 IN	USB3_FP_P0_RP	AA8 USBA_D2_RXP	USBA_D2_TXN	AB9	USB3_FP_P0_TN_C	C1096 1 2 0.1 UF 10% 16 V 201 X5R	USB3_FP_P0_TN OUT 39	FRONT
	39 IN	USB3_FP_P0_RN	AA7 USBA_D2_RXN						
				USBA_D0_DP	AC7	USB2_FP_P0_DP	BI	39	
				USBA_D0_DN	AC8	USB2_FP_P0_DN	BI	39	
				USBA_D1_DP	AF6	USB2_ACC_DP	BI	43	FRONT PANEL ACC
				USBA_D1_DN	AF5	USB2_ACC_DN	BI	43	
NOT USED	DB409 1	USB3_ACC_RP	AB1 USBA_D3_RXP	USBA_D3_TXP	AA3			USB3_ACC_TP 1 DB20	NOT USED
	DB17 1	USB3_ACC_RN	AB2 USBA_D3_RXN	USBA_D3_TXN	AA4			USB3_ACC_TN 1 DB22	

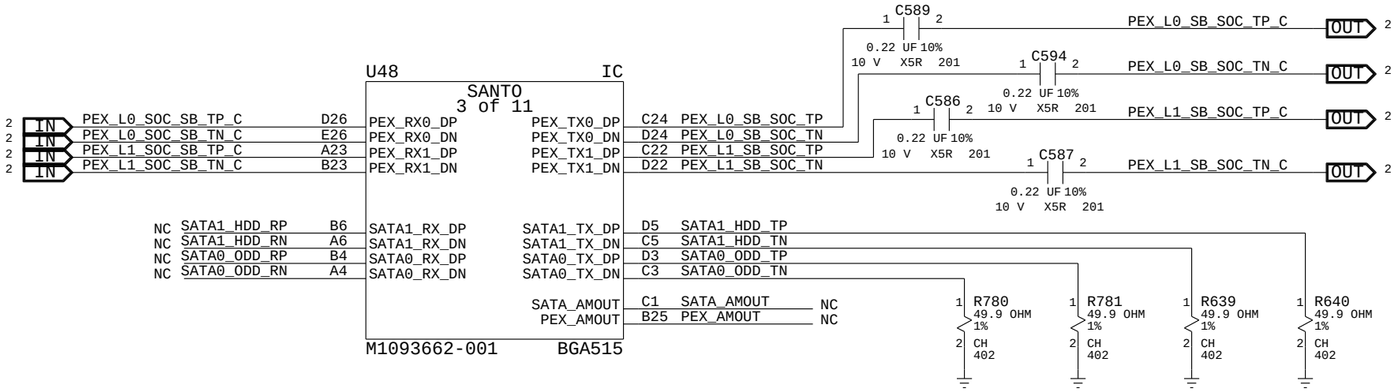
USBA_D2_AMOUT	AA5	NC
USBA_D1_AMOUT	AE6	
USBA_D0_AMOUT	AC11	
USBB_D2_AMOUT	R5	
USBB_D1_AMOUT	AD5	
USBB_D0_AMOUT	AF4	
USBC_D1_AMOUT	W5	
USBC_D0_AMOUT	AC5	
USBD_D0_AMOUT	AE9	

USBA_D1_TXRTUNE
1 R724 174 OHM 1% 2 CH 402
AB11 USBA_D1_TXRTUNE

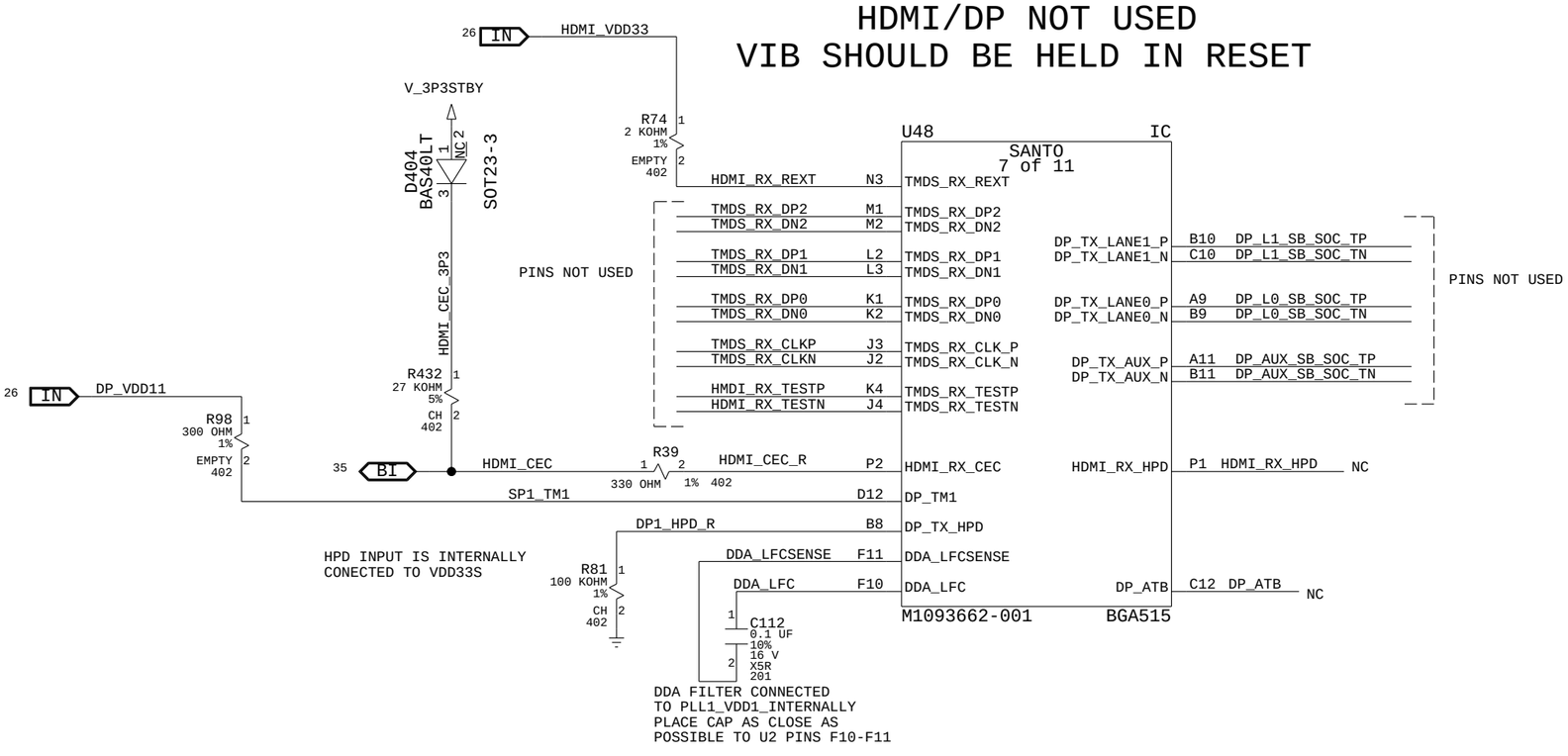
M1093662-001 BGA515

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	22/76	22/76	C	0.12

SB: PCIEX, SATA, VIDEO

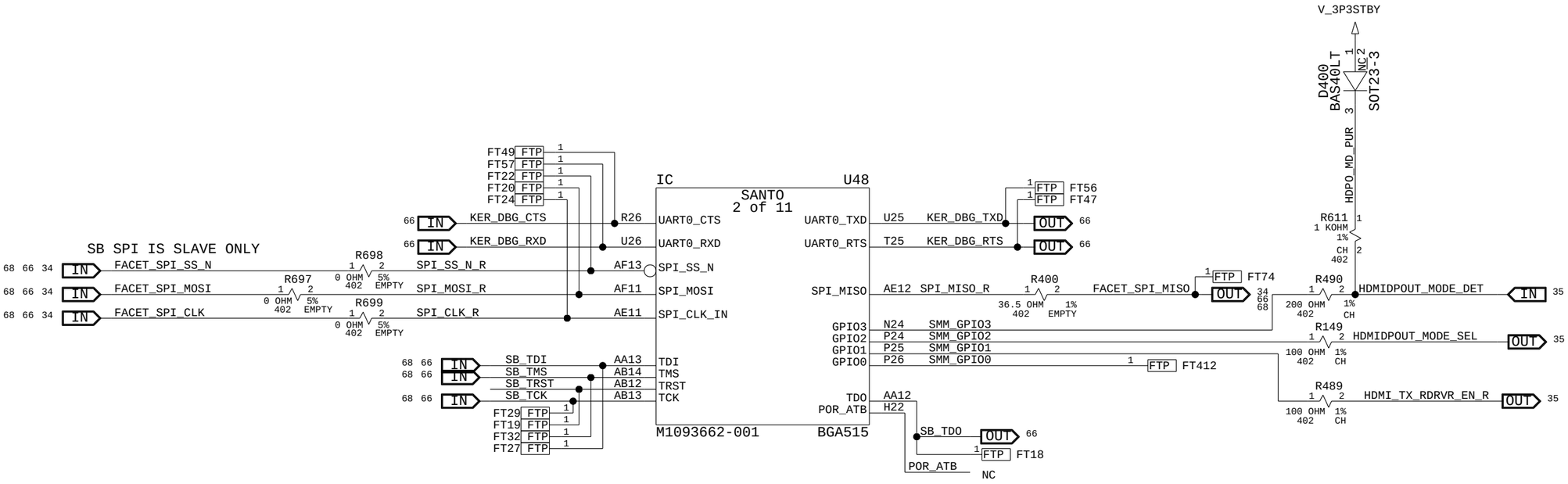


HDMI/DP NOT USED
VIB SHOULD BE HELD IN RESET



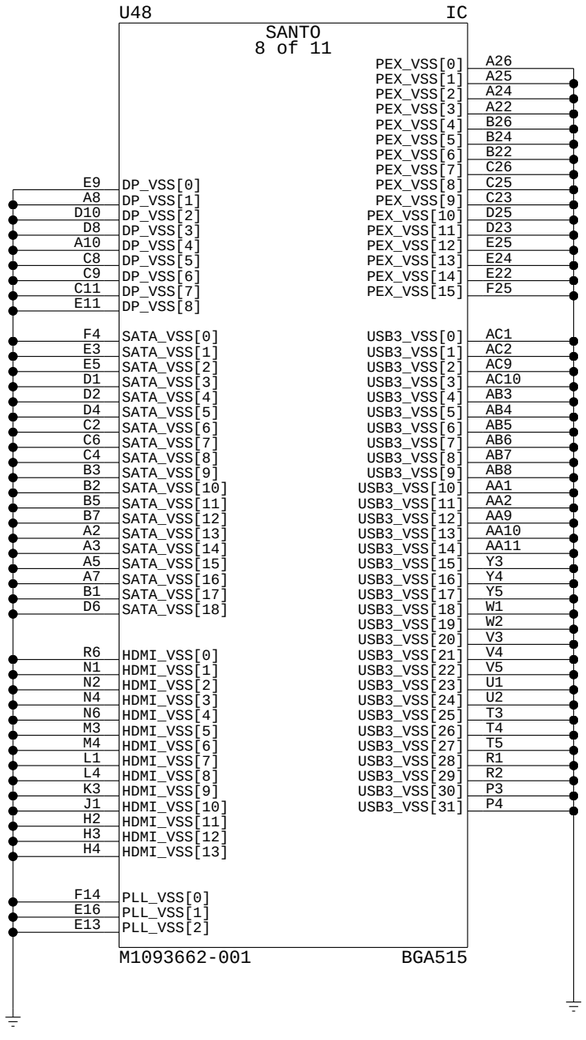
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	23/76	23/76	C	0.12

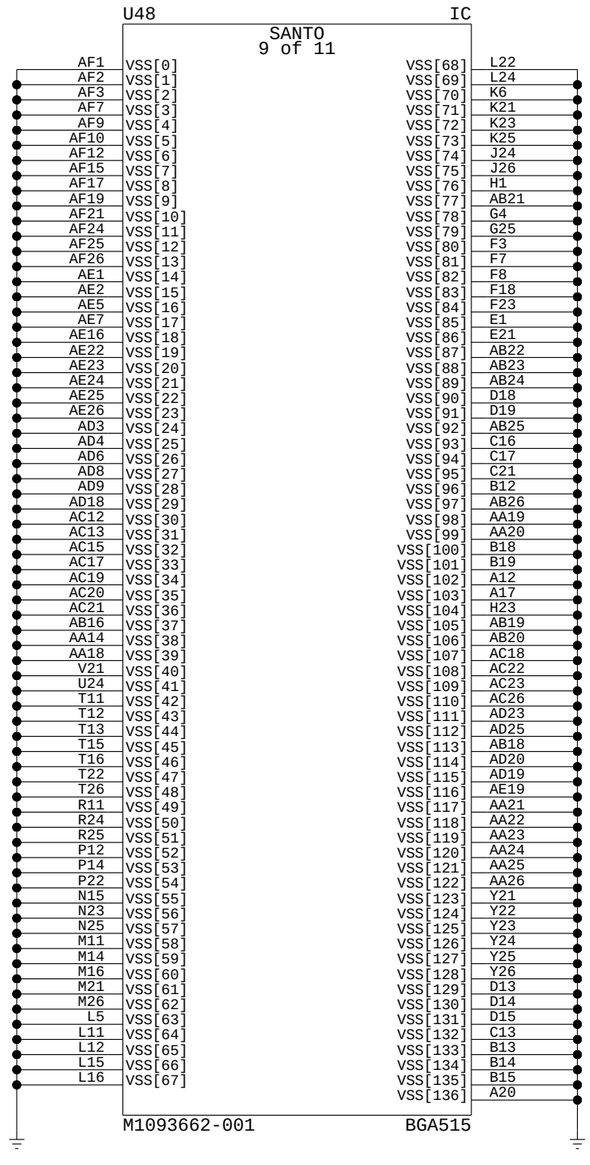
SB: SMM UART, SPI, JTAG, GPIO



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	24/76	24/76	C	0.12

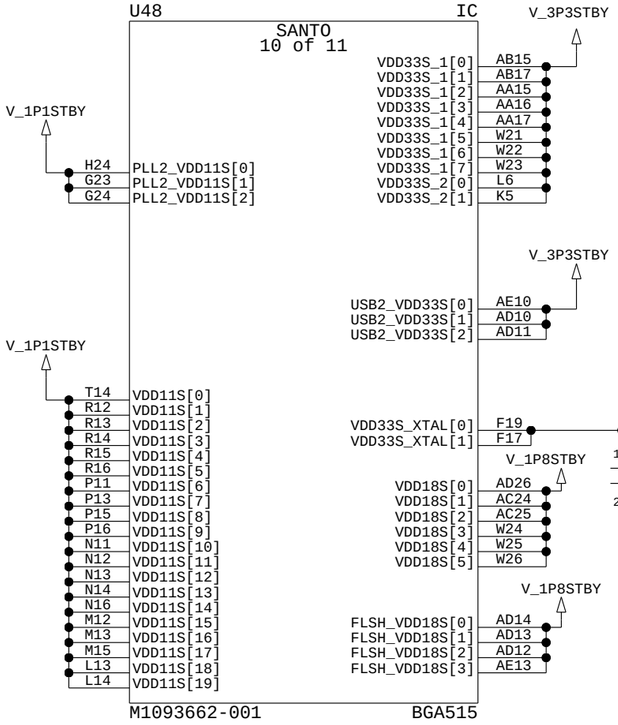
SB: POWER (VSS)



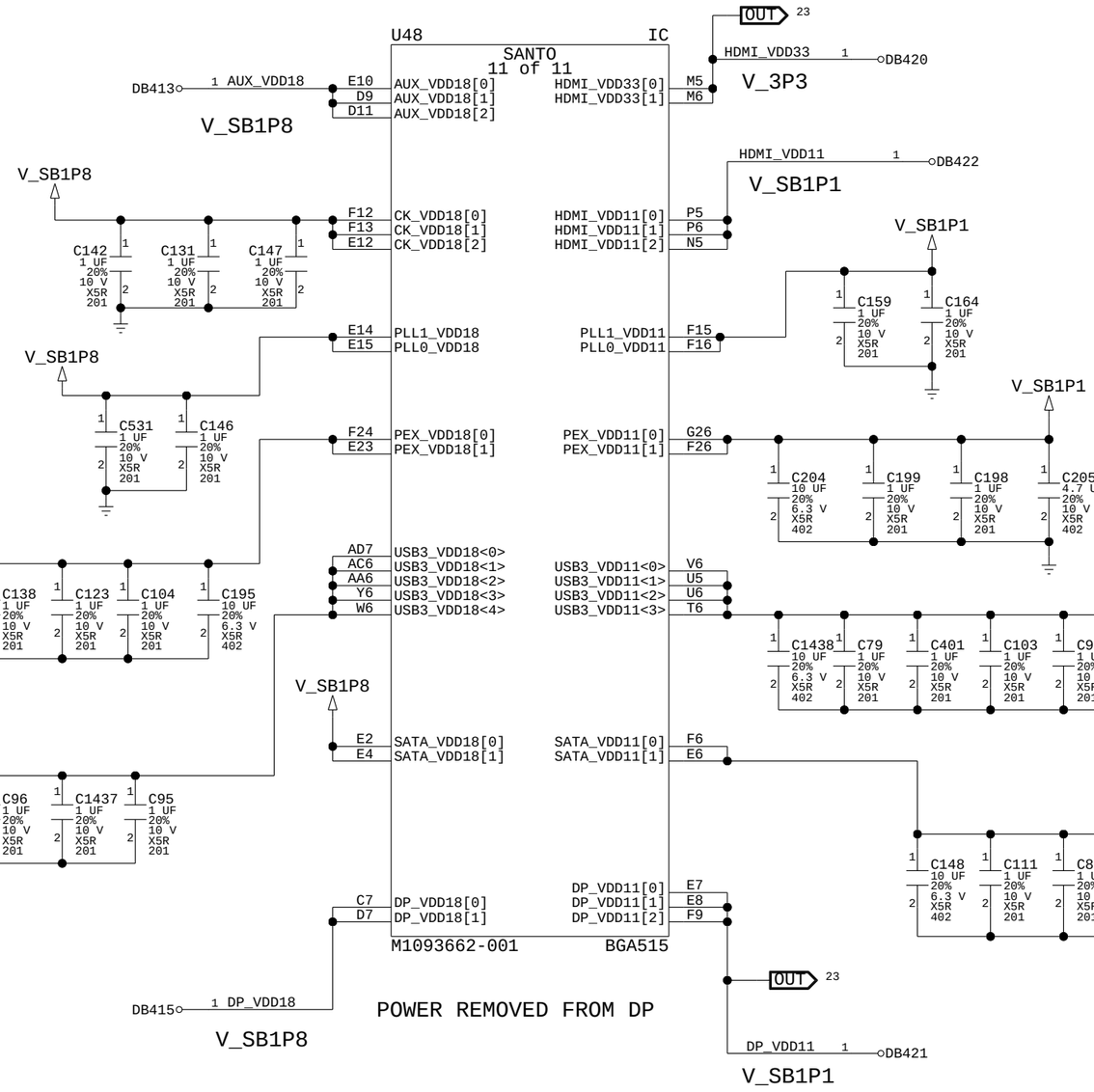


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	25/76	25/76	C	0.12

SB: POWER



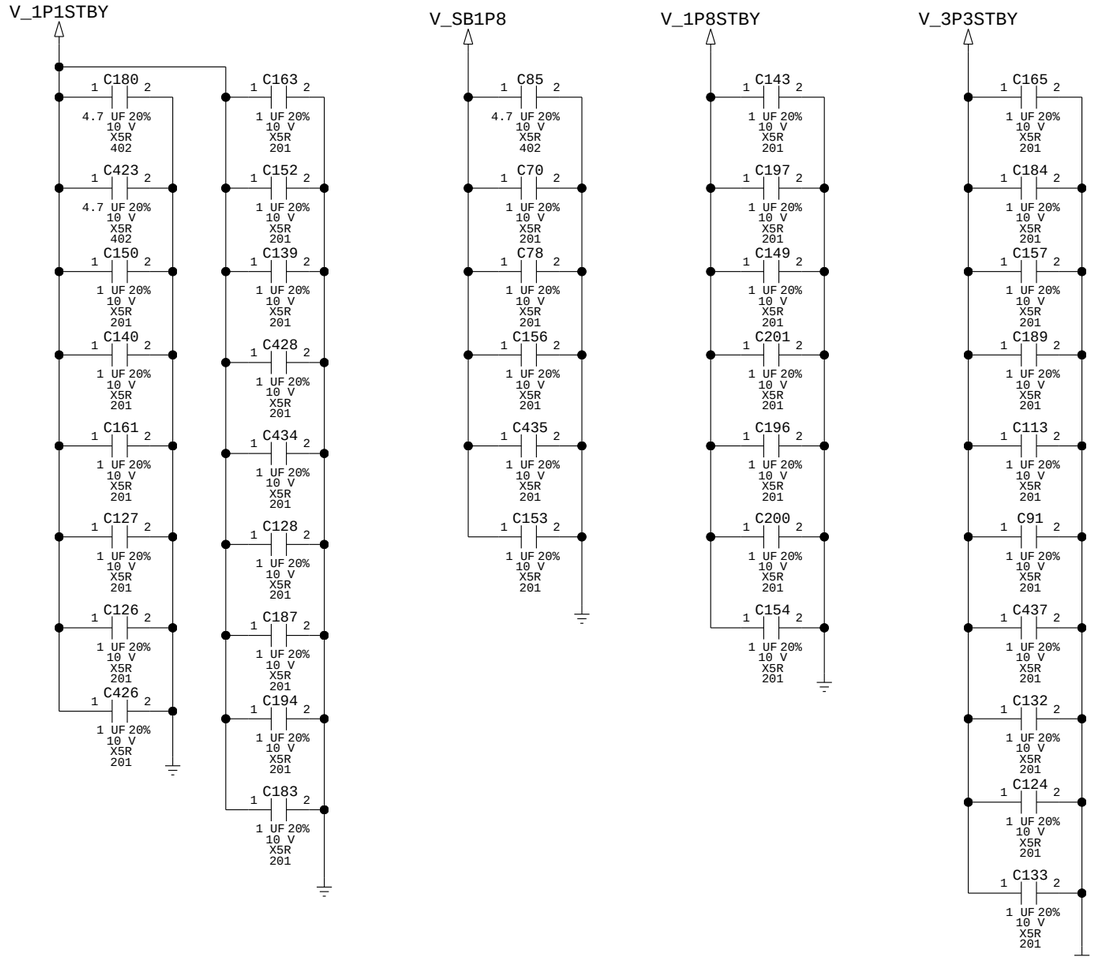
POWER REMOVED FROM AUX AND HDMI



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	26/76	26/76	C	0.12

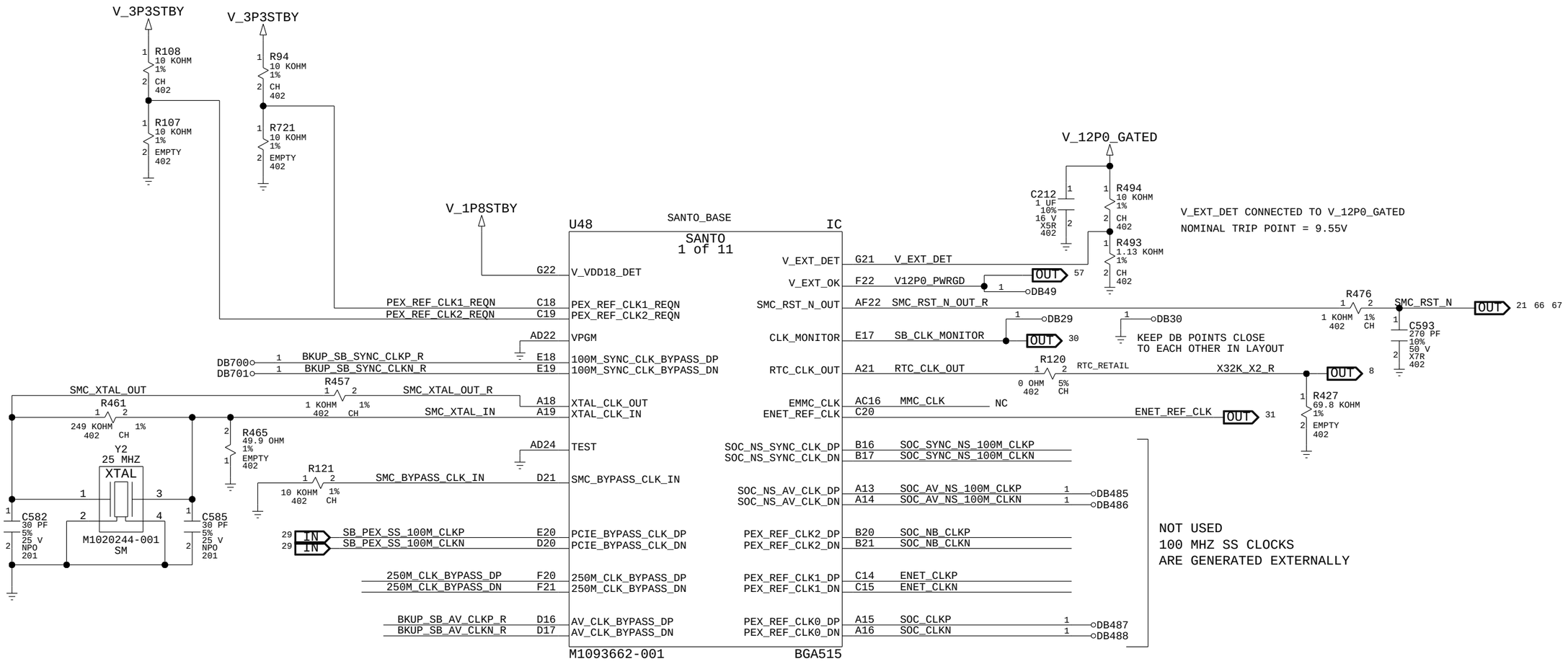
SB: DECOUPLING

NOTE: ALL V_SB1P1 DECOUPLING
IS SHOWN ON POWER PAGE 49



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	27/76	27/76	C	0.12

SB: CLOCKS, STRAPPING, POR



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1093668-001	IC	U48	IC,SANTO SB,BGA515	SANTO_RETAIL
M1093662-001	IC	U48	IC,SANTO SB,BGA515	SANTO_DEV
M1093668-001	EMPTY	U48	IC,SANTO SB,BGA515	SANTO_EMPTY

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	28/76	28/76	C	0.12

CLOCK: PCIE 100MHZ SS

9FGL0651 SMBUS ADDRESS
1101 010 R/W HEX
WRITE 1101 010 0 0XD4
READ 1101 010 1 0XD5

POWER SUBJECT TO REVIEW

85 OHM DIFF OUTPUTS

PLACE 0.1UF CAPS CLOSE TO EACH POWER PINS

PLACE 0.1UF CAPS CLOSE TO EACH POWER PIN

PLACE NEXT TO I2C ISOLATION RESISTORS

PLACE NEXT TO I2C ISOLATION RESISTORS

EN: 450K INTERNAL PU TO VCCA
V_3P3_SS_CLK HAS 10K PD TO GND

I2C BUFFER PREVENTS LEAKAGE PATH FROM SMBUS PULLUPS TO V_3P3_GATED THROUGH CLOCK GENERATORS

R166 = 1K TO ACCOUNT FOR ~60KOHM COMBINED INPUT IMPEDANCE OF CLOCK GENS

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	29/76	29/76	C	0.12

CLOCK: PCIE 100MHZ NS

9FGL04 SMBUS ADDRESS
1101 000 R/W HEX
WRITE 1101 000 0 0XD0
READ 1101 000 1 0XD1

30 V_3P3_NS_CLK
R665 10 KOHM 1% EMPTY 402
R667 10 KOHM 1% EMPTY 402
SS_LEVEL_NS_CLK
R666 10 KOHM 1% CH 402
ADR_SEL_NS_CLK
R668 10 KOHM 1% CH 402
SPREAD SPECTRUM TURNED OFF
29 OUT 25MHZ_REF
R593 49.9 OHM 1% 402 CH
25MHZ REF FOR SPREAD CLOCK GEN

V_3P3_GATED
C1345 1 UF 20% 10 V X5R 201
C1346 0.1 UF 10% 16 V X5R 201
FB4 1000 OHM 200 MA BEAD 402 1 OHM
U2 IC 6V41462
VDD3.3 11
VDD3.3 20
VDDA3.3 16
VDDDIG3.3 7
VDDXTAL3.3 3
C1422 0.1 UF 10% 16 V X5R 201
C92 0.1 UF 10% 16 V X5R 201
C93 0.1 UF 10% 16 V X5R 201
C94 0.1 UF 10% 16 V X5R 201
C1423 10 UF 20% 6.3 V X5R 402
30 V_3P3_NS_CLK
PLACE 0.1UF CAPS CLOSE TO EACH POWER PIN

POWER SUBJECT TO REVIEW

23 VSS_EN_TRI
4 VSADR/REF3.3

R670 0 OHM 402
30 SOC_NS_CLKREQ_N
12 VOE0_N
51 29 IN SOC_REFCLK_EN_N
R669 0 OHM EMPTY 402
30 SPARE_NS_CLKREQ_N
19 VOE1_N
30 NS_CKPWRGD_PD_N
22 CKPWRGD_PD_N
29 IN SMBUS_CLK_BUFFERED
R419 0 OHM 402 CH DEBUG
30 NS_SCLK
8 SCLK_3.3
29 BI SMBUS_DATA_BUFFERED
R435 0 OHM 402 CH DEBUG
30 NS_SDATA
9 SDATA_3.3
1 XIN/CLKIN_25
2 X2
M1092048-001
QFN25

DIF0 13 SOC_PEX_NS_100M_CLKP
DIF0_N 14 SOC_PEX_NS_100M_CLKN
OUT 2
OUT 2
DIF1 17 SPARE_PEX_NS_100M_CLKP 1 DB423
DIF1_N 18 SPARE_PEX_NS_100M_CLKN 1 DB424
GNDA 15
GND1 10
GND2 21
GNDREF 5
GNDXTAL 24
GNDDIG 6
MPAD 25

85 OHM DIFF OUTPUTS

28 IN SB_CLK_MONITOR
R135 0 OHM 402 5% EMPTY
R134 49.9 OHM 1% EMPTY 402
25MHZ CLOCK FROM SB

NS_XTAL_X1
R620 0 OHM 402
NS_XTAL_X1_R
R621 0 OHM 402 EMPTY
NS_XTAL_X2
R105 0 OHM 402
NS_XTAL_X2_R
Y0 25 MHZ XTAL
M1085687-001 SM
C1091 6.8 PF +/-0.5PF 50 V NPO 402
C1335 6.8 PF +/-0.5PF 50 V NPO 402
XTAL_25MHZ_BASE

30 V_3P3_NS_CLK
R671 10 KOHM 1% CH 402
30 SOC_NS_CLKREQ_N
R672 10 KOHM 1% CH 402
30 SPARE_NS_CLKREQ_N
R689 10 KOHM 1% CH 402
30 NS_CKPWRGD_PD_N
RETAIL R114 10 KOHM 1% CH 402
30 NS_SCLK
RETAIL R115 10 KOHM 1% CH 402
30 NS_SDATA

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1115898-001	IC	Y0	XTAL,25MHZ,15PPM,8PF,3.2X2.5MM	XTAL_25MHZ_KDS
M1085687-001	IC	Y0	XTAL,25MHZ,15PPM,8PF,3.2X2.5MM	XTAL_25MHZ_TXC
M1115904-001	IC	Y0	XTAL,25MHZ,15PPM,8PF,3.2X2.5MM	XTAL_25MHZ_NDK

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	30/76	30/76	C	0.12

ETHERNET CONTROLLER

V_3P3_ENET

RF C570 3 PF +/-0.1PF 25 V COG 201
RF C571 3 PF +/-0.1PF 25 V COG 201
RF C572 15 PF 5% 25 V COG 201
RF C573 15 PF 5% 25 V COG 201

BLUE = 1 GBPS LINK
GREEN = 100 MBPS LINK
RED = 10 MBPS LINK

V_3P3_ENET
D1 SM3 DEBUG
BLU
GRN
RED
M1090218-001

ENET_LED2_R — DEBUG R26 511 OHM 1% 402 CH
ENET_LED1_R — DEBUG R33 1 KOHM 1% 402 CH
ENET_LED0_R — DEBUG R17 2 KOHM 1% 402 CH

U47 IC
RTL8111HM
X896524-002 QFN33

MDIP3 9 MDIN3 10 MDIP2 6 MDIN2 7 MDIP1 4 MDIN1 5 MDIP0 1 MDIN0 2 (38 BI)
ENET_LED2 25 LED2
ENET_LED1 26 LED1/GPO
ENET_LED0 27 LED0

28 IN ENET_REF_CLK — R36 100 OHM 1% 402 CH
R35 2.49 KOHM 1% CH 402 — ENET_RSET 31 RSET
ENET_XTAL2 29 CKXTAL2
ENET_XTAL1 28 CKXTAL1
R37 0 OHM 5% 402 EMPTY
ENET_ISOLATE_N 20 ISOLATE_N
2 IN PEX_SOC_ENET_TP_C 13 HSIP
2 IN PEX_SOC_ENET_TN_C 14 HSIN
29 IN ENET_PEX_SS_100M_CLKP 15 REFCLK_P
29 IN ENET_PEX_SS_100M_CLKN 16 REFCLK_N
19 PERST_N

V_3P3_ENET
R365 10 KOHM 1% CH 402
FT9 FTP

41 21 IN PCIE_RST_N

FT2 FTP
V_3P3_ENET
DB78

PLACE 0.1UF CLOSE TO PINS 11, 23 AND 32
PLACE 4.7UF CLOSE TO PINS 11 AND 32
C502 0.1 UF 10% 16 V X5R 201
C482 0.1 UF 10% 16 V X5R 201
C477 0.1 UF 10% 16 V X5R 201
C505 4.7 UF 20% 10 V X5R 402
C1424 4.7 UF 20% 10 V X5R 402

V_3P3_ENET V_3P3_GATED
R791 0 OHM 5% 603 EMPTY

V_1P0_ENET
PLACE 0.1UF CLOSE TO PINS 3, 8, 22 AND 30
C481 0.1 UF 10% 16 V X5R 201
C491 0.1 UF 10% 16 V X5R 201
C485 0.1 UF 10% 16 V X5R 201
C496 0.1 UF 10% 16 V X5R 201
C1425 1 UF 20% 10 V X5R 201
C1428 4.7 UF 20% 10 V X5R 402

AVDD33_2 32
AVDD33_1 11
DVDD10 22
AVDD10_3 30
AVDD10_2 8
AVDD10_1 3
VDDREG 23
REGOUT 24

PLACE 0.1UF CLOSE TO PIN 24
C480 0.1 UF 10% 16 V X5R 201

FTP FT12
DB3

V_3P3_ENET
R366 10 KOHM 1% CH 402

LANWAKE_N 21 ENET_WAKE_N
CLKREQ_N 12 SB_REFCLK_N
OUT 29
USING ENET CLK REQ AS A GLOBAL REQUEST

HSOP 17
HSON 18
PEX_ENET_SOC_TP — C37 0.22 UF 10% 10 V X5R 201 — PEX_ENET_SOC_TP_C OUT 2
PEX_ENET_SOC_TN — C34 0.22 UF 10% 10 V X5R 201 — PEX_ENET_SOC_TN_C OUT 2

MPAD 33

NOM. VOLTAGE: 3.3V
MAX POWER: 590MW

V_12P0
60 IN V_1P65_VREF
60 58 56 21 IN VREG_PWRGPA_EN
U411 LM339 TSSOP14 X932792-001
R759 100 KOHM 1% CH 402
C1495 0.1 UF 10% 25 V X5R 201

V_3P3STBY
Q404 FET SOT23-3 X889117-002
C1496 0.1 UF 10% 25 V X5R 402
V_3P3_ENET_G_R — R761 100 OHM 1% 402 CH
V_3P3_ENET_G
V_3P3_ENET_OUT
C1497 0.1 UF 10% 25 V X5R 402
C1498 10 UF 20% 6.3 V X5R 402
R782 1 KOHM 1% CH 402
DEBUG_SHUNT R760 0 OHM 5% 805 CH
V_3P3_ENET

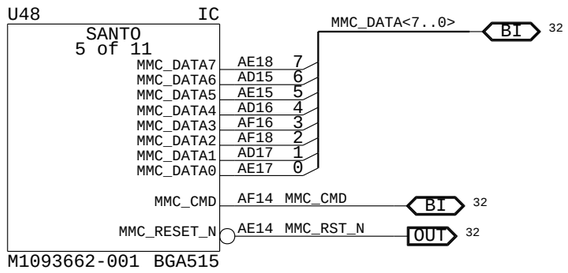
COMPARATOR 1 OF 2:
V_3P3_ENET GATE DRIVE

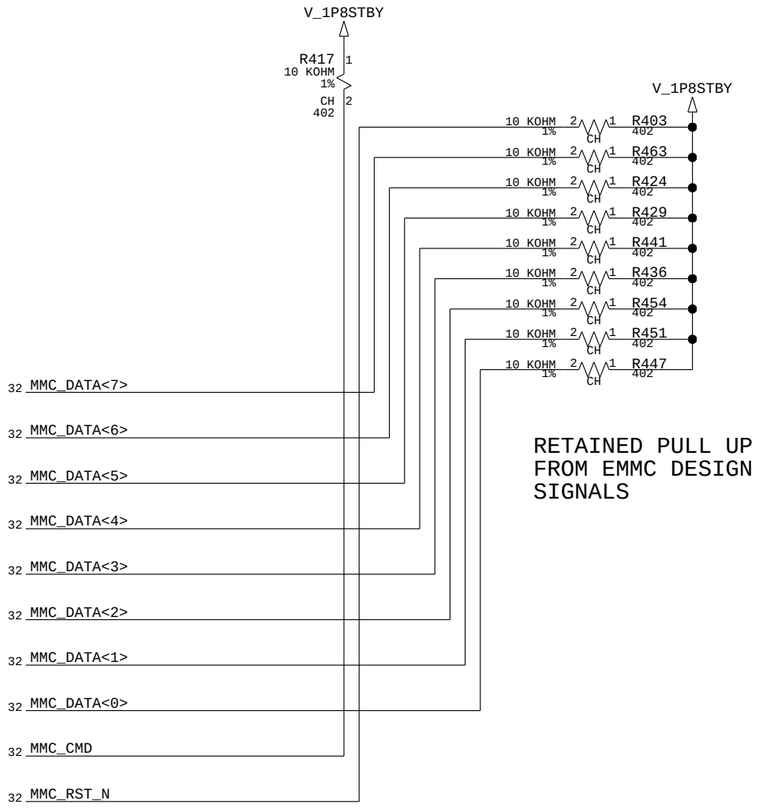
ETHERNET POWER ENABLE CIRCUIT MUST
MEET THE FOLLOWING TIMING REQUIREMENTS
RISE TIME: > 0.5 MS AND < 100 MS
POWER OFF/ON CYCLE TIME: > 50 MS

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	31/76	31/76	C	0.12

SB: EMMC (LEGACY)

EMMC PLACEHOLDER



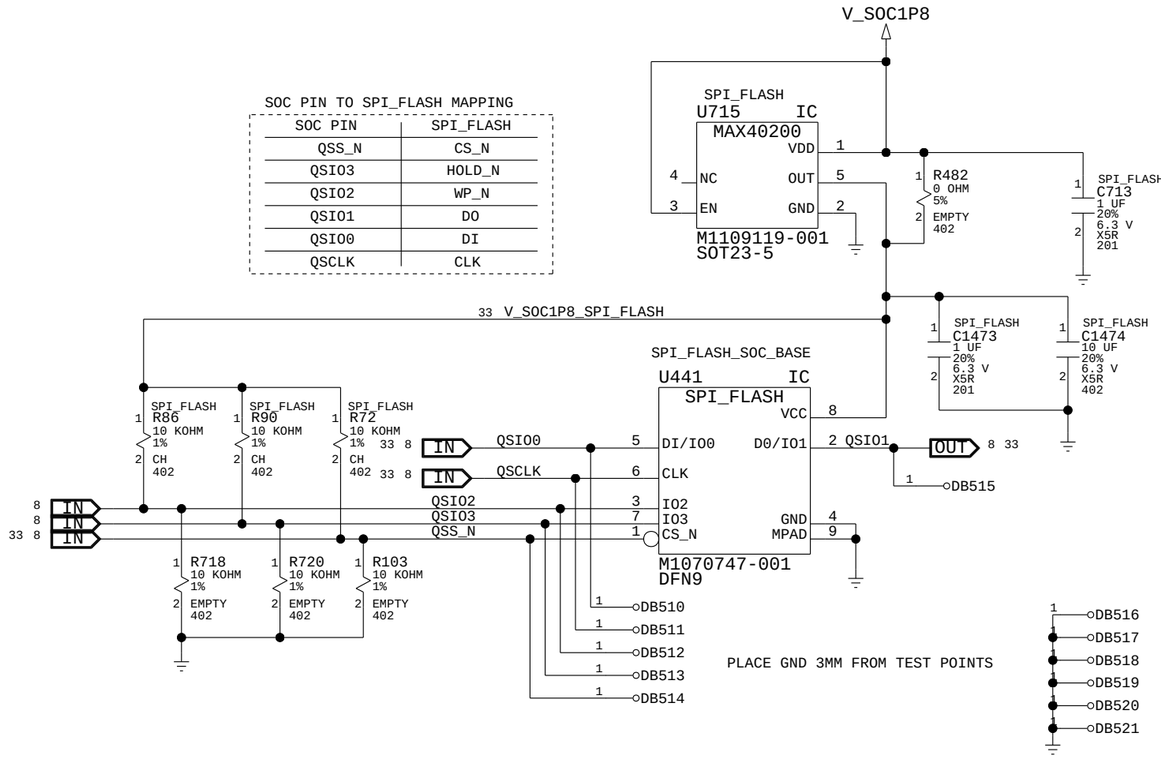


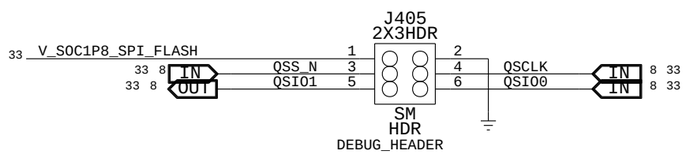
RETAINED PULL UP RESISTORS FROM EMMC DESIGN FOR SANTOS SIGNALS

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	32/76	32/76	C	0.12

MEMORY: SPI FLASH SOC

MAX40200 IDEAL DIODE PROVIDES BACKDRIVE PROTECTION FROM DEDIPROG

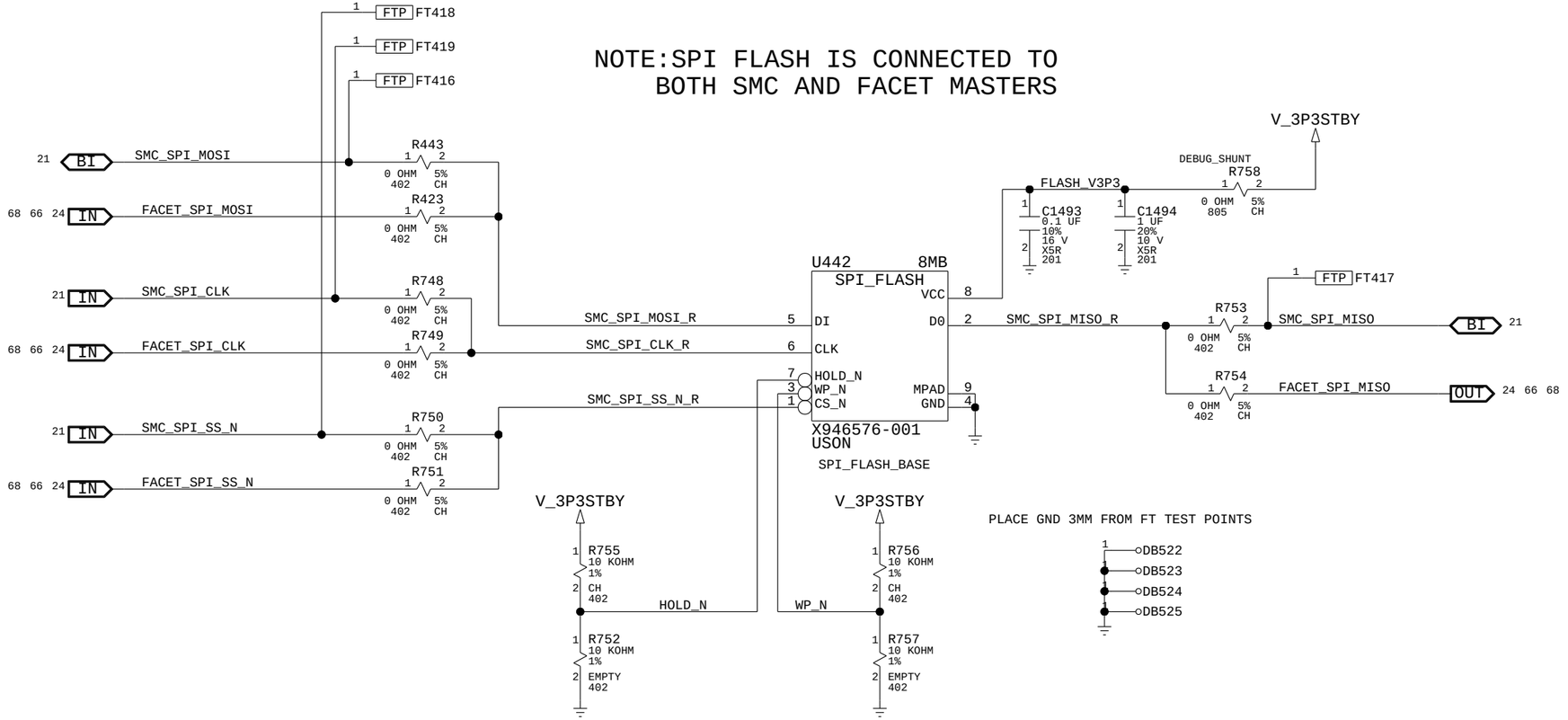




MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1070747-001	IC	U441	FLASH MEMORY,FLASH,256MBIT,SM,WSON8,SERIAL,W/DUAL/QUAD SPI	SPI_FLASH_SOC_WINBOND
M1104466-001	IC	U441	FLASH MEMORY,FLASH,256MBIT,SM,8-WSON,SERIAL,MULTI I/O,DTR,1.8V	SPI_FLASH_SOC_MACRONIX

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	33/76	33/76	C	0.12

MEMORY: SPI FLASH



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
X946576-001	IC	U442	WINBOND,SPI_FLASH,8GBIT,USON	SPI_FLASH_WINBOND
M1090771-001	IC	U442	MACRONIX,SPI_FLASH,8GBIT,USON	SPI_FLASH_MACRONIX

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	34/76	34/76	C	0.12

HDMI: VIDEO OUT

Q621M CONTROL SLAVE ADDRESS		
ADDR0/ADDR1	7-BIT ADDRESS	8-BIT ADDRESS
FLOAT/FLOAT	0X5E	BC/BD

16 AVAILABLE OPTIONS (7-BIT): 0X50 - 0X5E
SEE DATASHEET FOR MORE DETAILS

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1093444-001	IC	U40	HDMI RE-DRIVER PASS1 NB7NQ621M XB7N	HDMI_RDVR_PASS1
M1093444-002	IC	U40	HDMI RE-DRIVER PASS2 NB7NQ621M PB7N	HDMI_RDVR_PASS2
MXXXXXXX-XXX	IC	U40	HDMI RE-DRIVER PASS3 NB7NQ621M NB7N	HDMI_RDVR_PASS3

PLACE NEXT TO I2C ISOLATION RESISTORS

DB414
DB416

HDMI_RDVR_BASE
U40 IC
NB7NQ621M
1 OF 3
CONTROL
M1093444-001
QFN39

SMBUS_CLK
SMBUS_DATA
HDMI_TX_RDRVR_SCL_CTL
HDMI_TX_RDRVR_SDA_CTL
HDMI_TX_RDRVR_EN
HDMI_TX_RDRVR_EN_R
FT15 FTP

R28 0 OHM 5% 402 CH
R29 0 OHM 5% 402 CH
R30 0 OHM 5% 402 CH
R31 10 KOHM 1% 2 CH 402
C39 0.1 UF 10% 16 V EMPTY 201

OS/SCL
FG/SDA
EN
I2C_EN
EQ0/ADDR0
EQ1/ADDR1
MODE
LANE_SWAP

HDMI_TX_RDRVR_I2C_EN
HDMI_TX_RDRVR_ADDR0
HDMI_TX_RDRVR_ADDR1
HDMI_TX_RDRVR_MODE
HDMI_TX_RDRVR_LANE_SWAP

V_3P3STBY_HDMI

STRAP CONFIG: HIGH FLOAT FLOAT FLOAT LOW

R183 R552 R693 R559 R568 0 OHM 5% CH 402
R541 R692 R694 R560 R700 0 OHM 5% EMPTY 402 / CH 402

TMDS_TX_DP2 C52 0.1 UF 10% 16 V X5R 201 TMDS_TX_DP2_C
TMDS_TX_DN2 C49 TMDS_TX_DN2_C
TMDS_TX_DP1 C57 TMDS_TX_DP1_C
TMDS_TX_DN1 C55 TMDS_TX_DN1_C
TMDS_TX_DP0 C38 TMDS_TX_DP0_C
TMDS_TX_DN0 C36 TMDS_TX_DN0_C
TMDS_TX_CLKP C45 TMDS_TX_CLKP_C
TMDS_TX_CLKN C42 TMDS_TX_CLKN_C

HDMI_RDVR_BASE
U40 IC
NB7NQ621M
2 OF 3
HDMI
M1093444-001
QFN39

A_RXP A_RXN B_RXP B_RXN C_RXP C_RXN D_RXP D_RXN
A_TXP A_TXN B_TXP B_TXN C_TXP C_TXN D_TXP D_TXN
AUXP AUXN
HPD_SRC HPD_SNK
NC 38
NC 33 NC 32 NC 19

HDMI_TX_RDRVR_HPD

R533 0 OHM 5% 2 CH 402

V_3P3STBY_HDMI

C192 C504 C705 C707 C708 C709 0.1 UF 10% 16 V X5R 201
C506 22 PF 2% 50 V NP0 201
C706 1000 PF 10% 50 V EMPTY 201
C507 0.01 UF 10% 100 V EMPTY 201
C510 10 UF 20% 6.3 V X5R 201
C511 22 UF 20% 6.3 V EMPTY 201

HDMI_RDVR_BASE
U40 IC
NB7NQ621M
3 OF 3
POWER
M1093444-001
QFN39

VCC VCC VCC VCC VCC
GND GND GND GND MPAD

V_3P3STBY
V_5P0
C25 4.7 UF 20% 10 V X5R 402
C478 0.1 UF 10% 16 V X5R 201

V_3P3STBY
R50 2 KOHM 1% 2 CH 402
R54 2 KOHM 1% 2 CH 402

SB_DDC_CLK
SB_DDC_DATA
R52 0 OHM 5% CH 402
R51 0 OHM 5% CH 402
HDMI_TX_SCL_R
HDMI_TX_SDA_R

SOC_DDC_CLK
SOC_DDC_DATA
C24 0.1 UF 10% 16 V X5R 201
C15 0.1 UF 10% 16 V X5R 201
SOC_AUXP
SOC_AUXN

U21 IC
HDMIDP1_5F6
M1004155-002
WLCSP18

VDD_5V VDD_IC
R_SCL_IC R_SDA_IC
AUX_P SCL_IC
AUX_N SDA_IC
HPD_IC SELECT_IC ENABLE_IC
CEC SCL SDA 5V_OUT HPD GND GND

HDMI 5V LOAD SWITCH: 5V, 250MA MAX TDC
DP PWR LOAD SWITCH: 3.3V, 500MA MAX TDC

DP0_HPD
DP0_HPD_SB
R382 0 OHM 5% 402 CH

HDMIDPOUT_MODE_SEL
HDMI_V_5P0_EN
FT6 FTP
R48 10 KOHM 1% 2 CH 402
R148 10 KOHM 1% 2 CH 402

HDMI_TX_SCL_BUF
HDMI_TX_SDA_BUF
R19 0 OHM 5% CH 402
R18 0 OHM 5% CH 402
C14 2.2 UF 20% 6.3 V X5R 201

EG690 EG689 EG688 EG41 DIO SM M1015860-001
EG702 EG701 EG696 EG695 DIO SM M1015860-001

J401 CONN
HDMI_19P_10MH
M1097399-001 SM

TMDS_TX_DP2_CONN
TMDS_TX_DN2_CONN
TMDS_TX_DP1_CONN
TMDS_TX_DN1_CONN
TMDS_TX_DP0_CONN
TMDS_TX_DN0_CONN
TMDS_TX_CLKP_CONN
TMDS_TX_CLKN_CONN
HDMI_CEC
HDMIDPOUT_MODE_DET
HDMI_TX_SCL_CONN
HDMI_TX_SDA_CONN
V_5P0_HDMI_OUT
HDMI_TX_HPD_CONN

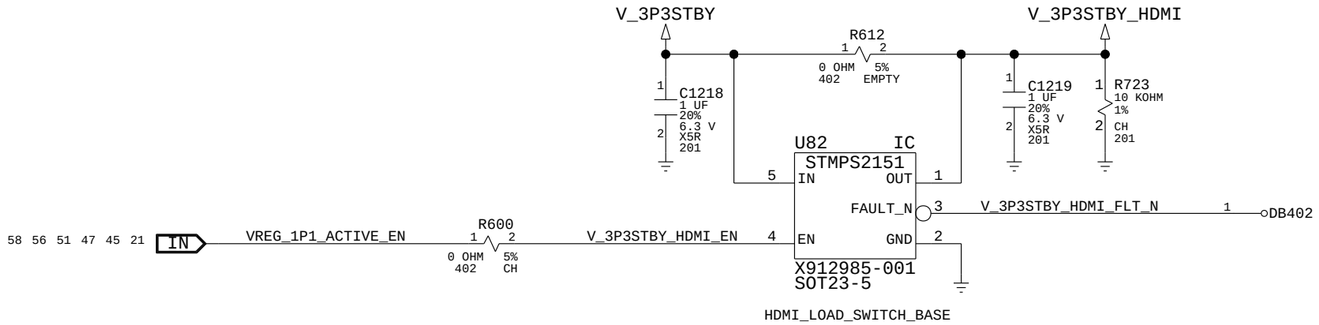
TMDS_DATA2_DP TMDS_DATA2_SHD TMDS_DATA2_DN TMDS_DATA1_DP TMDS_DATA1_SHD TMDS_DATA1_DN TMDS_DATA0_DP TMDS_DATA0_SHD TMDS_DATA0_DN TMDS_CLK_DP TMDS_CLK_SHD TMDS_CLK_DN CEC UTILITY SCL SDA DDC/CEC_GND +5V_POWER HOT_PLUG_DET

EG24 X882235-001 DIO 402

V_3P3STBY_HDMI
RF C563 3 PF +/-0.1PF 25 V COG 201
RF C564 3 PF +/-0.1PF 25 V COG 201
RF C565 15 PF 5% 25 V COG 201
RF C566 15 PF 5% 25 V COG 201

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	35/76	35/76	C	0.12

HDMI: LOAD SWITCHES

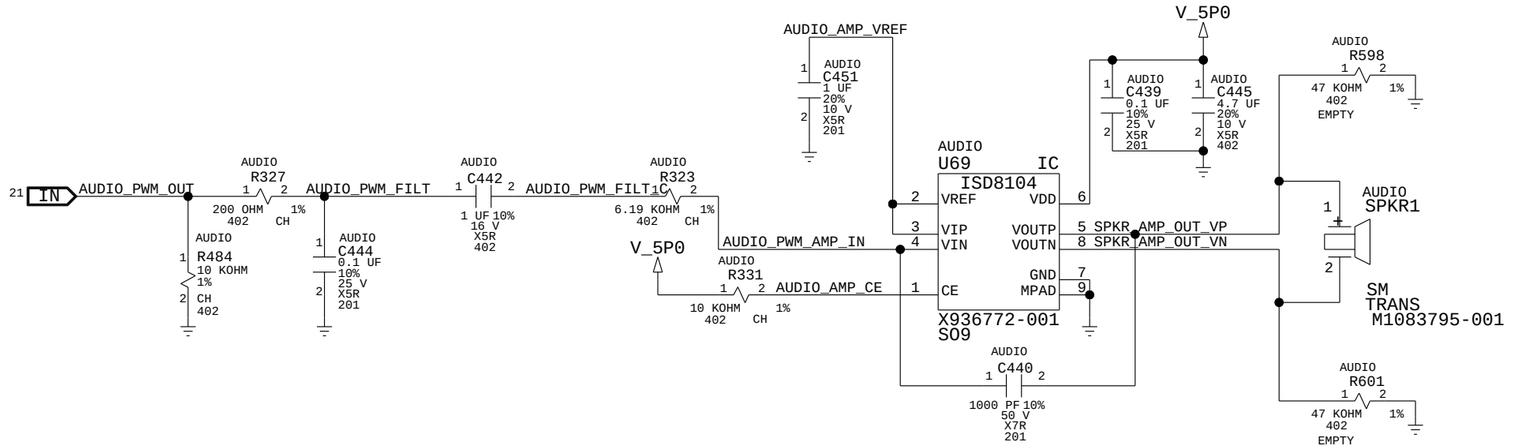


HDMI_LOAD_SWITCH_BASE

U82 IS MITIGATION FOR HDMI TMDS BACK-DRIVE CURRENT THROUGH Q621M RE-DRIVER

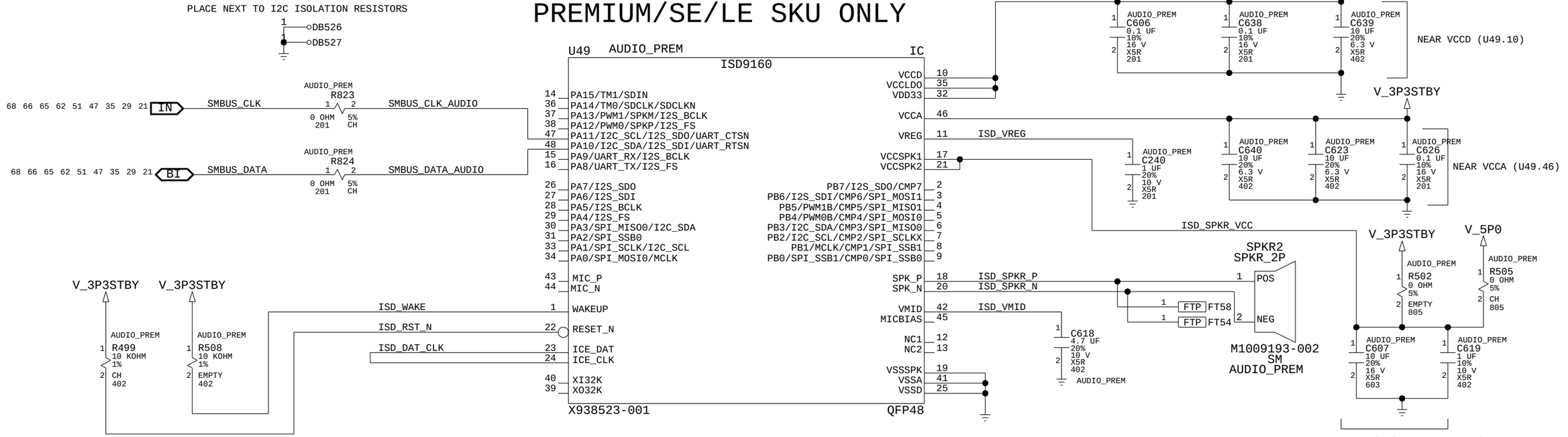
MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
X912985-001	IC	U82	IC,SM,SOT23-5,STMPS2151STR,PWR SW,1CH,0.5A	HDMI_LOAD_SWITCH_ST
X862402-001	IC	U82	IC,SM,SOT23-5,TPS2065DBVR,HI SIDE SW,1.5A	HDMI_LOAD_SWITCH_TI
X934019-001	IC	U82	IC,SM,SOT23-5,AP2151D,PWR SW,1CH,0.5A,DIODES QUAL	HDMI_LOAD_SWITCH_DIODES

AUDIO: PREMIUM AND RETAIL



PLACE NEXT TO I2C ISOLATION RESISTORS

PREMIUM/SE/LE SKU ONLY



ISD9160FIMS05 - REMOVED CAP TOUCH FUNCTIONALITY

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	VER
	Stockton	37/76	37/76	0.12

CONN: RJ45, SPDIF, CFEXPRESS

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1087814-001	CONN	J13	FOXCONN RJ45 CONNECTOR	CON_RJ45_FOXC
MXXXXXX-001	CONN	J13	AMPHENOL QUAL RJ45 CONNECTOR	CON_RJ45_AMP

J13 CONN
RJ45_10P_4MH
M1097403-001
TH

MDIP0 TD1_P 1
MDIN0 TD1_N 2
MDIP1 TD2_P 3
MDIN1 TD2_N 4
MDIP2 TD3_P 7
MDIN2 TD3_N 8
MDIP3 TD4_P 9
MDIN3 TD4_N 10
RJ45_CT CT1 5, CT2 6
MT1 11, MT2 12, MT3 13, MT4 14
C28 0.01 UF 10% 16 V X5R 201

V_3P3_GATED
R164 1 KOHM 1% CH 402
SPDIF_DETECT
Q166 FET SOT23-3
R165 0 OHM 5% 402 EMPTY
1 SPDIF_DETECT_N_R
R495 100 KOHM 1% CH 402
R497 1 KOHM 1% CH 402
C438 0.1 UF 10% 10 V X5R 201
EG1 X882235-001 DIO 402
C443 22 PF 2% 50 V NP0 201
R805 0 OHM 5% 603 CH DEBUG
3V_SPDIF_OUT
C1268 1 UF 20% 10 V X5R 201
C1269 10 UF 20% 6.3 V X5R 402
SPDIF_DETECT_N
SPDIF_OUT
EG20 X882235-001 EMPTY 402
C8 22 PF 2% 50 V NP0 201

J7 CONN
SPDIF_4P_10MH
M1097402-001
TH
VCC
DETECT
VIN
GND
MH

Q166 PROVIDES LOGIC INVERSION
SPDIF DETECT IS ACTIVE LOW
SOC REQUIRES ACTIVE HIGH

EG9
EMPTY
SP3010
MDIP2 D1A 1, D1B 10
MDIN2 D2A 2, D2B 9
MDIP3 D3A 4, D3B 7
MDIN3 D4A 5, D4B 6
GNDA 3, GNDB 8
CONNECT As TO Bs
X863136-001
DFN10

EG10
EMPTY
SP3010
MDIP0 D1A 1, D1B 10
MDIN0 D2A 2, D2B 9
MDIP1 D3A 4, D3B 7
MDIN1 D4A 5, D4B 6
GNDA 3, GNDB 8
CONNECT As TO Bs
X863136-001
DFN10

PEX_L1_SOC_CFX_TN_C
PEX_L1_SOC_CFX_TP_C
EG7 EMPTY SM M1015860-001
EG12 EMPTY SM M1015860-001

PEX_L1_CFX_SOC_TN
PEX_L1_CFX_SOC_TP
EG8 EMPTY SM M1015860-001
EG408 EMPTY SM M1015860-001

CFX_PEX_SS_100M_CLKN
CFX_PEX_SS_100M_CLKP
EG406 EMPTY SM M1015860-001
EG409 EMPTY SM M1015860-001

PEX_L0_SOC_CFX_TN_C
PEX_L0_SOC_CFX_TP_C
EG407 EMPTY SM M1015860-001
EG410 EMPTY SM M1015860-001

PEX_L0_CFX_SOC_TN
PEX_L0_CFX_SOC_TP
EG11 EMPTY SM M1015860-001
EG411 EMPTY SM M1015860-001

CFX_PERST_N
CFX_CLKREQ_N
EG2 EMPTY SM M1015860-001
EG6 EMPTY SM M1015860-001

V_3P3_CFX
EMPTY U132
NCP803
VCC
RESET_N
GND
M1095945-001
SOT23-3
C1452 0.1 UF 10% 10 V EMPTY 201
2 CFX_PERST_MONITOR_N
R695 0 OHM 5% 402 EMPTY
R104 10 KOHM 1% CH 402
R789 100 KOHM 1% 2 EMPTY 402
CFX_PERST_GPIO_N
R783 0 OHM 5% 402 CH

V_3P3_CFX_IN
C1444 22 UF 20% 6.3 V X5R 603
C1758 22 UF 20% 6.3 V X5R 603
C1456 10 UF 20% 6.3 V X5R 402
C1454 1 UF 20% 10 V X5R 201
DB433
EG86 EMPTY SM M1015860-001

CFX_ISENSE_P
DEBUG_SHUNT
R211 PWR
CURN SENSING PWR RESISTOR
E1 E1 E2 E2 CFX_ISENSE_N
I1 I1 I2 I2
0.01 OHM 1/2W 0.5% X867966-001 1206

RF FILTER CAPS
V_3P3_CFX_IN
RF C1457 15 PF 5% 25 V C0G 201
RF C1458 15 PF 5% 25 V C0G 201
RF C1459 15 PF 5% 25 V C0G 201
RF C1460 3 PF +/-0.1PF 25 V C0G 201
RF C1462 3 PF +/-0.1PF 25 V C0G 201

PEX_L1_CFX_SOC_TN
PEX_L1_CFX_SOC_TP
PEX_L1_SOC_CFX_TN_C
PEX_L1_SOC_CFX_TP_C
CFEXPRESS
2.5A EDC
1.55A TDC
R696 0 OHM 5% 402 CH
CFX_RSV1
CFX_PERST_N
CFX_CLKREQ_N
CFX_INS_N
CFX_PEX_SS_100M_CLKN
CFX_PEX_SS_100M_CLKP
PEX_L0_CFX_SOC_TN
PEX_L0_CFX_SOC_TP
PEX_L0_SOC_CFX_TN_C
PEX_L0_SOC_CFX_TP_C

J3 CONN
CF_EXPRESS
M1097401-002
SM
GND PER1_N PER1_P GND PET1_N PET1_P RESERVED RESERVED PERST_N +3.3V CLKREQ_N INS_N REFCLK- REFCLK+ GND PER0_N PER0_P GND PET0_N PET0_P GND MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8 MH9 MH10 MH11
MH12 MH13 MH14 MH15 MH16 MH17 MH18 MH19 MH20 MH21 MH22 MH23 MH24 MH25 MH26 MH27 MH28 MH29 MH30 MH31 MH32 MH33 MH34 MH35 MH36 MH37 MH38 MH39 MH40 MH41 MH42 MH43

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	38/76	38/76	C	0.12

CONN: USB (FRONT & REAR)

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1087813-001	CONN	J14,J15	FOXCONN USB CONNECTOR	CON_USB_FOXC
MXXXXXXX-001	CONN	J14,J15	AMPHENOL QUAL USB CONNECTOR	CON_USB_AMP

EG4
ESD ARRAY
SP3010
X863136-001
DFN10

39 22 BI USB3_AUX_RN — 1 D1A, 10 D1B
39 22 BI USB3_AUX_RP — 2 D2A, 9 D2B
39 22 BI USB2_AUX_DP — 4 D3A, 7 D3B
39 22 BI USB2_AUX_DN — 5 D4A, 6 D4B
GNDA 3, GNDB 8
CONNECT As TO Bs

PINS SWAPPED TO SUPPORT PLACEMENT ON BOTTOM

EG5
ESD ARRAY
SP3010
X863136-001
DFN10

68 39 BI USB2_BP_P1_IN_DN — 1 D1A, 10 D1B
68 39 BI USB2_BP_P1_IN_DP — 2 D2A, 9 D2B
39 22 BI USB3_BP_P1_RP — 4 D3A, 7 D3B
39 22 BI USB3_BP_P1_RN — 5 D4A, 6 D4B
GNDA 3, GNDB 8
CONNECT As TO Bs

EG27
ESD ARRAY
SP3010
X863136-001
DFN10

39 22 BI USB2_FP_P0_DN — 1 D1A, 10 D1B
39 22 BI USB2_FP_P0_DP — 2 D2A, 9 D2B
39 22 BI USB3_FP_P0_RP — 4 D3A, 7 D3B
39 22 BI USB3_FP_P0_RN — 5 D4A, 6 D4B
GNDA 3, GNDB 8
CONNECT As TO Bs

V_5P0
USB_LOAD_SWITCH_BASE
U717 IC
TPS2001D
M1089559-001
SOT23-5
IN 5, OUT 1, FLT_N 3, EN 4, GND 2
C1371 0.1 UF 10% 25 V X5R 201
39 21 IN USB_PWR_EN
39 V_5P0_USB3_P1
USB_PWR_FAULT_N OUT 21 39
USB PORT PROTECTION

C67 150 UF 20% 6.3 V POLY SM
C65 470 PF 10% 25 V X7R 201
C63 4.7 UF 20% 10 V X5R 402

PINS SWAPPED TO SUPPORT PLACEMENT ON BOTTOM
POLARITY INSENSITIVE

39 22 BI USB2_AUX_DN
39 22 BI USB2_AUX_DP
39 22 OUT USB3_AUX_RN
39 22 OUT USB3_AUX_RP
100 MA 9 OHM

FILT U76
ECMF02_2HSMX6
X900532-002
DFN6
22 IN USB3_AUX_TN — D+_IC
22 IN USB3_AUX_TP — D-_IC
GND
D+_CONN, D-_CONN, NC 4 NC
USB3_AUX_TN_CMC
USB3_AUX_TP_CMC

J14 CONN
USB3_9P_18MH
M1097400-001
TH
TX/RX FROM HOST PERSPECTIVE
VBUS 1, D- 2, D+ 3, GND 4, STDA_SSRX_N 5, STDA_SSRX_P 6, GND_DRAIN 7, STDA_SSTX_N 8, STDA_SSTX_P 9
MH 10–27

REAR 1
(FORMERLY KINECT)
39 V_5P0_USB3_P1
C540 3 PF +/-0.1PF 25 V COG 201
C543 3 PF +/-0.1PF 25 V COG 201
C546 15 PF 5% 25 V COG 201
C549 15 PF 5% 25 V COG 201

68 39 BI V_5P0_USB3_P0
V_5P0
USB_LOAD_SWITCH_BASE
U431 IC
TPS2001D
M1089559-001
SOT23-5
USB_DEBUG_FTDI
C1690 1 UF 20% 10 V X5R 201
C1397 0.1 UF 10% 25 V X5R 201
IN 5, OUT 1, FLT_N 3, EN 4, GND 2
USB_PWR_FAULT_N OUT 21 39

C68 150 UF 20% 6.3 V POLY SM
C64 470 PF 10% 25 V X7R 201
C62 4.7 UF 20% 10 V X5R 402

68 39 BI USB2_BP_P1_IN_DN
68 39 BI USB2_BP_P1_IN_DP
39 22 OUT USB3_BP_P1_RN
39 22 OUT USB3_BP_P1_RP

FILT U75
ECMF02_2HSMX6
X900532-002
DFN6
22 IN USB3_BP_P1_TN — D+_IC
22 IN USB3_BP_P1_TP — D-_IC
GND
D+_CONN, D-_CONN, NC 4 NC
USB3_BP_P1_TN_CMC
USB3_BP_P1_TP_CMC

J15 CONN
USB3_9P_18MH
M1097400-001
TH
TX/RX FROM HOST PERSPECTIVE
VBUS 1, D- 2, D+ 3, GND 4, STDA_SSRX_N 5, STDA_SSRX_P 6, GND_DRAIN 7, STDA_SSTX_N 8, STDA_SSTX_P 9
MH 10–27

REAR 0
(CLOSEST TO ENET PORT)
68 39 BI V_5P0_USB3_P0
C541 3 PF +/-0.1PF 25 V COG 201
C544 3 PF +/-0.1PF 25 V COG 201
C547 15 PF 5% 25 V COG 201
C550 15 PF 5% 25 V COG 201

V_12P0
R256 10 KOHM 1% CH 201 DEBUG_FTDI
PWR DETECT
3.0V NOM
VBUS_EN_PWR_SNS
R280 3.32 KOHM 1% CH 201 DEBUG_FTDI
R440 0 OHM 5% 201 EMPTY

V_3P3_FTDI
39 21 IN USB_PWR_EN
R609 0 OHM 5% 402 CH NO_DEBUG_FTDI
USB3_P0_EN
C1681 1 UF 20% 10 V X5R 201 DEBUG_FTDI

U51 IC
SN74LVC1G08
M1035197-001
SC70-5 DEBUG_FTDI
A, B, VCC 5, Y 4, GND 3
69 68 IN LOGIC_USB_HOST_PWR_EN
GATED_USB_HOST_PWR_EN
R610 0 OHM 5% 402 CH DEBUG_FTDI

V_5P0
USB_LOAD_SWITCH_BASE
U407 IC
TPS2001D
M1089559-001
SOT23-5
C1701 0.1 UF 10% 25 V X5R 201
IN 5, OUT 1, FLT_N 3, EN 4, GND 2
39 V_5P0_USB3_FP
USB_PWR_FAULT_N OUT 21 39
39 21 IN USB_PWR_EN
USB PORT PROTECTION

C1702 150 UF 20% 6.3 V POLY SM
C1703 470 PF 10% 25 V X7R 201
C1704 4.7 UF 20% 10 V X5R 402

39 22 BI USB2_FP_P0_DN
39 22 BI USB2_FP_P0_DP
39 22 OUT USB3_FP_P0_RN
39 22 OUT USB3_FP_P0_RP

FILT U438
ECMF02_2HSMX6
X900532-002
DFN6
22 IN USB3_FP_P0_TP — D+_IC
22 IN USB3_FP_P0_TN — D-_IC
GND
D+_CONN, D-_CONN, NC 4 NC
USB3_FP_P0_TN_CMC
USB3_FP_P0_TP_CMC

J27 CONN
USB3_9P_15MH
M1097400-002
TH
TX/RX FROM HOST PERSPECTIVE
VBUS 1, D- 2, D+ 3, GND 4, STDA_SSRX_N 5, STDA_SSRX_P 6, GND_DRAIN 7, STDA_SSTX_N 8, STDA_SSTX_P 9
MH 10–24

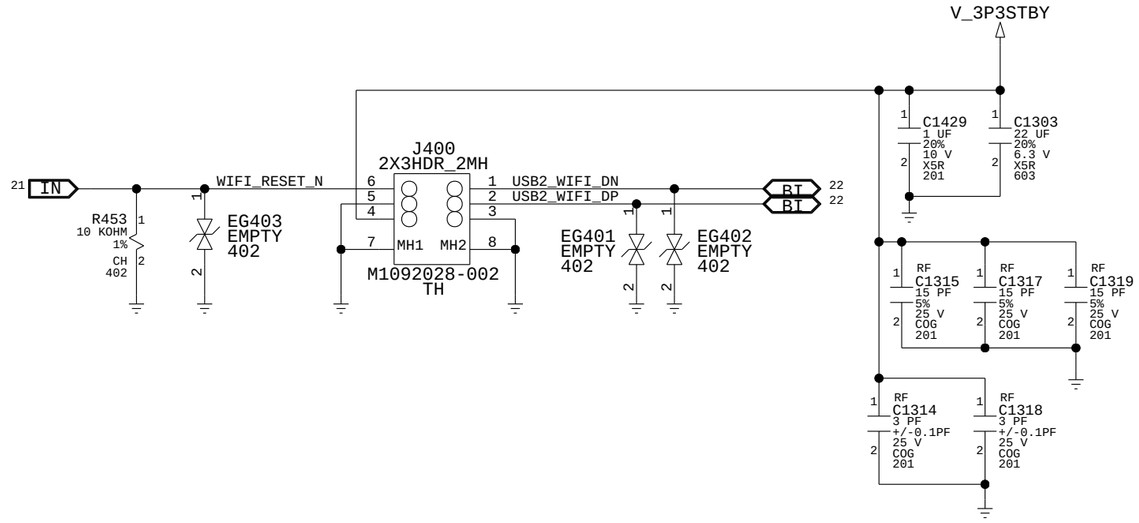
FRONT USB
39 V_5P0_USB3_FP
C542 3 PF +/-0.1PF 25 V COG 201
C545 3 PF +/-0.1PF 25 V COG 201
C548 15 PF 5% 25 V COG 201
C551 15 PF 5% 25 V COG 201

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1089694-001	IC	U431	IC,SM,SOT25,LOAD SWITCH,50 MOHM,2.5 A, SI	USB_LOAD_SWITCH_FTDI
M1089559-001	IC	U407, U717	IC,SM,SOT23-5,CURRENT LIMITED, POWER DISTRIBUTION SWITCH	USB_LOAD_SWITCH_FTDI
M1089559-001	IC	U431, U407, U717	IC,SM,SOT23-5,CURRENT LIMITED, POWER DISTRIBUTION SWITCH	USB_LOAD_SWITCH_TI
M1104212-001	IC	U431, U407, U717	IC-PWR,DC/DC CONV,SM,TSOT-23-5,HIGH SIDE POWER SWITCH	USB_LOAD_SWITCH_RICHTEK

USB_LOAD_SWITCH_FTDI STUFFS USB P0 LOAD SWITCH WITH REVERSE CURRENT PROTECTION

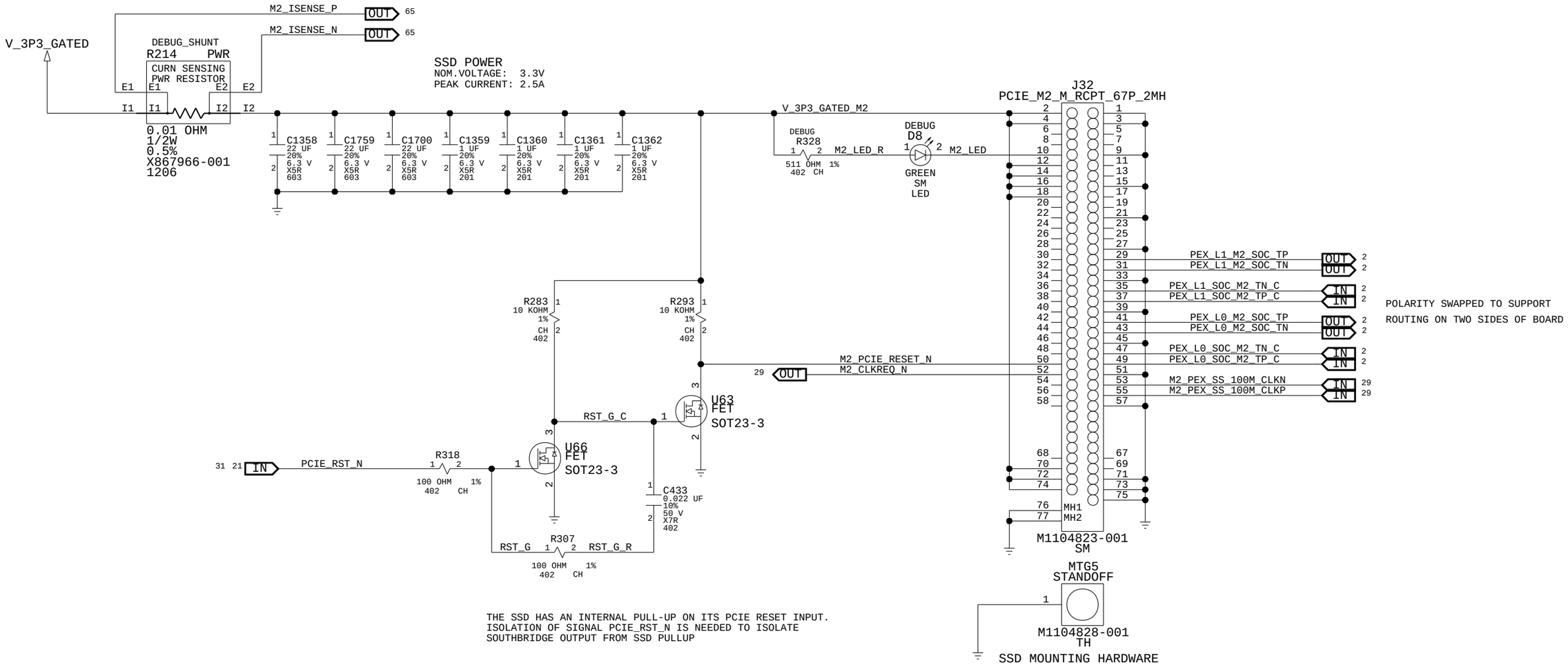
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	39/76	39/76	C	0.12

CONN: WIFI



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	40/76	40/76	C	0.12

CONN: M.2



POLARITY SWAPPED TO SUPPORT ROUTING ON TWO SIDES OF BOARD

THE SSD HAS AN INTERNAL PULL-UP ON ITS PCIE RESET INPUT. ISOLATION OF SIGNAL PCIE_RST_N IS NEEDED TO ISOLATE SOUTHBRIDGE OUTPUT FROM SSD PULLUP

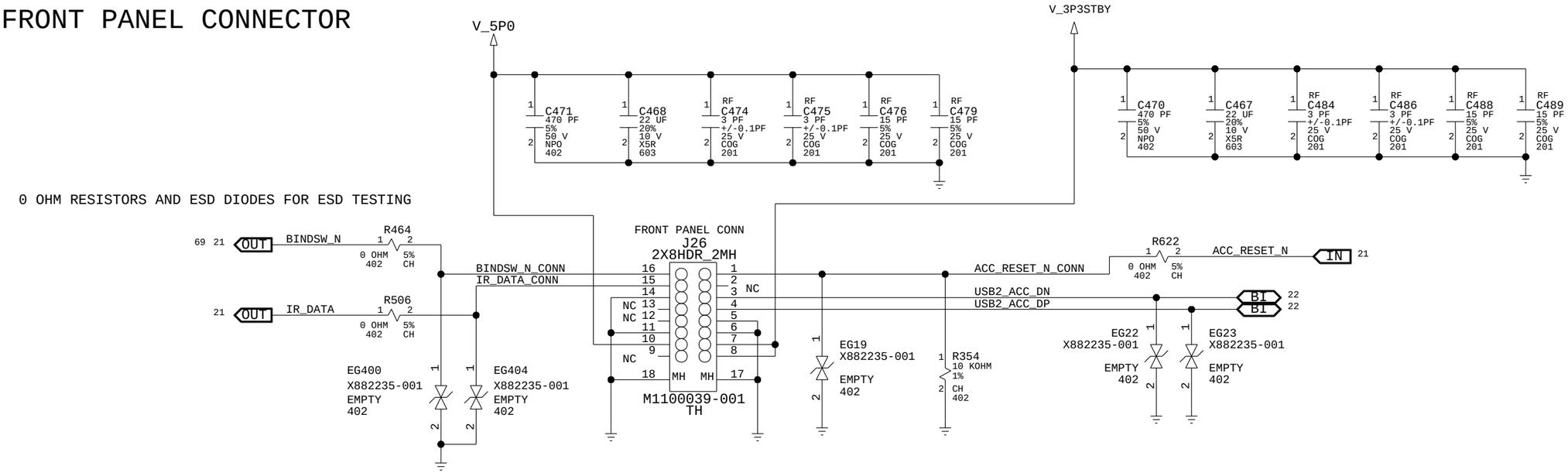
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	41/76	41/76	C	0.12

CONN: ODD

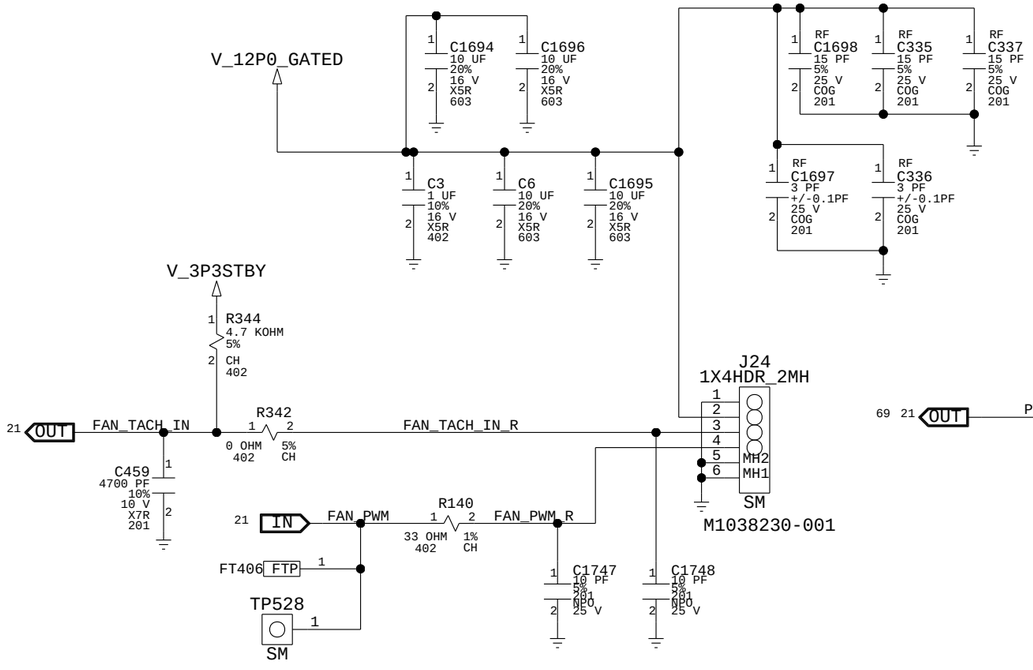
PLACEHOLDER FOR OBSOLETE ODD CIRCUITRY

CONN: FRONT PANEL, FAN, NEXUS

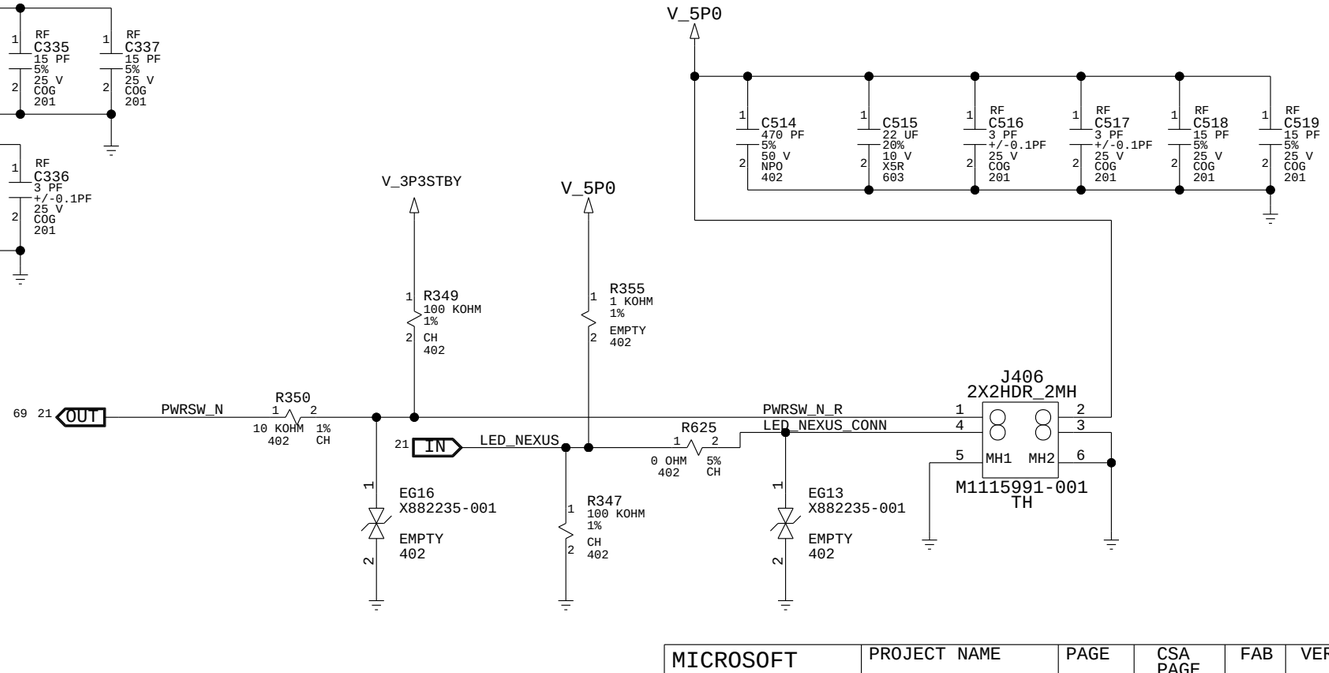
FRONT PANEL CONNECTOR



FAN CONNECTOR

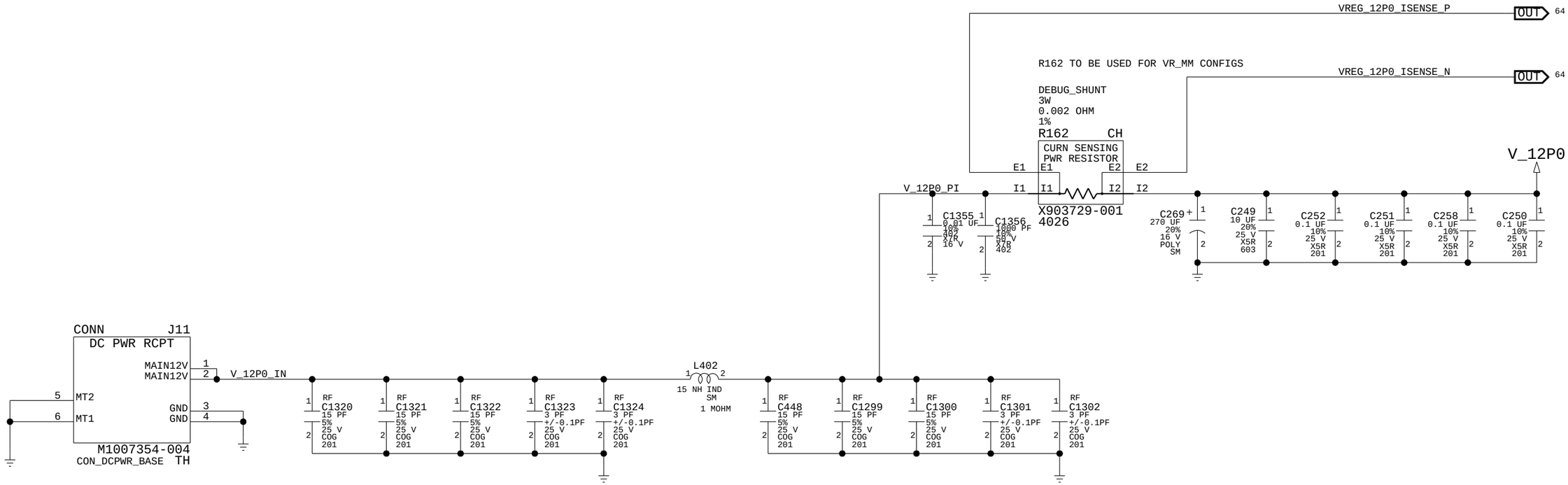


NEXUS CONNECTOR



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	43/76	43/76	C	0.12

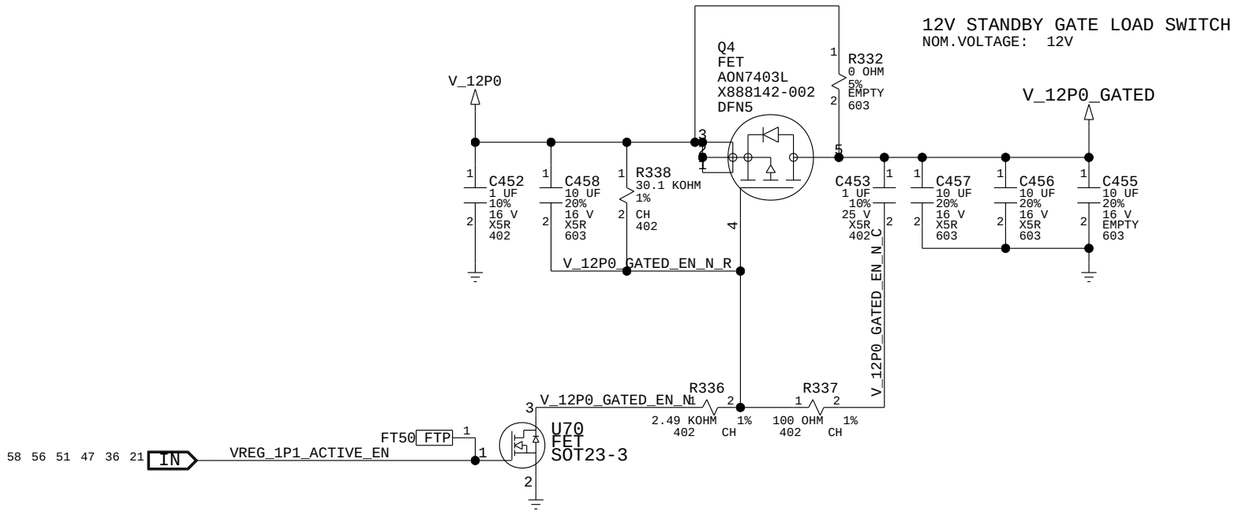
CONN: POWER



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1007354-004	CONN	J11	FOXCONN DC POWER CONNECTOR 1ST MAT SRC	CON_DCPWR_FOXC_1
M1021821-003	CONN	J11	FOXLINK QUAL DC POWER CONN 1ST MAT SRC	CON_DCPWR_FOXL_1
M1040539-001	CONN	J11	FOXCONN QUAL DC POWER CONN 2ND MAT SRC	CON_DCPWR_FOXC_2
M1040540-001	CONN	J11	FOXLINK QUAL DC POWER CONN 2ND MAT SRC	CON_DCPWR_FOXL_2

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	44/76	44/76	C	0.12

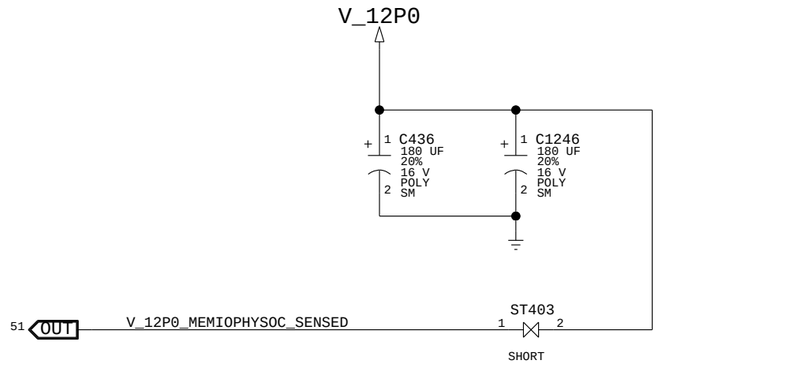
VREGS: V_12P0_GATED



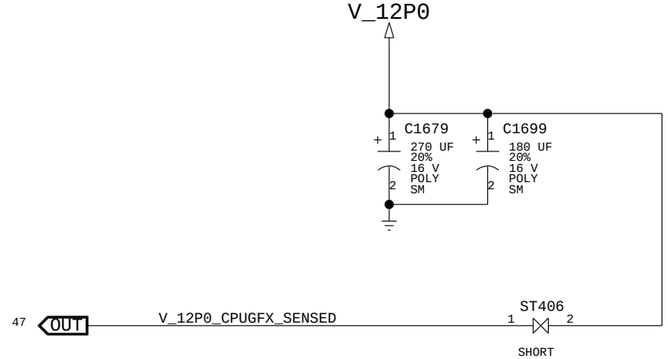
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	45/76	45/76	C	0.12

VREGS: INPUT DECOUPLING

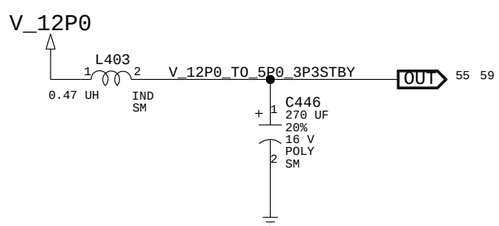
CPU/MEMIO/MEMPHY/SOC INPUT FILTER



GFX INPUT FILTER



5P0 AND 3P3STBY INPUT FILTER



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	46/76	46/76	C	0.12

VREGS: V_CPUCORE, V_GFXCORE CONTROLLER

PLACE NEXT TO I2C ISOLATION RESISTORS

DB491
DB492

62 51 37 35 29 21 68 66 65 IN SMBUS_CLK — R231 0 OHM 5% CH 402 — SMBUS_CLK_GFXCPU

62 51 37 35 29 21 68 66 65 BI SMBUS_DATA — R233 0 OHM 5% CH 402 — SMBUS_DATA_GFXCPU

46 IN V_12P0_CPUGFX_SENSED — R252 150 KOHM 1% 402 CH

R253 10 KOHM 1% CH 402

C395 0.01 UF 10% 16 V X5R 201

V_3P3STBY

R563 2.2 OHM 1% CH 603

VREG_GFXCPU_VDD33

C1009 1 UF 20% 10 V X5R 201

V_SOC1P8

R808 1 MOHM 1% CH 201

R809 1 MOHM 1% CH 201

V_3P3STBY

R449 10 KOHM 1% CH 402

R258 10 KOHM 1% CH 402

DB70 TP SVT — R228 0 OHM 5% CH

DB69 TP SVD — R219 0 OHM 5% CH

DB68 TP SVC — R220 0 OHM 5% CH

69 51 21 57 56 OUT VREG_PWRGPAB_CPUGFX_PWRGD

R581 0 OHM 5% CH 402

R580 100 KOHM 1% CH 402

49 48 OUT — R249 0 OHM 5% CH 402 — VREG_GFXCPU_PG1

R248 0 OHM 5% 402 EMPTY — VREG_GFXCPU_PG2

56 45 21 36 51 58 IN VREG_1P1_ACTIVE_EN

VREG_GFXCPU_EN

V_SOC1P8

C1010 1 UF 20% 10 V X5R 201

48 49 IN VREG_GFXCORE_TEMP — R456 24.9 KOHM 1% CH 402 — C449 0.1 UF 10% 16 V X5R 201

R122 0 OHM 5% CH 402

50 IN VREG_CPUCORE_TEMP — R244 0 OHM 5% EMPTY

C450 0.1 UF 10% 25 V EMPTY 402

FT1003 FTP — DB1004 — VREG_GFX_IMON_R — R245 0 OHM 5% CH — VREG_GFX_IMON

VREG_CPU_IMON

FT1002 FTP — DB1003 — VREG_CPU_IMON_R — R459 0 OHM 5% CH

C390 1000 PF 10% 50 V EMPTY 402

18	SCL_P		
17	SDA_P		
19	STB	50 49 48 OUT	VREG_GFXCPU_SYNC
12	VINSEN		VINSEN_12P0_GFXCORE
23	PWROK/PVID3	70 21 8 IN	SOC_PWR_OK
21	SVT		SVT_R
25	SVD/PVID1		SVD_R
24	SVC/PVID2		SVC_R
16	MUX_ALT		VREG_GFXCPU_MUX_ALT
15	PG1		VREG_GFXCPU_PG1
14	PG2		VREG_GFXCPU_PG2
20	EN		VREG_GFXCPU_EN
22	VDDIO		
9	TSENS1		
10	IMON1		VREG_GFX_IMON
11	IMON2		VREG_CPU_IMON
41	MPAD		

U57 IC MP2855 M1080755-102 QFN41

VDD33 35
VDD18 13

VREG_GFXCPU_VDD18

C391 1 UF 20% 10 V X5R 201

VORTN1 6 VREG_GFXCORE_S_RTN
VOSEN1 5 VREG_GFXCORE_S

CS1	36	VREG_GFXCORE_CS1	IN 48
CS2	37	VREG_GFXCORE_CS2	IN 48
CS3	38	VREG_GFXCORE_CS3	IN 49
CS4	39	VREG_GFXCORE_CS4	IN 49
CS5	40	NC	
CS6	1	NC	
CS7	2	NC	
CS8	3	VREG_CPUCORE_CS2	IN 50
CS9	4	VREG_CPUCORE_CS1	IN 50

VORTN2 8 VREG_CPUCORE_S_RTN
VOSEN2 7 VREG_CPUCORE_S

PWM1	34	VREG_GFXCORE_PWM1_R	
PWM2	33	VREG_GFXCORE_PWM2_R	
PWM3	32	VREG_GFXCORE_PWM3_R	
PWM4	31	VREG_GFXCORE_PWM4_R	
PWM5	30	NC	
PWM6	29	NC	
PWM7	28	NC	
PWM8	27	VREG_CPUCORE_PWM2_R	
PWM9	26	VREG_CPUCORE_PWM1_R	

DB444
DB445

PLACE GND CLOSE TO IMON

DB71 TP — FT1005 FTP — R1003 0 OHM 5% 402 CH — SOC_GFXCORE_S_RTN IN 8

R564 100 OHM 1% CH 402

C460 0.1 UF 10% 25 V EMPTY 402

V_GFXCORE

R225 100 OHM 1% CH 402

R1006 0 OHM 5% 402 CH — SOC_GFXCORE_S IN 8

DB1005 TP — FT1004 FTP

V_CPUCORE

R565 100 OHM 1% CH 402

DB1007 TP — FT1007 FTP — R230 0 OHM 5% 402 CH — SOC_CPUCORE_S IN 8

C462 0.1 UF 10% 25 V EMPTY 402

R617 0 OHM 5% 402 CH — SOC_CPUCORE_S_RTN IN 8

DB1006 TP — FT1006 FTP

R232 100 OHM 1% CH 402

R217 0 OHM 402 5% CH — VREG_GFXCORE_PWM1 OUT 48

R176 0 OHM 402 5% CH — VREG_GFXCORE_PWM2 OUT 48

R153 0 OHM 402 5% CH — VREG_GFXCORE_PWM3 OUT 49

R160 0 OHM 402 5% CH — VREG_GFXCORE_PWM4 OUT 49

R218 0 OHM 402 5% CH — VREG_CPUCORE_PWM2 OUT 50

R462 0 OHM 402 5% CH — VREG_CPUCORE_PWM1 OUT 50

MP2855 I2C ADDRESS

	7-BIT BASE	R/W	I2C ADDR	8-BIT HEX
WRITE	010 0000	0	0X20	0X40
READ	010 0000	1	0X20	0X41

MP2855 RAIL ASSIGNMENTS

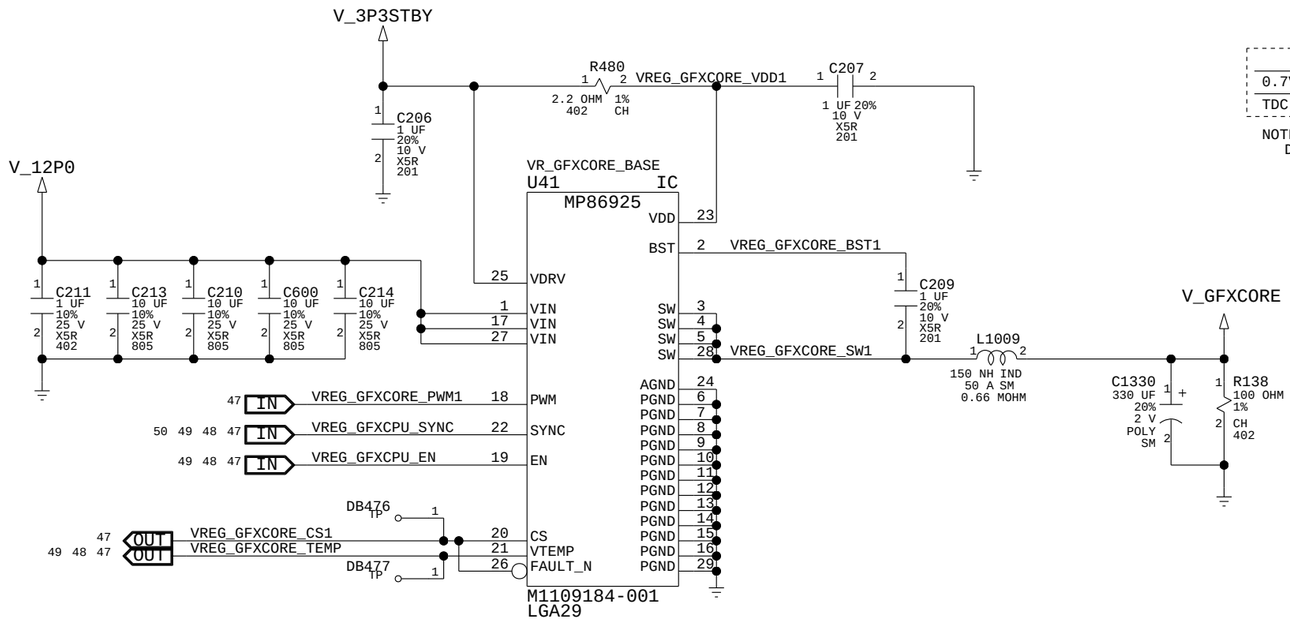
RAIL 1:	V_GFXCORE	(POWER GROUP B)
RAIL 2:	V_CPUCORE	(POWER GROUP B)

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	47/76	47/76	C	0.12

VREGS: V_GFXCORE OUTPUT PHASE 1 & 2

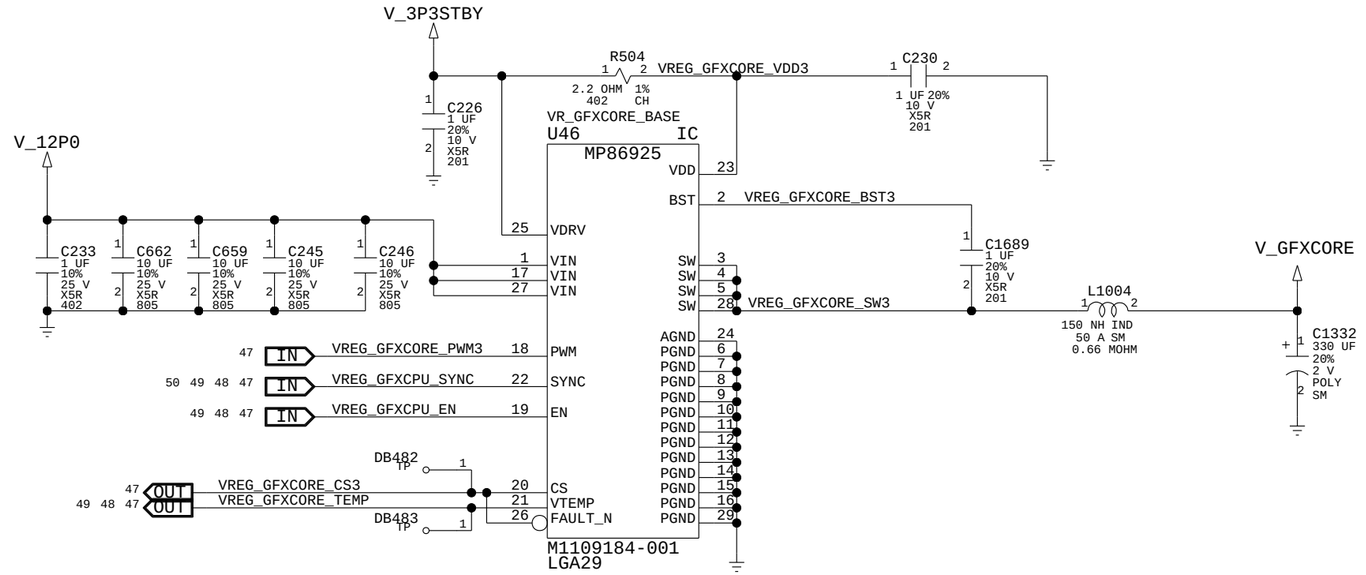
V_GFXCORE		
0.7V-0.8V		
TDC: 75A	EDC: 103A	FSW: 700KHZ

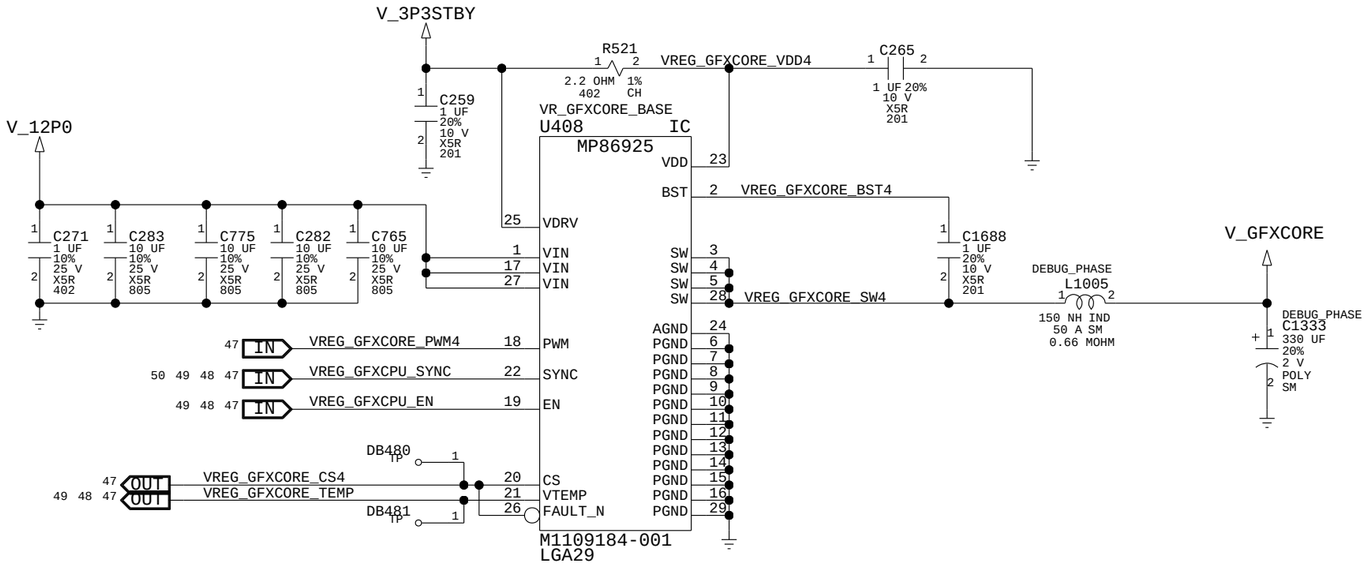
NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM_PROPERTY
M1109184-001	IC	U41, U52, U46, U408	IC-PWR, DC/DC CONV, MP86925	VR_GFXCORE_MP86925
M1079609-001	IC	U41, U52, U46, U408	IC-PWR, DC/DC CONV, MP86915	VR_GFXCORE_MP86915
M1109184-001	IC	U41, U52, U46	IC-PWR, DC/DC CONV, MP86925	VR_GFXCORE_RETAIL

VREGS: V_GFXCORE OUTPUT PHASE 3 & 4



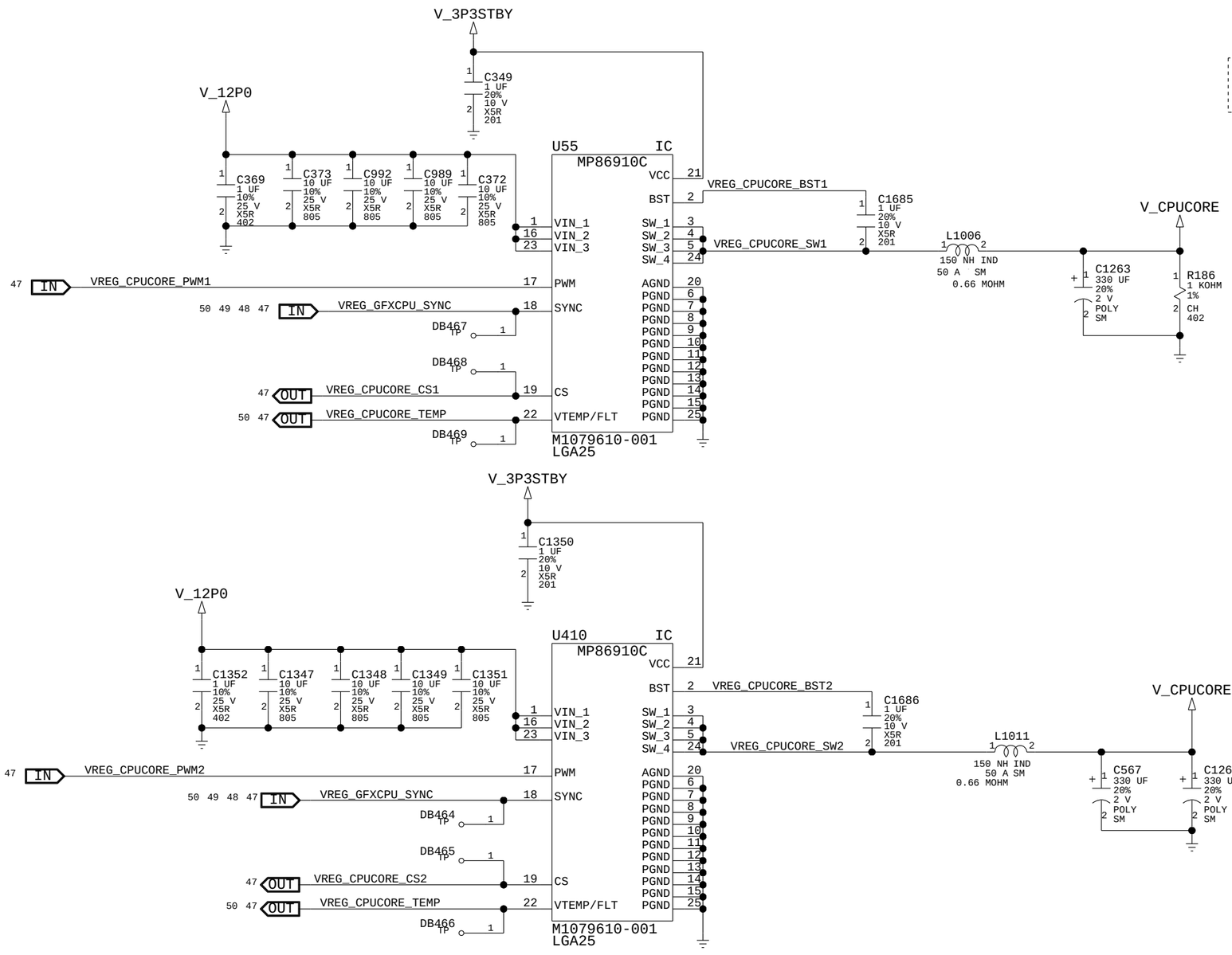


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	49/76	49/76	C	0.12

VREGS: V_CPUCORE OUTPUT

V_CPUCORE
0.9V-1.1V
TDC: 26A EDC: 69A FSW: 700KHZ

NOTE: X6S/X7R CAPACITORS USED NEAR SOC DUE TO HIGHER TEMPERATURES IN AREA



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	50/76	50/76	C	0.12

VREGS: V_MEMIO, V_MEMPHY, V_SOC CONTROLLER

PLACE NEXT TO I2C ISOLATION RESISTORS

DB411
DB412

68 66 65 62 47 37 35 29 21 IN SMBUS_CLK — R655 0 OHM 5% CH 402 — SMBUS_CLK_MEMIOPHYSOC

68 66 65 62 47 37 35 29 21 BI SMBUS_DATA — R675 0 OHM 5% CH 402 — SMBUS_DATA_MEMIOPHYSOC

46 IN V_12P0_MEMIOPHYSOC_SENSED — R132 150 KOHM 1% 402 CH — VINSEN_12P0_MEMIOPHYSOC

R676 10 KOHM 1% CH 402
C1441 0.01 UF 10% 16 V X5R 201

56 47 45 36 21 58 IN VREG_1P1_ACTIVE_EN — R657 0 OHM 5% 402 CH

R130 100 KOHM 1% EMPTY 402

69 57 56 47 21 OUT VREG_PWRGPAB_CPUGFX_PWRGD — R131 0 OHM 5% 402 CH

PG PULLED UP EXTERNALLY

3 IN 3P3V_SLEEP_S3_N — R790 0 OHM 5% 402 CH

3 IN 3P3V_FORCE_PWR — R678 0 OHM 5% 402 CH

V_3P3STBY

R171 2.2 OHM 1% CH 603

VREG_MEMIOPHYSOC_VDD33

C1443 1 UF 20% 10 V X5R 201

V_3P3_GATED

R654 10 KOHM 1% EMPTY 402
R679 10 KOHM 1% EMPTY 402
R683 10 KOHM 1% EMPTY 402

DB141

R170 10 KOHM 1% CH 402
R685 10 KOHM 1% CH 402
R686 10 KOHM 1% CH 402

DB661 1 VREG_MEMIOPHYSOC_GPIO1
38 OUT CFX_PERST_GPIO_N
60 OUT V_3P3_CFX_EN_GPIO
30 29 OUT SOC_REFCLK_EN_N

GPIO PULLUPS ON CFX PAGES

U480 IC
MP2926
1 of 2

19	SCL_P	VDD33	35
18	SDA_P	VDD18	17
13	VINSEN		
22	EN	STB	20 VREG_MEMIOPHYSOC_SYNC OUT 53 54
25	PGOOD		
		CS1	37 VREG_MEMPHY_CS IN 53
		CS2	38
		CS3	39
		CS4	40 VREG_MEMIO_CS IN 53
		CS5	1 VREG_SOC_CS2 IN 54
		CS6	2 VREG_SOC_CS1 IN 54
PVID0	VREG_MEMIOPHYSOC_PVID032		
PVID1	VREG_MEMIOPHYSOC_PVID131		
PVID2	VREG_MEMIOPHYSOC_PVID230		
		PWM1	34 VREG_MEMPHY_PWM_R
		PWM2	33
		PWM3	29
		PWM4	28 VREG_MEMIO_PWM_R
		PWM5	27 VREG_SOC_PWM2_R
		PWM6	26 VREG_SOC_PWM1_R
GPIO1	36		
GPIO2	21		
GPIO3	23		
GPIO4	24		
TSENS1	9	IMON1	14 VREG_MEMPHY_IMON
TSENS2	10	IMON2	15 VREG_MEMIO_IMON
TSENS3	11	IMON3	16
ADDR	12	MPAD	41

M1094197-102
QFN41

VREG_MEMIOPHYSOC_VDD18 — 51

C18 1 UF 20% 10 V X5R 201

R688 0 OHM 402 5% CH — VREG_MEMPHY_PWM — OUT 53

R182 0 OHM 402 5% CH — VREG_MEMIO_PWM — OUT 53

R682 0 OHM 402 5% CH — VREG_SOC_PWM2 — OUT 54

R684 0 OHM 402 5% CH — VREG_SOC_PWM1 — OUT 54

R681 0 OHM 402 5% CH — VREG_MEMPHY_IMON_R — DB685 — FTP FT686

C1447 1000 PF 10% 50 V EMPTY 402

R687 0 OHM 5% CH — VREG_MEMIO_IMON_R — DB677 — FTP FT679

C1445 1000 PF 10% 50 V EMPTY 402

53 IN VREG_MEMPHY_TEMP
53 IN VREG_MEMIO_TEMP
54 IN VREG_SOC_TEMP

R70 24.9 KOHM 1% CH 402 — C1439 0.1 UF 10% 16 V X5R 201
R674 24.9 KOHM 1% CH 402 — C1440 0.1 UF 10% 16 V X5R 201
R658 24.9 KOHM 1% CH 402 — C1442 0.1 UF 10% 16 V X5R 201

51 VREG_MEMIOPHYSOC_VDD18 — R677 3.32 KOHM 1% 402 EMPTY — VREG_MEMIOPHYSOC_ADDR

R680 10 KOHM 1% CH 402

PLACE GND CLOSE TO IMON

DB449
DB450
DB451

VREG_SOC_IMON — R673 0 OHM 5% 402 CH — VREG_SOC_IMON_R — DB678 — FTP FT680

C1446 1000 PF 10% 50 V EMPTY 402

V_MEMPHY/V_MEMIO PSTATES

V_MEMPHY	V_MEMIO	PVID1 3P3V_SLEEP_S3_N	PVID2 3P3V_FORCE_PWR
0.85	1.35	0	0
0.85	1.25	0	1
0.75	1.25	1	0
0.70	1.25	1	1

MP2926 RAIL ASSIGNMENTS

RAIL 1:	V_MEMPHY	(POWER GROUP B)
RAIL 2:	V_MEMIO	(POWER GROUP A)
RAIL 3:	V_SOC	(POWER GROUP B)

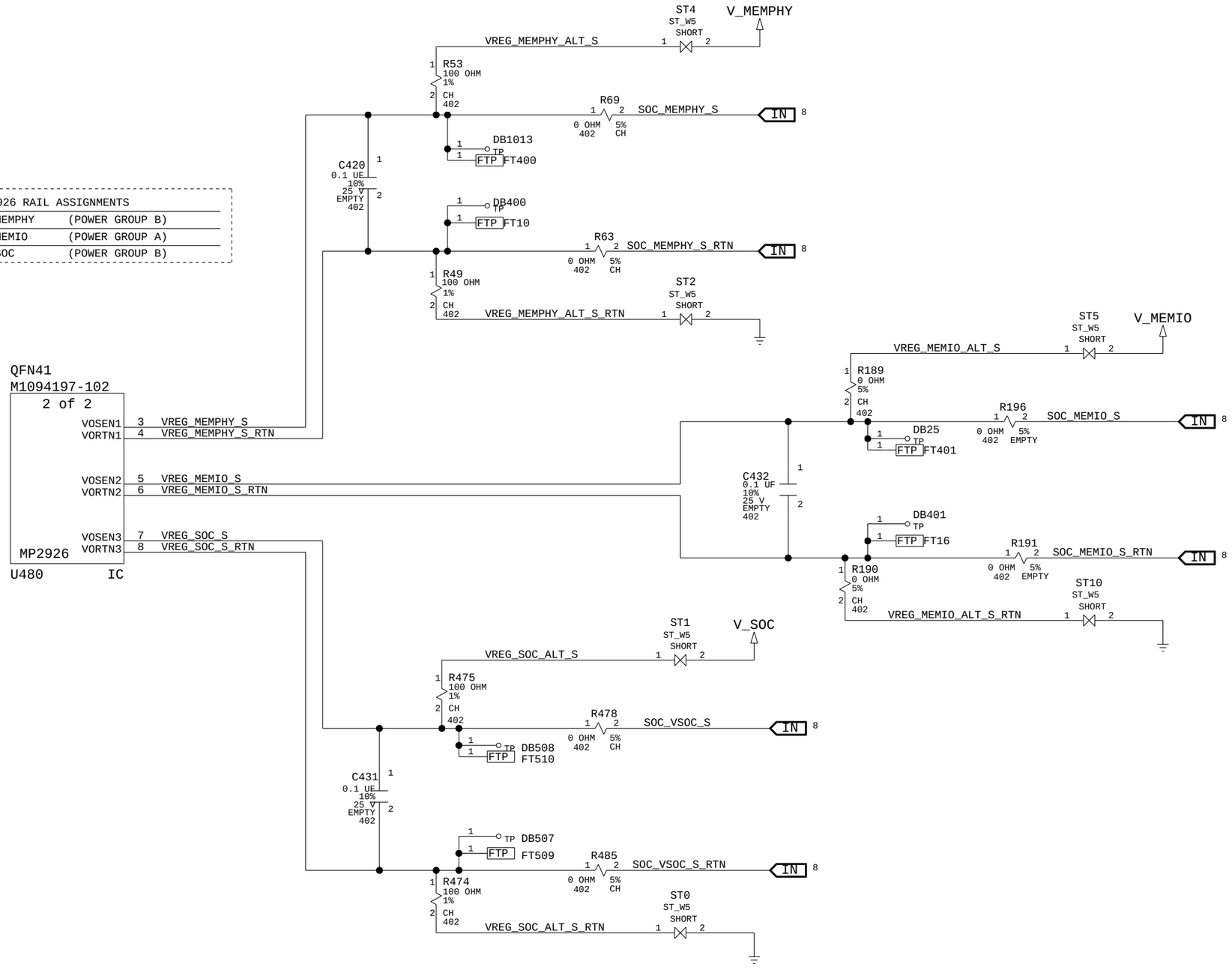
MP2926 I2C ADDRESS

	7-BIT BASE	R/W	I2C ADDR	8-BIT HEX
WRITE	010 0001	0	0X23	0X46
READ	010 0001	1	0X23	0X47

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	51/76	51/76	C	0.12

VREGS: V_MEMIO, V_MEMPHY, V_SOC SENSE

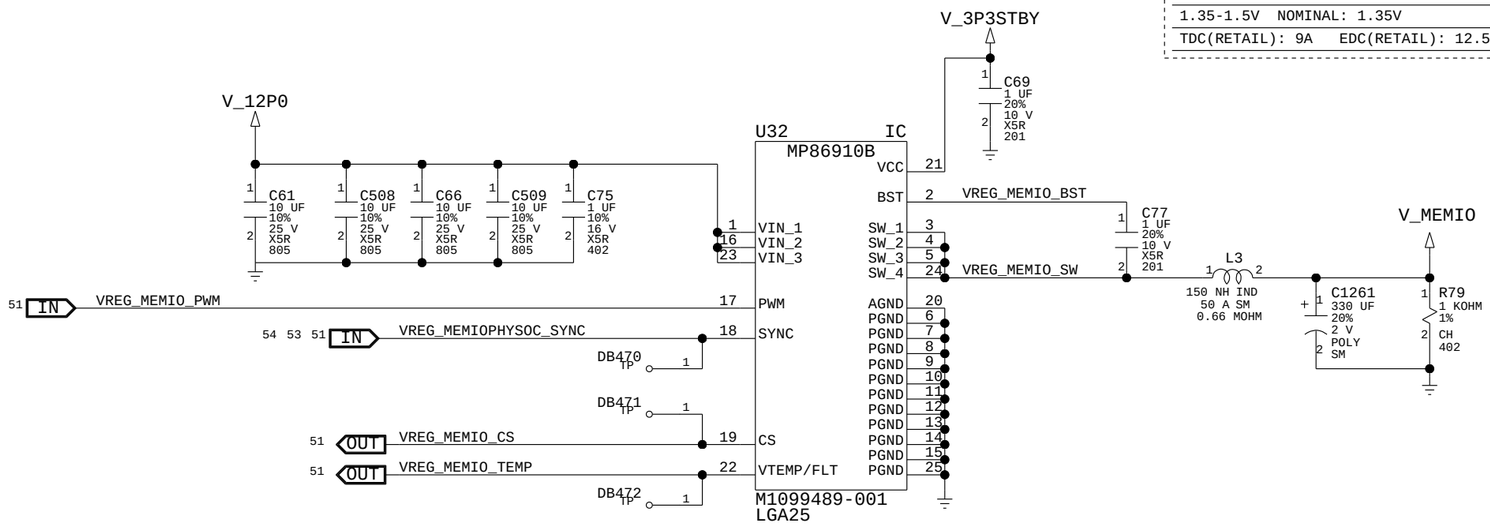
MP2926 RAIL ASSIGNMENTS		
RAIL 1:	V_MEMPHY	(POWER GROUP B)
RAIL 2:	V_MEMIO	(POWER GROUP A)
RAIL 3:	V_SOC	(POWER GROUP B)



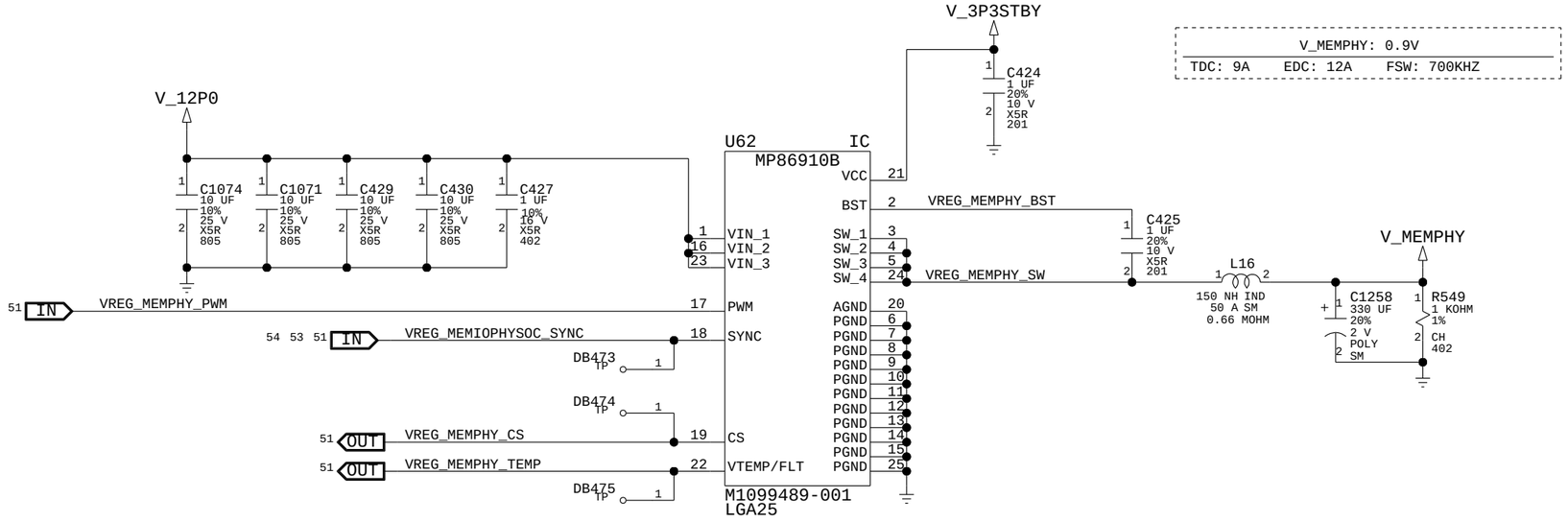
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	52/76	52/76	C	0.12

VREGS: V_MEMIO AND V_MEMPHY OUTPUT

V_MEMIO
1.35-1.5V NOMINAL: 1.35V
TDC(RETAIL): 9A EDC(RETAIL): 12.5A FSW: 700KHZ



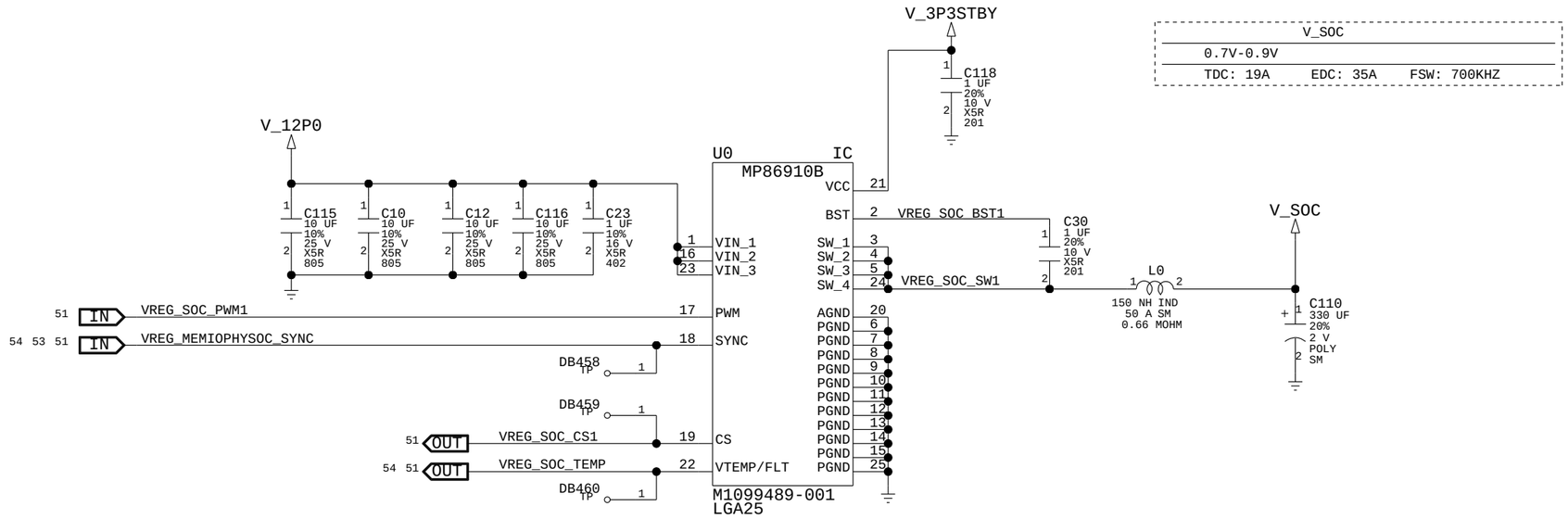
V_MEMPHY: 0.9V
TDC: 9A EDC: 12A FSW: 700KHZ

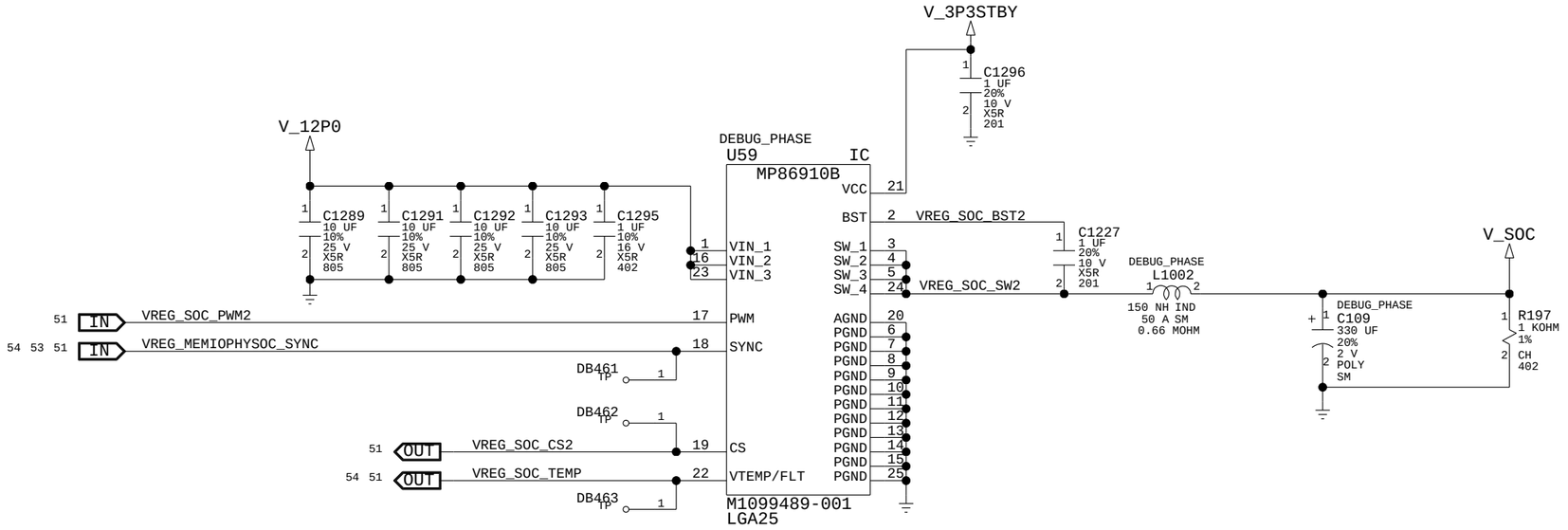


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	53/76	53/76	C	0.12

VREGS: V_SOC OUTPUT

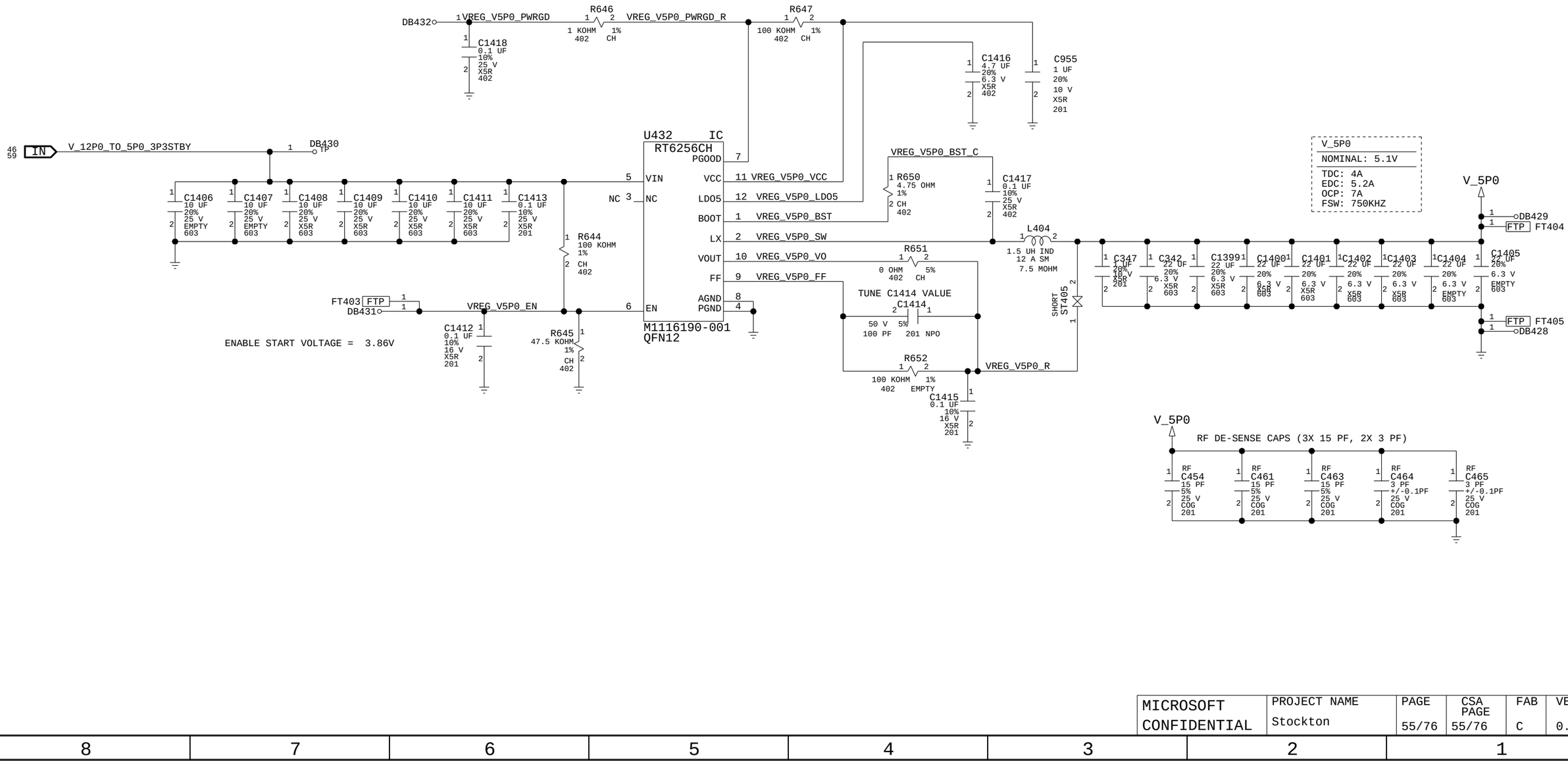
V_SOC		
0.7V-0.9V		
TDC: 19A	EDC: 35A	FSW: 700KHZ





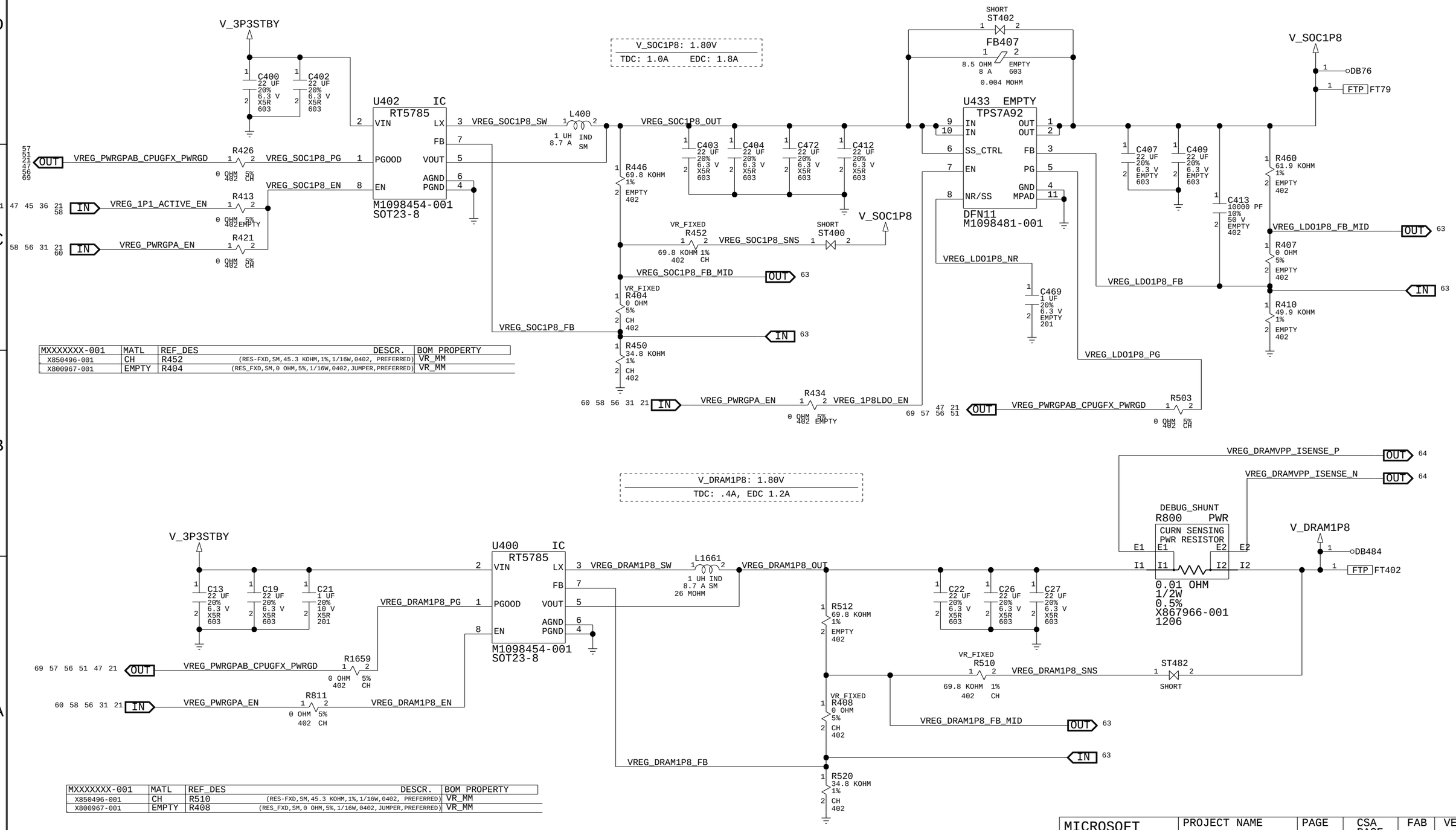
	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	54/76	54/76	C	0.12

VREGS: V_5P0



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	55/76	55/76	C	0.12

VREGS: V_SOC1P8, V_DRAM1P8



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	56/76	56/76	C	0.12

VREGS: V_SOCPHY, V_FUSE

V_SOCPHY: 0.75V
TDC: 1.3A EDC: 3.4A FSW: 2.2MHZ

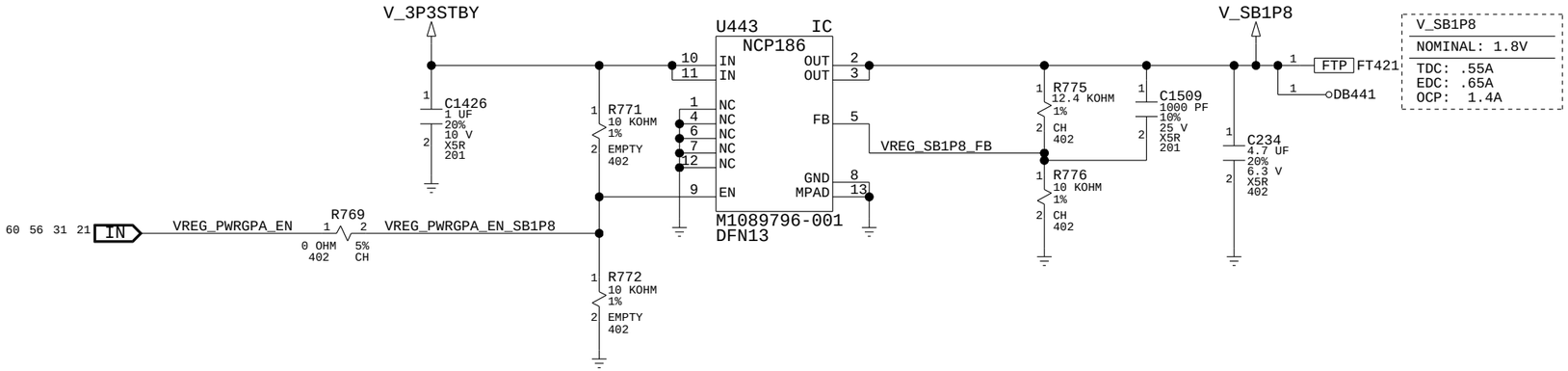
V_3P3STBY
C483 1 UF 20% 10 V X5R 201
C497 10 UF 20% 6.3 V X5R 402
C490 10 UF 20% 6.3 V X5R 402
U129 IC TPS62826 M1087390-001 DFN6
VIN SW PG FB EN GND
L1 0.47 UH IND 7.8 A SAT 0.01 OHM
X902974-001 SENSE RESISTOR WAS REMOVED BUT SHOULD BE REPLACED IN SCB
V_SOCPHY
FTP FT14 DB7
56 51 47 21 69 OUT VREG_PWRGPAB_CPUGFX_PWRGD
21 IN VREG_PWRGPB_EN
R136 0 OHM 402 5% CH
R743 0 OHM 402 5% CH
VREG_SOCPHY_PG
VREG_SOCPHY_EN
VREG_SOCPHY_SW
C40 120 PF 5% 50 V NPO 402
C503 22 UF 20% 6.3 V X5R 603
C1486 22 UF 20% 6.3 V X5R 603
C1487 22 UF 20% 6.3 V EMPTY 603
C1488 22 UF 20% 6.3 V EMPTY 603
FTP FT13 DB5
SHORT ST13
PWRGPAB_CPUGFX_PWRGD TIED TO 3P3_MAIN WITH 10K
VREG_PWRGPB_EN PULLED DOWN TO GND WITH 10K
VREG_SOCPHY_FB
VR_FIXED R68 24.9 KOHM 1% 402 CH
VREG_SOCPHY_S
R64 100 KOHM 1% CH 402
IN 63
OUT 63

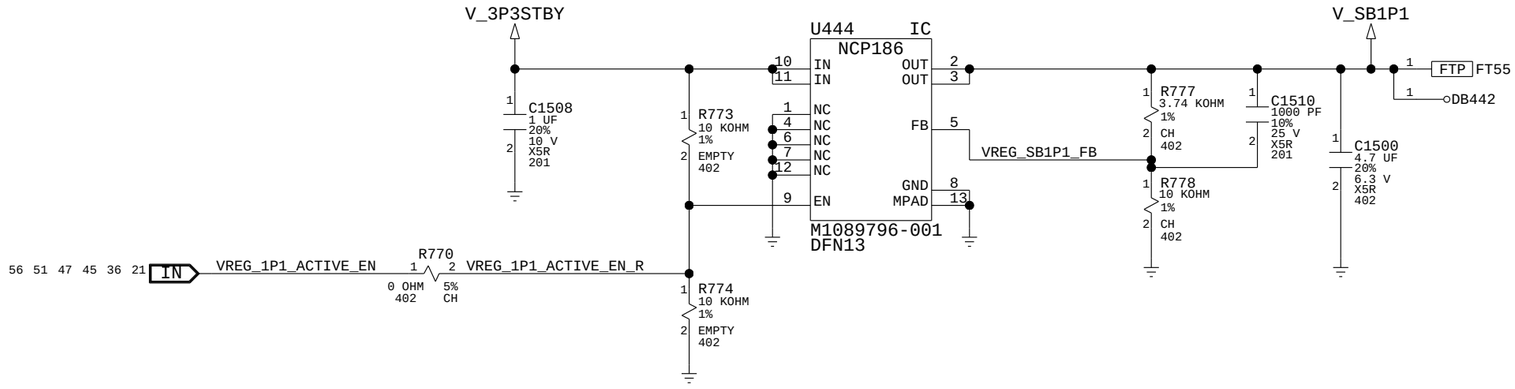
V_FUSE: 0.83V
TDC: 100MA

V_3P3_GATED
V_3P3STBY
R324 100 KOHM 1% CH 402
C447 1 UF 10% 10 V X5R 402
U68 IC AP7331_ADJ M1012324-001 SOT23-5
IN OUT ADJ EN GND
VREG_PWRGPC_EN_R
D9 SOD323 DIO
D7 SOD323 DIO
R599 20 KOHM 1% EMPTY 402
21 IN VREG_PWRGPC_EN
28 IN V12P0_PWRGD
VREG_VFUSE_ADJ
R596 45.3 KOHM 1% CH 402
C1084 0.022 UF 10% 25 V EMPTY 402
R595 42.2 KOHM 1% CH 402
C441 4.7 UF 20% 10 V X5R 402
R597 1 KOHM 1% EMPTY 402
V_FUSE
DB74

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	57/76	57/76	C	0.12

VREGS: V_SB1P8, V_SB1P1

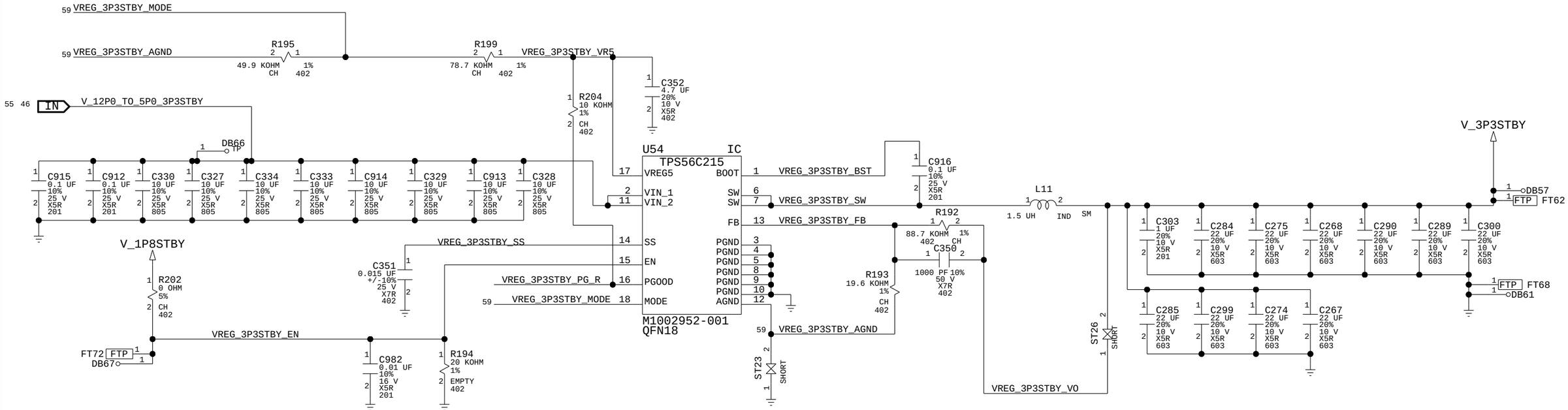




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	58/76	58/76	C	0.12

VREGS: V_3P3STBY

V_3P3STBY
NOM. VOLTAGE: 3.32
EST TDC = 9A
EST EDC = 12A

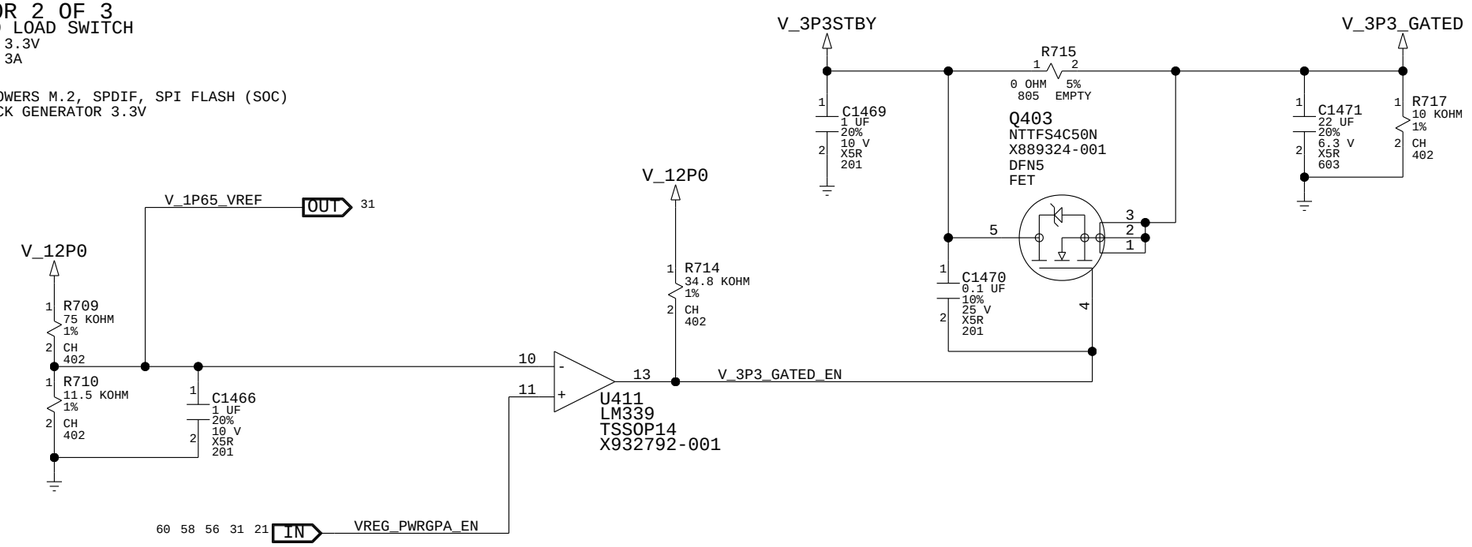


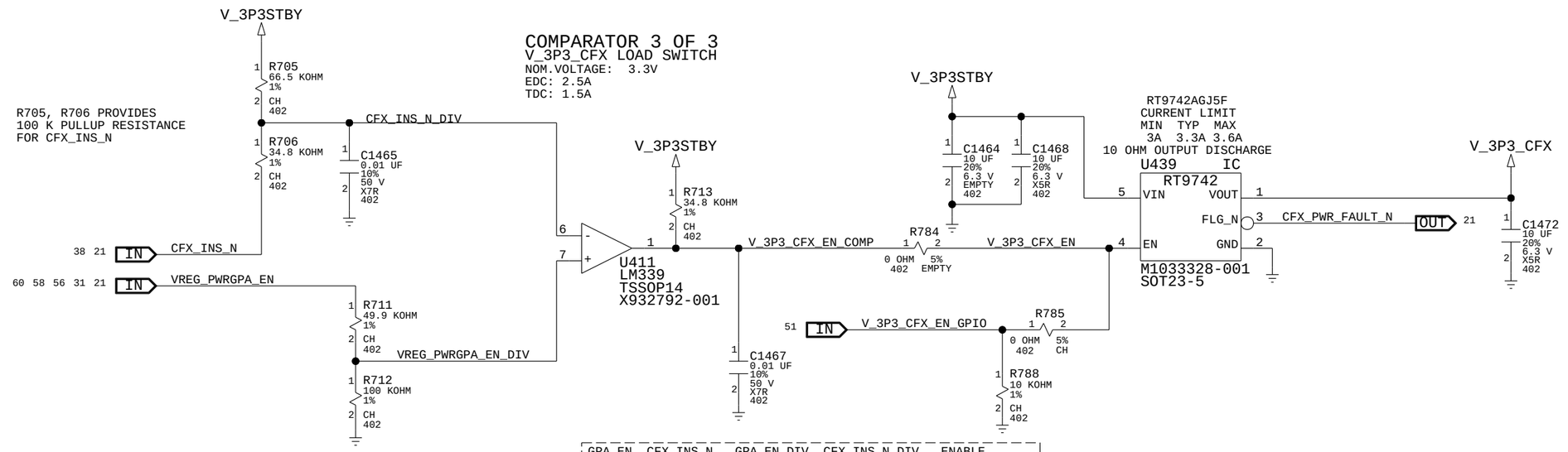
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	59/76	59/76	C	0.12

VREGS: V_3P3_GATED, V_3P3_CFX

COMPARATOR 2 OF 3
V_3P3_GATED LOAD SWITCH
NOM.VOLTAGE: 3.3V
PEAK CURRENT: 3A

V_3P3_GATED POWERS M.2, SPDIF, SPI FLASH (SOC)
SOC VDD3, CLOCK GENERATOR 3.3V

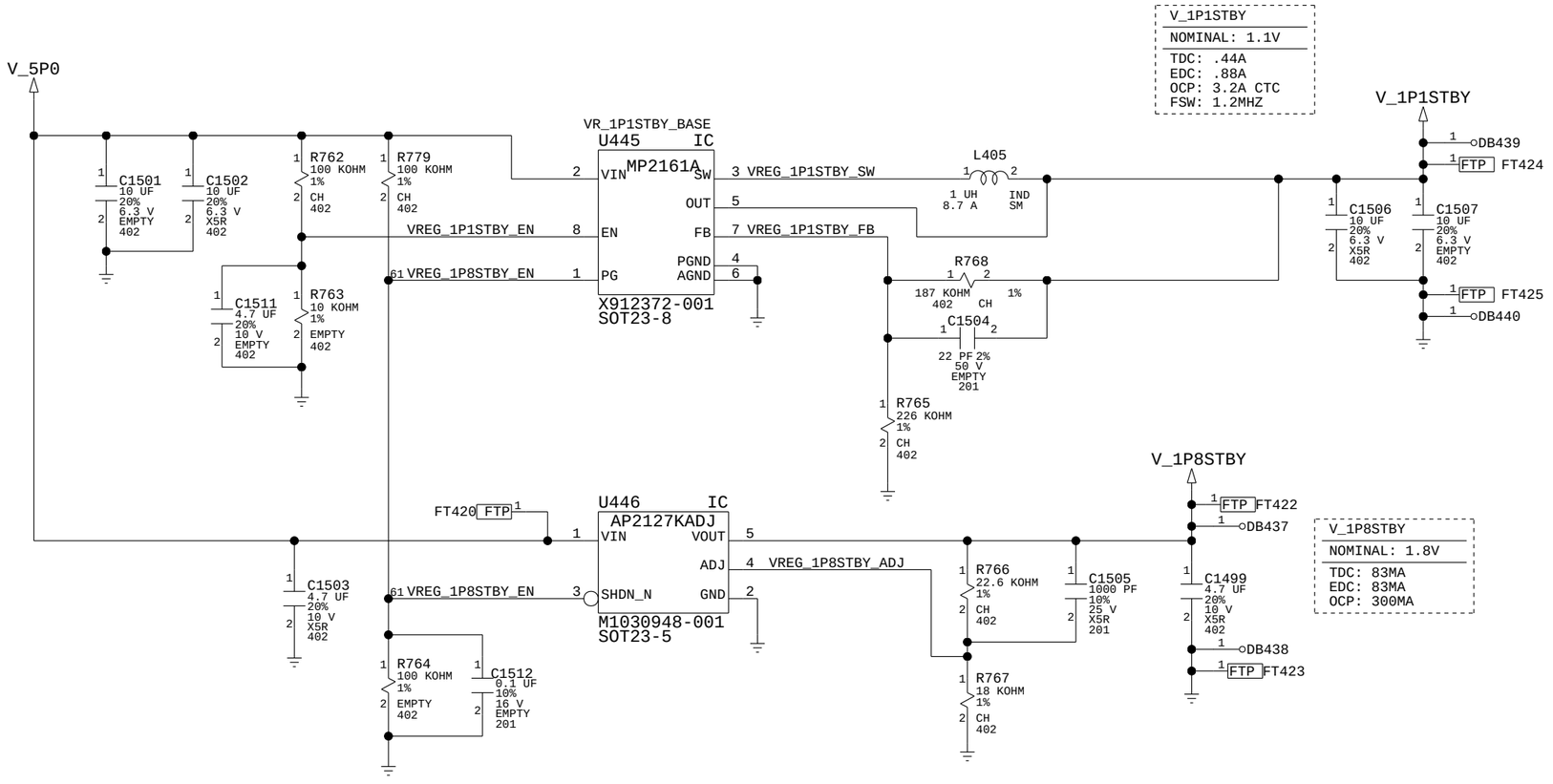




GPA_EN	CFX_INS_N	GPA_EN_DIV	CFX_INS_N_DIV	ENABLE
3.3V	0V	2.2V	1.13V	3.3V
3.3V	3.3V	2.2V	3.3V	0V
0V	0V	0V	1.13V	0V
0V	3.3V	0V	3.3V	0V

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	60/76	60/76	C	0.12

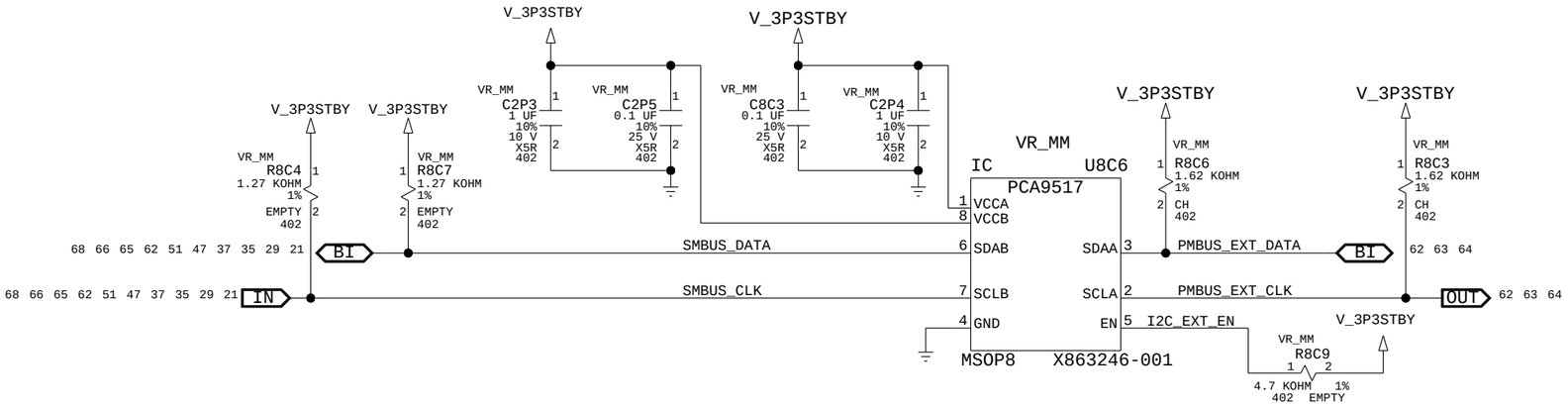
VREGS: V_1P1STBY, V_1P8STBY

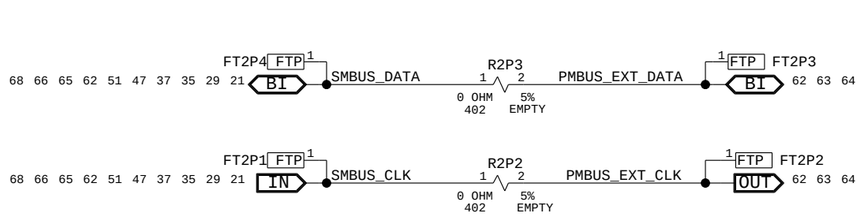


MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM_PROPERTY
X912372-001	IC	U445	IC-PWR,VREG,SM,TSOT23-8,STEP DOWN,6V,2A,MP2161A	VR_1P1STBY_MPS
M1018565-001	IC	U445	IC-PWR,VREG,SM,TSOT23-8,STEP DOWN,6V,2A,RICHTEK,RT5785C QUAL	VR_1P1STBY_RT

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	61/76	61/76	C	0.12

I2C





PMBUS JUMPERS REMOVE CAPACITANCE FOR MONITORING AND MARGINING. .
ALLOWS TESTING OF SMBUS WITHOUT EXTERNAL INTERFERANCE
REMOVE PMBUS IN RETAIL VERSIONS

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	62/76	62/76	C	0.12

DEBUG: MARGIN V_SOCPHY,V_SOC1P8, V_DRAM1P8

PLACE NEXT TO I2C ISOLATION RESISTORS

DB497
DB498

MCP4661 I2C ADDRESS
0101 110 R/W HEX
WRITE 0101 110 0 0X5C
READ 0101 110 1 0X5D

V_3P3STBY

R289 1 KOHM 1% CH 402
R466 1 KOHM 1% CH 402

MARGIN_SOC1P8_A2
MARGIN_SOC1P8_A1
MARGIN_SOC1P8_A0

64 63 62 IN PMBUS_EXT_CLK
R574 0 OHM 5% 201 CH
PMBUS_EXT_CLK_MM_SOC1P8

64 63 62 BI PMBUS_EXT_DATA
R577 0 OHM 5% 201 CH
PMBUS_EXT_DATA_MM_SOC1P8

R288 1 KOHM 1% CH 402

U404 IC
MCP4661
X871745-001
TSSOP14

A2	12		
A1	13		
HVC/A0	1		
SCL	2		
SDA	3		
WP_N	11		
VDD	14		
P0A	8		
P0W	9	VREG_SOC1P8_FB	OUT 56
P0B	10	VREG_SOC1P8_FB_MID	OUT 56
P1A	7		
P1W	6	VREG_LDO1P8_FB	OUT 56
P1B	5	VREG_LDO1P8_FB_MID	OUT 56
VSS1	4		

V_3P3STBY
C897 0.1 UF 10% 10 V X5R 201

DUAL 50KOHM, POWERS UP AT MIDSCALE

PLACE NEXT TO I2C ISOLATION RESISTORS

DB495
DB496

MCP4562 I2C ADDRESS
0101 111 R/W HEX
WRITE 0101 111 0 0X5E
READ 0101 111 1 0X5F

V_3P3STBY

R6 1 KOHM 1% CH 402
R8 1 KOHM 1% CH 402

MARGIN_SOCPHY_A0
MARGIN_SOCPHY_A1

64 63 62 IN PMBUS_EXT_CLK
R578 0 OHM 5% 201 CH
PMBUS_EXT_CLK_MM_SOCPHY

64 63 62 BI PMBUS_EXT_DATA
R579 0 OHM 5% 201 CH
PMBUS_EXT_DATA_MM_SOCPHY

U18 IC
MCP4562
X864019-001
DFN9

HVC/A0	1		
A1	7		
SCL	2		
SDA	3		
VDD	8		
P0B	6	VREG_SOCPHY_FB	OUT 57
P0W	5	VREG_SOCPHY_S	OUT 57
VSS	4		
MPAD	9		

V_3P3STBY
C4 0.1 UF 10% 10 V X5R 201

50KOHM, POWERS UP AT MIDSCALE

PLACE NEXT TO I2C ISOLATION RESISTORS

DB493
DB494

MCP4562 I2C ADDRESS
0101 101 R/W HEX
WRITE 0101 101 0 0X5A
READ 0101 101 1 0X5B

V_3P3STBY

R793 1 KOHM 1% CH 402
R794 1 KOHM 1% CH 402

MARGIN_DRAM1P8_A0
MARGIN_DRAM1P8_A1

64 63 62 IN PMBUS_EXT_CLK
R582 0 OHM 5% 201 CH
PMBUS_EXT_CLK_MM_DRAM1P8

64 63 62 BI PMBUS_EXT_DATA
R583 0 OHM 5% 201 CH
PMBUS_EXT_DATA_MM_DRAM1P8

U409 IC
MCP4562
X864019-001
DFN9

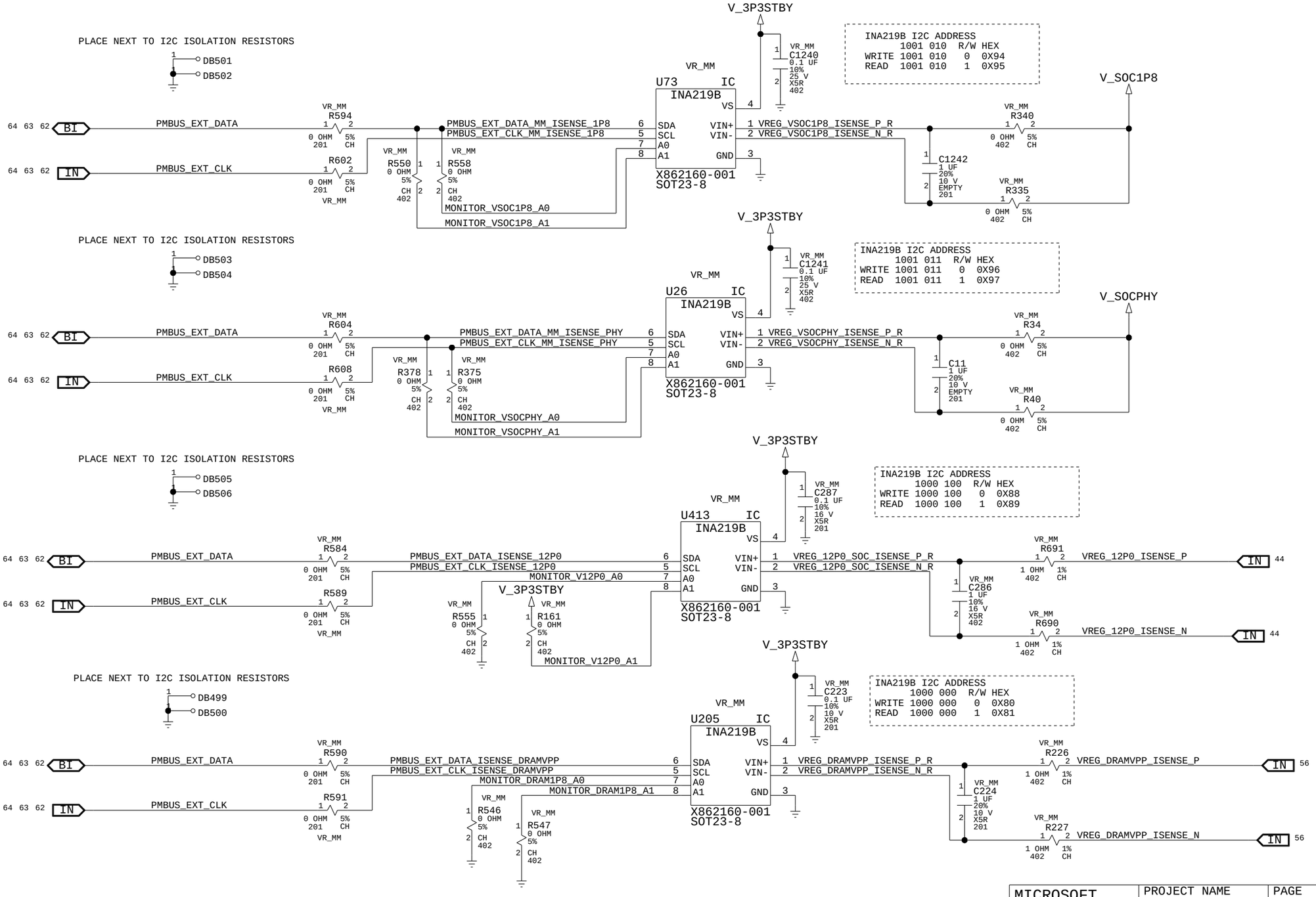
HVC/A0	1		
A1	7		
SCL	2		
SDA	3		
VDD	8		
P0B	6	VREG_DRAM1P8_FB	OUT 56
P0W	5	VREG_DRAM1P8_FB_MID	OUT 56
VSS	4		
MPAD	9		

V_3P3STBY
C1739 0.1 UF 10% 10 V X5R 201

50KOHM, POWERS UP AT MIDSCALE

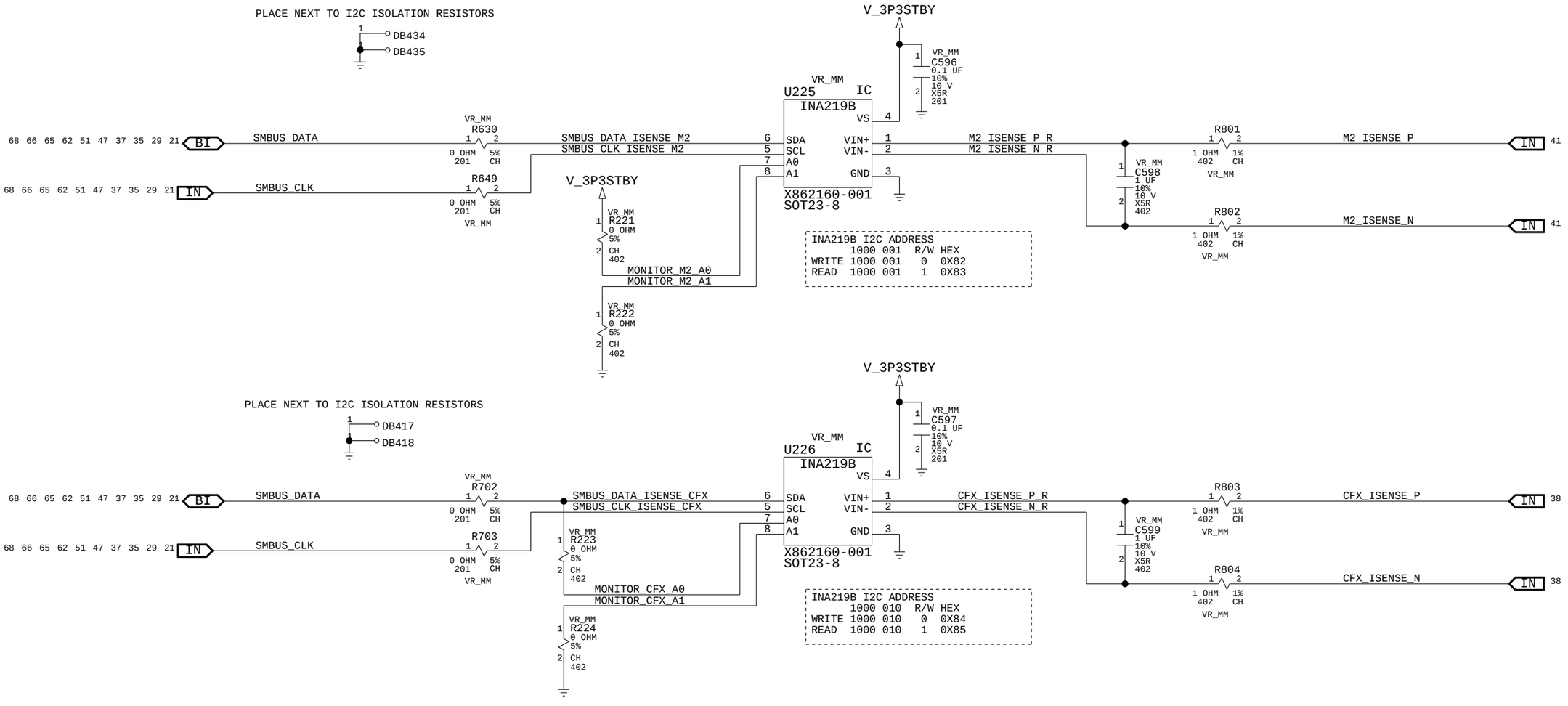
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	63/76	63/76	C	0.12

DEBUG: MONITOR V_SOC1P8, V_SOCPHY, V_12P0, V_DRAM1P8



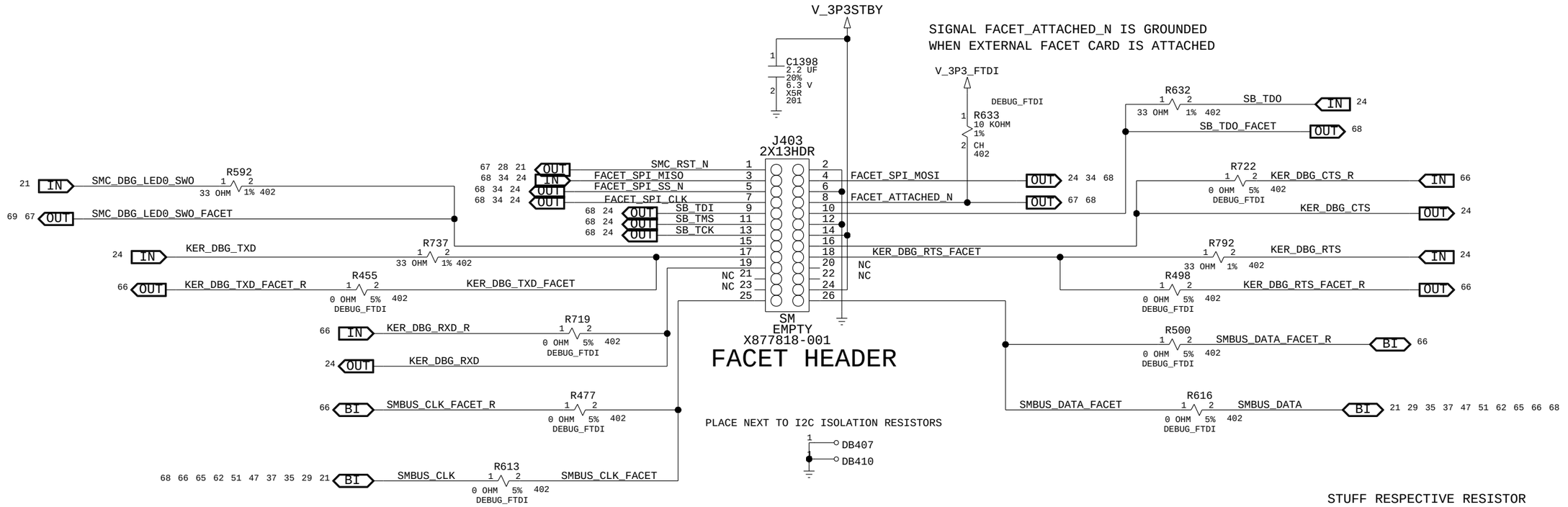
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	64/76	64/76	C	0.12

DEBUG: MONITOR M.2. CFEXPRESS



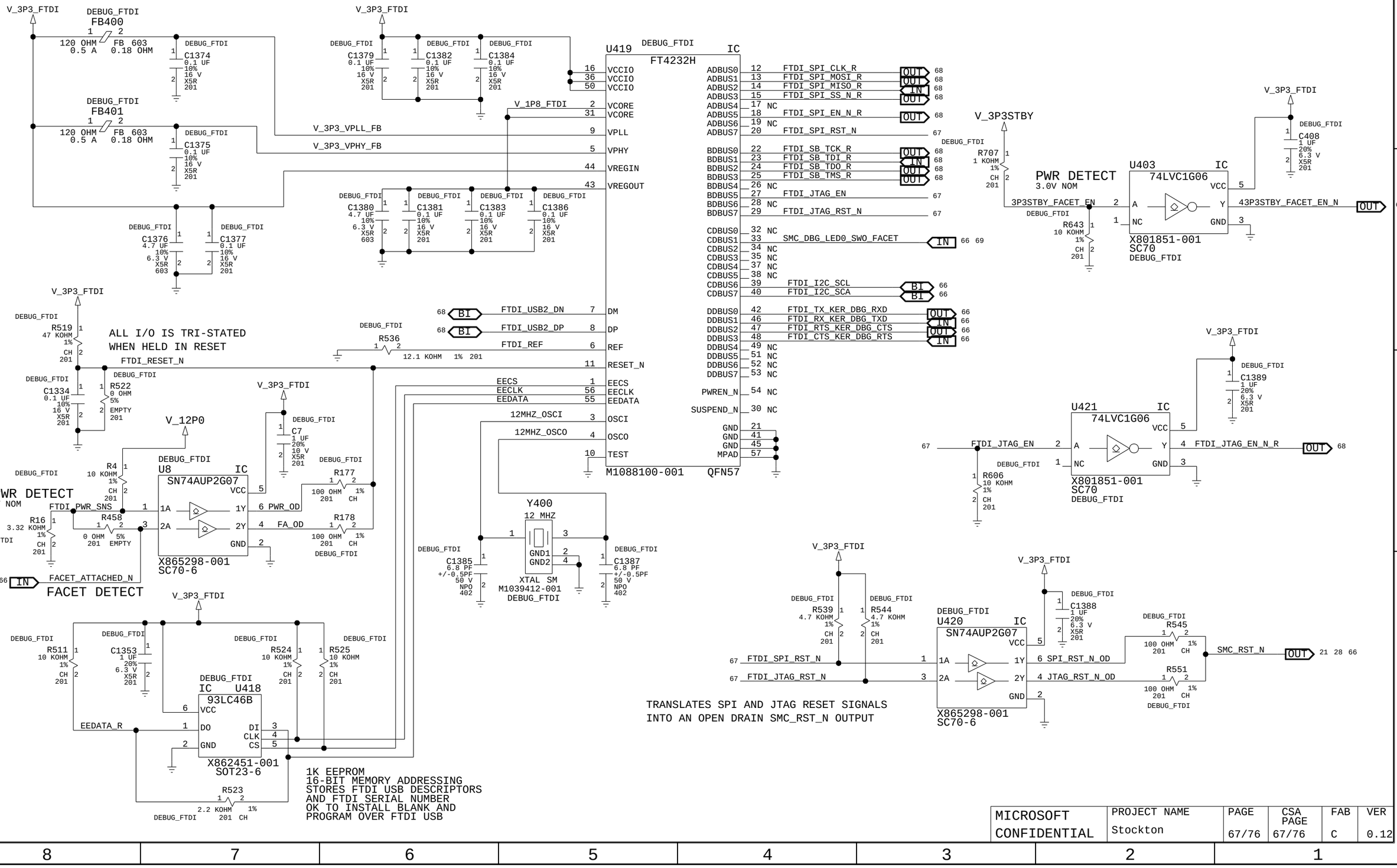
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	VER
	Stockton	65/76	65/76	0.12

DEBUG: FACET HEADER



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	66/76	66/76	C	0.12

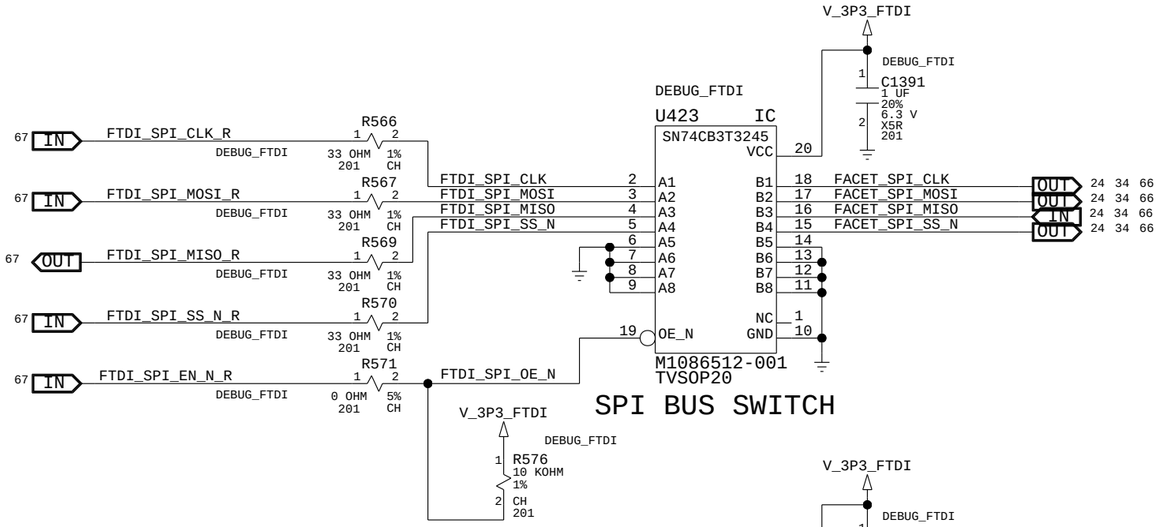
DEBUG: FTDI BRIDGE



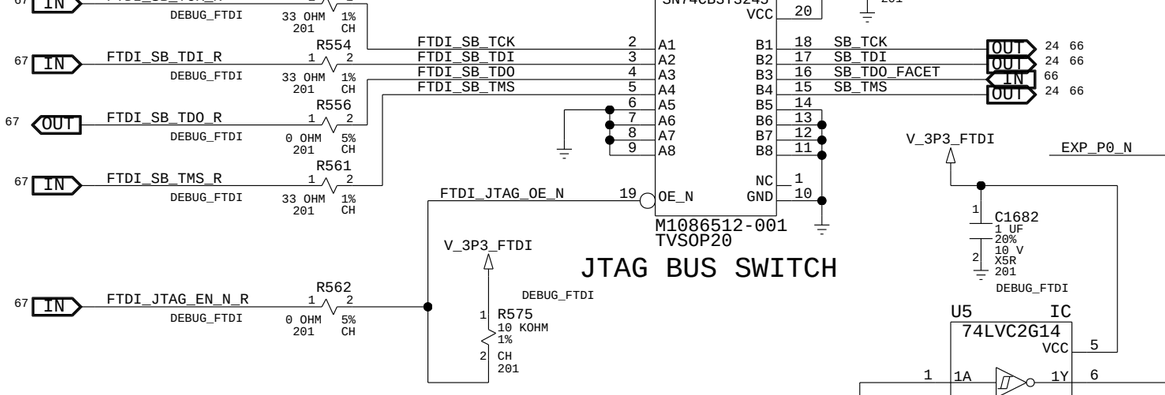
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	67/76	67/76	C	0.12

DEBUG: FTDI BUFF, USB, PWR

SPI BUS SWITCH



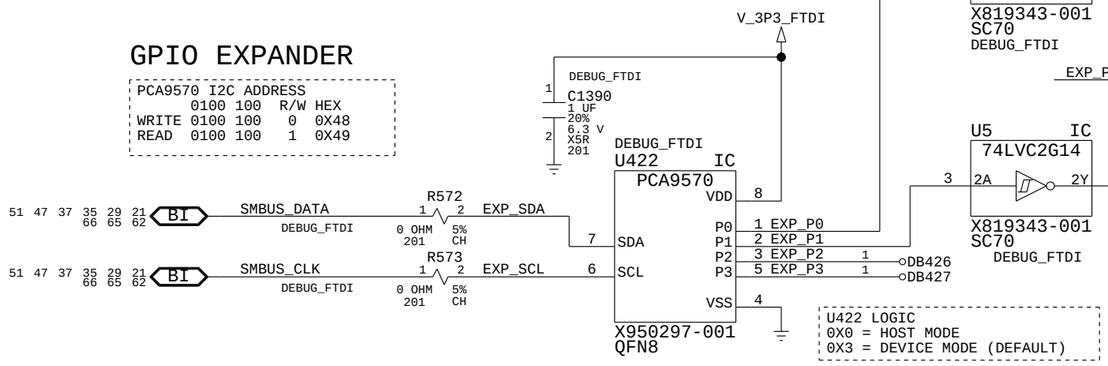
JTAG BUS SWITCH



GPIO EXPANDER

PCA9570 I2C ADDRESS

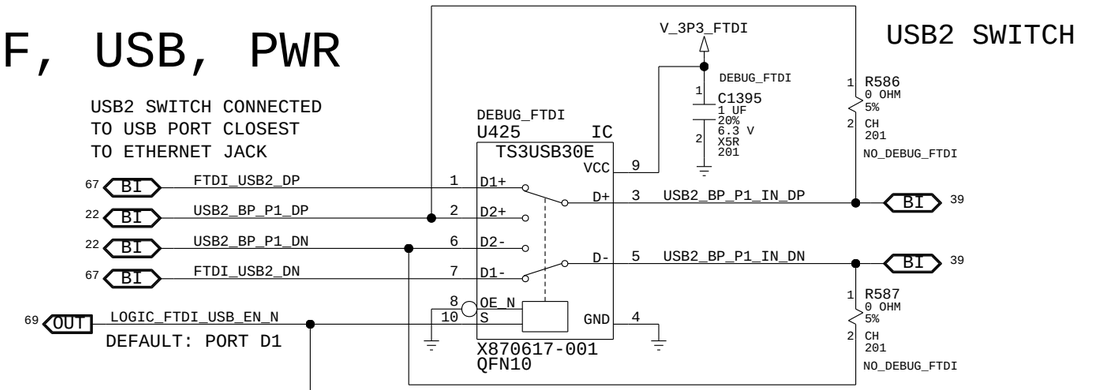
	0100 100	R/W	HEX
WRITE	0100 100	0	0X48
READ	0100 100	1	0X49



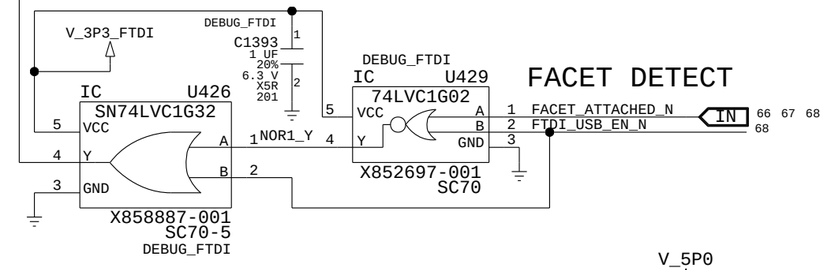
U422 LOGIC
0X0 = HOST MODE
0X3 = DEVICE MODE (DEFAULT)

USB2 SWITCH

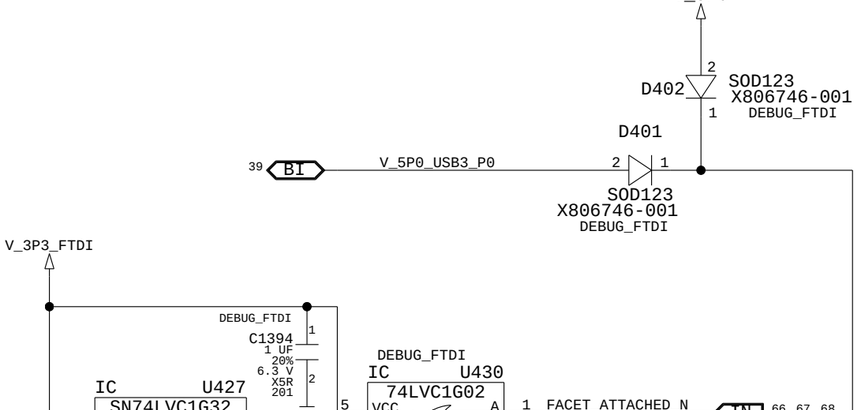
USB2 SWITCH CONNECTED
TO USB PORT CLOSEST
TO ETHERNET JACK



FACET DETECT

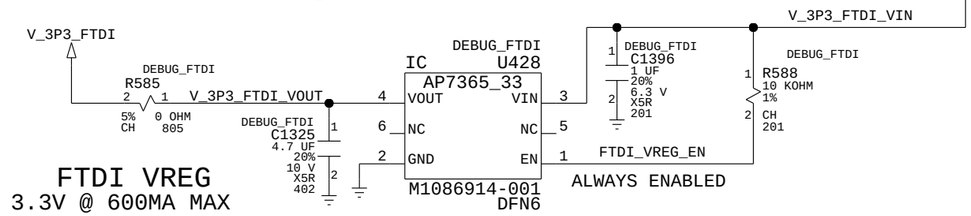


FACET DETECT



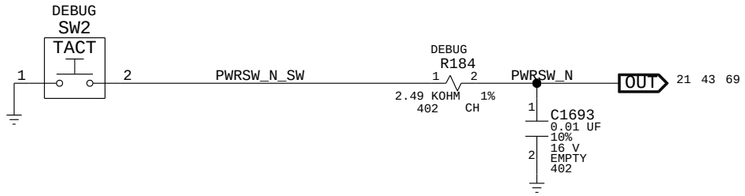
FTDI VREG

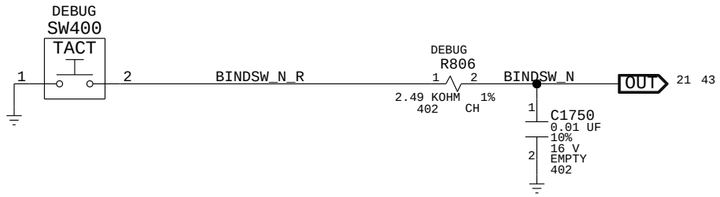
3.3V @ 600MA MAX

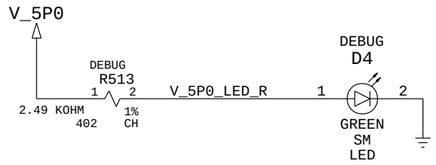


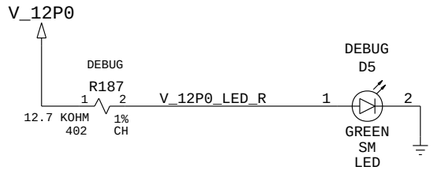
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	68/76	68/76	C	0.12

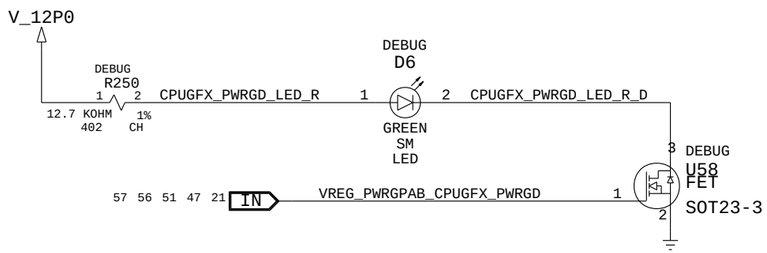
DEBUG: SWITCHES, LEDS

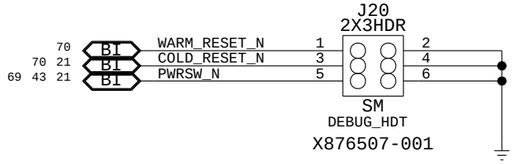


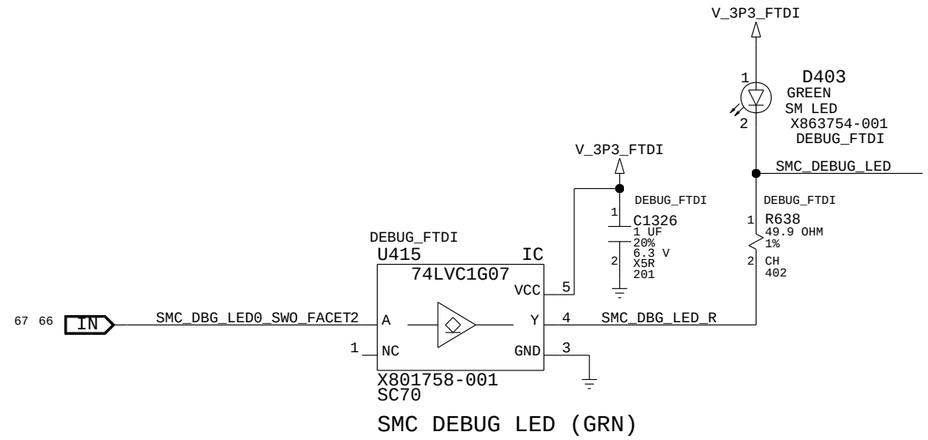




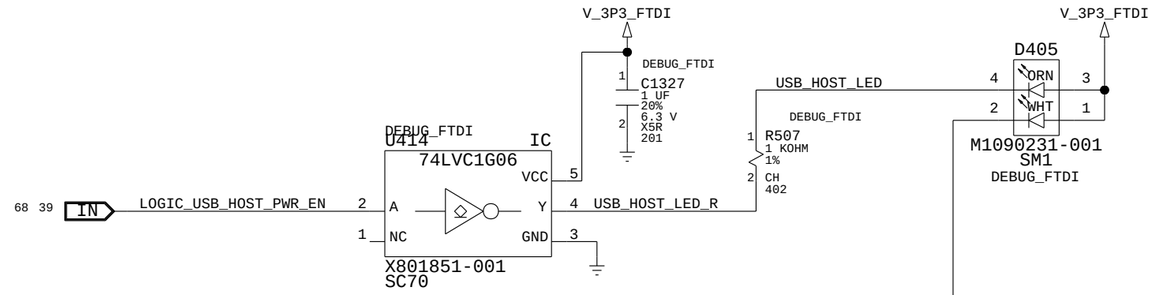




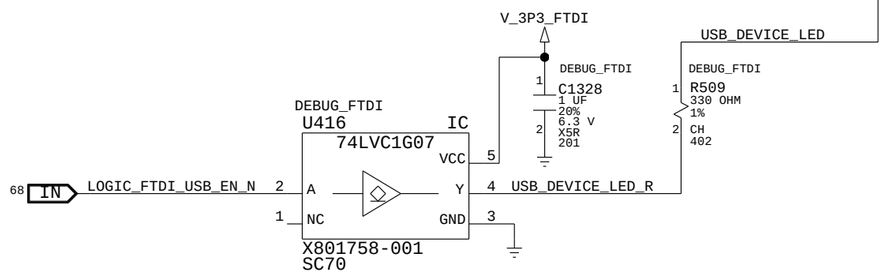




SMC DEBUG LED (GRN)



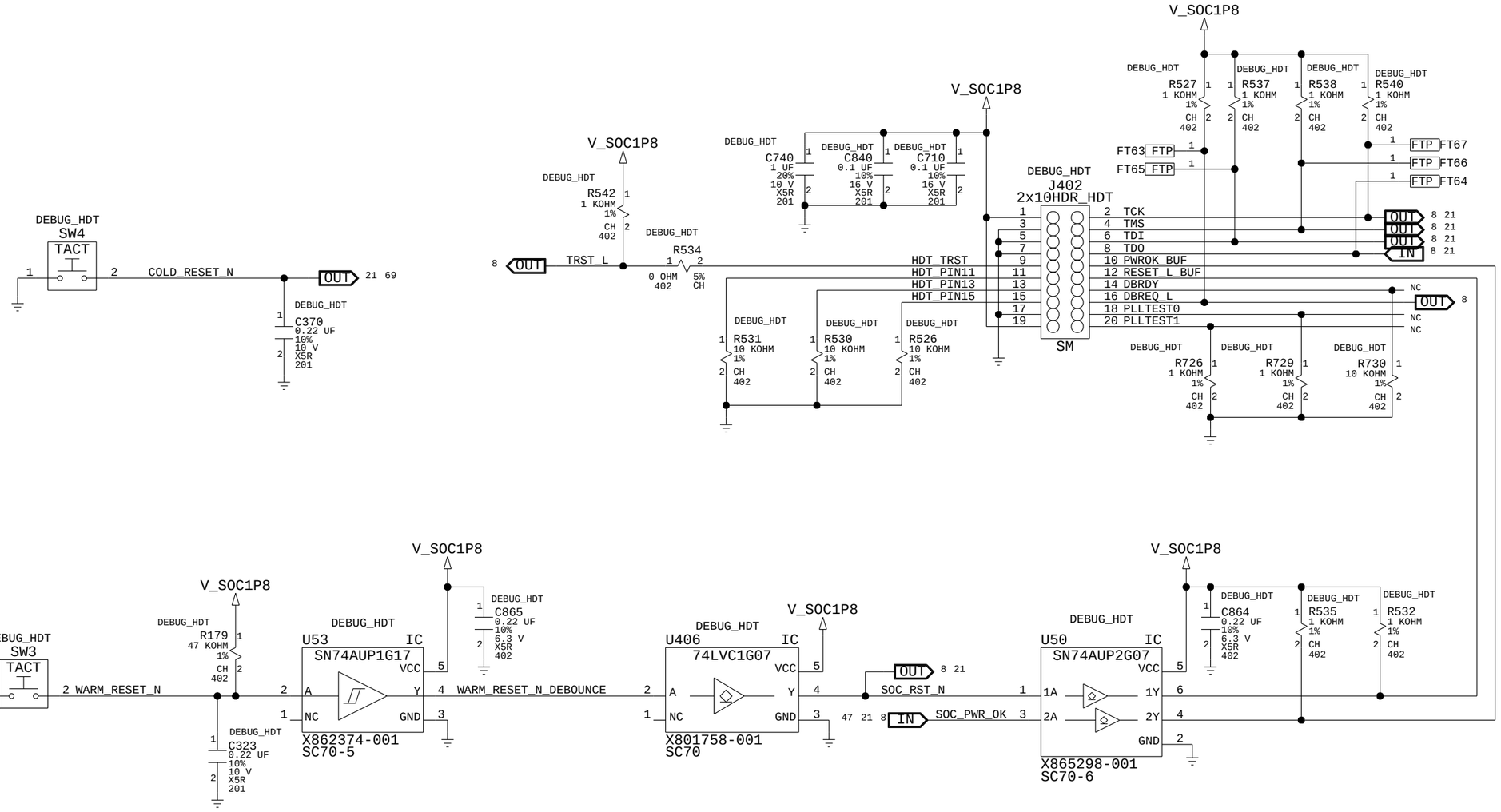
USB HOST MODE LED (ORG)



USB DEVICE MODE LED (WHT)

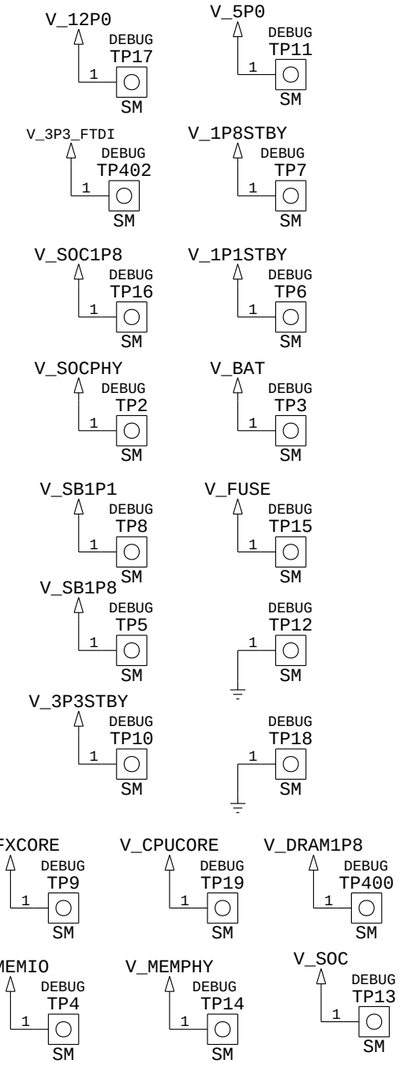
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	69/76	69/76	C	0.12

DEBUG: HDT



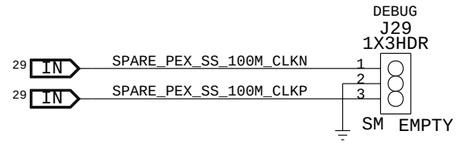
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	70/76	70/76	C	0.12

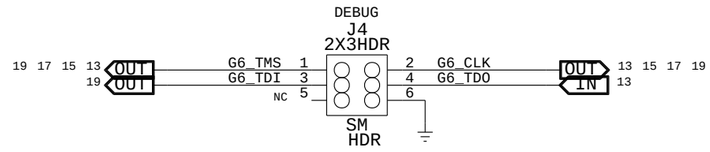
DEBUG: VR HEADERS, TEST POINTS, CONNECTORS



NOTE: THESE TEST POINTS ARE NOT TO BE USED FOR VOLTAGE REGULATOR QUALIFICATION TEST POINTS

PCIE CONNECTORS

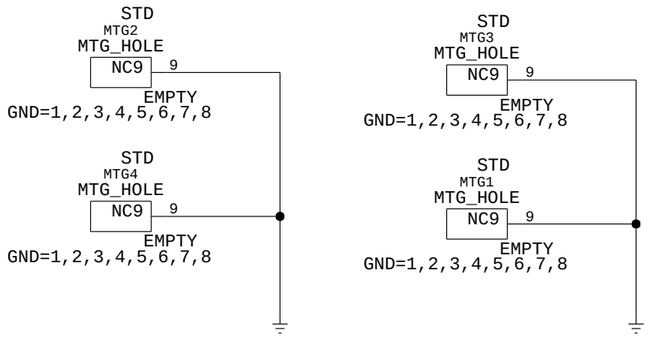




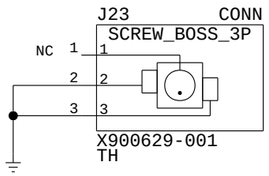
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	71/76	71/76	C	0.12

LABELS AND MOUNTING

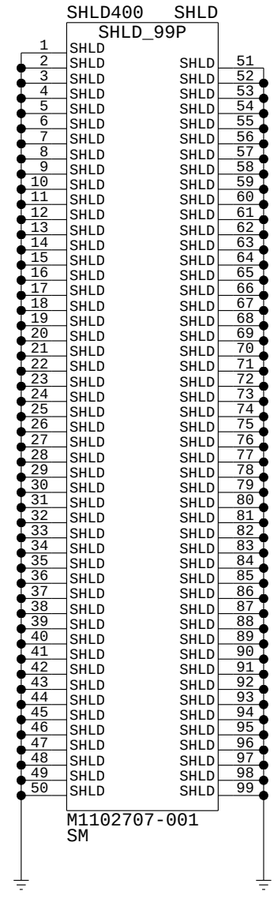
HEAT SINK MOUNTING HOLES



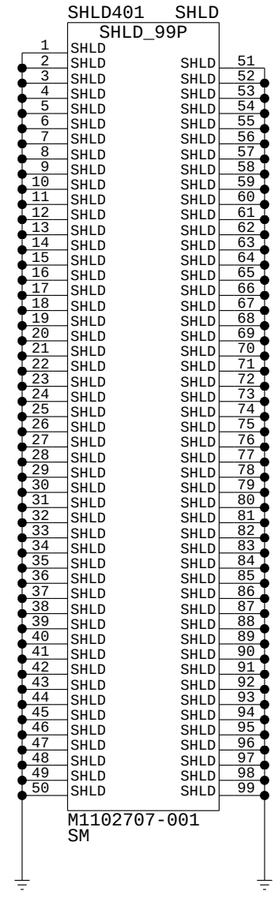
SCREW BOSS



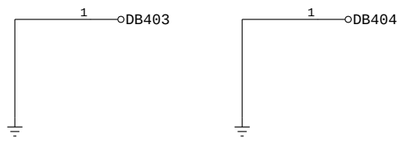
TOP BOARD LEVEL SHIELD



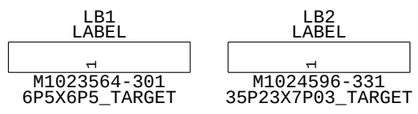
BOTTOM BOARD LEVEL SHIELD



GND PADS FOR HEATSINK ALIGNMENT PINS



INTELLIGENT SERIAL NUMBER TARGET



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1111890-001	FR4	PCB1	PCB,STOCKTON,FAB B,8 LAYERS,GI	PCB_GI
MXXXXXXX-001	FR4	PCB1	PCB,STOCKTON,FAB B,8 LAYERS,OSP	PCB_OSP

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	VER
	Stockton	72/76	72/76	0.12

BOM DEFINITIONS

BOM	DEFINITION
AUDIO	INCLUDES COMPONENTS FOR THE STANDARD AUDIO SOLUTION
AUDIO_PREM	INCLUDES COMPONENTS FOR THE PREMIUM SE/LE SPEAKER SOLUTION
COMMON	ALL COMPONENTS WITH NO BOM PROPERTY
DEBUG	COMPONENTS REQUIRED FOR BRING UP & DEBUG
DEBUG_HDT	HDT-RELATED DEBUG COMPONENTS
DEBUG_SHUNT	COMPONENTS WHICH ARE ON DEBUG BOARDS, BUT ARE REMOVED/SHORTED ON RETAIL
EMMC_BASE	DUMMY PLACE HOLDER FOR EMMC DEVICE & RESISTORS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM
EMMC_HYNIX_16NM	HYNIX EMMC DEVICE
EMMC_SAMSUNG_14NM	SAMSUNG EMMC DEVICE
EMMC_TOSHIBA_15NM	TOSHIBA EMMC DEVICE
SANTO_BASE	DUMMY PLACE HOLDER FOR SANTO SB. NEVER USE THIS IN THE RECIPE FILE. USE ONE OF THESE INSTEAD: SANTO_DEV OR SANTO_RETAIL
SANTO_DEV	DEBUG VERSION OF SANTO SB
SANTO_RETAIL	RETAIL VERSION OF SANTO SB
M2_ONLY	POPULATE TO SUPPORT AN M.2 INTERFACE
NO_M2	POPULATE WHEN THERE IS NO M2. INTERFACE
PCB_GI	FAB TYPE: GOLD
PCB_OSP	FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE GREEN SOLDERMASK
PCB_OSP_BLACK	FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE BLACK SOLDERMASK
RTC_RETAIL	RTC CIRCUIT IMPLEMENTATION FOR RETAIL BOARDS
RTC_XDK	RTC CIRCUIT IMPLEMENTATION FOR XDK BOARDS
SOC_BASE	DUMMY PLACE HOLDER FOR SOC. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM
SOC_EMPTY	DOES NOT STUFF SPARKMAN
SOC_INCLUDE	STUFFS SPARKMAN
VR_FIXED	SET ALL VRS TO FIXED VOLTAGES (NON-MARGINED). EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_MM
VR_MM	ALLOWS MOST VRS TO BE MARGINED FOR M&M BOARDS. EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_FIXED
RETAIL	COMPONENTS STUFFED FOR A RETAIL CONSOLE. DO NOT USE WITH DEBUG
DEBUG_PHASE	PHASES USED FOR INITIAL POWER UP
DRAM_VPP_DEBUG	SEPARATES SOC 1.8V AND DRAM 1.8V. USE IF MARGINING SOC 1.8V OUTSIDE OF DRAM 1.8V LIMITS. NEVER USE WITH DRAM_VPP_RETAIL
DRAM_VPP_RETAIL	COMBINES SOC 1,8V AND DRAM1.8V USEING A FILTER NETWORK. NEVER USE WITH DRAM_VPP_DEBUG
DEBUG_FTDI	STUFFS INTERCEPT CIRCUITRY FOR DEBUG
NO_DEBUG_FTDI	BYPASSES INTERCEPT CIRCUITRY FOR NO DEBUG
SPI_FLASH_BASE	DUMMY PLACE HOLDER FOR SPI FLASH. NEVER USE THIS IN THE RECIPE FILE.
SPI_FLASH_MACRONIX	STUFFS MACRONIX SPI FLASH
SPI_FLASH_WINBOND	STUFFS WINBOND SPI FLASH

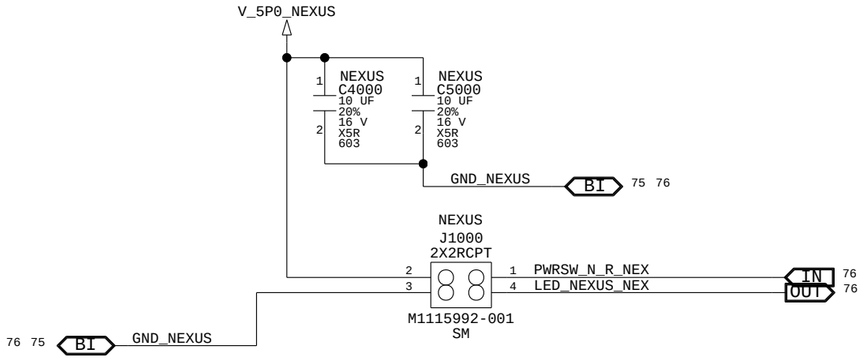
STOCKTON_NEXUS

NEXUS BOARD IS CO-PANELED WITH MAIN BOARD

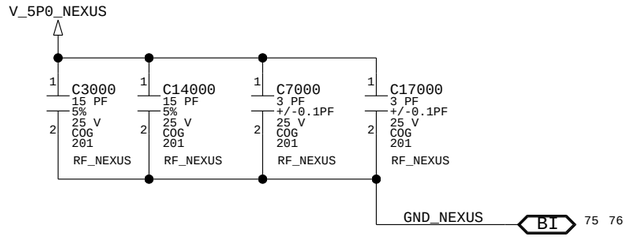
RULES: (APPLIED WHEN POSSIBLE)

1.) MSB TO LSB IS TOP TO BOTTOM
2.) WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
3.) ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
4.) AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
5.) LANED SIGNALS ARE GROUPED ON SYMBOLS
6.) TRANSIMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
7.) SUFFIX V_ IS USED FOR VOLTAGE RAIL SIGNAL NAMES
8.) SUFFIX _DP AND _DN ARE USED FOR DIFFERIENTAL PAIRS
9.) UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
10.) SUFFIX _N FOR ACTIVE LOW OR N JUNCTION
12.) SUFFIX _P FOR P JUNCTION
13.) SUFFIX _EN FOR ENABLE
14.) 'CLK' FOR CLOCKS, 'RST' FOR RESETS
15.) PWRGD FOR POWER GOOD

B2B CONN AND LABELS



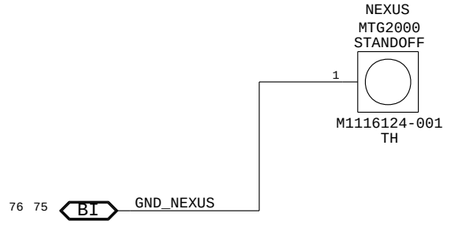
B2B CONNECTOR



LB3
LABEL

M1023564-801
6.35MM X 6.35MM
NEXUS

MOUNTING STANDOFF

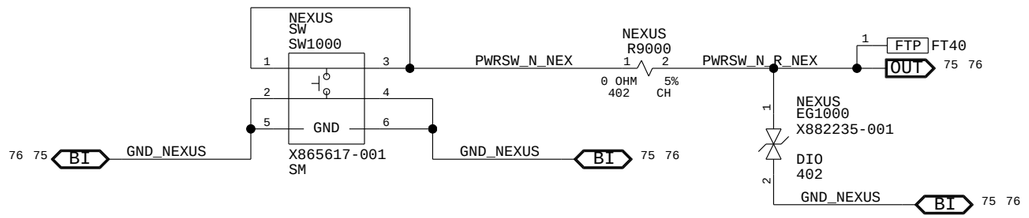


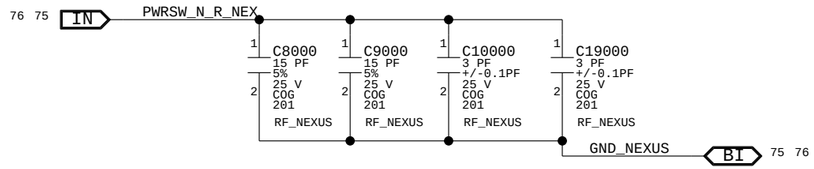
MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1110461-001	FR4	PCB1	PCB,STOCKTON,2LAYERS,NEXUS,FAB A	PCB

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	75/76	75/76	C	0.12

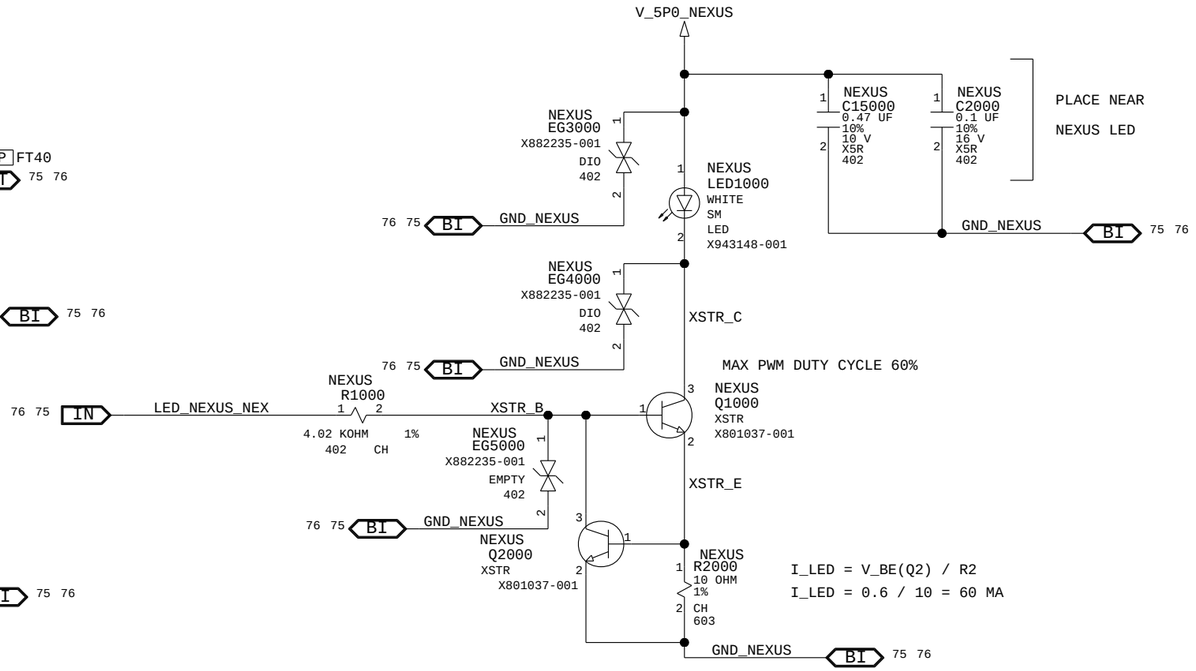
NEXUS LED AND POWER SWITCH

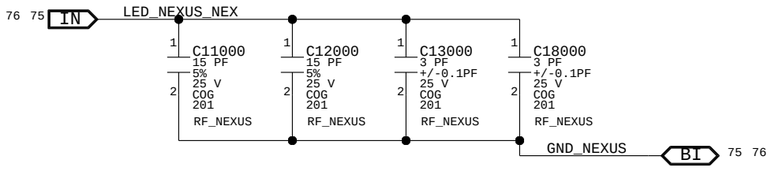
POWER SWITCH





NEXUS LED LIGHTING





MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Stockton	76/76	76/76	C	0.12