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[3]	SOC: VIDEO
[4]	SOC: POWER: MEMIO,CPUCORE,NBCORE,MISC
[5]	SOC: POWER: V_GFXCORE
[6]	SOC: POWER: VSS
[7]	SOC: POWER: VSS
[8]	SOC: MEMORY PARTITION F1 & F0
[9]	SOC: MEMORY PARTITION E1 & E0
[10]	SOC: MEMORY PARTITION D1 & D0
[11]	SOC: MEMORY PARTITION C1 & C0
[12]	SOC: MEMORY PARTITION B1 & B0
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[14]	SOC: DEBUG, SB SIGNALS, V_BAT
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[21]	MEMORY: CHANNEL B1
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[24]	MEMORY: CHANNEL C1
[25]	MEMORY: CHANNEL D0
[26]	MEMORY: CHANNEL D1
[27]	MEMORY: CHANNEL C/D DECOUPLING
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[33]	MEMORY: ADDITIONAL DECOUPLING
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[36]	KIC: SMC
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[40]	KIC: POWER
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[51]	CONN: FRONT PANEL, FAN, AUDIO
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[55]	VREGS: GFXCORE OUTPUT PHASE 1 & 2
[56]	VREGS: GFXCORE OUTPUT PHASE 3 & 4
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[58]	VREGS: MEMIO & MEMPHY
[59]	VREGS: MEMPHY OUTPUT
[60]	VREGS: MEMIO OUTPUT
[61]	VREGS: NBCORE
[62]	VREGS: V5P0
[63]	VREGS: V3P3, VSOC1P8
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[65]	VREGS: V_SB1P8, V_SB1P1
[66]	VREGS: V3P3 STANDBY
[67]	VREGS: V1P1 STANDBY, V1P8 STANDBY
[68]	STANDBY GATES
[69]	IR BLASTER
[70]	I2C
[71]	MARGIN: SOCPHY,SOC1P8,MEMIO,NBCORE
[72]	MONITOR: VSOC1P8, VSOCPHY, V12P0
[73]	CONN: FACET BOARD
[74]	CONN: SWITCHES
[75]	CONN: HDT
[76]	CONN: M.2
[77]	CLOCK BUFFER
[78]	PREMIUM SPEAKER (SE/LE)
[79]	DEBUG: VR HEADERS, TEST POINTS, CONNECTORS
[80]	LABELS AND MOUNTING
[81]	FRONT PANEL USB - NESTED PCB
[82]	BOM DEFINITIONS

CACTUS
REV 0.991
FAB G RETAIL

RULES: (APPLIED WHEN POSSIBLE)
1. MSB TO LSB IS TOP TO BOTTOM
2. WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
3. ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
4. AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
5. LANED SIGNALS ARE GROUPED ON SYMBOLS
6. TRANSIMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
7. SUFFIX _V IS USED FOR VOLTAGE RAIL SIGNAL NAMES
8. SUFFIX _DP AND _DN ARE USED FOR DIFFERIENTAL PAIRS
9. UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
10. SUFFIX _N FOR ACTIVE LOW OR N JUNCTION
12. SUFFIX _P FOR P JUNCTION
13. SUFFIX _EN FOR ENABLE
14. 'CLK' FOR CLOCKS, 'RST' FOR RESETS
15. PWRGD FOR POWER GOOD
16. REV AND FAB ARE SET USING CUSTOM VARIABLES
    TOOLS>OPTIONS>VARIABLES

DRAWING
Thu Apr 20 16:18:47 2017

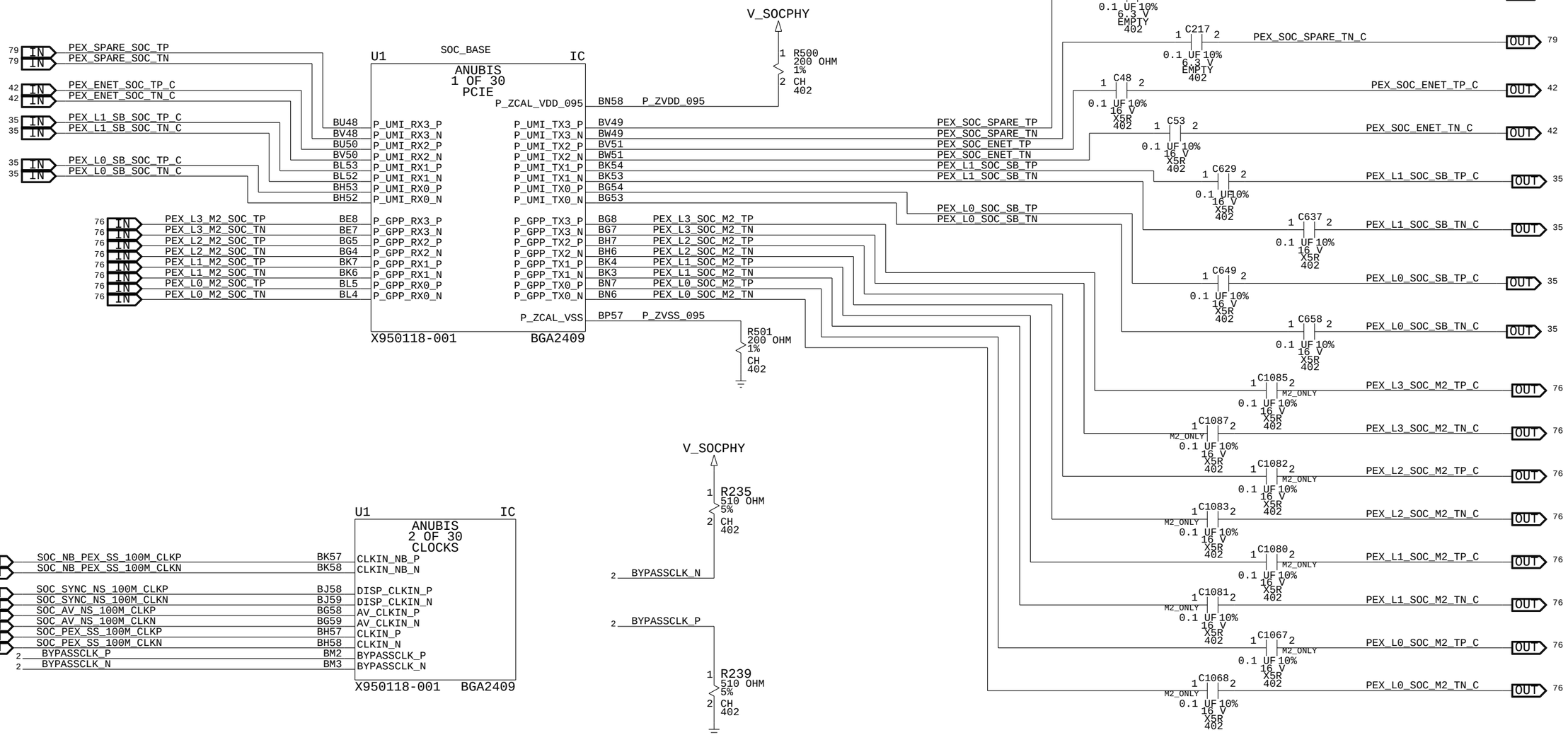
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	1/82	1/82	G-R	0.991

SOC:PCIEX,CLOCKS

NOTES:

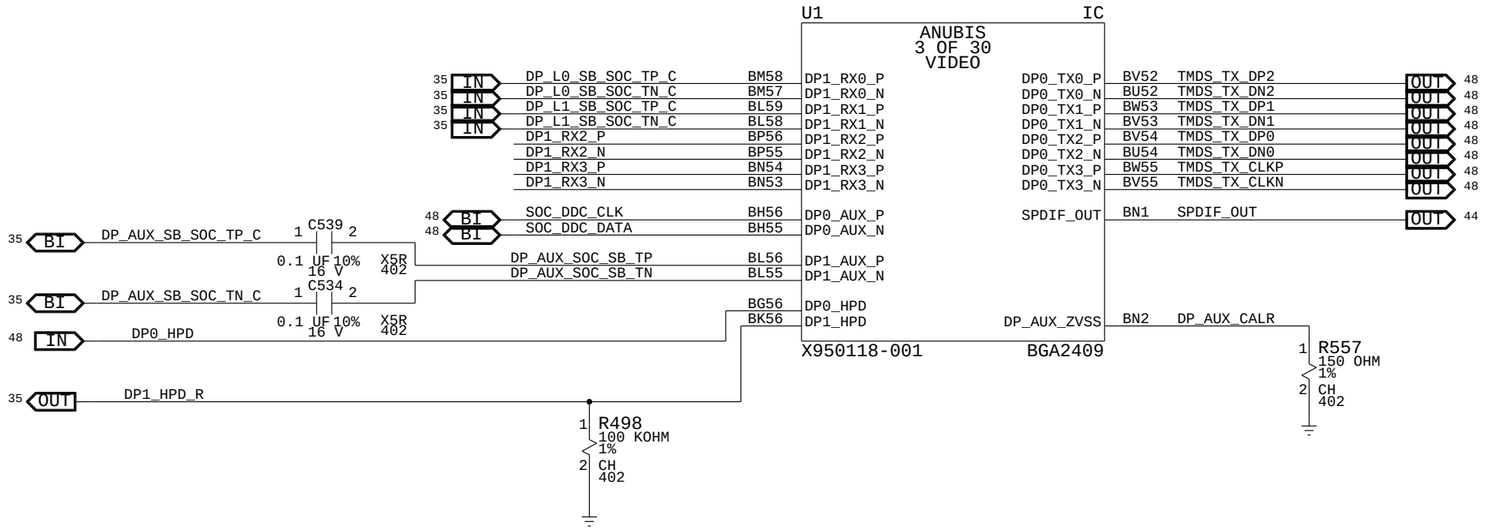
1.TO SUPPORT PCIE SPARE LANE INTERFACE (J28), POPULATE C215 AND C217

2.SEE PAGES 77 AND 79 FOR ADDITIONAL PCIE SPARE LANE INFORMATION



MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X950118-001	IC	U1	PROCSR-CPU-GPU,SM,1.0GHZ,BGA2049,ANUBIS	SOC_INCLUDE
X950118-001	EMPTY	U1	PROCSR-CPU-GPU,SM,1.0GHZ,BGA2049,ANUBIS	SOC_EMPTY

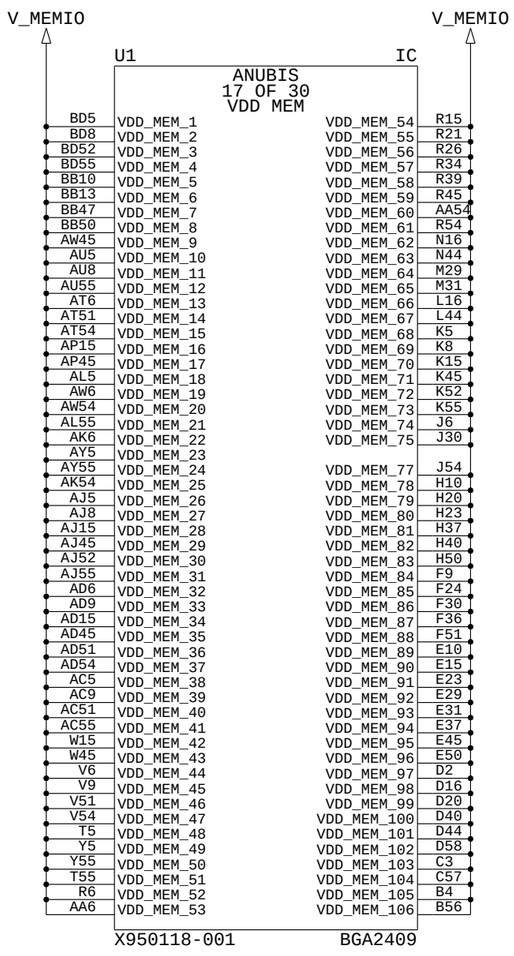
SOC: VIDEO

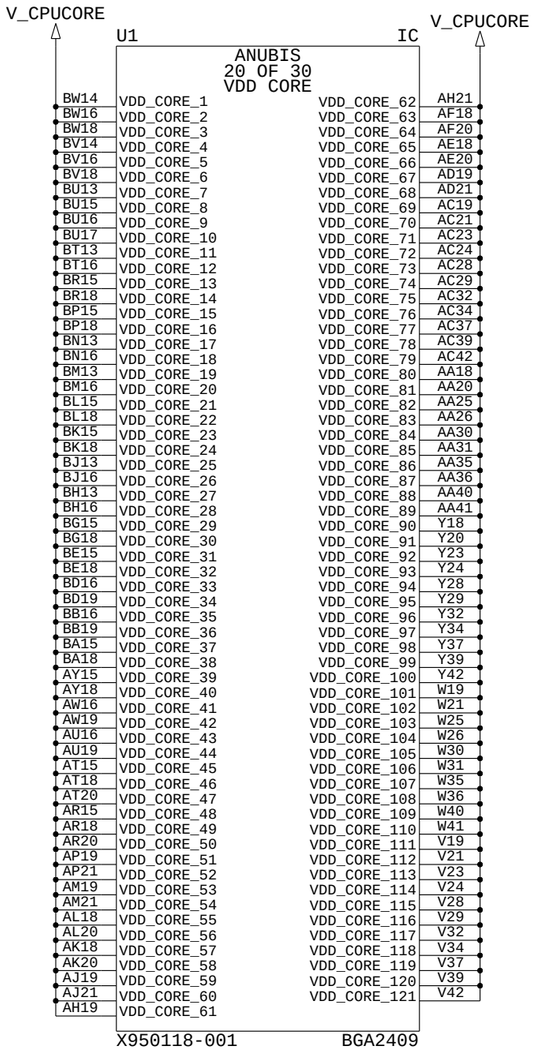


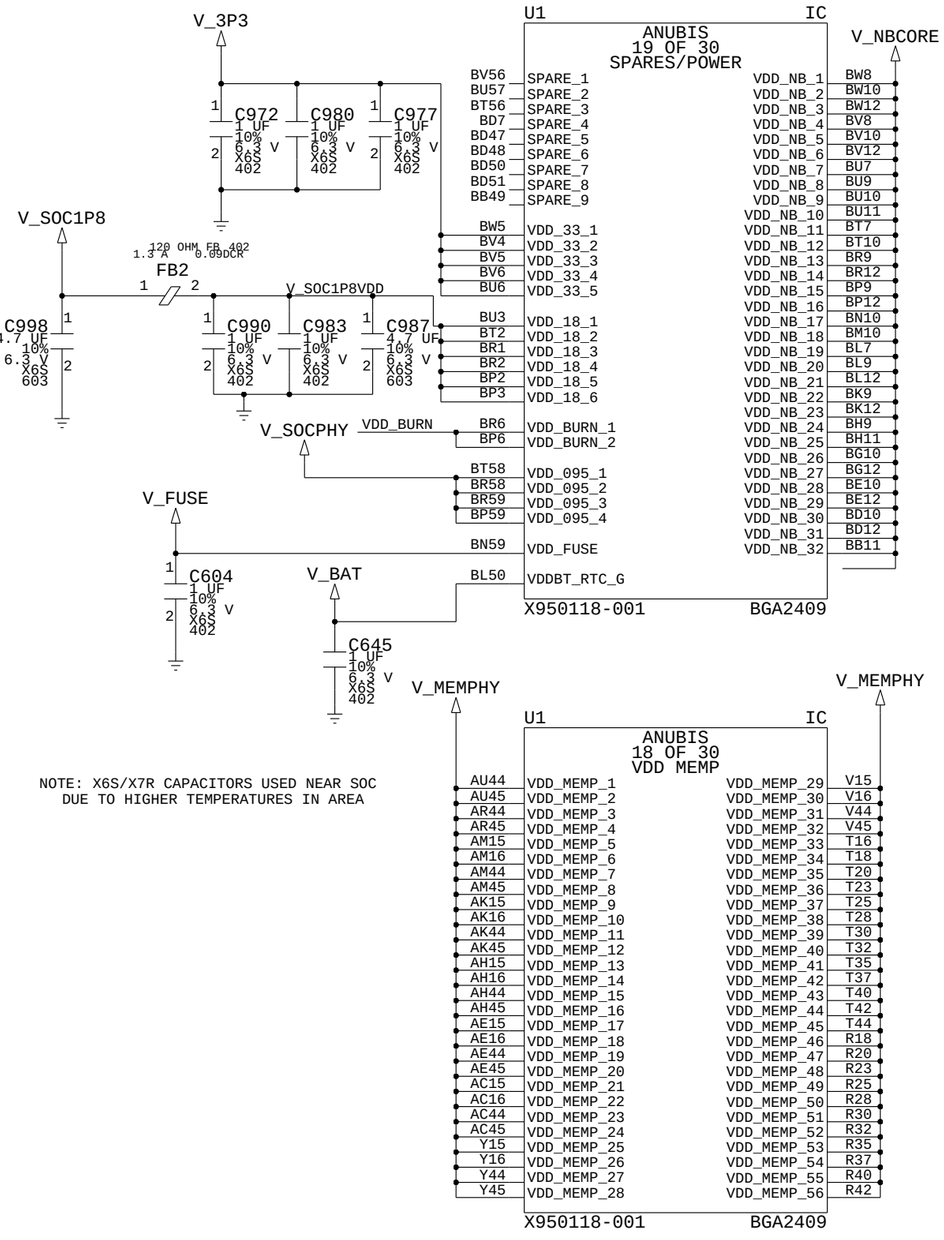
DVI PCB ROUTING ORDERING	DP PCB ROUTING ORDERING	PIN NAME
TMDS CLOCK -	DP LANE 3 -	DP0_TX3_N
TMDS CLOCK +	DP LANE 3 +	DP0_TX3_P
TMDS DATA0 -	DP LANE 2 -	DP0_TX2_N
TMDS DATA0 +	DP LANE 2 +	DP0_TX2_P
TMDS DATA1 -	DP LANE 1 -	DP0_TX1_N
TMDS DATA1 +	DP LANE 1 +	DP0_TX1_P
TMDS DATA2 -	DP LANE 0 -	DP0_TX0_N
TMDS DATA2 +	DP LANE 0 +	DP0_TX0_P

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	3/82	3/82	G-R	0.99

SOC: POWER: MEMIO,MEMPHY,CPUCORE,NBCORE,MISC



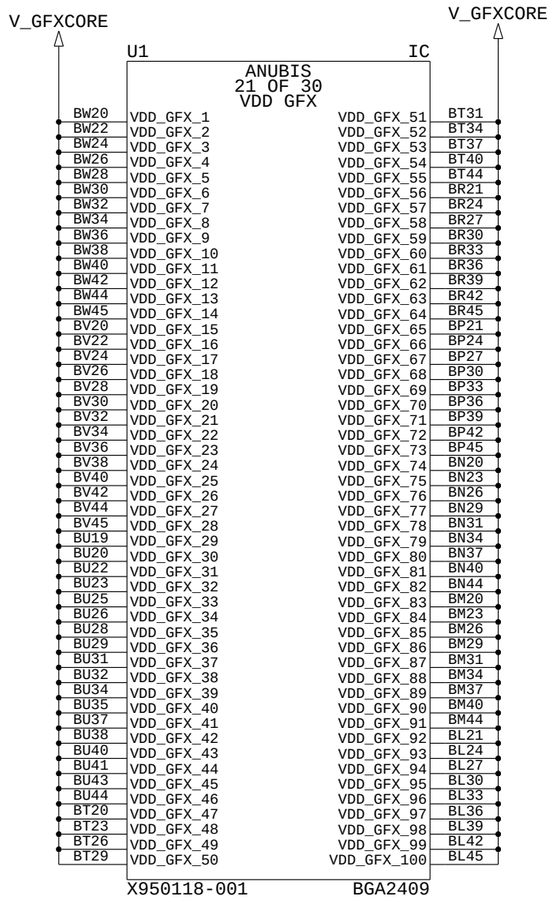


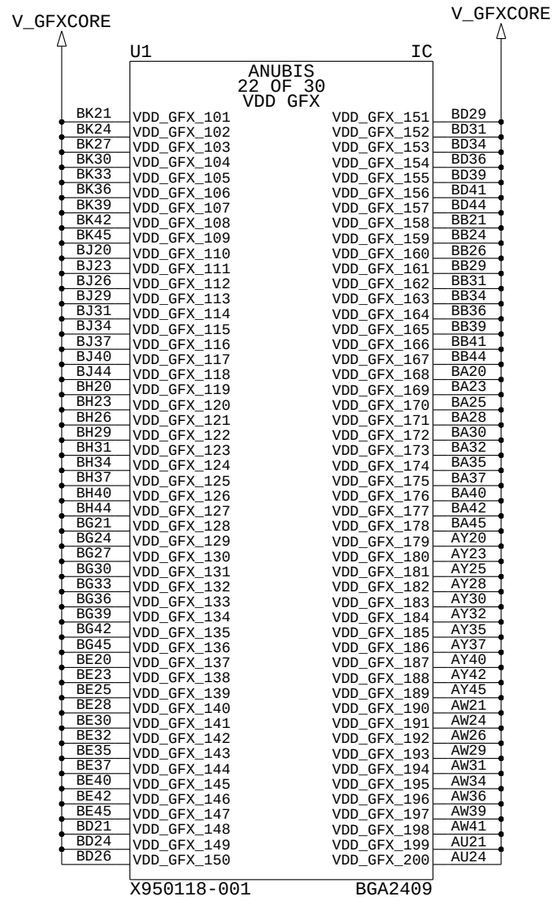


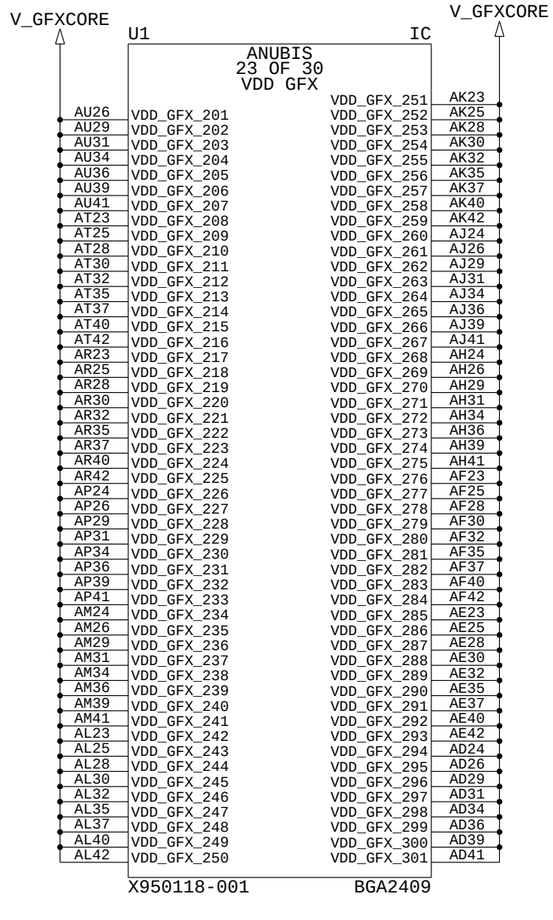
NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	4/82	4/82	G-R	0.991

SOC: POWER: GFXCORE

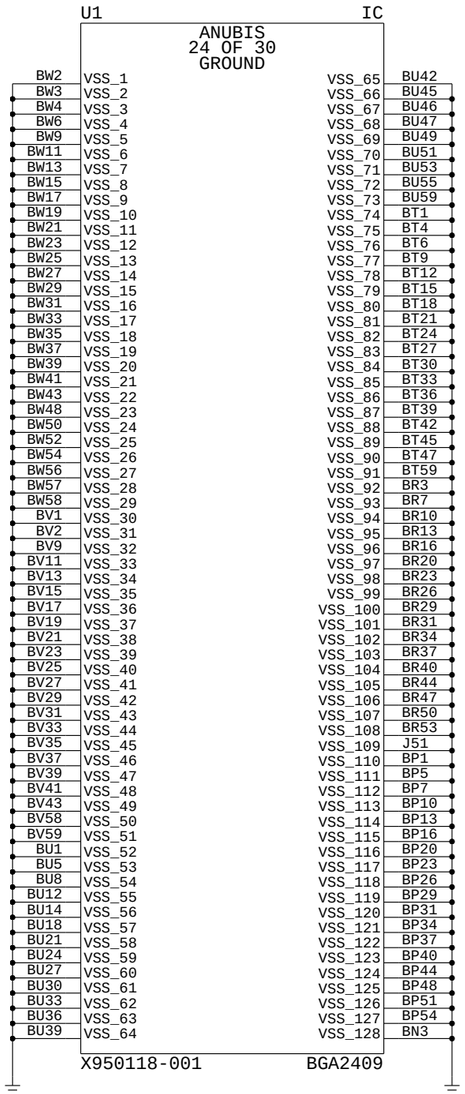


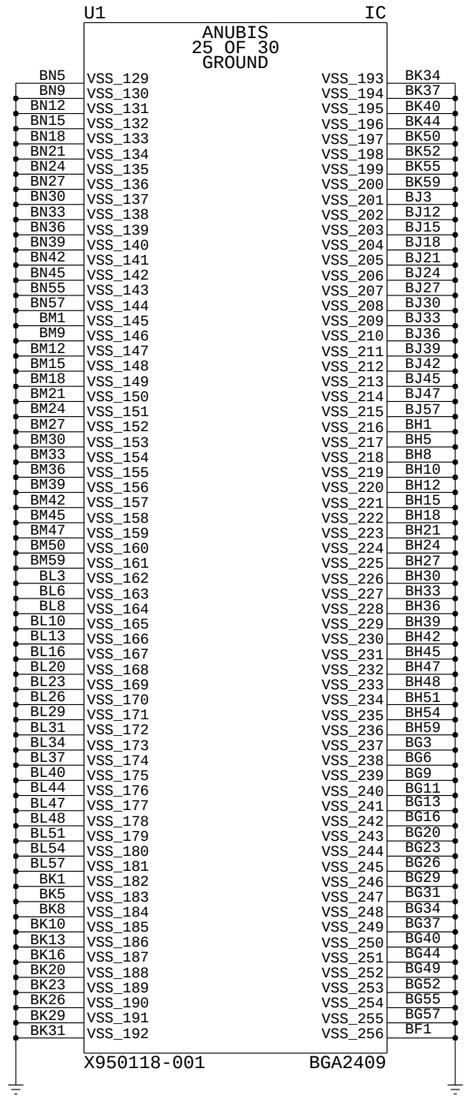


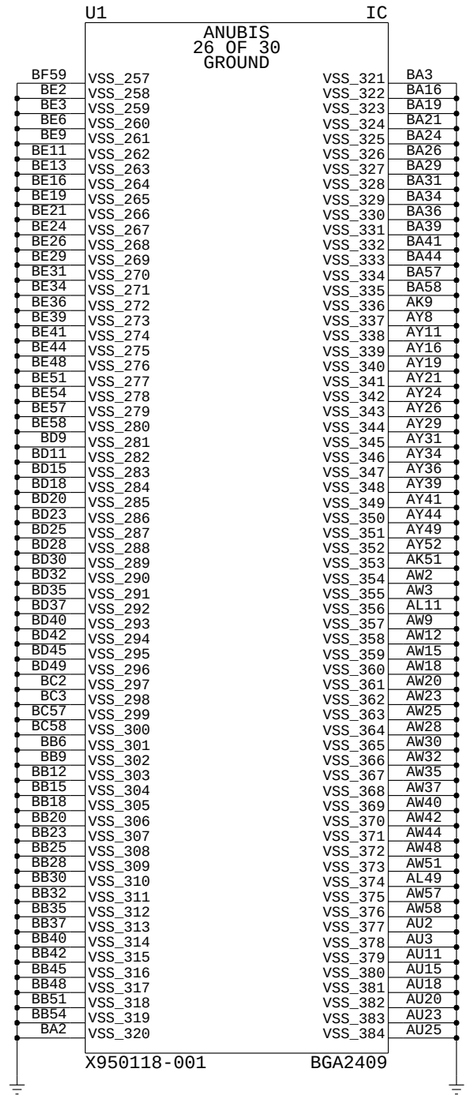


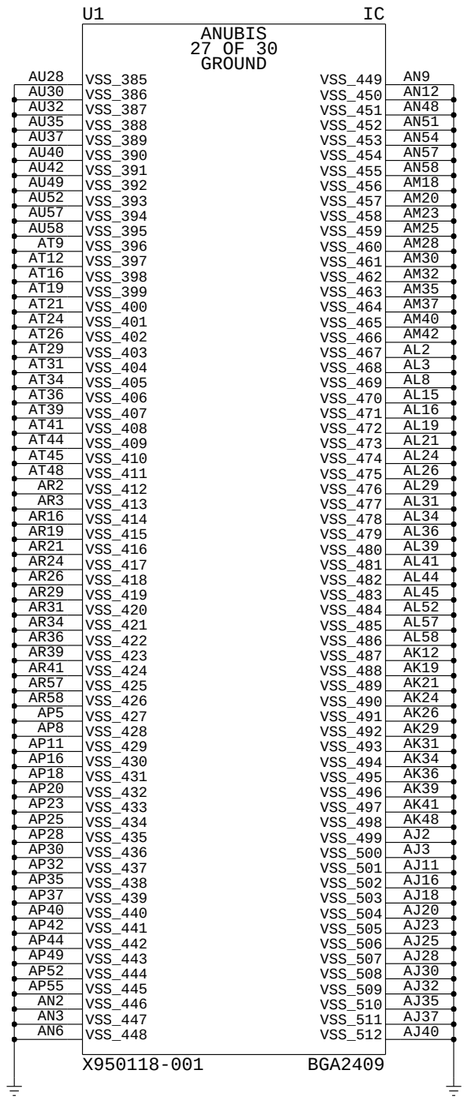
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	5/82	5/82	G-R	0.991

SOC: POWER: VSS



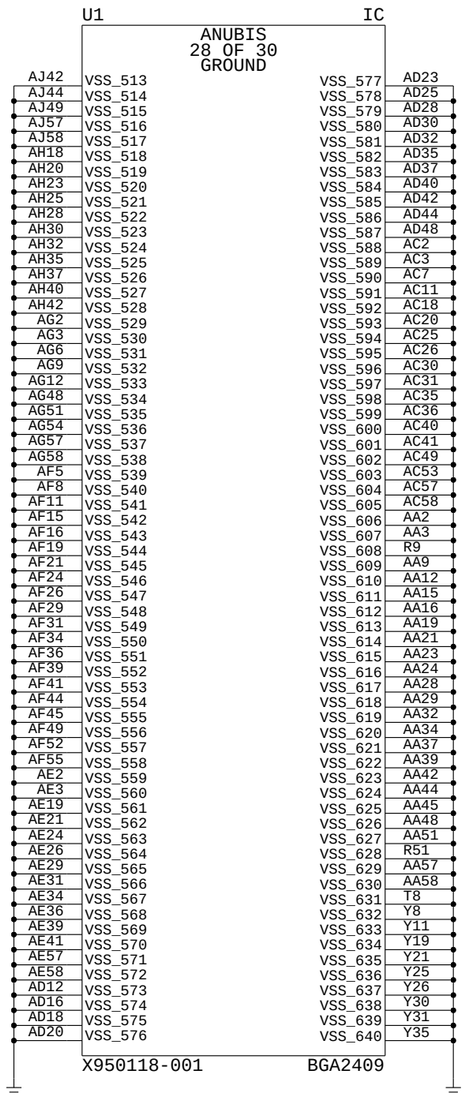


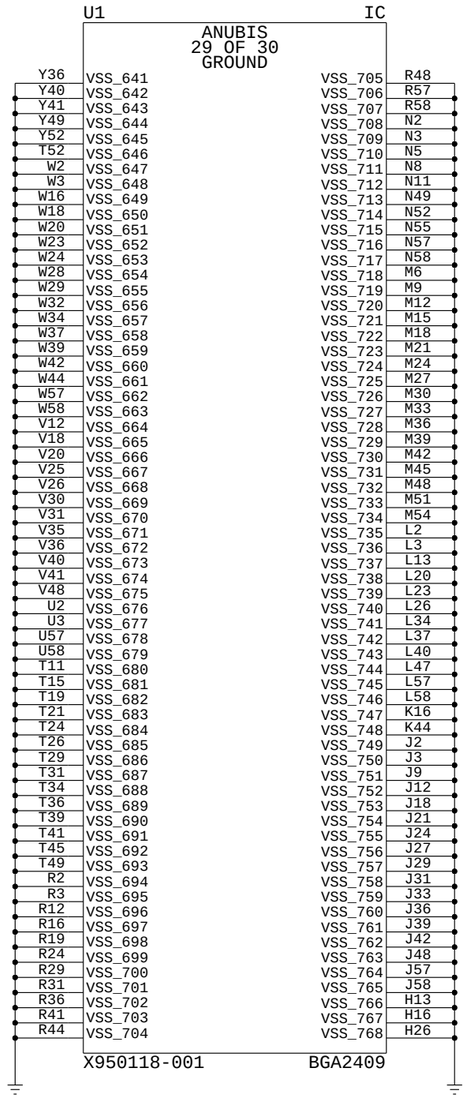


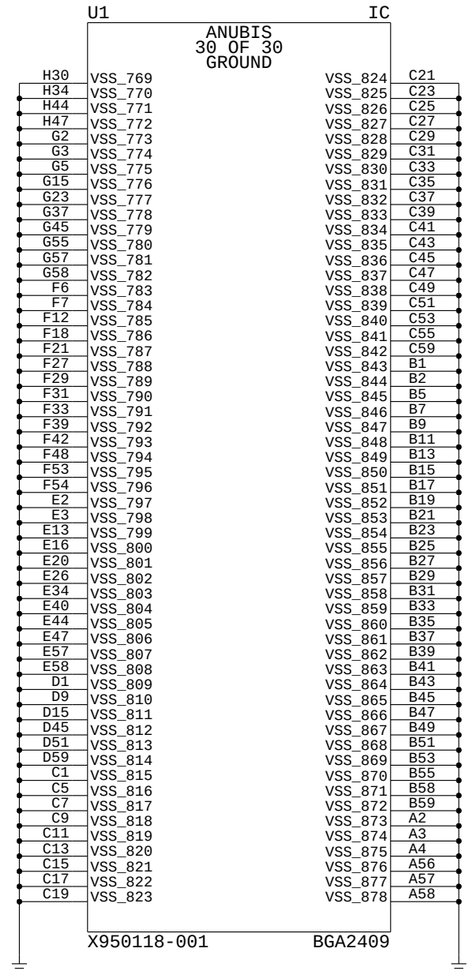


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	6/82	6/82	G-R	0.991

SOC: POWER: VSS

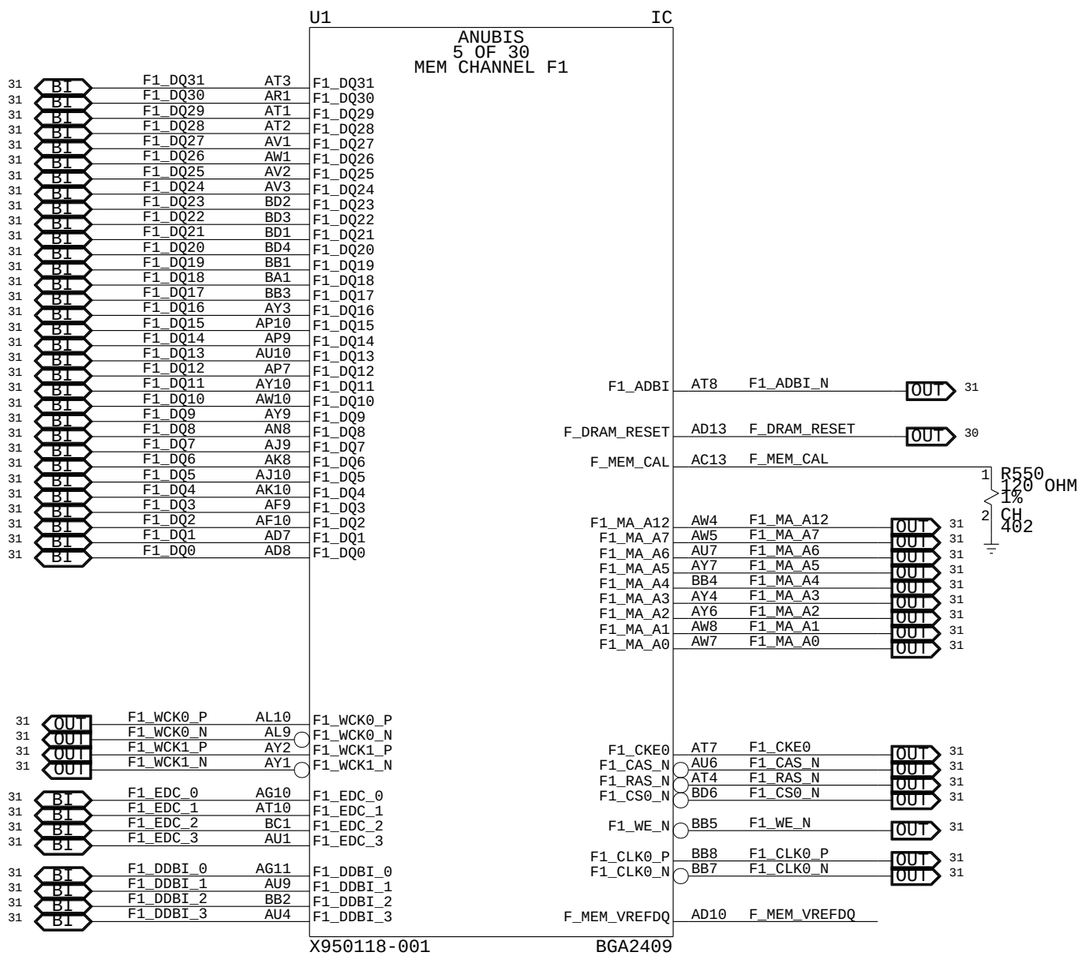


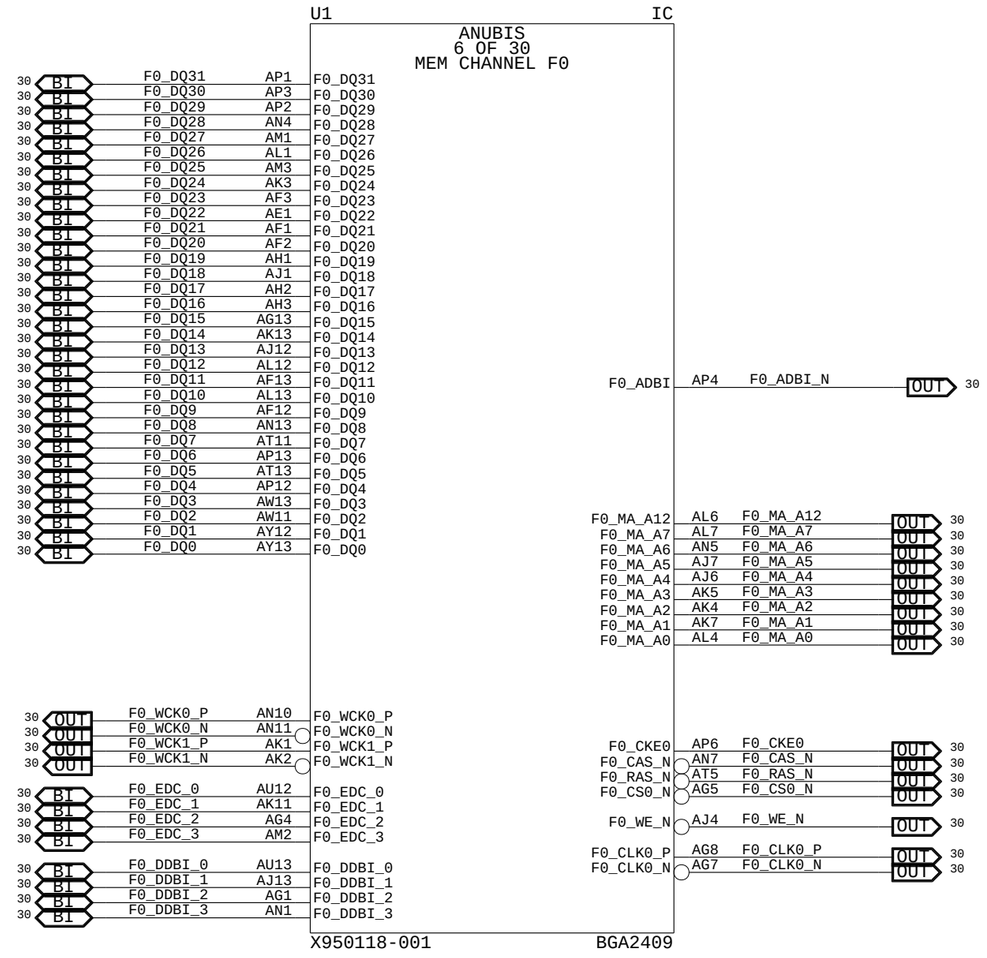




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	7/82	7/82	G-R	0.991

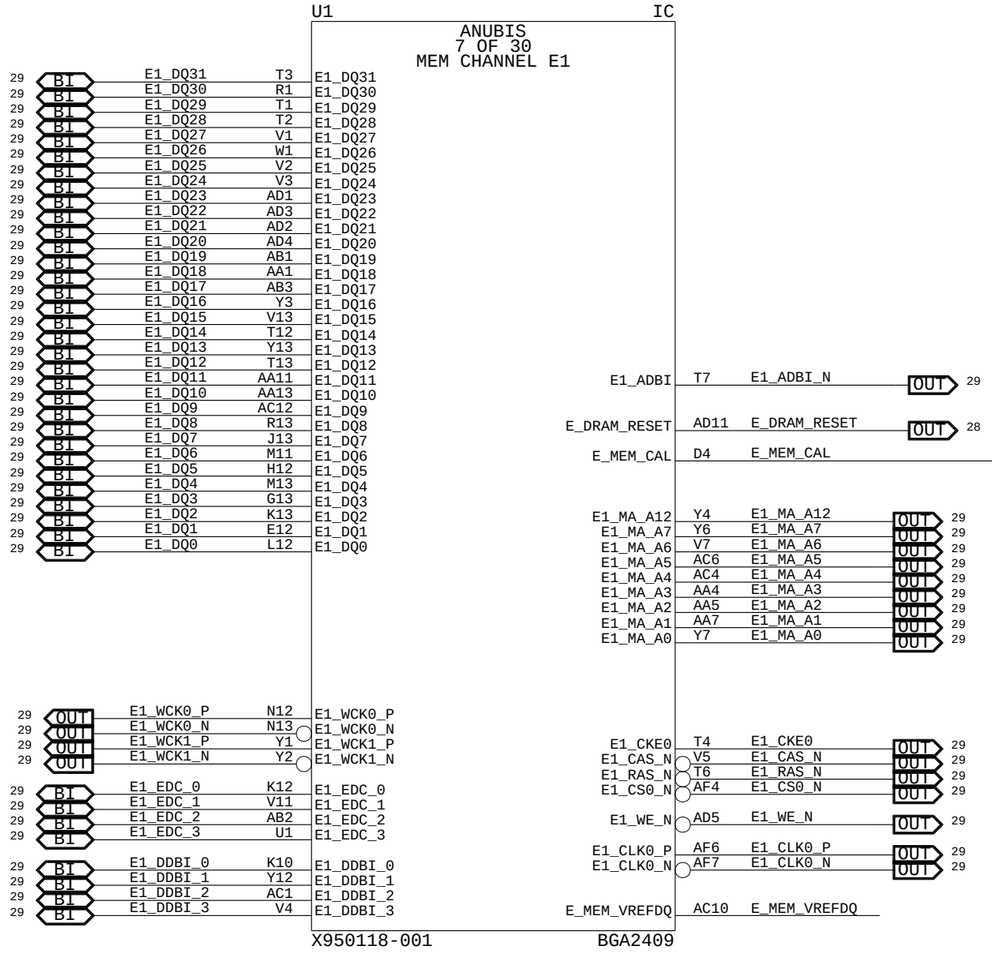
MEMORY: PARTITION F1/F0

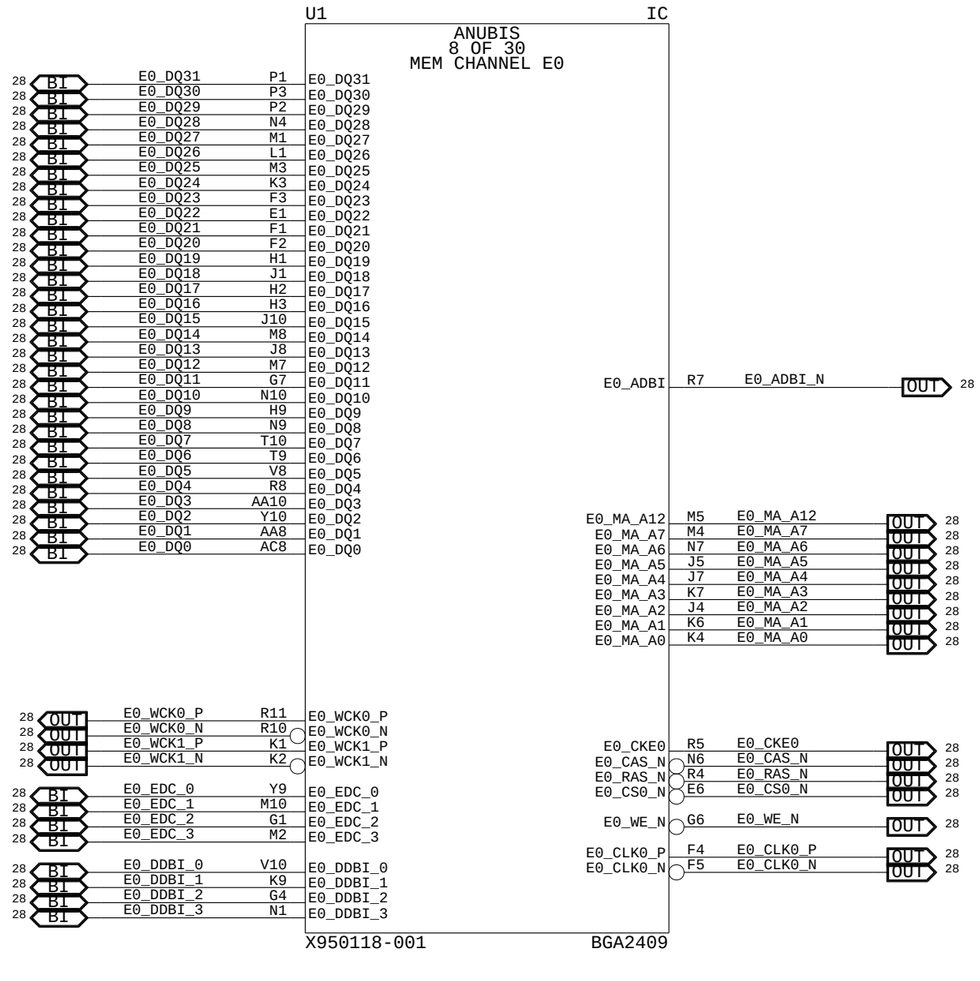




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	8/82	8/82	G-R	0.991

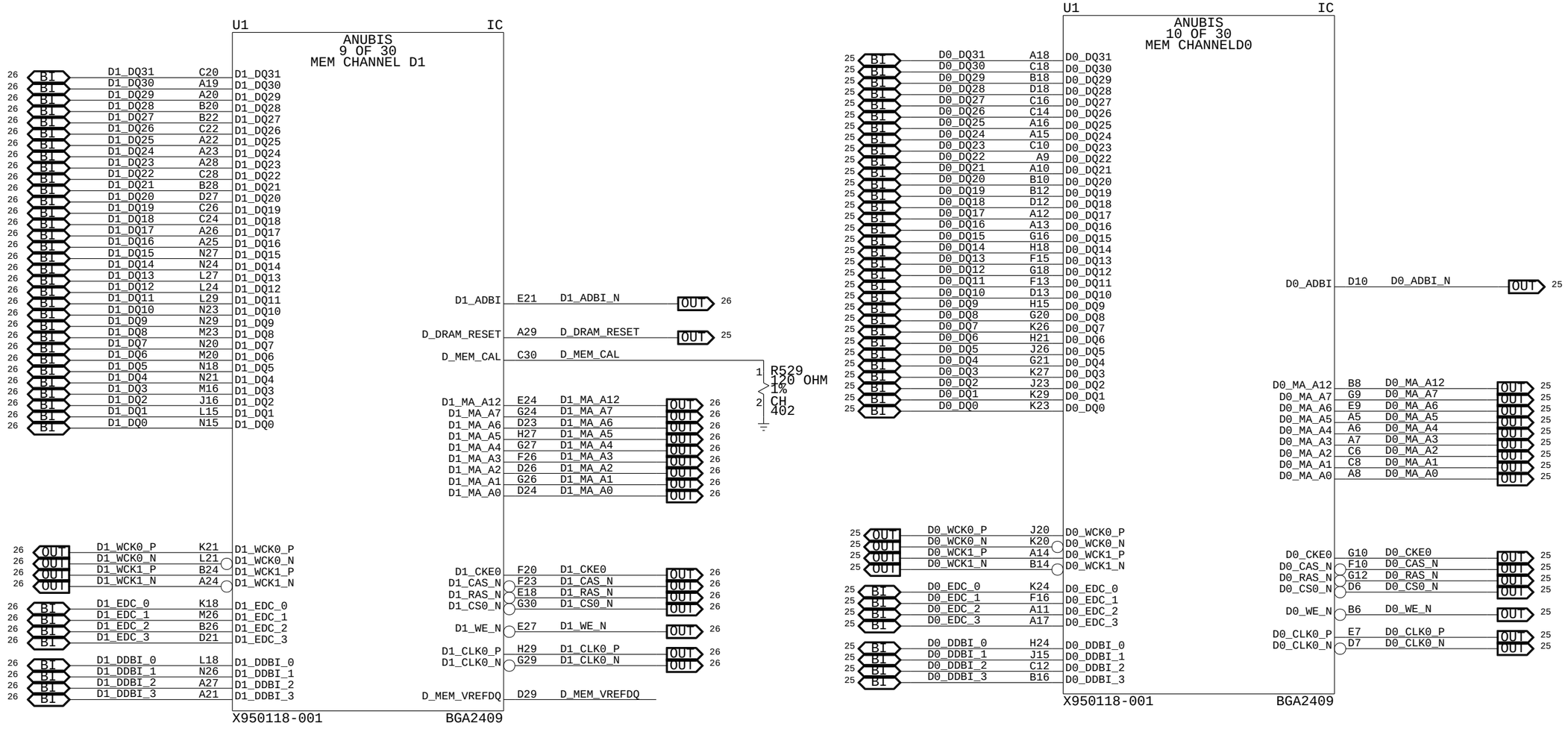
MEMORY: PARTITION E1/E0





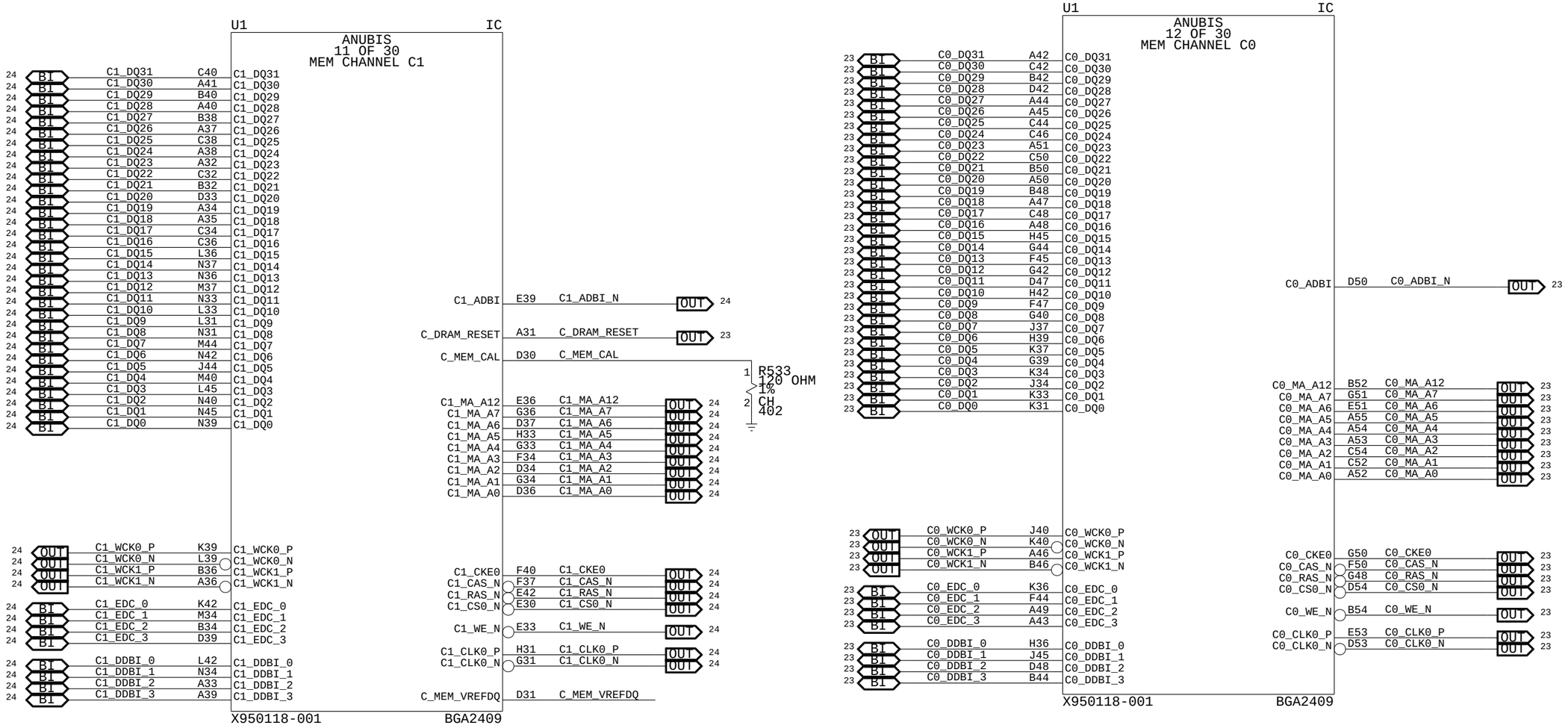
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	9/82	9/82	G-R	0.991

MEMORY: PARTITION D1/D0



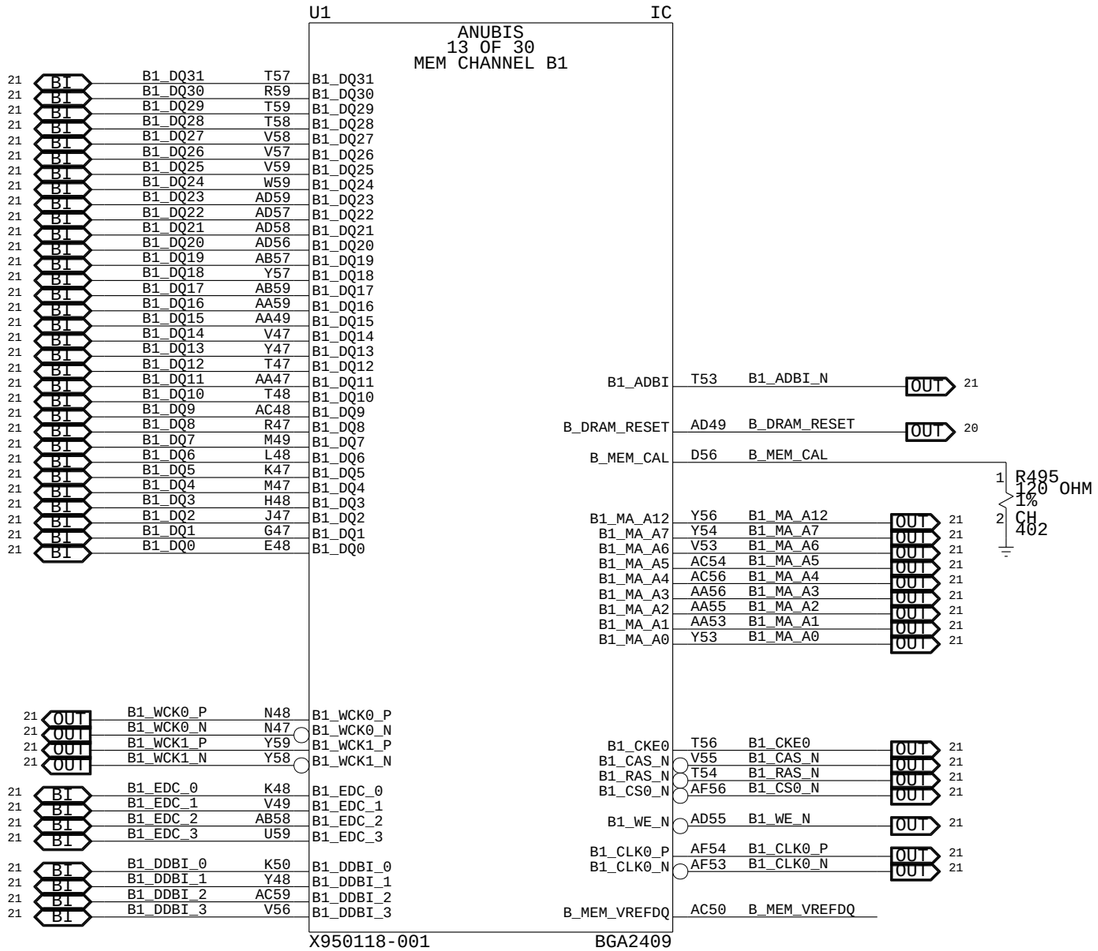
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	10/82	10/82	G-R	0.991

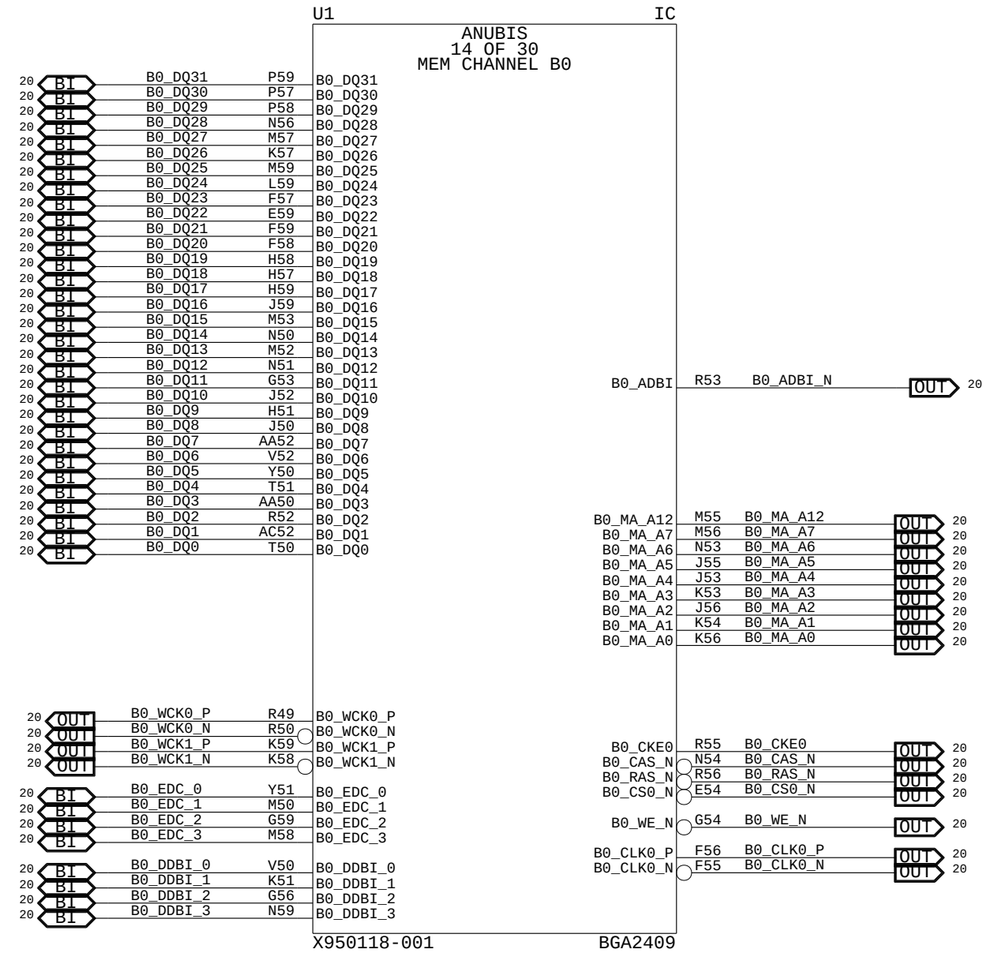
MEMORY: PARTITION C1/C0



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	11/82	11/82	G-R	0.991

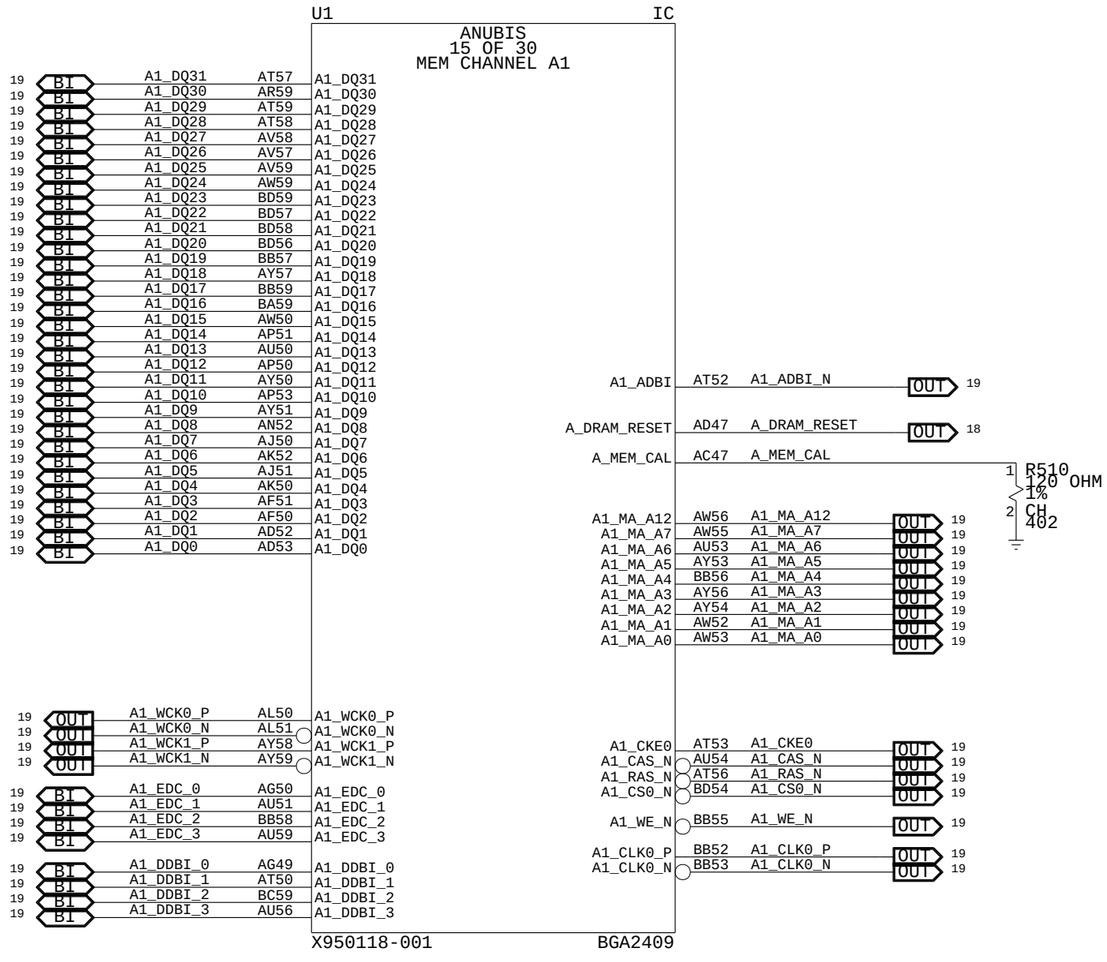
MEMORY: PARTITION B1/B0

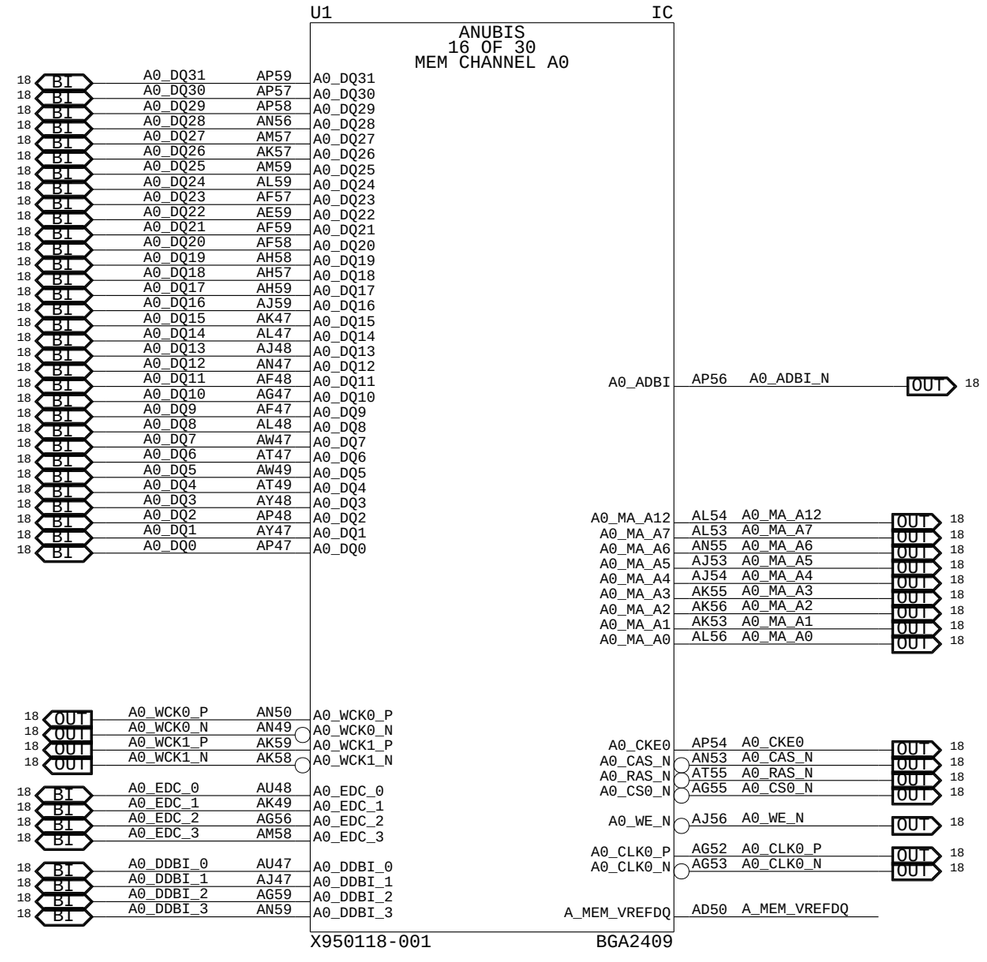




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	12/82	12/82	G-R	0.991

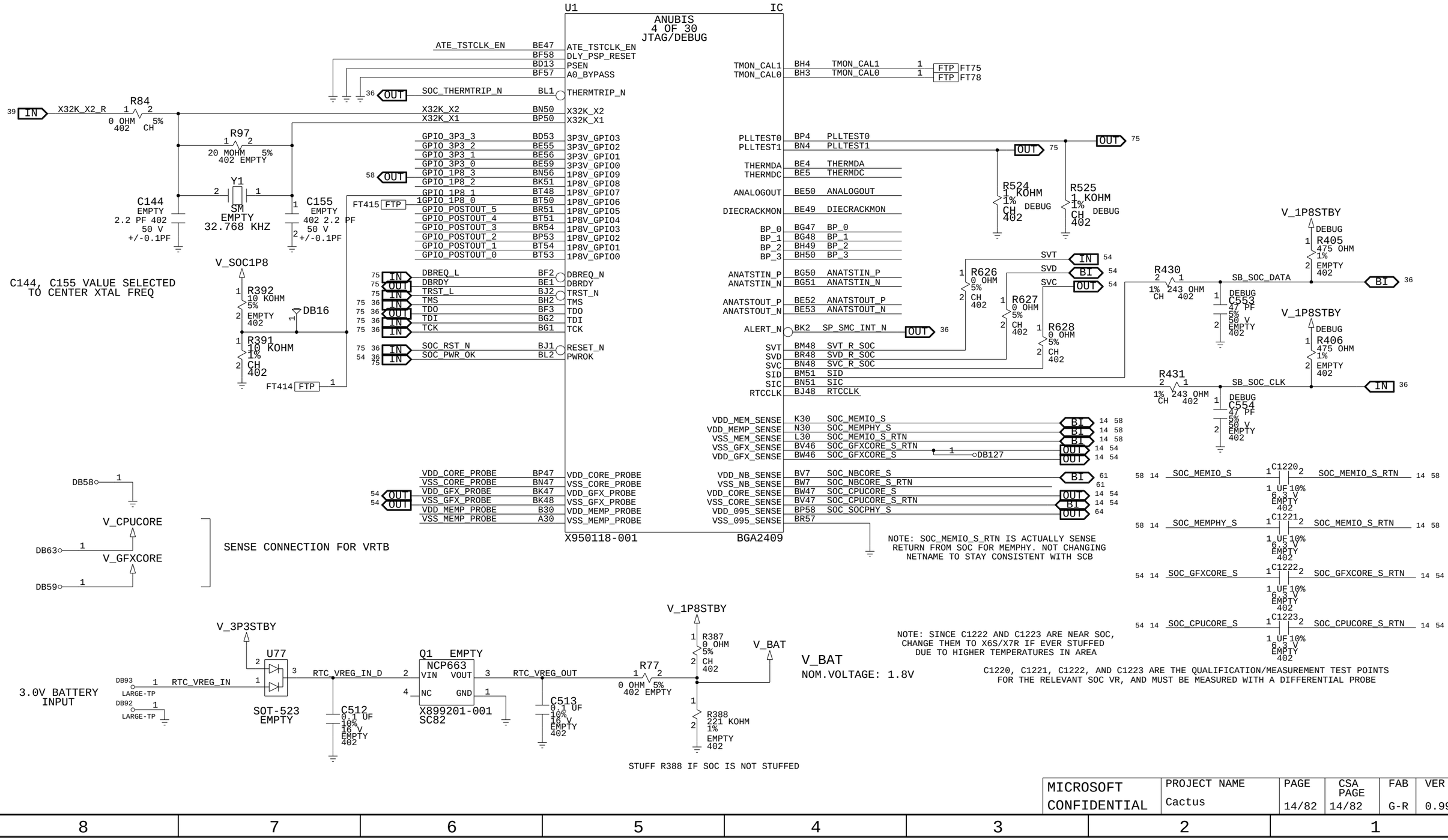
MEMORY: PARTITION A1/A0





MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	13/82	13/82	G-R	0.991

SOC:DEBUG,SB SIGNALS,V_BAT



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	14/82	14/82	G-R	0.991

SOC: DECOUPLING

V_GFXCORE

55 0805 22UF

C847 C771 C843 C735 C305
C772 C767 C692 C736 C279
C805 C804 C801 C846 C278
C693 C737 C845 C800 C277
C694 C802 C770 C768 C257
C293 C733 C803 C769 C690
C294 C734 C842 C844
C295 C280 C695 C691
C296 C281 C309 C732
C297 C264 C308 C262
C261 C254 C263
C260 C255 C253
C256 C307
C306

22 UF 20% 6.3 V X6S 805

V_GFXCORE

55 0805 22UF

C723 C703 C700 C722
C817 C727 C806 C697
C827 C834 C728 C698
C835 C701 C752 C838
C704 C758 C750 C837
C726 C751 C724 C808
C702 C836 C725 C782
C811 C749 C696
C780 C807
C699 C781

22 UF 20% 6.3 V X6S 805

2 0402 4.7UF

V_GFXCORE

C746 C747

4.7 UF 20% 6.3 V X6S 402

V_GFXCORE

57 0603 10UF

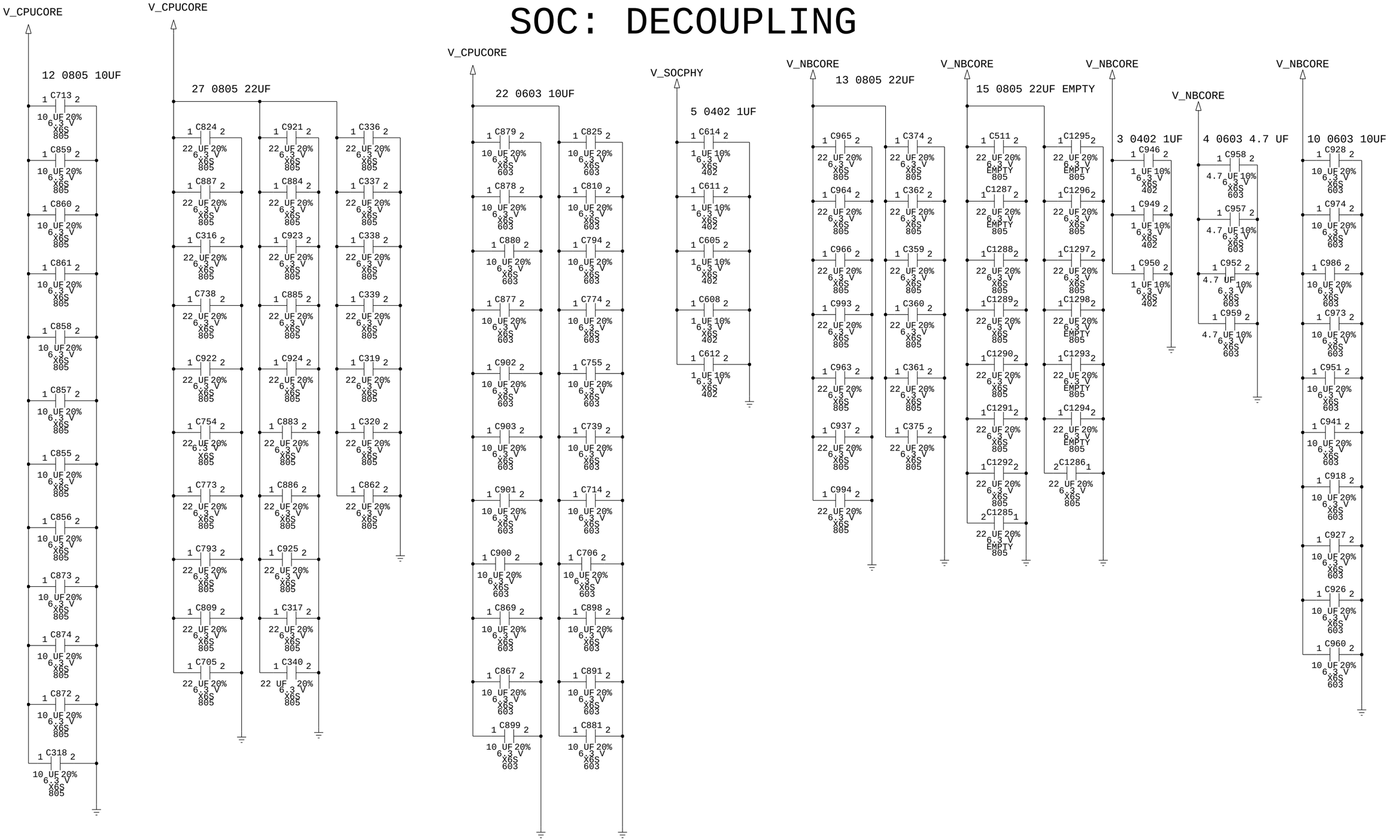
C742 C830 C687 C785
C761 C850 C718 C716
C789 C851 C744 C670
C678 C831 C763 C685
C684 C814 C791 C854
C712 C852 C815 C841
C730 C671 C719 C818
C741 C686 C688 C829
C759 C717 C745 C826
C766 C743 C764 C812
C784 C762 C792 C721
C798 C790 C816 C720
C832 C673 C833 C753
C813 C672 C853 C783
C828

10 UF 20% 6.3 V X6S 603

NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	15/82	15/82	G-R	0.991

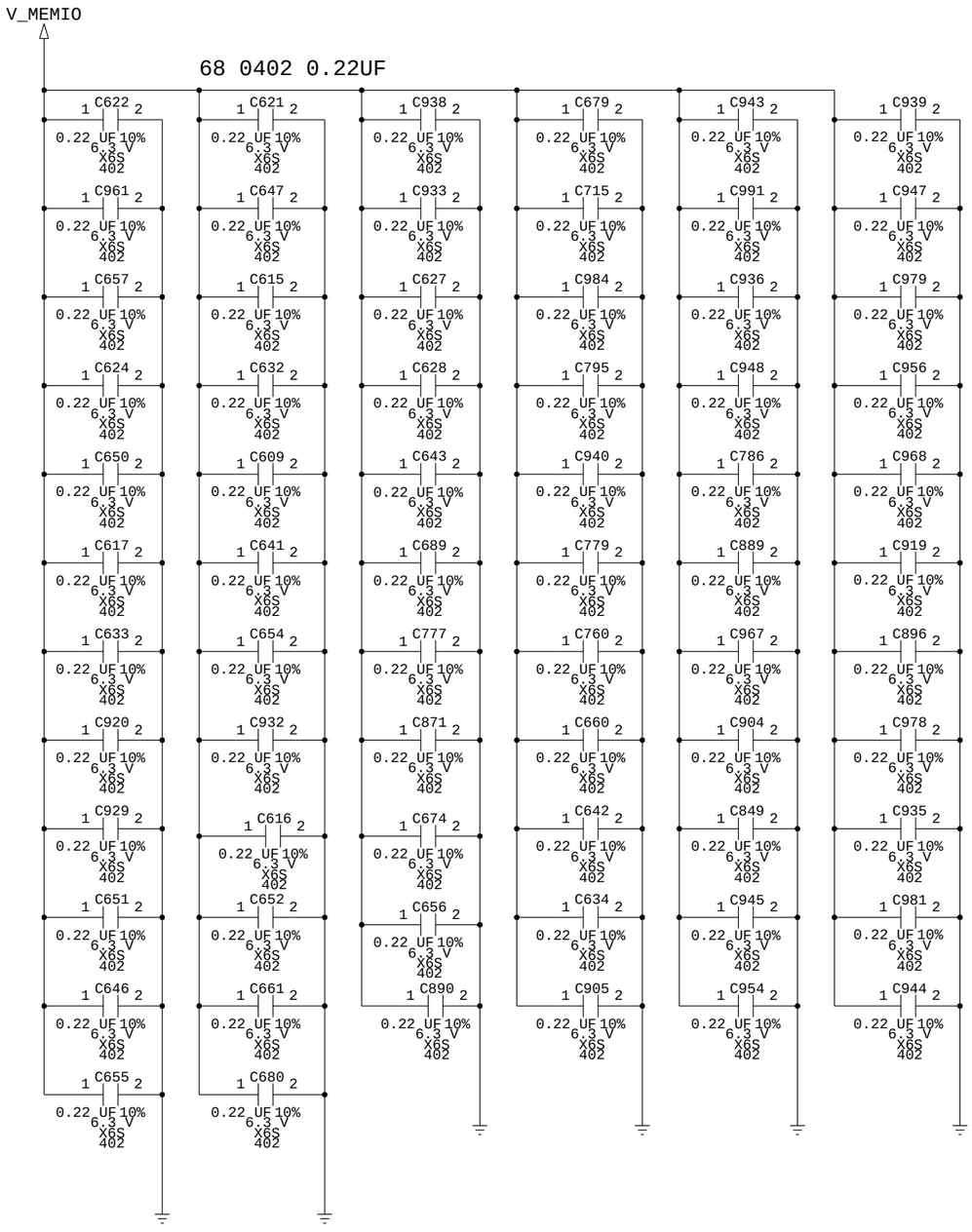
SOC: DECOUPLING

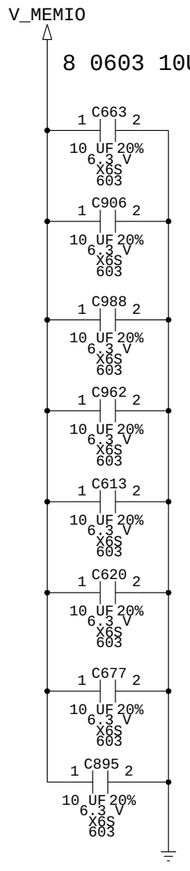


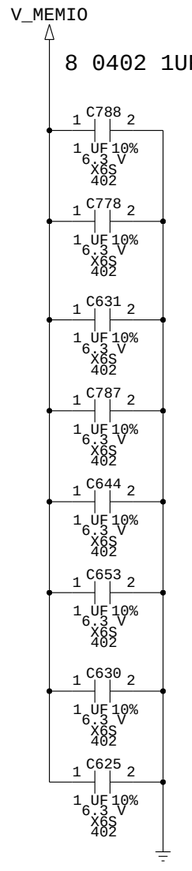
NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA

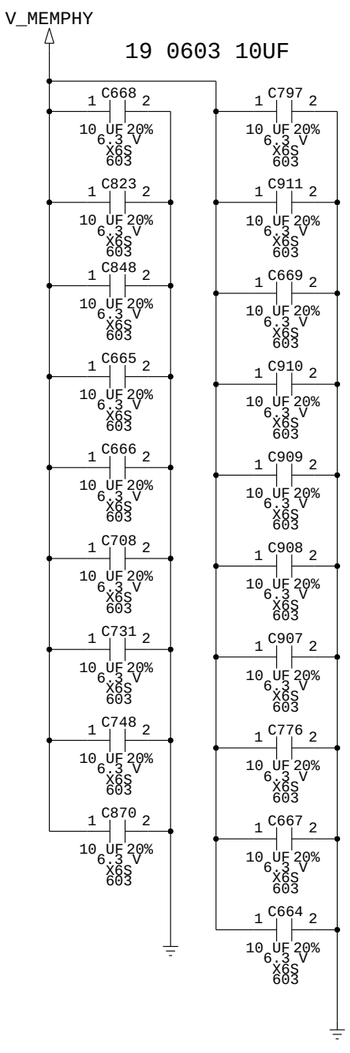
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	16/82	16/82	G-R	0.99

SOC: DECOUPLING





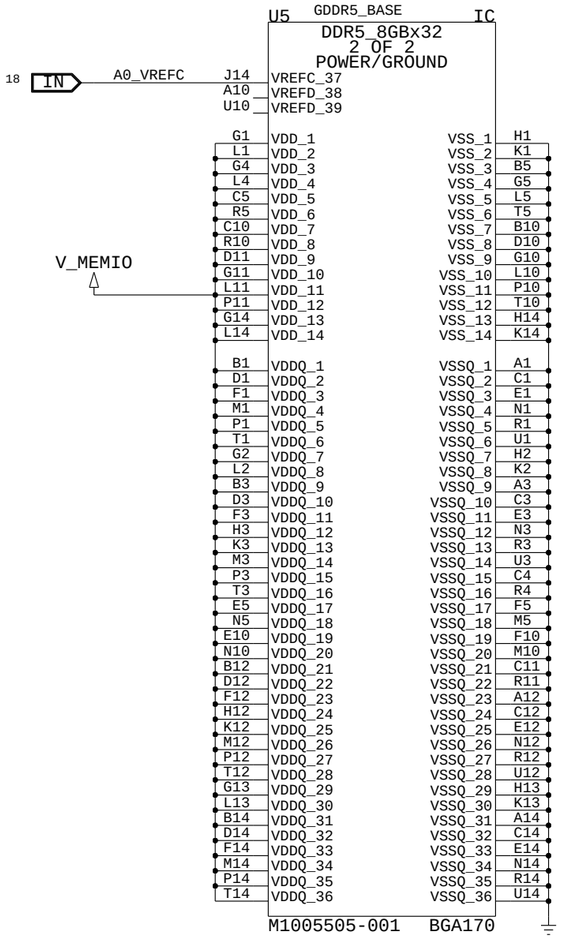


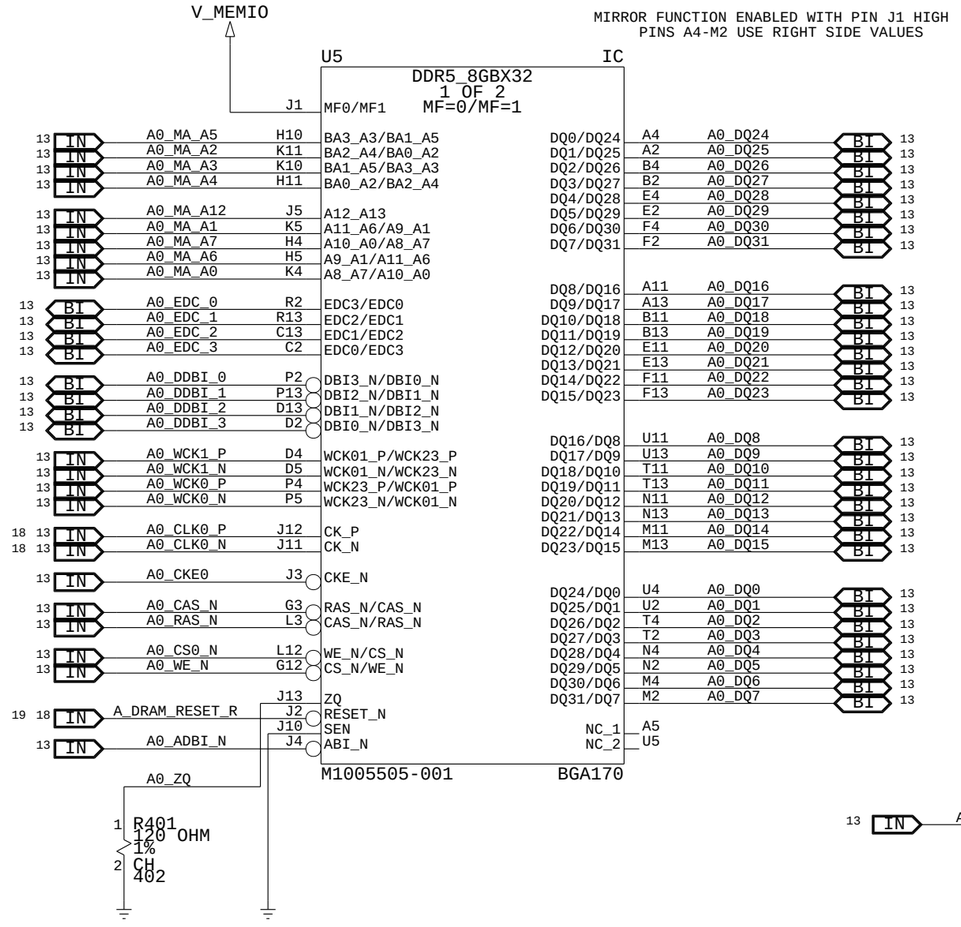


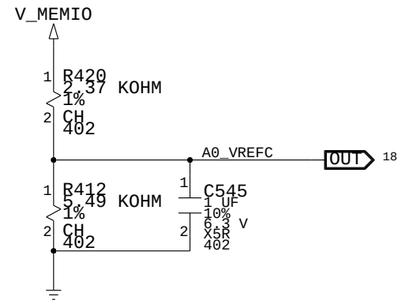
NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA

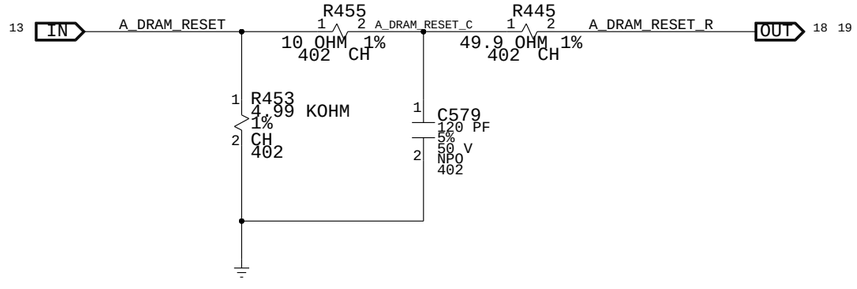
MICROSOFT CONFIDENTIAL	PROJECT NAME Cactus	PAGE 17/82	CSA PAGE 17/82	FAB G-R	VER 0.99

MEMORY: CHANNEL A0





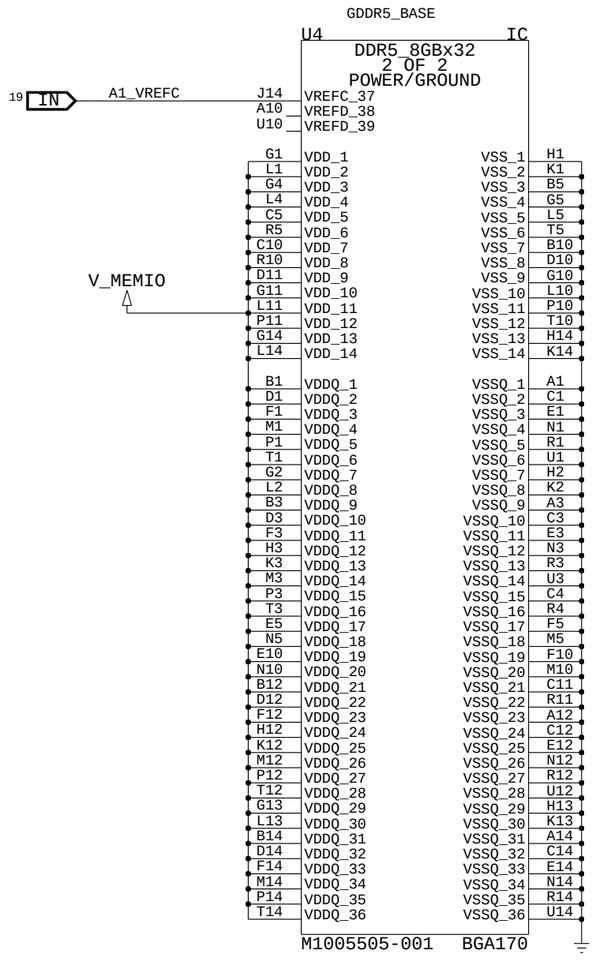


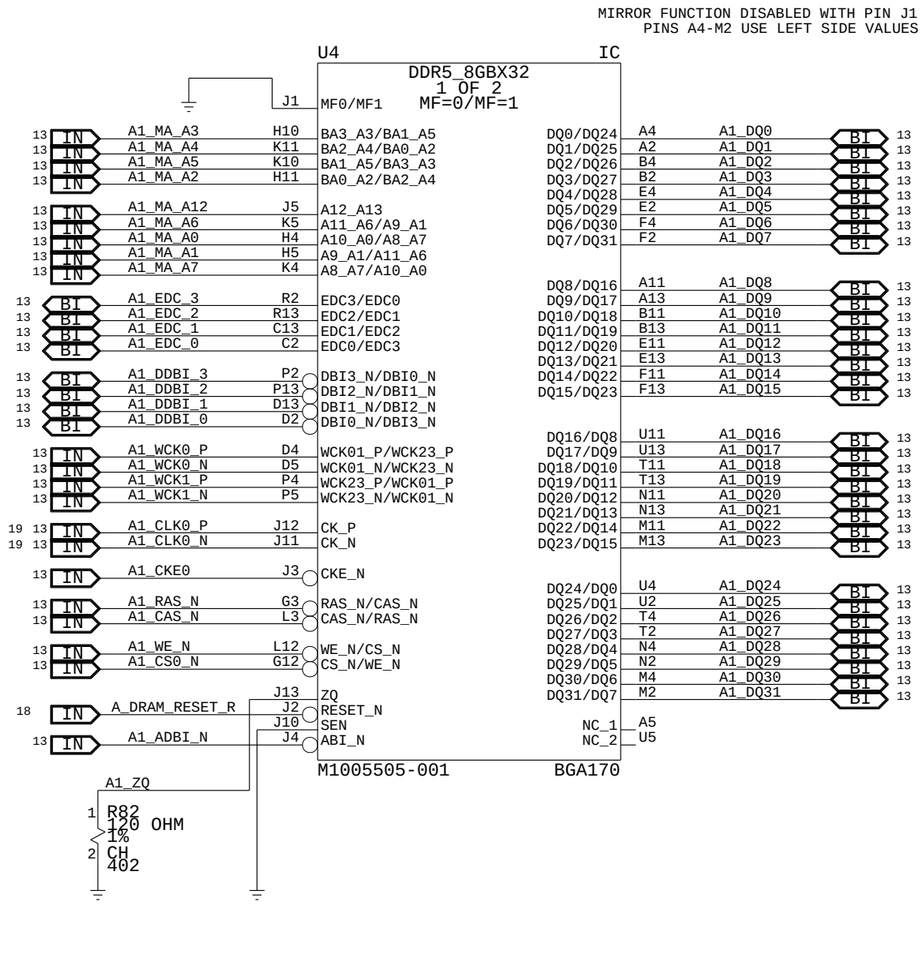


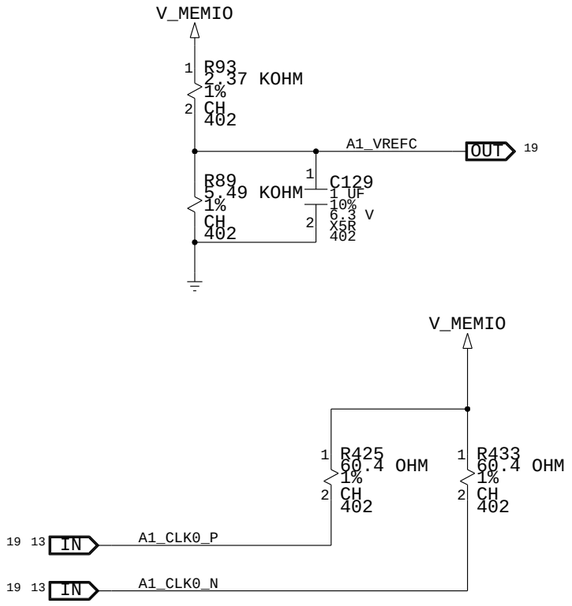
MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
M1005505-001	IC	U4,U5,U6,U7,U8,U9,U10,U11,U12,U13,U14,U15	MEM,SM,8GB,16MX32,GDDR5,170FBGA	GDDR5_SAMSUNG
M1005717-001	IC	U4,U5,U6,U7,U8,U9,U10,U11,U12,U13,U14,U15	MEM,SM,8GB,16MX32,GDDR5,170FBGA	GDDR5_HYNIX

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	18/82	18/82	G-R	0.991

MEMORY: CHANNEL A1

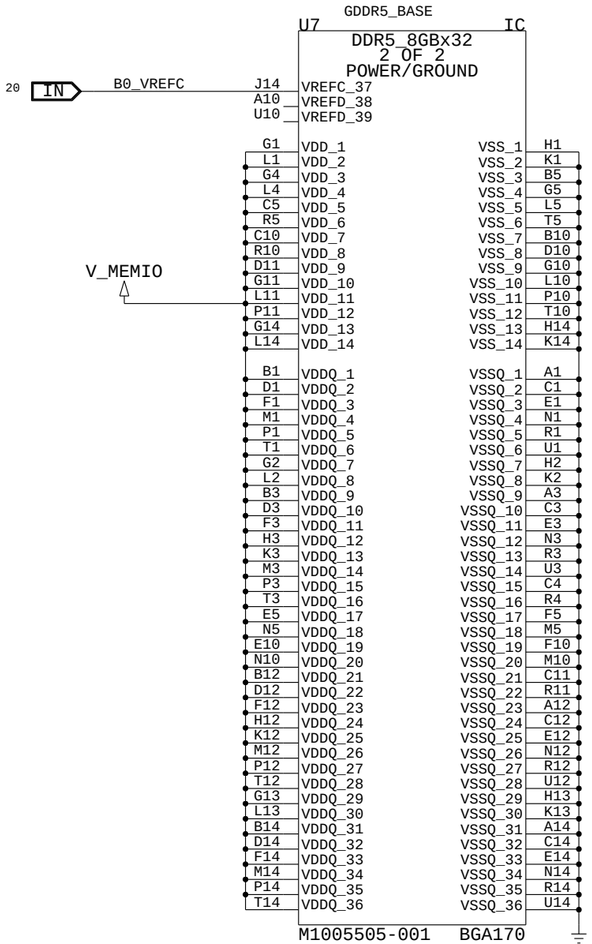


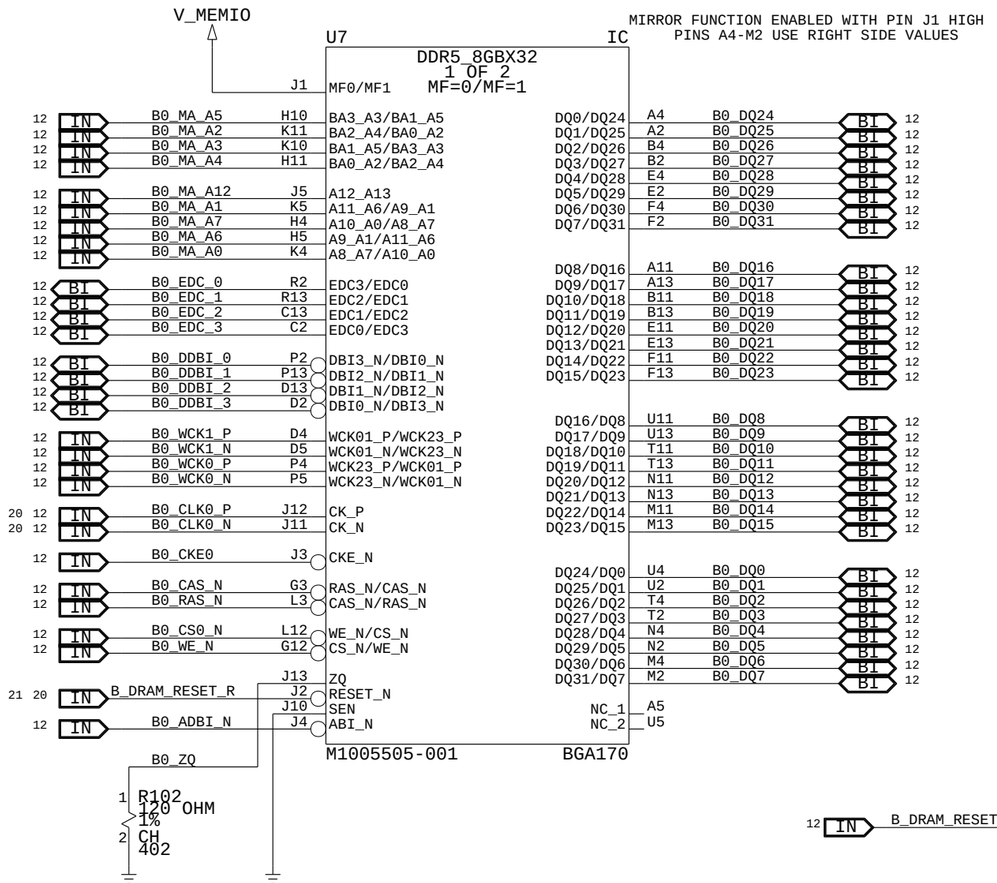


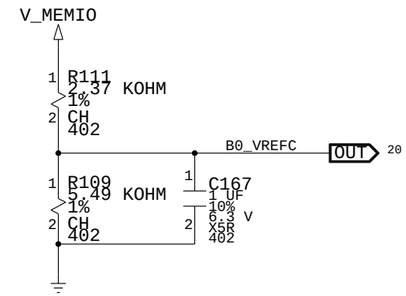


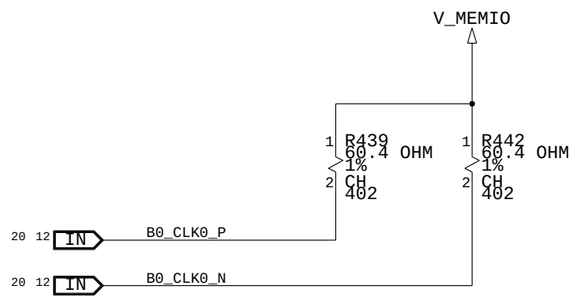
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	19/82	19/82	G-R	0.991

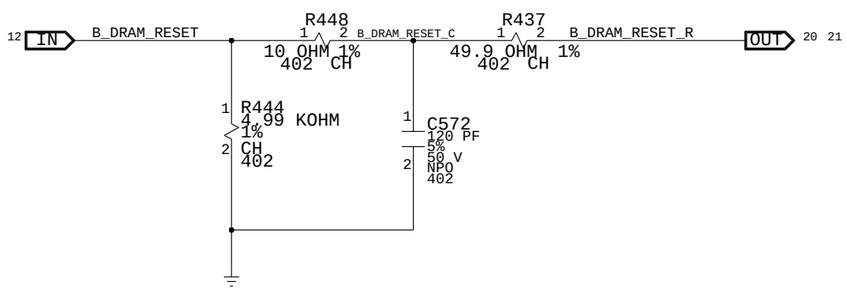
MEMORY: CHANNEL B0











MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	20/82	20/82	G-R	0.991

MEMORY: CHANNEL B1

GDDR5_BASE

U6 IC

DDR5_8GBx32
2 OF 2
POWER/GROUND

21 IN	B1_VREFC	J14	VREFC_37		
		A10	VREFD_38		
		U10	VREFD_39		
		G1	VDD_1	VSS_1	H1
		L1	VDD_2	VSS_2	K1
		G4	VDD_3	VSS_3	B5
		L4	VDD_4	VSS_4	G5
		C5	VDD_5	VSS_5	L5
		R5	VDD_6	VSS_6	T5
		C10	VDD_7	VSS_7	B10
		R10	VDD_8	VSS_8	D10
		D11	VDD_9	VSS_9	G10
		G11	VDD_10	VSS_10	L10
		L11	VDD_11	VSS_11	P10
		P11	VDD_12	VSS_12	T10
		G14	VDD_13	VSS_13	H14
		L14	VDD_14	VSS_14	K14
		B1	VDDQ_1	VSSQ_1	A1
		D1	VDDQ_2	VSSQ_2	C1
		F1	VDDQ_3	VSSQ_3	E1
		M1	VDDQ_4	VSSQ_4	N1
		P1	VDDQ_5	VSSQ_5	R1
		T1	VDDQ_6	VSSQ_6	U1
		G2	VDDQ_7	VSSQ_7	H2
		L2	VDDQ_8	VSSQ_8	K2
		B3	VDDQ_9	VSSQ_9	A3
		D3	VDDQ_10	VSSQ_10	C3
		F3	VDDQ_11	VSSQ_11	E3
		H3	VDDQ_12	VSSQ_12	N3
		K3	VDDQ_13	VSSQ_13	R3
		M3	VDDQ_14	VSSQ_14	U3
		P3	VDDQ_15	VSSQ_15	C4
		T3	VDDQ_16	VSSQ_16	R4
		E5	VDDQ_17	VSSQ_17	F5
		N5	VDDQ_18	VSSQ_18	M5
		E10	VDDQ_19	VSSQ_19	F10
		N10	VDDQ_20	VSSQ_20	M10
		B12	VDDQ_21	VSSQ_21	C11
		D12	VDDQ_22	VSSQ_22	R11
		F12	VDDQ_23	VSSQ_23	A12
		H12	VDDQ_24	VSSQ_24	C12
		K12	VDDQ_25	VSSQ_25	E12
		M12	VDDQ_26	VSSQ_26	N12
		P12	VDDQ_27	VSSQ_27	R12
		T12	VDDQ_28	VSSQ_28	U12
		G13	VDDQ_29	VSSQ_29	H13
		L13	VDDQ_30	VSSQ_30	K13
		B14	VDDQ_31	VSSQ_31	A14
		D14	VDDQ_32	VSSQ_32	C14
		F14	VDDQ_33	VSSQ_33	E14
		M14	VDDQ_34	VSSQ_34	N14
		P14	VDDQ_35	VSSQ_35	R14
		T14	VDDQ_36	VSSQ_36	U14

M1005505-001 BGA170

V_MEMIO

MIRROR FUNCTION DISABLED WITH PIN J1 LOW
PINS A4-M2 USE LEFT SIDE VALUES

U6 IC

DDR5_8GBX32
1 OF 2
MF=0/MF=1

		J1	MF0/MF1	MF=0/MF=1			
12 IN	B1_MA_A3	H10	BA3_A3/BA1_A5	DQ0/DQ24	A4	B1_DQ0	B1 12
12 IN	B1_MA_A4	K11	BA2_A4/BA0_A2	DQ1/DQ25	A2	B1_DQ1	B1 12
12 IN	B1_MA_A5	K10	BA1_A5/BA3_A3	DQ2/DQ26	B4	B1_DQ2	B1 12
12 IN	B1_MA_A2	H11	BA0_A2/BA2_A4	DQ3/DQ27	B2	B1_DQ3	B1 12
				DQ4/DQ28	E4	B1_DQ4	B1 12
12 IN	B1_MA_A12	J5	A12_A13	DQ5/DQ29	E2	B1_DQ5	B1 12
12 IN	B1_MA_A6	K5	A11_A6/A9_A1	DQ6/DQ30	F4	B1_DQ6	B1 12
12 IN	B1_MA_A0	H4	A10_A0/A8_A7	DQ7/DQ31	F2	B1_DQ7	B1 12
12 IN	B1_MA_A1	H5	A9_A1/A11_A6				
12 IN	B1_MA_A7	K4	A8_A7/A10_A0				
				DQ8/DQ16	A11	B1_DQ8	B1 12
12 B1	B1_EDC_3	R2	EDC3/EDC0	DQ9/DQ17	A13	B1_DQ9	B1 12
12 B1	B1_EDC_2	R13	EDC2/EDC1	DQ10/DQ18	B11	B1_DQ10	B1 12
12 B1	B1_EDC_1	C13	EDC1/EDC2	DQ11/DQ19	B13	B1_DQ11	B1 12
12 B1	B1_EDC_0	C2	EDC0/EDC3	DQ12/DQ20	E11	B1_DQ12	B1 12
				DQ13/DQ21	E13	B1_DQ13	B1 12
12 B1	B1_DDBI_3	P2	DBI3_N/DBI0_N	DQ14/DQ22	F11	B1_DQ14	B1 12
12 B1	B1_DDBI_2	P13	DBI2_N/DBI1_N	DQ15/DQ23	F13	B1_DQ15	B1 12
12 B1	B1_DDBI_1	D13	DBI1_N/DBI2_N				
12 B1	B1_DDBI_0	D2	DBI0_N/DBI3_N				
				DQ16/DQ8	U11	B1_DQ16	B1 12
12 IN	B1_WCK0_P	D4	WCK01_P/WCK23_P	DQ17/DQ9	U13	B1_DQ17	B1 12
12 IN	B1_WCK0_N	D5	WCK01_N/WCK23_N	DQ18/DQ10	T11	B1_DQ18	B1 12
12 IN	B1_WCK1_P	P4	WCK23_P/WCK01_P	DQ19/DQ11	T13	B1_DQ19	B1 12
12 IN	B1_WCK1_N	P5	WCK23_N/WCK01_N	DQ20/DQ12	N11	B1_DQ20	B1 12
				DQ21/DQ13	N13	B1_DQ21	B1 12
21 12 IN	B1_CLK0_P	J12	CK_P	DQ22/DQ14	M11	B1_DQ22	B1 12
21 12 IN	B1_CLK0_N	J11	CK_N	DQ23/DQ15	M13	B1_DQ23	B1 12
12 IN	B1_CKE0	J3	CKE_N				
				DQ24/DQ0	U4	B1_DQ24	B1 12
12 IN	B1_RAS_N	G3	RAS_N/CAS_N	DQ25/DQ1	U2	B1_DQ25	B1 12
12 IN	B1_CAS_N	L3	CAS_N/RAS_N	DQ26/DQ2	T4	B1_DQ26	B1 12
				DQ27/DQ3	T2	B1_DQ27	B1 12
12 IN	B1_WE_N	L12	WE_N/CS_N	DQ28/DQ4	N4	B1_DQ28	B1 12
12 IN	B1_CS0_N	G12	CS_N/WE_N	DQ29/DQ5	N2	B1_DQ29	B1 12
		J13	ZQ	DQ30/DQ6	M4	B1_DQ30	B1 12
20 IN	B_DRAM_RESET_R	J2	RESET_N	DQ31/DQ7	M2	B1_DQ31	B1 12
		J10	SEN				
12 IN	B1_ADBI_N	J4	ABI_N	NC_1	A5		
				NC_2	U5		

M1005505-001 BGA170

B1_ZQ

R399
120 OHM
1%
CH
402

V_MEMIO

1 R409
2.37 KOHM
1%
2 CH
402

B1_VREFC OUT 21

1 R402
5.49 KOHM
1%
2 CH
402

1 C537
1 UF
10%
6.3 V
2 X5R
402

V_MEMIO

1 R414
60.4 OHM
1%
2 CH
402

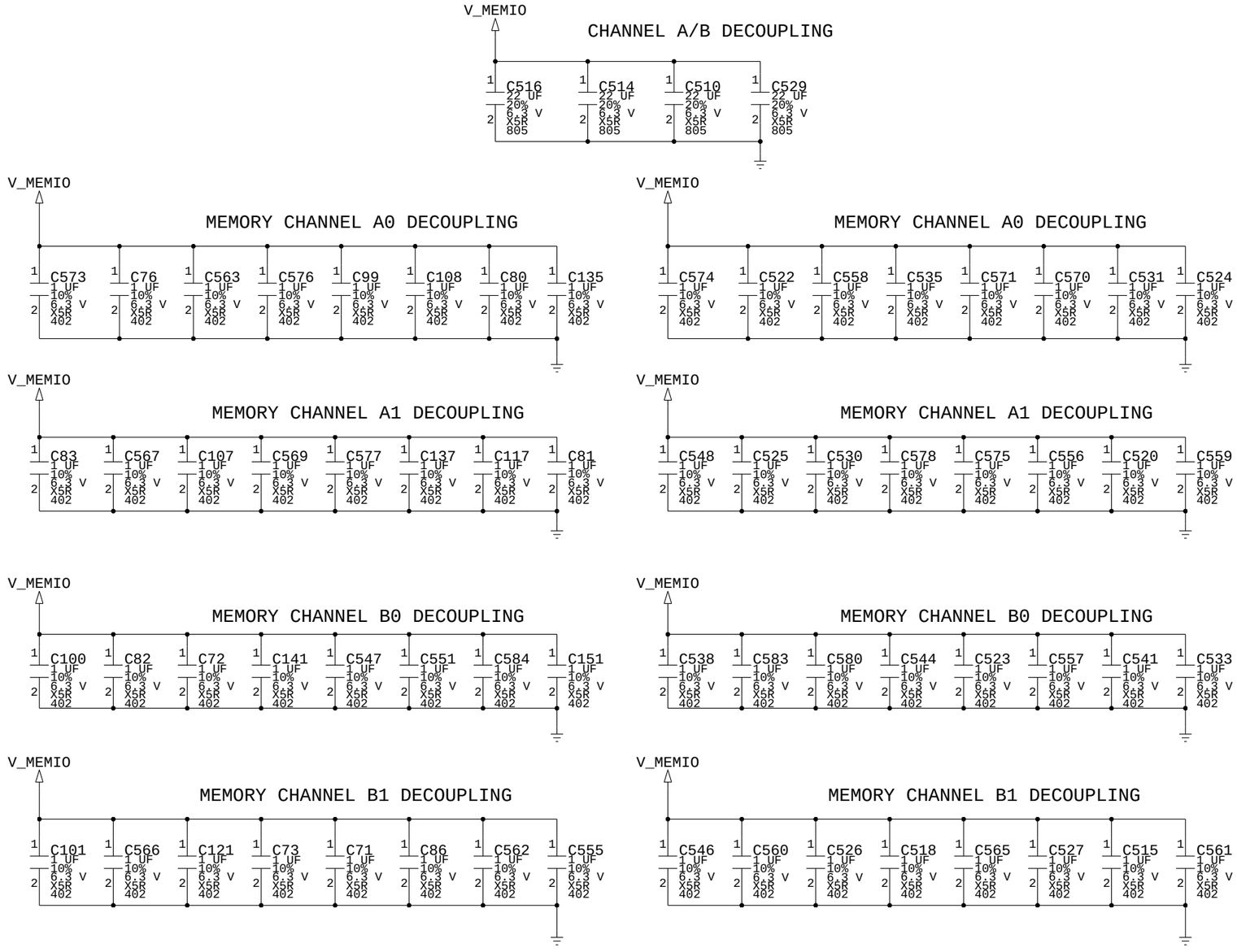
1 R415
60.4 OHM
1%
2 CH
402

21 12 IN B1_CLK0_P

21 12 IN B1_CLK0_N

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	21/82	21/82	G-R	0.991

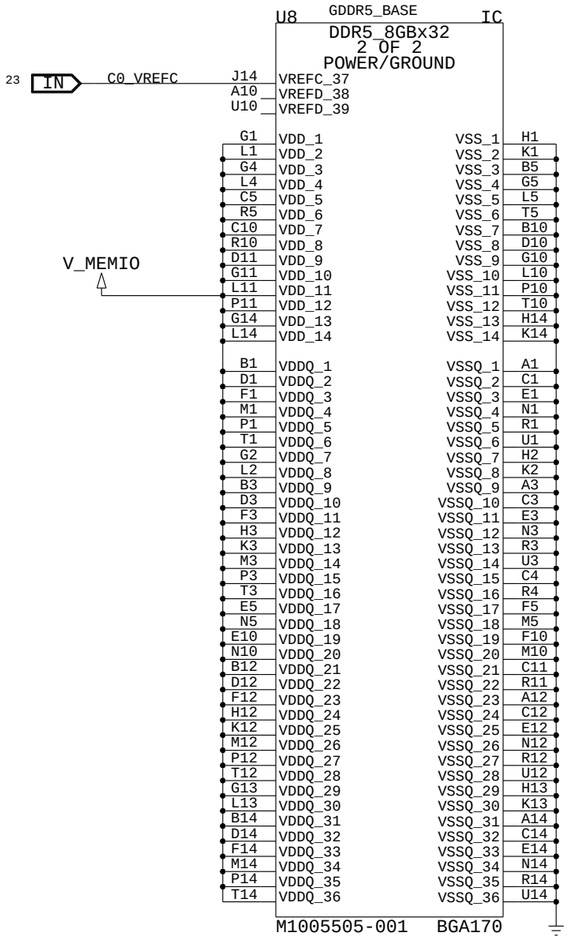
MEMORY: CHANNEL A/B DECOUPLING



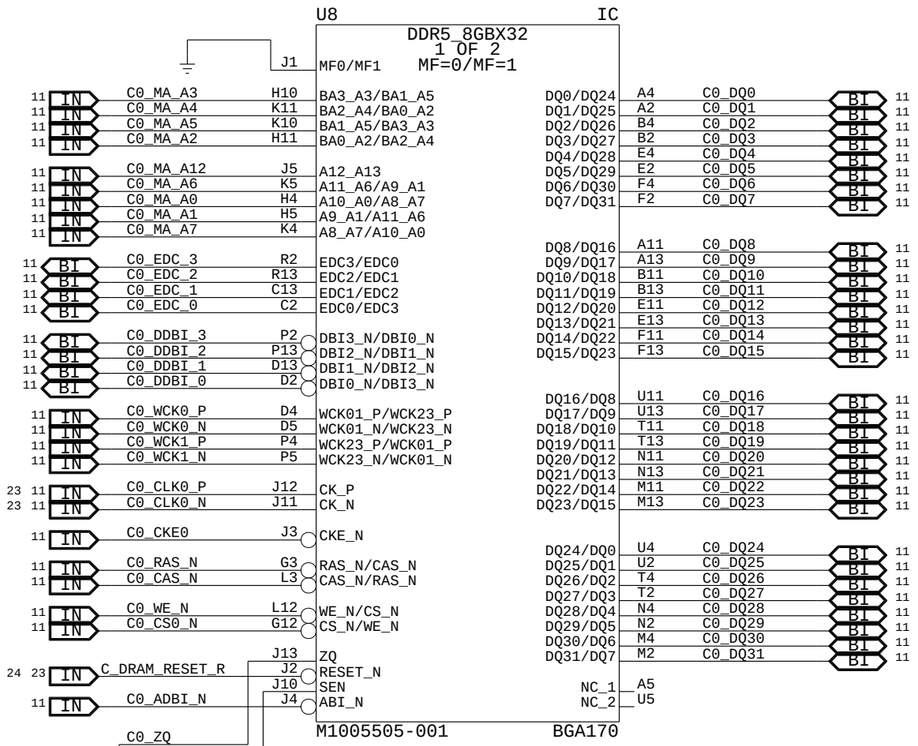
NOTE: ADDITIONAL MEMORY DECOUPLING ON PAGE 33

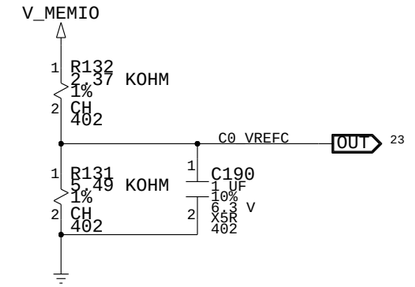
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	22/82	22/82	G-R	0.991

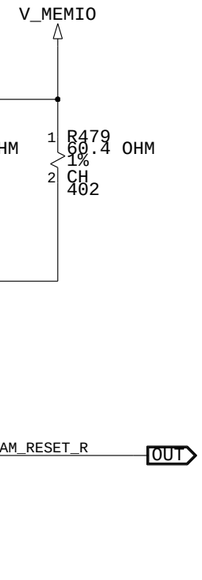
MEMORY: CHANNEL C0

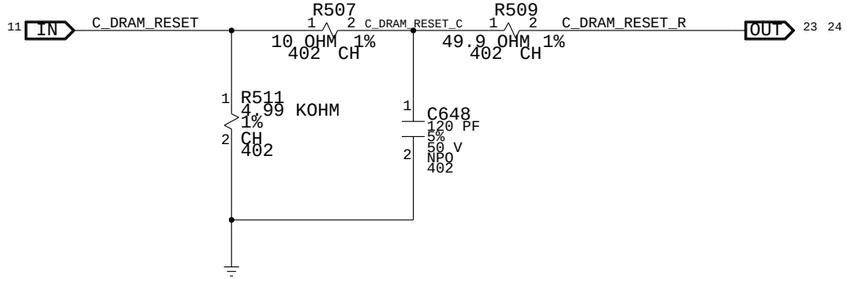


MIRROR FUNCTION DISABLED WITH PIN J1 LOW
PINS A4-M2 USE LEFT SIDE VALUES



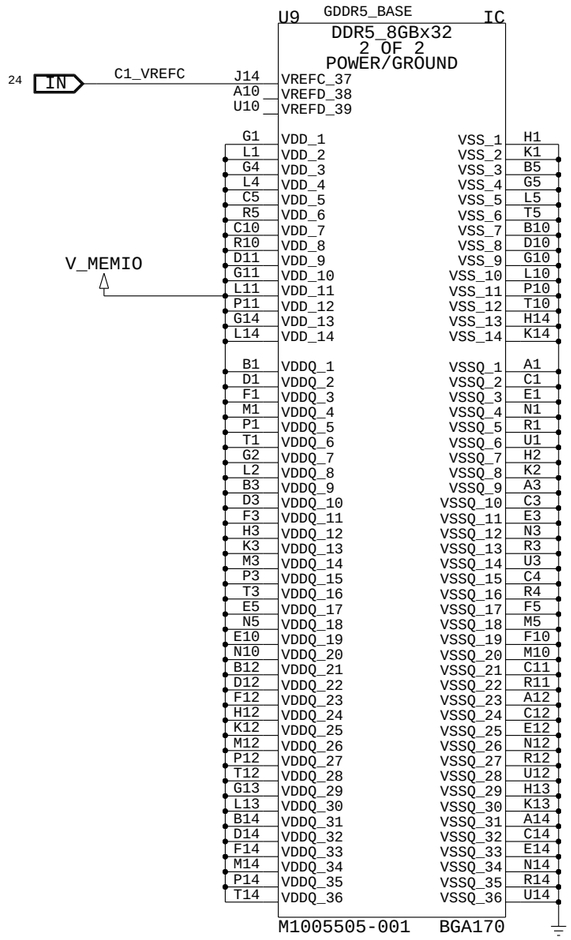


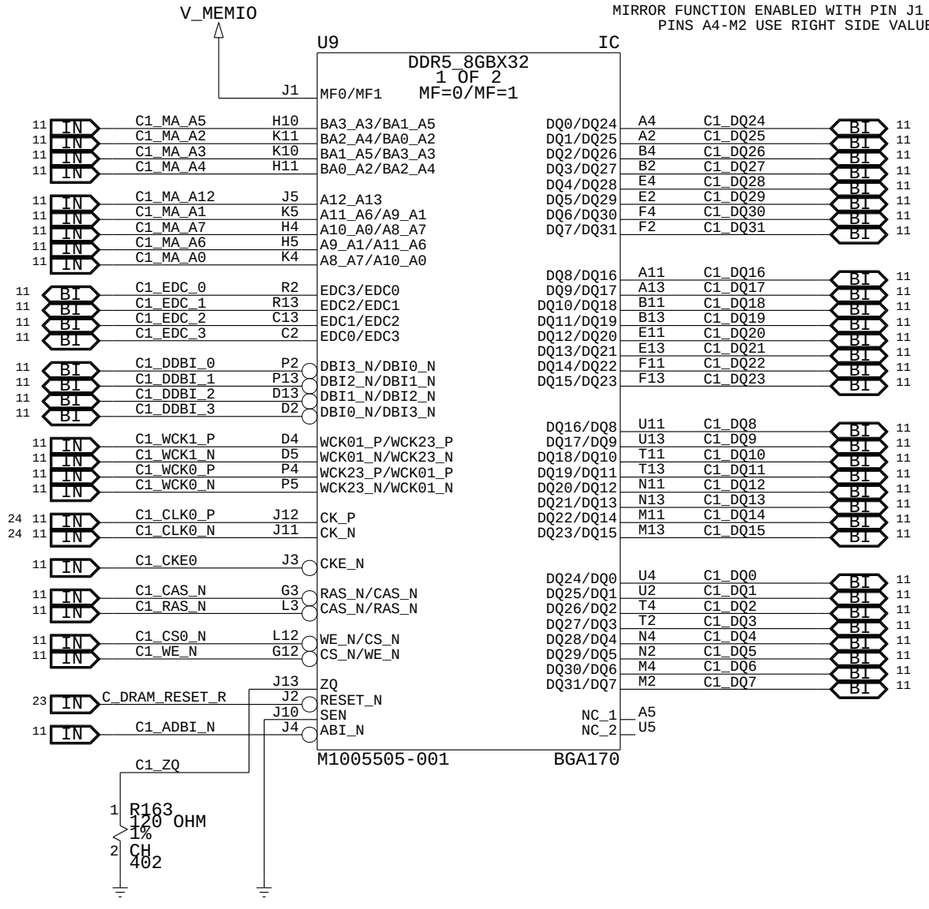


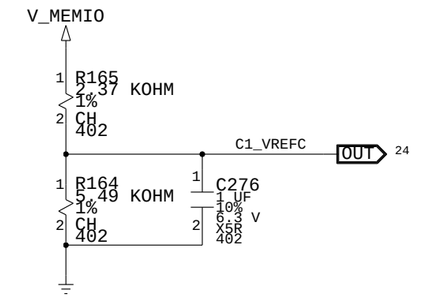


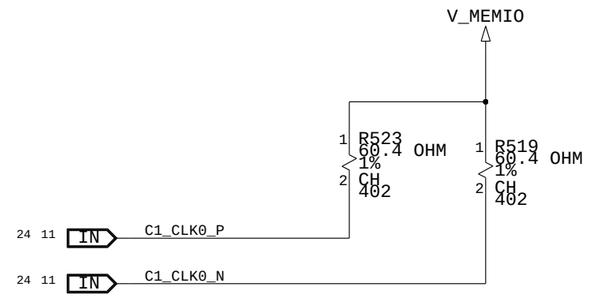
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	23/82	23/82	G-R	0.991

MEMORY: CHANNEL C1



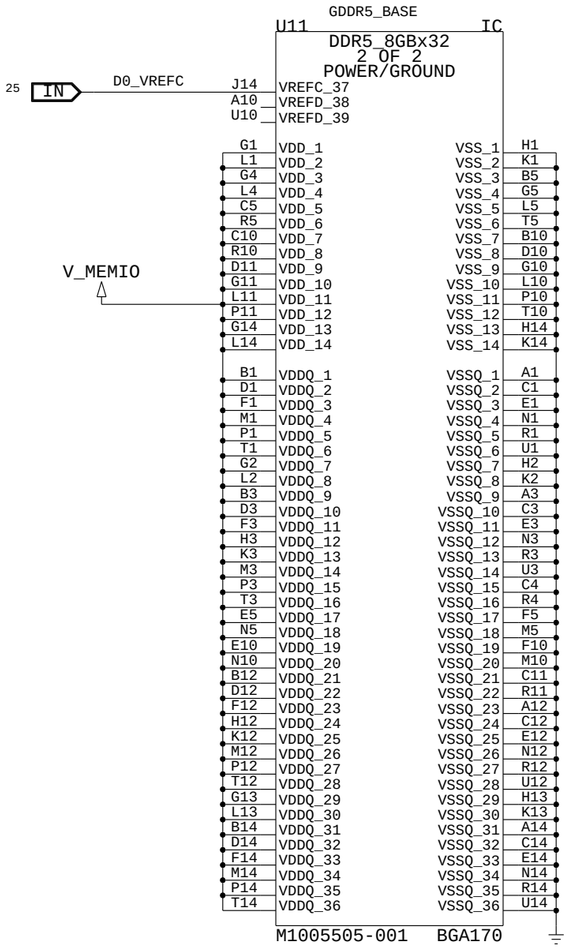


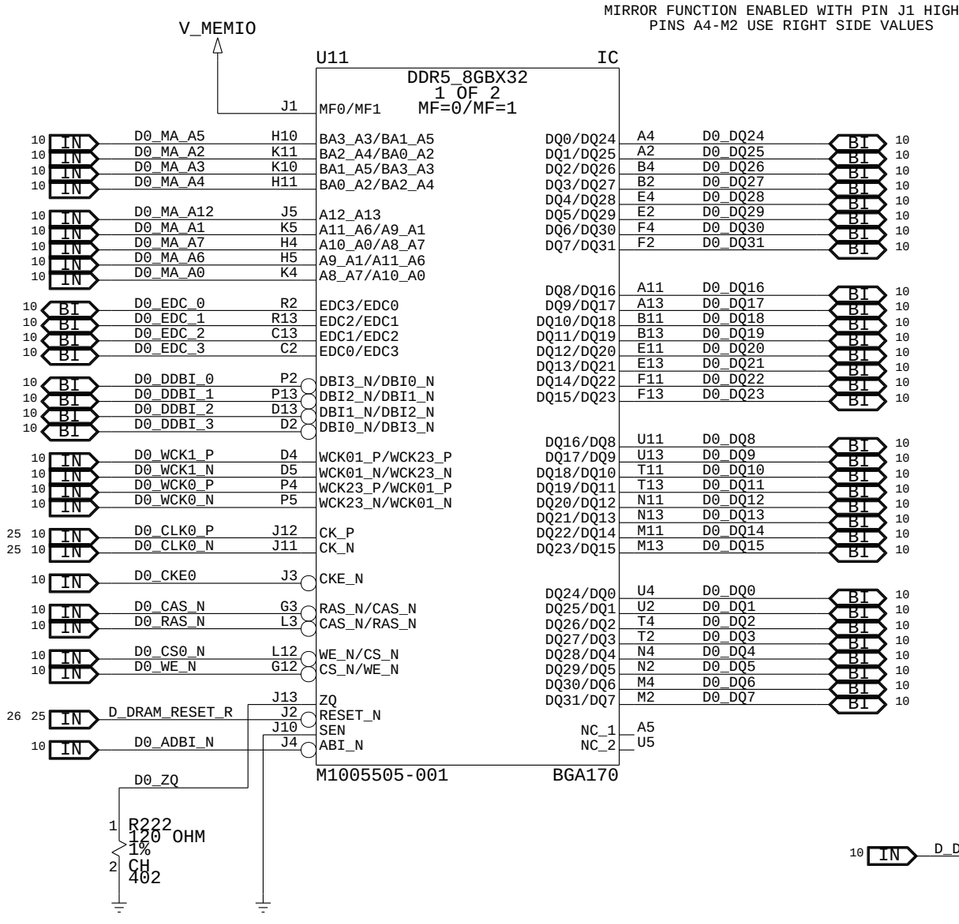




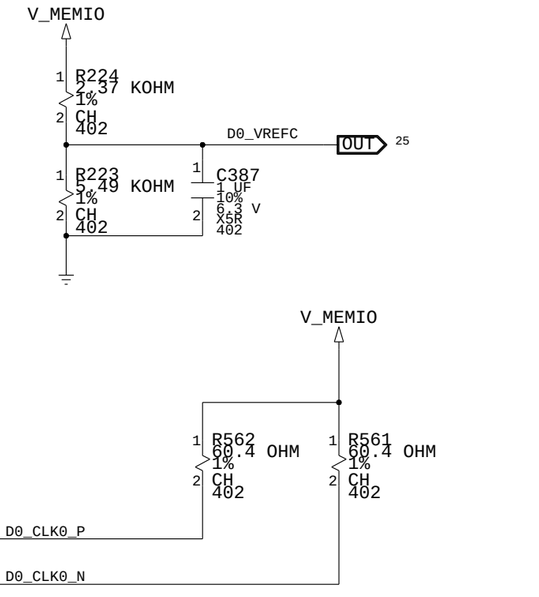
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	24/82	24/82	G-R	0.991

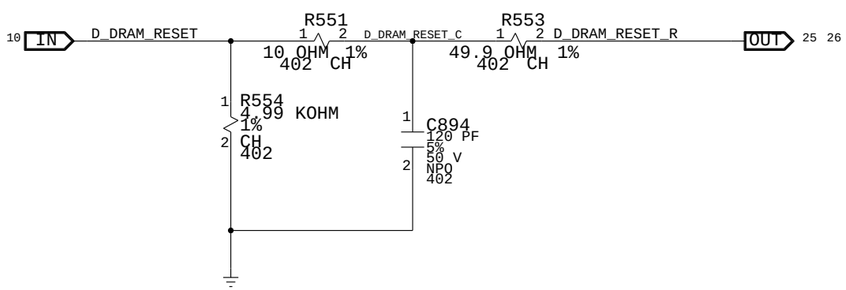
MEMORY: CHANNEL D0





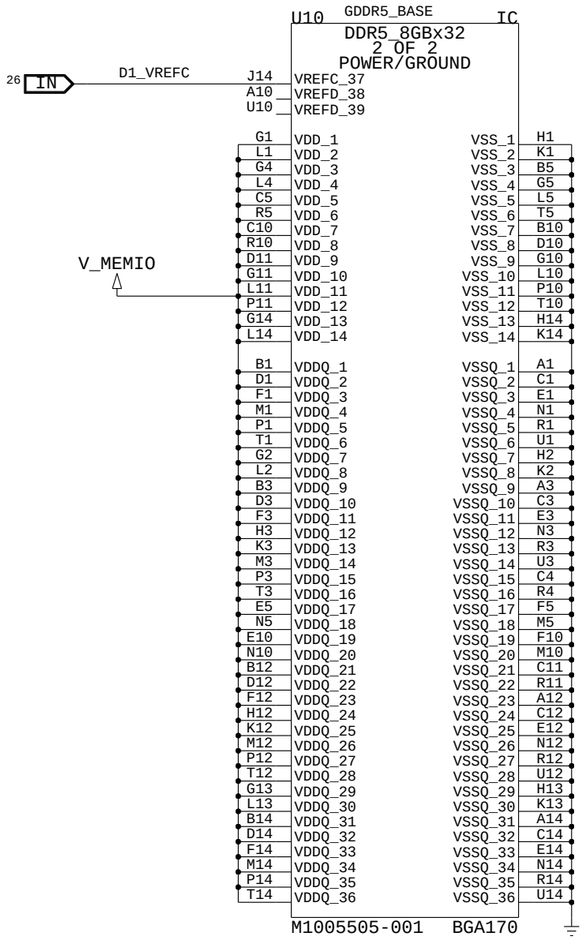
MIRROR FUNCTION ENABLED WITH PIN J1 HIGH
PINS A4-M2 USE RIGHT SIDE VALUES

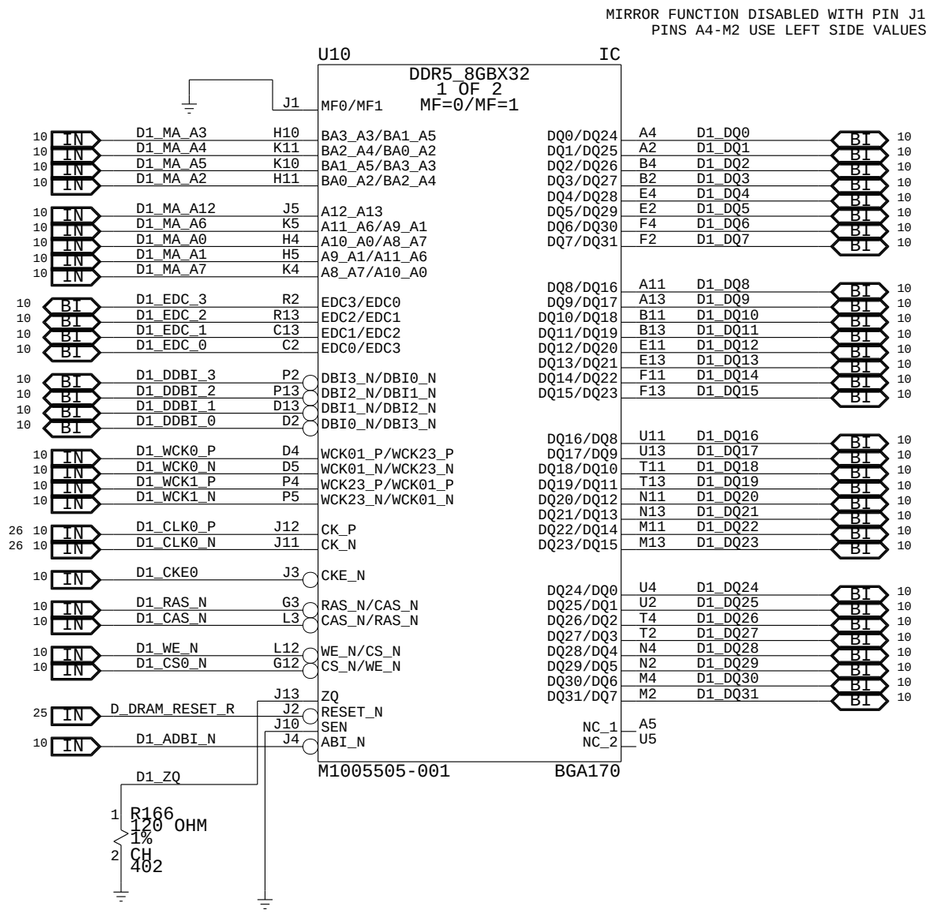


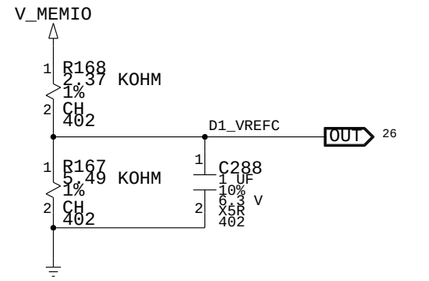


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	25/82	25/82	G-R	0.991

MEMORY: CHANNEL D1



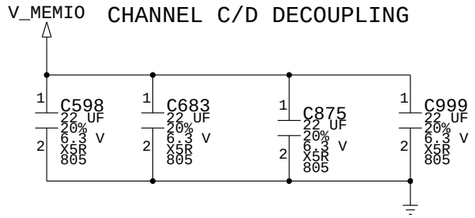




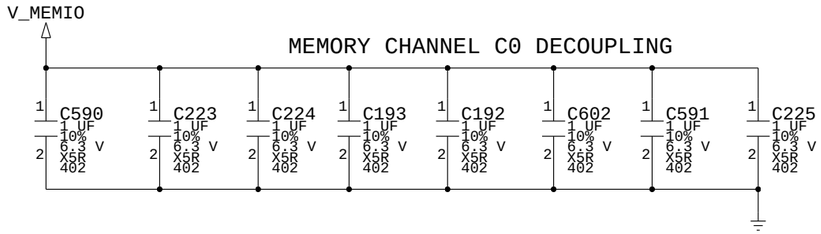
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	26/82	26/82	G-R	0.991

MEMORY: CHANNEL C/D DECOUPLING

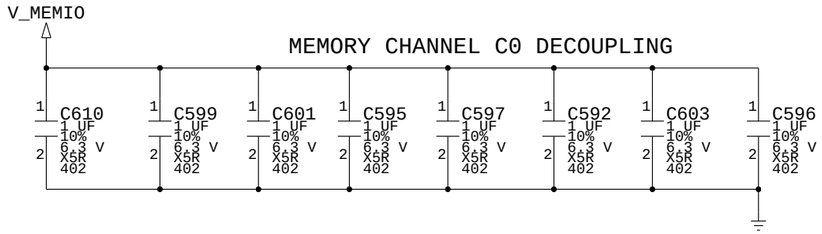
CHANNEL C/D DECOUPLING



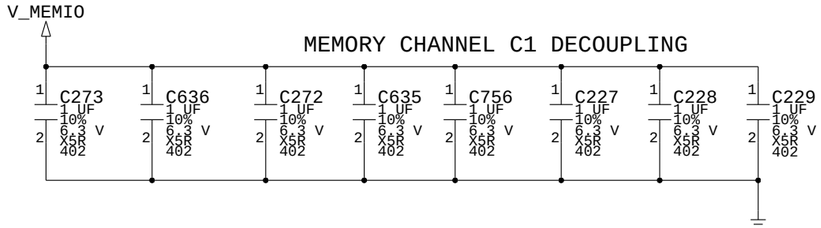
MEMORY CHANNEL C0 DECOUPLING



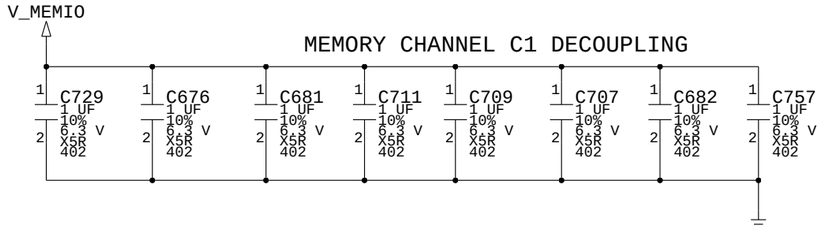
MEMORY CHANNEL C0 DECOUPLING



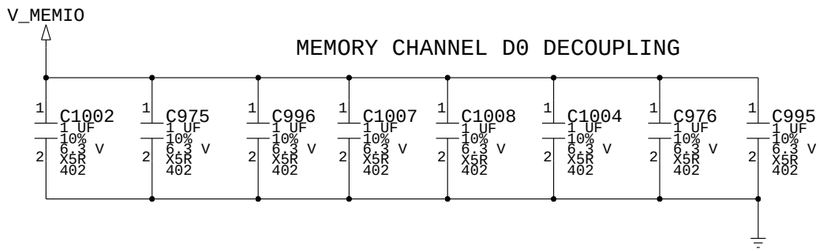
MEMORY CHANNEL C1 DECOUPLING



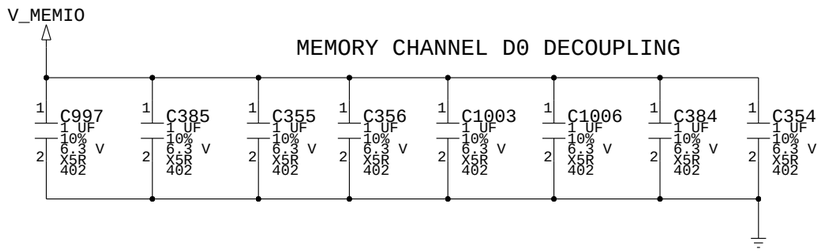
MEMORY CHANNEL C1 DECOUPLING



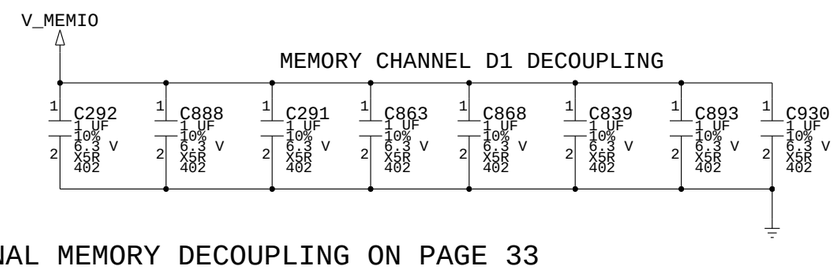
MEMORY CHANNEL D0 DECOUPLING



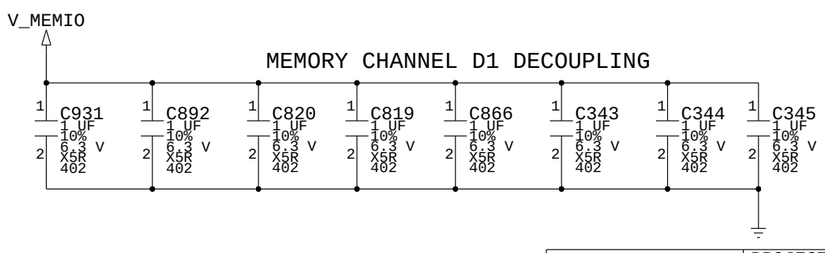
MEMORY CHANNEL D0 DECOUPLING



MEMORY CHANNEL D1 DECOUPLING

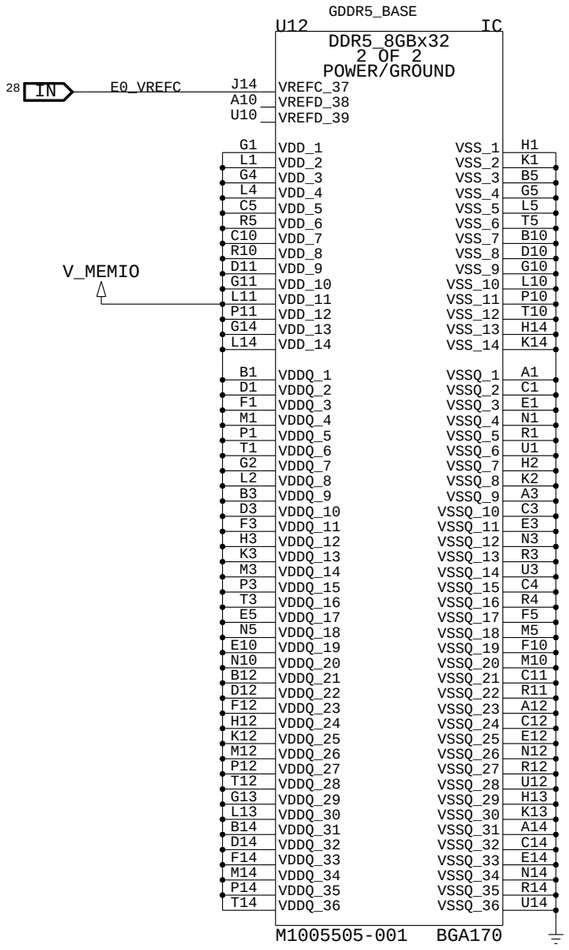


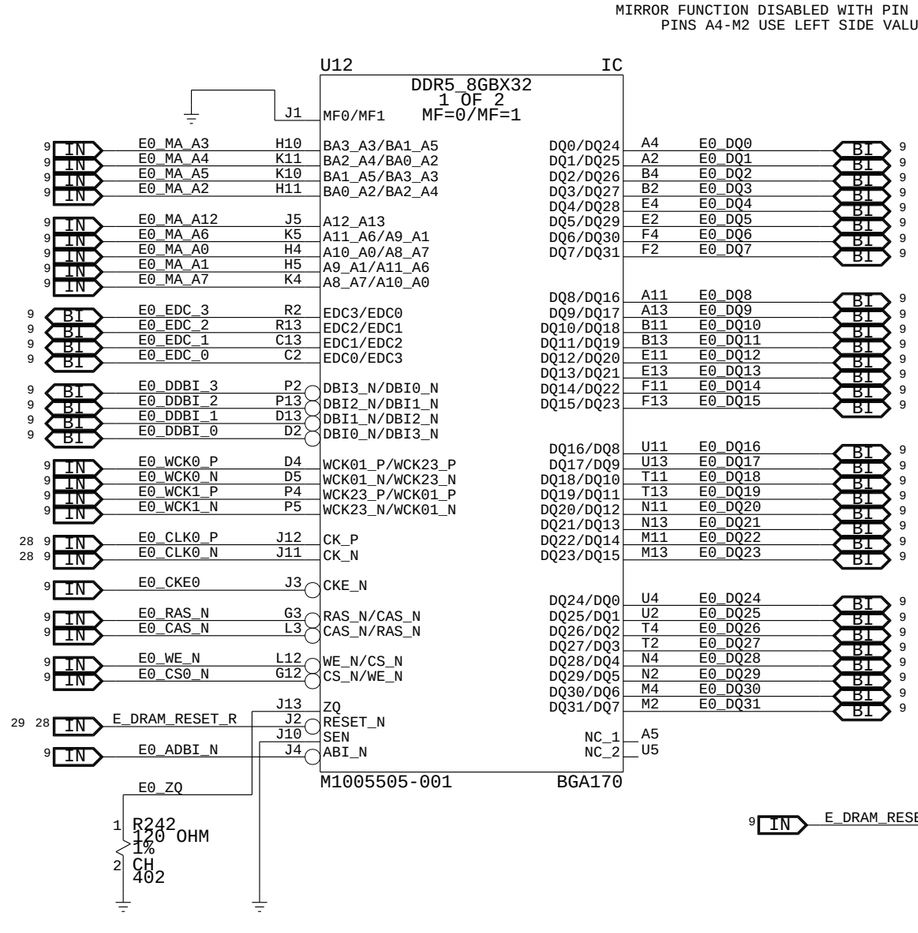
MEMORY CHANNEL D1 DECOUPLING

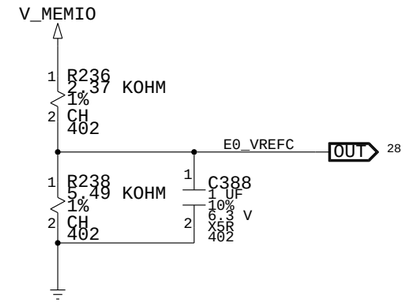


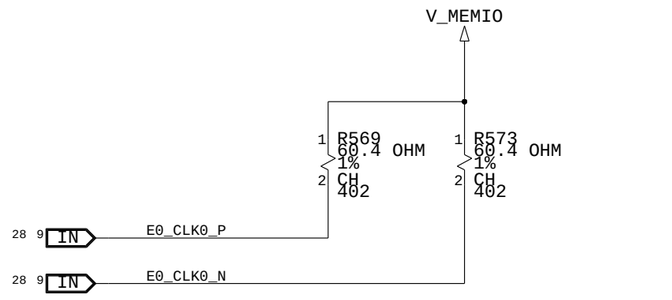
NOTE: ADDITIONAL MEMORY DECOUPLING ON PAGE 33

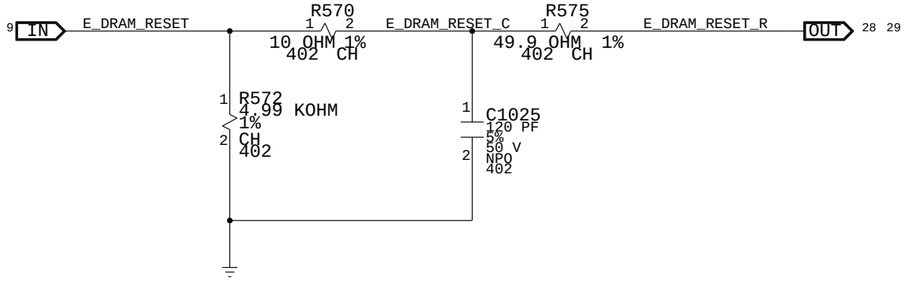
MEMORY: CHANNEL E0





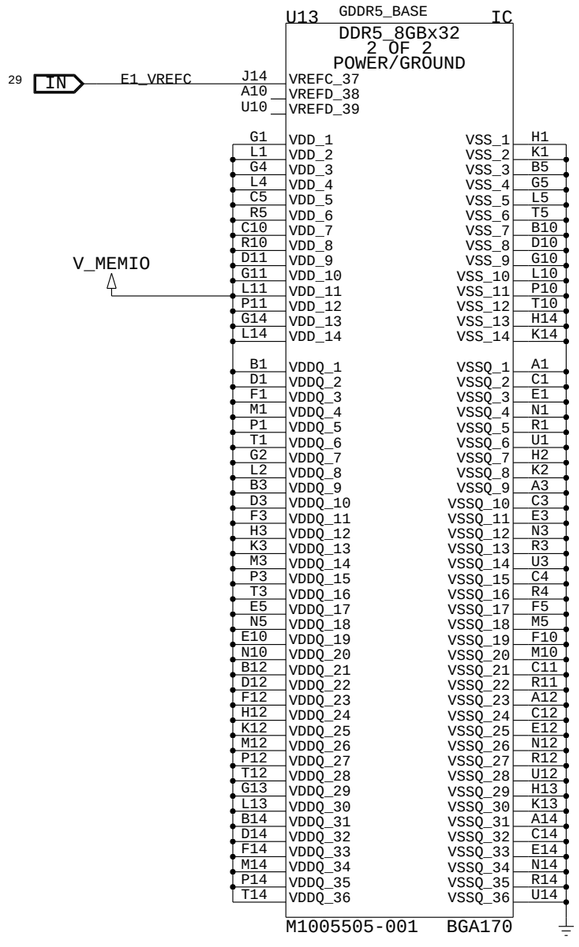




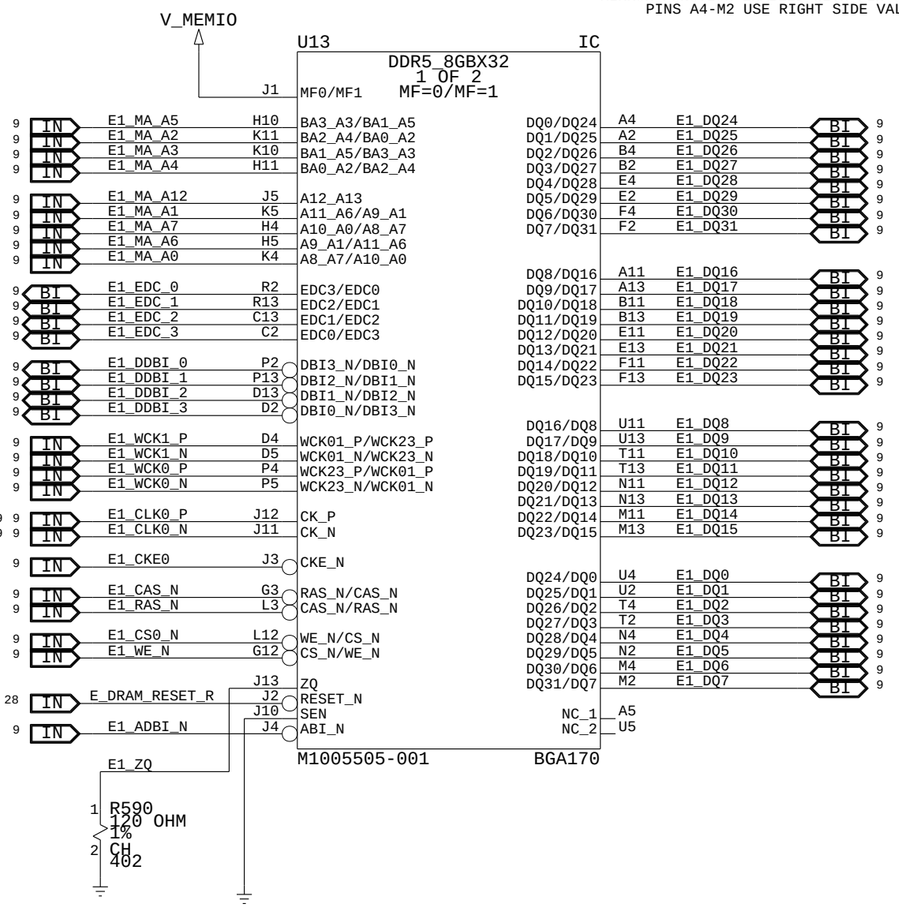


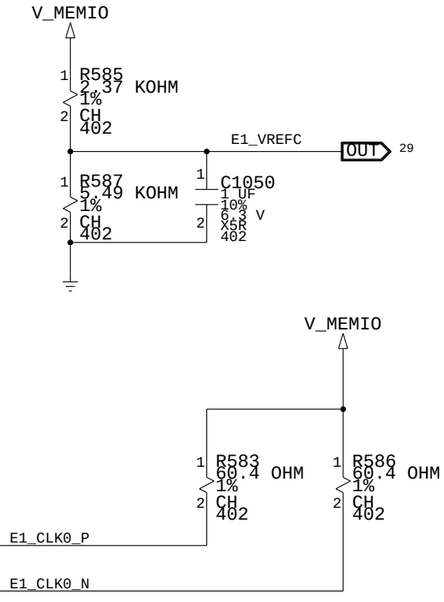
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	28/82	28/82	G-R	0.991

MEMORY: CHANNEL E1



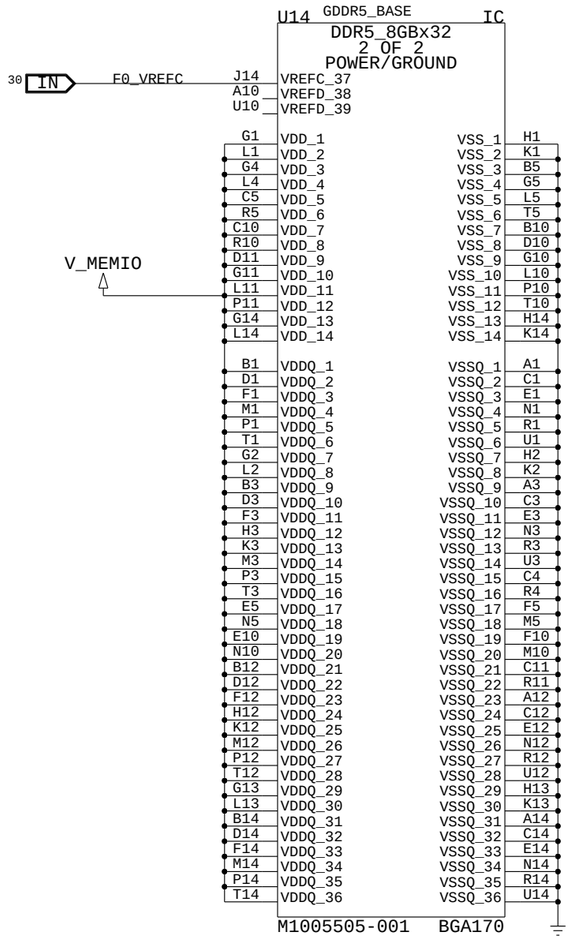
MIRROR FUNCTION ENABLED WITH PIN J1 HIGH
PINS A4-M2 USE RIGHT SIDE VALUES



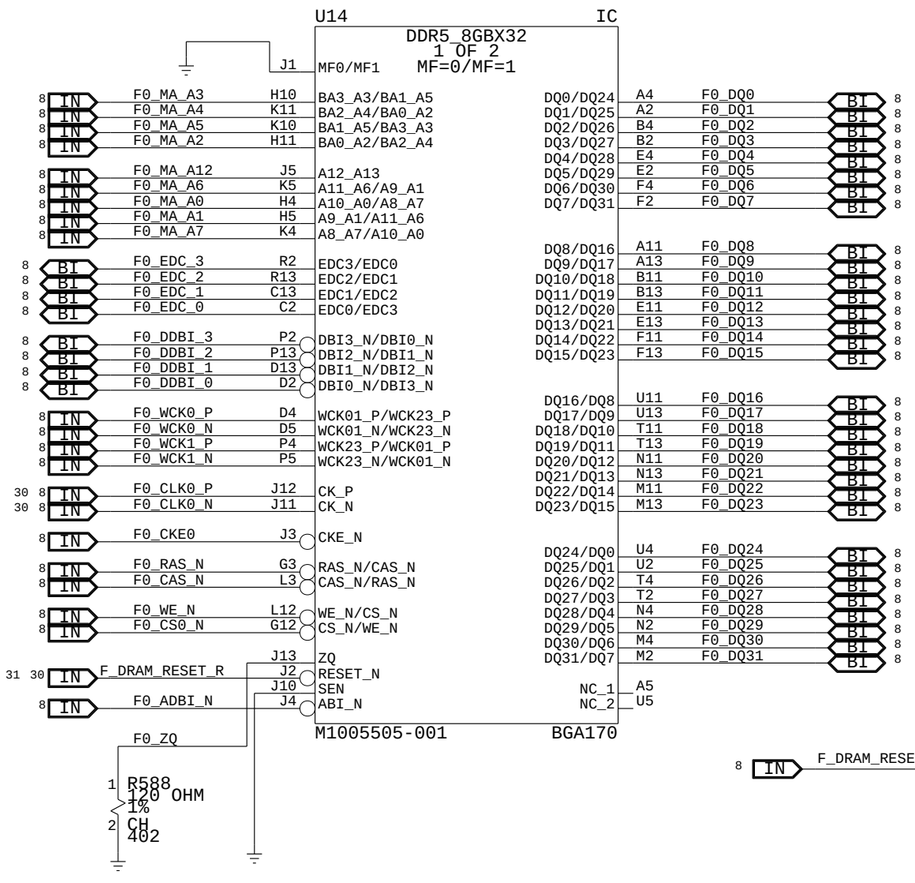


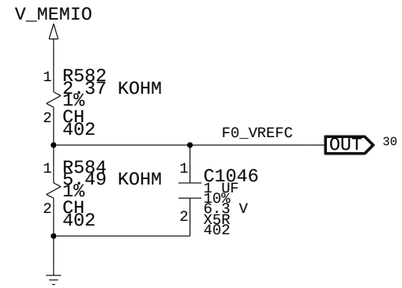
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	29/82	29/82	G-R	0.991

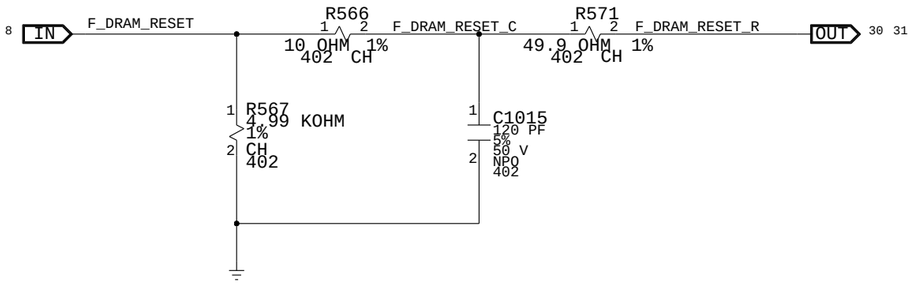
MEMORY: CHANNEL F0



MIRROR FUNCTION DISABLED WITH PIN J1 LOW
PINS A4-M2 USE LEFT SIDE VALUES

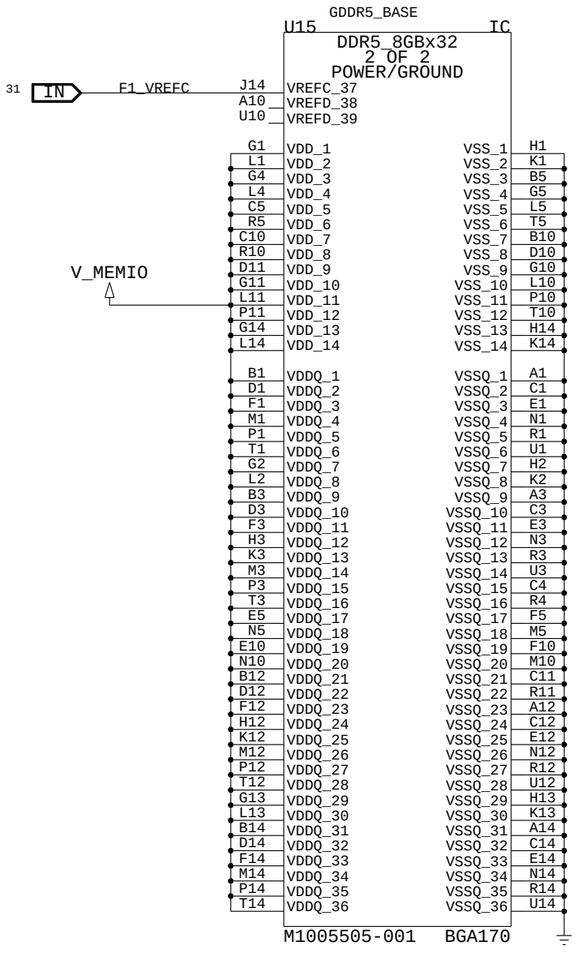


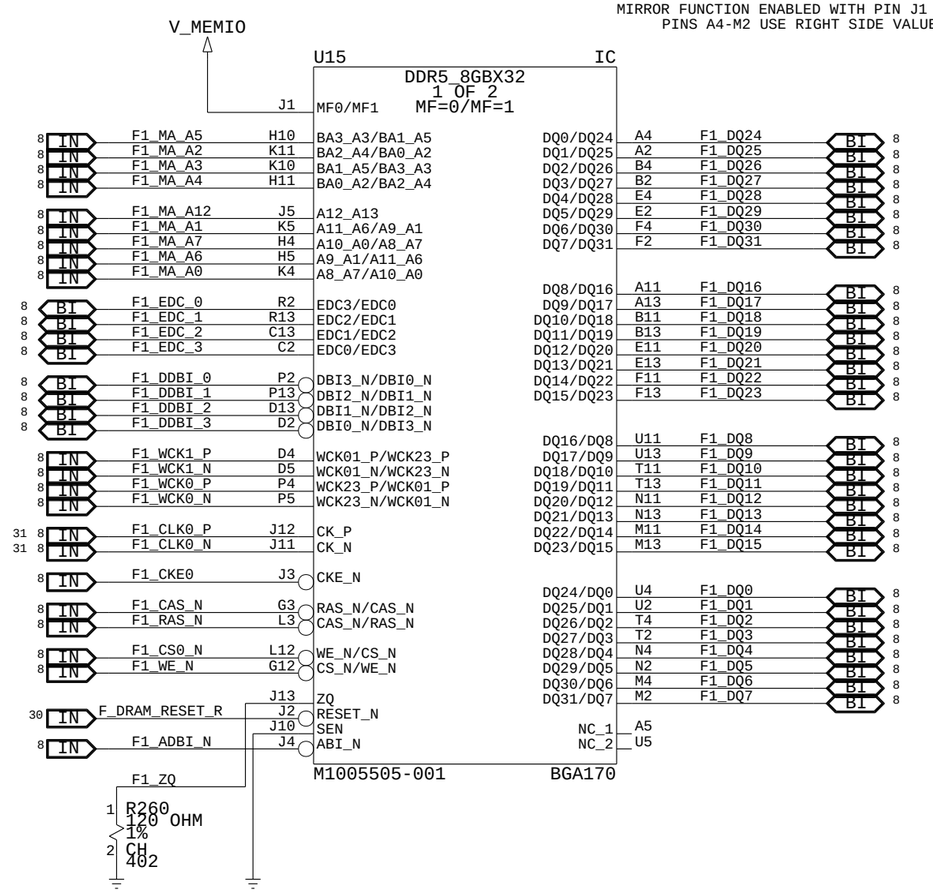


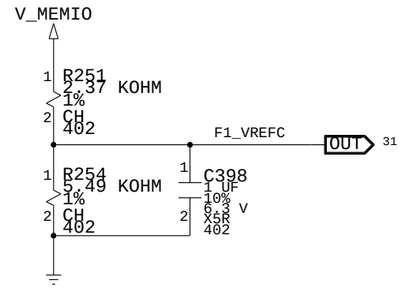


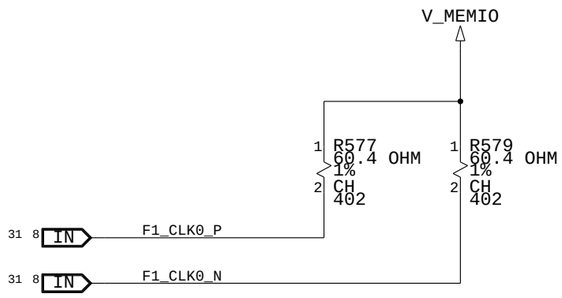
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	30/82	30/82	G-R	0.991

MEMORY: CHANNEL F1





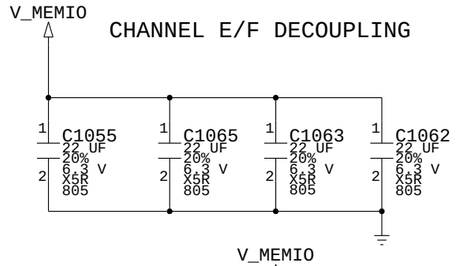




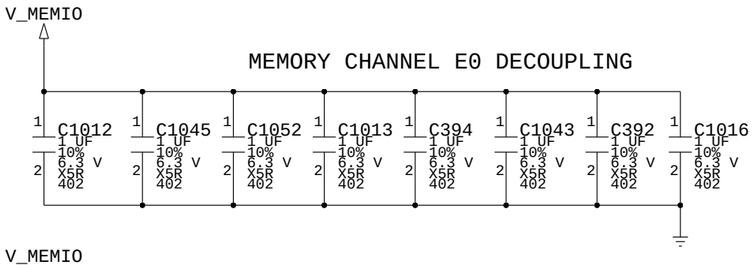
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	31/82	31/82	G-R	0.991

MEMORY: CHANNEL E/F DECOUPLING

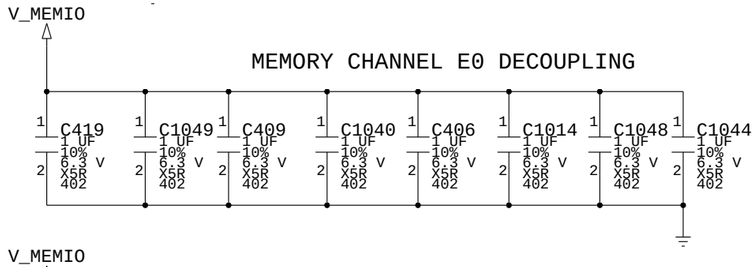
CHANNEL E/F DECOUPLING



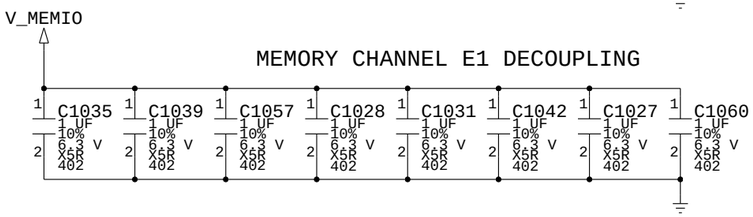
MEMORY CHANNEL E0 DECOUPLING



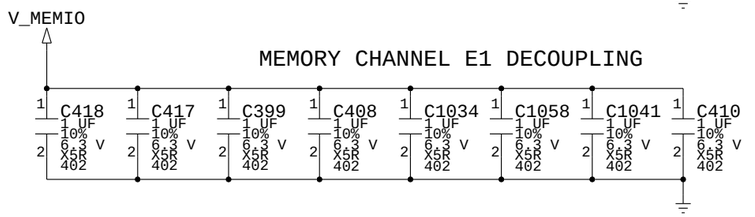
MEMORY CHANNEL E0 DECOUPLING



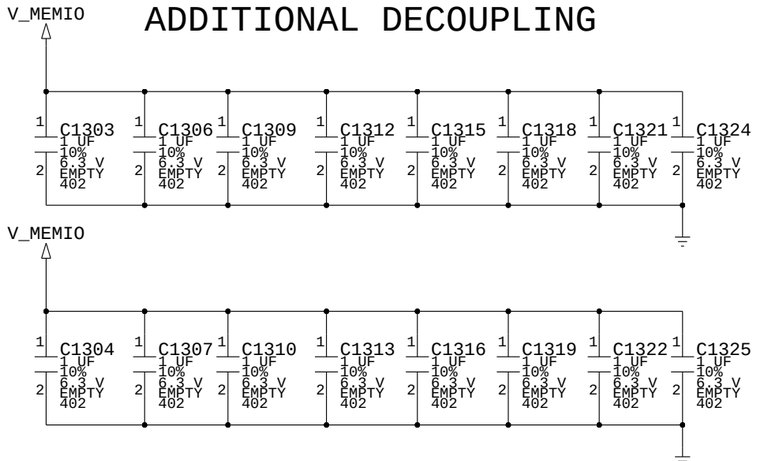
MEMORY CHANNEL E1 DECOUPLING



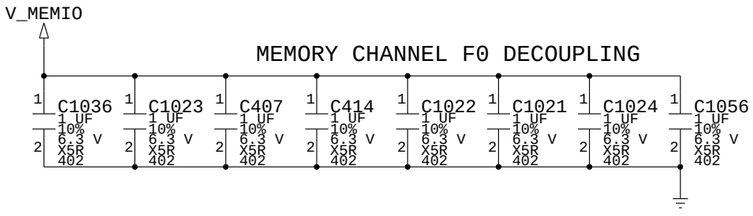
MEMORY CHANNEL E1 DECOUPLING



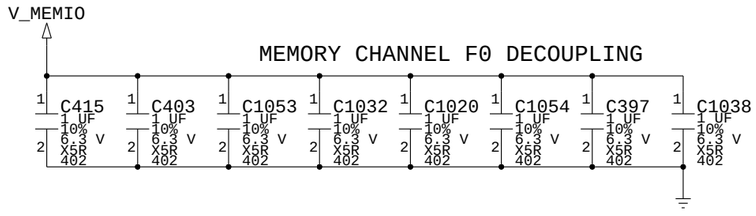
ADDITIONAL DECOUPLING

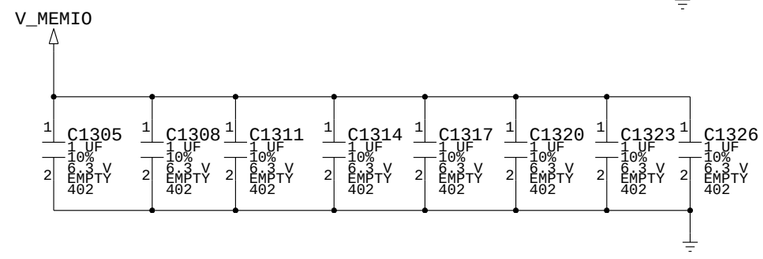


MEMORY CHANNEL F0 DECOUPLING

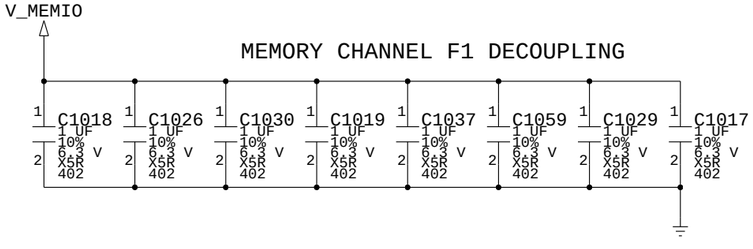


MEMORY CHANNEL F0 DECOUPLING

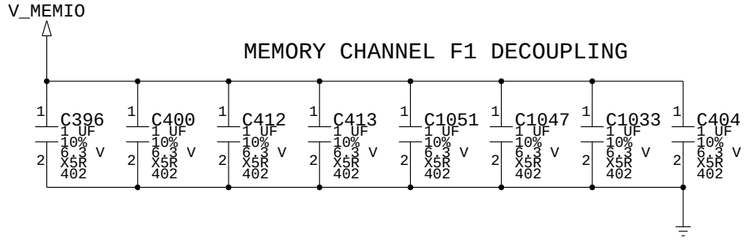




MEMORY CHANNEL F1 DECOUPLING



MEMORY CHANNEL F1 DECOUPLING

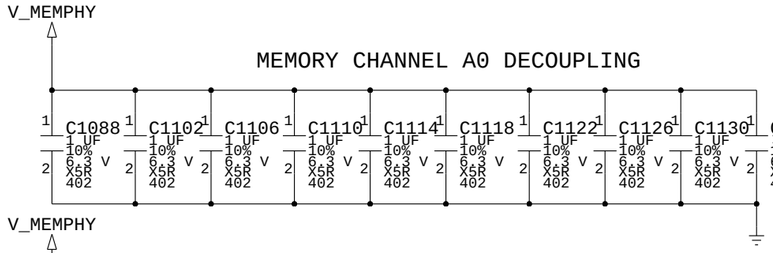


NOTE: ADDITIONAL MEMORY DECOUPLING ON PAGE 33

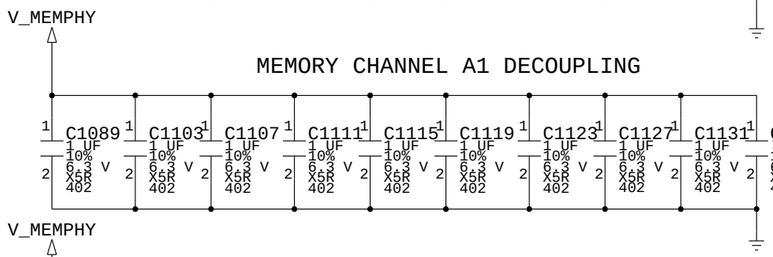
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	32/82	32/82	G-R	0.991

MEMORY: ADDITIONAL DECOUPLING

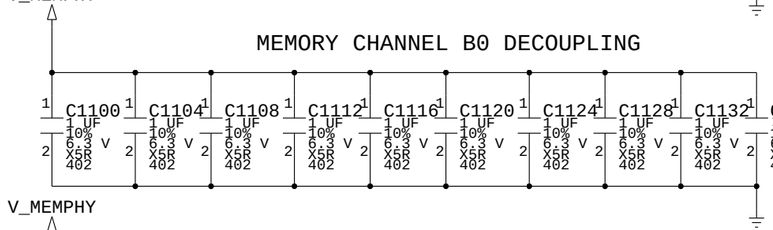
MEMORY CHANNEL A0 DECOUPLING



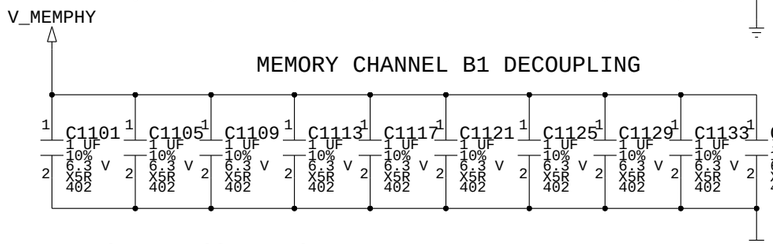
MEMORY CHANNEL A1 DECOUPLING



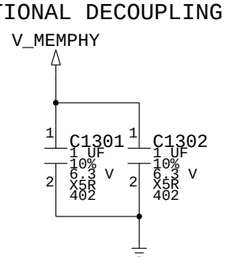
MEMORY CHANNEL B0 DECOUPLING



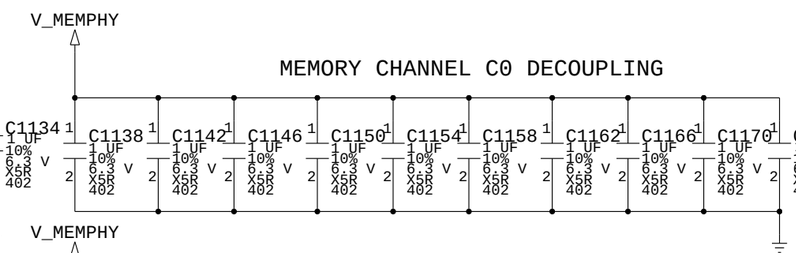
MEMORY CHANNEL B1 DECOUPLING



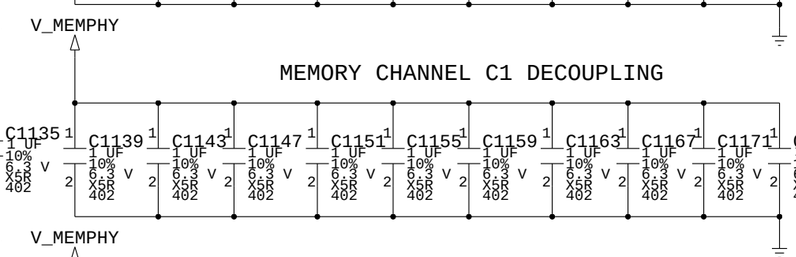
ADDITIONAL DECOUPLING



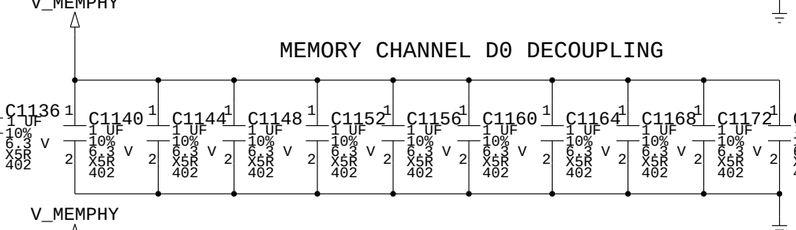
MEMORY CHANNEL C0 DECOUPLING



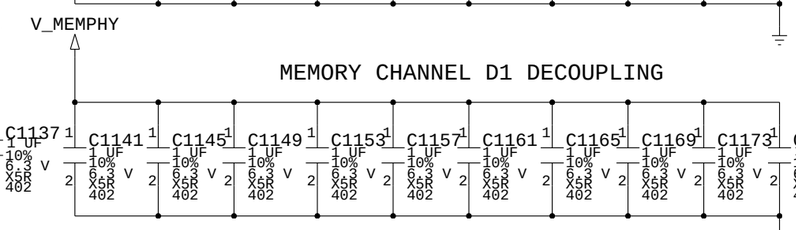
MEMORY CHANNEL C1 DECOUPLING



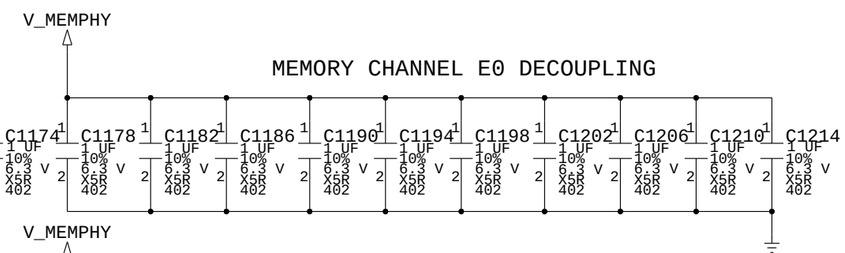
MEMORY CHANNEL D0 DECOUPLING



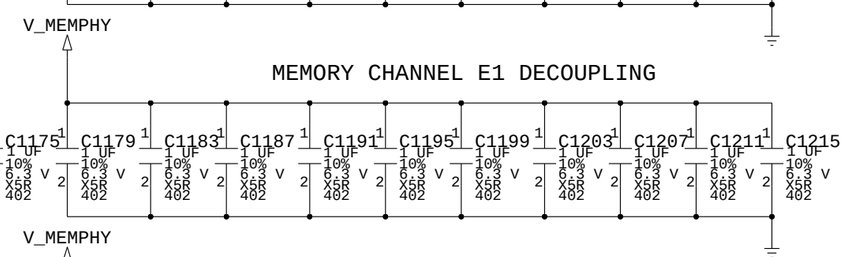
MEMORY CHANNEL D1 DECOUPLING



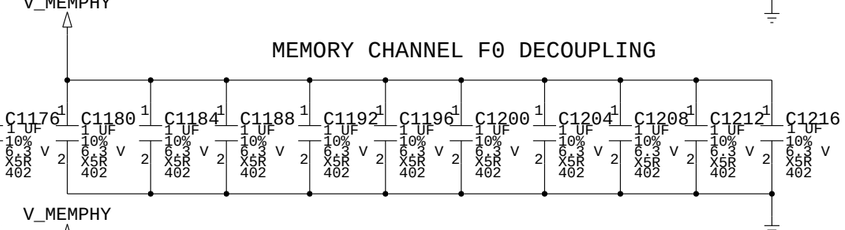
MEMORY CHANNEL E0 DECOUPLING



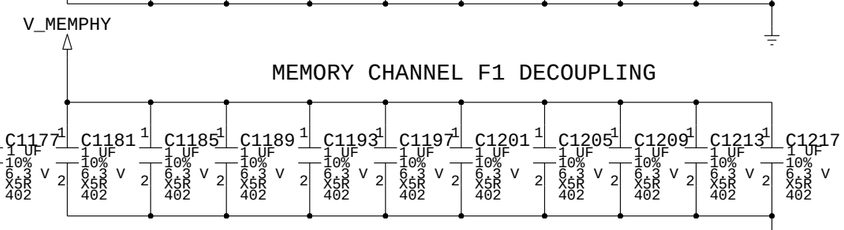
MEMORY CHANNEL E1 DECOUPLING



MEMORY CHANNEL F0 DECOUPLING



MEMORY CHANNEL F1 DECOUPLING



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	33/82	33/82	G-R	0.991

KIC: USB

U2 KIC IC

6 of 11

USBD_D0_DP	AF8			USB2_WIFI_DP	BI	46	WIFI
USBD_D0_DN	AE8			USB2_WIFI_DN	BI	46	
USBC_D0_DP	AC4			USB2_AUX_DP	BI	45	REAR 1
USBC_D0_DN	AC3			USB2_AUX_DN	BI	45	
REAR 1 45 IN USB3_AUX_RP	Y1	USBC_D1_RXP	USBC_D1_TXP	W3 USB3_AUX_TP_C	C501 0.1 UF 10% X5R 16 V 402	USB3_AUX_TP OUT	45
REAR 1 45 IN USB3_AUX_RN	Y2	USBC_D1_RXN	USBC_D1_TXN	W4 USB3_AUX_TN_C	C500 0.1 UF 10% X5R 16 V 402	USB3_AUX_TN OUT	45
REAR 0 45 IN USB3_BP_P1_RP	V1	USBB_D2_RXP	USBB_D2_TXP	U3 USB3_BP_P1_TP_C	C499 0.1 UF 10% X5R 16 V 402	USB3_BP_P1_TP OUT	45
REAR 0 45 IN USB3_BP_P1_RN	V2	USBB_D2_RXN	USBB_D2_TXN	U4 USB3_BP_P1_TN_C	C498 0.1 UF 10% X5R 16 V 402	USB3_BP_P1_TN OUT	45
			USBB_D0_DP	AE4		USB2_BP_P1_DP BI	45
			USBB_D0_DN	AE3		USB2_BP_P1_DN BI	45
			USBB_D1_DP	AD2		USB2_BP_P0_DP 1 DB85	NOT USED
			USBB_D1_DN	AD1		USB2_BP_P0_DN 1 DB84	
NOT USED DB90 1 USB3_BP_P0_RP	T1	USBB_D3_RXP	USBB_D3_TXP	R3		USB3_BP_P0_TP 1 DB14	
NOT USED DB91 1 USB3_BP_P0_RN	T2	USBB_D3_RXN	USBB_D3_TXN	R4		USB3_BP_P0_TN 1 DB15	
FRONT 45 IN USB3_FP_P0_RP_BUFF	AA8	USBA_D2_RXP	USBA_D2_TXP	AB10 USB3_FP_P0_TP_C	C1097 0.1 UF 10% X5R 16 V 402	USB3_FP_P0_TP OUT	45
FRONT 45 IN USB3_FP_P0_RN_BUFF	AA7	USBA_D2_RXN	USBA_D2_TXN	AB9 USB3_FP_P0_TN_C	C1096 0.1 UF 10% 16 V 402 X5R	USB3_FP_P0_TN OUT	45
			USBA_D0_DP	AC7		USB2_FP_P0_DP BI	45
			USBA_D0_DN	AC8		USB2_FP_P0_DN BI	45
			USBA_D1_DP	AF6		USB2_ACC_DP BI	51 FRONT PANEL ACC
			USBA_D1_DN	AF5		USB2_ACC_DN BI	51
NOT USED DB18 1 USB3_ACC_RP	AB1	USBA_D3_RXP	USBA_D3_TXP	AA3		USB3_ACC_TP 1 DB20	NOT USED
NOT USED DB17 1 USB3_ACC_RN	AB2	USBA_D3_RXN	USBA_D3_TXN	AA4		USB3_ACC_TN 1 DB22	

USBA_D2_AMOUT	AA5	USBA_D2_AMOUNT 1	DB97
USBA_D1_AMOUT	AE6	USBA_D1_AMOUNT 1	DB23
USBA_D0_AMOUT	AC11	USBA_D0_AMOUNT 1	DB100
USBB_D2_AMOUT	R5	USBB_D2_AMOUNT 1	DB10
USBB_D1_AMOUT	AD5	USBB_D1_AMOUNT 1	DB95
USBB_D0_AMOUT	AF4	USBB_D0_AMOUNT 1	DB94
USBC_D1_AMOUT	W5	USBC_D1_AMOUNT 1	DB24
USBC_D0_AMOUT	AC5	USBC_D0_AMOUNT 1	DB21
USBD_D0_AMOUT	AE9	USBD_D0_AMOUNT 1	DB98

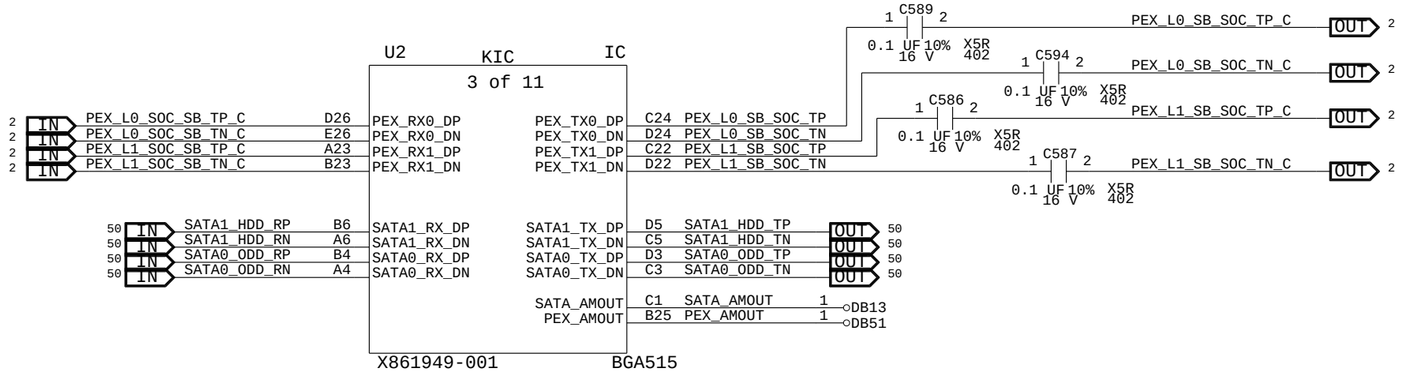
USBA_D1_TXRTUNE AB11 USBA_D1_TXRTUNE

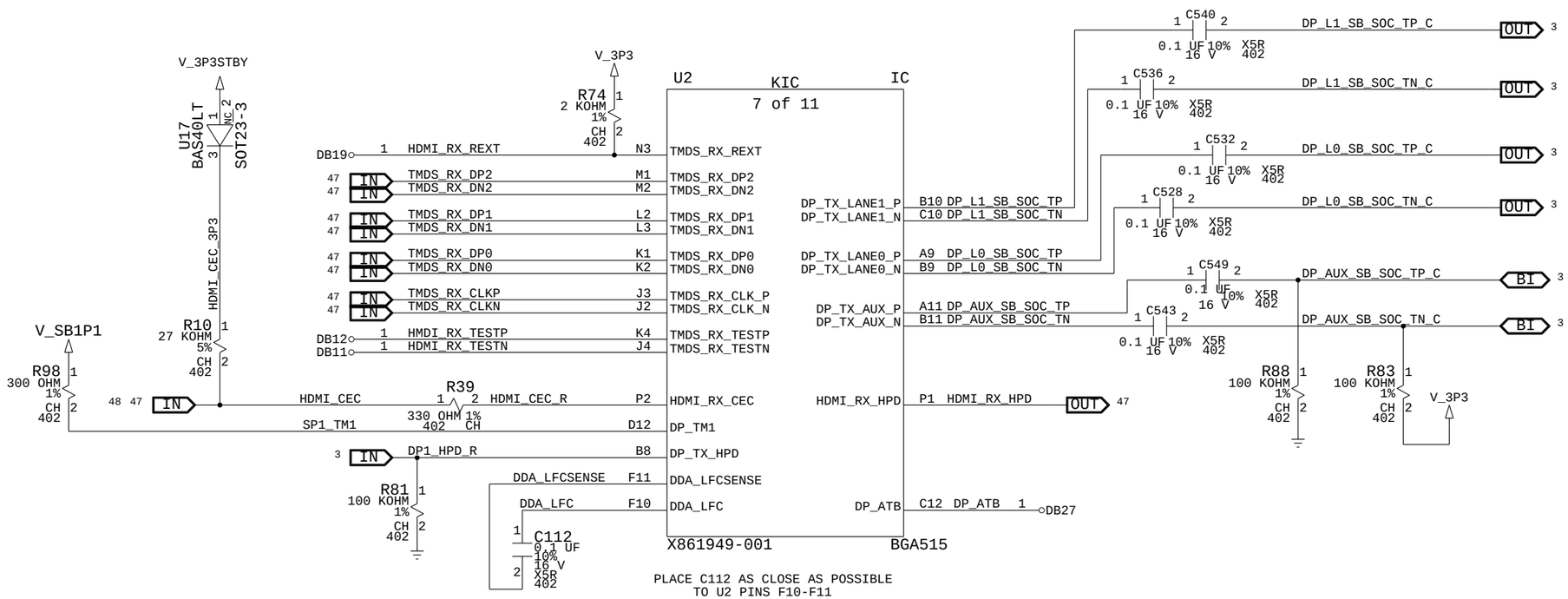
R86 1 2 174 OHM 1% CH 402

X861949-001 BGA515

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	34/82	34/82	G-R	0.99

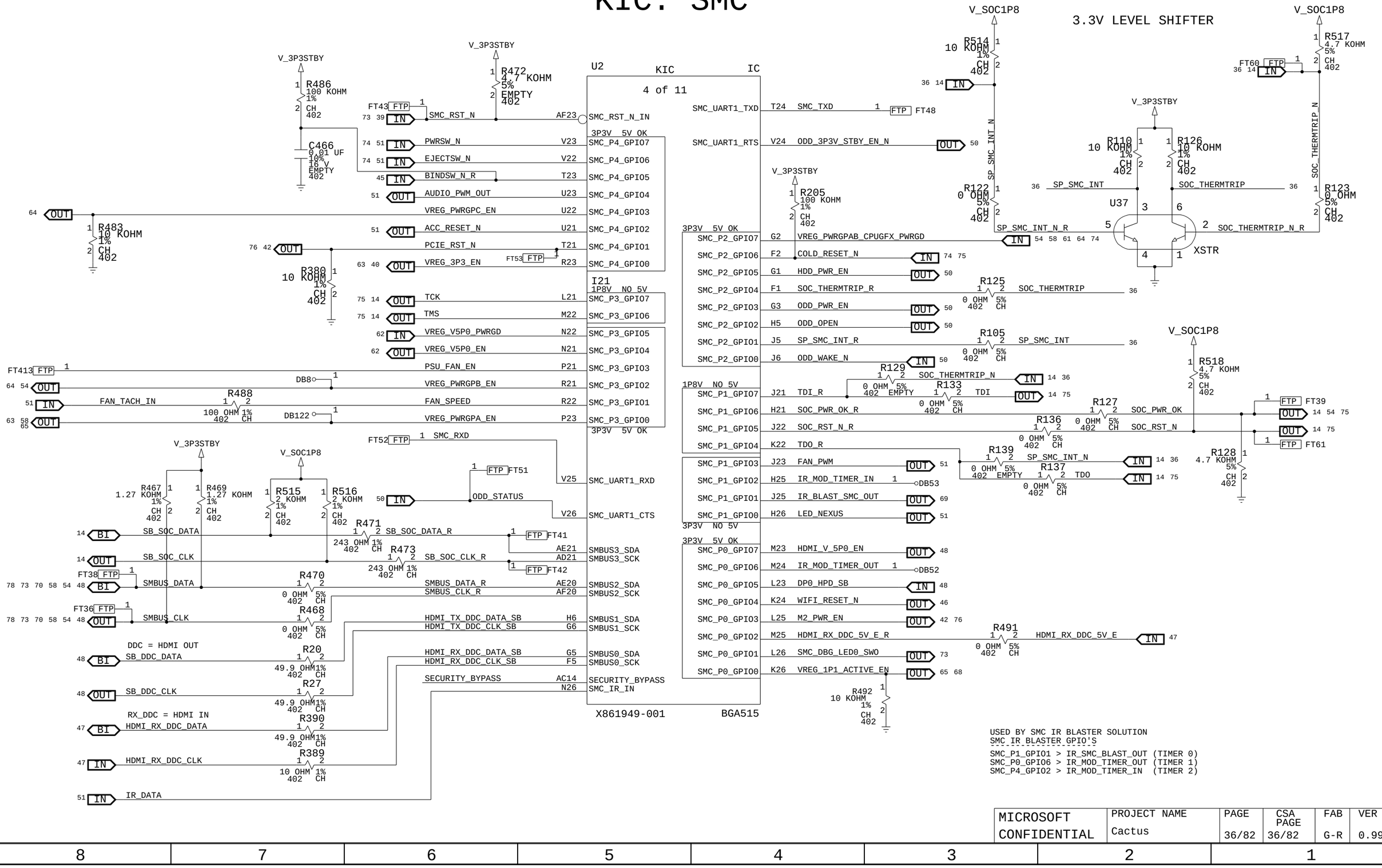
KIC: PCIEX,SATA,VIDEO





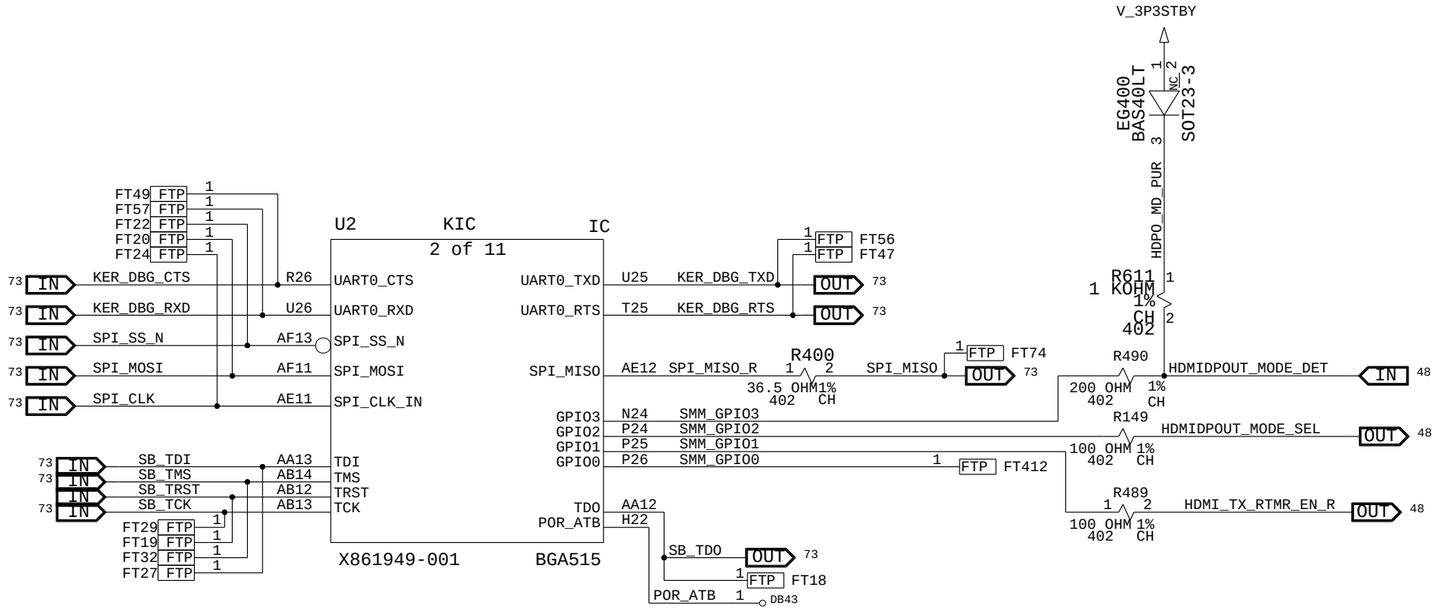
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	35/82	35/82	G-R	0.991

KIC: SMC



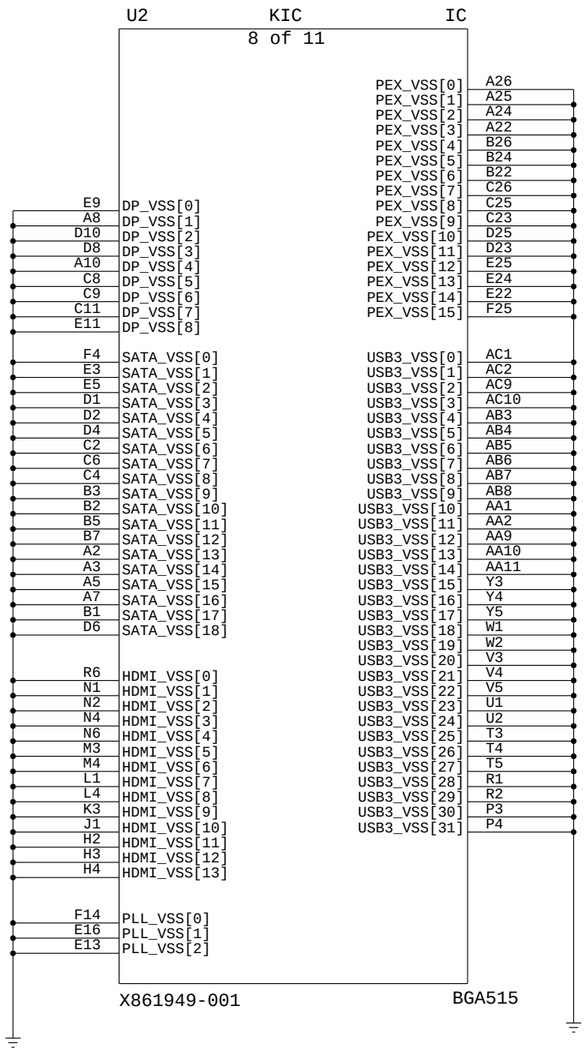
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	36/82	36/82	G-R	0.991

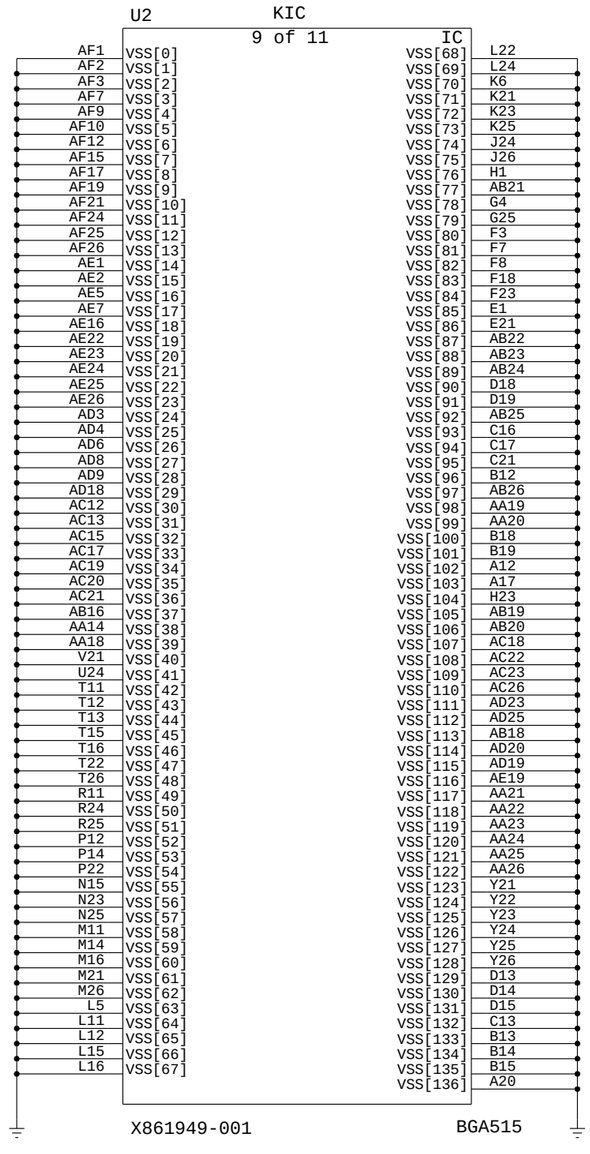
KIC: FACET



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	37/82	37/82	G-R	0.991

KIC: POWER





MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	38/82	38/82	G-R	0.991

KIC: CLOCKS,STRAPPING,POR

PEX REF CLOCKS CONTROLLED BY SMC

V_3P3
R94 10 KOHM 1% 2 CH 402
R90 10 KOHM 1% 2 EMPTY 402
R108 10 KOHM 1% 2 CH 402
R107 10 KOHM 1% 2 EMPTY 402
V_1P8STBY

SMC_XTAL_OUT
R461 249 KOHM 1% 402 CH
Y2 25 MHZ XTAL M1020244-001 SM
C582 30 PF 5% 50 V NPO 402
C585 30 PF 5% 50 V NPO 402
R465 49.9 OHM 1% EMPTY 402
R457 1 KOHM 1% 402 CH
SMC_XTAL_OUT_R
SMC_XTAL_IN
R121 10 KOHM 1% 402 CH
SMC_BYPASS_CLK_IN

KIC_BASE
U2 KIC 1 of 11 IC

	G22	V_VDD18_DET	
PEX_REF_CLK1_REQN	C18	PEX_REF_CLK1_REQN	
PEX_REF_CLK2_REQN	C19	PEX_REF_CLK2_REQN	
	AD22	VPGM	
DB36 1 BKUP_SB_SYNC_CLKP	E18	100M_SYNC_CLK_BYPASS_DP	
DB42 1 BKUP_SB_SYNC_CLKN	E19	100M_SYNC_CLK_BYPASS_DN	
SMC_XTAL_IN	A18	XTAL_CLK_OUT	
	A19	XTAL_CLK_IN	
	AD24	TEST	
SMC_BYPASS_CLK_IN	D21	SMC_BYPASS_CLK_IN	
DB25 1 BKUP_SB_PEX_REF_CLKP	E20	PCIE_BYPASS_CLK_DP	
DB28 1 BKUP_SB_PEX_REF_CLKN	D20	PCIE_BYPASS_CLK_DN	
DB46 1 250M_CLK_BYPASS_DP	F20	250M_CLK_BYPASS_DP	
DB47 1 250M_CLK_BYPASS_DN	F21	250M_CLK_BYPASS_DN	
DB31 1 BKUP_SB_AV_CLKP	D16	AV_CLK_BYPASS_DP	
DB32 1 BKUP_SB_AV_CLKN	D17	AV_CLK_BYPASS_DN	

X861949-001

BGA515

V_12P0_GATED
C212 1 UF 10% 16 V X5R 603
R494 10 KOHM 1% 2 CH 402
R493 1.13 KOHM 1% 2 CH 402
R494/V_EXT_DET IS NOW CONNECTED TO V_12P0_GATED
NOMINAL TRIP POINT = 9.55V

V_EXT_DET	G21	V_EXT_DET	
V_EXT_OK	F22	V12P0_PWRGD	OUT 64 → DB49
SMC_RST_N_OUT	AF22	SMC_RST_N_OUT_R	R476 1 KOHM 1% 402 CH → SMC_RST_N OUT 36 73
CLK_MONITOR	E17	SB_CLK_MONITOR	DB29
RTC_CLK_OUT	A21	RTC_CLK_OUT	R120 0 OHM 5% 402 CH → X32K_X2_R OUT 14
EMMC_CLK	AC16	MMC_CLK	OUT 43
ENET_REF_CLK	C20		ENET_REF_CLK OUT 42
SOC_NS_SYNC_CLK_DP	B16	SOC_SYNC_NS_100M_CLKP	OUT 2
SOC_NS_SYNC_CLK_DN	B17	SOC_SYNC_NS_100M_CLKN	OUT 2
SOC_NS_AV_CLK_DP	A13	SOC_AV_NS_100M_CLKP	OUT 2
SOC_NS_AV_CLK_DN	A14	SOC_AV_NS_100M_CLKN	OUT 2
PEX_REF_CLK2_DP	B20	SOC_NB_CLKP	R456 NO_M2 0 OHM 5% 402 CH; R460 NO_M2 0 OHM 5% 402 CH → SOC_NB_PEX_SS_100M_CLKP OUT 2 77
PEX_REF_CLK2_DN	B21	SOC_NB_CLKN	OUT 77 → R464 NO_M2 0 OHM 5% 402 CH; R459 NO_M2 0 OHM 5% 402 CH → SOC_NB_PEX_SS_100M_CLKN OUT 2 77
PEX_REF_CLK1_DP	C14	ENET_CLKP	R411 NO_M2 0 OHM 5% 402 CH; R423 NO_M2 0 OHM 5% 402 CH → ENET_PEX_SS_100M_CLKP OUT 42 77
PEX_REF_CLK1_DN	C15	ENET_CLKN	OUT 77 → R419 NO_M2 0 OHM 5% 402 CH; R428 NO_M2 0 OHM 5% 402 CH → ENET_PEX_SS_100M_CLKN OUT 42 77
PEX_REF_CLK0_DP	A15	SOC_CLKP	R427 NO_M2 0 OHM 5% 402 CH; R443 NO_M2 0 OHM 5% 402 CH → SOC_PEX_SS_100M_CLKP OUT 2 77
PEX_REF_CLK0_DN	A16	SOC_CLKN	R435 NO_M2 0 OHM 5% 402 CH; R449 NO_M2 0 OHM 5% 402 CH → SOC_PEX_SS_100M_CLKN OUT 2 77

KEEP DB29 AND DB30 CLOSE TO EACH OTHER IN LAYOUT

R112 69.8 KOHM 1% 2 EMPTY 402

C593 270 PF 10% 50 V X7R 402

M2_ONLY R432 10 KOHM 1% CH 402

M2_ONLY R462 10 KOHM 1% CH 402

TODO; IF SMCFW CHANGES BASED ON M2_ONLY STUFFING OPTION, THEN TURN OFF CLOCKS INSTEAD OF TERMINATING

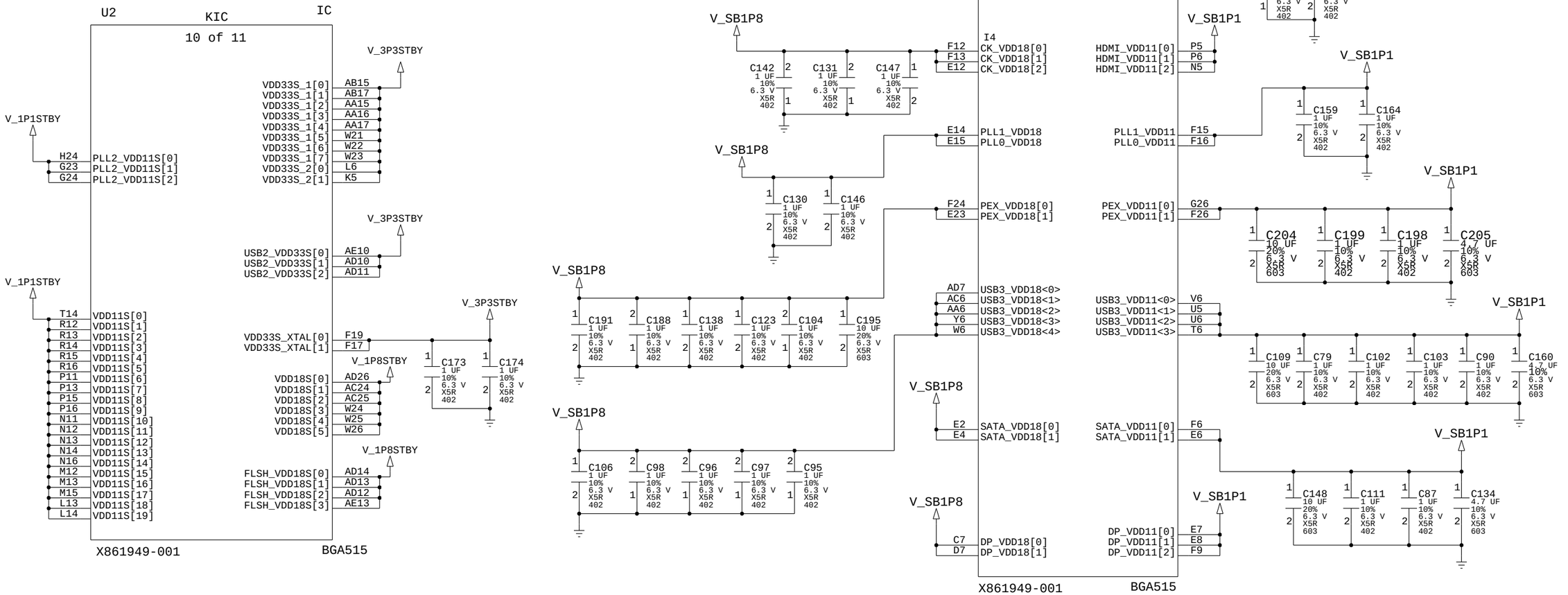
DO NOT STUFF RESISTORS IF BOTH HDD AND M2 ARE STUFFED

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X861949-007	IC	U2	IC,KRAKEN SB,BGA515	KIC_RETAIL
X861949-008	IC	U2	IC,KRAKEN SB,BGA515	KIC_DEV
X861949-008	EMPTY	U2	IC,KRAKEN SB,BGA515	KIC_EMPTY

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	39/82	39/82	G-R	0.991

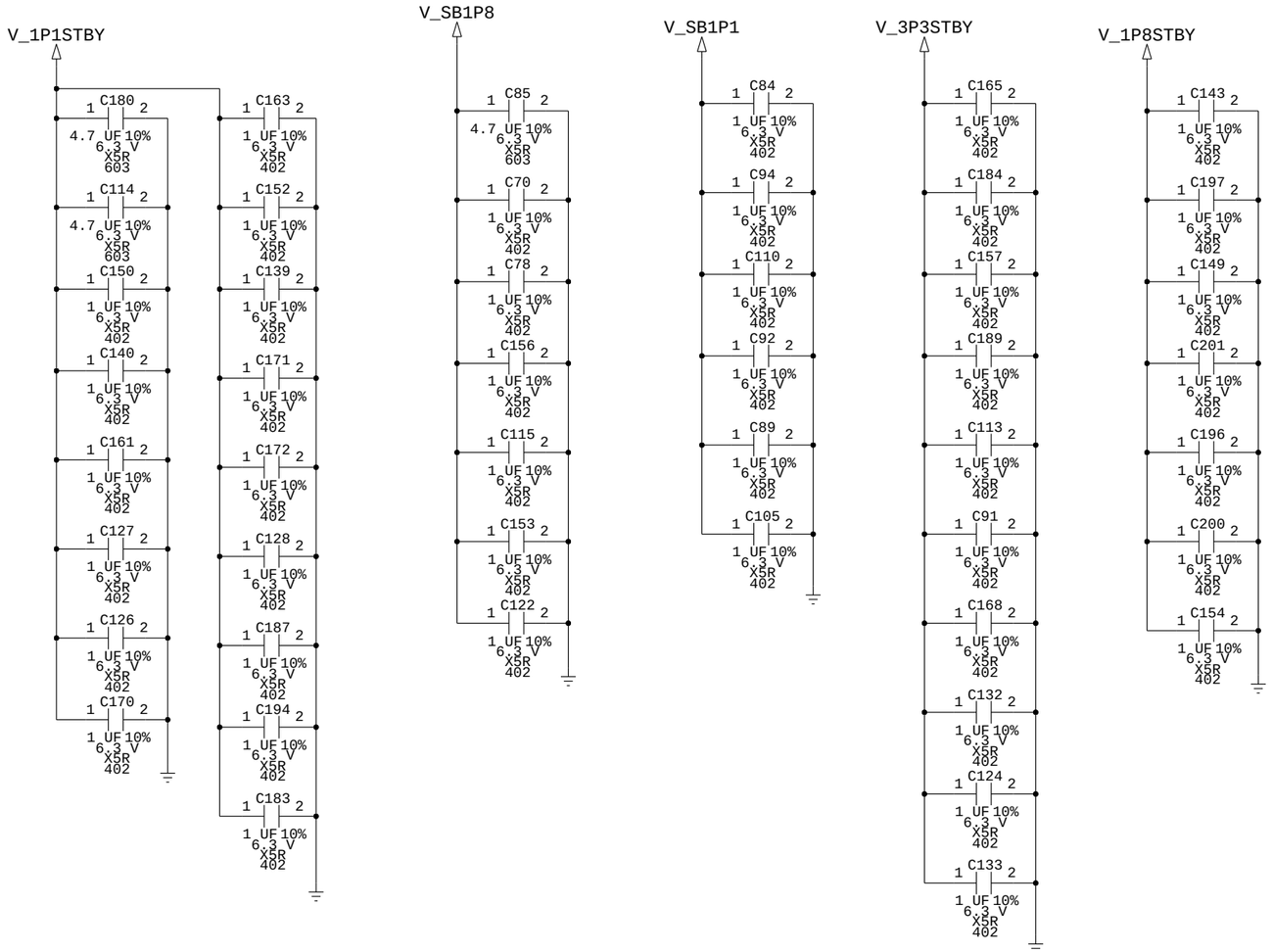
KIC: POWER

FET PREVENTS LEAKAGE THROUGH KRAKEN
FROM STANDBY RAILS TO 3P3 RAIL



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	40/82	40/82	G-R	0.991

KIC: DECOUPLING



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	41/82	41/82	G-R	0.991

ETHERNET CONTROLLER

RED = 1 GBPS LINK
GREEN = 10 MBPS LINK
NO INDICATION FOR 100 MBPS LINK

DEBUG D1 LED RED-GREEN SM

V_3P3_ENET
DEBUG R33 10 KOHM 1% CH 402
R357 0 OHM 5% 402 EMPTY
M2_PWR_EN
FT1 FTP
DEBUG R26 511 OHM 1% 402 CH
DEBUG R17 511 OHM 1% CH 402
R36 100 OHM 1% 402 CH
ENET_REF_CLK
DB4
R35 2.49 KOHM 1% CH 402
R37 0 OHM 5% 402 EMPTY
R365 10 KOHM 1% CH 402
FT9 FTP
PCIE_RST_N

U28 IC
RTL8111HM
X896524-002 QFN33

MDIP3	9	MDIP3	
MDIN3	10	MDIN3	
MDIP2	6	MDIP2	
MDIN2	7	MDIN2	
MDIP1	4	MDIP1	
MDIN1	5	MDIN1	
MDIP0	1	MDIP0	
MDIN0	2	MDIN0	
ENET_LED2	25	LED2	
ENET_GPO	26	LED1/GPO	
ENET_LED0	27	LED0	
ENET_RSET	31	RSET	
ENET_XTAL2	29	CKXTAL2	
ENET_XTAL1	28	CKXTAL1	
ENET_ISOLATE_N	20	ISOLATE_N	
PEX_SOC_ENET_TP_C	13	HSIP	
PEX_SOC_ENET_TN_C	14	HSIN	
ENET_PEX_SS_100M_CLKP	15	REFCLK_P	
ENET_PEX_SS_100M_CLKN	16	REFCLK_N	
	19	PERST_N	
		MPAD	33

FT2 FTP DB78
V_3P3_ENET
PLACE 0.1UF CLOSE TO PINS 11, 23 AND 32
PLACE 4.7UF CLOSE TO PINS 11 AND 32
C502 0.1 UF 10% 16 V X5R 402
C482 0.1 UF 10% 16 V X5R 402
C477 0.1 UF 10% 16 V X5R 402
C505 4.7 UF 10% 6.3 V X5R 603
C12 4.7 UF 10% 6.3 V X5R 603

V_1P0_ENET
PLACE 0.1UF CLOSE TO PINS 3, 8, 22 AND 30
C481 0.1 UF 10% 16 V X5R 402
C491 0.1 UF 10% 16 V X5R 402
C485 0.1 UF 10% 16 V X5R 402
C496 0.1 UF 10% 16 V X5R 402
C30 1 UF 10% 6.3 V X5R 402
C10 4.7 UF 10% 6.3 V X5R 603

AVDD33_2	32		
AVDD33_1	11		
DVDD10	22		
AVDD10_3	30		
AVDD10_2	8		
AVDD10_1	3		
VDDREG	23		
REGOUT	24		
LANWAKE_N	21	ENET_WAKE_N	
CLKREQ_N	12	ENET_CLKREQ_N	
HSOP	17		
HSON	18		
MPAD	33		

PLACE 0.1UF CLOSE TO PIN 24
C480 0.1 UF 10% 16 V X5R 402
FT12 FTP DB3

V_3P3_ENET
R366 10 KOHM 1% CH 402
V_3P3_ENET
R383 10 KOHM 1% CH 402
REF CLK CONTROLLED BY SMC

PEX_ENET_SOC_TP
C37 0.1 UF 10% 16 V X5R 402
PEX_ENET_SOC_TP_C OUT 2

PEX_ENET_SOC_TN
C34 0.1 UF 10% 16 V X5R 402
PEX_ENET_SOC_TN_C OUT 2

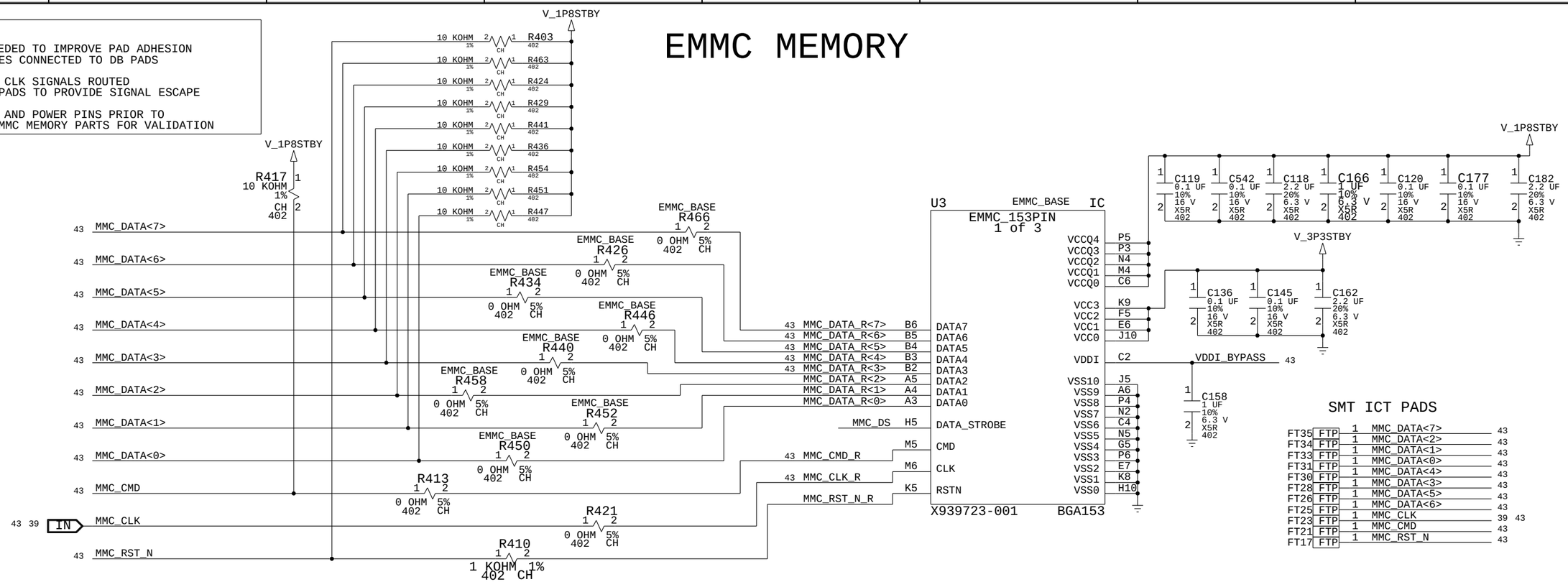
SOFT START
NOM. VOLTAGE: 3.3V
MAX POWER: 590MW

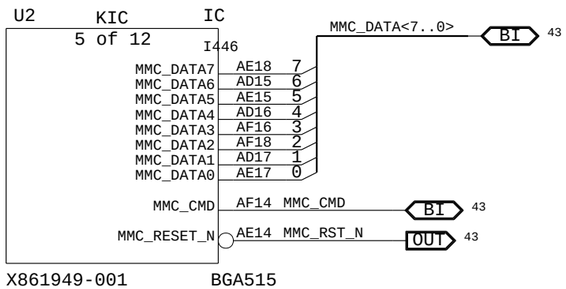
V_3P3
U30 FET SOT23 X889118-002
C47 1 UF 10% 6.3 V X5R 402
R61 100 OHM 1% 402 CH
V_ENET_G
V_ENET_G_R
R67 20 KOHM 1% CH 402
C32 0.22 UF 10% 25 V X7R 603
V_3P3_ENET
C31 10 UF 20% 6.3 V X5R 603

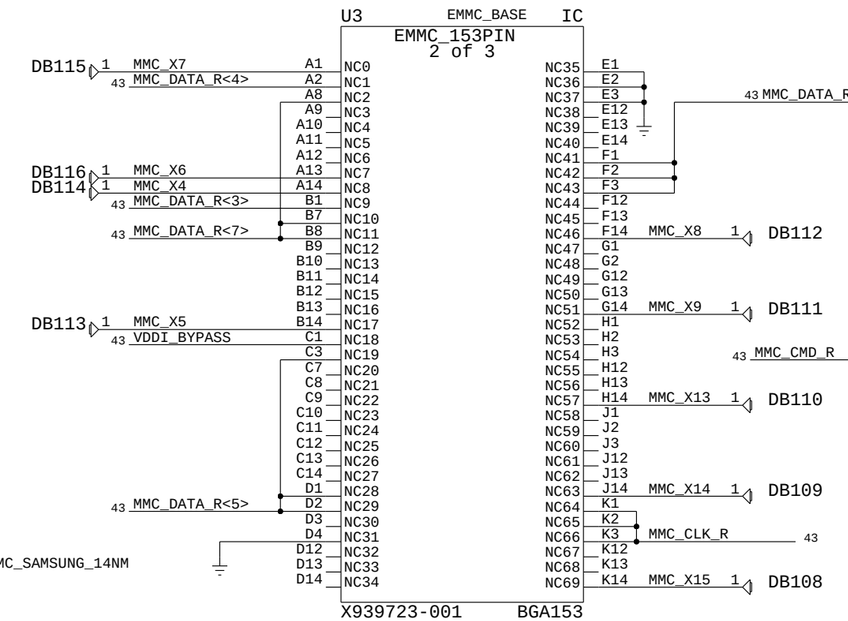
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	42/82	42/82	G-R	0.991

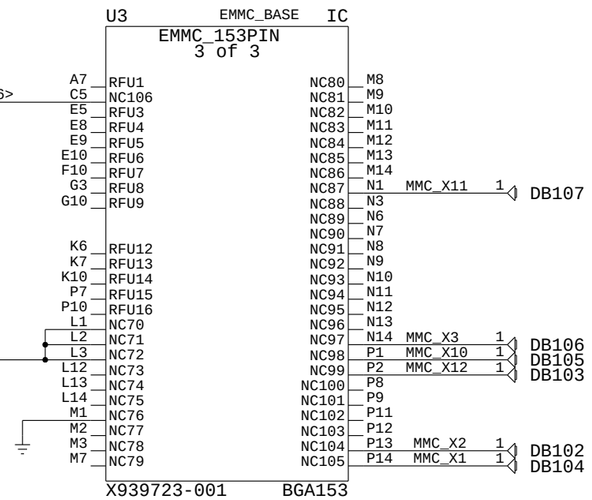
EMMC MEMORY

NOTES:
1. MMC_X NETS ARE NEEDED TO IMPROVE PAD ADHESION USING 13 MIL TRACES CONNECTED TO DB PADS
2. EMMC DATA,CMD AND CLK SIGNALS ROUTED THROUGH MULTIPLE PADS TO PROVIDE SIGNAL ESCAPE
3. VERIFY ALL SIGNAL AND POWER PINS PRIOR TO CONSIDERING NEW EMMC MEMORY PARTS FOR VALIDATION





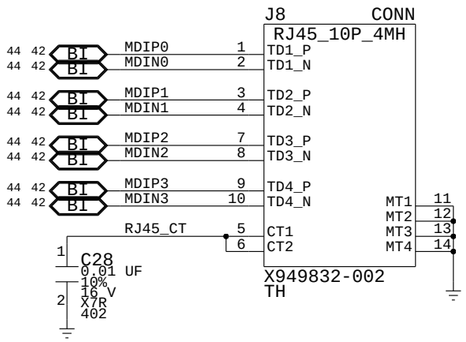


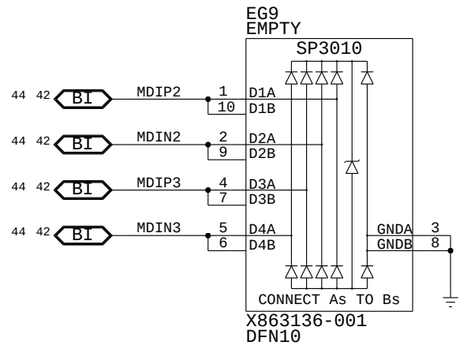


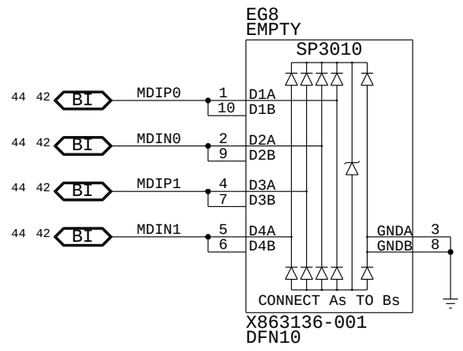
MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X934261-001	IC	U3	MEM,8GB,EMMC,FLASH,15NM,BGA153,TOSHIBA	EMMC_TOSHIBA_15NM
X945540-002	IC	U3	MEM,8GB,EMMC,FLASH,14NM,BGA153,SAMSUNG	EMMC_SAMSUNG_14NM
X939723-001	IC	U3	MEM,8GB,EMMC,FLASH,16NM,BGA153,HYNIX	EMMC_HYNIX_16NM
X800617-001	RES	R426,R434,R440,R446,R450,R452,R458,R466	49.9 OHM 1%,1/16W,0402	EMMC_TOSHIBA_15NM,EMMC_SAMSUNG_14NM
X809936-001	RES	R426,R434,R440,R446,R450,R452,R458,R466	100 OHM 1%,1/16W,0402	EMMC_HYNIX_16NM

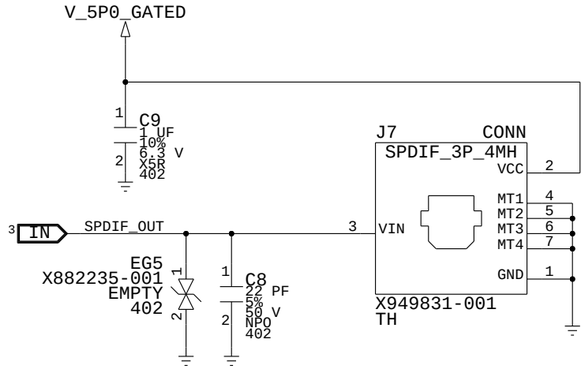
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	43/82	43/82	G-R	0.991

CONN: RJ45,TOSLINK









MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	44/82	44/82	G-R	0.991

CONN: USB (FRONT & REAR)

EG26
ESD ARRAY
SP3010
X863136-001
DFN10

EG25
ESD ARRAY
SP3010
X863136-001
DFN10

EG27
EMPTY
SP3010
X863136-001
DFN10

REAR 1 (KINECT)
J4 CONN
USB3_9P_4MH
X949829-004
TH
TX/RX FROM
HOST PERSPECTIVE

REAR 0
J5 CONN
USB3_9P_4MH
X949829-004
TH
TX/RX FROM
HOST PERSPECTIVE

FRONT USB
MTG6
STANDOFF
M1015028-001
SM
MTG7
STANDOFF
M1015028-001
SM

FRONT USB CONNECTION
J27
2X10RCPT
SM

U79 IC
PTN36001
X949696-001
QFN12

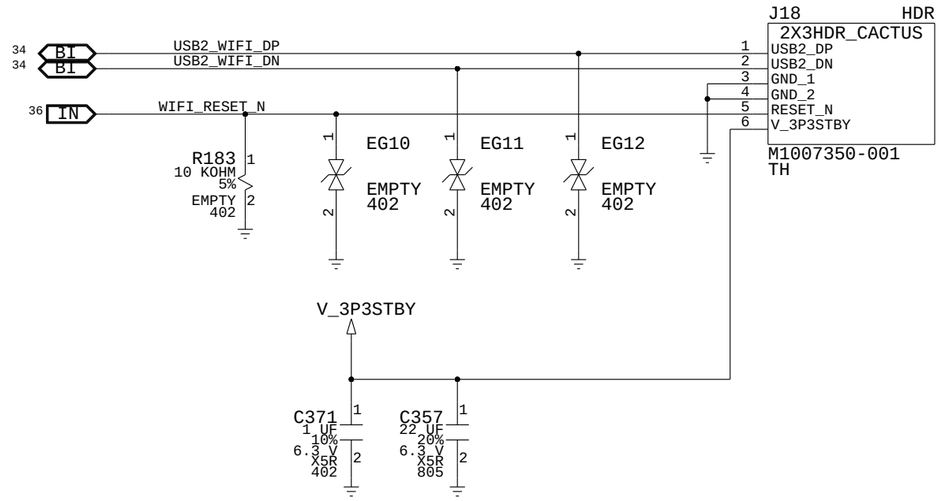
FILT U76
ECMF02_2HSMX6
X900532-002
DFN6

FILT U75
ECMF02_2HSMX6
X900532-002
DFN6

FILT U80
ECMF02_2HSMX6
X900532-002
DFN6

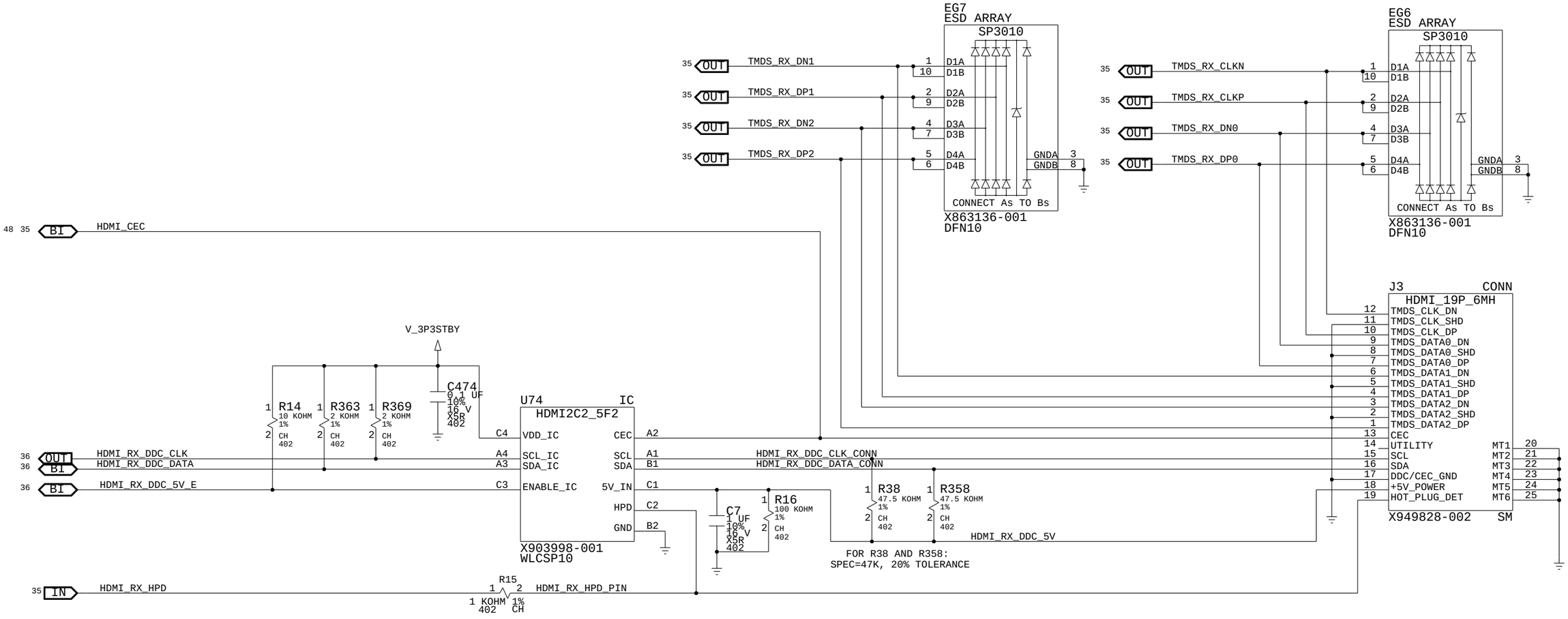
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	45/82	45/82	G-R	0.99

CONN: WIFI



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	46/82	46/82	G-R	0.991

CONN: HDMI IN



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	47/82	47/82	G-R	0.991

CONN: HDMI OUT

TDP158 CONTROL SLAVE ADDRESS			
SELECTED	A1/A0	7-BIT ADDRESS	8-BIT ADDRESS
-->	00	0X5E	BC/BD
	01	0X5D	BA/BB
	10	0X5C	B8/B9
	11	0X5B	B6/B7

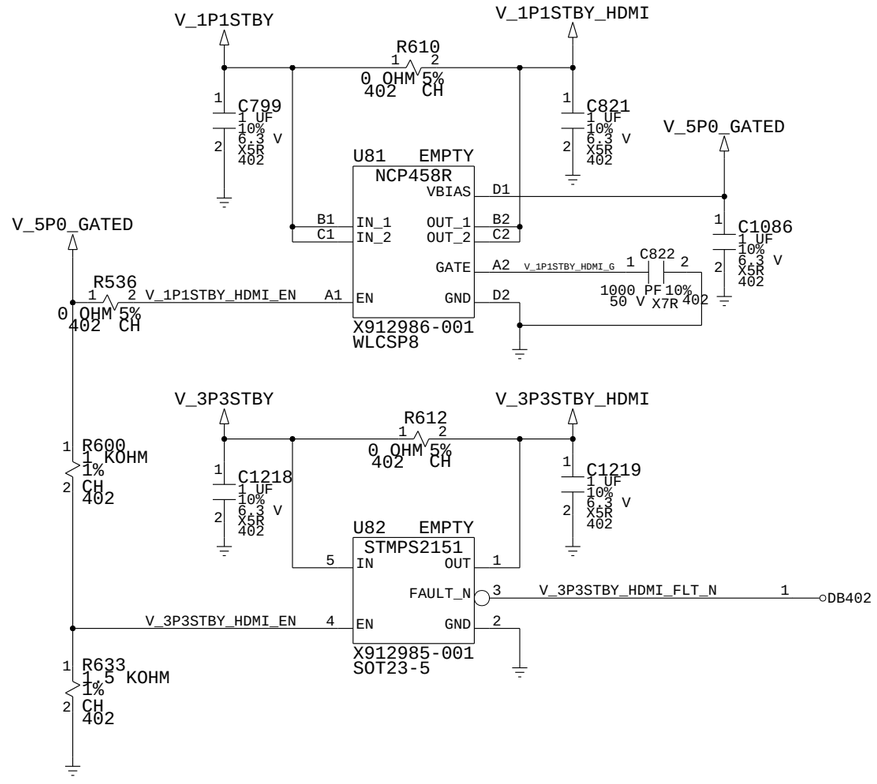
LANE_SWAP MUST BE ENABLED DUE TO INVERTED TMDS PIN-ORDER IMPLEMENTATION (0X09[7]=1)

HDMI 5V LOAD SWITCH: 5V, 250MA MAX TDC

DP PWR LOAD SWITCH: 3.3V, 500MA MAX TDC

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	48/82	48/82	G-R	0.991

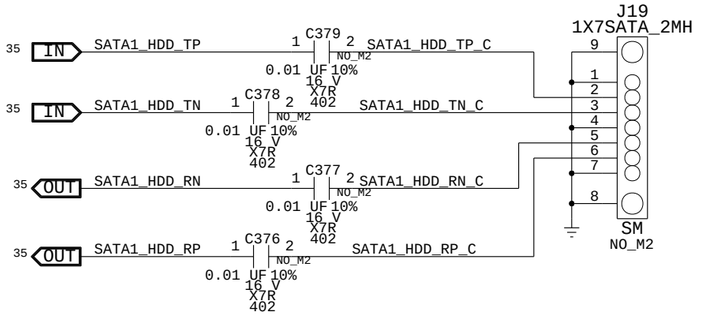
HDMI LOAD SWITCHES



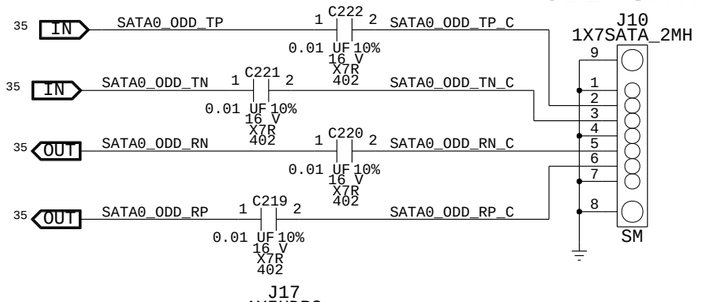
RE-DRIVER	U29	R610	R612	U81	U82
PG1.0	M1003966-001	EMPTY	EMPTY	STUFF	STUFF
PG1.1	M1003966-002	STUFF	STUFF	EMPTY	EMPTY

CONN: ODD & HDD

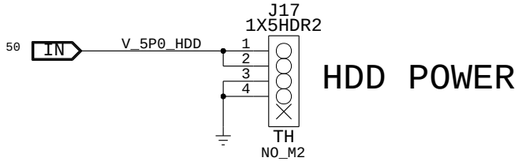
HDD SATA



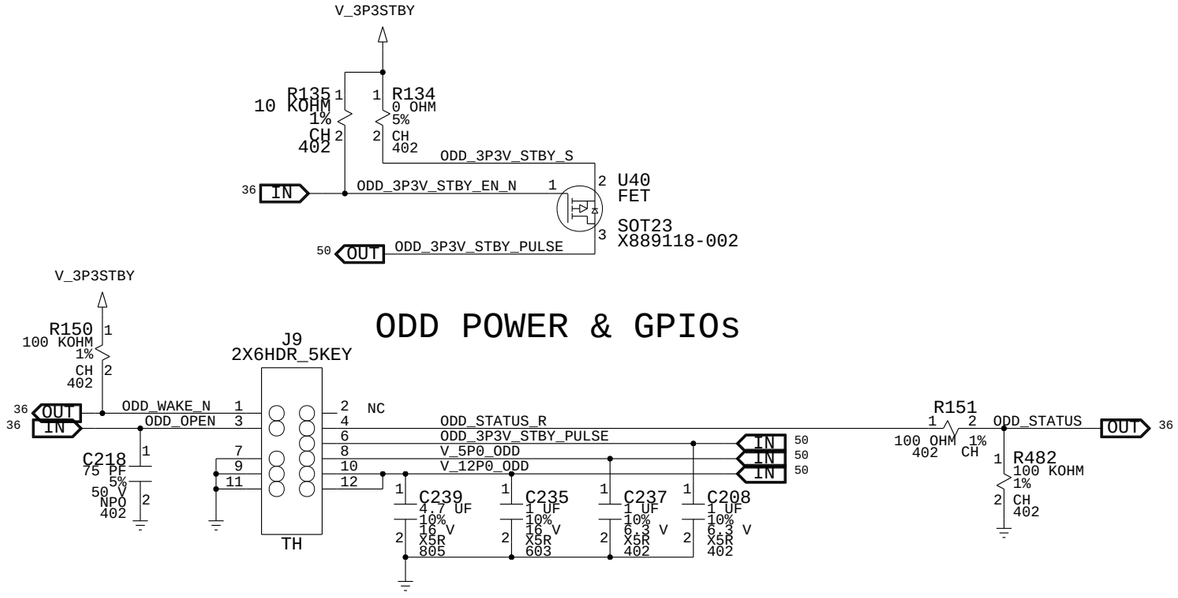
ODD SATA



HDD POWER

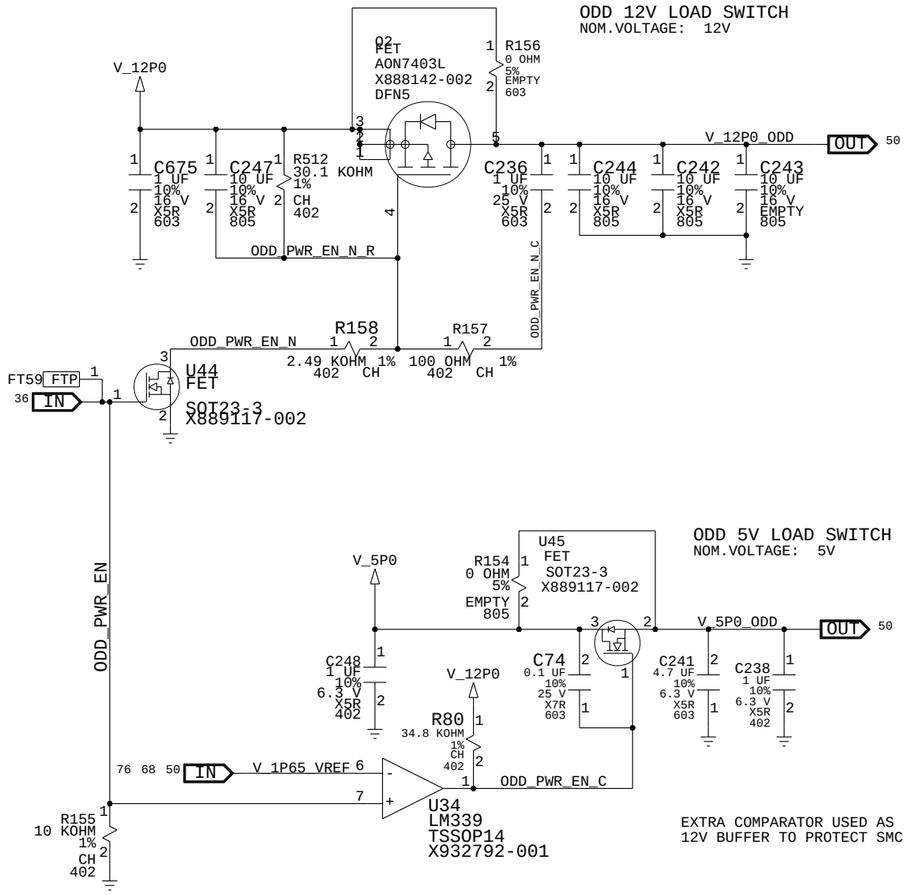


ODD POWER & GPIOs



ODD 12V LOAD SWITCH

NOM.VOLTAGE: 12V

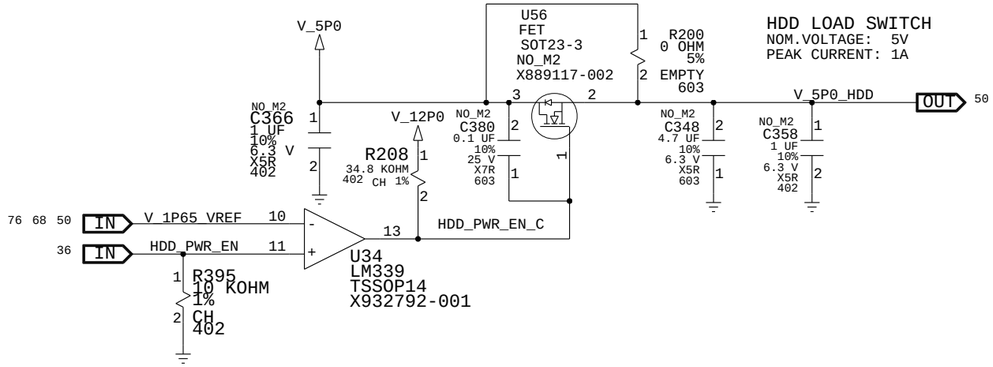


ODD 5V LOAD SWITCH

NOM.VOLTAGE: 5V

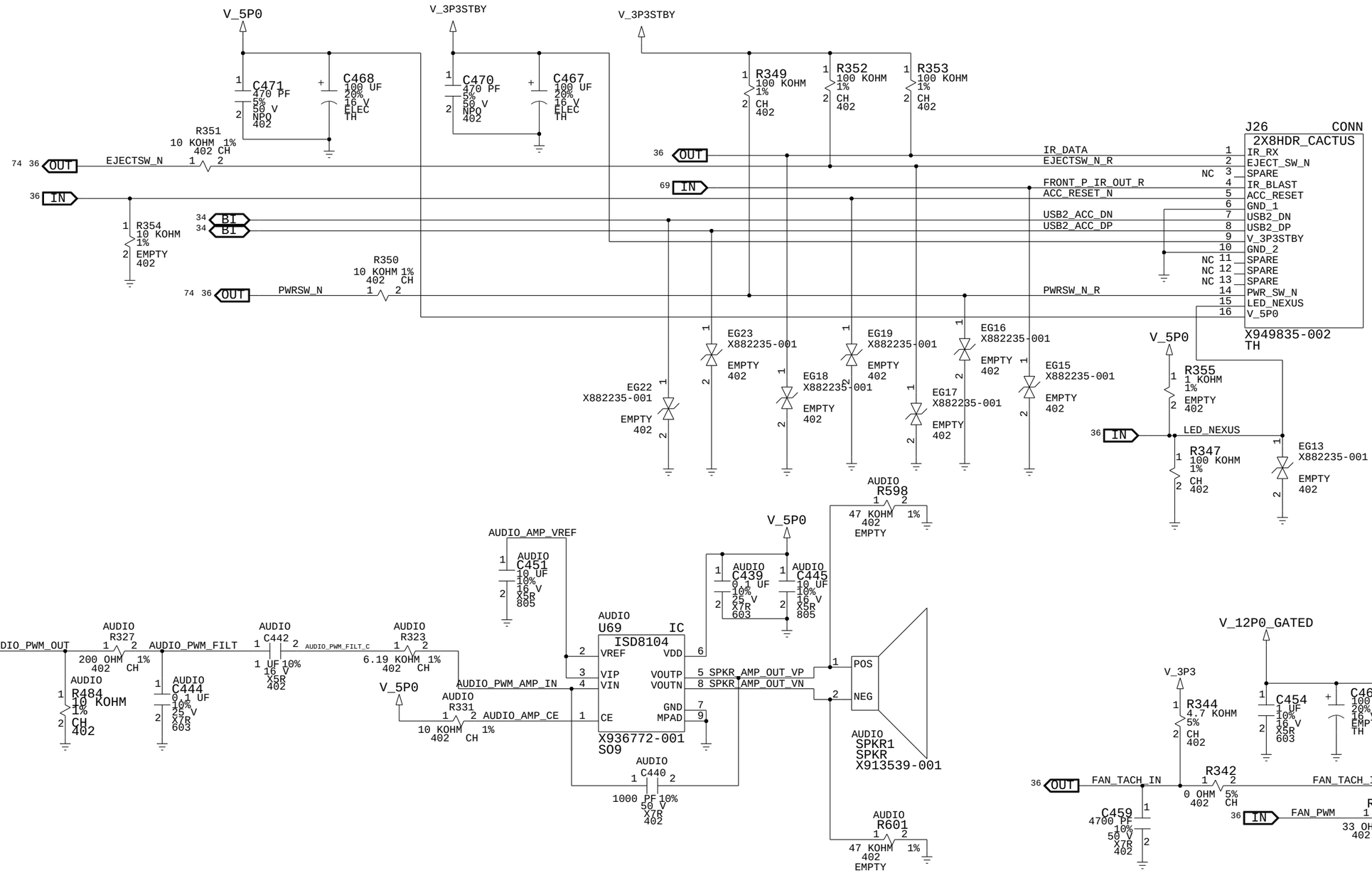
HDD LOAD SWITCH

NOM.VOLTAGE: 5V
PEAK CURRENT: 1A



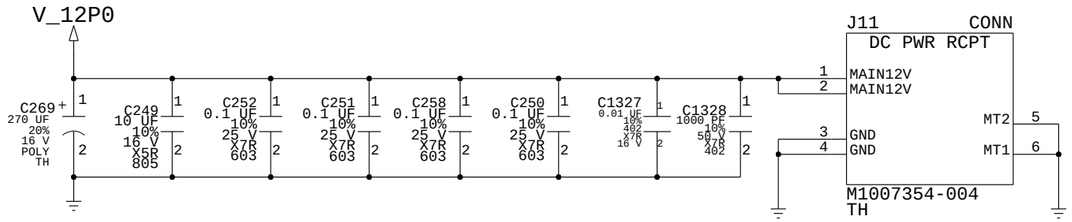
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	50/82	50/82	G-R	0.99

CONN: FRONT PANEL,FAN, AUDIO



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	51/82	51/82	G-R	0.991

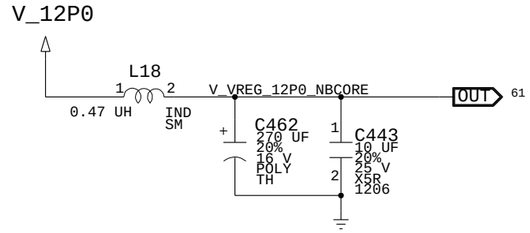
CONN: POWER



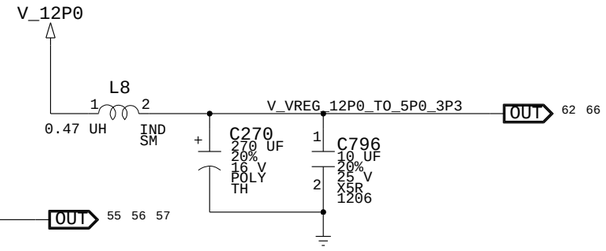
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	52/82	52/82	G-R	0.991

VREGS: INPUT AND OUTPUT FILTERS

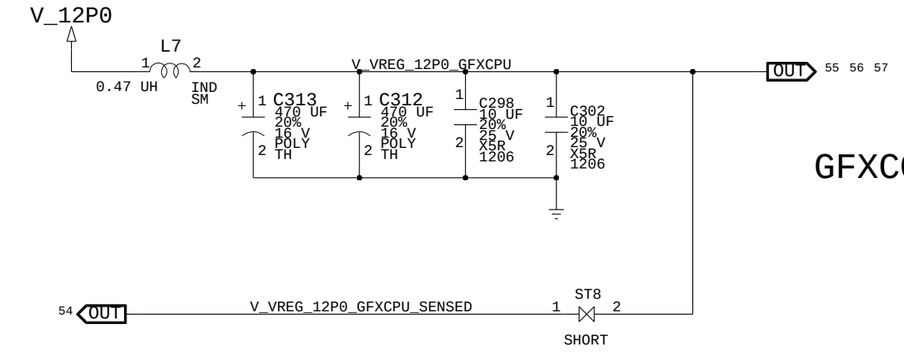
NBCORE INPUT FILTER



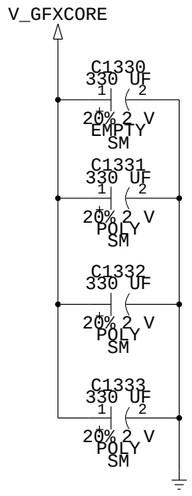
V_5P0 AND V_3P3 INPUT FILTER



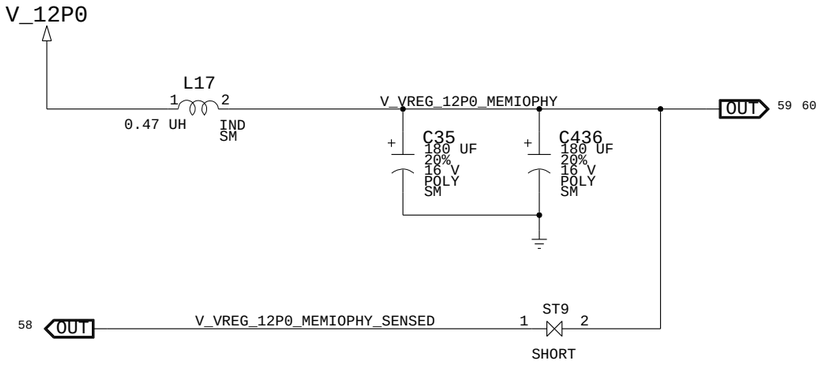
GFX/CPU INPUT FILTER



GFXCORE OUTPUT FILTER

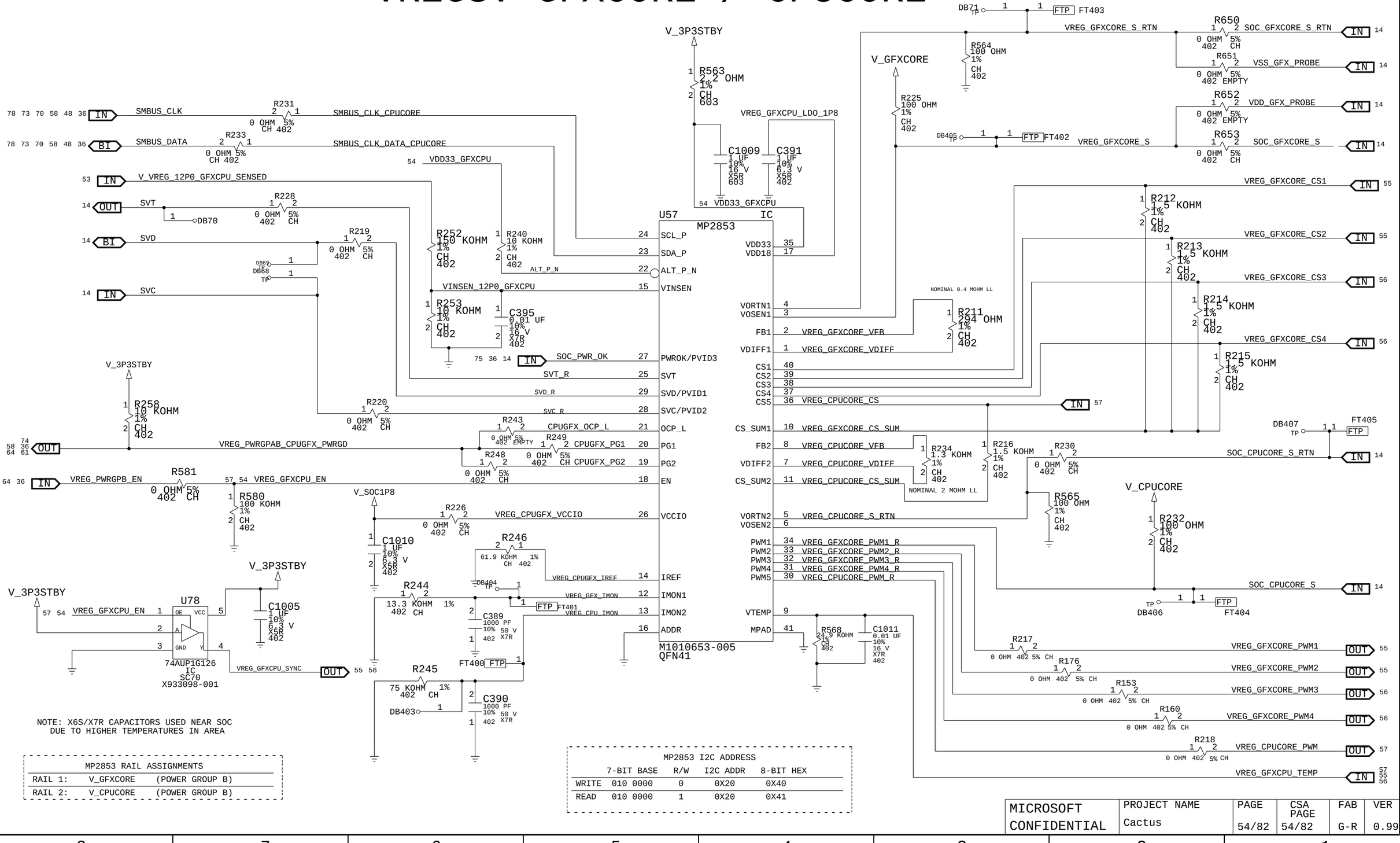


MEMIO/MEMPHY INPUT FILTER



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	53/82	53/82	G-R	0.991

VREGS: GFXCORE / CPUCORE



MP2853 RAIL ASSIGNMENTS

RAIL 1:	V_GFXCORE	(POWER GROUP B)
RAIL 2:	V_CPUCORE	(POWER GROUP B)

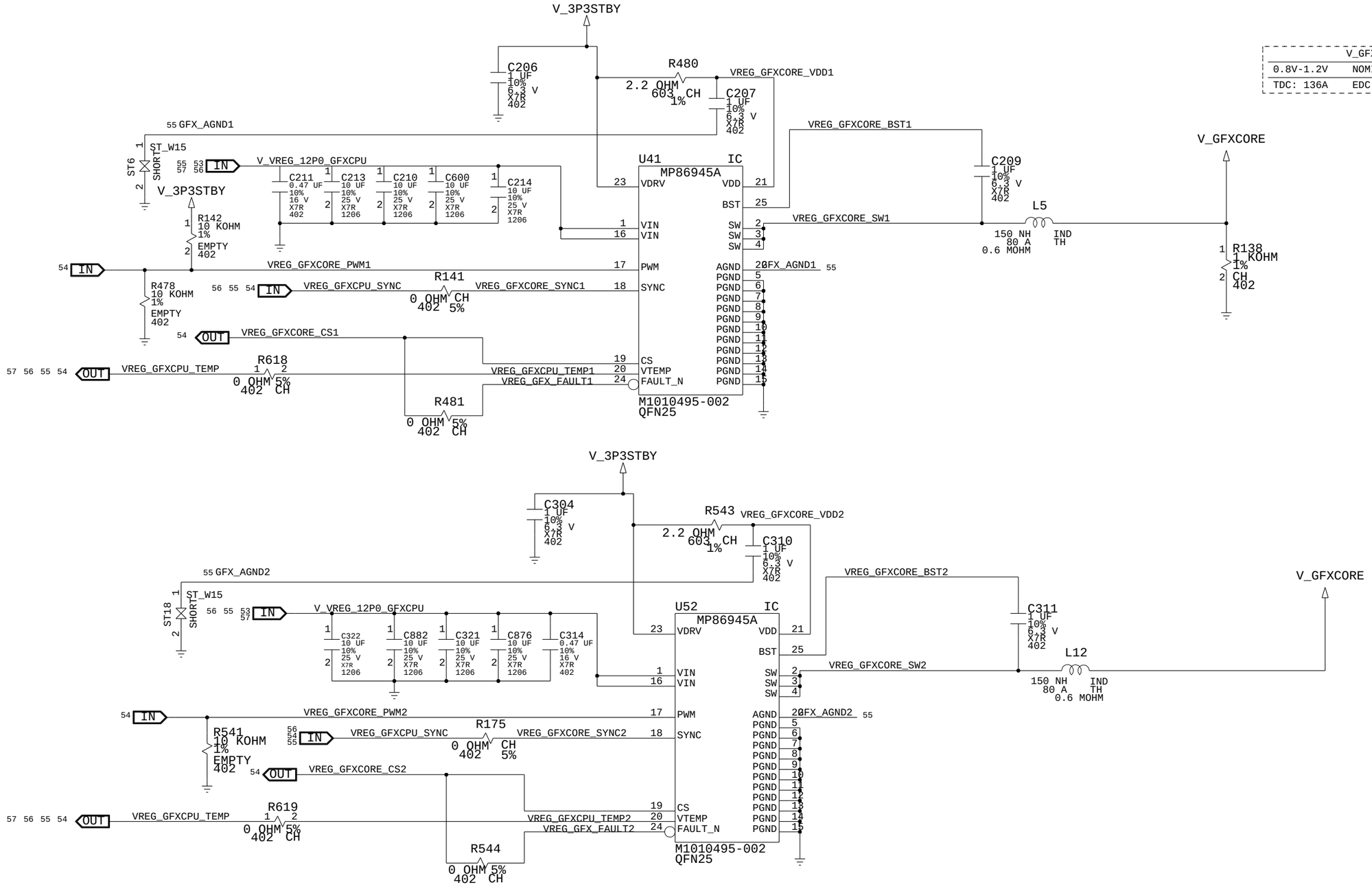
MP2853 I2C ADDRESS

	7-BIT BASE	R/W	I2C ADDR	8-BIT HEX
WRITE	010 0000	0	0X20	0X40
READ	010 0000	1	0X20	0X41

MICROSOFT CONFIDENTIAL	PROJECT NAME Cactus	PAGE 54/82	CSA PAGE 54/82	FAB G-R	VER 0.991

VREGS: GFXCORE OUTPUT PHASE 1 & 2

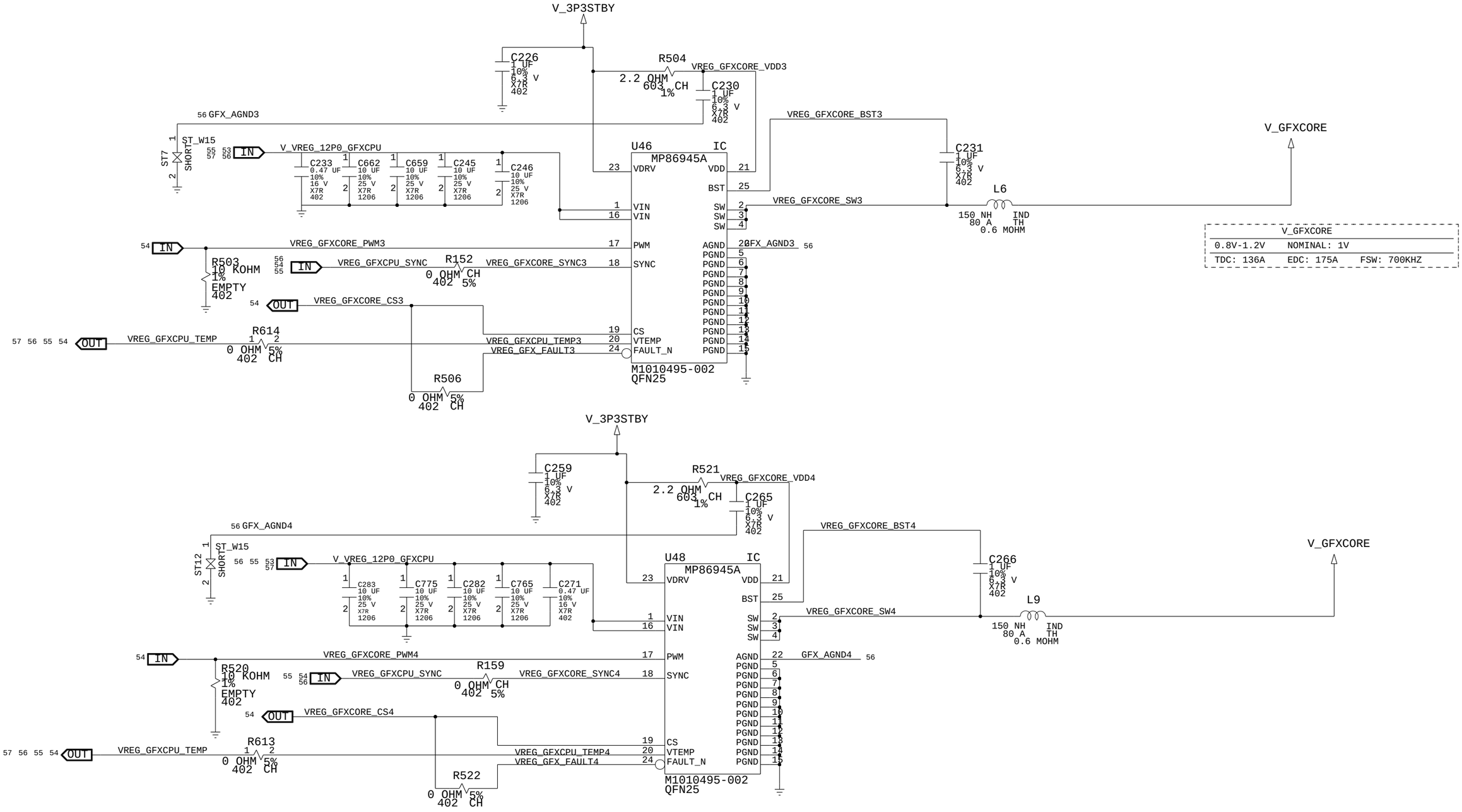
V_GFXCORE		
0.8V-1.2V	NOMINAL: 1V	
TDC: 136A	EDC: 175A	FSW: 700KHZ



NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	55/82	55/82	G-R	0.991

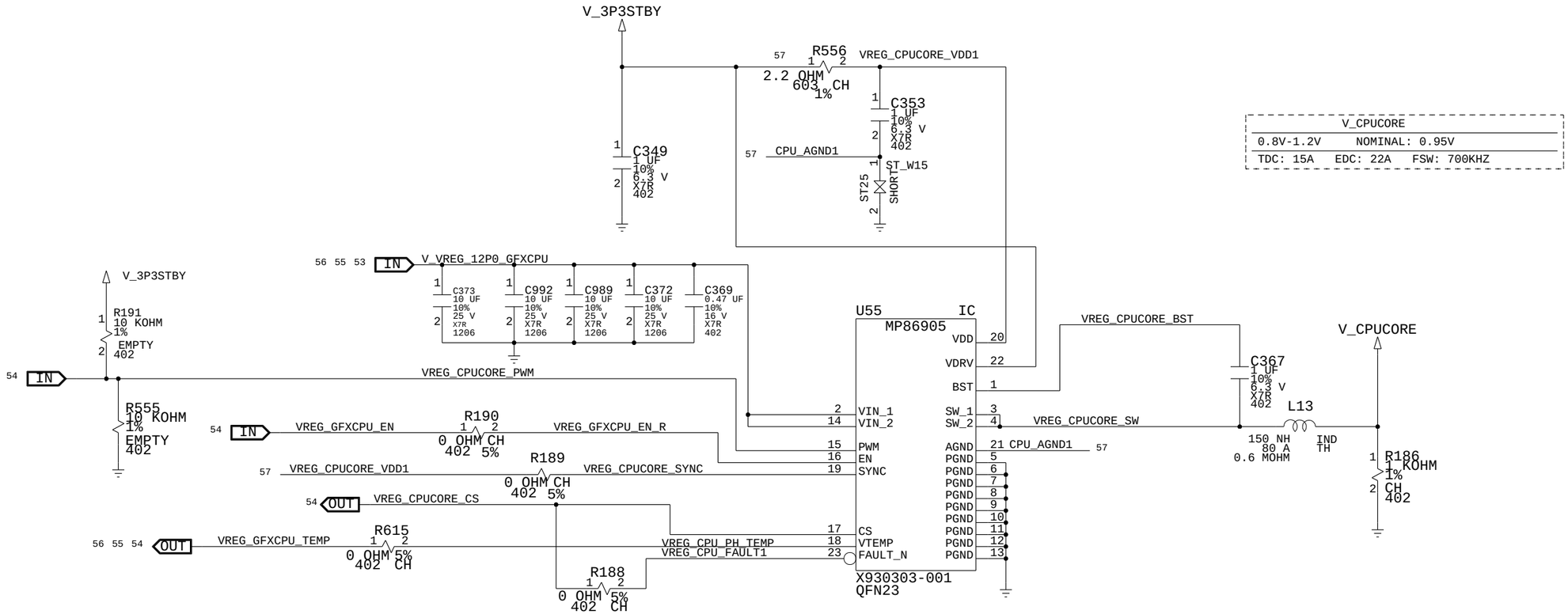
VREGS: GFXCORE OUTPUT PHASE 3 & 4



NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	56/82	56/82	G-R	0.991

VREGS: CPUCORE OUTPUT PHASE



NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	57/82	57/82	G-R	0.991

VREGS: MEMPHY / MEMIO

MEMIO OUTPUT VOLTAGE SELECT (PVID)
GPIO_1P8_3 = LOW: MEMIO VOUT = 1.5V
GPIO_1P8_3 = HIGH: MEMIO VOUT = 1.35V

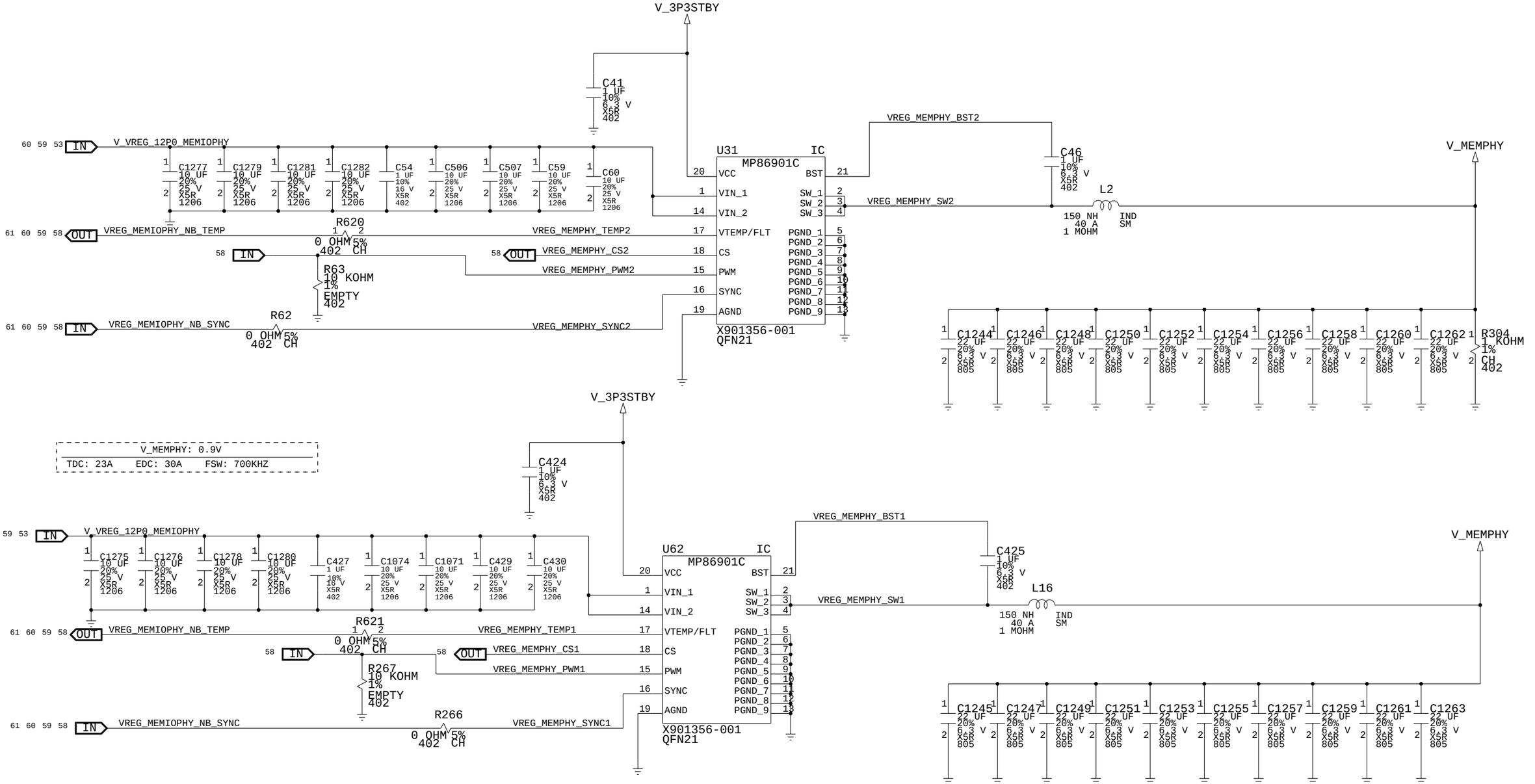
MP2949A RAIL ASSIGNMENTS		
RAIL 1:	V_MEMPHY	(POWER GROUP B)
RAIL 2:	V_MEMIO	(POWER GROUP A)
RAIL 3:	V_NBCORE	(POWER GROUP B)

MP2949A I2C ADDRESS				
	7-BIT BASE	R/W	I2C ADDR	8-BIT HEX
WRITE	010 0010	0	0X22	0X44
READ	010 0010	1	0X22	0X45

NOTE: SOC_MEMIO_S_RTN IS ACTUALLY SENSE RETURN FROM SOC FOR MEMPHY. NOT CHANGING NETNAME TO STAY CONSISTENT WITH SCB

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	58/82	58/82	G-R	0.991

VREGS: MEMPHY OUTPUT



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	59/82	59/82	G-R	0.991

VREGS: MEMIO OUTPUT

V_MEMIO				
1.35-1.5V	NOMINAL: 1.5V			
TDC(RETAIL):	20A	EDC(RETAIL):	23A	FSW: 700KHZ
TDC(XDK):	25A	EDC(XDK):	30A	FSW: 700KHZ

V_3P3STBY

C69 1 UF 10% 6.3 V X5R 402

60 59 53 IN V_VREG_12P0_MEMIOPHY

C1268 10 UF 20% 25 V X5R 1206
C1270 10 UF 20% 25 V X5R 1206
C1272 10 UF 20% 25 V X5R 1206
C1274 10 UF 20% 25 V X5R 1206
C61 10 UF 20% 25 V X5R 1206
C508 10 UF 20% 25 V X5R 1206
C66 10 UF 20% 25 V X5R 1206
C509 10 UF 20% 25 V X5R 1206
C75 1 UF 10% 16 V X5R 402

61 60 59 58 OUT VREG_MEMIOPHY_NB_TEMP

R617 0 OHM 5% 402 CH

VREG_MEMIO_TEMP1

58 IN

R72 10 KOHM 1% EMPTY 402

58 OUT VREG_MEMIO_CS1

VREG_MEMIO_PWM1

61 60 59 58 IN VREG_MEMIOPHY_NB_SYNC

R73 0 OHM 5% 402 CH

VREG_MEMIO_SYNC1

U32 IC MP86901C X901356-001 QFN21

20	VCC	BST	21
1	VIN_1	SW_1	2
14	VIN_2	SW_2	3
		SW_3	4
17	VTEMP/FLT	PGND_1	5
18	CS	PGND_2	6
		PGND_3	7
		PGND_4	8
15	PWM	PGND_5	9
		PGND_6	10
16	SYNC	PGND_7	11
		PGND_8	12
19	AGND	PGND_9	13

VREG_MEMIO_BST1

C77 1 UF 10% 6.3 V X5R 402

VREG_MEMIO_SW1

L3 150 NH 40 A 1 MOHM IND SM

V_MEMIO

C1224 C1226 C1228 C1230 C1232 C1234 C1236 C1238 C1240 C1242 22 UF 20% 6.3 V X5R 805

R79 1 KOHM 1% CH 402

V_3P3STBY

C423 1 UF 10% 6.3 V X5R 402

60 59 53 IN V_VREG_12P0_MEMIOPHY

C1267 10 UF 20% 25 V X5R 1206
C1269 10 UF 20% 25 V X5R 1206
C1271 10 UF 20% 25 V X5R 1206
C1273 10 UF 20% 25 V X5R 1206
C428 10 UF 20% 25 V X5R 1206
C426 10 UF 20% 25 V X5R 1206
C1069 10 UF 20% 25 V X5R 1206
C1072 10 UF 20% 25 V X5R 1206
C421 1 UF 10% 16 V X5R 402

61 60 59 58 OUT VREG_MEMIOPHY_NB_TEMP

R616 0 OHM 5% 402 CH

VREG_MEMIO_TEMP2

58 IN

R281 10 KOHM 1% EMPTY 402

58 OUT VREG_MEMIO_CS2

VREG_MEMIO_PWM2

61 60 59 58 IN VREG_MEMIOPHY_NB_SYNC

R270 0 OHM 5% 402 CH

VREG_MEMIO_SYNC2

U60 IC MP86901C X901356-001 QFN21

20	VCC	BST	21
1	VIN_1	SW_1	2
14	VIN_2	SW_2	3
		SW_3	4
17	VTEMP/FLT	PGND_1	5
18	CS	PGND_2	6
		PGND_3	7
		PGND_4	8
15	PWM	PGND_5	9
		PGND_6	10
16	SYNC	PGND_7	11
		PGND_8	12
19	AGND	PGND_9	13

VREG_MEMIO_BST2

C422 1 UF 10% 6.3 V X5R 402

VREG_MEMIO_SW2

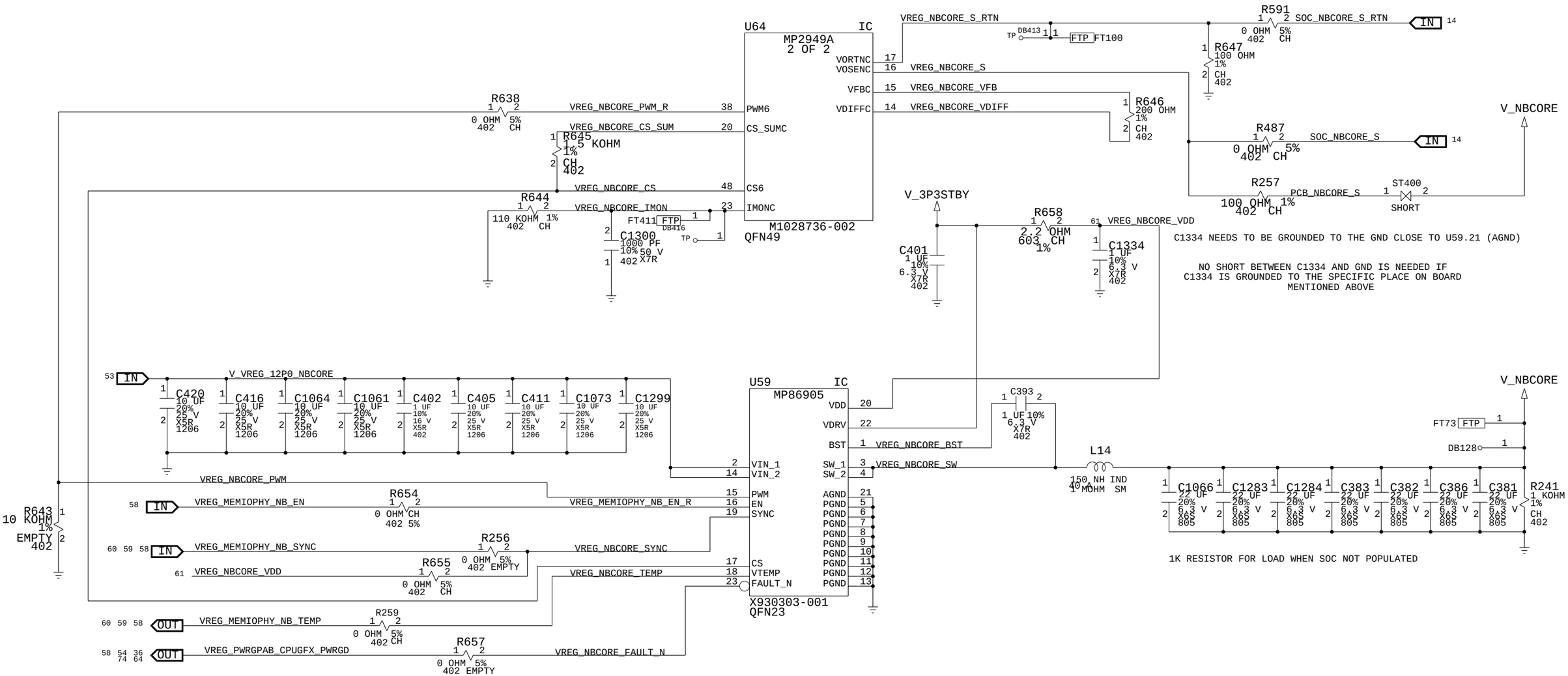
L15 150 NH 40 A 1 MOHM IND SM

V_MEMIO

C1225 C1227 C1229 C1231 C1233 C1235 C1237 C1239 C1241 C1243 22 UF 20% 6.3 V X5R 805

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	60/82	60/82	G-R	0.99

VREGS: NBCORE

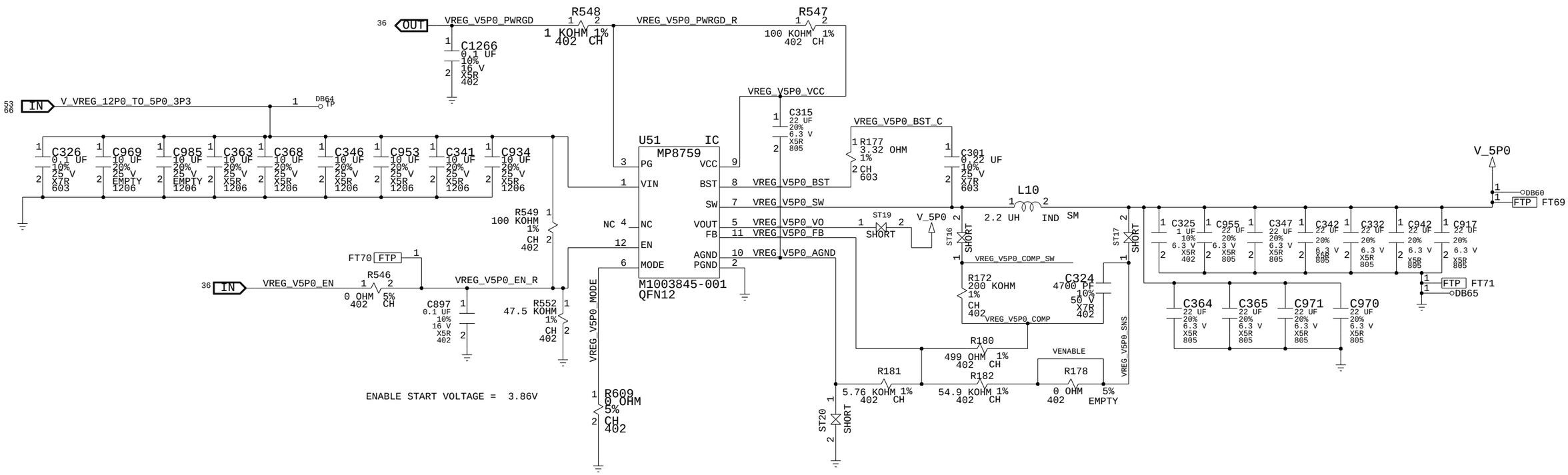


V_NBCORE		
0.8V-1.2V	NOMINAL: 0.95V	
TDC: 16A	EDC: 25A	FSW: 700KHZ

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	61/82	61/82	G-R	0.991

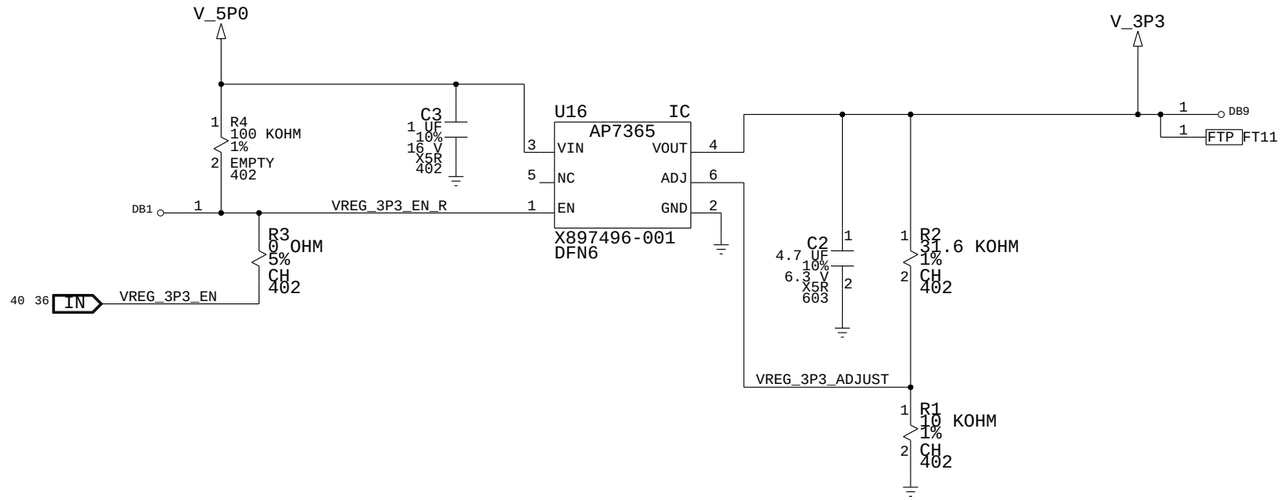
VREGS: V5P0

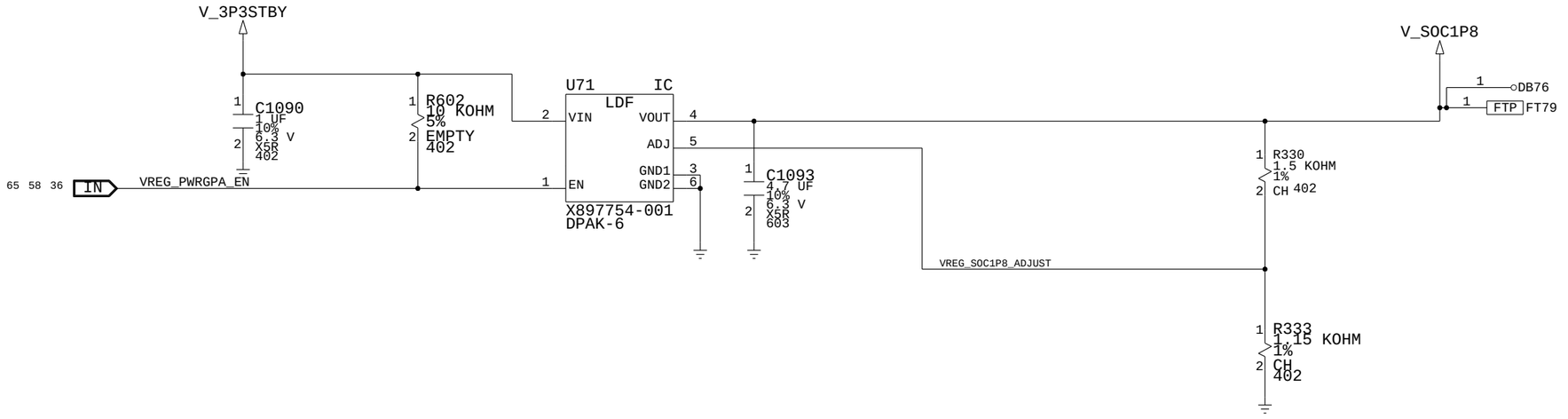
V_5P0
NOM. VOLTAGE: 5.1



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	62/82	62/82	G-R	0.99

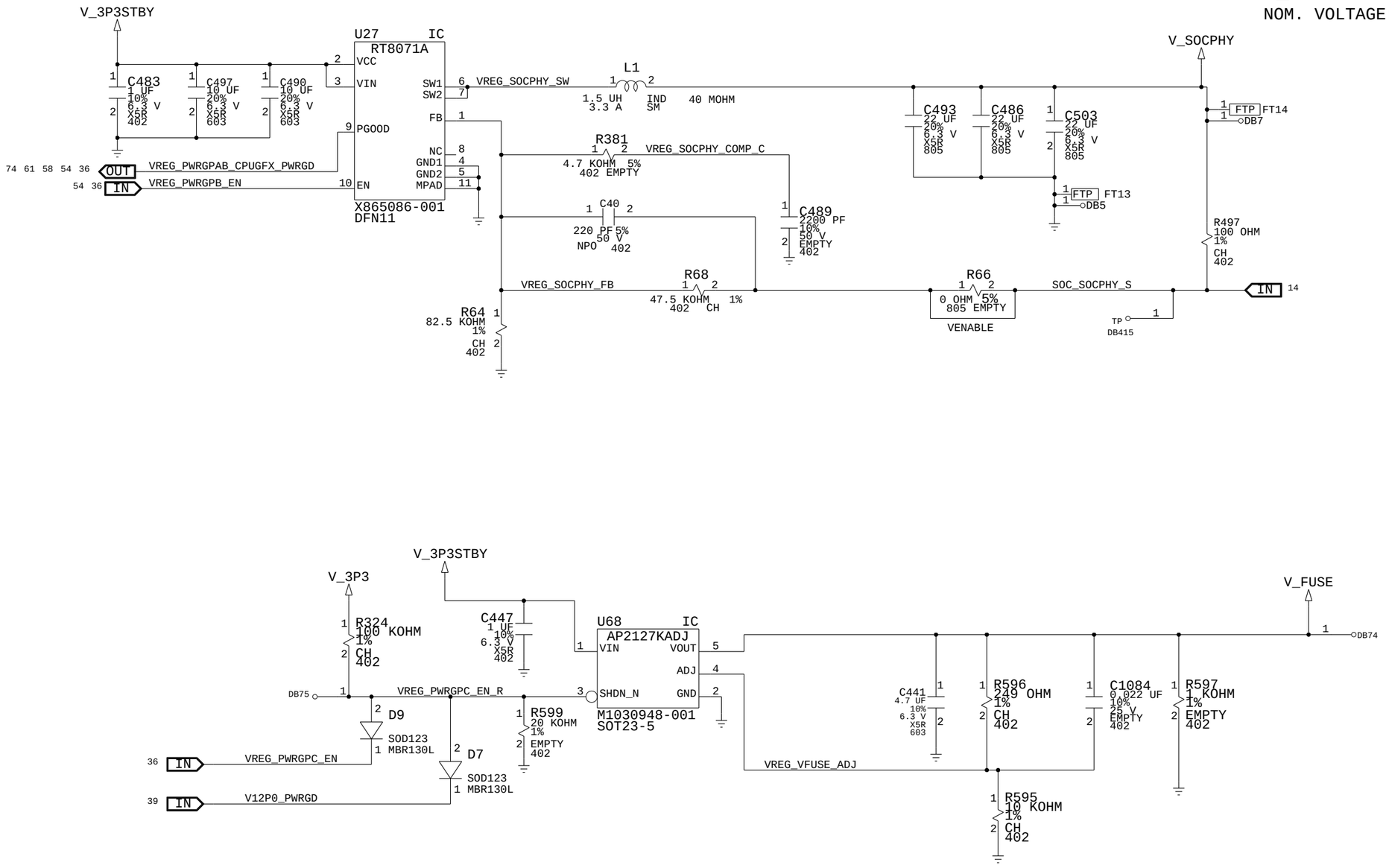
VREGS: V3P3, VSOC1P8





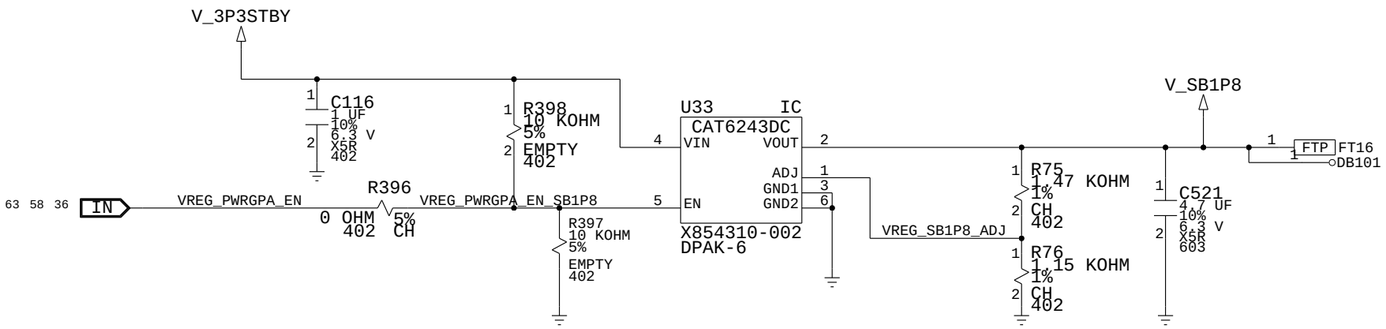
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	63/82	63/82	G-R	0.991

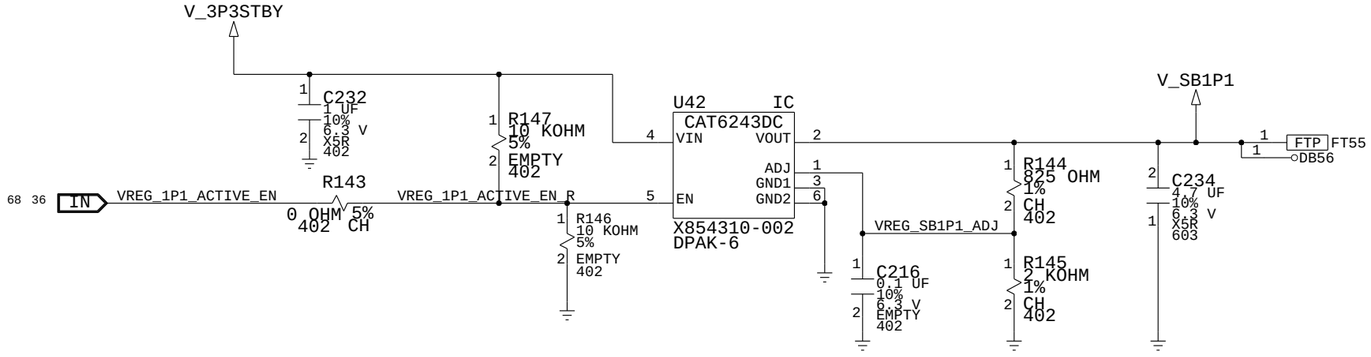
VREGS: VSOCPHY/VFUSE



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	64/82	64/82	G-R	0.991

VREGS: V_SB1P8, V_SB1P1

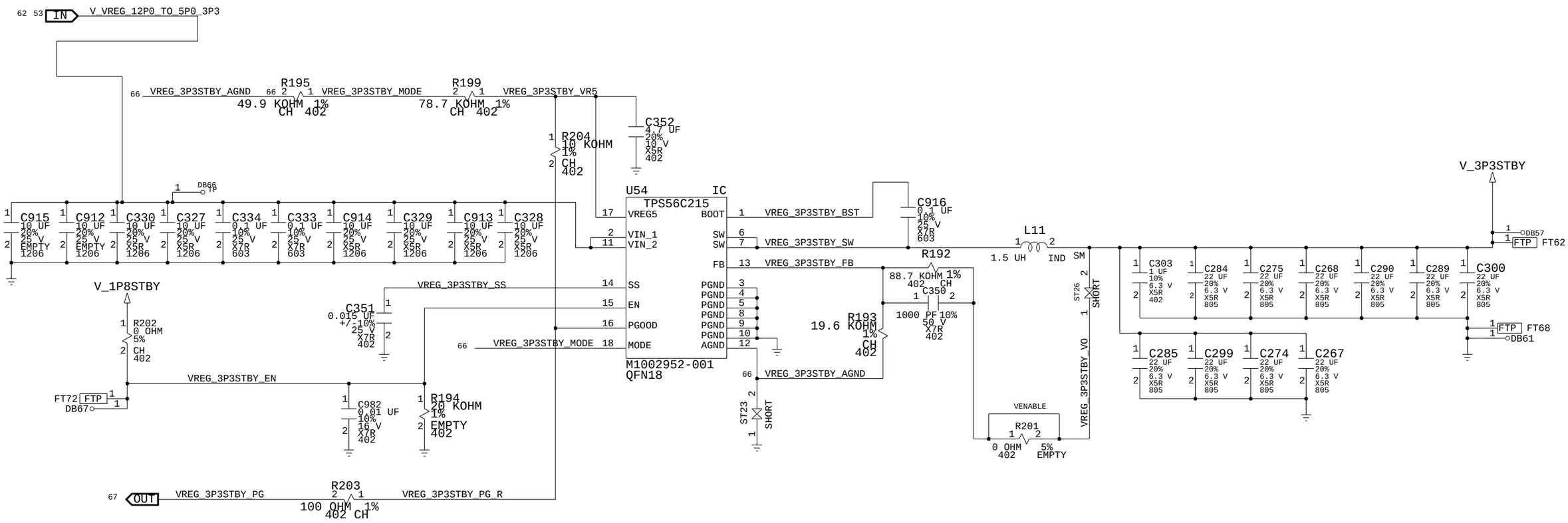




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	65/82	65/82	G-R	0.991

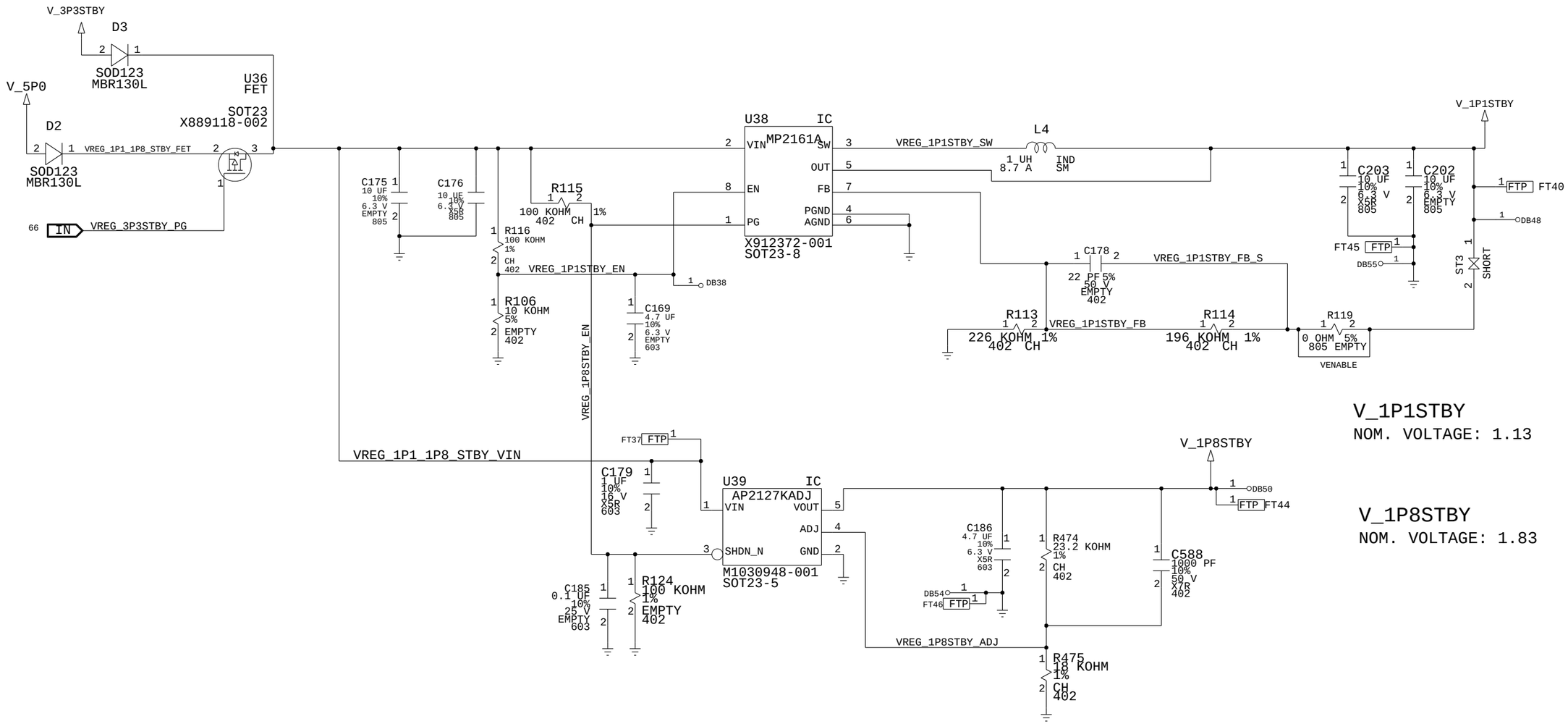
VREGS: V3P3 STANDBY

V_3P3STBY
NOM. VOLTAGE: 3.32



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	66/82	66/82	G-R	0.991

VREGS: V1P1 STANDBY, V1P8 STANDBY



V_1P1STBY

NOM. VOLTAGE: 1.13

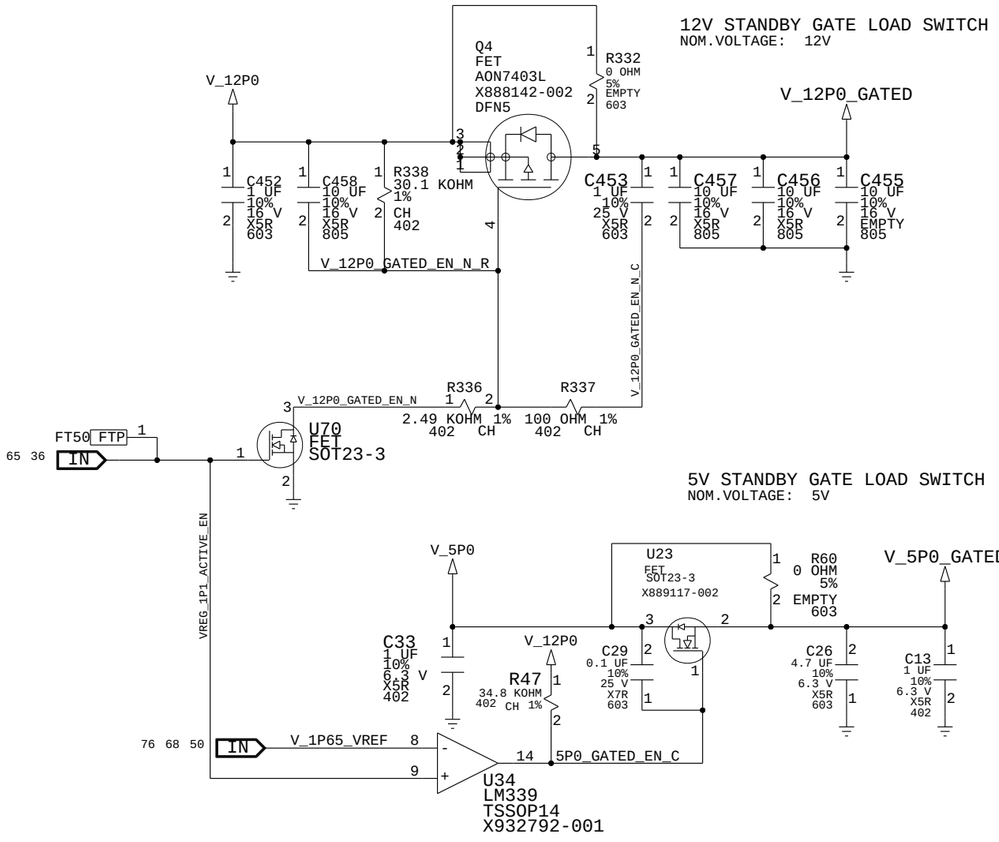
V_1P8STBY

NOM. VOLTAGE: 1.83

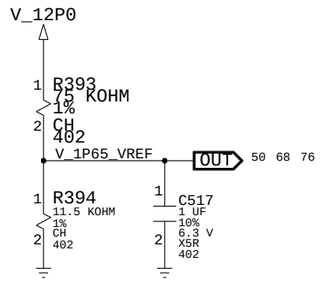
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	67/82	67/82	G-R	0.991

STANDBY GATES

12V STANDBY GATE LOAD SWITCH
NOM.VOLTAGE: 12V

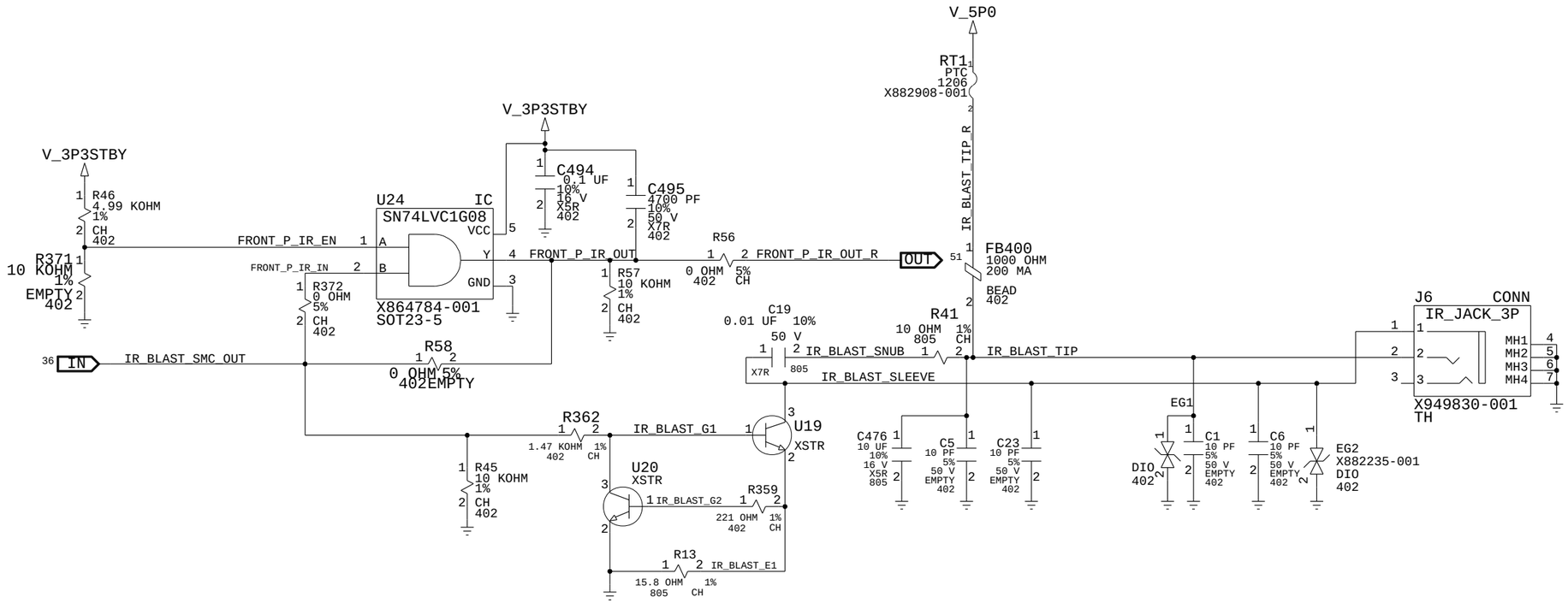


5V STANDBY GATE LOAD SWITCH
NOM.VOLTAGE: 5V



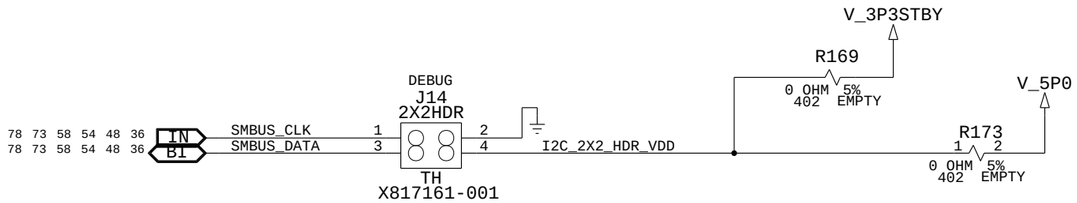
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	68/82	68/82	G-R	0.991

IR BLASTER



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	69/82	69/82	G-R	0.99

I2C



FOR AARDVARK, CAN CHOOSE 3.3V OR 5V VDD

MARGIN: SOCPHY,SOC1P8

BLANK

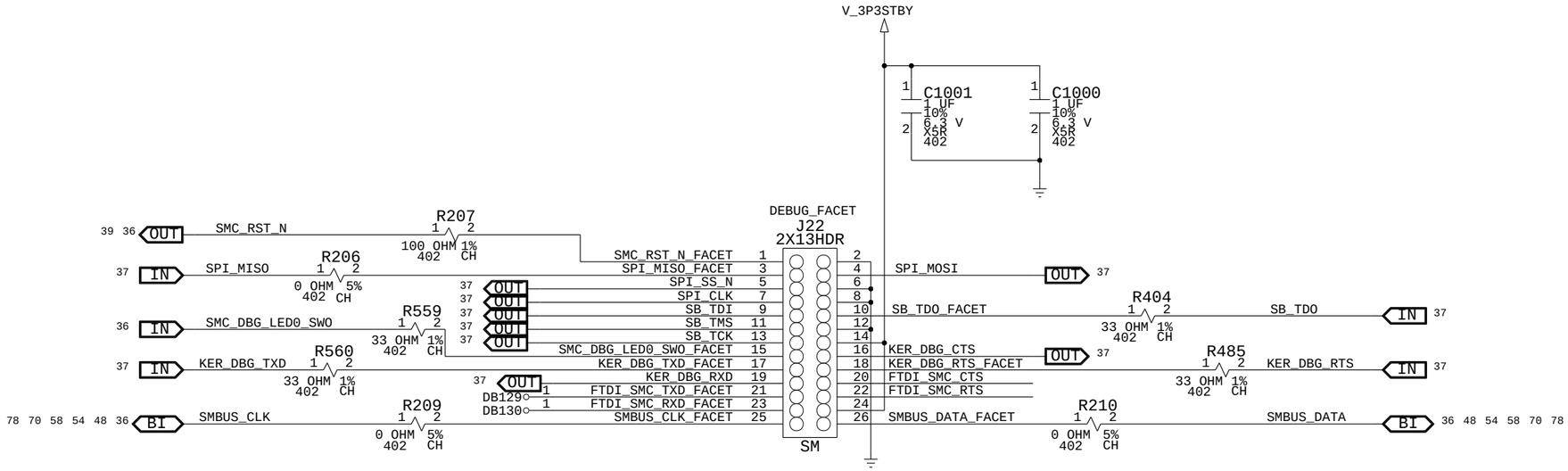
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	71/82	71/82	G-R	0.991

MONITOR: VSOC1P8,VSOCPHY,V12P0

BLANK

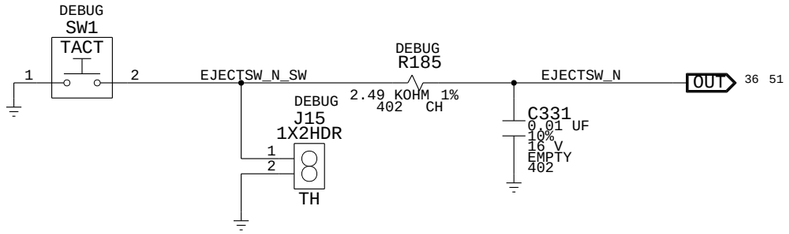
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	72/82	72/82	G-R	0.991

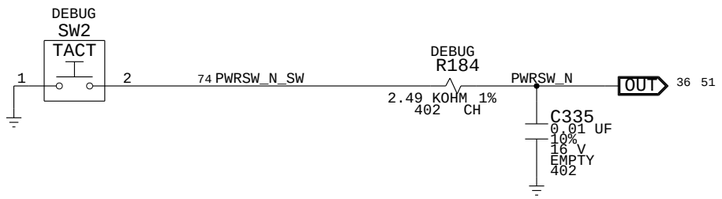
CONN: FACET BOARD

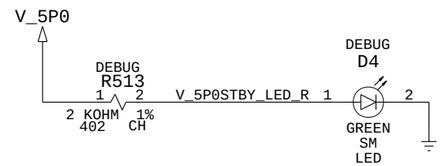


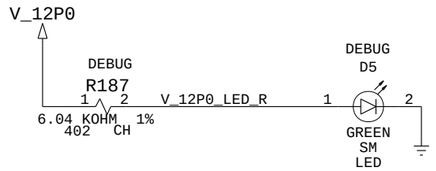
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	73/82	73/82	G-R	0.991

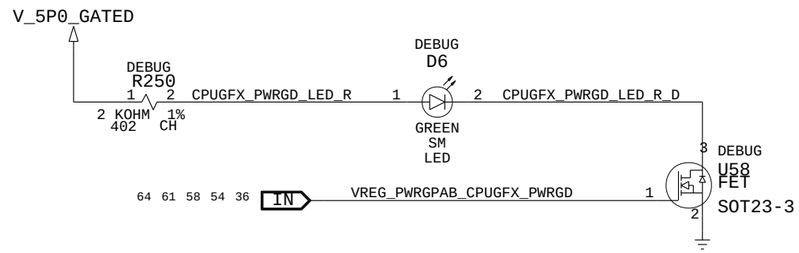
CONN: SWITCHES

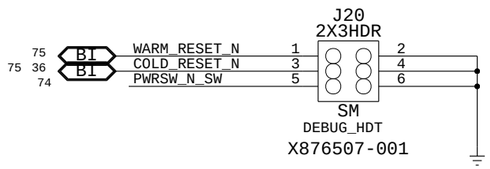






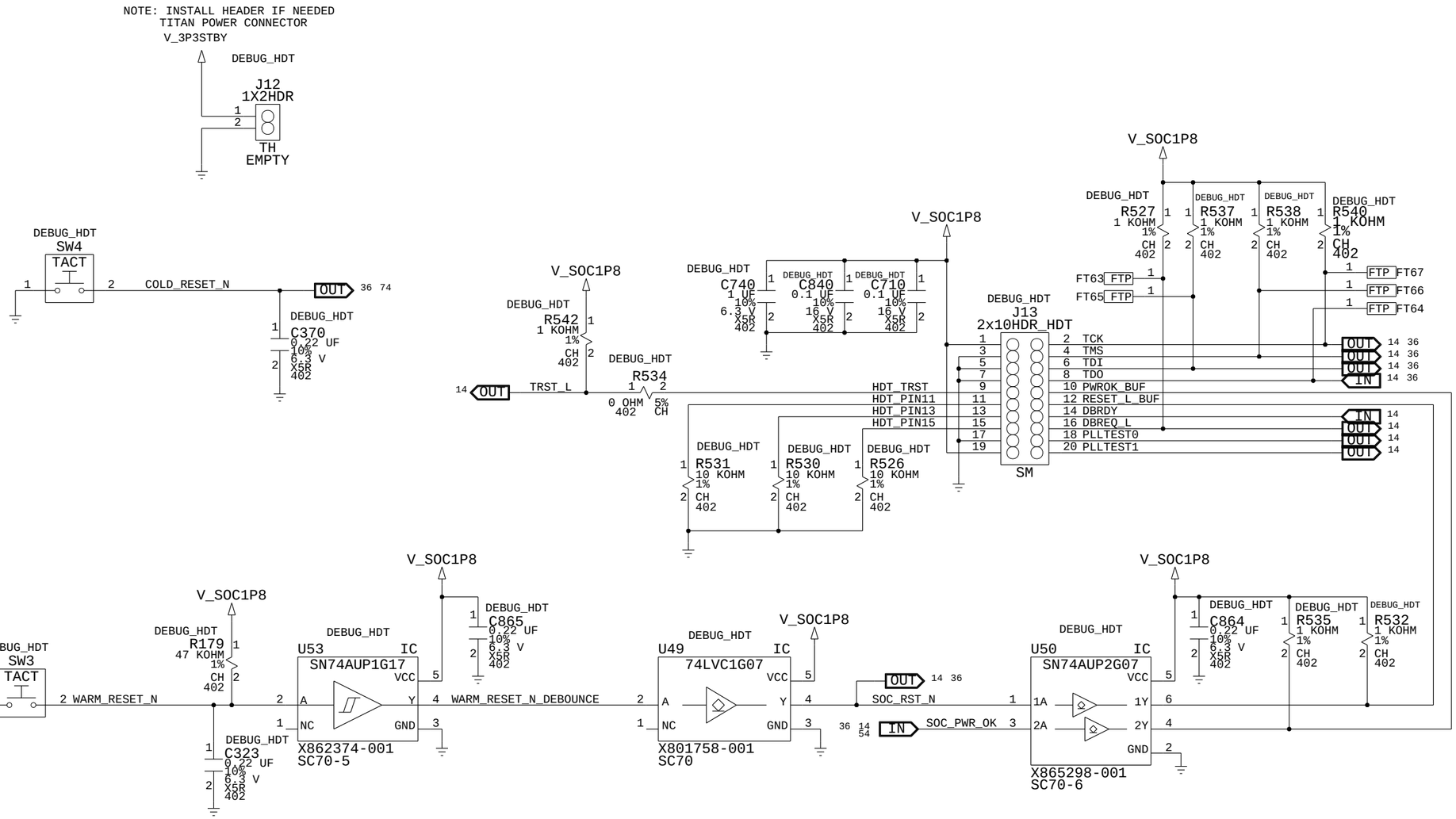






MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	74/82	74/82	G-R	0.991

CONN: HDT



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	75/82	75/82	G-R	0.991

CONN: M.2

MTG5
SPACER_1P
M1008483-001
TH
M2_ONLY
SSD MOUNTING HARDWARE

SSD LOAD SWITCH
NOM.VOLTAGE: 3.3V
PEAK CURRENT: 2.5A

NOTE: R328 AND D8 ARE DEBUG COMPONENTS AND NEED TO BE REMOVED FROM RETAIL CONFIGS

R325 0 OHM 5% 805 EMPTY
Q3 NTTFS4C50N X889324-001 DFN5 FET
V_3P3STBY
V_12P0
V_3P3_M2
M2_ONLY J32 PCIE_M2_M_RCPT_67P_2MH
M1007401-001 SM

C434 1 UF 10% 6.3 V X5R 402
C437 0.1 UF 10% 25 V X7R 603
C519 0.1 UF 10% 25 V X7R 603
C450 4.7 UF 10% 6.3 V X5R 603
C448 1 UF 10% 6.3 V X5R 402
C1075 C1078 1 UF 10% 6.3 V X5R 402
C449 1 UF 10% 6.3 V X5R 402
C446 22 UF 20% 6.3 V X5R 805

R637 10 KOHM 1% CH 402
R328 511 OHM 1% 402 CH
D8 GREEN SM LED
M2_LED
M2_LED_R

R78 34.8 KOHM 402 CH 1%
U34 LM339 TSSOP14 X932792-001
68 50 IN V_1P65_VREF
V_3P3
M2_ENABLE_C

R634 10 KOHM 1% EMPTY 402
M2_PWR_EN_R
36 42 IN M2_PWR_EN
R635 0 OHM 5% 402 CH M2_ONLY
R636 10 KOHM 1% CH 402

R283 10 KOHM 1% CH 402 M2_ONLY
R293 10 KOHM 1% CH 402 M2_ONLY
M2_PCIE_RESET_N
77 OUT M2_CLKREQ_N
REF CLK CONTROLLED BY SSD TO SUPPORT POWER MODE EXPERIMENTS

U63 FET SOT23-3 M2_ONLY
RST_G_C
U66 FET SOT23-3 M2_ONLY
42 36 IN PCIE_RST_N
R318 100 OHM 1% 402 CH M2_ONLY
C433 0.022 UF 10% 50 V X7R 402 M2_ONLY
R307 100 OHM 1% 402 CH M2_ONLY
RST_G
RST_G_R

THE SSD HAS AN INTERNAL PULL-UP ON ITS PCIE RESET INPUT.
ISOLATION OF SIGNAL PCIE_RST_N IS NEEDED TO ISOLATE
SOUTHBRIDGE OUTPUT FROM SSD PULLUP

PEX_L3_M2_SOC_TN
PEX_L3_M2_SOC_TP
PEX_L3_SOC_M2_TN_C
PEX_L3_SOC_M2_TP_C
PEX_L2_M2_SOC_TN
PEX_L2_M2_SOC_TP
PEX_L2_SOC_M2_TN_C
PEX_L2_SOC_M2_TP_C
PEX_L1_M2_SOC_TN
PEX_L1_M2_SOC_TP
PEX_L1_SOC_M2_TN_C
PEX_L1_SOC_M2_TP_C
PEX_L0_M2_SOC_TN
PEX_L0_M2_SOC_TP
PEX_L0_SOC_M2_TN_C
PEX_L0_SOC_M2_TP_C
M2_PEX_SS_100M_CLKN
M2_PEX_SS_100M_CLKP

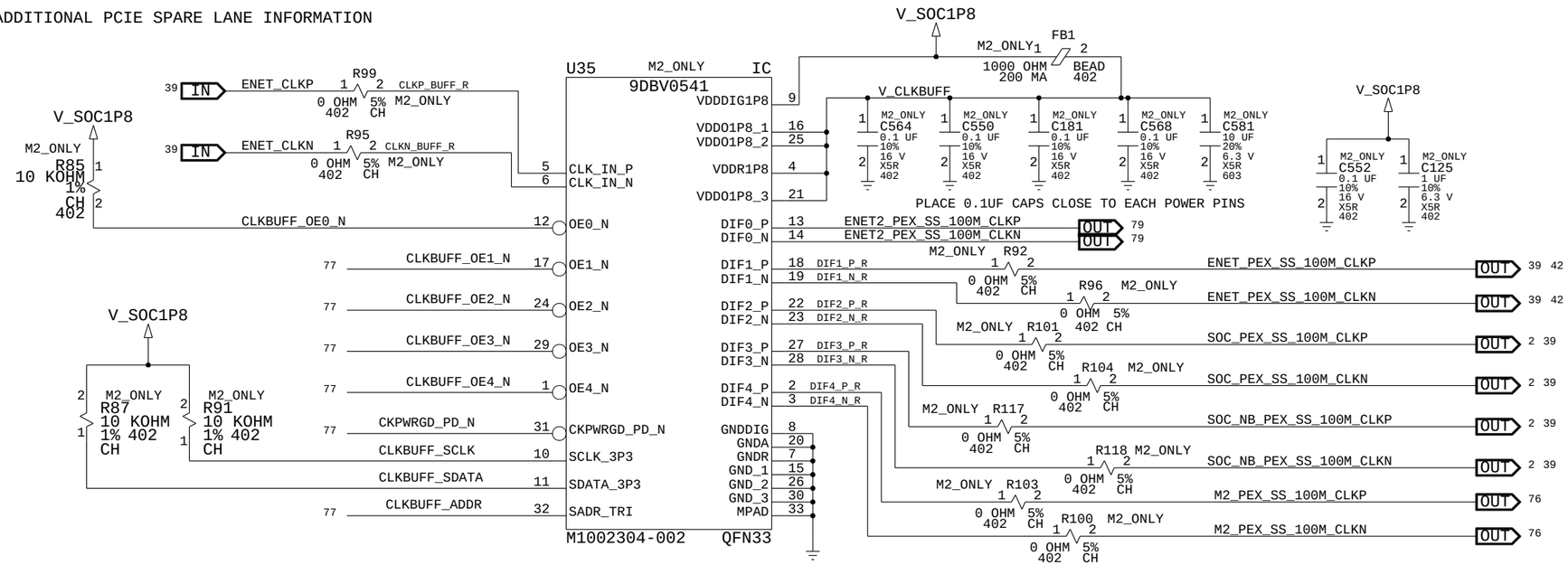
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	76/82	76/82	G-R	0.991

CLOCK BUFFER

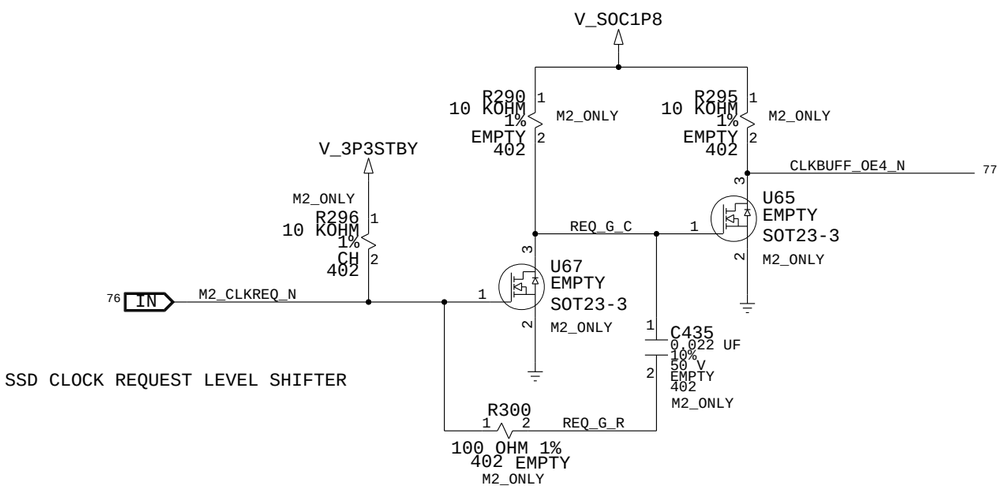
NOTES:

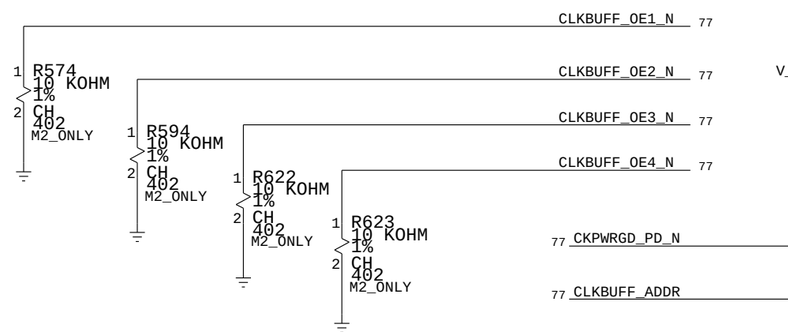
1.TO ENABLE ENET2 CLOCK ON J28 HEADER, UNSTUFF R85. U35 HAS INTERNAL PULL DOWN.

2.SEE PAGES 2 AND 79 FOR ADDITIONAL PCIE SPARE LANE INFORMATION



TO ADDRESS LONG TERM RELIABILITY CONCERNS
PERMANENT PULL UP/DOWN RESISTORS HAVE BEEN ADDED
EVEN THOUGH THIS PART HAS ITS OWN INTERNAL 100K EQUIVALENTS

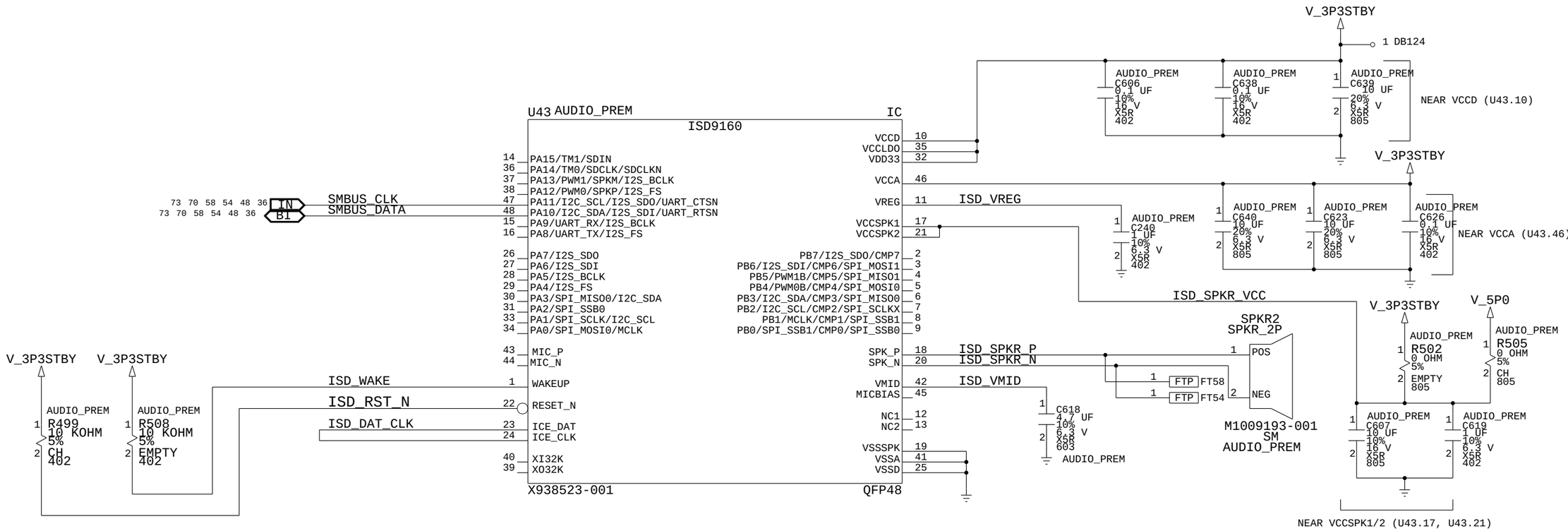




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Cactus	77/82	77/82	G-R	0.99

PREMIUM SPEAKER (SE/LE)

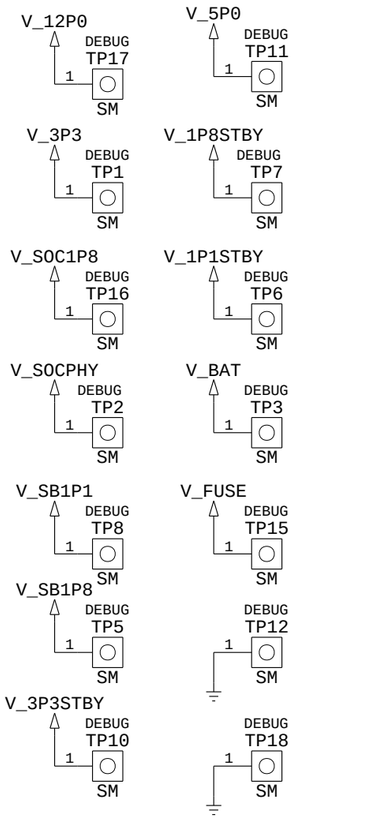
PREMIUM/SE/LE SKU ONLY

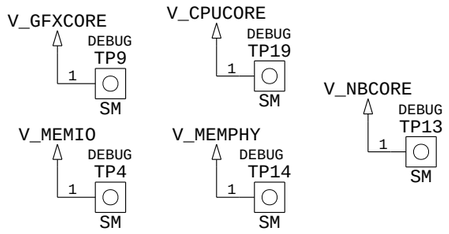


ISD9160FIMS05 - REMOVED CAP TOUCH FUNCTIONALITY

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	VER
	Cactus	78/82	78/82	0.991

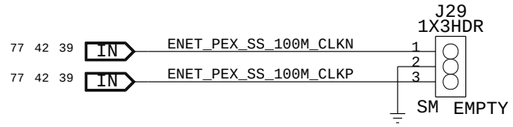
DEBUG: VR HEADERS, TEST POINTS, CONNECTORS

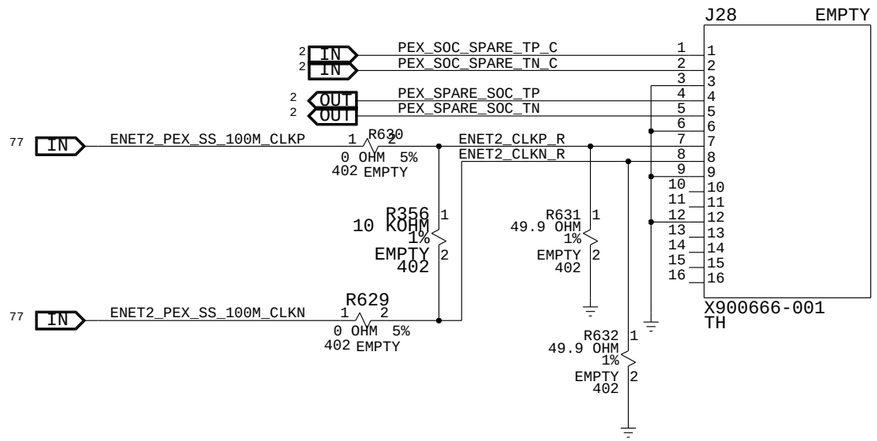




NOTE: THESE TEST POINTS ARE NOT TO BE USED FOR VOLTAGE REGULATOR QUALIFICATION TEST POINTS

PCIE CONNECTORS



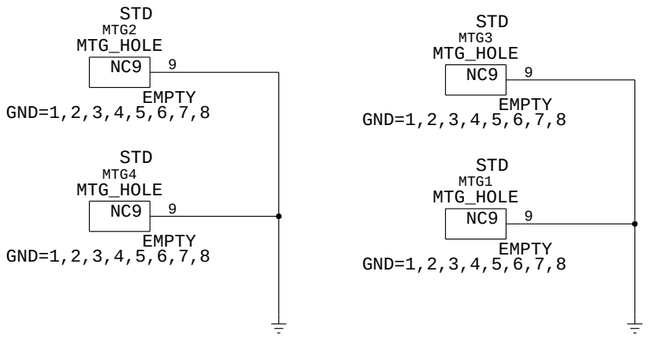


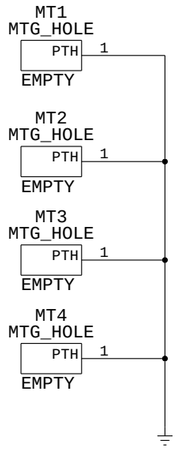
NOTES: TO ENABLE 100 MHZ REF CLOCK ON HEADER J28:

1. WHEN CLOCK BUFFER U35 IS INSTALLED: POPULATE R629 AND R630.
2. WITHOUT CLOCK BUFFER INSTALLED:
   - A. POPULATE R631 AND R632.
   - B. WIRE JUMPER ETHERNET 100 MHZ CLOCK FROM HEADER J29.1 AND J29.3 TO J28.8 AND J28.7 RESPECTIVELY.
3. SEE PAGES 2 AND 77 FOR ADDITIONAL PCIE SPARE LANE INFORMATION.

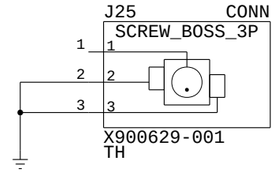
LABELS AND MOUNTING

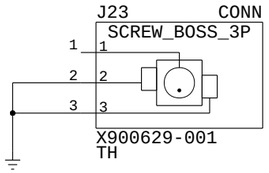
HEAT SINK MOUNTING HOLES



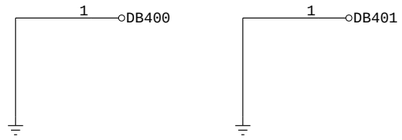


SCREW BOSS



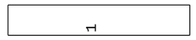


GND PADS FOR HEATSINK ALIGNMENT PINS



INTELLIGENT SERIAL NUMBER TARGET

LB1
M1024596-331
LABEL

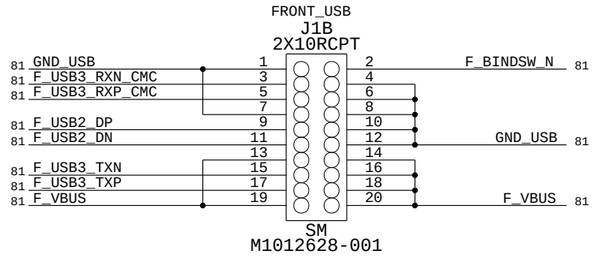


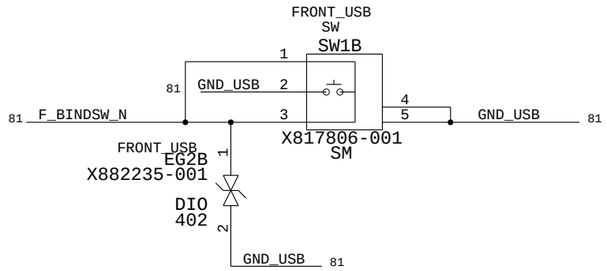
35P23X7P03_TARGET

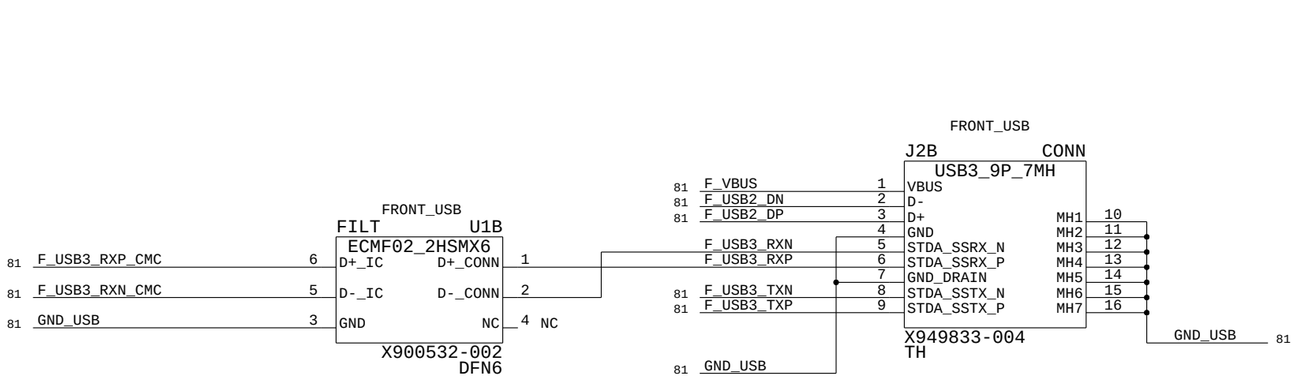
MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
NA	FR4	PCB1	PCB,CACTUS,FAB G RETAIL,8 LAYERS,GI	PCB_GI
M1037358-002	FR4	PCB1	PCB,CACTUS,FAB G RETAIL,8 LAYERS,OSP	PCB_OSP

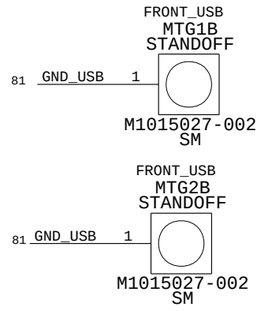
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	VER
	Cactus	80/82	80/82	0.991

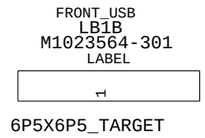
FRONT PANEL USB - NESTED PCB

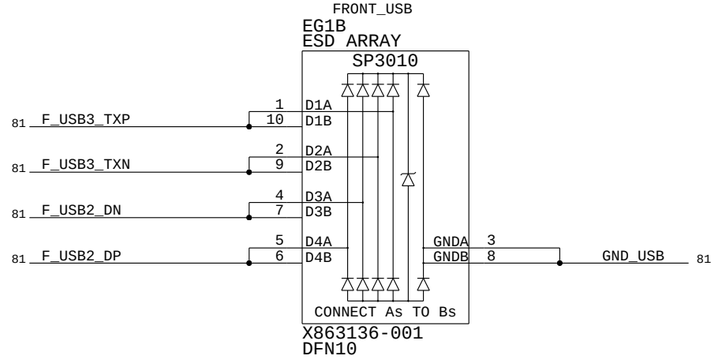












MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
M1033394-001	FR4	PCB1B	PCB,CACTUS,FAB E RETAIL,FRONT USB,8 LAYERS,G1	FRONT_USB

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	VER
	Cactus	81/82	81/82	0.991

BOM DEFINITIONS

BOM	DEFINTION
AUDIO	INCLUDES COMPONENTS FOR THE STANDARD AUDIO SOLUTION
AUDIO_PREM	INCLUDES COMPONENTS FOR THE PREMIUM SE/LE SPEAKER SOLUTION
COMMON	ALL COMPONENTS WITH NO BOM PROPERTY
DEBUG	COMPONENTS REQUIRED FOR BRING UP & DEBUG
DEBUG_HDT	HDT-RELATED DEBUG COMPONENTS
DEBUG_SHUNT	COMPONENTS WHICH ARE ON DEBUG BOARDS, BUT ARE REMOVED/SHORTED ON RETAIL
EMMC_BASE	DUMMY PLACE HOLDER FOR EMMC DEVICE & RESISTORS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM
EMMC_HYNIX_16NM	HYNIX EMMC DEVICE
EMMC_SAMSUNG_14NM	SAMSUNG EMMC DEVICE
EMMC_TOSHIBA_15NM	TOSHIBA EMMC DEVICE
GDDR5_BASE	DUMMY PLACE HOLDER FOR GDDR5. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM
GDDR5_HYNIX	HYNIX GDDR5 MEMORY
GDDR5_SAMSUNG	SAMSUNG GDDR5 MEMORY
FRONT_USB	COMPONENTS ON THE FRONT PANEL USB
KIC_BASE	DUMMY PLACE HOLDER FOR KIC. NEVER USE THIS IN THE RECIPE FILE. USE ONE OF THESE INSTEAD: KIC_DEV OR KIC_RETAIL
KIC_DEV	DEBUG VERSION OF KRAKEN
KIC_RETAIL	RETAIL VERSION OF KRAKEN
M2_ONLY	POPULATE TO SUPPORT AN M.2 INTERFACE
NO_M2	POPULATE WHEN THERE IS NO M2. INTERFACE
PCB_GI	FAB TYPE: GOLD
PCB_OSP	FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE GREEN SOLDERMASK
PCB_OSP_BLACK	FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE BLACK SOLDERMASK
RTC_RETAIL	RTC CIRCUIT IMPLEMENTATION FOR RETAIL BOARDS
RTC_XDK	RTC CIRCUIT IMPLEMENTATION FOR XDK BOARDS
SOC_BASE	DUMMY PLACE HOLDER FOR SOC. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM
SOC_EMPTY	DOES NOT STUFF ANUBIS
SOC_INCLUDE	STUFFS ANUBIS
VR_FIXED	SET ALL VRS TO FIXED VOLTAGES (NON-MARGINED). EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_MM
VR_MM	ALLOWS MOST VRS TO BE MARGINED FOR M&M BOARDS. EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_FIXED