Raspored pinova za komponente MAX 10 platforme

	Naziv	Smer	Aktivna	Lokacija	I/O banka	VREF grupa	I/O standard
TAKT RESET	i_clk	input	1	PIN_H6	2	B2_N0	3.3-V LVTTL
	in_rst	input	0	PIN_E6	8	B8_N0	3.3 V Schmitt Trigger
TASTERI	i_pb_rst	input	1	PIN_F1	1A	B1_N0	3.3 V Schmitt Trigger
	i_pb_down	input	1	PIN_C1	1A	B1_N0	3.3 V Schmitt Trigger
	i_pb_left	input	1	PIN_D1	1A	B1_N0	3.3 V Schmitt Trigger
	i_pb_right	input	1	PIN_E3	1A	B1_N0	3.3 V Schmitt Trigger
	i_pb_center	input	1	PIN_C2	1A	B1_N0	3.3 V Schmitt Trigger
	i_pb_up	input	1	PIN_E1	1A	B1_N0	3.3 V Schmitt Trigger
PREKIDAČI	i_sw[7]	input	1	PIN_K1	2	B2_N0	3.3 V Schmitt Trigger
	i_sw[6]	input	1	PIN_K2	2	B2_N0	3.3 V Schmitt Trigger
	i_sw[5]	input	1	PIN_N2	2	B2_N0	3.3 V Schmitt Trigger
	i_sw[4]	input	1	PIN_N3	2	B2_N0	3.3 V Schmitt Trigger
	i_sw[3]	input	1	PIN_M1	2	B2_N0	3.3 V Schmitt Trigger
	i_sw[2]	input	1	PIN_M2	2	B2_N0	3.3 V Schmitt Trigger
	i_sw[1]	input	1	PIN_L3	2	B2_N0	3.3 V Schmitt Trigger
	i_sw[0]	input	1	PIN_M3	2	B2_N0	3.3 V Schmitt Trigger
LED DIODE	o_led[7]	output	1	PIN_D8	8	B8_N0	3.3-V LVTTL
	o_led[6]	output	1	PIN_C10	8	B8_N0	3.3-V LVTTL
	o_led[5]	output	1	PIN_C9	8	B8_N0	3.3-V LVTTL
	o_led[4]	output	1	PIN_B10	8	B8_N0	3.3-V LVTTL
	o_led[3]	output	1	PIN_A10	8	B8_N0	3.3-V LVTTL
	o_led[2]	output	1	PIN_A11	8	B8_N0	3.3-V LVTTL
	o_led[1]	output	1	PIN_A9	8	B8_N0	3.3-V LVTTL
	o_led[0]	output	1	PIN_A8	8	B8_N0	3.3-V LVTTL
IZBOR KOMPONENTE	o_mux_row_or_digit_0	output	1	PIN_J13	5	B5_N0	3.3-V LVTTL
	o_mux_row_or_digit_1	output	1	PIN_K11	5	B5_N0	3.3-V LVTTL
	o_mux_row_or_digit_2	output	1	PIN_K12	5	B5_N0	3.3-V LVTTL
	o_mux_sel_color_or_7segm_0	output	1	PIN_J10	5	B5_N0	3.3-V LVTTL
	o_mux_sel_color_or_7segm_1	output	1	PIN_H10	5	B5_N0	3.3-V LVTTL
7-SEGMENTNI DISPLEJ	o_n_col_0_or_7segm_a	output	0	PIN_H8	5	B5_N0	3.3-V LVTTL
	o_n_col_1_or_7segm_b	output	0	PIN_K10	5	B5_N0	3.3-V LVTTL
	o_n_col_2_or_7segm_c	output	0	PIN_H5	2	B2_N0	3.3-V LVTTL
	o_n_col_3_or_7segm_d	output	0	PIN_H4	2	B2_N0	3.3-V LVTTL
	o_n_col_4_or_7segm_e	output	0	PIN_J1	2	B2_N0	3.3-V LVTTL
	o_n_col_5_or_7segm_f	output	0	PIN_J2	2	B2_N0	3.3-V LVTTL
	o_n_col_6_or_7segm_g	output	0	PIN_L12	5	B5_N0	3.3-V LVTTL
	o_n_col_7_or_7segm_dp	output	0	PIN_J12	5	B5_N0	3.3-V LVTTL
SEMAFOR	o_sem_g	output	1	PIN_B1	1A	B1_N0	3.3-V LVTTL
	o_sem_r	output	1	PIN_H13	5	B5_N0	3.3-V LVTTL
	o_sem_y	output	1	PIN_E4	1A	B1_N0	3.3-V LVTTL