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(54) **GRADED DIELECTRIC STRUCTURES**

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(58) **Field of Classification Search**

None

See application file for complete search history.

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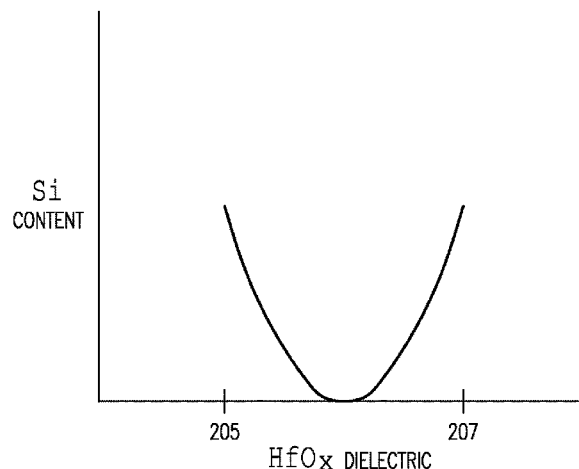
(57) **ABSTRACT**

Graded dielectric layers and methods of fabricating such  
dielectric layers provide dielectrics in a variety of electronic  
structures for use in a wide range of electronic devices and  
systems. In an embodiment, a dielectric layer is graded with  
respect to a doping profile across the dielectric layer. In an  
embodiment, a dielectric layer is graded with respect to a  
crystalline structure profile across the dielectric layer. In an  
embodiment, a dielectric layer is formed by atomic layer  
deposition incorporating sequencing techniques to generate  
a doped dielectric material.

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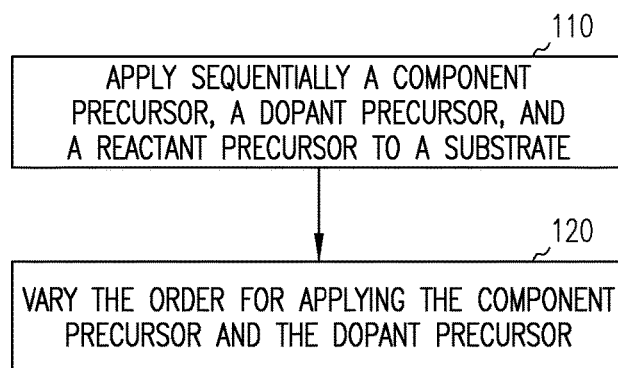


FIG. 1

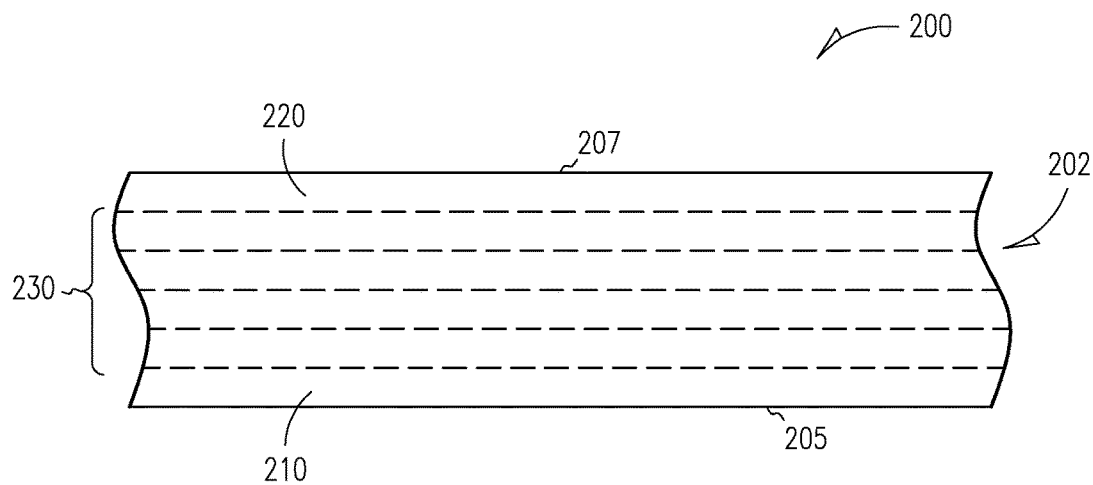


FIG. 2

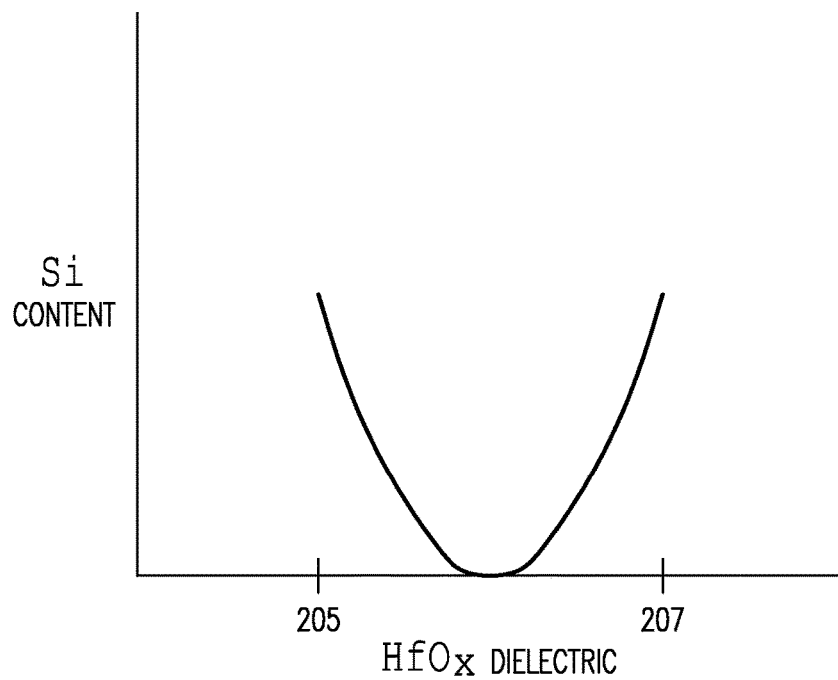


FIG. 3

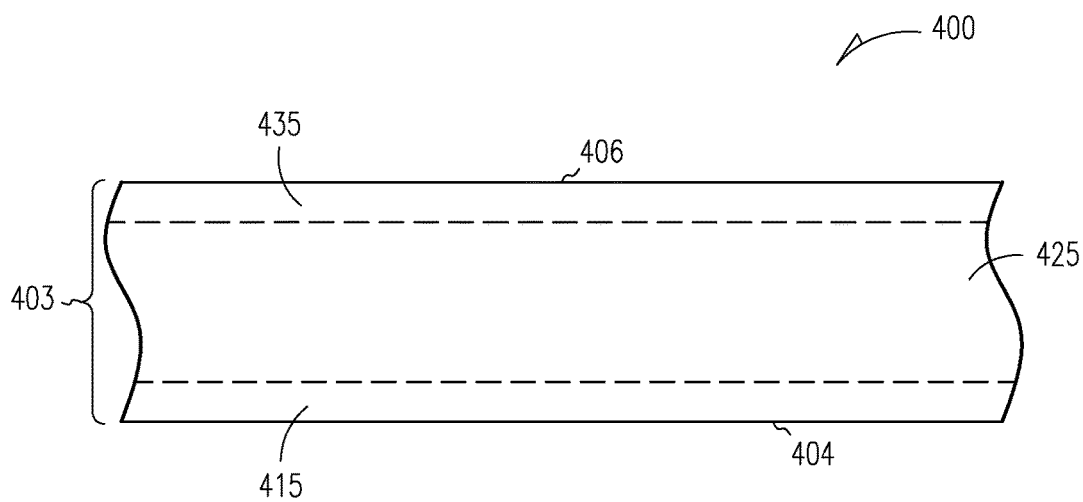


FIG. 4



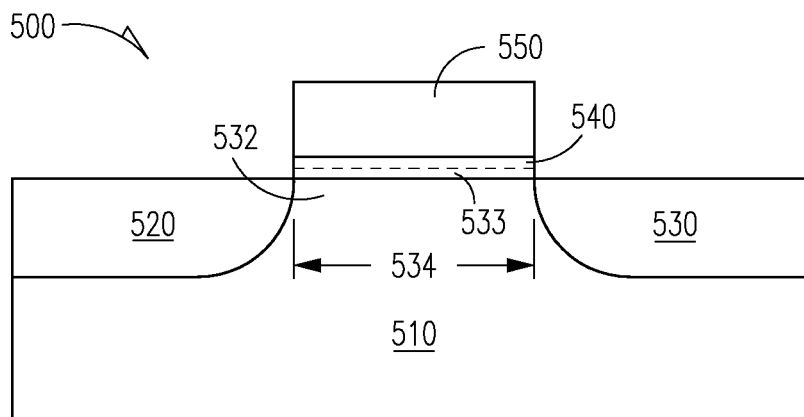


FIG. 5

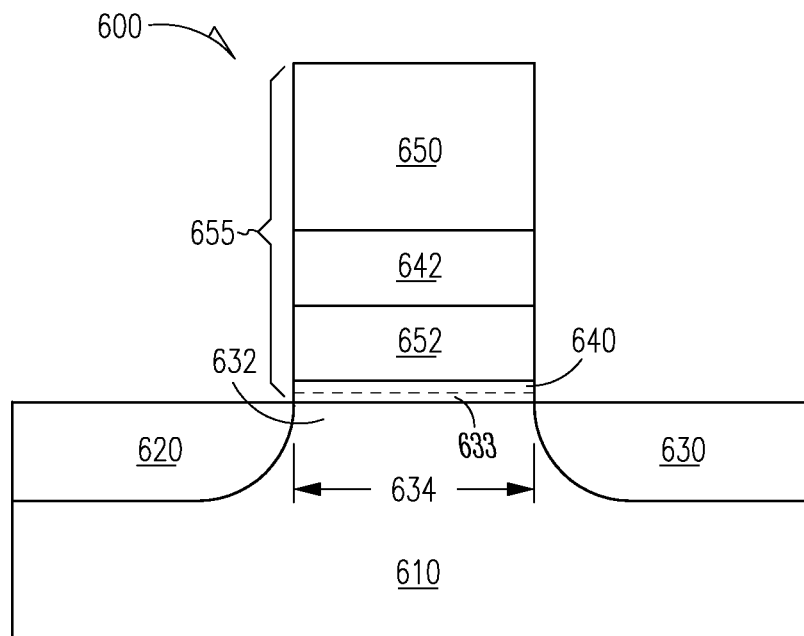


FIG. 6

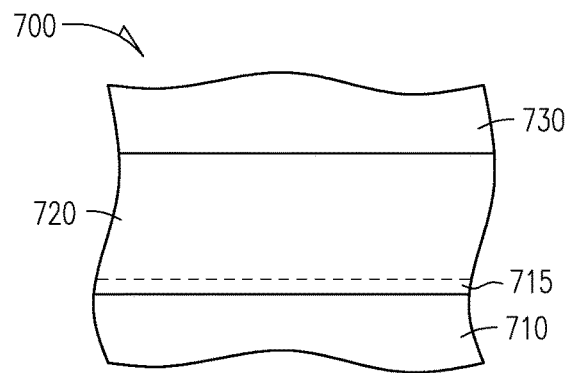


FIG. 7

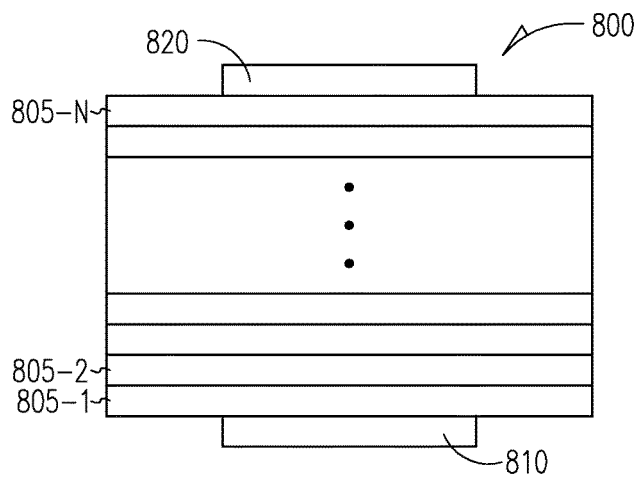


FIG. 8

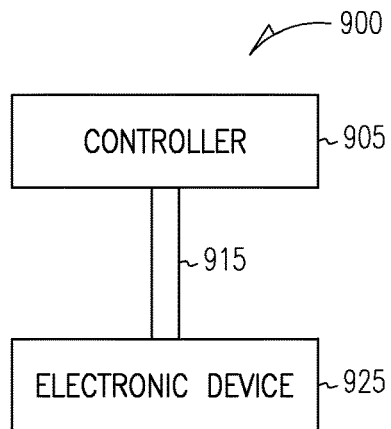


FIG. 9

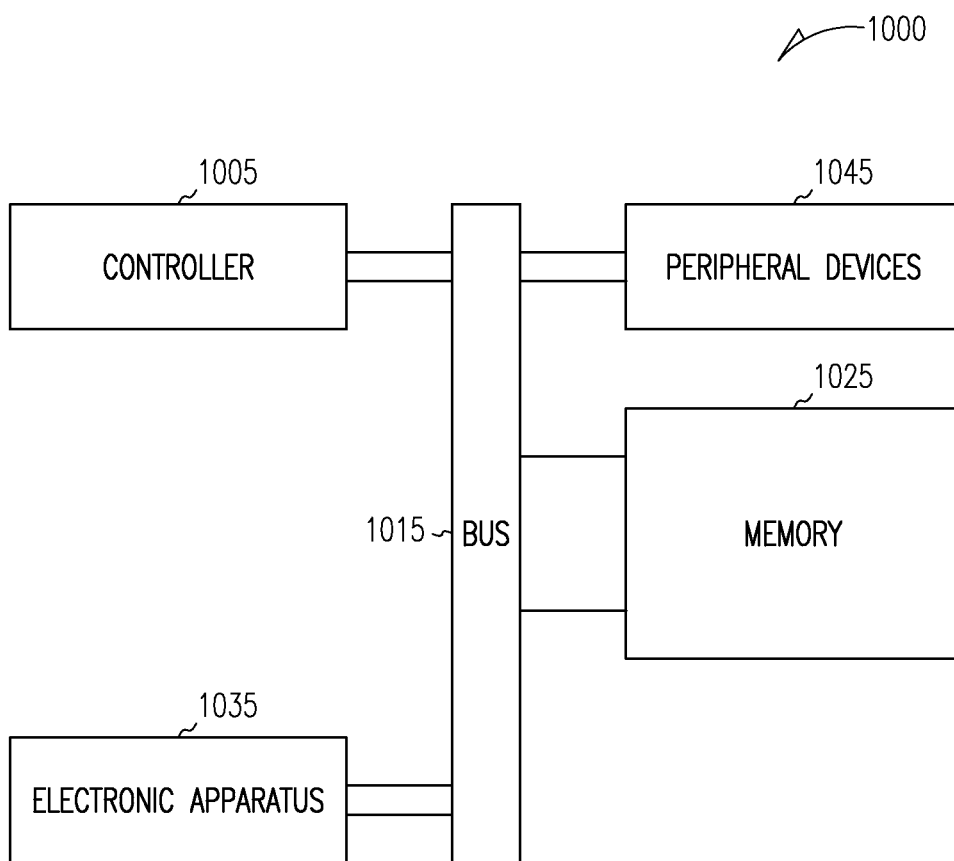


FIG. 10

## GRADED DIELECTRIC STRUCTURES

## PRIORITY APPLICATION

This application is a divisional of U.S. application Ser. No. 13/366,025, filed Feb. 3, 2012, which is a divisional of U.S. application Ser. No. 11/216,542, filed Aug. 30, 2005, now issued as U.S. Pat. No. 8,110,469, all of which are incorporated herein by reference in their entirety.

## TECHNICAL FIELD

This application relates generally to semiconductor devices and device fabrication and, more particularly, to dielectric layers and their method of fabrication.

## BACKGROUND

Higher capacitance, lower leakage dielectric layers for capacitor dielectric and transistor gate applications are needed for scaling down device dimensions to realize a higher density memory. An approach to increasing the capacitance is to increase the dielectric constant of the capacitor dielectric. Although metal oxide dielectric films, such as  $\text{HfO}_2$ , have higher dielectric constants compared to  $\text{SiO}_2$  and  $\text{Al}_2\text{O}_3$ , such metal oxide dielectrics typically exhibit higher leakage current. In order to reduce this leakage current to acceptable levels for these films, these metal oxide films are formed as thicker dielectric films. Forming the thicker metal oxide dielectric in turn reduces the capacitance of the structure. Additionally, the thermal stability of some metal oxides may be poor, presumably due to crystallization at higher temperature, where the crystallization temperature decreases with increased film thickness.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 depicts features of an embodiment of a method to form a graded dielectric layer.

FIG. 2 depicts an embodiment of a dielectric layer for an electronic device, where the dielectric layer has a number of regions that provides a dopant profile that varies across dielectric layer.

FIG. 3 illustrates an example embodiment for a dopant profile between two opposite ends of a dielectric layer, such as between the interfaces of the dielectric layer of FIG. 2.

FIG. 4 shows an embodiment of a graded dielectric layer for an electronic device, where the graded dielectric layer has a number of regions that provide a structure profile that varies across the graded dielectric layer.

FIG. 5 shows an embodiment of a configuration of a transistor having a graded dielectric layer.

FIG. 6 shows an embodiment of a configuration of a floating gate transistor having a graded dielectric layer.

FIG. 7 shows an embodiment of a configuration of a capacitor with a dielectric having a graded dielectric layer.

FIG. 8 depicts an embodiment of a nanolaminate having at least one graded dielectric layer.

FIG. 9 is a simplified diagram for an embodiment of a controller coupled to an electronic device, where the controller, electronic device, or the controller and the electronic device have a graded dielectric layer.

FIG. 10 illustrates a diagram for an embodiment of an electronic system having one or more devices having a graded dielectric layer.

## DETAILED DESCRIPTION

The following detailed description refers to the accompanying drawings that show, by way of illustration, specific

aspects and embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form an integrated circuit (IC) structure. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to generally include n-type and p-type semiconductors and the term insulator or dielectric is defined to include any material that is less electrically conductive than the materials referred to as conductors.

A dielectric film has both a physical dielectric thickness and an equivalent oxide thickness ( $t_{eq}$ ). The equivalent oxide thickness quantifies the electrical properties, such as capacitance, of the dielectric film in terms of a representative physical thickness.  $t_{eq}$  is defined as the thickness of a theoretical  $\text{SiO}_2$  layer that would be required to have the same capacitance density as a given dielectric, ignoring leakage current and reliability considerations.

For some typical dielectric layers, the capacitance is determined as one for a parallel plate capacitance:  $C = \kappa \epsilon_0 A / t$ , where  $\kappa$  is the dielectric constant,  $\epsilon_0$  is the permittivity of free space,  $A$  is the area of the capacitor, and  $t$  is the thickness of the dielectric. The thickness,  $t$ , of a material is related to its  $t_{eq}$  for a given capacitance, with  $\text{SiO}_2$  having a dielectric constant  $\kappa_{ox} = 3.9$ , as

$$t = (\kappa / \kappa_{ox}) t_{eq} = (\kappa / 3.9) t_{eq}.$$

Thus, materials with a dielectric constant greater than that of  $\text{SiO}_2$ , 3.9, will have a physical thickness that can be considerably larger than a desired  $t_{eq}$ , while providing the desired equivalent oxide thickness. For example, an alternate dielectric material with a dielectric constant of 10 could have a thickness of about 25.6 Å to provide a  $t_{eq}$  of 10 Å, not including any depletion/inversion layer effects. Thus, a reduced equivalent oxide thickness for transistors can be realized by using dielectric materials with higher dielectric constants than  $\text{SiO}_2$ .

One of the advantages using  $\text{SiO}_2$  as a gate dielectric or a capacitor dielectric has been that the formation of the  $\text{SiO}_2$  layer results in an amorphous dielectric. Having an amorphous structure for a dielectric provides for reducing problems of leakage current associated with grain boundaries in polycrystalline dielectrics that provide high leakage paths. Additionally, grain size and orientation changes throughout a polycrystalline dielectric can cause variations in the film's dielectric constant, along with uniformity and surface topography problems. Typically, materials having the advantage of a high dielectric constant relative to  $\text{SiO}_2$  also have the disadvantage of a crystalline form, at least in a bulk configuration. The best candidates for replacing  $\text{SiO}_2$  as a gate dielectric or a capacitor dielectric are those with high dielectric constant, which can be fabricated as a thin layer with an amorphous form.

Candidates to replace SiO<sub>2</sub> include high-κ dielectric materials. High-κ materials include materials having a dielectric constant greater than silicon dioxide, for example, dielectric materials having a dielectric constant greater than about twice the dielectric constant of silicon dioxide. A set of high-κ dielectric candidates for replacing silicon oxide as the dielectric material in electronic components in integrated circuit includes lanthanide oxides, HfO<sub>2</sub>, ZrO<sub>2</sub>, TiO<sub>2</sub>, and other binary metal oxides.

An embodiment for a method of forming an electronic device includes forming a graded dielectric layer in an integrated circuit including controlling a doping profile of the dielectric layer formed substantially as monolayers across the dielectric layer. An embodiment for a method of forming an electronic device includes forming a graded dielectric layer in an integrated circuit including controlling a structure profile of the dielectric layer that varies across the dielectric layer. In an embodiment, a dielectric layer is formed using a pulsing sequence of a component precursor/a dopant precursor/a reactant precursor and varying the order of pulsing the component precursor and the dopant precursor. Embodiments provide for capacitors, transistors, memory devices, and electronic systems having structures including a graded dielectric layer, and methods for forming such structures.

In an embodiment, a dielectric layer has a number of regions with varying characteristics across the dielectric layer to provide a graded dielectric layer. The regions may be multiple layers of the dielectric layer, where these multiple layers may be referred to as sub-layers or films within the dielectric layer. The films may have a thickness ranging from a number of monolayers to thousands of Angstroms or more depending on the electronic device in which the dielectric layer is located. The varying characteristics may include a dopant profile across the dielectric layer, a structure profile across the dielectric layer, or a dopant profile across the dielectric layer and a structure profile across the dielectric layer. Herein, a structure profile that varies across a dielectric layer includes one or more layers of crystalline material and one or more layers of amorphous material. In an embodiment, the graded dielectric layer may include a metal oxide. The metal oxide may be doped with silicon. The metal oxide may be doped with a metal dopant. The metal oxide may include hafnium oxide, zirconium oxide, hafnium oxide doped with silicon, hafnium oxide doped with a metal dopant, zirconium oxide doped with silicon, zirconium oxide doped with a metal dopant, or combinations of doped and undoped metal oxides.

Embodiments of graded dielectric layers may be formed using a variety of fabrication techniques. In an embodiment, a dopant element or elements are added to a dielectric material in a uniform, controlled manner to reduce the leakage current properties of the dielectric material with minimum detrimental impact on the dielectric constant of the dielectric material. As a result, the dielectric material may have a relatively low leakage without compromising capacitance for an electronic device in which the dielectric material is disposed. In an embodiment, a method includes fabricating a hafnium based dielectric, such as a HfO<sub>2</sub> film, having a silicon dopant. Since a hafnium oxide film having a silicon dopant may have a low leakage film, much thinner hafnium oxide dielectrics may be formed compared to a conventional HfO<sub>2</sub> film. Embodiments may include hafnium based dielectrics having one or more metal dopants. In an embodiment, a graded dielectric layer is formed by atomic layer deposition (ALD) or a variation thereof.

ALD, also known as atomic layer epitaxy (ALE), is a modification of chemical vapor deposition (CVD) and is also called "alternately pulsed-CVD." In ALD, gaseous precursors are introduced one at a time to the substrate surface mounted within a reaction chamber (or reactor). This introduction of the gaseous precursors takes the form of pulses of each gaseous precursor. In a pulse of a precursor gas, the precursor gas is made to flow into a specific area or region for a short period of time. Between the pulses, the reaction chamber may be purged with a gas, where in many cases the purge gas is an inert gas. Between the pulses, the reaction chamber may be evacuated. Between the pulses, the reaction chamber may be purged with a gas and evacuated. The pulses may be switched between reactant gases, essentially providing a "zero second" purge.

In a chemisorption-saturated ALD (CS-ALD) process, during the first pulsing phase, reaction with the substrate occurs with the precursor saturatively chemisorbed at the substrate surface. Subsequent pulsing with a purging gas removes precursor excess from the reaction chamber.

The second pulsing phase introduces another precursor on the substrate where the growth reaction of the desired film takes place. Subsequent to the film growth reaction, reaction byproducts and precursor excess are purged from the reaction chamber. With favourable precursor chemistry where the precursors adsorb and react with each other on the substrate aggressively, one ALD cycle can be performed in less than one second in properly designed flow type reaction chambers. Typically, precursor pulse times range from about 0.5 sec to about tens of seconds.

In ALD, the saturation of all the reaction and purging phases makes the growth self-limiting. This self-limiting growth results in large area uniformity and conformality, which has important applications for such cases as planar substrates, deep trenches, and in the processing of porous silicon and high surface area silica and alumina powders. Significantly, ALD provides for controlling film thickness in a straightforward manner by controlling the number of growth cycles.

The precursors used in an ALD process may be gaseous, liquid or solid. However, liquid or solid precursors should be volatile. The vapor pressure should be high enough for effective mass transportation. In addition, solid and some liquid precursors may need to be heated inside the reaction chamber and introduced through heated tubes to the substrates. The necessary vapor pressure should be reached at a temperature below the substrate temperature to avoid the condensation of the precursors on the substrate. Due to the self-limiting growth mechanisms of ALD, relatively low vapor pressure solid precursors can be used though evaporation rates may vary somewhat during the process because of changes in their surface area.

There are several other characteristics for precursors used in ALD. The precursors should be thermally stable at the substrate temperature, because their decomposition may destroy the surface control and accordingly the advantages of the ALD method that relies on the reaction of the precursor at the substrate surface. A slight decomposition, if slow compared to the ALD growth, can be tolerated.

The precursors should chemisorb on or react with the surface, though the interaction between the precursor and the surface as well as the mechanism for the adsorption is different for different precursors. The molecules at the substrate surface should react aggressively with the second precursor to form the desired solid film. Using highly reactive precursors in ALD contrasts with the selection of precursors for conventional CVD. The by-products in the

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reaction should be gaseous in order to allow their easy removal from the reaction chamber.

In a reaction sequence ALD (RS-ALD) process, the self-limiting process sequence involves sequential surface chemical reactions. RS-ALD relies on chemistry between a reactive surface and a reactive molecular precursor. In an RS-ALD process, molecular precursors are pulsed into the ALD reaction chamber separately. A metal precursor reaction at the substrate is typically followed by an inert gas pulse to remove excess precursor and by-products from the reaction chamber prior to pulsing the next precursor of the fabrication sequence.

By RS-ALD, films can be layered in equal metered sequences that are all identical in chemical kinetics, deposition per cycle, composition, and thickness. RS-ALD sequences generally deposit less than a full layer per cycle. Typically, a deposition or growth rate of about 0.25 to about 2.00 Å per RS-ALD cycle can be realized.

The advantages of RS-ALD include continuity at an interface avoiding poorly defined nucleating regions that are typical for chemical vapor deposition (<20 Å) and physical vapor deposition (<50 Å), conformality over a variety of substrate topologies due to its layer-by-layer deposition technique, use of low temperature and mildly oxidizing processes, lack of dependence on the reaction chamber, growth thickness dependent solely on the number of cycles performed, and ability to engineer multilayer laminate films with resolution of one to two monolayers. RS-ALD processes allows for deposition control on the order on monolayers and the ability to deposit monolayers of amorphous films. In an embodiment, ALD processes may allow composition control within each monolayer.

FIG. 1 shows features of an embodiment of a method to form a graded dielectric layer. At 110, a precursor for a component element of the dielectric layer, a dopant precursor, and a reactant precursor are sequentially applied to a substrate. This application scheme provides for applying both the component element precursor and the dopant precursor prior to applying the reactant precursor. For a metal oxide having a metal dopant, the scheme may be referred to as a MMO scheme. For a metal oxide having a silicon dopant, the scheme may be referred to as a MSO scheme. At 120, the order for applying the precursor for the component element and the dopant precursor is varied. An application cycle may include a MSO sequence followed by another MSO sequence. Varying the order may include a cycle having a SMO sequence followed by a MSO sequence. Varying the order to the application of the precursors for the component element and the dopant provides an alternating cycle scheme. Applying an alternating cycle scheme to a MSO scheme, a MMO scheme, or a variation thereof may be controlled to provide substantially mixed layers of component element and dopant at each sub-layer of a dielectric layer. The amount of dopant incorporated into the formed dielectric may be controlled by the order that the component element precursor comes in the cycle with respect to the dopant precursor. In an embodiment, the amount of dopant depends on the first precursor applied. In an embodiment, the dielectric material includes a metal oxide, such as, but not limited to, a hafnium oxide. In an embodiment, the component element is a metal of the metal oxide and the dopant includes silicon.

Various embodiments of a method for forming a dielectric layer overcome problems associated with introducing controlled amounts of a dopant typically associated with both the control of the doping process and the lack of well behaved precursors for the dielectric component element

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and the dopant. For example, problems of depositing a silicon dopant in a metal oxide, such as hafnium oxide, may arise due to differences in typical processing temperatures for the silicon and the metal oxide. In an embodiment, hafnium oxide having silicon dopant is deposited on a substrate in an integrated circuit by atomic layer deposition. In an embodiment, a hafnium oxide film is formed by ALD with a thickness in the range from about 60 Å to about 100 Å with a silicon uniformly distributed in the film. The uniform distribution of silicon may include uniformly varying silicon concentration between selected regions in the hafnium oxide film. In an embodiment, silicon doped hafnium oxide is formed by ALD using a MSO scheme combined with an alternating cycle scheme. In an embodiment, silicon may be distributed in quantized amounts across the hafnium oxide layer to provide a varying dopant profile across the hafnium oxide layer. Quantized doping may be accomplished using intermittent (periodic) atomic layer deposition cycles of a silicon source. In various embodiments, a zirconium oxide layer may be formed in place of or in combination with a hafnium oxide layer.

In an embodiment, a method includes varying silicon concentration uniformly from about a 1:30 to 1:2 Si:Hf ratio. In an embodiment, a method includes varying silicon concentration uniformly from about a 1:15 to 1:1 Si:Hf ratio. In an embodiment, any of the amido hafnium precursors may be used as a Hf source and TDMAS (tetraakisdimethyl amido Si) may be used as a tractable Si source. A TDMAS/oxidizer ALD process has a monotonically decreasing deposition rate, but in concert with HfO<sub>x</sub> or sequentially with amido Hf precursors, the deposition rate may be controlled and moderated. In an embodiment, silicon is incorporated in hafnium oxide using a pulse/purge sequence such as: Hf/purge/Si/purge/O<sub>3</sub>/purge/Hf/purge/O<sub>3</sub>/purge/Si/purge/O<sub>3</sub>/purge, where Hf comes from an amido Hf precursor and Si comes from a TDMAS precursor. In an embodiment, this entire pulse/purge sequence constitutes one cycle, a MSO/MO/SO cycle. This cycle can be repeated any number of times to realize the desired thickness. In an embodiment, the silicon concentration may be varied by changing the order of Hf precursor pulses and the Si precursor pulses, such as: Si/purge/Hf/purge/O<sub>3</sub>/purge/Si/purge/O<sub>3</sub>/purge/Hf/purge/O<sub>3</sub>/purge, generating a SMO/SO/MO cycle. In an embodiment, ALD processing generates silicon dopant in a hafnium oxide. In an embodiment, ALD processing generates a silicon oxide/hafnium oxide mixture. In an embodiment, ALD processing generates a hafnium silicate. In various embodiments, a zirconium oxide layer may be formed in place of or in combination with a hafnium oxide layer. In an embodiment, a method includes varying silicon concentration uniformly from about a 1:30 to 1:2 Si:Zr ratio. In an embodiment, a method includes varying silicon concentration uniformly from about a 1:15 to 1:1 Si:Zr ratio.

In an embodiment, a metal precursor is applied to provide partial monolayer coverage that allows mixture of the metal with silicon at a monolayer level with the subsequent application of the silicon precursor. In an embodiment, sequencing hafnium and then silicon generates an appropriate hafnium silicon ratio of about 22:1, and sequencing silicon and then hafnium generates a hafnium silicon ratio of about 1:3.5. In an embodiment, sequencing hafnium and then silicon generates an appropriate hafnium silicon ratio of about 22:1, and sequencing silicon and then hafnium generates a hafnium silicon ratio of about 1:5. The ratio difference is provided by changing the order. The order change allows partial but mixed layer at every sub-layer of the dielectric layer. To obtain a mixed sub-layer, the element

ratio may be changed by changing the ALD process particulars. The silicon concentration may be adjusted reproducibly and uniformly over a large range by combining MSO schemes and alternating cycle schemes. Silicon may be strongly dependent on the order that the metal (Hf) precursor is applied in the cycle. Silicon in hafnium oxide film may aid in suppressing crystallization providing better thermal stability than for conventional films.

FIG. 2 shows an embodiment of a dielectric layer **202** for an electronic device **200**, where dielectric layer **202** has a number of regions that provides a dopant profile that varies across dielectric layer **202**. The dopant profile may vary continuously or in continuous segments across dielectric layer **202**. Alternatively, portions of dielectric layer **202** may have a dopant profile that is relatively constant. In an embodiment, the dopant concentration of dielectric layer **202** is graded across dielectric layer **202** from a dopant concentration at an interface **205** to a region or a point within dielectric layer **202** at which there is no dopant concentration or the dopant concentration is substantially less than that at interface **205** and graded back to a dopant concentration at an opposite interface **207** that is at a dopant level near or at that of interface **205**. An embodiment provides for any dopant profile across dielectric layer **202** that is not substantially constant across the entire dielectric layer.

Dielectric layer **202** may be formed as a fixed number of regions. Dielectric layer **202** may be configured as a nanolaminate structure with distinct layers. The term “nanolaminate” means a composite film of ultra thin layers of two or more materials in a layered stack. Typically, each layer in a nanolaminate has a thickness of an order of magnitude in the nanometer range. Further, each individual material layer of the nanolaminate can have a thickness as low as a monolayer of the material or as high as 20 nanometers.

Dielectric layer **202** may be configured as a graded structure within quantized deposition levels generated in the formation of dielectric layer **202**. In an example embodiment, dielectric layer **202** includes regions **210**, **230**, and **220**, where regions **210**, **220**, and **230** provide dielectric layer **203** with a varying dopant profile. Regions **210**, **230**, and **220** include a dopant concentration such that the dopant concentration is not constant across dielectric layer **202**. Region **230** may be lightly doped or undoped with regions **210**, **220** having a higher concentration of the dopant element or elements. The dopant profile may provide for the largest dopant concentration at one or both of interfaces **205**, **207**. The dopant profile may include quantized levels such that regions **210**, **220**, **230** have a relatively constant dopant profile, which is not at the same level across all regions. In an embodiment, regions **210**, **230**, and **220** may be configured as a nanolaminate. Dielectric layer **202** is not limited to three regions, but may include any number of regions depending on the application.

In embodiment, dielectric layer **202** may be a metal oxide. Dielectric layer **202** may be a metal oxide having a silicon dopant, other non-metal dopant, or a silicon dopant and other non-metal dopant. Dielectric layer **202** may be a metal oxide having one or more metal dopants. Dielectric layer **202** may be a metal oxide having one or more metal dopants and a silicon dopant, another non-metal dopant, or a silicon dopant and another non-metal dopant. In an embodiment, dielectric layer **202** includes a silicon doped hafnium oxide. A silicon doped hafnium oxide may be configured with the silicon content graded across the hafnium oxide. In an embodiment, silicon content is graded across a hafnium oxide dielectric layer having a thickness in the range from about 60 Angstroms to about 100 Angstroms. In an embodi-

ment, at interface **205**, a silicon doped hafnium oxide has a Hf:Si ratio of about 2:1 to 3:1, that is, the hafnium oxide is silicon-rich. Herein, silicon-rich metal oxide means having a silicon to metal ratio of 1:5 or larger. Within this definition of silicon-rich metal oxide is included a traditional view of silicon-rich in which a silicon metal oxide has an atomic percentage of silicon being greater than the atomic percentage of the metal. The silicon content is graded such that a region or level in the hafnium oxide has either no silicon or substantially less silicon than at interface **205**, such as less than a 1:20 (Si:Hf) ratio. From this low silicon content region, the hafnium oxide has a silicon content graded back to a silicon-rich content at opposite interface **207** such as a silicon content having a 2:1 to 3:1 (Hf:Si) ratio. In an embodiment, silicon-rich regions having a Hf:Si ratio of about 2:1 to 3:1 may extend to about 20 or about 30 Angstroms from one or both of the interfaces **205**, **207** towards the hafnium-rich region within dielectric layer **202**. In an embodiment, silicon-rich regions having a Hf:Si ratio of about 2:1 to 5:1 may extend to about 20 or about 30 Angstroms from one or both of the interfaces **205**, **207** towards the hafnium-rich region within dielectric layer **202**. The hafnium-rich region may be a center layer of region **230** having a Hf:Si ratio of about 22:1. A hafnium-rich region may be located at other regions within dielectric layer **202** other than the center layer, with a silicon-rich hafnium oxide layer at one or both interfaces. In various embodiments, a zirconium oxide layer may be formed in place of or in combination with a hafnium oxide layer.

In an embodiment, the silicon doped hafnium oxide dielectric layer, as dielectric layer **202** of FIG. 2, is a substantially a hafnium oxide layer having silicon dopants rather than a hafnium silicate or a mixture of silicon oxide and hafnium oxide. In an embodiment, silicon content is graded across dielectric layer **202** including a hafnium silicate layer or sub-layer. In an embodiment, silicon content is graded across dielectric layer **202** including a layer or sub-layer of a hafnium oxide-silicon oxide mixture. Dielectric layer **202** having a silicon content graded from a silicon-rich hafnium oxide layer at interface **205** to a center having hafnium oxide with effectively little or no silicon and back to a silicon-rich hafnium oxide layer at interface **207** may provide a dielectric having effective permittivity increased by about one-third relative to conventional silicon hafnium oxides. Other embodiments include aluminum doped hafnium oxide dielectric layers, aluminum or silicon doped zirconium oxide, and mixtures or variations of these dielectric materials. Various embodiments are not limited to hafnium or zirconium metal oxides, but may include any metal oxide.

In embodiment, dielectric layer is configured as a number of layers whose formation is highly controlled to provide the graded dopant profile, where the layers are constructed as a series of monolayers. Each of the monolayers contains the basic material of the primary dielectric material with dopants mixed in the monolayer. In an embodiment of a dielectric layer containing silicon doped hafnium oxide, silicon may be mixed with the hafnium at every layer at which the dielectric is structured to include silicon. The amount of silicon mixed into the monolayers of hafnium oxide is varied across the dielectric layer from one interface to the opposite interface of the dielectric layer. An interior region may be configured with little or no silicon content. In various embodiments, a zirconium oxide layer may be formed in place of or in combination with a hafnium oxide layer.

FIG. 3 illustrates an example embodiment for a silicon dopant profile between two opposite ends of a hafnium oxide dielectric layer, such as between interface 205 and interface 207 of dielectric layer 202. In an embodiment, either or both interface 205 and interface 207 are interfaces to an insulative material. For instance, a larger dielectric structure may include dielectric layer 202 as a component. In an embodiment, either or both interface 205 and interface 207 are interfaces to a conductive material. In an embodiment, dielectric layer 202 is a capacitor dielectric in a capacitor with interfaces 205, 207 being the interfaces between the capacitor dielectric 202 and electrodes of the capacitor. In an embodiment, dielectric layer 202 is a gate dielectric in a transistor with interface 205 being the interface to the transistor channel. Interface 207 may be the interface to a control gate or a floating gate in a transistor.

Typically, crystalline dielectrics exhibit higher permittivity than their amorphous counterparts. However, they also often exhibit higher leakage currents. The higher leakage currents may reduce or even negate the benefit of high- $\kappa$  structures in charge storage devices or in low-power transistors, because, typically, the high- $\kappa$  material must be made physically thicker to control leakage current. In an embodiment, crystalline dielectrics may be used for enhanced permittivity dielectrics with lower leakage by depositing or generating high- $\kappa$  crystalline material on, in, or under an amorphous insulating material. Various embodiments include bilayers, trilayers, multiple layer dielectric stacks, or nanolaminate-type dielectrics composed of selected crystalline layers with amorphous layers. In various embodiments, the elements of the crystalline layers may differ from the elements of the amorphous layer.

An embodiment may include a single-layer amorphous dielectric with controlled nanocrystalline content within the amorphous layer. In an embodiment, a crystalline region may be configured as a wave of crystallinity, where the long range order varies across a region of the graded dielectric layer. In an embodiment, a crystalline region may be configured as a wave of crystallinity, where the crystal grain size varies across a region of the graded dielectric layer. In an embodiment, crystallinity is driven by doping factors in the material.

In an embodiment, the crystallinity of a high- $\kappa$  layer is separated, via an amorphous layer or layers, from the existing crystallinity of the material on which such a structure is disposed. In an embodiment, the crystallinity of a high- $\kappa$  layer is separated, via an amorphous layer or layers, from crystallization mechanical stress during downstream thermal processing induced by the material coupled above and below such structures. In an embodiment, a structure with a dielectric layer between two conductive layers, such as electrodes, has at least one amorphous layer between a crystalline region of the dielectric layer and one of the conductive layers. Having the amorphous region in such a structure may prevent grain boundaries from propagating from one conductive layer to the other conductive layer. The degree of crystallinity of a high- $\kappa$  dielectric layer may be more intrinsic to its own composition, thermodynamics, and internal thermal and mechanical stresses and is less dictated by external thermal or mechanical stresses, due to inclusion of such amorphous regions.

FIG. 4 shows an embodiment of a graded dielectric layer 403 for an electronic device 400, where graded dielectric layer 403 has a number of regions that provide a structure profile that varies across graded dielectric layer 403. In an embodiment, graded dielectric layer 403 includes a crystalline dielectric film 425 interior to graded dielectric layer 403

and an amorphous dielectric film 415 at an interface 404 of graded dielectric layer 403 with another material. In an embodiment, amorphous dielectric film 415 is coupled to a conductive layer at interface 404. In an embodiment, graded dielectric layer 403 has amorphous dielectric film 415 contacting interface 405 and an amorphous layer 435 at an interface 406. In an embodiment, interfaces 404 and 406 each couple dielectric layer 403 to conductive material. In an embodiment, region 415 may be a crystalline region in graded dielectric layer 403 that is configured with an amorphous layer 435 and a crystalline layer 425. Graded dielectric 403 may be integral to an electronic device in an integrated circuit such that charge injection occurs at interface 406. In such an electronic device, crystalline layers 425 and 415 may be configured as one layer such that graded dielectric layer 403 is a bilayer.

Crystalline content or amorphous content in discrete layers may be controlled by various techniques or combinations thereof, including atomic layer deposition compositional control, process conditions such as reactant gas selection or processing temperature, and in-situ or ex-situ annealing. For example, increasing silica incorporation in hafnium silicates raises the crystallization temperature of  $\text{HfO}_2$  or  $\text{HfSiO}_x$ .

In an example embodiment, a graded dielectric layer having crystalline and amorphous regions may be used in capacitors to provide higher capacitance with low leakage current than expected from conventional capacitors. The graded dielectric layer may be used in capacitors having a titanium nitride electrode. The graded dielectric layer may be used in capacitors having a tantalum nitride electrode. In an embodiment, a capacitor has an amorphous silicon-rich  $\text{HfSiO}_x$  layer disposed prior to a top electrode in a bilayer or trilayer dielectric stack composed of Hf-rich  $\text{HfSiO}_x$  with a Hf:Si ratio of about 22:1. The top electrode may be a TiN electrode processed at temperatures as high as 600° C. The top electrode may be a TaN electrode. The presence of this top amorphous layer may prevent significant leakage current gains that would otherwise occur due to crystallization of  $\text{HfO}_2$ . An embodiment of a crystalline/amorphous trilayer graded dielectric structure in a capacitor dielectric stack may include a structure such as a TiN electrode\ALD Si-rich  $\text{HfSiO}_x$  (amorphous) dielectric layer\ALD chloride-based  $\text{HfO}_2$  or ALD amido-based  $\text{HfO}_2$  or  $\text{HfAlO}_x$  or ALD  $\text{HfO}_x\text{N}_y$  dielectric layer\Si-rich  $\text{HfSiO}_x$  (amorphous) dielectric layer\TiN electrode. Chloride-based  $\text{HfO}_2$  is typically crystalline as-deposited at higher temperatures. In formation of such a structure, Amido-based  $\text{HfO}_2$  and  $\text{HfON}$  films may benefit from annealing in the range of about 500° C. to about 700° C. to encourage crystallization of the middle dielectric layer prior to depositing the top amorphous dielectric layer. Such a process may encourage the top layer (Si-rich  $\text{HfSiO}_x$ ) to remain amorphous at lower  $\text{SiO}_2$  doping levels to enhance permittivity of the stack. In an embodiment, silica content in the Si-rich  $\text{HfSiO}_x$  is controlled and the formation process may be conducted without a dielectric anneal. An embodiment of a layered stack that balances crystalline and amorphous components to control thermal stability in desired places within the dielectric may include TiN\thick ALD  $\text{HfON}$ \ex-situ 500° C. anneal\thin ALD Si-rich  $\text{HfSiO}_x$ \600° C. deposited TiN. In various embodiments, zirconium may be deposited in place of or in combination with hafnium.

In an embodiment, graded dielectric layer 403 may have amorphous dielectric film that includes a silicon-rich metal silicon oxide. A crystalline dielectric film in graded dielectric layer 403 may include a metal oxide whose metal compound includes the metal of the silicon-rich metal



silicon oxide. In an embodiment, the silicon-rich metal silicon oxide includes a silicon-rich hafnium silicon oxide. The silicon-rich hafnium silicon oxide may be a silicon-rich hafnium silicate. In an embodiment, the crystalline dielectric film includes a metal oxide containing a plurality of metal species. In an embodiment, the crystalline dielectric film includes forming a metal oxynitride.

Various embodiments for forming a graded dielectric layer having a structure profile that varies across the dielectric layer include forming regions in the graded dielectric layer by atomic layer deposition. Properties of the graded dielectric layer may vary depending on the precursors used in the ALD process. For example a trimethylaluminum (TMA) precursor may behave differently at a substrate surface than an aluminum chloride precursor. Variation of the structure profile may be attained by changing precursors to obtain different compositions. In an embodiment, selection of precursors may determine the crystallinity of the dielectric layer. Chlorides tend to go down crystalline, while amides tend to provide amorphous structure.

The structure of the dielectric layer may be driven crystalline or amorphous depending on selection of such factors as the choice of precursor and reaction temperature. A stoichiometry may be approximately equivalent for two films formed using different precursors but the properties of these films may be different, providing different films for an electronic device. Further, film characteristics may change as the film crystallizes. Film compression may occur, while stresses may be relieved as the film is warmed during processing. In an embodiment, temperatures and precursors are selected to aid in forming the crystalline region, while forming an amorphous region on the crystalline region. In an embodiment, the dielectric layer may be annealed prior to forming the top amorphous region on the crystalline region.

A transistor **500** as depicted in FIG. **5** may be constructed including using an embodiment for forming a graded dielectric layer. The graded dielectric layer may be formed by atomic layer deposition. Transistor **500** includes a source region **520** and a drain region **530** in a silicon based substrate **510** where source and drain regions **520**, **530** are separated by a body region **532**. Body region **532** defines a channel having a channel length **534**. A dielectric layer is disposed on substrate **510** as a graded dielectric layer in a manner similar to an embodiment described herein. The resulting dielectric layer forms gate dielectric **540**. Gate dielectric **540** may be realized as a graded dielectric layer formed substantially as monolayers across the dielectric layer having a doping profile that varies across the dielectric layer or formed substantially having a structure profile that varies across the dielectric layer. Gate dielectric **540** may be realized as a graded dielectric layer formed substantially as monolayers across the dielectric layer having a doping profile that varies across the dielectric layer and formed substantially having a structure profile that varies across the dielectric layer. Gate dielectric **540** may contain one or more insulating layers in which at least one layer is a graded dielectric layer. A gate **550** is formed over and contacts gate dielectric **540**. In an embodiment, an amorphous region of gate dielectric is in contact with gate **550**.

An interfacial layer **533** may form between body region **532** and gate dielectric **540**. In an embodiment, interfacial layer **533** may be limited to a relatively small thickness compared to gate dielectric **540**, or to a thickness significantly less than gate dielectric **540** as to be effectively eliminated. Forming the substrate, the gate, and the source and drain regions may be performed using standard processes known to those skilled in the art. Additionally, the

sequencing of the various elements of the process for forming a transistor may be conducted with standard fabrication processes, also as known to those skilled in the art. In an embodiment, gate dielectric **540** may be realized as a gate insulator in a silicon CMOS transistor. Transistor **500** is not limited to silicon based substrates, but may be used with a variety of semiconductor substrates.

FIG. **6** shows an embodiment of a configuration of a floating gate transistor **600** having an embodiment of a graded dielectric layer. Transistor **600** includes a silicon based substrate **610** with a source **620** and a drain **630** separated by a body region **632**. However, transistor **600** is not limited to silicon based substrates, but may be used with a variety of semiconductor substrates. Body region **632** between source **620** and drain **630** defines a channel region having a channel length **634**. Located above body region **632** is a stack **655** including a gate dielectric **640**, a floating gate **652**, a floating gate dielectric **642**, and a control gate **650**. An interfacial layer **633** may form between body region **632** and gate dielectric **640**. In an embodiment, interfacial layer **633** may be limited to a relatively small thickness compared to gate dielectric **640**, or to a thickness significantly less than gate dielectric **640** as to be effectively eliminated.

Gate dielectric **640** includes a graded dielectric layer formed in embodiments similar to those described herein. Gate dielectric **640** may be realized as a graded dielectric layer with an amorphous layer contacting floating gate **652**. Gate dielectric **640** may include one or more dielectric layers in which at least one layer is a graded dielectric layer.

In an embodiment, floating gate dielectric **642** includes a graded dielectric layer formed in embodiments similar to those described herein. Floating gate dielectric **642** may include one or more insulating layers in which at least one layer is a graded dielectric layer. In an embodiment, control gate **650** is formed over and contacts an amorphous layer of floating gate dielectric **642**.

Alternatively, both gate dielectric **640** and floating gate dielectric **642** may be formed containing a graded dielectric layer. Floating gate **652** and floating gate dielectric **642** may be realized by embodiments similar to those described herein with the remaining elements of the transistor **600** formed using processes known to those skilled in the art. In an embodiment, gate dielectric **640** forms a tunnel gate insulator and floating gate dielectric **642** forms an inter-gate insulator in flash memory devices, where gate dielectric **640**, floating gate dielectric **642** gate, or dielectric **640** and floating gate dielectric **642** include a graded dielectric layer. Use of graded dielectric layers for a gate dielectric or a floating gate dielectric is not limited to silicon based substrates, but may be used with a variety of semiconductor substrates.

Embodiments of methods for forming graded dielectric layers may also be applied to forming capacitors in various integrated circuits, memory devices, and electronic systems. In an embodiment, a capacitor **700**, illustrated in FIG. **7**, includes a first conductive layer **710**, a dielectric layer **720** containing a graded dielectric disposed on first conductive layer **710**, and a second conductive layer **730** disposed on dielectric layer **720**. Dielectric layer **720** may include one or more insulating layers in which at least one layer is a graded dielectric layer. In an embodiment, dielectric layer **720** includes a graded dielectric layer having an amorphous layer in contact with second conductive layer **730**. Dielectric layer **720** may be formed by atomic layer deposition or other appropriate technique to form the graded dielectric layer in accordance with embodiments herein. An interfacial layer **715** may form between first conductive layer **710** and

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dielectric layer **720**. In an embodiment, interfacial layer **715** may be limited to a relatively small thickness compared to dielectric layer **720**, or to a thickness significantly less than dielectric layer **720** as to be effectively eliminated. Embodiments for dielectric layer **720** including a graded dielectric layer in a capacitor includes, but is not limited to, dielectrics in DRAM capacitors and dielectrics in capacitors in analog, radio frequency (RF), and mixed signal integrated circuits.

Various embodiments for a graded dielectric film may provide for enhanced device performance by providing devices with reduced leakage current. Additional improvements in leakage current characteristics may be attained by forming one or more layers of a graded dielectric layer in a nanolaminate structure with metal oxides, with non-metal containing dielectrics, or with metal oxides and with non-metal containing dielectrics. The transition from one layer of the nanolaminate to another layer of the nanolaminate provides further disruption to a tendency for an ordered structure in the nanolaminate stack.

FIG. **8** depicts a nanolaminate structure **800** for an embodiment of a dielectric structure including a graded dielectric layer. Nanolaminate structure **800** includes a plurality of layers **805-1**, **805-2** to **805-N**, where at least one layer contains a graded dielectric layer. In an embodiment, nanolaminate structure **800** is formed by atomic layer deposition. The effective dielectric constant associated with nanolaminate structure **800** is that attributable to  $N$  capacitors in series, where each capacitor has a thickness defined by the thickness of the corresponding layer. By selecting each thickness and the composition of each layer, a nanolaminate structure can be engineered to have a predetermined dielectric constant. In an embodiment, nanolaminate structure **800** has conductive contacts **810** and **820** to provide electrical conductivity to the electronic device structure in which it is formed. Embodiments for structures such as nanolaminate structure **800** may be used as nanolaminate dielectrics in NROM flash memory devices as well as other integrated circuits.

Transistors, capacitors, and other devices having graded dielectric films formed by the methods described above may be implemented into memory devices and electronic systems including information handling devices. Embodiments of these information handling devices may include telecommunication systems, wireless systems, and computers. Further, embodiments of electronic devices having graded dielectric films may be realized as integrated circuits.

FIG. **9** illustrates a diagram for an electronic system **900** having one or more devices having a graded dielectric layer in accordance with various embodiments. Electronic system **900** includes a controller **905**, a bus **915**, and an electronic device **925**, where bus **915** provides electrical conductivity between controller **905** and electronic device **925**. In various embodiments, controller **905**, electronic device **925**, or controller **905** and electronic device **925** include an embodiment for a graded dielectric layer. Electronic system **900** may include, but is not limited to, information handling devices, wireless systems, telecommunication systems, fiber optic systems, electro-optic systems, and computers.

FIG. **10** depicts a diagram of an embodiment of a system **1000** having a controller **1005** and a memory **1025**. Controller **1005**, memory **1025**, or controller **1005** and memory **1025** may include an embodiment of a graded dielectric layer in accordance with the teachings herein. System **1000** also includes an electronic apparatus **1035** and a bus **1015**, where bus **1015** provides electrical conductivity between controller **1005** and electronic apparatus **1035**, and between controller **1005** and memory **1025**. Bus **1015** may include an

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address, a data bus, and a control bus, each independently configured. Alternatively, bus **1015** may use common conductive lines for providing address, data, or control, the use of which is regulated by controller **1005**. Alternatively, bus **1015** may use common conductive lines for providing address, data, and control, the use of which is regulated by controller **1005**. In an embodiment, electronic apparatus **1035** may be additional memory configured similar as memory **1025**. An embodiment may include an additional peripheral device or devices **1045** coupled to bus **1015**. In an embodiment, controller **1005** is a processor. In an embodiment, controller **1005** is a processor having a memory. Any of controller **1005**, memory **1025**, bus **1015**, electronic apparatus **1035**, and peripheral device devices **1045** may include a graded dielectric layer. System **1000** may include, but is not limited to, information handling devices, telecommunication systems, and computers.

Peripheral devices **1045** may include displays, additional storage memory, or other control devices that may operate in conjunction with controller **1005**. Alternatively, peripheral devices **1045** may include displays, additional storage memory, or other control devices that may operate in conjunction with controller **1005**, memory **1025**, or controller **1005** and memory **1025**.

Memory **1025** may be realized as a memory device containing a graded dielectric layer in accordance with various embodiments. It will be understood that embodiments are equally applicable to any size and type of memory circuit and are not intended to be limited to a particular type of memory device. Memory types include a DRAM, SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as Synchlink or Rambus DRAMs and other emerging DRAM technologies.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of embodiments of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive, and that the phraseology or terminology employed herein is for the purpose of description and not of limitation. Combinations of the above embodiments and other embodiments will be apparent to those of skill in the art upon studying the above description. The scope of the present invention includes any other applications in which embodiment of the above structures and fabrication methods are used. The scope of the embodiments of the present invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A device comprising:

a metal oxide doped with a dopant, the metal oxide having a top surface and a bottom surface, wherein the metal oxide has varying amounts of the dopant across the metal oxide between the top and bottom surfaces with concentrations of the dopant at the top surface and at the bottom surface each being greater than a concentration of the dopant in a center of the metal oxide between the top surface and the bottom surface, the dopant including a metal dopant and/or silicon.

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2. The device of claim 1, wherein the metal oxide comprises monolayers across the metal oxide.

3. The device of claim 1, wherein the dopant includes a metal dopant.

4. The device of claim 1, further comprising first and second electrodes;

wherein the top and bottom surfaces are in contact with the first and second electrodes, respectively.

5. The device of claim 3, wherein the dopant concentration at the center of the metal oxide is less than a concentration of the metal dopant in any other part of the metal oxide.

6. The device of claim 1, wherein the metal oxide includes a binary metal oxide.

7. The device of claim 6, wherein the metal oxide includes any one of Lanthanide oxides, HfO<sub>2</sub>, ZrO<sub>2</sub> and TiO<sub>2</sub>.

8. The device of claim 3, wherein the metal dopant includes more than one type of metal dopant.

9. The device of claim 4, wherein the metal oxide between the first and second electrodes is a dielectric layer of a capacitor.

10. A device comprising:

a metal oxide doped with a dopant, the metal oxide having a top surface and a bottom surface, wherein the metal oxide has varying amounts of the dopant across the metal oxide between the top and bottom surfaces with concentrations of the dopant at the top surface and at the bottom surface each being greater than a concentration of the dopant in a center of the metal oxide between the top surface and the bottom surface, wherein the center of the metal oxide includes a crystalline layer, and each of the first and second interfaces includes an amorphous layer.

11. A device comprising a capacitor, the capacitor including a dielectric layer between first and second electrodes, the dielectric layer including a metal oxide doped with a dopant, the metal oxide comprising:

a first interface region on a side of the first electrode, the first interface region having a first concentration of the dopant;

a second interface region on a side of the second electrode, the second interface region having a second concentration of the dopant; and

a intermediate region between the first and second interface regions, the intermediate region having a third concentration of the dopant, the third concentration

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being lower than each of the first and second concentrations, wherein the dopant includes a metal dopant and/or silicon.

12. The device of claim 11, wherein the metal oxide comprises monolayers across the metal oxide.

13. The device of claim 11, wherein the metal oxide includes a binary metal oxide.

14. The device of claim 13, wherein the metal oxide includes any one of Lanthanide oxides, HfO<sub>2</sub>, ZrO<sub>2</sub> and TiO<sub>2</sub>.

15. The device of claim 11, wherein the dopant includes a metal dopant.

16. The device of claim 15, wherein the metal dopant includes more than one type of metal dopant.

17. A device comprising a capacitor, the capacitor including a dielectric layer between first and second electrodes, the dielectric layer including a metal oxide doped with a dopant, the metal oxide comprising:

a first interface region on a side of the first electrode, the first interface region having a first concentration of the dopant;

a second interface region on a side of the second electrode, the second interface region having a second concentration of the dopant; and

a intermediate region between the first and second interface regions, the intermediate region having a third concentration of the dopant, the third concentration being lower than each of the first and second concentrations, wherein the intermediate region of the metal oxide includes a crystalline layer, and each of the first and second interface regions includes an amorphous layer.

18. A device comprising a transistor, the transistor including a gate dielectric film having a first interface toward a gate electrode and a second interface toward a channel region, the gate dielectric film including a metal oxide doped with a dopant, wherein each of the first and second interfaces is larger in a concentration of the dopant than a center of the metal oxide between the first and second interfaces, the dopant including a metal dopant and/or silicon.

19. The device of claim 18, wherein the metal oxide includes a binary metal oxide.

20. The device of claim 18, wherein the dopant includes a metal dopant.

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