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A TCAD Study on Achieving Better Gate Oxides by Using κ-Graded Stacking for Trigate FinFETs

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Abstract: One of the most important developments in metal-oxide-semiconductor field effect transistors (MOS-FETs) since their creation in the 1960s is the three-dimensionalized variant, known as FinFET, which creates a vertical wrapping of the semiconducting channel by conformal gate electrodes. Nanoscaled dielectric materials enable semiconductor-to-gate insulation function in all FinFET topologies. Yet there exists no simple binary oxide dielectric between the dielectric constant (κ) greater than 35 (of Nb_2O_5) and less than 95 (of TiO_2). Here emerges the opportunity to generate materials with κ in the range of 35-95 through utilization of κ-grading in gate dielectrics. Studies show multi-material stacked gate-oxides continue to demonstrate their potential as semiconductor-to-gate insulators, yet in these studies the effective dielectric constant (κ_{EFF}) calculation step and effect of κ-ordered stacking is vastly ignored. In this paper, taking these two factors into account, we present simulation results obtained using TCAD tools for a 3-D silicon on insulator (SOI) n-FinFET structure with various gate dielectrics with "κ-graded stacking" in FinFET geometries by utilizing of the dielectric stack. In conjunction with studies on stacked laminates of gate-oxides like SiO_2, Al_2O_3 and HfO_2, this study further explores role of ordered stacking of oxide laminates towards gate metal with increasing κ value, artificially forming a κ-graded functionally graded material (FGM). We show k-graded gate oxides decrease adverse interface trap effects and decrease gate-channel leakage currents. A numerical analysis via introduction of a custom benchmark is conducted to show viability of usage of FGM structures against conventional single layer high-κ dielectrics on 14-nm FinFET geometry. Impact on key electrical performance parameters are analyzed using SILVACO ATLAS TCAD as device simulation tool. Within 13 different 2- and 3-stage κ-graded stacked gate-oxide combinations some FinFET structures with κ-graded gate oxides (κG-FinFET) promise lesser gate leakage current up to 53 times, lesser drain induced barrier lowering (DIBL) up to %38.2, lesser subthreshold slope (SS) up to %7.6, lower drain off current (I_{OFF}) up to 2 decades, higher drain on current (I_{ON}) up to %62, higher I_{ON}/I_{OFF} up to 45 times and lesser threshold voltage (V_{TH}) up to %19.2, with respect to the FinFET of same dimensions with a single layer HfO_2 gate dielectric.

Keywords: κ-graded gate oxides, Technology Computer-Aided-Design (TCAD) Simulation; stacked high-κ gate-oxide dielectrics, Functionally Graded Material (FGM); Junctionless Thin Film Transistor (JLTFT); Fin-Field Effect Transistor (FinFET); Drain Induced Barrier Lowering (DIBL); Subthreshold Slope (SS); Threshold Voltage (V_{TH}); I_{ON}/I_{OFF} ratio.

1. Introduction

Stacked laminates of gate-oxides on FinFETs have been investigated in several research works. Lorenzo et.al proposed a gate engineered oxide stack silicon on insulator (SOI) FinFET device with a high-κ dielectric gate oxide stack structure, which improved the analog and RF performance of the device compared to standard single gate oxide

structures [1]. Gangwani et.al analyzed the temperature performance of a stacked oxide top-bottom gated junctionless FinFET, which showed enhanced output performance and reduced short channel effects compared to conventional junctionless FinFET [2]. Das et.al proposed a dual-material-gate dual-stacked-gate dielectrics gate-source overlap Germanium FinFET with low leakage current, high on drain current, and high ratio of on current to off current [3].

INTRODUCTION ın yapısı aynı https://doi.org/10.1038/s41467-020-15096-0 daki gibi olsun

FGM lerin yönü önemli mi yorumla ! (Önce TiO2 başlasaydık ne olacaktı ?)

- especially when methods exist to calculate the equivalent dielectric constant of the epsilon-graded stacked FGM materials.

HfO_2 thin films have wide band gap of ≈ 5.8 eV, high dielectric constant (κ ≈ 25) and suitable band offset values relative to Si substrate. In addition to their excellent thermodynamic and chemical stability, HfO_2 has been strongest candidate material for replacing single layer SiO_2 gate dielectrics. (reference koy) however, Among existing methods Maxwell-Garnet equation [4] for calculation of effective κ for 2-layer dielectrics. As we need 3-layer effective κ calculation we need to derive the two equations for 3-layer dielectrics.

In this paper we introduce functional gate dielectrics consisting of 2- or 3- layer known dielectrics working on FinFETs, which might be candidate for fabrication on top of Si-channeled FinFETs. Similar work and simulations were addressed in papers [5], [6], [7].,

Modified Penn Model [8], [9] is used to calculate the dielectric constant of thin nanolaminate material forming each FGM laminate, using their bulk dielectric constant κ_b, bandgap energy E_G, high frequency dielectric constant κ_∞ and its Fermi wave vector K_f. Maxwell-Garnet (MG) approximation [4] is selected to calculate the effective dielectric constant (κ_{EFF}) for the 2-and 3-layered FGM dielectrics. Quantum tunneling model and Hot Electron / Hot Hole Injection (HEI-HHI) models [10] are used to model gate leakage current within SILVACO ATLAS/Deckbuild simulation tool and results were found to be consistent with experimental results within [11] with systematically varying thickness of mentioned dielectric layers to form a graded structured 3 nm-thickness FGM gate dielectrics. FinFET Buried Oxide (BOX) material was kept as Al_2O_3 through all simulations.

In this work, simulations were performed with single and double FGM dielectric materials for trigate FinFET structure. Our research focused on conducting a simulation-based study of FinFETs since their introduction in the year 2000 [12], performance of FinFET technology, including analytical modeling and simulation of FinFET devices [13], the influence of fin geometry on corner effects in multifin dual and tri-gate SOI-FinFETs [14], benchmarking of FinFET, nanosheet, and nanowire FET architectures for future technology nodes [15], the analog performance analysis of stacked oxide top-bottom gated junctionless FinFET [2] and a detailed study of single-material gate, double-material gate, and triple-material gate FinFETs were carried out [16]. In-depth analysis of typical types of FinFETs were presented in [17] with which we tried to match the terminology and abbreviations within that paper.

Performance Parameters: threshold voltage (**V_{TH}**), on-state current (**I_{ON}**), off-state current (**I_{OFF}**), drain-induced barrier lowering (**DIBL**) and subthreshold slope (**SS**), **I_{ON}/I_{OFF}** ratio and gate metal-to-silicon leakage current (**I_G**).

2. Description of Device Structure

The 3D Technology Computer-Aided Design (TCAD) structure for FinFETs is shown in Fig. 1.

Using SILVACO ATLAS for device simulation, we start with SiO_2, Al_2O_3, HfO_2, La_2O_3 and TiO_2 as single layer gate dielectrics of 3 nm thickness (t_{ox}) for a 14nm channel (fin) length (L_{FET}), 2 nm channel width (W_{FET}), 5 nm channel height (h_{fin}) FinFET structure, then formed 13 different FGM materials with systematically varying thickness of mentioned dielectrics to form a graded structured 3 nm-thickness gate oxide dielectric. With thickness of 3 nm, BOX material (Figure 1) is kept as Al_2O_3 and never changed through simulations. Equal doping concentration of $5x10^{19}$ cm^{-3} is used source - drain channel region.

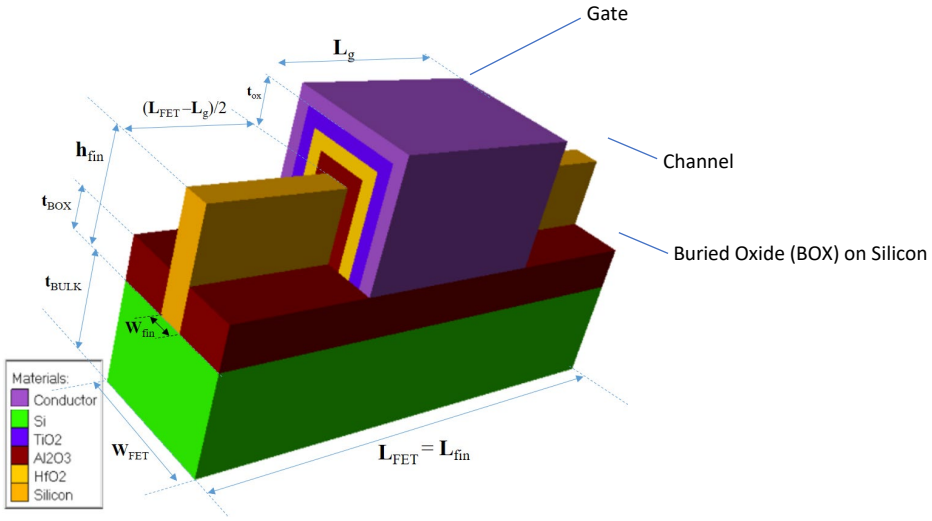

Figure 1. Proposed 3-material FGM gate oxide dielectric based **G**κ-FinFET

Table 1. Proposed **G**κ-FinFET properties.

Property	Value	Note / Abbreviation
Channel (Fin) Length	14 nm	L_{fin}
Gate thickness	10 nm	Tg
Channel (Fin) Width	2 nm	W_{fin}
Gate Length	14 nm	L_g
Fin Width	2 nm	W_{fin}
Fin Height	5 nm	H_{fin}
Channel Concentration	$5x10^{19}$ cm^{-3}	N_d
Gate work function	5 eV	ϕ_w
FET Length	34 nm	L_{FET}
FET Width	10 nm	W_{FET}
Total Gate Oxide thickness	3 nm	t_{ox}
BOX Thickness	3 nm	t_{BOX}
BOX material	Al_2O_3	-
Bulk Si Thickness	10 nm	t_{BULK}

Figure 2. depicts the cross-sectional view of the G**κ**-FinFET implemented using stack approach. The design parameters considered for the device are depicted in Table 1. Both the device structures are of n-type FinFET, comprising of two gates, control gate and polarity gate which are isolated in nature. The control gates and the polarity gates are used for modulation of effective tunnelling barrier width. The Work function of 5 eV, is applied at the control gate thus converting n + layer under the control gate into intrinsic region and a work function of 5.93 eV is applied at the polarity gate, thus, converting n +

layer under polarity gate into p+, which acts as the source region. Thus, n + −n + −n + region is converted into n + −i–p + region which works as n + −i–p + FinFET. The work function of 5.93 eV (Platinum) has been used at the source metal electrode in order to form the source region through concept of charge plasma, by inducing approximately 1019/cm3 of hole concentration on the silicon surface at the source side of device [26]. Similarly, the work function of 3.9 eV has been used at drain side, to form the drain region through charge plasma concept, by inducing electron concentration on silicon surface at drain side of device. All the parameters for FinFET same, with one main difference. In the case of the SO PG FinFET, (SiO2 + HfO2) stack is used, while in the case of PG FİNFET, only SiO2 stack is used. Both the positive and negative ITCs are applied at the silicon oxide interface.

The fixed charge density of ITCs is taken to be Nf = ±1.0 × 1012 /cm2) [25, 27, 28]. It should be noted that in the simulation, INTERFACE statement from [29] has been considered to analyze the density of interface fixed charges and their position available at interface of silicon and oxide layer.

INTERFACE statement has been implemented in Silvaco TCAD as follows:

INTERFACE QS=+1e12 x.min=0.020 x.max=0.040 y.min=- 0.0030 y.max=-0.0020.

Here QS represents the interface charge density, and it can be positive or negative, x represents the channel length position in μm and y represents channel width position in μm. Although the presence of interface traps is there at the interface of HfO2 and oxide layer in SO PG FinFET and will be absent in case of PG FinFET, but in present manuscript only the ITCs along the channel length at the silicon and oxide interface has been considered. The ITCs at the HfO2 and oxide interface has been neglected because, in case of TFETs mainly the impact of drain junction and the tunneling junction is there on the device behavior [23]. The spacer thickness, which is 5 nm between polarity gate and source and electrodes, finds how the gate field is closer to the tunneling path towards the source side. Thus, while finding the tunneling probability it becomes an important parameter. The impact of ITCs on the dc performance, analog/RF and linear distortion performance of both the PG FinFET and SO PG FinFET has been studied in this work. 2-D Silvaco Atlas device simulator has been used to conduct all the simulations. Shockley Read Hall and Auger models have been used in order to account for presence of highly doped impurity atoms in channel and minority recombination region. Nonlocal band-to-band tunneling (BTBT) model [30, 31], has been used, which analyses the rate of generation of carriers at each point. For implementing this model, region of quantum tunneling are defined at interface of source and channel and drain and channel interface, in order to account for ON state tunnelling of carriers, and ambipolar nature of FİNFET respectively. Use of bandgap narrowing model is done to account for high doping concentration in the channel region [20]. The quantum confinement model has also been applied, which is incorporated by using the Schrodinger Poisson model. The nonlocal BTBT model utilizes the isotropic tunneling effective mass of hole as well as the electron [32]. This model provides the solutions of Schrodinger's equation, for the energies of the bound states in conduction bands and valence bands, as well as the solution of Poisson equation for electric potential. The Schrodinger's equation solution also determines the quantum electron density calculations. Quantum electron density calculations have to be solved for wave function as well as magnitude of Eigen state energy at each cross section of the device. Fermi Dirac model has been used to calculate electron and hole concentrations, as well as wave function and Eigen energy [32]. These parameters have been utilized for calculating the potential using Poisson's equation [32]. Schottky tunnelling model has also been used. The nonlocal trap-assisted tunneling (TAT) model has been incorporated in order to account for TAT, which is based on the Wentzel–Kramer–

Brillouin (WKB) transmission coefficient with an exact tunneling barrier [33]. This model utilizes the material parameters that is tunneling mass of hole considered as 0.16 and tunneling mass of electron considered as 0.21 [34].

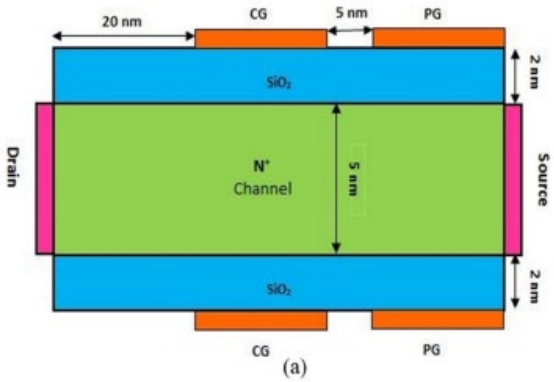

Figure 2. Proposed 3-material FGM gate oxide dielectric based FinFET

Figure 1. (a) View of cross-sectional for e-graded FinFET

(b)
View of cross-sectional for (a) PG JL-TFET (b) SO PG JL-TFET (c) Fabrication steps for SO PG JL-TFET

Fabrication Process

Fabrication of the FinFET can be done using nonplanar technologies. The procedure of fabrication as shown in Fig. 1(c) is explained as follows:

Fabrication of channel can be done by Bosch processes or deep reactive ion etching [32]; (ii) Deposition of gate oxide can be done by using low pressure chemical vapor deposition (LPCVD) [32]; (iii) The patterning of window, which defines region of tunneling can be done using plasma etching [35]; (iv) Successively, deposition of HfO2

layer can be done by using Atomic Layer Deposition at 200° C, which can be followed by annealing in O2 ambient [36]. (v) Formation of source/drain contact can be done by growing it epitaxially over the substrate [31]; Successively, patterning of the polarity gates (PGs) can be done by using the process of e-beam lithography [32]; and (vii) Finally, the spacer formation and contact deposition can be done [32].

3. Materials and Methods

As we target to prove that FGM gate oxide dielectric structures behave and perform better than single material dielectric structure in FinFET design, our method will be 5 steps. We need to analyze, model and evaluate the nanoscaled dielectric structures decreasing thickness will reduce the bulk capacitance and dielectric constant of the dielectric. First in IIIa, Modified Penn Model [8], [9] is used to calculate the dielectric constant of thin nanolaminate material forming each FGM laminate, using their bulk dielectric constant κ_b, bandgap energy E_G, high frequency dielectric constant κ_∞ and its Fermi wave vector K_f. In part IIIb thru IIIc, Maxwell-Garnet (MG) approximation [4] is selected to calculate the effective dielectric constant (κ_{EFF}) for the 2-and 3-layered FGM dielectrics. In IIId and IIIe, FinFET model in Figure 1 is implemented via ATLAS language and Hot Electron / Hot Hole Injection (HEI-HHI) model [10] is used to model gate leakage current within SILVACO ATLAS/Deckbuild simulation tools are used to calculate with experimental results within [11], with systematically varying thickness of mentioned dielectric layers to form a graded structured 3 nm-thickness FGM gate dielectrics. Eighteen different FinFET model simulations are performed in Silvaco Atlas Deckbuild, first five models include single material gate oxide dielectrics in Table 4A and subsequent thirteen models include FGM dielectrics as gate-oxide (in Table 4B). Thru IIIf and IIIg, key electrical performance parameters like threshold voltage (**V_{TH}**), on-state current (**I_{ON}**), off-state current (**I_{OFF}**), drain-induced barrier lowering (**DIBL**) and subthreshold slope (**SS**), **I_{ON}/I_{OFF}** ratio and gate metal-to-silicon leakage current (**I_{GL}**) are selected and evaluated for each simulation. We also design a customized figure of merit in order to justly evaluate each FinFET performance with respect to each other. Here we present details each step as below:

3.1. Thickness Dependence of Under Quantum Confinement Effects

Theoretical foundation for constructing a κ-graded FGM is given in US Patent 8110469 by Gealy et.al. [18] and we model our gate oxide for FinFET as below:

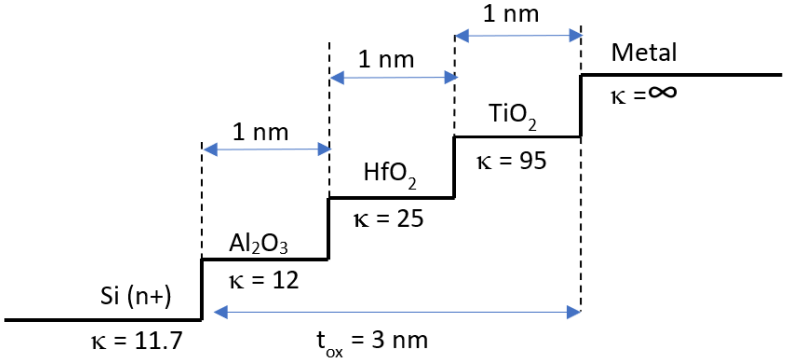

Figure 2. Stepwise Grading Profile for an example FGM (FGM-H in Table 4B.) as gate oxide dielectric.

Gate oxide dielectric constant has to be evaluated for according to the formula, Equation-1,

$$\kappa_{ox} = 1 + \frac{\kappa_b - 1}{1 + \left(\frac{\kappa_\infty 2\pi}{K_f t_{ox}}\right)^2}$$

where $\kappa_b$is the bulk dielectric constant, κ_∞ is the high frequency dielectric constant, K_f is Fermi wave vector, t_{ox} is the thickness of the nanoscaled dielectric material [8].

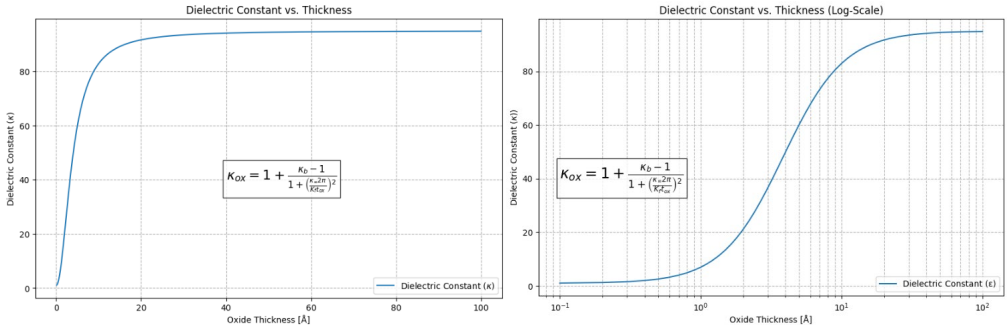

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Figure 3. Modified Penn Model for dielectric constant against thickness applied to TiO_2 [8], [9].

For silicon (Si), it has been shown that for thicknesses greater than 10 Å (1 nm), bulk κ_b can be considered to be unchanged and equivalent to κ_{ox} [9]. If t_{ox} is less than 10 Å then we need to consider generalized Penn model [19] for modelling dielectric constant κ as against thickness, under quantum confinement effects for nanolaminates for each FGM's κ_{EFF} to be calculated correctly. As we herein try to model nanolaminates around 5-30 Å, we calculated κ_{ox} of interlayer nanolaminate according to Equation-1. This can be numerically further fitted to the Equation-2 in [19] ;

$$\kappa_{ox} = 1 + \frac{\kappa_b - 1}{1 + \frac{1.7}{t_{ox}^{1.8}}}$$

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and when we calculate the resultant kappa κ_{ox} of same material due to its nanolaminate thickness t_{ox} and observe the significant loss in dielectric effect when we observe Table-2. This numerical approximation is depicted in Figure 4, showing that in orders of few nanometers nanolaminate TiO_2 thickness, kappa reduction is significant.

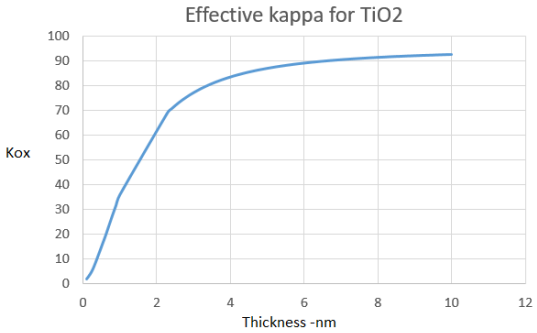

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Figure 4. A numerical approximation for Penn Model evaluated by Equation-2.

Table 2. Bulk dielectric constant κ_b and resultant oxide kappa κ_{ox} with respect to nanolaminate thickness t_{ox} of dielectric materials calculated with Equation-2.

Material	SiO2	Al2O3	HfO2	La2O3	TiO2
κ_b	3,90	12,00	25,00	30,00	95,00
κ_{ox} in 0.5nm	1,42	2,59	4,47	5,19	14,58
κ_{ox} in 1nm	2,07	5,07	9,89	11,74	35,81
κ_{ox} in 1.5nm	2,59	7,05	14,19	16,94	52,67
κ_{ox} in 2nm	2,95	8,39	17,13	20,49	64,16
κ_{ox} in 2.5nm	3,19	9,29	19,09	22,86	71,85
κ_{ox} in 3nm	3,35	9,90	20,43	24,48	77,09

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3.2. Modelling Oxide Nanolaminates as FinFET Gate oxide Dielectrics

In order to isolate the gate metal and form a proper electric field to control the drain current, gate dielectrics are of great importance. Dielectric constants (κ) of some selected gate oxides vary from 3.9 to 95 and their respective bandgaps vary from 9 eV down to 3.5 eV in Table 3.

Table 3. Bandgap and dielectric constant for simple binary oxides used in this paper [22], [23.]

Material	Dielectric Constant (κ)	Bandgap (eV)
SiO_2	3,9	9
Al_2O_3	9	8,8
HfO_2	25	5,8
$La2O_3$	30	6
TiO_2	95	3,5

HfO_2 thin films have wide band gap of ≈ 5.8 eV, high dielectric constant (κ ≈ 25) and suitable band offset values relative to Si substrate. In addition to their excellent thermodynamic and chemical stability, HfO_2 has been strongest candidate material for replacing single layer SiO_2 gate dielectrics. There exists no simple binary oxide dielectric between the κ greater than 35 (of Nb_2O_5) and less than 95 (of TiO_2). Thus there starts the possibility and opportunity to generate materials with κ in the range of 35-95 through FGMs, that have the potential to show better performance properties than HfO_2, especially when we utilize a method to calculate the equivalent dielectric constant of the stacked FGM materials. Among existing methods Maxwell-Garnet equation [4] for calculation of effective for 2 layer dielectrics. As we need 3-layer effective calculation we need to derive the two equations for 3-layer dielectrics as follows:

3.3. κ_{EFF} Derivations for 3-Stage FGM with Materials A,B,C

When two layers or phases of dielectric materials are deposited on top of each other, calculation of their effective or resultant dielectric constant of this serially connected sheets of two dielectric materials, also called as, effective dielectric constant for A-B material (effective κ_{AB}) would be calculated by two models, first by Maxwell-Garnet approximation model [4], [22] as Eq.2;

$$\kappa_{EFF,AB} = \kappa_B \frac{\kappa_A + 2\kappa_B + 2f(\kappa_A - \kappa_B)}{\kappa_A + 2\kappa_B - f(\kappa_A - \kappa_B)}$$

where κ_A, κ_B are dielectric constants for material A and B and f is the volumetric filling factor for material A and $(1 - f)$ is the volumetric filling factor for material B in the two phase dielectric system of Fig 5.

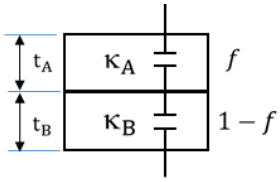


Figure 5. Two phase dielectric system connected in series.

To extend this theory for a three-phase system, we need to consider additional complexities due to the interaction between three different dielectric materials. If we denote the dielectric constants of the three materials as κ_A, κ_B , and κ_C and their respective volumetric filling factors as f_A, f_B, and f_C with $f_A + f_B + f_C = 1$, we need to derive an expression that considers all three materials. Thus we can;

- Calculate the effective dielectric constant κ_{AB} for materials A and B using the Maxwell-Garnett equation.
- Consider κ_{AB} as one material and apply the Maxwell-Garnett equation again with κ_{AB} and κ_C to find the overall effective dielectric constant κ_{EFF}, with $f_{AB} + f_C = 1$, finally as Eq.3,

$$\kappa_{EFF,ABC} = \kappa_C \frac{\kappa_{AB} + 2\kappa_C + 2f_{AB}(\kappa_{AB} - \kappa_C)}{\kappa_{AB} + 2\kappa_C - f_{AB}(\kappa_{AB} - \kappa_C)}$$

Table 4A. Control Group: Thickness and bulk □□values and calculated (modified Penn model) dielectric constants values of 5 single material gate dielectrics for 3 nm thickness.

	SiO2	Al2O3	HfO2	La2O3	TiO2
κ_b value	3,9	12	25	30	95
κ_{ox} in 3nm	3,35	9,9	20,43	24,48	77,09

Table 4B. FGM Group: Thickness and κ_{EFF} (applying modified Penn + MG model) values of 13 FGM gate oxide dielectrics between SiO_2 and TiO_2, shown as lower and upper limits of achievable κ_{EFF} within 3nm material thickness.

Material	SiO2	FGM-A	FGM-B	FGM-C	FGM-D	FGM-E	FGM-F	FGM-G	FGM-H	FGM-J	FGM-K	FGM-L	FGM-M	FGM-N	TiO2
SiO2 thickness (nm)	3	1	1	0,5	1	0	0,5	0	0	1	1,5	0	0	0	0
Al2O3 thickness (nm)	0	1	1	0,5	0	0,5	0	0,5	1	0,5	0	0	0,5	0	0
HfO2 thickness (nm)	0	1	0	2	1	2	2,5	2,5	1	0	0	1,5	0,5	0,5	0
TiO2 thickness (nm)	0	0	1	0	1	0,5	0	0	1	1,5	1,5	1,5	2	2,5	0
Total Thickness (nm)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
κ_{EFF}	**3,35**	**4,26**	**9,39**	**9,57**	**10,57**	**12,30**	**14,15**	**14,55**	**16,39**	**18,98**	**19,28**	**27,02**	**33,88**	**52,93**	**77,09**

3.4. FinFET Modelling in Silvaco ATLAS Deckbuild Tool

We start with modeling our FinFET in Silvaco's Atlas/Deckbuild. The family of such tools were used in many research to design and simulate the FinFET devices. The ATLAS Deckbuild simulation employing many standard recombination and continuity models like Shockley-Read-Hall, Schrödinger and Auger; used widespread for 2D/3D simulations of normal or heterogated single, double or triple-gated FinFETs [13],[16],[5].

3.5. Gate Leakage Current Modelling

In devices that have a metal-insulator-semiconductor (MIS) formation, the conductance of the insulating film would ideally be considered as zero. However, for the sub 0.5um generation of MOS devices there is considerable conductance being measured on the gate contacts [10]. In our case we used two lines of code for proper solvers to be activated in ATLAS/Deckbuild given in Appendix A, among tunneling-through-dielectric models available we used the hot electron/hole injection (HEI-HHI) tunneling model

within ATLAS tool [10], so that gate-to-dielectric leakage current was properly and realistically modeled, which gave most accurate results comparable with [11].

Table 5. Summary of used models for tunneling and carrier injection for gate-dielectric leakage current in ATLAS [4.]

Model	Syntax	Notes
Band-to-Band (standard)	BBT.STD	For direct transitions. Required with very high fields.
Concannon Gate Current Model	N.CONCAN P.CONCAN	Non-local gate model consistent with Concannon substrate current model.
Direct Quantum tunneling (Electrons)	QTUNN.EL	Quantum tunneling through conduction band barrier due to an insulator.
Direct Quantum tunneling (Hole)	QTUNN.HO	Quantum tunneling through valence band barrier due to an insulator.
Fowler-Nordheim (electrons)	FNORD	Self-consistent calculation of tunneling through insulators. Used in EEPROMs.
Fowler-Nordheim (holes)	FNHOLES	Same as FNORD for holes.
Klaassen Band-to-Band	BBT.KL	Includes direct and indirect transitions.
Hot Electron Injection	HEI	Models energetic carriers tunneling through insulators. Used for gate current and Flash EEPROM programming.
Hot Hole Injection	HHI	HHI means hot hole injection.

3.6. Choice of Performance Metrics

Our performance metrics were selected as:

- **I_G**, On-state gate leakage Current, in Amperes, leaks from gate metal through dielectric into the channel, when V_{GS} = 0.75V in our case, needs to be minimized.
- **I_{ON}**, On-state Drain Current, in Amperes, when $V_{DS} = V_{DD}$ (=1.2V in our case) and $V_{GS} = V_{DD}$, needs to be maximized.
- **I_{OFF}**, Off-state Drain Current, in Amperes, when $V_{DS} = V_{DD}$ and V_{GS} = 0.0V, needs to be minimized.
- **I_{ON}/I_{OFF} Ratio**, unitless, accepted and powerful measure of TFT design quality, needs to be maximized.
- **V_{TH}**, Threshold Voltage, in Volts, the minimum V_{GS} voltage that drain current I_D slightly exceeds a limit current ($1x10^{-7}$ A in our case) significant for the design, needs to be minimized.
- **SS**, Subthreshold Slope, in mV/decade, change in the gate voltage required to decrease the drain current I_D by one decade, $SS = \Delta V_{GS}/\Delta \log(I_D)$, needs to be minimized.
- **DIBL**, Drain-Induced Barrier Lowering, in mV/V, represents the drain voltage V_{DS} influence on the threshold voltage V_{TH}, defined as $DIBL = |\Delta V_{TH}|/|\Delta V_{DS}|$, needs to be minimized.

as these are the primary parameters for evaluation of thin film transistors' performance. [23]

3.7. Selection Process for the FGM – Creation of a Custom Figure of Merit

At the end of calculation process, we introduce and propose a unitless figure of merit as Equation-4:

$$FOM_{FET} = \frac{97.62(log(I_{ON}/I_{OFF}))^3\,(-log(I_{GL}))^3}{(10V_{TH})^3\,.\,DIBL^2\,.\,SS}$$

with which we can evaluate the overall performance of FinFET under consideration. We developed this figure of merit that equally and mostly cares for I_{GL}, I_{ON}/I_{OFF} ratio and V_{TH}, gives less importance to DIBL and even lesser importance to SS. Overall FOM value is multiplied by an arbitrary constant 97.62 to achieve best performing FinFET to appear with FOM_{FET} value equals to 100 and all other performance values to be normalized

between 1 and 100. We compared the FOM_{FET} values of all single and FGM dielectric configurations so that it may help better to decide the selection among all configurations.

4. Results and Discussion

4.1. I_D - V_{GS} Transfer Characteristics

Figure 6. shows the drain current (Id) versus gate-source voltage (Vgs) characteristics for the FinFET device we examined with various gate dielectric materials. The threshold voltage is the point where the curve starts to steeply rise, which is a critical parameter for switching characteristics. The graph includes TiO_2, La_2O_3, HfO_2, Al_2O_3, and SiO_2 as gate dielectrics. These materials are high-k dielectrics, with the exception of SiO2, which is a traditional dielectric material with a lower dielectric constant. TiO_2 seems to have a higher on-current for the same gate voltage compared to the others, which may suggest better channel formation or a higher dielectric constant, which can modify the effective channel thickness. The choice of dielectric material significantly impact device performance. Higher-k materials like HfO_2 and TiO_2 may allow for thinner dielectrics, which can enhance gate control and reduce leakage currents, while also allowing for scaling down the device dimensions.

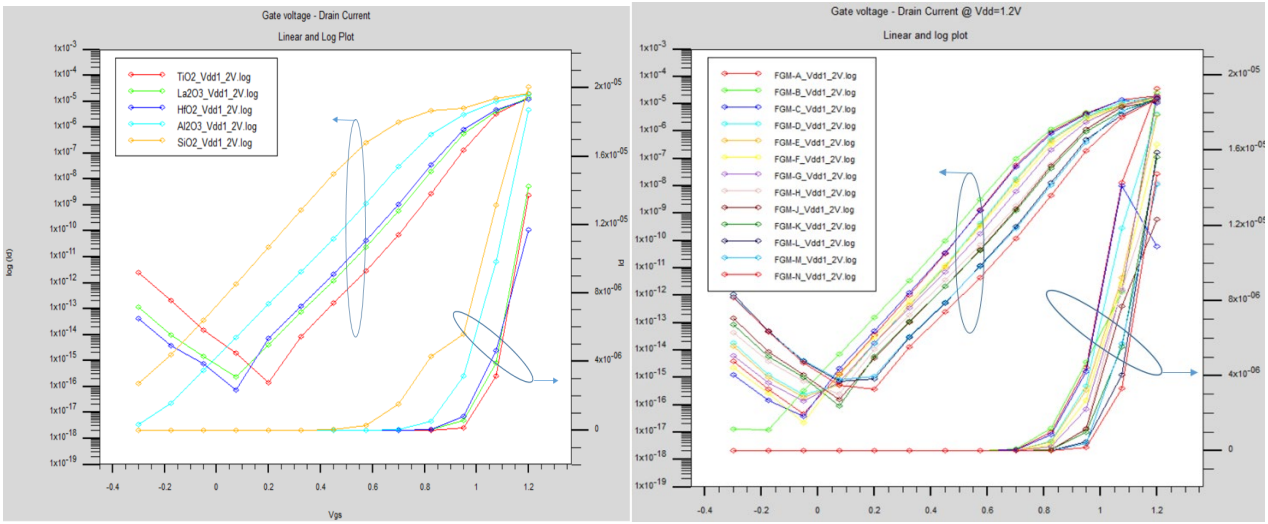
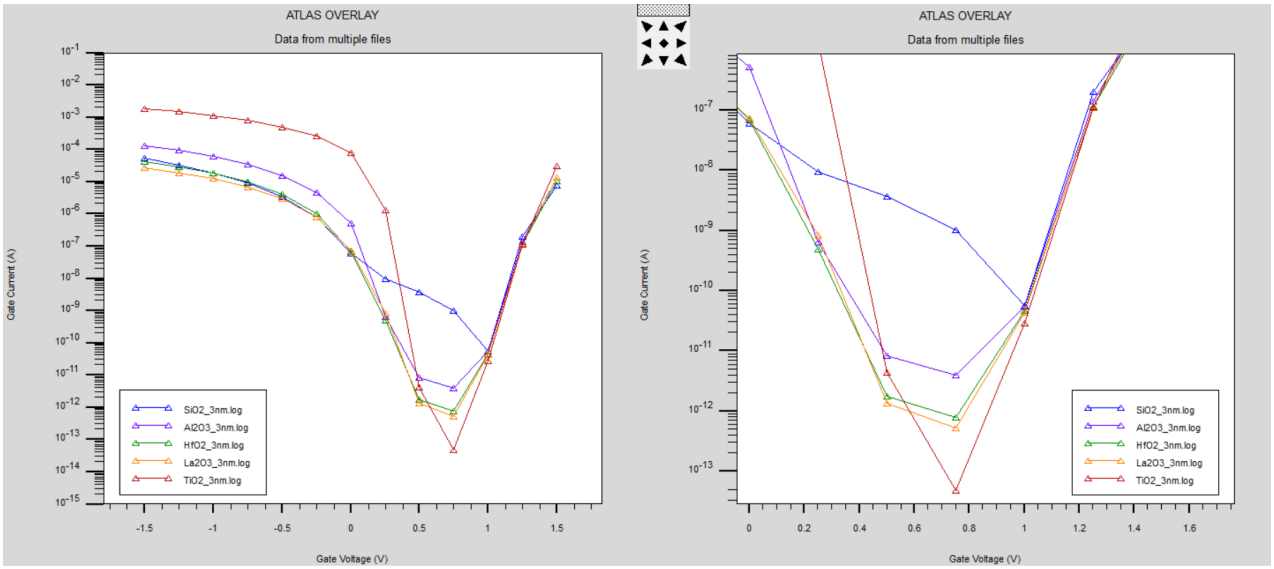
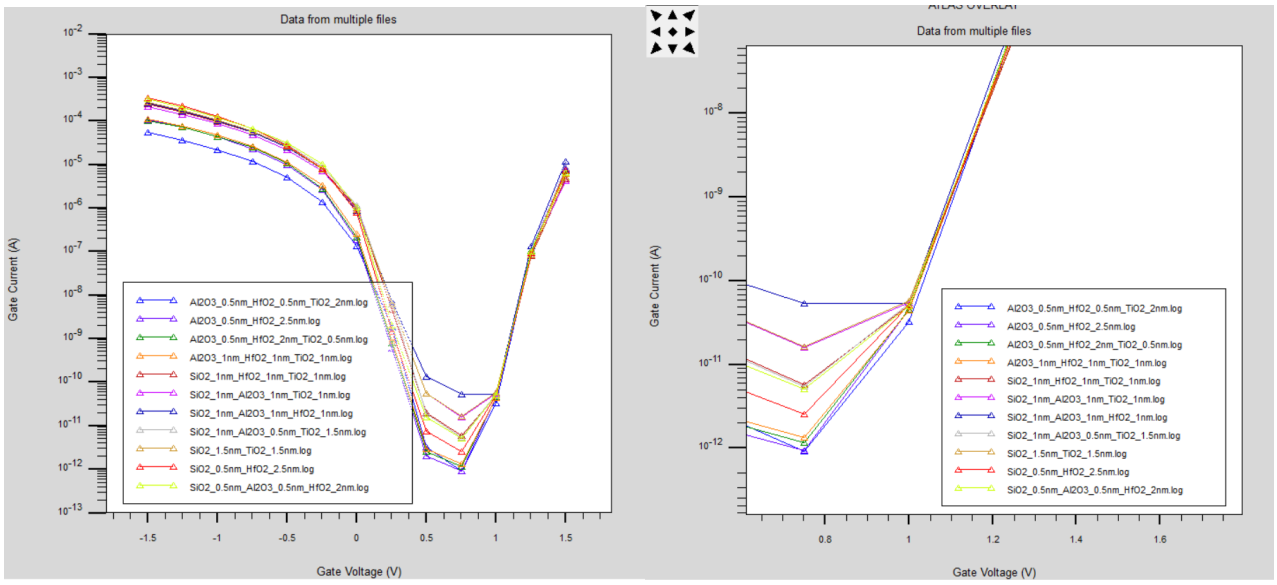


Figure 6. a. I_D for single material gate oxide dielectrics (control group) log(I_D) –V_{GS} (left) and I_D–V_{GS} (right) b. I_D current for FGM-group of gate oxide dielectrics log(I_D) –V_{GS} (left) and I_D–V_{GS} (right).

4.2. I_G per V_{GS} Leakage Current



(a) (b)



(c) (d)

Figure 7. a, 7b (zoom): I_G leakage current for single material gate oxide dielectrics (control group) log (I_G) –V_{GS} 7c, 7d (zoom): I_G leakage current for FGM group gate oxide dielectrics, log (I_G) –V_{GS}.

[10]This graph shows the leakage current characteristics in the hot electron/hole injection model.[10] for traditional single-material gate dielectrics such as TiO_2, with the lowest leakage current around 10^{-13} A at 0.75V for our specific FinFET under study, shown in Figure 1. The curves generally show a similar trend, with this leakage current decreasing with increasing gate-source voltage due to better depletion region formation. The right graph shows the leakage current for FinFETs with FGM gate oxides, labeled FGM-A through FGM-N. The curves are closely grouped and follow a similar trend to the control group, but with some variation between the different FGM materials. Lower leakage current is preferable, especially for memory devices such as EEPROMs where high I_G can contribute to charge loss and memory degradation over time. The performance of FGMs in terms of I_G appears to be similar to that of single-material dielectrics, suggesting that FGMs may provide a slight, non-significant advantage in reducing I_G, but they do not exhibit any deficiency in device reliability.

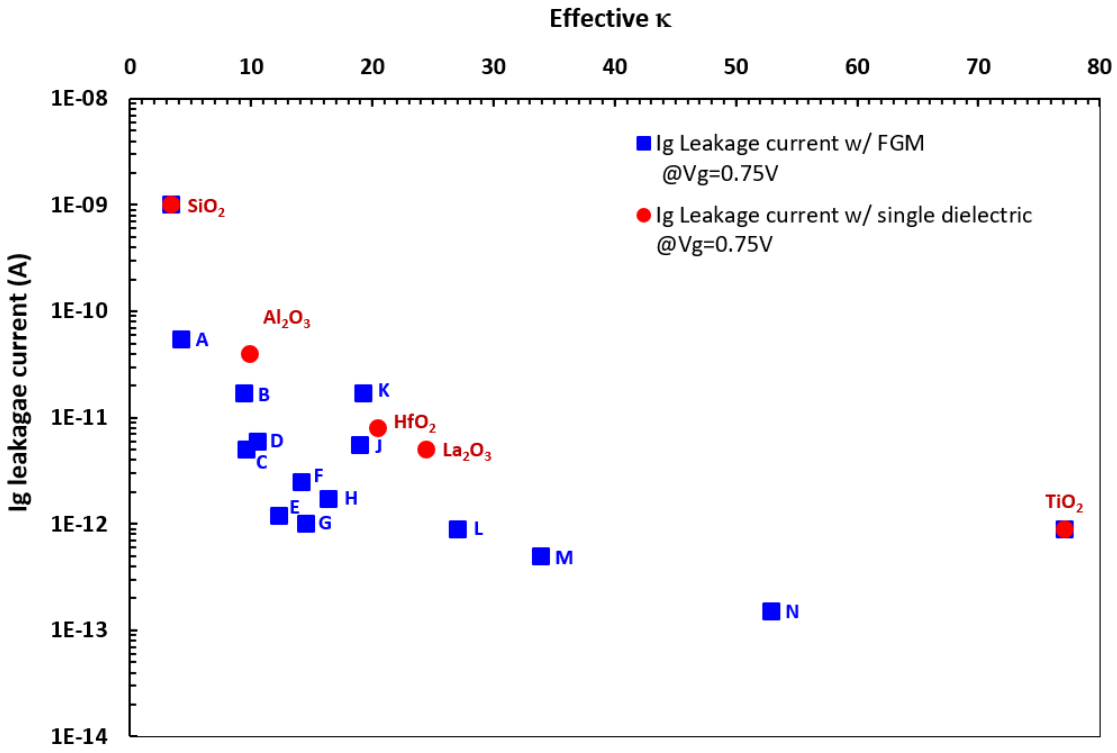


Figure 8. Ig Leakage Current for FinFET with single material and FGM gate oxide dielectrics (□□calculated with MG model).

We find that the use of FGM dielectrics has the potential to generate lower gate-to-channel leakage currents, and for FGM-N it is almost 53 times lower than that of the FinFET with single HfO2 dielectric, as it becomes apparent that interface effects are minimized when smoother dielectric constant transitions are fabricated from the channel to the gate material.

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4.3. Drain Induced Barrier Lowering

Figure 9 plots the Drain Induced Barrier Lowering (DIBL) against the effective dielectric constant (k) for different materials used in FinFETs. As DIBL is the short-channel effect where the drain voltage can influence the threshold voltage of the transistor, a lower DIBL value does generally better because it means the device has better control over the threshold voltage and is less susceptible to variations due to changes in the drain voltage. DIBL with single dielectric (Solid Line) represented the DIBL performance across a range of dielectrics for a standard single-layer dielectric material, starts high with SiO_2 and then decreases significantly as the effective □□increases, showing improved performance for materials with higher κ values like HfO_2, Al_2O_3, and TiO_2. The trend suggests that as the effective dielectric constant increases, the DIBL effect decreases, which is a favorable outcome. DIBL values when using FGM techniques have peaks (labeled from A to N) that indicate where the DIBL is higher, possibly due to process variations, material properties or anomalies. DIBL performance of FGM's seems best for FGM-N with 5.48 mV/V which is %38.2 lower than that of HfO_2.

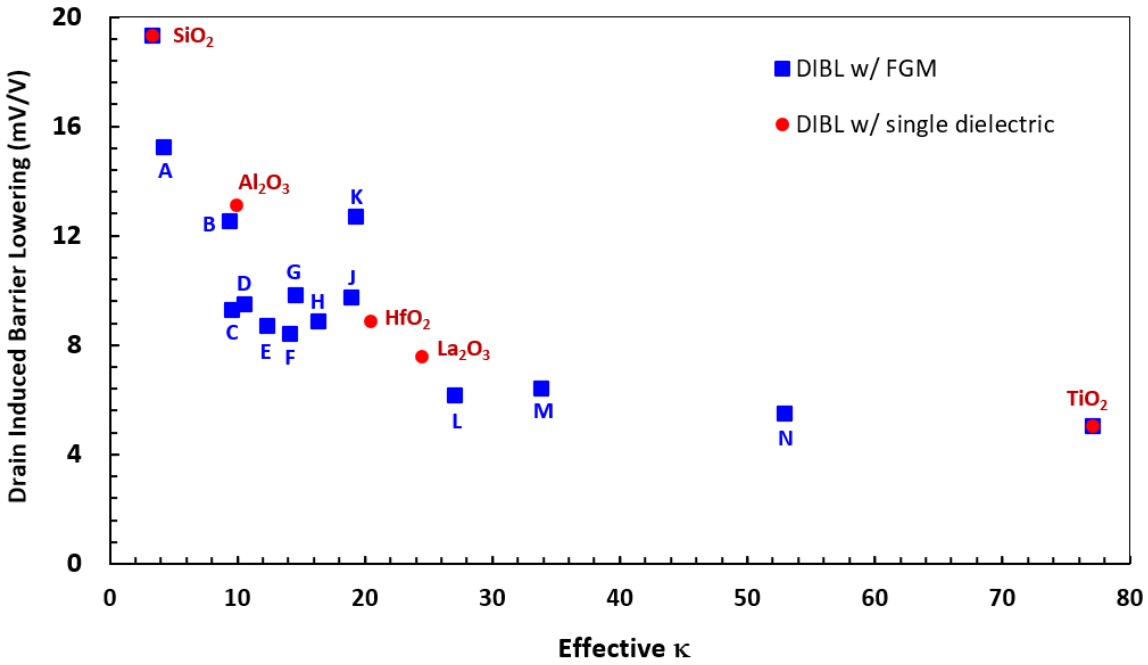

Figure 9. DIBL with single material and FGM gate oxide dielectrics

4.4. Subthrehold Slope

Subthreshold slope performance of FGM's seems best for FGM-K with 76.2 mV/decade which is %7.64 lower than that of HfO_2.

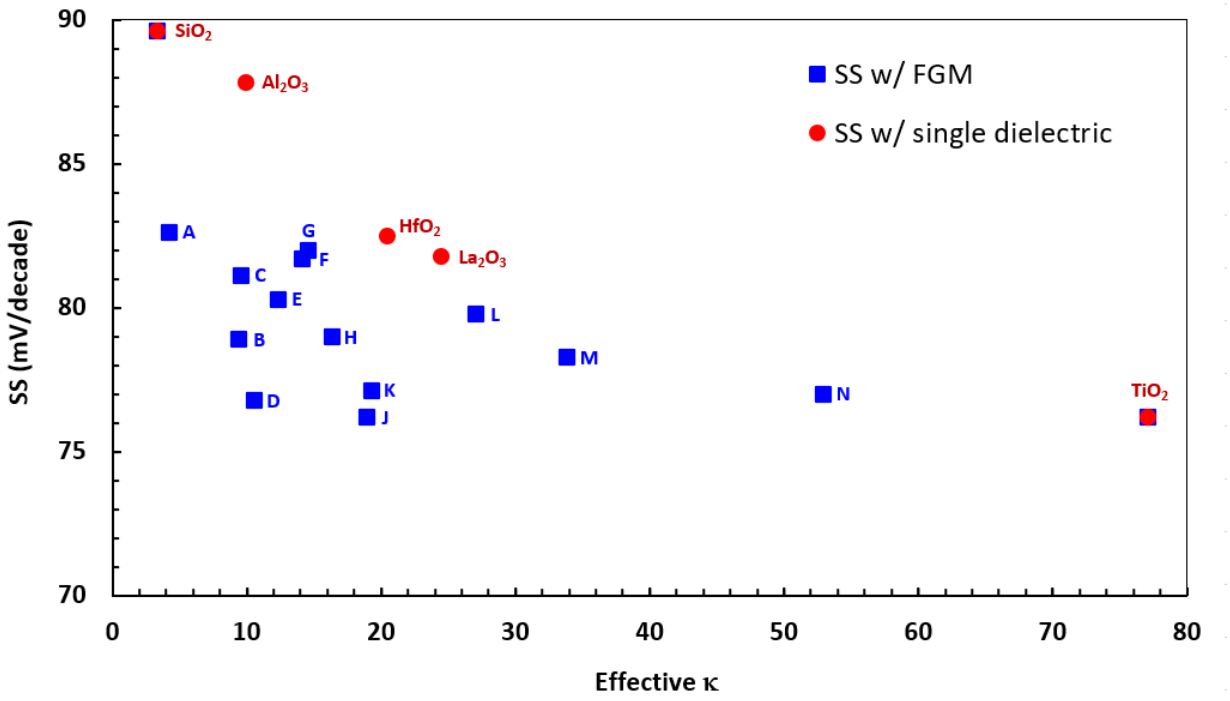

Figure 10. SS with single material and FGM gate oxide dielectrics

4.5. Off-State I_D Current

Off-State I_D Current performance of FGM's seems better for FGM-B with $2.23x10^{-17}$ A which is almost 2 orders of magnitude lower than that of HfO_2.

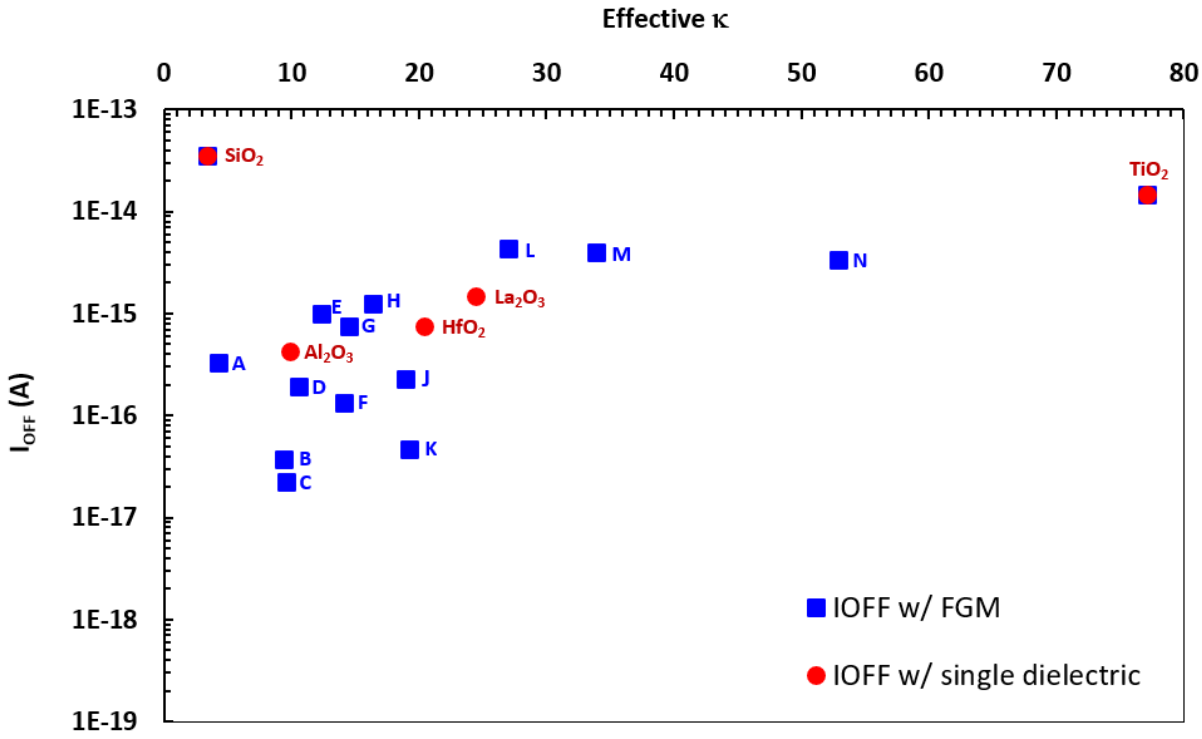

Figure 11. I_{OFF} with single material and FGM gate oxide dielectrics

4.6. On-State I_D Current

ON-State I_D Current performance for FGM-K with 1.93×10^{-5} A which is almost %62 better than that of with HfO_2.

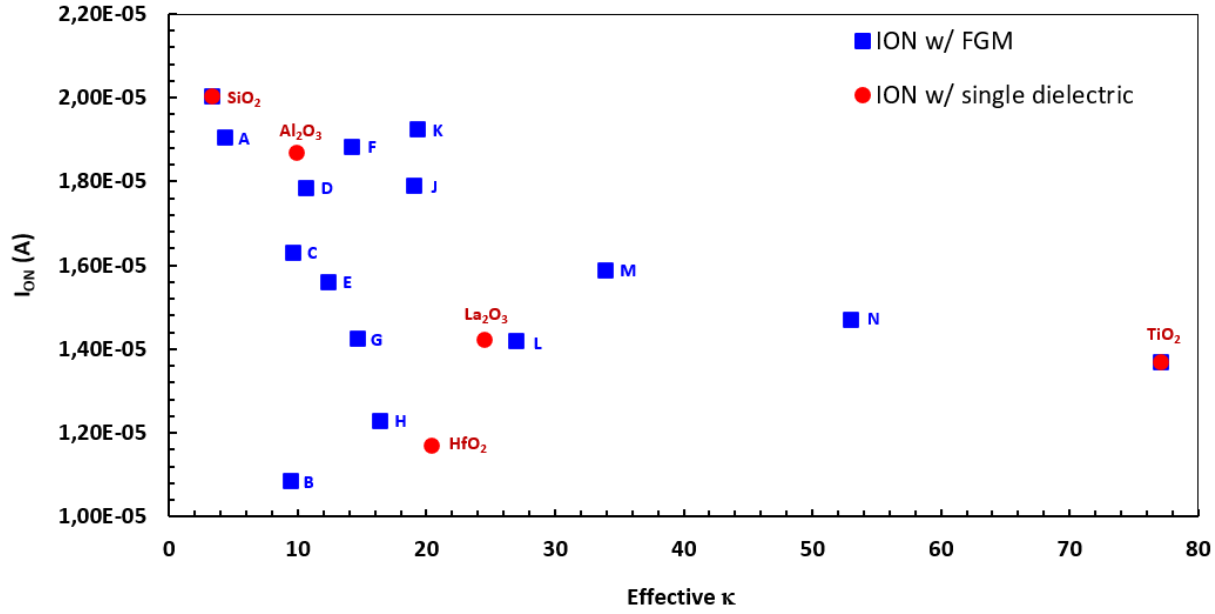

Figure 12. I_{ON} with single material and FGM gate oxide dielectrics

4.7. I_{ON} / I_{OFF} Ratio

I_{ON}/I_{OFF} ratio performance of FGM is better for FGM-C with 7.31×10^{11} which is almost 45 times better than that of HfO_2.

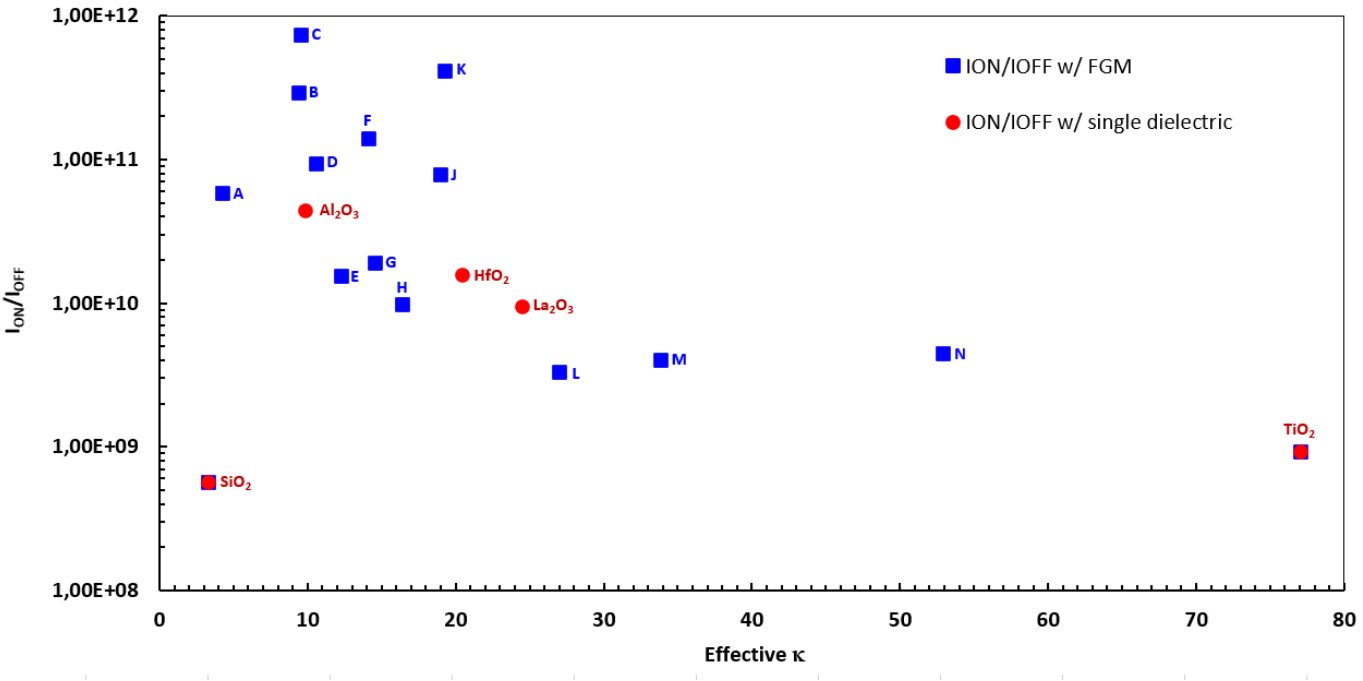

Figure 13. Ion/Ioff ratio with single material and FGM gate oxide dielectrics

4.8. Threshold Voltage VTH

VTH performance of FGM is better for FGM-A with 0.7012 V which is almost %19.2 better than that of HfO2.

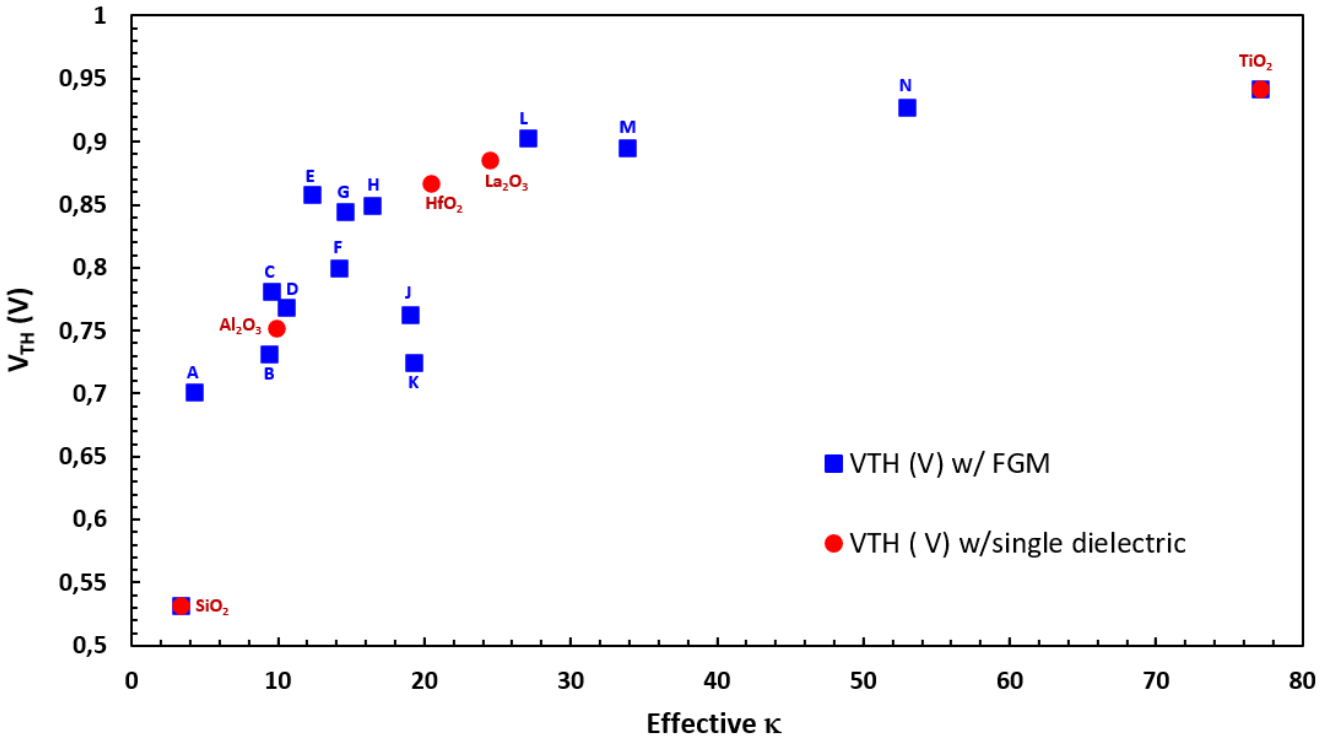

Figure 14. VTH with single material and FGM gate oxide dielectrics.

5. Conclusion

The FGM technique may offer a way to engineer specific device characteristics, but it requires careful control and understanding of the material properties to achieve the desired outcomes consistently. Our results indicate that proposed FinFET with FGM gate dielectrics has lesser I_{GL} up to 53 times, lesser DIBL up to %38.2, lesser SS up to %7.6, lower I_{OFF} up to 2 decades, higher I_{ON} up to %62, higher I_{ON}/I_{OFF} up to 45 times and lesser V_{TH} up to %19.2.

Table 6. FOM_{FET} values for each configuration of single dielectric and FGM configurations.

Material	FOM_FET
SiO_2	9,5
Al_2O_3	20,6
HfO_2	33,4
La_2O_3	43,0
TiO_2	76,0
FGM-A	20,0
FGM-B	70,2
FGM-C	70,9
FGM-D	38,4
FGM-E	45,6
FGM-F	38,0
FGM-G	58,0
FGM-H	41,6
FGM-J	40,3
FGM-K	56,1
FGM-L	65,9
FGM-M	69,3
FGM-N	100,0

Looking at the FOM_{FET} values calculated by Equation-4, single dielectric gate oxides TiO_2 has the best performance. HfO_2 performance achieved 33.4 whereas FGMs B, C, K, L, M and N achieve better than HfO_2 and entire single material dielectrics except TiO_2.

FGM approach aimed to improve the gate's control over the channel and seemed to achieve a success with respect to the FOM_{FET} selected as a figure of merit for overall FinFET performance, which can be always be customized due to importance of the performance parameter selected by the designer.

FGMs seem to provide some space to engineer new gate oxides between dielectric constants 35-95 and at least to try these as gate dielectric material. With respect to the same FinFET with single layer HfO_2 gate dielectric performance, most FGMs showed superior performance. Within gate insulators and BOX structures, FGMs may provide versatile opportunities for optimizing FinFET devices.

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References

[1] P. Vijaya and L. Rohit, "Improvement of Ion, Electric Field and Transconductance of TriGate FinFET by 5nm Technology," *Silicon*, vol. 14, no. 13, pp. 7889–7900, Aug. 2022, doi: 10.1007/s12633-021-01536-z.

[2] L. Gangwani and S. Hajela, "Analog Performance Analysis of a Novel 5nm Stacked Oxide Top Bottom Gated Junctionless FinFET," *IOP Conf Ser Mater Sci Eng*, vol. 1258, no. 1, p. 012046, Oct. 2022, doi: 10.1088/1757-899x/1258/1/012046.

[3] R. Das and S. Baishya, "Dual-material gate dual-stacked gate dielectrics gate-source overlap tri-gate germanium FinFET: analysis and application," *Indian Journal of Physics*, vol. 93, no. 2, pp. 197–205, Feb. 2019, doi: 10.1007/s12648-018-1289-y.

[4] V. A. Markel, "Introduction to the Maxwell Garnett approximation: tutorial," *Journal of the Optical Society of America A*, vol. 33, no. 7, p. 1244, Jul. 2016, doi: 10.1364/josaa.33.001244.

[5] N. B. Bousari, M. K. Anvarifard, and S. Haji-Nasiri, "Improving the electrical characteristics of nanoscale triple-gate junctionless FinFET using gate oxide engineering," *AEU - International Journal of Electronics and Communications*, vol. 108, pp. 226–234, Aug. 2019, doi: 10.1016/j.aeue.2019.06.017.

[6] N. Jankovic, "Numerical simulations of N-type CdSe poly-TFT electrical characteristics with trap density models of Atlas/Silvaco," *Microelectronics Reliability*, 2012, doi: 10.1016/j.microrel.2012.03.031.

[7] D. Dosev, B. Iñíguez, L. F. Marsal, J. Pallares, and T. Ytterdal, "Device simulations of nanocrystalline silicon thin-film transistors," *Solid State Electron*, vol. 47, no. 11, pp. 1917–1920, 2003, doi: 10.1016/S0038-1101(03)00167-9.

[8] R. Tsu, D. Babić, and L. Loriatti, "Simple model for the dielectric constant of nanoscale silicon particle," *J Appl Phys*, vol. 82, no. 3, pp. 1327–1329, Aug. 1997, doi: 10.1063/1.365762.

[9] D. R. Penn, "Wave Number Dependent Dielectric Function of Semiconductors," *Electron Transport Mechanism in Insulating Films*, vol. 2093, 1962.

[10] "Atlas User Manual DEVICE SIMULATION SOFTWARE," 1984.

[11] S. I. Garduño, J. Alvarado, A. Cerdeira, M. Estrada, V. Kilchytska, and D. Flandre, "Gate leakage currents model for FinFETs implemented in Verilog-A for electronic circuits design," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 27, no. 5–6, pp. 846–862, 2014, doi: 10.1002/jnm.1988.

[12] D. Hisamoto *et al.*, "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," 2000.

[13] N. El, I. Boukortt, B. Hadri, and S. Patanè, "Effects of High-k Dielectric Materials on Electrical Characteristics of DG n-FinFETs," 2016.

[14] M. K. AN, G.-B. A, and B. B, "3D Simulation of Fin Geometry Influence on Corner Effect in Multifin Dual and Tri-Gate SOI-Finfets.," *Int J Nano Stud Technol*, pp. 29–32, Oct. 2013, doi: 10.19070/2167-8685-130006.

[15] D. Nagy, G. Espineira, G. Indalecio, A. J. Garcia-Loureiro, K. Kalna, and N. Seoane, "Benchmarking of FinFET, Nanosheet, and Nanowire FET Architectures for Future Technology Nodes," *IEEE Access*, vol. 8, pp. 53196–53202, 2020, doi: 10.1109/ACCESS.2020.2980925.

[16] P. Vimala and T. S. Arun Samuel, "TCAD Simulation Study of Single-, Double-, and Triple-Material Gate Engineered Trigate FinFETs," *Semiconductors*, vol. 54, no. 4, pp. 501–505, Apr. 2020, doi: 10.1134/S1063782620040211.

[17] D. Bhattacharya and N. K. Jha, "FinFETs: From Devices to Architectures," *Advances in Electronics*, vol. 2014, pp. 1–21, Sep. 2014, doi: 10.1155/2014/365689.

[18] D. Gealy, B. Vishnavath, V. S. Cancheepuram, and M. N. Rocklein, "US8110469 Graded Dielectric Structures," US8110469, Feb. 27, 2012

[19] A. C. Sharma, "Size-dependent energy band gap and dielectric constant within the generalized Penn model applied to a semiconductor nanocrystallite," *J Appl Phys*, vol. 100, no. 8, 2006, doi: 10.1063/1.2357421.

[20] J. Azadmanjiri, C. C. Berndt, J. Wang, A. Kapoor, V. K. Srivastava, and C. Wen, "A review on hybrid nanolaminate materials synthesized by deposition techniques for energy storage applications," *Journal of Materials Chemistry A*, vol. 2, no. 11. pp. 3695–3708, Mar. 21, 2014. doi: 10.1039/c3ta14034b.

[21] J. D. Plummer and P. B. Griffin, "Material and Process Limits in Silicon VLSI Technology," 2001.

[22] G. A. Niklasson, C. G. Granqvist, and O. Hunderi, "Effective medium models for the optical properties of inhomogeneous materials," *Appl Opt*, vol. 20, no. 1, p. 26, Jan. 1981, doi: 10.1364/ao.20.000026.

[23] A. Nowbahari, A. Roy, and L. Marchetti, "Junctionless transistors: State-of-the-art," *Electronics (Switzerland)*, vol. 9, no. 7, pp. 1–22, 2020, doi: 10.3390/electronics9071174.

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