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HIGH PERFORMANCE TFT OF a-Si:H ON A SiO_2 DIELECTRIC

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An amorphous silicon thin-film transistor has been developed which uses CVD-SiO_2 as gate dielectric. The structure of the TFT is of the inverted staggered type. This transistor has an on/off-current ratio of 2×10^9. The off-current is below 1 pA, even at a channel width of 3000µm; the on-current is in the range of 100 - 180µA (l = 10µm, U_G = 20V).

1. INTRODUCTION

For the development of thin-film transistors with amorphous silicon, silicon nitride is usually quoted as the best gate dielectric[1]. Several attempts have been made to use SiO_2, but the characteristics achieved were not satisfying[2, 3, 4]. With this work we were able to demonstrate the possibility of producing high-quality TFTs using silicon dioxide as dielectric. A process has been developed which is compatible with the production process of the addressing matrix for liquid crystal displays on glass substrates. Test transistors with different channel lengths have been used to optimize the process parameters.

2. TECHNOLOGICAL

The cross-section of the transistor is shown in fig. 1. On Corning 7059 substrates, the gate electrode is formed by a 200nm thick layer of tantalum (doped with nitrogen), onto which the SiO_2 for the gate dielectric is deposited, 420nm thick, by CVD at 420°C. As the next step the amorphous silicon is

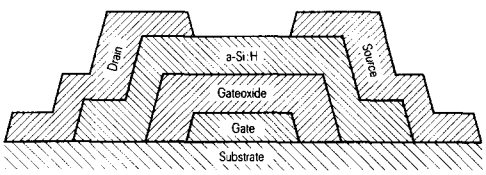

FIGURE 1
Cross-section of the TFT

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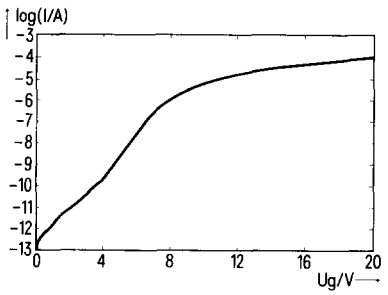

FIGURE 2

Transfer characteristic log I_D vs. U_G of one TFT

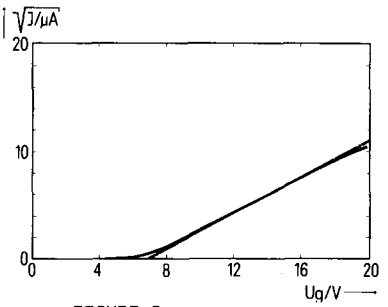

FIGURE 3

Transfer characteristic $\sqrt{I_D}$ vs. U_G of one TFT

deposited by glow discharge using pure silane with an rf power of 11mW/cm². During the deposition process the substrates are held at 250°C. The silicon layer is structured by plasma etching with CF_4. Finally the source and drain contacts are thermally evaporated into the photolithographic lift-off mask. With a double layer of magnesium and aluminum or chromium, good ohmic contacts are achieved and no n^+-doped silicon layer is required.

The amorphous silicon was characterized by IR transmission measurements, which showed no absorption band at 2100cm^{-1}. Measurements of temperature dependent conductivity yielded an activation energy of 0.84 eV.

3. RESULTS AND DISCUSSION

The TFTs produced in the described manner with SiO_2 gate dielectric have an excellent switching ratio exceeding 10^9 (fig. 2). At a channel length and width of 10μm and 3000μm respectively, the off-current is lower than 1 pA and the on-current exceeds 100μA. The threshold voltage of this TFT is 6.8V, as has been determined from the square root plot of the transfer characteristic

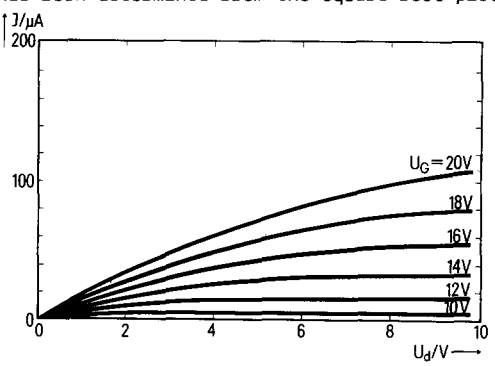

FIGURE 4

Output characteristics I_D vs. U_D of one TFT.

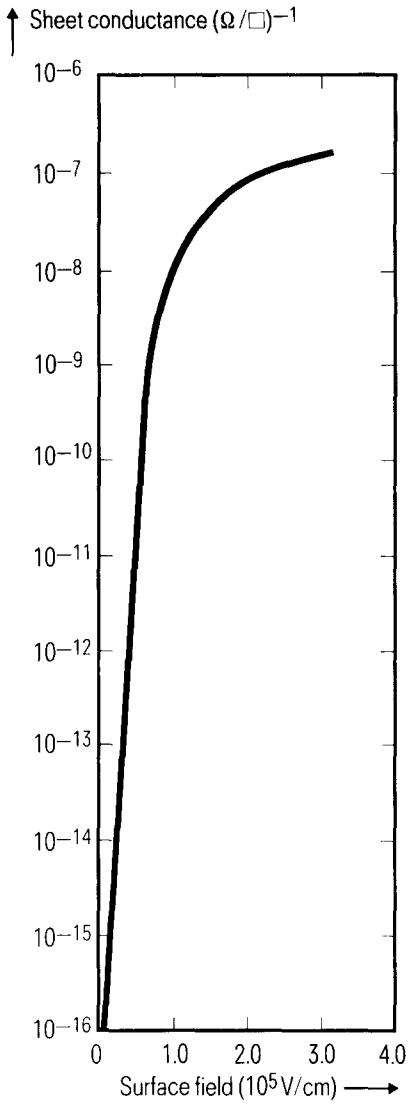

FIGURE 5
Sheet conductance vs. surface field of one TFT

I_D vs. U_G (fig. 3). The mobility is calculated as 0.71 cm^2/Vs. The output characteristics (I_D vs. U_D) of this device are shown in fig. 4.

For better comparison with other results, the channel conductance of our device is plotted vs. the field strength at the dielectric/semiconductor interface (fig. 5). It increases over nine orders of magnitude as the gate voltage varies from 0 to 40 volts. From field effect measurements the density of states in the band gap of the a-Si:H can be calculated[5]. When assuming a constant density of states throughout the gap, a model calculation yields the resulting characteristics of the TFT[6]. When comparing our results with these characteristics, we obtain a first measure of the DOS in the gap, which is about $1x10^{17} cm^{-3} eV^{-1}$. This estimation is also confirmed by a constant photocurrent measurement made on a silicon sample prepared under the same conditions, which yields about $5x10^{16} cm^{-3} eV^{-1}$ defect states.

The drift of these transistors is small; the on-current decreases by 5-10% after 100 sec. As the off-current drops too, but faster, the switching ratio increases with time. The cause of the small decrease in on-current is a small change in threshold voltage which amounts to only 0.4 eV after the transistor has been switched on for one hour.

The preparation of the interface between semiconductor and contacts has a significant influence on the TFT characteristics. Sputter-cleaning of

the semiconductor before contact evaporation decreases the on-current of the transistor markedly, as does contact evaporation by an electron gun. Best results were obtained when the contact material was evaporated by resistive heating onto the heated substrate (80°C).

The interface between gate oxide and semiconductor, too, is very sensitive to cleaning processes. Heating to 300°C as well as a glow discharge with H_2, Ar or forming gas (5% H_2 in N_2) increases the threshold voltage and so decreases the on-current of the device. However a weak glow discharge with N_2 does not decrease the on-current. This process increases the steepness of the transfer characteristic by 30%. It is likely that the density of interface states decreased, since the silicon process and the contacts remained unchanged. The threshold voltage of these TFTs moved to 3-5V, a value which is usually found for TFTs with a-SiN_x:H dielectric. The reason for this change could be an incorporation of nitrogen at the SiO_2/a-Si:H interface. A more detailed investigation should focus upon the structure of the interface to verify this assumption.

4. CONCLUSION

We have been able to show that it is possible to produce excellent transistors with SiO_2 as gate insulator. The production process does not require the deposition of gate dielectric and a-Si:H in one run without breaking the vacuum. As these transistors have a very low off-current and a small drift, they are suitable for driving LCDs. Test samples with an addressing matrix have already been made.

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REFERENCES

1) M.J. Powell, 4th Display Res. Conf. (Eurodisplay 84) 131

2) K.Asama, T.Kodama, S.Kawai, Y.Nasu, S.Yanagisawa, SID Symp. Digest (1983)144

3) K.Suzuki, T.Aoki, M.Ikeda, Y.Okada, Y.Zohta, K.Ide, SID Symp. Digest (1983) 146

4) F.Morin, M.LeContellec, Displays January (1983) 3

5) K.Weber, M. Grünewald, W. Fuhs, P.Thomas, phys.stat.sol.(b) 110 (1982) 133

6) A.vanCalster, Thin Solid Films 126 (1984) 219