A TCAD Study on Simulation and Benchmarking of Nanometer Scale Functionally Graded Materials as Gate Dielectrics for FinFETs

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ABSTRACT

In this paper, we present simulation results obtained using TCAD tools for a 3-D silicon on insulator (SOI) n-FinFET structure with various functionally graded materials (FGMs) as gate dielectric, with a gate length of 14 nm at 300K. Study explores the potential of FGMs as a viable alternative to conventional single layer high-κ dielectrics in FinFET structures. We investigate the impact of using FGMs as gate oxide dielectric on key electrical performance parameters, threshold voltage ($\mathbf{V}_{TH}$), on-state current ($\mathbf{I}_{ON}$), off-state current ($\mathbf{I}_{OFF}$), drain-induced barrier lowering (**DIBL**) and subthreshold slope (**SS**), $\mathbf{I}_{ON}/I_{OFF}$ ratio and gate metal-to-silicon leakage current ($\mathbf{I}_{GL}$). Using SILVACO ATLAS for device simulation, we start with SiO_2, Al_2O_3, HfO_2, La_2O_3 and TiO_2 as single layer gate dielectrics of 3nm thickness ($\mathbf{t}_{ox}$) for a 14nm channel (fin) length ($\mathbf{L}_{FET}$), 2nm channel width ($\mathbf{W}_{FET}$), 5nm channel height ($\mathbf{h}_{fin}$) FinFET structure; then formed 13 different 2- or 3-stage FGM combinations as gate dielectrics, like [Al_2O_3:HfO_2:TiO_2] staged in parallel sheets, connected serially, as a 3-stage example. Modified Penn Model [1], [2] is used to calculate the dielectric constant of thin nanolaminate material forming each FGM laminate, using their bulk dielectric constant κ_b, bandgap energy E_G, high frequency dielectric constant κ_∞ and its Fermi wave vector K_f. Maxwell-Garnet (MG) approximation [3] is selected to calculate the effective dielectric constant (κ_{EFF}) for the 2-and 3-layered FGM dielectrics. Hot Electron / Hot Hole Injection (HEI-HHI) model [4] is used to model gate leakage current within SILVACO ATLAS/Deckbuild simulation tool and results were found to be consistent with experimental results within [5], with systematically varying thickness of mentioned dielectric layers to form a graded structured 3 nm-thickness FGM gate dielectrics. FinFET Buried Oxide (BOX) material was kept as Al_2O_3 through all simulations. Our results indicate that proposed FinFET with FGM gate dielectrics has lesser I_{GL} up to 53 times, lesser DIBL up to %38.2, lesser SS up to %7.6, lower I_{OFF} up to 2 decades, higher I_{ON} up to %62, higher I_{ON}/I_{OFF} up to 45 times and lesser V_{TH} up to %19.2, with respect to the FinFET of same dimensions composed of single layer HfO_2 gate dielectric. FGMs show better performance than single material dielectric when used as gate insulating materials. Results may provide versatile opportunities for optimizing FinFET devices.

Keywords: Technology Computer-Aided-Design (TCAD) Simulation, Functionally Graded Material (FGM), Junctionless Thin Film Transistor (JLTFT); Fin-Field Effect Transistor (FinFET), Drain Induced Barrier Lowering (DIBL); Subthreshold Slope (SS), Threshold Voltage (V_{TH}), I_{ON}/I_{OFF} ratio.

I. INTRODUCTION

Functionally graded materials (FGMs) are composite materials with a continuously variable distribution of two or more constituent phases [6]. The composition and/or microstructures of FGMs change gradually, resulting in a graded pattern of material properties. FGMs have applications in various fields such as structural materials, biomaterials, semiconductors, coating materials, and electrode materials [7]. FGMs eliminate sharp interfaces between different materials and instead have a gradual variation from one material to another [8] FGMs are inhomogeneous materials whose properties change continuously with spatial positions [9]. The manufacturing of FGMs can be achieved through different techniques, including additive manufacturing (AM), physical vapor deposition, chemical vapor deposition, powder metallurgy, and centrifugal casting [10], [11]. FGM grading is achieved by controlling the distribution of certain properties within the material. FGM grading is either discrete or continuous and this gradient can be of either material composition, orientation or fraction gradient [12]. In case we have a discrete profile grading we can have a stepwise profile. In case we have continuous profile grading we can have either a linear profile so that the material properties change linearly from one surface to the other, or an exponential or an n^{th}-power thickness profile or a sigmoidal profile, so that the material property changes with a smooth transition that can represented by functions like an hyperbolic tangent function. There might exist many phases of the materials neighboring each other so that as thickness is varied the material property changes from phase A to phase B which means that this is single FGM. As material A concentration increases the other material B concentration decreases. In a double FGM, there are 3 seperate materials or phases so that while thickness changes, material property is gradually varied starting with A emerging into B and fully ending up in C. In this work, we performed simulations with single and double FGM dielectric materials for trigate FinFET structure. Our research focused on conducting simulation-based studies of FinFETs since their introduction in the year 2000 [13], performance of FinFET technology, including analytical modeling and simulation of FinFET devices [14], the influence of fin geometry on corner effects in multifin dual and tri-gate SOI-FinFETs [15], benchmarking of FinFET, nanosheet, and nanowire FET architectures for future technology nodes [16], the analog performance analysis of stacked oxide top-bottom gated junctionless FinFET [17] and a detailed study of single-material gate, double-material gate, and triple-material gate FinFETs were carried out [18]. In-depth analysis of typical types of FinFETs were presented in [19] with which we tried to match the terminology and abbreviations within that paper.

II. DEVICE STRUCTURE

The 3D Technology Computer-Aided Design (TCAD) structure for FinFETs is shown in Fig. 1. Using SILVACO ATLAS for device simulation, we start with SiO_2, Al_2O_3, HfO_2, La_2O_3 and TiO_2 as single layer gate dielectrics of 3nm thickness (t_{ox}) for a 14nm channel (fin) length (L_{FET}), 2nm channel width (W_{FET}), 5nm channel height (h_{fin}) FinFET structure, then formed 13 different FGM materials with systematically varying thickness of mentioned dielectrics to form a graded structured 3nm-thickness gate oxide dielectric. With thickness of 3 nm, BOX material (Figure 1) is kept as Al_2O_3 and never changed through simulations. Equal doping concentration of $5x10^{19}$ cm^{-3} is used source - drain channel region.

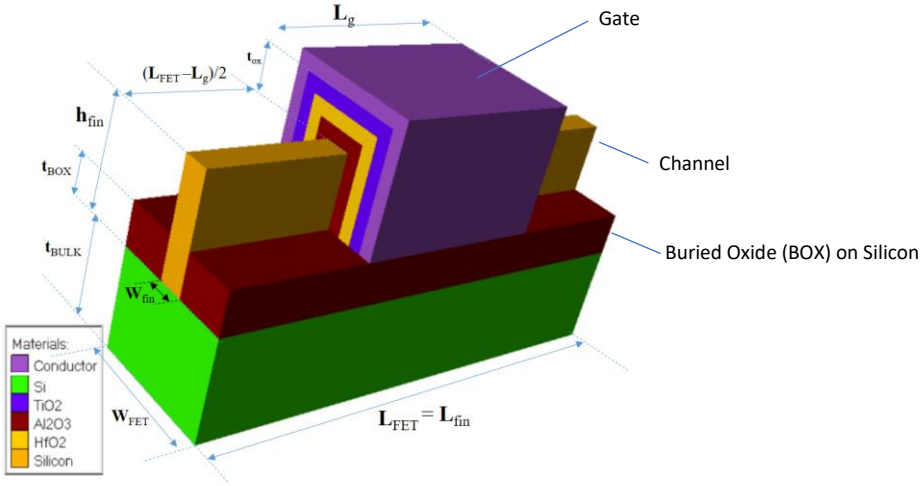

Figure 1. Proposed 3-material FGM gate oxide dielectric based FinFET Şekle BOX caption ekle

Table 1. Proposed FinFET properties

Property	Value	Note / Abbreviation
Channel (Fin) Length	14 nm	L_{fin}
Gate thickness	10 nm	Tg
Channel (Fin) Width	2 nm	W_{fin}
Gate Length	14 nm	L_g
Gate-to-Gate length	X nm	L_{gg}
Fin Width	2 nm	W_{fin}
Fin Height	5 nm	H_{fin}
Channel Concentration	$5x10^{19}$ cm^{-3}	N_d
Gate work function	5 eV	ϕ_w
FET Length	34 nm	L_{FET}
FET Width	10 nm	W_{FET}
Total Gate Oxide thickness	3 nm	t_{ox}
BOX Thickness	3 nm	t_{BOX}
BOX material	Al_2O_3	-
Bulk Si Thickness	10 nm	t_{BULK}

III. METHOD

As we target to prove that FGM gate oxide dielectric structures behave and perform better than single material dielectric structure in FinFET design, our method will be 5 steps. We need to analyze, model and evaluate the nanoscaled dielectric structures decreasing thickness will reduce the bulk capacitance and dielectric constant of the dielectric. First in IIIa, Modified Penn Model [1], [2] is used to calculate the dielectric constant of thin nanolaminate material forming each FGM laminate, using their bulk dielectric constant κ_b, bandgap energy E_G, high frequency dielectric constant κ_∞ and its Fermi wave vector K_f. In part IIIb thru IIIc, Maxwell-Garnet (MG) approximation [3] is selected to calculate the effective dielectric constant (κ_{EFF}) for the 2-and 3-layered FGM dielectrics. In IIId and IIIe, FinFET model in Figure 1 is implemented via ATLAS language and Hot Electron / Hot Hole Injection (HEI-HHI) model [4] is used to model gate leakage current within SILVACO ATLAS/Deckbuild simulation tools are used to calculate with experimental results within [5][5], with systematically varying thickness of mentioned dielectric layers to form a graded structured 3 nm-thickness FGM gate dielectrics. 18 different FinFET model simulations are performed in Silvaco Atlas Deckbuild, 5 of which include single material gate oxide dielectrics in Table 4A, 13 of which include FGM dielectrics as gate oxide (in Table 4B). Thru IIIf and IIIg, key electrical performance parameters like threshold voltage (**V_{TH}**), on-state current (**I_{ON}**), off-state current (**I_{OFF}**), drain-induced barrier lowering (**DIBL**) and subthreshold slope (**SS**), **I_{ON}/I_{OFF}** ratio and gate metal-to-silicon leakage current (**I_{GL}**) are selected and evaluated for each simulation. We also design a customized figure of merit in order to justly evaluate each FinFET performance with respect to each other. Here we present details each step as below:

a. Thickness Dependence of κ under quantum confinement effects

Theoretical foundation for constructing a κ-graded FGM is given in US Patent 8110469 by Gealy et.al. [20] and we model our gate oxide for FinFET as below:

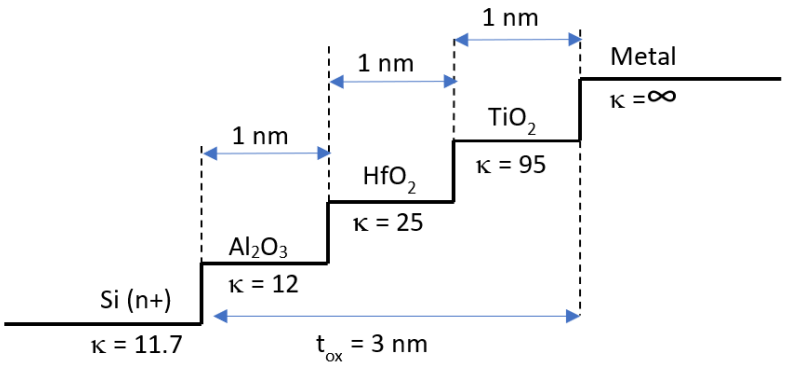

Figure 2. Stepwise Grading Profile for an example FGM (FGM-H in Table 4B.) as gate oxide dielectric

Gate oxide dielectric constant has to be evaluated for according to the formula, Equation-1,

$$\kappa_{ox} = 1 + \frac{\kappa_b - 1}{1 + \left(\frac{\kappa_\infty 2\pi}{K_f t_{ox}}\right)^2}$$

where κ_b is the bulk dielectric constant, κ_∞ is the high frequency dielectric constant, K_f is Fermi wave vector, t_{ox} is the thickness of the nanoscaled dielectric material [1].

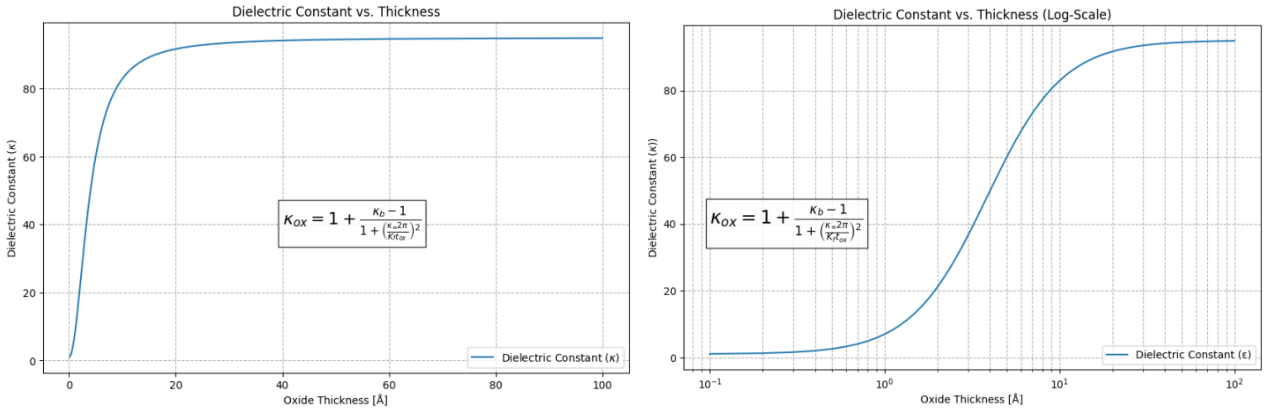

Figure 3. Modified Penn Model for dielectric constant against thickness applied to TiO_2 [1], [2].

For silicon (Si), it has been shown that for thicknesses greater than 10 Å (1 nm), bulk κ_b can be considered to be unchanged and equivalent to κ_{ox} [2]. If t_{ox} is less than 10 Å then we need to consider generalized Penn model [21] for modelling dielectric constant κ as against thickness, under quantum confinement effects for nanolaminates for each FGM's κ_{EFF} to be calculated correctly. As we herein try to model nanolaminates around 5-30 Å, we calculated κ_{ox} of interlayer nanolaminate according to Equation-1. This can be numerically further fitted to the Equation-2 in [21] ;

$$\kappa_{ox} = 1 + \frac{\kappa_b - 1}{1 + \frac{1.7}{t_{ox}^{1.8}}}$$

and when we calculate the resultant kappa κ_{ox} of same material due to its nanolaminate thickness t_{ox} and observe the significant loss in dielectric effect when we observe Table-2. This numerical approximation is depicted in Figure 4, showing that in orders of few nanometers nanolaminate TiO_2 thickness, kappa reduction is significant.

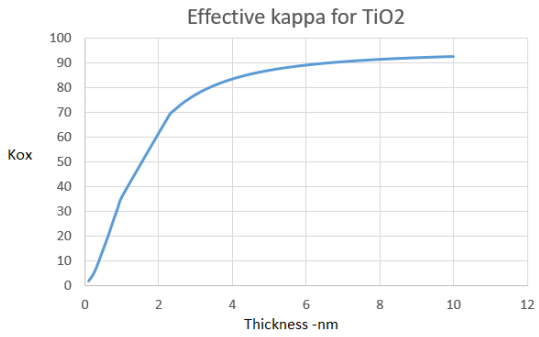

Figure 4. A numerical approximation for Penn Model evaluated by Equation-2

Table 2. Bulk dielectric constant κ_b and resultant oxide kappa κ_{ox} with respect to nanolaminate thickness t_{ox} of dielectric materials calculated with Equation-2.

Material	SiO2	Al2O3	HfO2	La2O3	TiO2
κ_b	3,90	12,00	25,00	30,00	95,00
κ_{ox} in 0.5nm	1,42	2,59	4,47	5,19	14,58
κ_{ox} in 1nm	2,07	5,07	9,89	11,74	35,81
κ_{ox} in 1.5nm	2,59	7,05	14,19	16,94	52,67
κ_{ox} in 2nm	2,95	8,39	17,13	20,49	64,16
κ_{ox} in 2.5nm	3,19	9,29	19,09	22,86	71,85
κ_{ox} in 3nm	3,35	9,90	20,43	24,48	77,09

b. Modelling oxide nanolaminates as FinFET gate oxide dielectrics

In order to isolate the gate metal and form a proper electric field to control the drain current, gate dielectrics are of great importance. Dielectric constants (κ) of some selected gate oxides vary from 3.9 to 95 and their respective bandgaps vary from 9 eV down to 3.5 eV in Table 2.

Table 3. Bandgap and dielectric constant for simple binary oxides used in this paper [22], [23]

Material	Dielectric Constant (κ)	Bandgap (eV)
SiO_2	3,9	9
Al_2O_3	9	8,8
HfO_2	25	5,8
$La2O_3$	30	6
TiO_2	95	3,5

HfO_2 thin films have wide band gap of ≈ 5.8 eV, high dielectric constant (κ ≈ 25) and suitable band offset values relative to Si substrate. In addition to their excellent thermodynamic and chemical stability, HfO_2 has been strongest candidate material for replacing single layer SiO_2 gate dielectrics. There exists no simple binary oxide dielectric between the κ greater than 35 (of Nb_2O_5) and less than 95 (of TiO_2). Thus there starts the possibility and opportunity to generate materials with κ in the

range of 35-95 through FGMs, that have the potential to show better performance properties than HfO_2, especially when we utilize a method to calculate the equivalent dielectric constant of the stacked FGM materials. Among existing methods Maxwell-Garnet equation [3] for calculation of effective κ for 2 layer dielectrics. As we need 3-layer effective κ calculation we need to derive the two equations for 3-layer dielectrics as follows:

c. κ_{EFF} derivations for 3-stage FGM with materials A,B,C

When two layers or phases of dielectric materials are deposited on top of each other, calculation of their effective or resultant dielectric constant of this serially connected sheets of two dielectric materials, also called as, effective dielectric constant for A-B material (effective κ_{AB}) would be calculated by two models, first by Maxwell-Garnet approximation model [3], [24] as Eq.2;

$$\kappa_{EFF,AB} = \kappa_B \frac{\kappa_A + 2\kappa_B + 2f(\kappa_A - \kappa_B)}{\kappa_A + 2\kappa_B - f(\kappa_A - \kappa_B)}$$

where κ_A, κ_B are dielectric constants for material A and B and f is the volumetric filling factor for material A and $(1 - f)$ is the volumetric filling factor for material B in the two phase dielectric system of Fig 5.

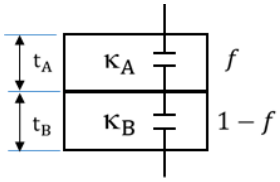

Figure 5. Two phase dielectric system connected in series

To extend this theory for a three-phase system, we need to consider additional complexities due to the interaction between three different dielectric materials. If we denote the dielectric constants of the three materials as κ_A, κ_B , and κ_C and their respective volumetric filling factors as f_A, f_B, and f_C with $f_A + f_B + f_C = 1$, we need to derive an expression that considers all three materials. Thus we can;

- Calculate the effective dielectric constant κ_{AB} for materials A and B using the Maxwell-Garnett equation.
- Consider κ_{AB} as one material and apply the Maxwell-Garnett equation again with κ_{AB} and κ_C to find the overall effective dielectric constant κ_{EFF}, with $f_{AB} + f_C = 1$, finally as Eq.3,

$$\kappa_{EFF,ABC} = \kappa_C \frac{\kappa_{AB} + 2\kappa_C + 2f_{AB}(\kappa_{AB} - \kappa_C)}{\kappa_{AB} + 2\kappa_C - f_{AB}(\kappa_{AB} - \kappa_C)}$$

Table 4A. Control Group: Thickness and bulk κ values and calculated (modified Penn model) dielectric constants values of 5 single material gate dielectrics for 3 nm thickness.

	SiO2	Al2O3	HfO2	La2O3	TiO2
κ_b value	3,9	12	25	30	95
κ_{ox} in 3nm	3,35	9,9	20,43	24,48	77,09

Table 4B. FGM Group: Thickness and κ_{EFF} (applying modified Penn + MG model) values of 13 FGM gate oxide dielectrics between SiO_2 and TiO_2, shown as lower and upper limits of achievable κ_{EFF} within 3nm material thickness.

Material	SiO2	FGM-A	FGM-B	FGM-C	FGM-D	FGM-E	FGM-F	FGM-G	FGM-H	FGM-J	FGM-K	FGM-L	FGM-M	FGM-N	TiO2
SiO2 thickness (nm)	3	1	1	0,5	1	0	0,5	0	0	1	1,5	0	0	0	0
Al2O3 thickness (nm)	0	1	1	0,5	0	0,5	0	0,5	1	0,5	0	0	0,5	0	0
HfO2 thickness (nm)	0	1	0	2	1	2	2,5	2,5	1	0	0	1,5	0,5	0,5	0
TiO2 thickness (nm)	0	0	1	0	1	0,5	0	0	1	1,5	1,5	1,5	2	2,5	0
Total Thickness (nm)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
κ_{EFF}	**3,35**	**4,26**	**9,39**	**9,57**	**10,57**	**12,30**	**14,15**	**14,55**	**16,39**	**18,98**	**19,28**	**27,02**	**33,88**	**52,93**	**77,09**

d. FinFET modelling in Silvaco ATLAS Deckbuild Tool

We start with modeling our FinFET in Silvaco's Atlas/Deckbuild. The family of such tools were used in many research to design and simulate the FinFET devices. The ATLAS Deckbuild simulation employing many standard recombination and continuity models like Shockley-Read-Hall, Schrödinger and Auger; used widespread for 2D/3D simulations of normal or heterogated single, double or triple-gated FinFETs [14],[18],[25].

e. Gate Leakage Current Modelling

In devices that have a metal-insulator-semiconductor (MIS) formation, the conductance of the insulating film would ideally be considered as zero. However, for the sub 0.5um generation of MOS devices there is considerable conductance being measured on the gate contacts [4]. In our case we used two lines of code for proper solvers to be activated in ATLAS/Deckbuild given in Appendix A, among tunneling-through-dielectric models available we used the hot electron/hole injection (HEI-HHI) tunneling model within ATLAS tool [4], so that gate-to-dielectric leakage current was properly and realistically modeled, which gave most accurate results comparable with [5].

Table 2. Summary of used models for tunneling and carrier injection for gate-dielectric leakage current in ATLAS [4]

Model	Syntax	Notes
Band-to-Band (standard)	BBT.STD	For direct transitions. Required with very high fields.
Concannon Gate Current Model	N.CONCAN P.CONCAN	Non-local gate model consistent with Concannon substrate current model.
Direct Quantum tunneling (Electrons)	QTUNN.EL	Quantum tunneling through conduction band barrier due to an insulator.
Direct Quantum tunneling (Hole)	QTUNN.HO	Quantum tunneling through valence band barrier due to an insulator.
Fowler-Nordheim (electrons)	FNORD	Self-consistent calculation of tunneling through insulators. Used in EEPROMs.
Fowler-Nordheim (holes)	FNHOLES	Same as FNORD for holes.
Klaassen Band-to-Band	BBT.KL	Includes direct and indirect transitions.
Hot Electron Injection	HEI	Models energetic carriers tunneling through insulators. Used for gate current and Flash EEPROM programming.
Hot Hole Injection	HHI	HHI means hot hole injection.

f. Choice of performance metrics

Our performance metrics were selected as:

- **I_{GL}**, On-state Leakage Current, in Amperes, leaks from Gate metal through dielectric into the channel, when V_{GS} = 0.75V in our case, needs to be minimized.
- **I_{ON}**, On-state Drain Current, in Amperes, when $V_{DS} = V_{DD}$ (=1.2V in our case) and $V_{GS}= V_{DD}$, needs to be maximized.
- **I_{OFF}**, Off-state Drain Current, in Amperes, when $V_{DS} = V_{DD}$ and V_{GS} = 0.0V, needs to be minimized.
- **I_{ON}/I_{OFF} Ratio**, unitless, accepted and powerful measure of TFT design quality, needs to be maximized.
- **V_{TH}**, Threshold Voltage, in Volts, the minimum V_{GS} voltage that drain current I_D slightly exceeds a limit current ($1x10^{-7}$ A in our case) significant for the design, needs to be minimized.
- **SS**, Subthreshold Slope, in mV/decade, change in the gate voltage required to decrease the drain current I_D by one decade, $SS = \Delta V_{GS}/\Delta \log(I_D)$, needs to be minimized.
- **DIBL**, Drain-Induced Barrier Lowering, in mV/V, represents the drain voltage V_{DS} influence on the threshold voltage V_{TH}, defined as $DIBL = |\Delta V_{TH}|/|\Delta V_{DS}|$, needs to be minimized.

as these are the primary parameters for evaluation of thin film transistors' performance. [26]

g. Selection process for the FGM – Creation of a custom figure of merit

At the end of calculation process, we introduce and propose a unitless figure of merit as Equation-4:

$$FOM_{FET} = \frac{97.62(log(I_{ON}/I_{OFF}))^3\,(-log(I_{GL}))^3}{(10V_{TH})^3\,.\,DIBL^2\,.\,SS}$$

with which we can evaluate the overall performance of FinFET under consideration. We developed this figure of merit that equally and mostly cares for I_{GL}, I_{ON}/I_{OFF} ratio and V_{TH}, gives less importance to DIBL and even lesser importance to SS. Overall FOM value is multiplied by an arbitrary constant 97.62 to achieve best performing FinFET to appear with FOM_{FET} value equals to 100 and all other performance values to be normalized between 1 and 100. We compared the FOM_{FET} values of all single and FGM dielectric configurations so that it may help better to decide the selection among all configurations.

IV. RESULTS AND DISCUSSION

a. I_D - V_{GS} transfer characteristics

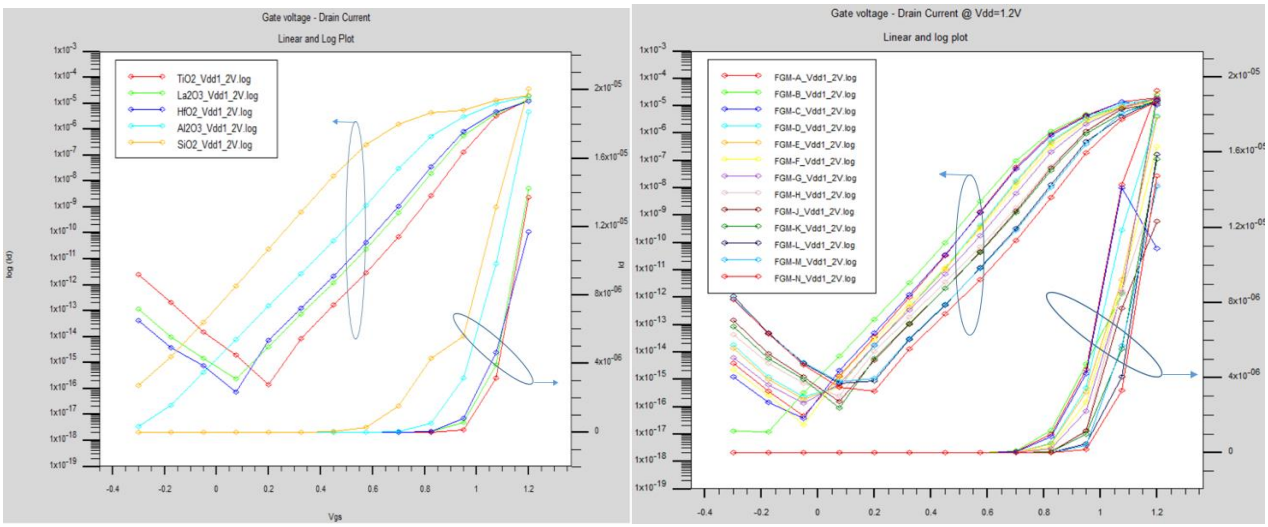

Figure 6a. I_D for single material gate oxide dielectrics (control group) log(I_D) –V_{GS} (left) and I_D –V_{GS} (right)

b. I_D current for FGM-group of gate oxide dielectrics log(I_D) –V_{GS} (left) and I_D –V_{GS} (right)

Figure 6. shows the drain current (Id) versus gate-source voltage (Vgs) characteristics for the FinFET device we examined with various gate dielectric materials. The threshold voltage is the point where the curve starts to steeply rise, which is a critical parameter for switching characteristics. The graph includes TiO_2, La_2O_3, HfO_2, Al_2O_3, and SiO_2 as gate dielectrics. These materials are high-k dielectrics, with the exception of SiO2, which is a traditional dielectric material with a lower dielectric constant. TiO_2 seems to have a higher on-current for the same gate voltage compared to the

others, which may suggest better channel formation or a higher dielectric constant, which can modify the effective channel thickness. The choice of dielectric material significantly impact device performance. Higher-k materials like HfO_2 and TiO_2 may allow for thinner dielectrics, which can enhance gate control and reduce leakage currents, while also allowing for scaling down the device dimensions.

b. **I_G per V_{GS} leakage current**

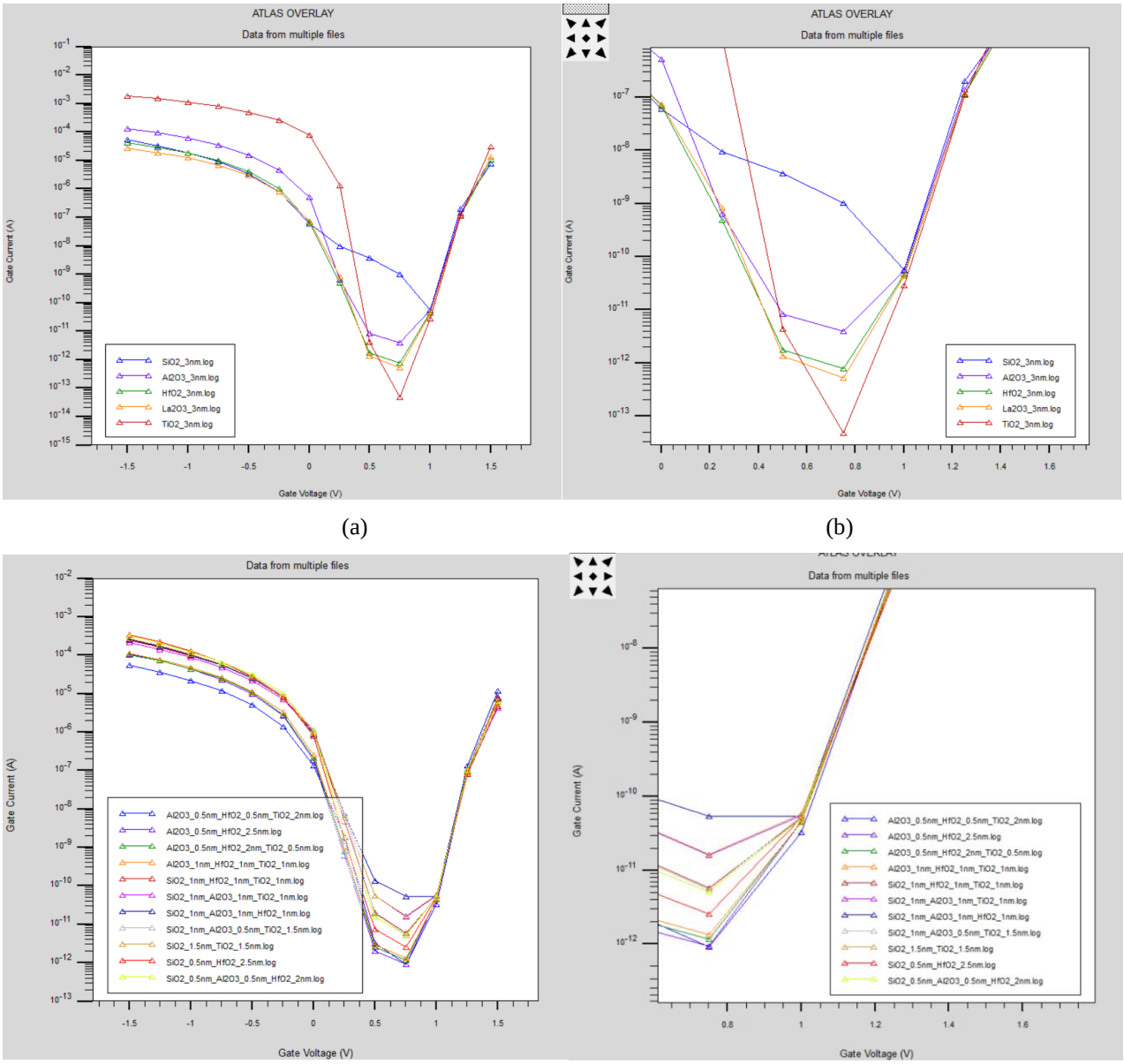

Figure 7a, 7b (zoom): I_G leakage current for single material gate oxide dielectrics (control group) log (I_G) –V_{GS}

7c, 7d (zoom): I_G leakage current for FGM group gate oxide dielectrics, log (I_G) –V_{GS}

This graph shows the leakage current characteristics in hot electron/hole injection model [4] for traditional single material gate dielectrics like TiO_2 having least leakage current around 10^{-13} A at 0.75V for our specific FinFET under examination depicted in Figure 1. The curves generally show a similar trend, with this leakage current decreases with increasing gate-source voltage due to better formation of depletion region. The right graph displays the leakage current for FinFETs with FGM gate oxides, labeled FGM-A through FGM-N. The curves are closely grouped and follow a similar trend to the control group, but with some variation between the different FGM materials. Lower leakage current is preferable, especially for memory devices like EEPROMs where high I_G can contribute to charge loss and memory degradation over time. The performance of FGMs in terms of I_G appears similar to single-material dielectrics, suggesting that FGMs might provide not significant but slight advantage in reducing I_G, but they also do not exhibit any deficiency in device reliability.

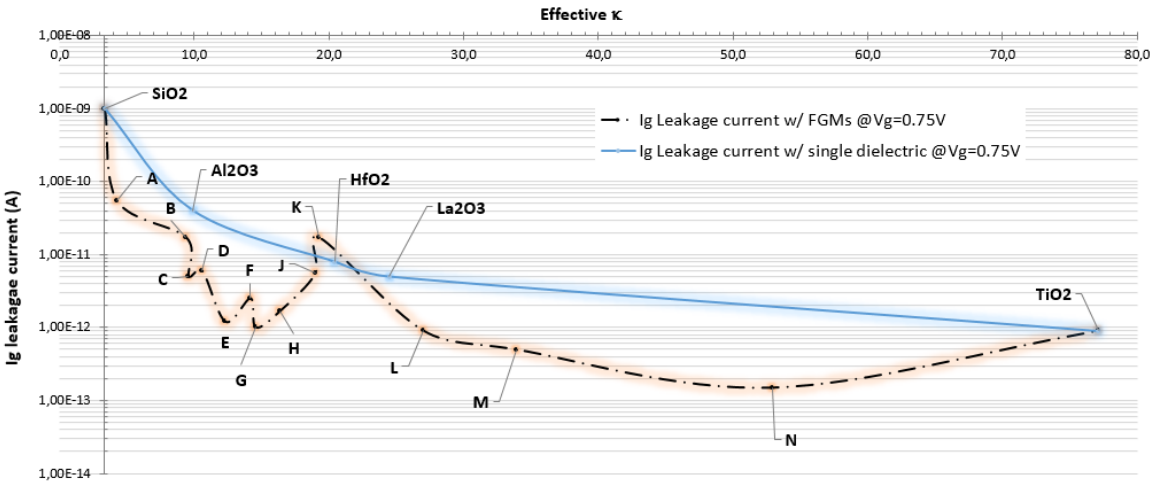

Figure 8. Ig Leakage Current for FinFET with single material and FGM gate oxide dielectrics (κ calculated with MG model)

We realize that usage of FGM dielectrics has potential of generating lower leakage currents from gate to channel, and for FGM-N, it is almost 53 times less than that of the FinFET with single HfO_2 dielectric, as it becomes evident that interface effects minimize when smoother transitions of dielectric constant are fabricated starting from channel to gate material.

c. **Drain Induced Barrier Lowering**

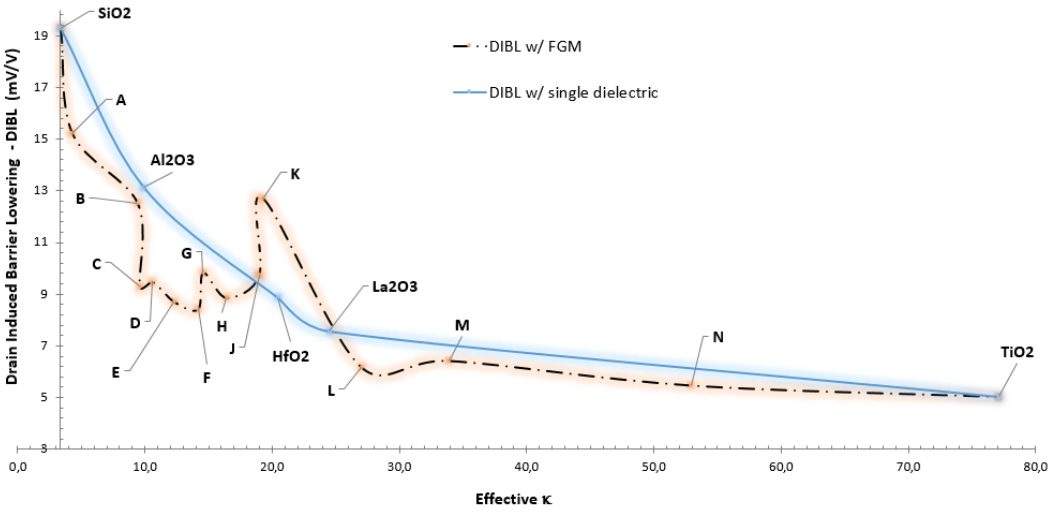

Figure 9. DIBL with single material and FGM gate oxide dielectrics (κ calculated with MG model)

Figure 9 plots the Drain Induced Barrier Lowering (DIBL) against the effective dielectric constant (k) for different materials used in FinFETs. As DIBL is the short-channel effect where the drain voltage can influence the threshold voltage of the transistor, a lower DIBL value does generally better because it means the device has better control over the threshold voltage and is less susceptible to variations due to changes in the drain voltage. DIBL with single dielectric (Solid Line) represented the DIBL performance across a range of dielectrics for a standard single-layer dielectric material, starts high with SiO_2 and then decreases significantly as the effective κ increases, showing improved performance for materials with higher κ values like HfO_2, Al_2O_3, and TiO_2. The trend suggests that as the effective dielectric constant increases, the DIBL effect decreases, which is a favorable outcome. DIBL values when using FGM techniques have peaks (labeled from A to N) that indicate where the DIBL is higher, possibly due to process variations, material properties or anomalies. DIBL performance of FGM's seems best for FGM-N with 5.48 mV/V which is %38.2 lower than that of HfO_2.

d. Subthrehold Slope

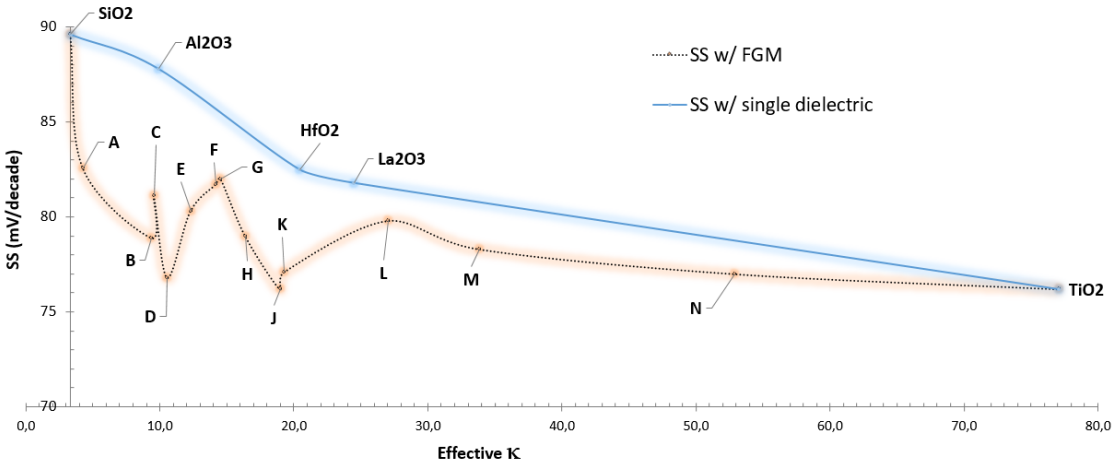

Figure 10. SS with single material and FGM gate oxide dielectrics (Effective κ calculated with MG model)

Subthreshold slope performance of FGM's seems best for FGM-K with 76.2 mV/decade which is %7.64 lower than that of HfO_2.

e. Off-State I_D Current

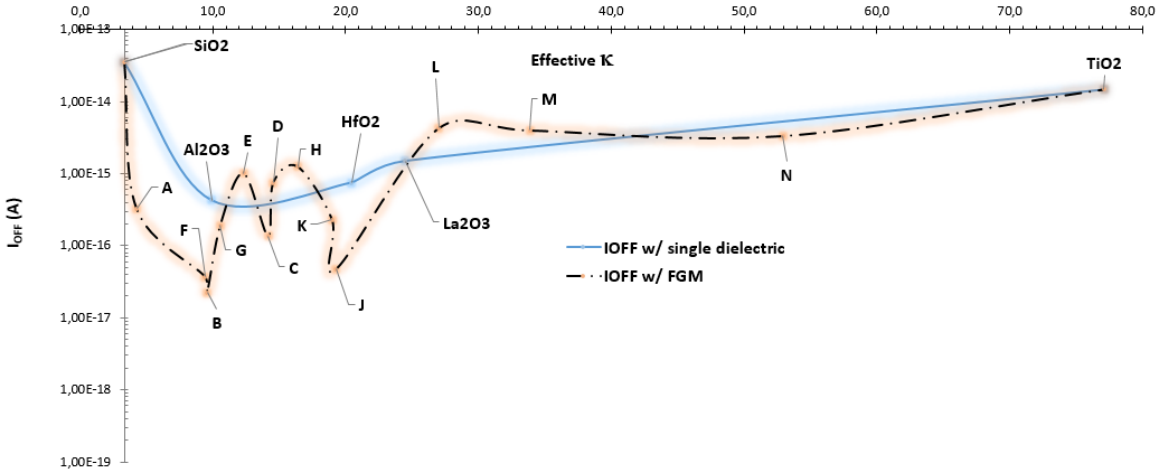

Figure 11. I_{OFF} with single material and FGM gate oxide dielectrics (Effective κ calculated with MG model)

Off-State I_D Current performance of FGM's seems better for FGM-B with $2.23x10^{-17}$ A which is almost 2 orders of magnitude lower than that of HfO_2.

a. On-State I_D Current

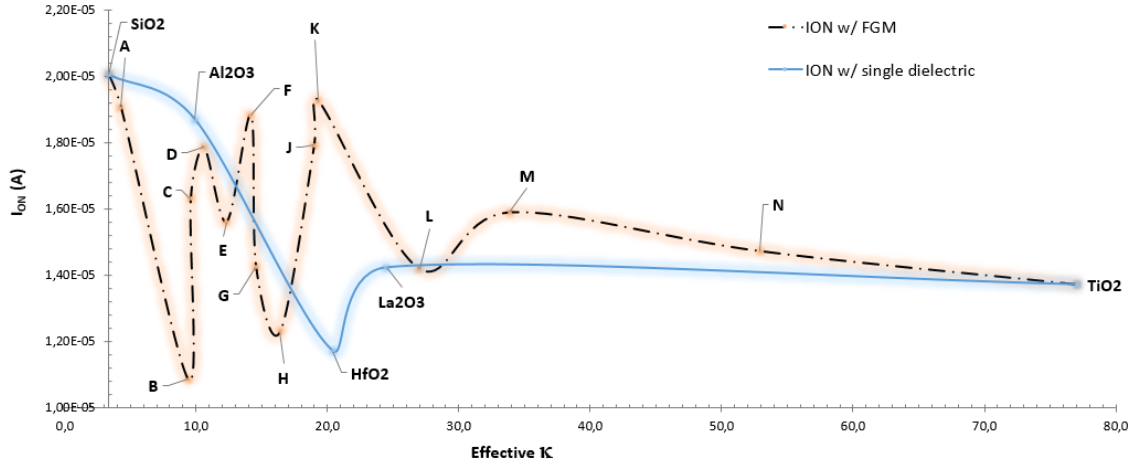

Figure 12. I_{ON} with single material and FGM gate oxide dielectrics (Effective κ calculated with MG model)

ON-State I_D Current performance for FGM-K with $1.93x10^{-5}$ A which is almost %62 better than that of with HfO_2.

b. I_{ON} / I_{OFF} Ratio

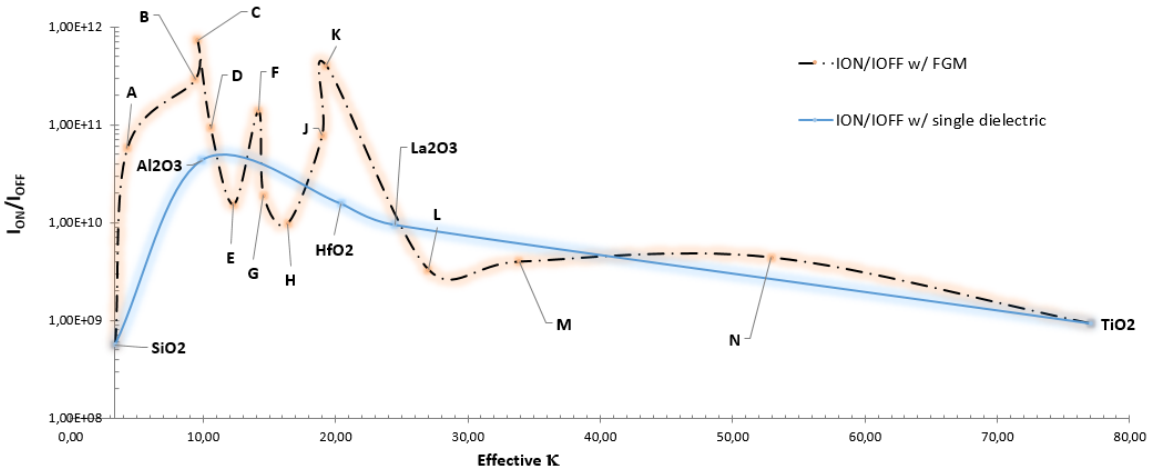

Figure 13. I_{ON}/I_{OFF} ratio with single material and FGM gate oxide dielectrics (Effective κ calculated with MG model)

I_{ON}/I_{OFF} ratio performance of FGM is better for FGM-C with $7.31x10^{11}$ which is almost 45 times better than that of HfO_2.

c. Threshold Voltage V_{TH}

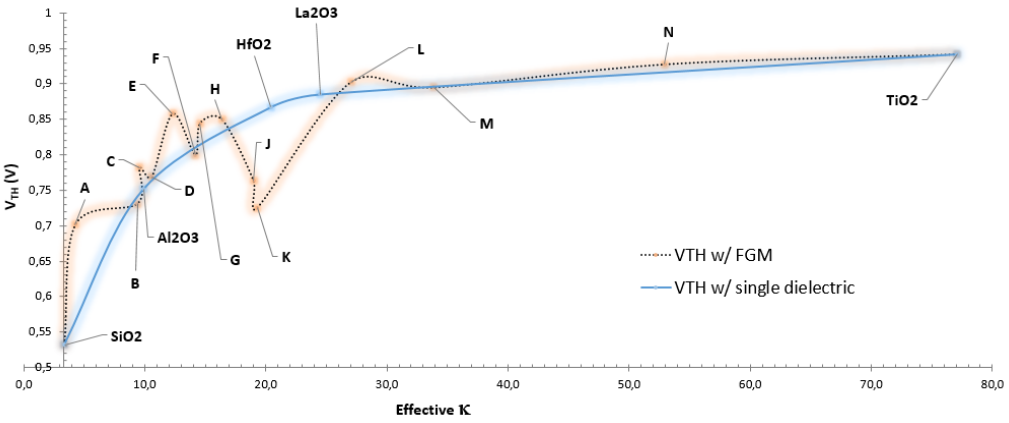

Figure 14. V_{TH} with single material and FGM gate oxide dielectrics

V_{TH} performance of FGM is better for FGM-A with 0.7012 V which is almost %19.2 better than that of HfO_2.

V. CONCLUSION

The FGM technique may offer a way to engineer specific device characteristics, but it requires careful control and understanding of the material properties to achieve the desired outcomes consistently. Our results indicate that proposed FinFET with FGM gate dielectrics has lesser I_{GL} up to 53 times, lesser DIBL up to %38.2, lesser SS up to %7.6, lower I_{OFF} up to 2 decades, higher I_{ON} up to %62, higher I_{ON}/I_{OFF} up to 45 times and lesser V_{TH} up to %19.2.

Table 5. FOM_{FET} values for each configuration of single dielectric and FGM configurations.

Material	FOM_FET
SiO2	9,5
Al2O3	20,6
HfO2	33,4
La2O3	43,0
TiO2	76,0
FGM-A	20,0
FGM-B	70,2
FGM-C	70,9
FGM-D	38,4
FGM-E	45,6
FGM-F	38,0
FGM-G	58,0
FGM-H	41,6

FGM-J	40,3
FGM-K	56,1
FGM-L	65,9
FGM-M	69,3
FGM-N	100,0

Looking at the FOM_{FET} values calculated by Equation-4, single dielectric gate oxides TiO2 has the best performance. HfO_2 performance achieved 33.4 whereas FGMs B, C, K, L, M and N achieve better than HfO_2 and entire single material dielectrics except TiO_2.

FGM approach aimed to improve the gate's control over the channel and seemed to achieve a success with respect to the FOM_{FET} selected as a figure of merit for overall FinFET performance, which can be always be customized due to importance of the performance parameter selected by the designer. FGMs seem to provide some space to engineer new gate oxides between dielectric constants 35-95 and at least to try these as gate dielectric material. With respect to the same FinFET with single layer HfO_2 gate dielectric performance, most FGMs showed superior performance. Within gate insulators and BOX structures, FGMs may provide versatile opportunities for optimizing FinFET devices.

VI. ACKNOWLEDGMENTS

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