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3D modelling based comprehensive analysis of high-κ gate stack graded channel dual material trigate MOSFET

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Abstract: The evolution of the traditional metal oxide semiconductor field effect transistor (MOSFET) from planar single gate devices into 3D multiple gates has led to higher package density and high current drive. However, due to continuous scaling and as a consequent close proximity between source and drain in the nano-regime, these multigate devices have been found to suffer from performance degrading short channel effects (SCEs). In this paper, a three dimensional analytical model of a trigate MOSFET incorporating non-conventional structural techniques like silicon-on-insulator, gate and channel engineering in addition to gate oxide stack is presented. The electrostatic integrity and device capability of suppressing SCEs is investigated by deriving the potential distribution profile using the three dimensional Poisson's equation along with suitable boundary conditions. The other device parameters like threshold voltage and subthreshold swing are produced from the surface potential model. The validity of the proposed structure is established by the close agreement among the results obtained from the analytical model and simulation results.

Key words: silicon-on-nothing; short channel effects; dual material gate; graded channel; trigate MOSFET
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1. Introduction

The unremitting device scaling for continuous growth of silicon technology has resulted in higher device density alongside the extraordinary functional capacity in terms of high current drive in semiconductor integrated chips (ICs)[1]. However, the current CMOS logic circuits not only require high transconductance but also low leakage and low subthreshold swing. The device scaling has weakened the gate control over the channel due to the increased influence of the drain voltage in the channel in addition to lowering of the source potential barrier in a traditional planar bulk MOSFET. This has resulted in the introduction of performance degrading short channel effects (SCEs) like drain induced barrier lowering (DIBL), $V_{\rm th}$ roll-off, higher subthreshold swing (SS), and hot carrier effects (HCEs) in nanoscale planar MOSFET[2, 3]. In order to mitigate the underlying SCEs, the nanoscale MOSFET has ushered in non-conventional structures like trigate and SOI[4–6]. The trigate (TG) configuration enhances threefold the gate control over the channel and its innate ability of suppressing various SCEs has subsequently forged into an appealing structural choice to continue the MOSFET scaling trend[7, 8]. Further, the multiple material gate and graded channel have also demonstrated aptness in diminishing the deteriorating impact of draining the electric field on the channel[9, 10]. The use of high-κ gate dielectric and gate stack (GS) in nanometer MOSFET has been found effective in reducing the gate leakage current and attaining enhanced control of the channel[11, 12]. The techniques of separating the device body and substrate by a buried insulating layer (BL) has further improved the device electrostatics by reducing parasitic capacitances[13].

Goel *et al*.[14] have reported a 2-D analytical threshold model of a graded channel dual material double gate MOSFET and have reported that the optimized values of gate-length ratio, doping concentrations, and gate materials can effectively control performance degrading effects like threshold voltage roll-off, HCEs, and DIBL. A 3D analytical surface potential model of Trigate SOI MOSFET has been given by Ghanatian and Hosseini while the performance analysis of a dual material trigate-silicon-on-nothing (SON) MOSFET has been proposed by Pritha *et al.* employing a gate electrode composed of two materials to improve the device ability in mitigating SCEs[15, 16].

To combine the advantages of gate and channel engineering alongside the high-κ GS and BL with TG MOSFET, a new device structure called gate-stack graded-channel dual material trigate (GSGCDMT) SON MOSFET is proposed in this work where the BL layer is composed of air/vacuum. An analytical model of the proposed structure has been developed illustrating the potential distribution, electric field profile, $V_{\rm th}$, and SS. The rest of the paper has been organized as follows. The proposed GSGCDMT-SON-MOSFET is demonstrated in Section 2. The 3-D analytical model is derived in section 3. Results and discussions are presented in Section 4. The conclusion is drawn in Section 5.

2. Device structure

The proposed structure of GSGCDMT-SON MOSFET

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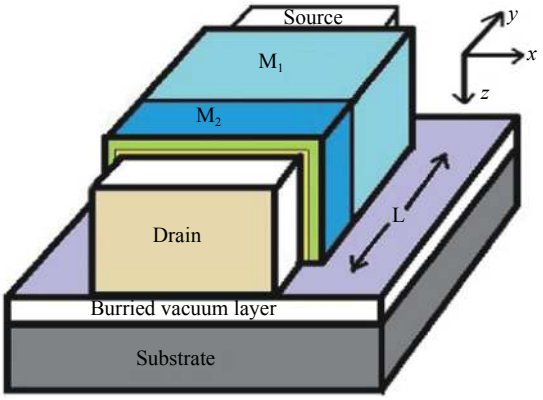

Fig. 1. (Color online) 3-D schematic of gate-stack graded-channel dual material trigate MOSFET.

has been shown in Fig. 1. The device consists of a channel being surrounded by gate electrodes on three sides. The gate is engineered to be made of two metals of M_1 and M_2 with work-functions ϕ_{m1} = 4.8 eV and ϕ_{m2} = 4.4 eV respectively. The length of gate metals are in the ratio of 2 : 1. The channel is graded into two regions with two different doping concentrations $Na_1 = 1.5 \times 10^{20}$ cm^{-3} and $Na_2 = 1 \times 10^{18}$ cm^{-3}, and the ratio of the lengths of the two regions is 1 : 2. The device channel and substrate are separated by a buried insulating layer of air. The source and drain doping concentrations are $N_D = 2 \times 10^{26}$ m^{-3}. The other device parameters - channel length (L), thickness of BL layer t_{box}, thickness of channel (t_{Si}), and width of channel (w) are taken as 40, 10, 30, and 10 nm respectively. The stacked gate oxide is composed of two oxides: low-κ silicon dioxide (SiO_2) and high-κ hafnium dioxide (HfO_2) with thickness t_{SiO_2} = 1 nm and t_{HfO_2} = 2 nm respectively. The high-κ oxide layer helps in overcoming the leakage and scaling problems while SiO_2 provides the interface stability and mitigates the fringing fields. In order to calculate the effective oxide thickness (EOT), the use of EOT = $t_{\text{High-}\kappa}\frac{\varepsilon_{SiO_2}}{\varepsilon_{\text{High-}\kappa}}$ is considered inappropriate for non-planar devices, so we have considered the expression given in Eq. (1) for calculating the EOT in the proposed trigate MOSFET [17]

$$\text{EOT} = \frac{w}{\mathcal{F}_{\text{High-}\kappa}}\left[\left(1+\mathcal{F}_{\text{High-}\kappa}\frac{t_{SiO_2}}{w}\right)^{\frac{\mathcal{F}_{\text{High-}\kappa}\varepsilon_{\text{High-}\kappa}}{\mathcal{F}_{SiO_2}\varepsilon_{SiO_2}}}-1\right], \quad (1)$$

where t_{SiO_2}, ε_{SiO_2}, $\varepsilon_{\text{High-}\kappa}$, and $\mathcal{F}_{\text{High-}\kappa}$ are dielectric thickness of SiO_2, dielectric constant of SiO_2, and high-κ dielectric respectively. $\mathcal{F}_{\text{High-}\kappa}$ and $\mathcal{F}_{SiO_2}$ are fitting parameters of SiO_2 and high-κ dielectric (HfO_2) whose values are estimated as 1.5 and 0.95 respectively.

3. Analytical model formulation

In order to have better insight into the operation of the proposed MOSFET structure, the physics based compact analytical model of the surface potential and threshold voltage has been presented in this section.

3.1. Surface potential modeling

The device considered is GSGCDMT-SON MOSFET and has been divided into three regions – Region 1 corresponding to halo doping Na_1 controlled by gate material M_1 of length L_1, Region 2 corresponds to doping Na_2 under the control of gate material M_1, and Region 3 corresponds to channel doping of Na_2 and gate material M_2 given as

$$\text{Region 1: } 0 \leqslant y \leqslant L_1;\ 0 \leqslant z \leqslant t_{Si};\ -\frac{w}{2} \leqslant x \leqslant \frac{w}{2}, \quad (2)$$

$$\text{Region 2: } L_1 \leqslant y \leqslant L_2 - L_1;\ 0 \leqslant z \leqslant t_{Si};\ -\frac{w}{2} \leqslant x \leqslant \frac{w}{2}, \quad (3)$$

$$\text{Region 3: } L_2 \leqslant y \leqslant L - L_3;\ 0 \leqslant z \leqslant t_{Si};\ -\frac{w}{2} \leqslant x \leqslant \frac{w}{2}. \quad (4)$$

The source is assumed to be grounded and drained at a potential V_{DS}. The gate-source voltage (V_{GS}) is common to trigate and across different gate materials. As the potential in the channel gradually increases from source to drain, this variation can be approximated by a parabolic function[18]. If λ = 1, 2, and 3 represent the channel region, then the potential profile between the lateral gates can be written as

$$\psi_\lambda(x,y,z) = \mu_{0\lambda}(y,z)x^2 + \mu_{1\lambda}(y,z)x + \mu_{2\lambda}(y,z), \quad (5)$$

where $\psi_1(x, y, z)$, $\psi_2(x, y, z)$, and $\psi_3(x, y, z)$ represent the electrostatic potential distribution in Region 1, Region 2, and Region 3.

The coefficients of Eq. (5) can be found using following boundary conditions[19]

$$\psi_1(x,y,z)\big|_{y=0} = V_{bi,1}, \quad (6a)$$

$$\psi_1(x,y,z)\big|_{y=L} = V_{bi,2} + V_{DS}. \quad (6b)$$

$V_{bi,1}$ and $V_{bi,2}$ are the built-in potential at the source/channel and drain/channel junction respectively.

The electric field at the gate–oxide and channel interface is assumed to be continuous in GSGCDMT-SON MOSFET, we have

$$\left.\frac{d\psi_\lambda(x,y,z)}{dz}\right|_{x=0,z=0} = \frac{\varepsilon_{eff}}{\varepsilon_{Si}.EOT}\left(\psi_{s\lambda}(y) - V'_{GS\lambda}\right), \quad (6c)$$

$$\left.\frac{d\psi_\lambda(x,y,z)}{dz}\right|_{x=0,z=t_{Si}} = \frac{\varepsilon_{BL}}{\varepsilon_{Si}t_{BL}}\left(V'_{sb\lambda} - \psi_{sb\lambda}(y)\right). \quad (6d)$$

Because of the symmetry along the x-direction as shown in Fig. 2(b), we have

$$\psi_\lambda\left(-\frac{w}{2},y,z\right) = \psi_\lambda\left(+\frac{w}{2},y,z\right). \quad (6e)$$

ε_{eff}, ε_{BL}, and ε_{Si} are the dielectric constant of the front gate oxide, BL, and silicon body respectively. EOT and t_{BL} are the thicknesses of the front gate oxide and BL respectively. $V_{GS}' = V_{GS} - V_{Fb\lambda}$, where V_{Fb1}, V_{Fb2}, and V_{Fb3}, represent the channel flatband voltage in Region 1, Region 2, and Region 3 respectively. $V_{sb\lambda}' = V_{sub} - V_{Fbb\lambda}$, V_{sub} is the substrate bias voltage and $V_{Fbb\lambda}$ is the back channel interface flatband voltage. $\psi_{s\lambda}(y)$ and $\psi_{sb\lambda}(y)$ represent the front channel surface potential and back channel potential.

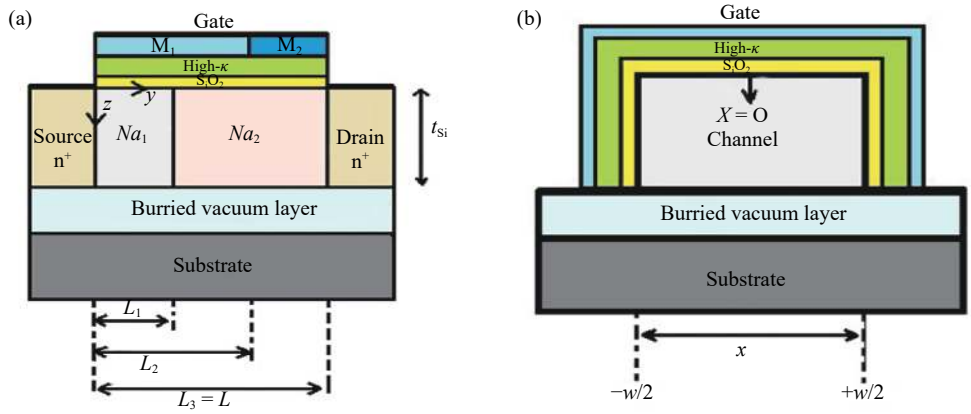

Fig. 2. (Color online) Cross-sectional view of graded-channel gate-stack dual material trigate MOSFET.

Using above boundary conditions, the coefficients are obtained as

$$\mu_{0\lambda}(y,z)=\left(\frac{4}{w^2}\left(\psi_{s\lambda}(y)-\mu_{2\lambda}(y,z)\right)\right), \tag{7}$$

$$\mu_{1\lambda}(y,z)=0. \tag{8}$$

The coefficient $\mu_{2\lambda}(x, y)$ can be derived by assuming the parabolic potential profile in the vertical direction for low V_{DS} such that the potential in the center plane of the channel of GSGCDMT-SON MOSFET can be written as [20]:

$$\mu_{2\lambda}(y,z)=\psi_s(y)+\frac{\varepsilon_{eff}}{\varepsilon_{Si}.EOT}\left(\psi_s(y)-V'_{GS\lambda}\right)z-\frac{\left[\left(\frac{C_{BL}}{C_{eff}}+\frac{C_{BL}}{C_{Si}}+1\right)\psi_{s\lambda}(y)-\left(1+\frac{C_{BL}}{C_{Si}}\right)V'_{GS1}\right]\frac{C_{eff}t_{BL}}{\varepsilon_{BL}}-V'_{sb\lambda}}{t_{Si}^2\left(1+2\frac{C_{Si}}{C_{BL}}\right)}z^2, \tag{9}$$

where C_{eff}, C_{BL}, C_{Si} represent the effective front gate oxide capacitance, BL capacitance, and Si channel capacitance.

The surface potential $\psi_{s\lambda}$ in GSGCDMT-SON MOSFET can be calculated by solving a three dimensional Poisson's equation [21] given by

$$\frac{\partial^2\psi(x,y,z)}{\partial x^2}+\frac{\partial^2\psi(x,y,z)}{\partial y^2}+\frac{\partial^2\psi(x,y,z)}{\partial z^2}=-\frac{qNa_j(x,y,z)\big|_{j=1,2}}{\varepsilon_{Si}}, \tag{10}$$

where $Na_j(x,y,z)\big|_{j=1,2}=\left(Na_j+n(x,y,z)\right)$, and $n(x, y, z)$ is the mobile electron charge density and j corresponds to channel doping. Considering full depletion approximation for the channel under zero bias condition and $Na_j \gg n(x,y,z)$ such that $Na_j(x,y,z)\cong qNa_j$, q is electron charge.

On solving Eqs. (5) and (10) using the coefficients derived in Eqs. (7), (8), and (9), we get

$$\frac{\partial^2\psi_{s\lambda}(y)}{\partial y^2}-\alpha\psi_s(y)=\beta_\lambda-2\frac{t_{Si}}{\delta C_{Si}}\left[w^2-4\left(x^2+z^2\right)-\right]V'_{sb\lambda}, \tag{11}$$

$$\alpha=\left\{8\frac{C_{eff}}{\delta}\left[t_{Si}^2\left(1+\frac{C_{Si}}{C_{BL}}\right)\right]z+2\frac{C_{Si}}{\delta t_{Si}}\left[\frac{C_{eff}}{C_{BL}}+\frac{C_{eff}}{C_{Si}}+1\right]\times\left(w^2-4\left(y^2+z^2\right)\right)\right\},$$

$$\beta_\lambda=qNa_{|}w^2\delta^{-1}\left(1+2\frac{C_{Si}}{C_{BL}}\right)t_{Si}^2+4t_{Si}^2\frac{\varepsilon_{eff}}{EOT\delta}\left(1+2\frac{C_{Si}}{C_{BL}}\right)\times xt_{Si}^2V'_{GS\lambda}+\left(\frac{C_{eff}}{C_{BL}}+\frac{C_{eff}}{C_{Si}}\right)\left(w^2-\left(x^2+z^2\right)\right)\frac{C_{Si}}{t_{Si}\delta}V'_{GS\lambda},$$

$$\delta=\left(t_{Si}^2\left(1+2\frac{C_{Si}}{BL}\right)\right)\left(w^2\varepsilon_{Si}+C_{eff}\left(w^2-4z^2\right)x\right)-\left(\frac{C_{eff}}{C_{BL}}+\frac{C_{eff}}{C_{Si}}+1\right)\left(\varepsilon_{Si}\left(4z^2-w^2\right)x^2\right),$$

The general form of surface potential $\psi_{s\lambda}(y)$ in GSGCDMT-SON MOSFET can be obtained by solving the second order differential equation given in Eq. (11). Its solution is given as

$$\psi_{s\lambda}(y)=C_\lambda e^{\eta\mathcal{P}_\lambda}-\mathcal{D}_\lambda e^{-\eta\mathcal{P}_\lambda}-\sigma_\lambda. \tag{12}$$

Here $\sigma_\lambda=-\frac{\beta_\lambda}{\alpha}$, $\eta=\sqrt{\alpha}$, and $\mathcal{P}_\lambda$ takes the value $\mathcal{P}_1=y$, $\mathcal{P}_2=y-(L_2-L_1)$, and $\mathcal{P}_3=y-L_2$. C_λ and $\mathcal{D}_\lambda$ are arbitrary constants to be determined by using the following boundary conditions:

i. $\psi_1(x,L_1,z)\big|_{x=0,z=0}=\psi_2(x,(L_2-L_1),z)\big|_{x=0,z=0}$

ii. $\psi_{s1}(L_1)=\psi_{s2}(L_2-L_1)$

iii. $\left.\frac{d\psi_{s1}(x,y,z)}{dy}\right|_{y=L_1}=\left.\frac{d\psi_{s2}(x,y,z)}{dy}\right|_{y=L_2-L_1}$

iv. $\psi_2(x,L_2,z)\big|_{x=0,z=0}=\psi_3(x,L_2,z)\big|_{x=0,z=0}$

v. $\psi_{s2}(L_2)=\psi_{s3}(L_2)$

vi. $\left.\frac{d\psi_{s2}(x,y,z)}{dy}\right|_{y=L_2}=\left.\frac{d\psi_{s3}(x,y,z)}{dy}\right|_{y=L_2}$.

Using the above boundary conditions, we get the coefficients C_λ and $\mathcal{D}_\lambda$ as

$$C_1=\left\{\left(V_{bi,2}+V_{DS}+\sigma_3\right)-\left(V_{bi,1}+\sigma_1\right)e^{-\eta L}+(\sigma_1-\sigma_2)\cosh(\eta(L_3-(L_1-L_2)))+(\sigma_2-\sigma_3)\cosh\eta(L_3-L_2)\right\}\{2\sinh(\eta L)\}^{-1},$$

Table 1. Employed device parameters.

Device structure	ϕ_{m1} (eV)	ϕ_{m2} (eV)	Na_1 (cm^{-3})	Na_2 (cm^{-3})
Conventional	4.8	4.8	1.5×10^{20}	1.5×10^{20}
DMG	4.8	4.4	1.5×10^{20}	1.5×10^{20}
GC	4.8	4.8	1.5×10^{20}	1×10^{18}
DMG-GC	4.8	4.4	1.5×10^{20}	1×10^{18}

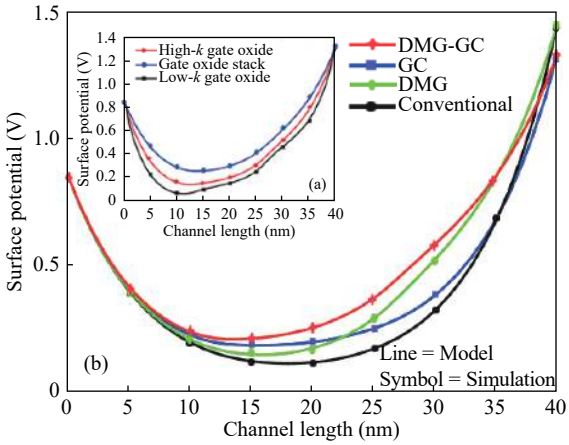

Fig. 3. (Color online) Surface potential distribution as a function of channel length. (a) Surface potential versus different gate oxide. (b) Surface potential distribution for conventional, DMG-, GC-, and DMG-GC- GS Trigate SON MOSFET as a function channel length.

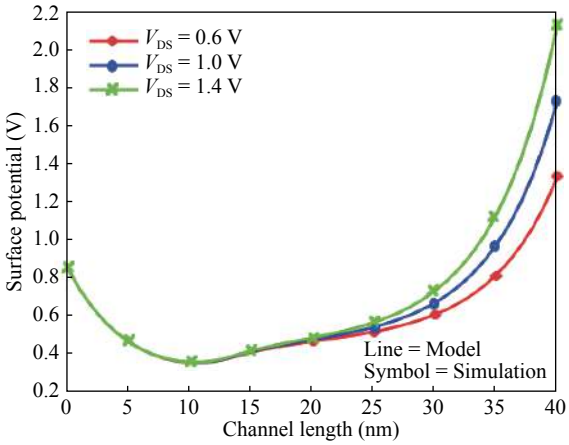

Fig. 4. (Color online) Surface potential distribution as a function of channel length for GSGCDMT SON MOSFET against different values of V_{ds}.

$$\mathcal{D}_1 = \left(V_{bi,1} + \sigma_1\right) - C_1,$$

$$C_2 = C_1 e^{\eta L_1} - (\sigma_1 - \sigma_2)/2,$$

$$\mathcal{D}_2 = \mathcal{D}_1 e^{-\eta L_1} - (\sigma_1 - \sigma_2)/2,$$

$$C_3 = C_2 e^{\eta}(L_2 - L_1) - (\sigma_2 - \sigma_3)/2,$$

$$\mathcal{D}_3 = \mathcal{D}_2 e^{-\eta}(L_2 - L_1) - (\sigma_2 - \sigma_3)/2.$$

3.2. Threshold voltage modelling

The threshold voltage is taken to be that value of gate source voltage (V_{GS}) at which the minimum surface potential $\psi_s(y_{min}) = 2\phi_F$, where ϕ_F is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level[22]. y_{min} is the position of minimum surface potential in the channel, which occurs under the higher work-function gate material (M_1), and can be calculated as:

$$\left.\frac{\partial^2 \psi_{s1}(y)}{\partial y^2}\right|_{y=y_{min}} = 0. \quad (13)$$

4. Result and discussion

To verify the proposed 3-D analytical model, all the device simulations have been performed using 3D device simulator ATLAS[23]. Several physics-based models are used for GSGCDMT-SON MOSFET simulation like the concentration dependent mobility model, transverse field and temperature dependent Arora models. Shockley-Read-Hall and Auger recombination model have also been employed in the simulation. The employed device parameters are as given in Table 1.

Fig. 3 shows the surface potential distribution plotted as a function of channel length for gate and channel engineered devices and against different gate oxides. Fig. 3(a) shows the comparison of surface potential distribution for different gate dielectrics for GSGCDMT-SON MOSFET. It can be observed that the high-κ dielectric (HfO_2 + SiO_2) gate stack increases the surface potential than a low-κ dielectric (SiO_2), implying higher gate capacitance and reduced gate leakage current while assuring small capacitive coupling than high-κ gate dielectric (HfO_2). The comparison of surface potential distribution between conventional (single material gate and non-graded channel), dual material gate (DMG), graded channel (GC), and the DMG-GC with gate stack TG SON MOSFET is shown in Fig. 3(b). The conventional TG device has the lowest minimum potential and has been found to suffer from DIBL due to V_{DS} fluctuations. With DMG TG device structure, the source junction is shielded from V_{DS} fluctuations because of the step in the potential profile. In the GC TG device, the high-doped implant is confined around the source region, while rest of the channel is lightly doped. The V_{th} of the device will be controlled by the implant region reducing the effective channel length resulting in a higher drive current. The DMG-GC TG device will be a high performance device as the DMG will shield the device against the DIBL effect and GC will improve the drain-to-source punch through resistance and consequently improve the short channel behavior of the device.

Fig. 4 shows the variation of the GSGCDMT-SON MOSFET surface potential distribution as a function of channel length for different values of drain voltage (V_{DS}). It can be observed that no or little change in surface potential distribu-

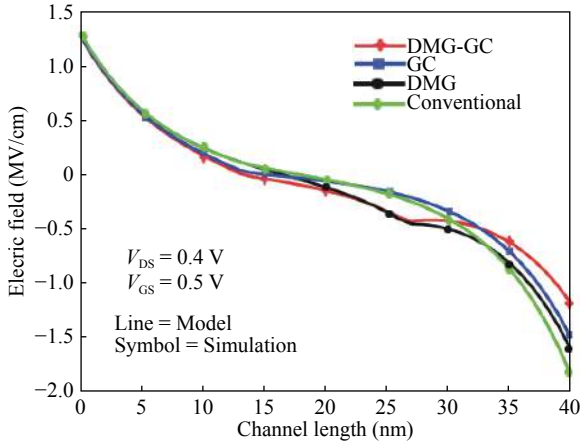

Fig. 5. (Color online) Variation of electric field along the channel for conventional, GCTG, DMTG, and GSGCDMT SON MOSFET.

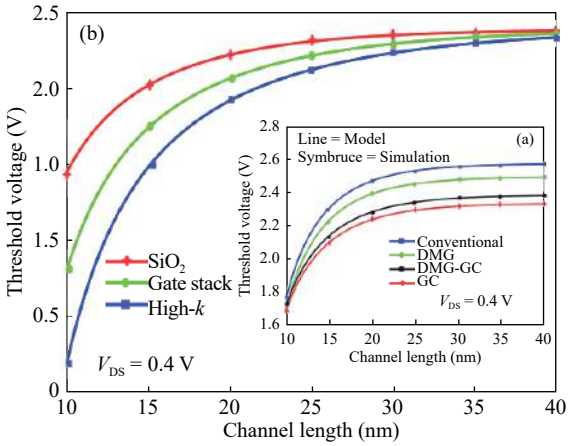

Fig. 6. (Color online) Threshold voltage variation as a function of channel length. (a) Threshold voltage variations for conventional, DMG-, GC-, and DMG-GC-GS Trigate SON MOSFET. (b) Threshold voltage variations for different gate oxides.

tion occurs in a major portion of the channel length except towards the drain side of the channel. This indicates the device's ability in suppressing the performance degrading DIBL effect due to gate and channel engineering techniques. The analytical and simulated values are in close agreement with each other. Fig. 5 shows the comparison in the variation of lateral electric field $E_{\lambda}(y) = -\partial\psi_{s\lambda}(y)/\partial y$ of DMG-GC, DMG, GC, and conventional gate stack TG SON MOSFET as a function of the position along the channel length[24]. It can be seen that the electric field is almost uniform throughout the channel and redistributes mostly at the drain side, which is a desired characteristic for superior device performance. The electric field at the drain in case of the proposed DMG-GC-GS-TG SON MOSFET is significantly reduced due to low doping of the corresponding channel region and use of low work-function gate material near the drain. This results in an enhanced HCE suppression thus improving device reliability.

Fig. 6 shows the plots of the threshold voltage as a function of position along the channel. In Fig. 6(a), the threshold voltage is compared between conventional, DMG, GC, and DMG-GC gate stack TG SON MOSFET as a function of channel length. It can be observed that the threshold at the smaller gate length tends to roll off due to the close proximity between source and drain and at the large gate length, remains constant. The V_{th} is minimum in the case of the graded channel as the high-doped channel region reduces the effective channel length while it is highest in the case of the conventional Trigate structure due to the higher channel potential barrier. The DMG-GC has a slightly higher V_{th} than the GC structure due to the dual material gate configuration and thus provides higher transconductance than the conventional and DMG trigate structure. Fig. 6(b) shows the influence of different gate oxides on the threshold voltage of GSGCDMT-SON MOSFET. It can be observed that the threshold roll off increases with high-κ gate dielectric signifying higher carrier velocity. The DMG-GC trigate SON MOSFET with HfO_2 as gate dielectric can be seen to provide higher threshold voltage roll-off due to higher field induced barrier lowering which substantiate faster device operation in addition to reduction of leakage current in the off state of the device.

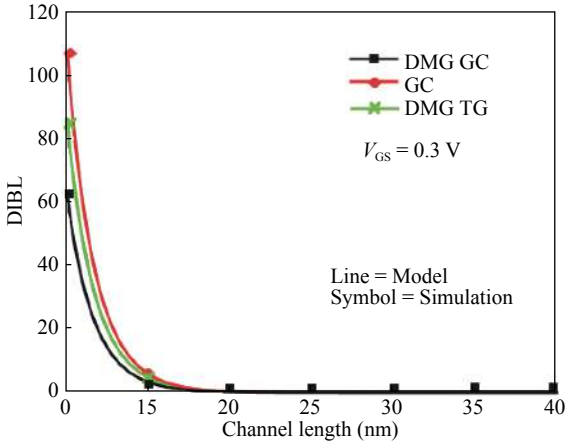

Fig. 7. (Color online) DIBL comparison along the channel for DMG, GC, and DMG-GC GS-TG-SON MOSFET. The symbols in the graph represent the simulated values from TCAD for the proposed model.

Fig. 7 shows the DIBL comparison of DMG, GC, and DMG-GC with GS TG SON MOSFET as a function of position along the channel from source to drain. It can be seen from the figure that the GSGCDMT SON MOSFET shows better performance in suppressing DIBL, which is defined as

$$\mathrm{DIBL} = \frac{\Delta V_{\mathrm{th}}}{\Delta V_{\mathrm{DS}}} = \frac{V_{\mathrm{th}}|_{\mathrm{lin}} - V_{\mathrm{th}}|_{\mathrm{sat}}}{V_{\mathrm{DS}}|_{\mathrm{sat}} - V_{\mathrm{DS}}|_{\mathrm{lin}}}.$$

This reduction of DIBL in GSGCDMT structure is due to better gate controllability and screening of the minimum potential position from V_{DS} due to gate and channel engineering techniques. The calculated and simulated values are in close agreement.

Fig. 8 shows the variation of the subthreshold swing $\mathrm{SS} = 2.3v_t\left[\frac{\mathrm{d}\phi_{s1}(y)}{\mathrm{d}V_{GS}}\Big|_{y=y_{\min}}\right]^{-1}$ along the channel length for the DMG, GC, and DMG-GC with GS TG SON MOSFET[25]. It can be observed that the subthreshold swing is minimum in the case of GSGCDMT -SON MOSFET. This can be attributed to the small off state leakage current and better gate control of the channel due to the graded channel and dual materi-

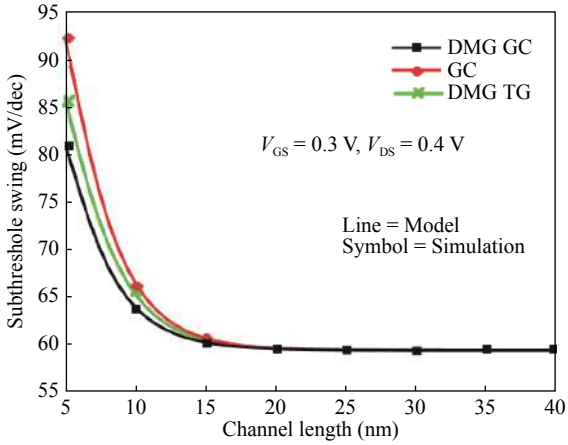

Fig. 8. (Color online) Subthreshold Swing comparison along the channel GC-, DMG-, and DMG-GC- GS-TG SON MOSFET. The symbols in the graph represent the simulated values from TCAD for the proposed model.

al gate architecture of the device. The subthreshold swing attains a maximum value of about 80 mV/dec at the source junction, and it gradually goes down and saturates to about 60 mV/dec. Thus, a major portion of the channel is protected against SCEs and hence improves the performance of nanoscale MOSFET. All this detailed analysis about SCEs over the proposed model brings us to a conclusion about the aptness of this structure to subdue various SCEs like DIBL, HCEs, and improve the device electrostatics. This makes the proposed MOSFET structure quite a promising candidate in the era of device miniaturization as the structure is compatible with conventional planar technology. The calculated and simulated results almost match each other.

5. Conclusion

In this work, the graded channel gate stack dual material trigate SON MOSFET has been investigated for SCEs in the nano regime by the developed analytical model of the surface potential and threshold voltage based on three dimensional Poisson's equation. The results obtained clearly establish that the proposed structure exhibits higher immunity to SCEs, which can be understood from the surface potential distribution, electric field, threshold voltage, DIBL, and subthreshold characteristics. The close agreement between the results obtained from the analytical model and the simulation validates the proposed model.

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