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ORIGINAL PAPER

Investigation and Design of Stacked Oxide Polarity Gate JLTFET in the Presence of Interface Trap Charges for Analog/RF Applications

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Abstract
In this manuscript, the reliability of stacked oxide (SO) heterogeneous gate dielectric polarity gate junction less tunnel FET (PG JLTFET) has been investigated. The stacked oxide PG JLTFET (SO PG JLTFET) has been implemented using a high-k gate dielectric material (HfO_2) layer that has been modeled on top of the silicon dioxide (SiO_2) layer to improve the device performance. The stacked oxide based approach leads to decrement in leakage current at gate-channel interface and improves the channel interface maintenance quality of the device. The study has been conducted by analyzing the effect of both donor and acceptor interface charges (ITCs), present at the interface of silicon and oxide layer. Various DC and analog/RF performance parameters such as electric field, carrier concentration, device efficiency, cut off frequency (f_T), input, output characteristics, higher order transconductance coefficients (g_{m2}, g_{m3}), transconductance frequency product (TFP) etc. have been analyzed. Besides, impact of ITCs on signal distortion and linearity for SO PG JLTFET using the parameters such as second order voltage intercept point (V_{IP2}), third order voltage intercept point (V_{IP3}), third order input intercept point (IIP_3), third order intermodulation distortion (IMD_3) and 1-dB compression point have been studied in depth. The results obtained have also been compared with conventional polarity gate JLTFET (PG JLTFET). It has been observed, that the SO PG JLTFET is less sensitive to ITCs as compared to PG JLTFET.

Keywords TFET · PG JL-TFET · Inter face trap charge · Interface · Analog/ RF · CMOS

1 Introduction

According to the current trend in semiconductor industry, the device performance, reliability and power consumption are some of the stringent issues to be dealt with. In order to decrease power consumption and improve the device performance, Moore's law is followed, leading to reduction in the size of semiconductor device. However, with the following of Moore's law, certain reliability issues have emerged. Scaling down of MOSFETs makes the device prone to many challenges faced by nanoscale CMOS technology such as short channel effects (SCE), hot carrier effect (HCE) and drain induced barrier lowering (DIBL) [1]. Therefore, changes in device structures and new fabrication methods are imperative in order to maintain the desired performance reliability as progress is made from one generation of semiconductor devices to another. Owing to the above mentioned issues, conventional MOSFETs are being substituted with variety of alternative device structures such as double gate [1], tri gate [2] and gate-all-around (GAA) MOSFETs [3]. In this scenario, Tunnel FETs (TFETs) have been gaining a lot of attention recently. TFETs operate on the principle based on quantum tunneling mechanism across the barrier, while in case of conventional MOSFETs, working principle is based on thermionic emission across the barrier. Thus, dissipation of less power occurs in TFET and hence, can be used for low-power applications [4–6]. It shows very less OFF-state current and steep subthreshold slope (SS < 60 mV/decade). TFETs also provide robustness towards drain induced barrier lowering (DIBL) and short channel effects [4, 7–11].

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Even though TFETs provide multiple advantages, however, they possess few challenges such as low current driving capability and ambipolar behavior [11]. Ambipolarity refers to conduction of current for both positive gate bias and negative gate bias. Ambipolarity occurs mainly because of the shifting of tunnel junction from source side towards the drain side in case of operation of n-type TFET when the gate to source voltage, $Vgs < 0$ [11]. Studies have been conducted to use alternative materials with lower bandgap such as indium arsenide (InAs) [12, 13] over Si TFETs to improve the ON-state current in TFETs. Since, TFETs work on the basis of p-n junction thus; fabrication of these junctions for short channel devices is becoming extremely stringent because of their requirement of very sharp doping profile. In order to overcome the aforementioned issues, researchers have proposed junction less TFETs (JLTFETs) as a more viable option because they are devoid of any metallurgical junction. However, they are simpler to fabricate, since for the formation of drain, channel and source region, it avoids the need for any physical doping and has enhanced efficiency. [14–16]

JLTFET is also free from random-dopant fluctuations (RDF), making it less susceptible to degradation in its electrostatic behavior. The effects of random dopant fluctuations in TFETs have been demonstrated in [17–21]. JLTFETs make use of techniques such as spacer material band gap, engineering of gate work function, improvisation of high-k dielectric and polarity gate control so that the device performance can be made better. To overcome reliability issues, engineering of work function is applied at polarity and control gates. Concept of polarity gate engineering is used, in which the polarity gate terminal is biased with external voltage in order to create p^+ region below polarity gate [22].

Due to the continuous scaling of devices, gate oxide thickness is reducing continuously. Due to this phenomenon, leakage takes place at the gate oxide-silicon interface, thus impeding device performance [23]. Thus, to overcome this issue, high-k materials are introduced, along with the gate oxide-stack in the oxide region. As the high-k materials are introduced, coupling capacitance between channel and gate electrode becomes better, thus leading to improvement in SS and ON state current. The gate-oxide-stack approach using HfO_2/SiO_2 leads to decrement in leakage current at gate-channel interface and improves the channel interface maintenance quality of the device [23].

When nanoscale devices are fabricated, interface trap charges (ITCs) usually occur due to stress and radiation- induced damages, caused due to fixed and mobile ionic charges getting trapped at the semiconductor-insulator interface [24]. These charges lead to impeding of the reliability and lifetime of device performance, affecting the device efficiency. A donor interface trap charge which is devoid of electrons can show the behavior of positive localized charge, or electron filled neutral localized charge. On the other hand, an acceptor interface trap which is devoid of holes displays the behavior of electron filled negative localized charge, or neutral localized charge. Various researches on the study of ITCs on JL-TFETs has been carried out recently. Wangkheirakpam et al. studied the impact of interface traps using complementary junction less vertical TFET digital inverter application and comparison was done with the one without interface traps [24]. Gupta et al. investigated the consequences of interface trap charges on the variation of heterogeneous gate dielectric junction less-tunnel FET (JL-TFET) [25]. In this work, a detailed investigation has been carried out on the effect of ITCs on PG JL-TFET and the SO PG-JL-TFET with stack approach, in terms of DC, analog/RF and linearity distortion parameters.

This paper explains the stacked oxide device structure, simulation setup and operation in Section 2. Results and discussions are presented in Section 3, and finally, the conclusion is presented in Section 4.

2 Description of Device and Simulation Setup

Figure 1(a) and (b) depict the cross-sectional view of the PG JLTFET and the SO PG JLTFET implemented using stack approach respectively. The design parameters considered for both the devices are depicted in Table 1. Both the device structures are of n-type JL-TFET, comprising of two gates, control gate and polarity gate which are isolated in nature. The control gates and the polarity gates are used for modulation of effective tunnelling barrier width. The Work function of 4.3 eV, is applied at the control gate thus converting n + layer under the control gate into intrinsic region and a work function of 5.93 eV is applied at the polarity gate, thus, converting n + layer under polarity gate into p+, which acts as the source region. Thus, n + −n + −n + region is converted into n + −i–p + region which works as n + −i–p + JLTFET. The work function of 5.93 eV (Platinum) has been used at the source metal electrode in order to form the source region through concept of charge plasma, by inducing approximately $10^{19}/cm^3$ of hole concentration on the silicon surface at the source side of device [26]. Similarly, the work function of 3.9 eV has been used at drain side, to form the drain region through charge plasma concept, by inducing electron concentration on silicon surface at drain side of device. All the parameters for both PG JLTFET and SO PG JLTFET are same, with one main difference. In the case of the SO PG JLTFET, $(SiO_2 + HfO_2)$ stack is used, while in the case of PG JLTFET, only SiO_2 stack is used. Both the positive and negative ITCs are applied at the silicon oxide interface. The fixed charge density of ITCs is taken to be $N_f = \pm 1.0 \times 10^{12}$ /cm^2) [25, 27, 28]. It should be noted that in the simulation, INTERFACE statement from [29] has been considered to analyze the density of interface fixed charges and their position available at interface of silicon and oxide layer. INTERFACE statement has been implemented in Silvaco TCAD as follows:

Table 1 Device structure and simulation setup

Parameters	PG JL-TFET	SO PG JL-TFET
Drain Length (L_D)	20 nm	20 nm
Source Length (L_S)	20 nm	20 nm
Source Doping (N_S)	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}
Channel Doping (N_{CH})	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}
Drain Doping (N_D)	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}
SiO_2 Thickness (Tox)	2 nm	0.8 nm
Si Thickness (T_{Si})	2 nm SiO_2	0.8 nm SiO_{2+} 1.2 nm HfO_2
CG Work function (φ_{CG})	4.3 eV	4.3 eV
PG Work Function ($\varphi_{P\ G}$)	5.93 eV	5.93 eV
Source Work Function (φ_S)	5.93 eV	5.93 eV
Drain Work Function (φ_D)	3.9 eV	3.9 eV
Drain Voltage (V_D)	1 V	1 V
Trap charge Density N_f)	1×10^{12} cm^{-3}	1×10^{12} cm^{-3}

INTERFACE QS=+1e12 x.min=0.020 x.max=0.040 y.min=-0.0030 y.max=-0.0020.

Here QS represents the interface charge density, and it can be positive or negative, x represents the channel length position in μm and y represents channel width position in μm.

Although the presence of interface traps is there at the interface of HfO_2 and oxide layer in SO PG JLTFET and will be absent in case of PG JLTFET, but in present manuscript only the ITCs along the channel length at the silicon and oxide interface has been considered. The ITCs at the HfO_2 and oxide interface has been neglected because, in case of TFETs mainly the impact of drain junction and the tunneling junction is there on the device behavior [23]. The spacer thickness, which is 5 nm between polarity gate and source and electrodes, finds how the gate field is closer to the tunneling path towards the source side. Thus, while finding the tunneling probability it becomes an important parameter. The impact of ITCs on the dc performance, analog/RF and linear distortion performance of both the PG JLTFET and SO PG JLTFET has been studied in this work.

2-D Silvaco Atlas device simulator has been used to conduct all the simulations. Shockley Read Hall and Auger models have been used in order to account for presence of highly doped impurity atoms in channel and minority recombination region. Nonlocal band-to-band tunneling (BTBT) model [30, 31], has been used, which analyses the rate of generation of carriers at each point. For implementing this model, region of quantum tunneling are defined at interface of source and channel and drain and channel interface, in order to account for ON state tunnelling of carriers, and ambipolar nature of JLTFET respectively. Use of bandgap narrowing model is done to account for high doping concentration in the channel region [20]. The quantum confinement model has also been applied, which is incorporated by using the Schrodinger Poisson model. The nonlocal BTBT model utilizes the isotropic tunneling effective mass of hole as well as the electron [32]. This model provides the solutions of Schrodinger's equation, for the energies of the bound states in conduction bands and valence bands, as well as the solution of Poisson equation for electric potential. The Schrodinger's equation solution also determines the quantum electron density calculations. Quantum electron density calculations have to be solved for wave function as well as magnitude of Eigen state energy at each cross section of the device. Fermi Dirac model has been used to calculate electron and hole concentrations, as well as wave function and Eigen energy [32]. These parameters have been utilized for calculating the potential using Poisson's equation [32]. Schottky tunnelling model has also been used. The nonlocal trap-assisted tunneling (TAT) model has been incorporated in order to account for TAT, which is based on the Wentzel–Kramer–Brillouin (WKB) transmission coefficient with an exact tunneling barrier [33]. This model utilizes the material parameters that is tunneling mass of hole considered as 0.16 and tunneling mass of electron considered as 0.21 [34].

Fabrication of the SO PG JL-TFET can be done using nonplanar technologies. The procedure of fabrication as shown in Fig. 1(c) is explained as follows:

(i) Fabrication of channel can be done by Bosch processes or deep reactive ion etching [32];
(ii) Deposition of gate oxide can be done by using low pressure chemical vapor deposition (LPCVD) [32];
(iii) The patterning of window, which defines region of tunneling can be done using plasma etching [35];
(iv) Successively, deposition of HfO_2 layer can be done by using Atomic Layer Deposition at 200°C, which can be followed by annealing in O_2 ambient [36].
(v) Formation of source/drain contact can be done by growing it epitaxially over the substrate [31];

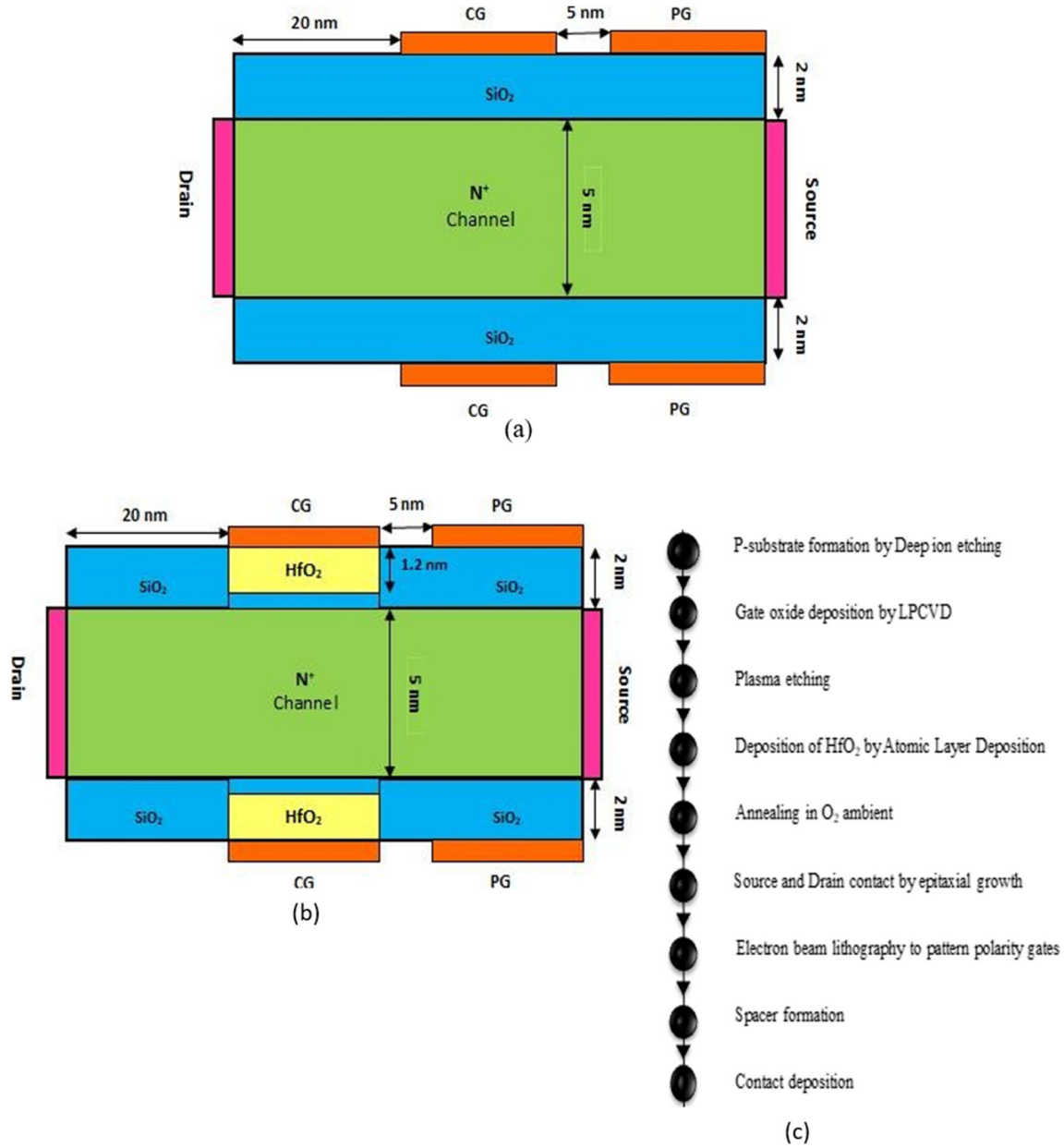


Fig. 1 View of cross-sectional for (a) PG JL-TFET (b) SO PG JL-TFET (c) Fabrication steps for SO PG JL-TFET

(vi) Successively, patterning of the polarity gates (PGs) can be done by using the process of e-beam lithography [32]; and
(vii) Finally, the spacer formation and contact deposition can be done [32].

3 Results and Disscussion

In this section, the comparative analysis of performance for the PG JL-TFET with the SO PG JL-TFET is illustrated.

3.1 Effect of Interface Trap Charges on Dc Performance

In order to study the tunneling process, energy band diagrams of PG JLTFET and SO PG JLTFET in thermal state, OFF state and ON state is depicted in Fig. 2(a-f). In both the SO PG JLTFET and the PG JLTFET, in the case of thermal state, there exists high energy barrier width at drain-channel and source-channel areas. In OFF state, electron tunneling probability from the valence band of source to the conduction band of the channel is negligible because increased energy barrier is there between junction of channel and source for both SO PG

JLTFET and PG JLTFET. Now when both the devices move towards the ON-state, energy barrier width reduces between source and channel, so that quantum tunneling takes place between valence band of source and conduction band of channel. The width of energy barrier for the SO PG JLTFET is less in comparison to the PG JLTFET at the source channel junction, thus exhibiting more band bending and more tunneling of electrons from the valence band of source to the conduction band of the channel. The width of energy barrier is less in the case of SO PG JLTFET because high-k gate dielectric HfO_2, has been considered at source side below the gate electrode in comparison to the PG JLTFET. It is observed from plots that potential barrier reduces below 10 nm at the junctions of the channel and source, required for the tunneling mechanism to take place. Also it is observed that with positive ITCs more band bending takes place in comparison to case where no ITCs are there, thus leading to reduced tunneling barrier width. While in case of negative ITCs less band bending takes place, thus leading to the increased tunneling barrier width. The PG JLTFET shows a slight variation with different ITCs in case of channel bending as compared to the SO PG JLTFET.

Electric field variation in the direction of channel is depicted in Fig. 3(a) and (b) for the PG JLTFET and the SO PG JLTFET with stack approach, respectively. Now in case of SO PG JLTFET, electric field, which is higher in magnitude in comparison to PG JLTFET, is observed near the source, thus showing that the effect of HfO_2 is concentrated at the junction of source and channel. The highest amplitude of electric field is present at the interface of source and channel closer to the drain region, leading to the highest tunneling in this region. The reason for this is that the band to band tunneling rate (GBTBT) varies with the electric field ε at the inteface in accordance with the eq. (1) [34]:

$$G_{BTBT} = A\varepsilon^{\sigma}\exp\left(-\frac{B}{\varepsilon}\right) \tag{1}$$

Where, A is constant related to the effective mass of an electron, σ is the transition constant and B is the tunneling

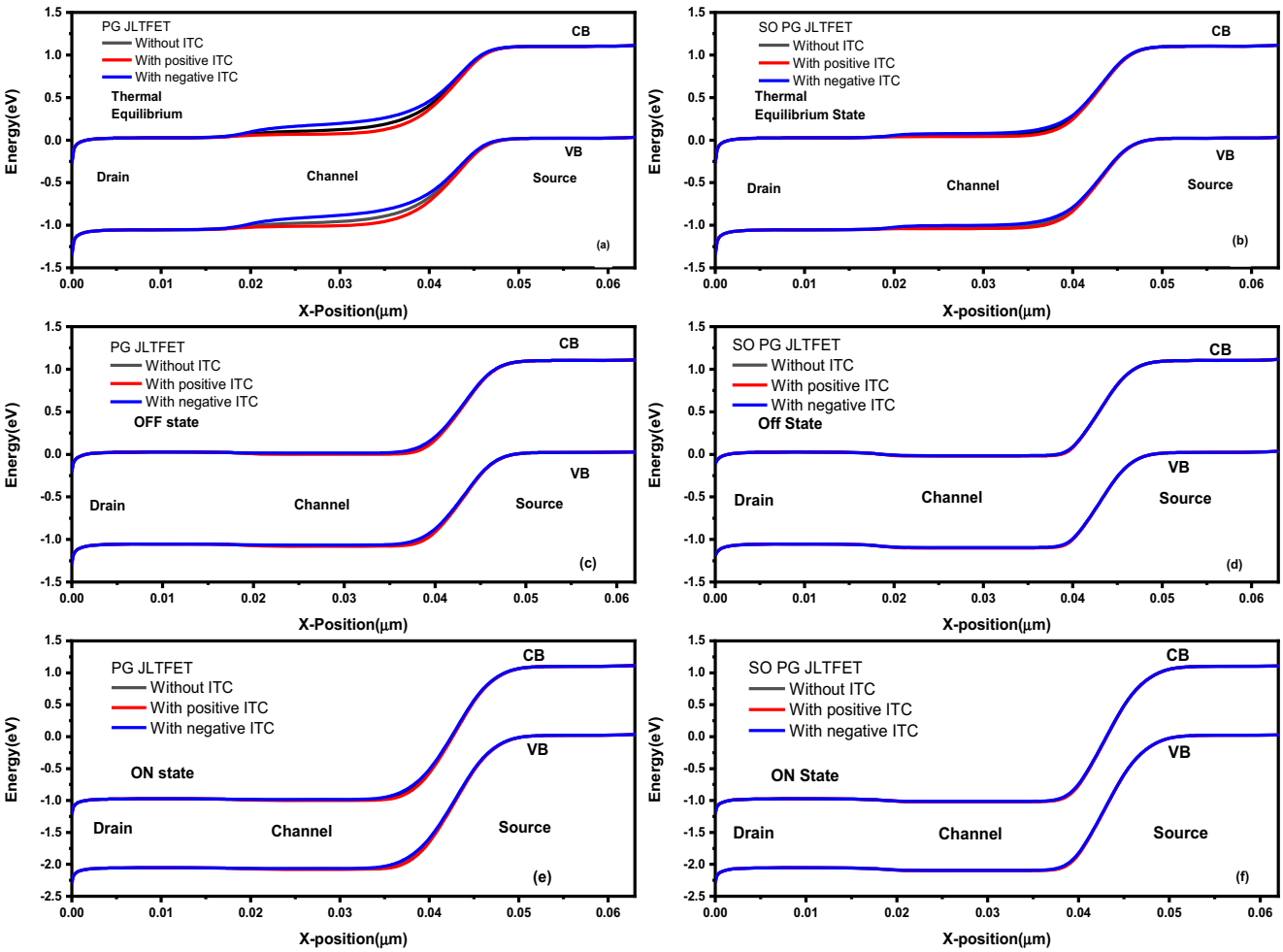
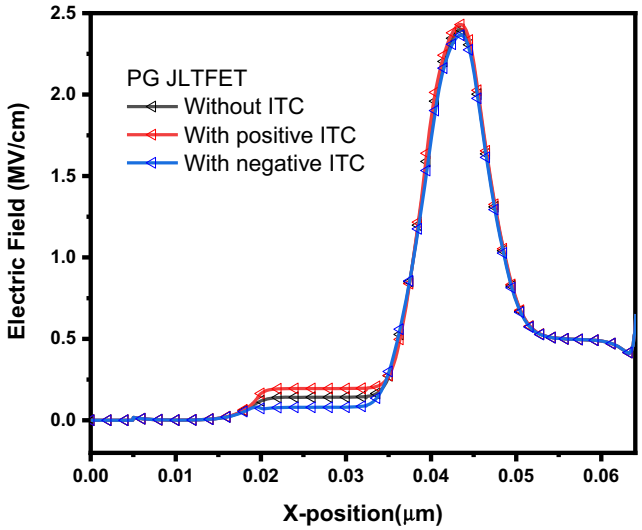
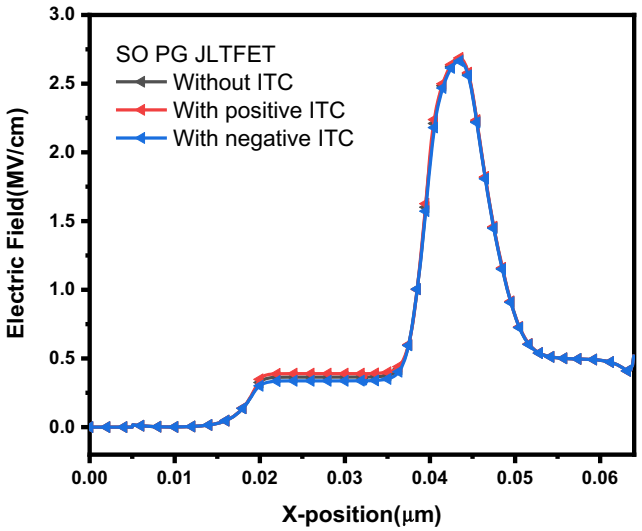


Fig. 2 Energy band diagram of PG JLTFET and SO PG JLTFET for (a-b) thermal equilibrium, (c-d) OFF-state, and (e-f) in ON-state, respectively



(a)



(b)

Fig. 3 Variation in electric field with different ITCs for **(a)** PG JL-TFET **(b)** SO PG JL-TFET

probability constant. The charge carrier transmission probability (T_{WKB}) at the barrier, where tunneling occurs is determined by WKB approximation, given in eq. (2) [34].

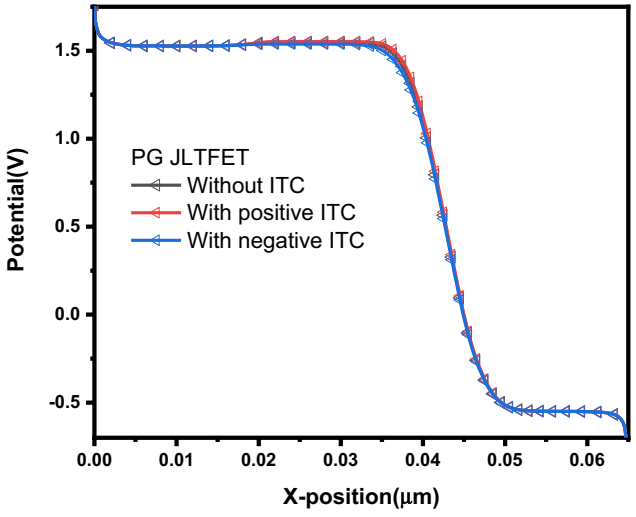
$$T_{WKB} \approx exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g{}^3}}{3qh\left(E_g+\Delta\phi\right)}\right) \tag{2}$$

Where, h is Plank's constant, *q* is the electron charge, *Eg* is the semiconductor bandgap, Δϕ represents the range of energy for which tunneling takes place and λ is the barrier width of tunneling junction. In the SO PG JLTFET, the T_{WKB} is increased at the junction of source and channel as compared to PG JLTFET, because it has higher electric field because of the decrement in λ. It is also observed that positive ITCs in both the devices lead to enhanced electric field near the source channel interface, while, negative ITCs lead to reduced electric field. This is basically due to increased band bending due to positive ITCs and decreased band bending in case of negative ITCs. It is also noticed that the SO PG JL TFET shows almost no change in electric field with various ITCs, when compared with the PG JL TFET.

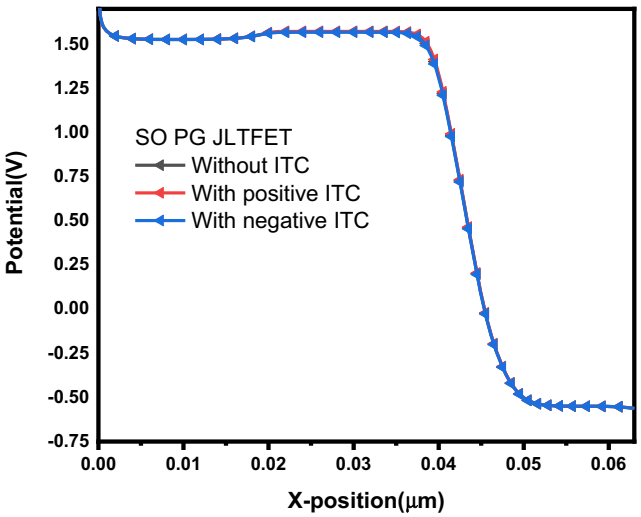
A similar pattern as that of electric field, is also observed for the potential, implying that there is an increase in potential with positive ITCs and decreases with negative ITCs, as shown in Fig. 4(a) and (b). Also the SO PG JLTFET exhibits enhanced potential as compared to the conventional device owing to the enhanced electric field in the SO PG JLTFET. The SO PG JLTFET shows almost no change in the potential with various ITCs when compared with the PG JLTFET.

Figure 5(a) and 5(b) depict the carrier concentration for the PG JLTFET as well as SO PG JL TFET along the X-direction. It is noted that the magnitude of concentration profile is almost same as that of conventional TFET near the top surface of Si-film. As the gate voltage increase, more electrons get accumulated at the surface of silicon layer. The concentration of electron in the channel region changes to approximately around 10^{20} cm^{-3}, which is all most equal to that of n + region, when the controlling gate voltage of 1.2 V is applied, creating an abrupt junction. As a result, electrons tunnel towards the conduction band of the channel from the valence band of source. Presence of positive trap charges leads to higher electrons accumulation on the surface of silicon, resulting in an increased tunneling rate of electrons. Whereas, when negative ITCs are present, there is an increased accumulation of holes, leading to their recombination with the electrons in the channel, which results in a decrement in the tunneling rate of electrons. Lower coupling takes place between channel and gate in case of PG JL-TFET due to presence of SiO_2 layer, whereas, better coupling takes place between channel and gate for the stacked oxide PG JL-TFET, due to high-κ dielectric (HfO_2), present at the source side. Decrement in variation is seen in carrier concentration for the SO PG JLTFET, in comparison to the PG JLTFET, with different ITCs.

Figure 6 depicts the I_{ds} -V_{gs} characteristics for various ITCs for the SO PG JLTFET and PG JLTFET. Enhanced ON current is observed in case of the SO PG JLTFET as compared to PG JLTFET. One of the reasons is, since in SO PG JLTFET, high-k dielectric has been introduced, leads to increased electrical coupling between gate and channel, thus leading to enhanced drain current. As discussed before, positive ITCs enhance band bending, thus, increasing the band to band generation rate, which leads to increase in the ON-state current, I_{ds}. While, the reverse phenomenon takes place due to the impact of negative ITCs, which results in decrease of drain current for both the devices in case of negative ITCs. The positive ITCs and negative ITCs, increase and decrease the drain current by 62.81% and 43.96% respectively, in case of PG JLTFET.

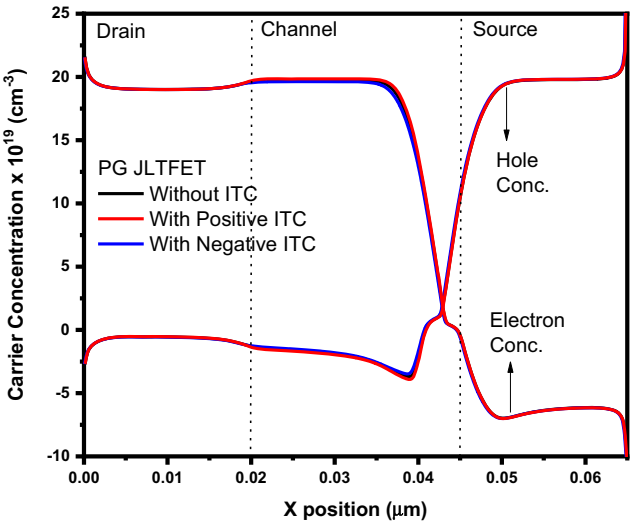


(a)

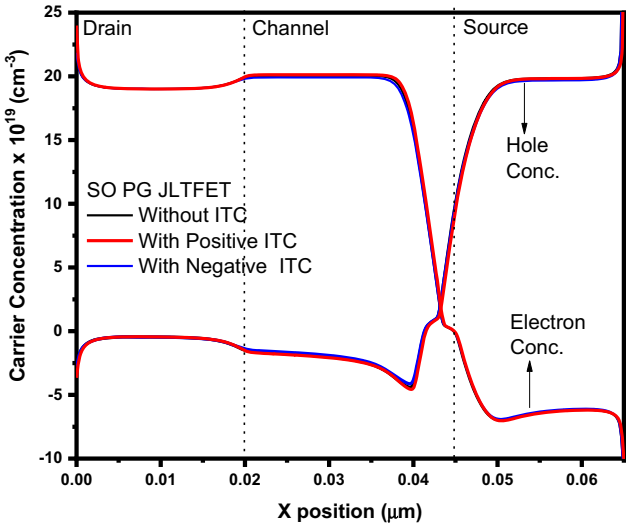


(b)

Fig. 4 Variation in potential with different ITCs for **(a)** PG JL-TFET **(b)** SO PG JL-TFET



(a)



(b)

Fig. 5 Variation in profile of carrier concentration with different ITCs for **(a)** PG JLTFET **(b)** SO PG JLTFET

While in case of SO PG JLTFET, this data is 17.90% and 16.68% respectively. Thus, it is clear that the SO PG JLTFET is more reliable with different ITCs in comparison to PG JLTFET.

Threshold voltage (V_{th}) is very important parameter for semiconductor devices. In case of MOSFETs, threshold voltage (V_{th}) is described as the gate voltage at which strong inversion occurs, but this is not valid for TFET, because for TFET no strong inversion takes place [32]. Hence, for the TFET, V_{th} can be determined by using a transconductance change method [32]. In this method, V_{th} is defined as the gate voltage at which dg_m/dV_{gs} is maximum. Drain-induced barrier lowering (DIBL) is a short-channel effect in semiconductor devices, which causes reduction of threshold voltage of the device at higher drain voltages. In the manuscript DIBL has been estimated as the gate-to-source voltage difference at $I_{ds} = 10^{-13}$ A, between the $V_{ds} = 50$ mV and $V_{ds} = 1$ V transfer curves [37]. Table 2 shows the calculated parameters V_{th}, DIBL for the SO PG JLTFET, with zero, positive and negative trap charges. Positive trap charges lead to decrease in threshold voltage and DIBL while negative trap charges lead to increase in threshold voltage and DIBL, as compared to case of zero trap charges.

Subthreshold swing is the inverse of the subthreshold slope. On the I_{ds} vs V_{gs} plot with logarithmic (base 10) axis for I_{ds} the subthreshold slope is found as the straight-line approximation of the subthreshold current, and is defined in units of decades/mV. The subthreshold swing has the units

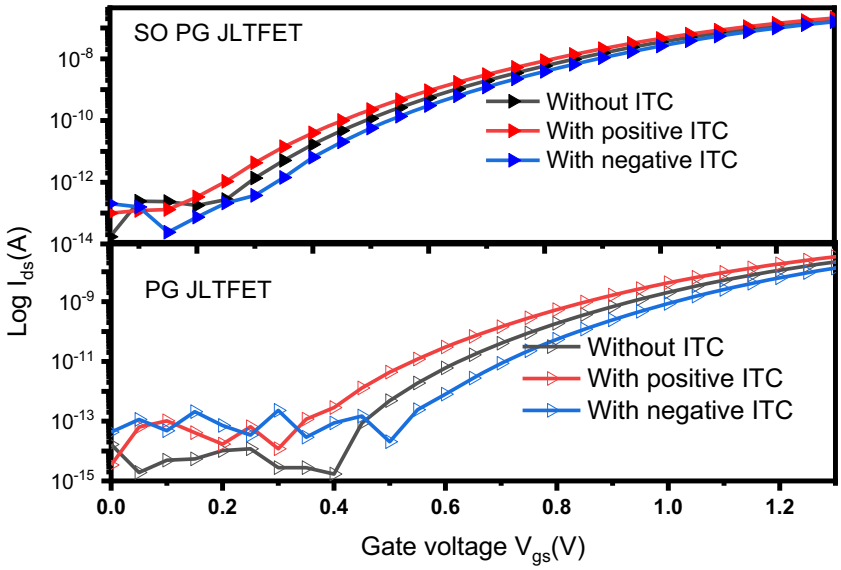


Fig. 6 Variation in I_{ds} vs. V_{gs} for various ITCs for SO PG JLTFET and PG JLTFET

of mV/decade. There are two types of subthreshold swing: - point subthreshold swing and average subthreshold swing [37]. Point subthreshold slope is given by Eq. (3) and average subthreshold slope is given by eq. (4).

$$(SS_{POINT})_{V_{GS}} = \left(\frac{dV_{GS}}{d\log(I_{DS})}\right)_{V_{GS}} \tag{3}$$

$$SS_{AVG} = \frac{(V_T - V_{OFF})}{\log(I_{VT}) - \log(I_{OFF})} \tag{4}$$

Where V_T is threshold voltage, I_{VT} is drain current at threshold voltage, V_{OFF} and I_{OFF} are off state voltage and current respectively and are shown in Fig. 7. Figure 7 also depicts the method of calculation of average subthreshold swing. Table 2 shows the point and average subth reshold swing for the SO PG JLTFET, with zero, positive and negative trap charges.

The impact of various ITCs on the output characteristics is shown in Fig. 8. It is observed that positive ITCs lead to increase in the tunneling current, while negative ITCs lead to decrease in the tunneling current. Also, the SO PG JLTFET displays higher value of tunneling current, as compared to the conventional one. Again, the SO PG JLTFET is less vulnerable to the ITCs, as compared to the conventional device.

3.2 Effect of Interface Trap Charges on Analog / RF Performance

The transconductance is a significant design parameter for different analogue/RF applications which relates the voltage across the device input and the current output and is given as

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \tag{5}$$

It plays very significant role, while designing the analogue circuits. Figure 9 shows the variation in transconductance with gate voltage, for the stacked oxide and the PG JLTFET, with different ITCs. It can be observed that in the case of the SO PG JLTFET, transconductance is higher, as compared to the conventional device, which can be attributed to the enhanced drain current in the former. The enhanced drain current is owed to better coupling between gate and channel, because of high-k dielectric on the source side in the SO PG JLTFET. It can also be observed in Fig. 8, that the impact of interface trap charges is less significant in the case of SO PG JLTFET as compared to the conventional device. In both the cases, positive ITCs have an increasing effect on transconductance because of increment in tunneling rate whereas negative ITCs haves a decreasing effect due to decrement in the tunneling rate. The positive ITCs and negative ITCs, lead to an increase

Table 2 V_{th}, DIBL, point and average subthreshold swing for the SO PG JLTFET

SO PG JLTFET	Zero ITCs	Positive ITCs	Negative ITCs
V_{th} (V)	1.15	1.1	1.2
DIBL (mV/V)	379.98	274.365	459.659
Point Subthreshold Swing (mV/decade)	37	41.9	32.9
Average Subthreshold Swing (mV/decade)	142.38	158.33	138.12

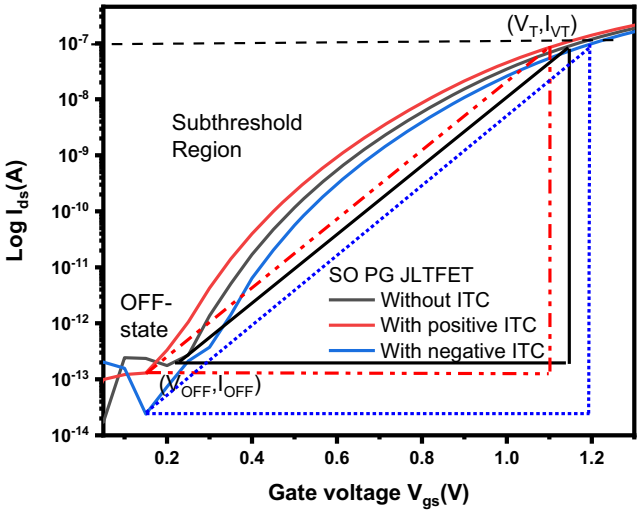


Fig. 7 Calculation of average subthreshold swing for SO PG JLTFET

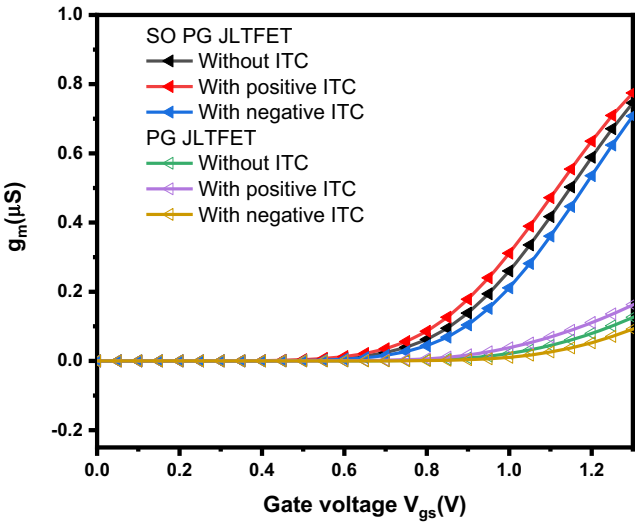


Fig. 9 Transconductance vs. gate voltage for PG JLTFET and SO PG JLTFET

and decrease in transconductance by 39.44% and 33.96% respectively, in the case of PG JLTFET. While in the the case of SO PG JLTFET, this data is 7.93% and 9% respectively, thus, indicating higher reliability in this device as compared to the conventional one.

Figure 10 shows the variation of output conductance, g_{ds}, with drain voltage, for the PG JLTFET and SO PG JLTFET with different ITCs. It is observed from the graphs that, with increase in drain voltage, output conductance rises to the peak value and then reduces, which is attributed to mobility degradation [32]. For the SO PG JLTFET, high output conductance as compared to the PG JLTFET is reported, which is because of the higher electric field in the SO PG JLTFET. Also, with positive ITCs, g_{ds} increases, for both the devices, as compared to the case when there is no ITC. This is because of an enhanced electric field at the source channel junction. The reverse phenomenon takes place in case of negative ITCs, leading to decreased g_{ds}. The positive ITCs and negative ITCs, increase and decrease output conductance by 83.15% and 53.76%, respectively, in the case of PG JLTFET. While, in the case of SO PG JLTFET, this data is 23.13% and 20.93%, respectively.

Transconductance to current ratio (g_m/I_{ds}) or the device efficiency is another important design parameter, which determines how efficiently power, can be converted into speed. The effect of various ITCs on device efficiency, for both PG JLTFET and SO PG JLTFET is shown in Fig. 11. As observed before, positive and negative ITCs lead to an increase and decrease in drain current and transconductance, respectively, for both the devices [see Figs. 6 and 9]. This leads to decrease in device efficiency with positive ITCs, and vice-versa in case of negative ITCs. The reduction in device efficiency with positive ITCs takes place because more deviations

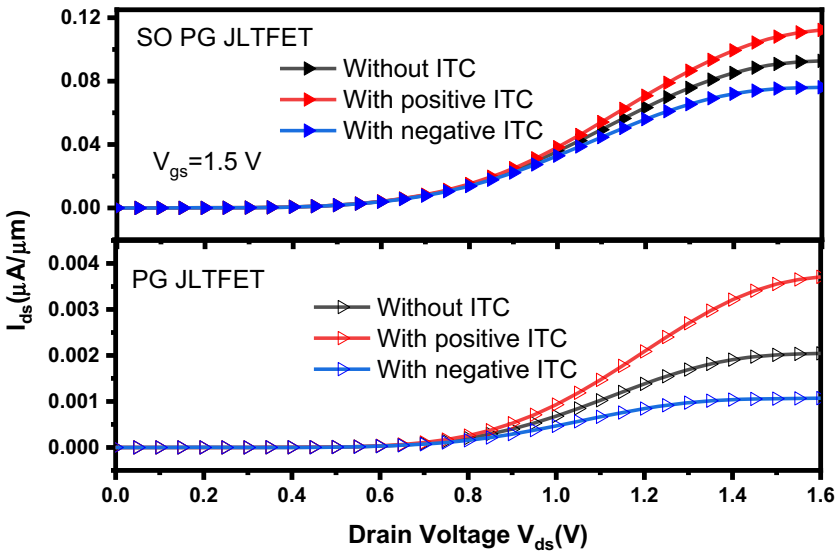


Fig. 8 Variation in I_{ds} vs. V_{ds} for various ITCs for SO PG JLTFET and PG JLTFET

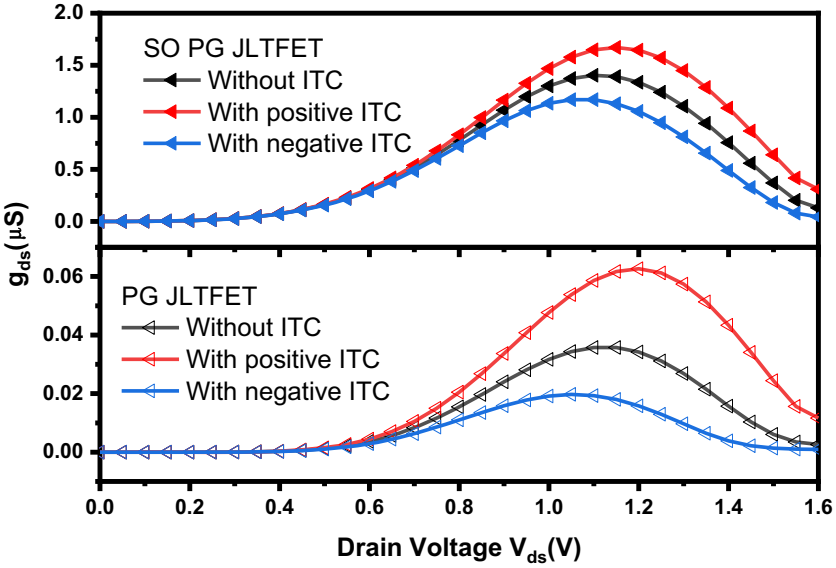


Fig. 10 Output conductance vs. drain voltage for PG JLTFET and SO PG JLTFET

occur in drain current, when compared to the transconductance, while the reverse phenomenon takes place in case of negative ITCs. It is also observed that for the SO PG JLTFET device efficiency is less as compared to the conventional device. This is again due to an enhanced drain current and transconductance in the SO PG JLTFET, and more deviations in drain current with respect to the transconductance. The positive ITCs and negative ITCs, decrease and increase device efficiency by 14.35% and 17.83% respectively, in the case of the PG JLTFET. While in the case of the SO PG JLTFET, this data is 8.45% and 9.22%, respectively, thus, indicating higher reliability in this device as compared to the conventional device.

C_{gs} and C_{gd} capacitances are the important parameters for measuring the RF performance of any device [29]. Figures 12 and 13 depict the graph of C_{gs} and C_{gd} for the PG JLTFET and the SO PG JLTFET with various ITCs with respect to the gate voltage $V_{gs,}$ respectively. From the graphs, it can be interpreted that, both the capacitances, exhibit lesser variation in case of SO PG JLTFET in comparison to the PG JLTFET. It is evident from the graphs, that with an increase in voltage, V_{gs}, C_{gs} decreases due to the potential barrier [36, 37]. There is not much difference in C_{gs} for the SO PG JLTFET and the PG JLTFET. The capacitance C_{gd} plays significant role with the voltage V_{gs}, because the inversion region is formed in between the source and drain, in both the devices. From the graphs, it can be observed that enhancement in C_{gd}, occurs with increase in V_{gs}, which is because, increase in gate bias leads to the decrement in barrier across the drain and channel, hence leading to improved coupling between gate and drain.

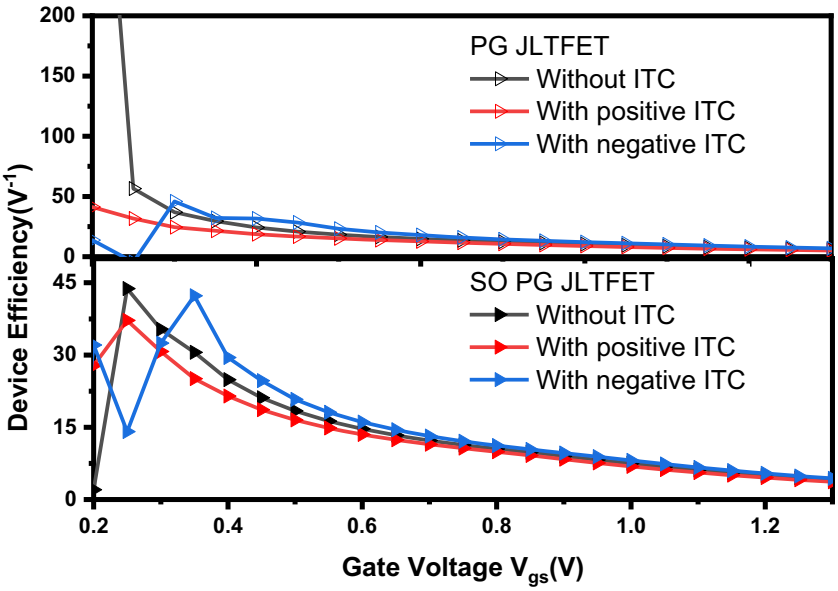


Fig. 11 Device efficiency vs. gate voltage for PG JLTFET and SO PG JLTFET

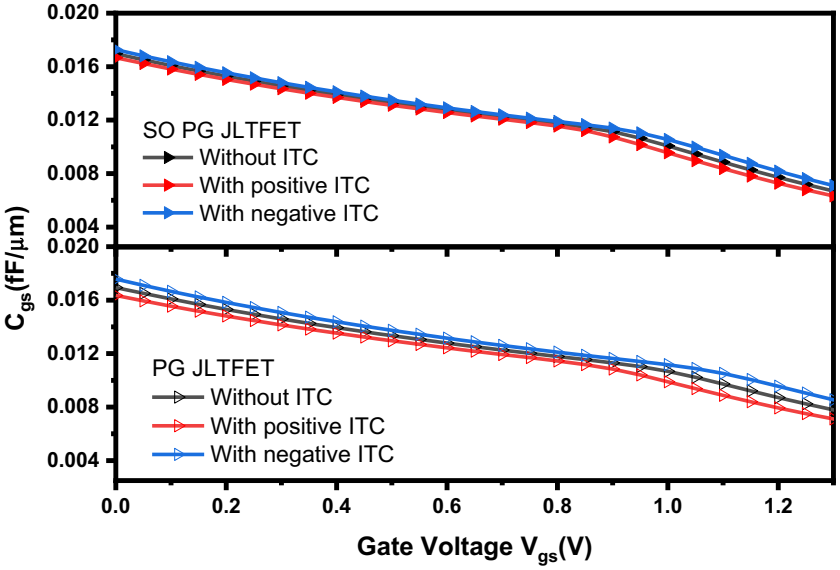


Fig. 12 C_{gs} vs. gate voltage for PG JLTFET and SO PG JLTFET

The same phenomenon is responsible for the increase in C_{gd} with positive ITCs, because as already discussed; positive ITCs lead to reduction in the barrier between drain and channel as compared to the case when no ITCs are there. The reverse phenomenon takes place in case of negative ITCs, leading to reduction in C_{gd}. Also enhancement in C_{gd} takes place in the SO PG JLTFET, as compared to the conventional device, again because of the decreased potential barrier between the drain and channel in SO PG JLTFET. The positive ITCs and negative ITCs, decrease and increase C_{gs} by 8.89% and 9.66% respectively, in case of PG JLTFET. While, for the SO PG JLTFET, this data is 5.65% and 6%, respectively.

The cut-off frequency (f_T) is an important design parameter for high-speed radio-frequency devices. It is the frequency at which short circuit output current becomes equal to the input current. The effect on cut-off frequency f_T due to various ITCs, for both the devices is depicted in Fig. 14. It is dependent on parasitic capacitances and transconductance of the device. It is defined as:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{6}$$

where; C_{gs} and C_{gd} are gate-to-source and gate-to-drain capacitance respectively. It can be clearly interpreted from the graphs that f_T for SO PG JLTFET is several orders greater as compared to the PG JLTFET. Since the positive ITCs, lead to increase in transconductance as seen before, thus they lead to increase in f_T as well in comparison to the case when there

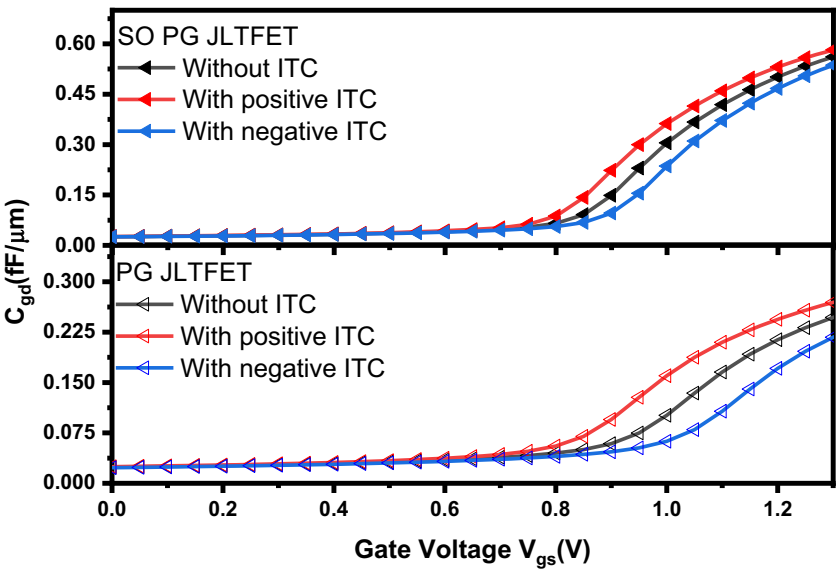


Fig. 13 C_{gd} vs. gate voltage for PG JLTFET and SO PG JLTFET

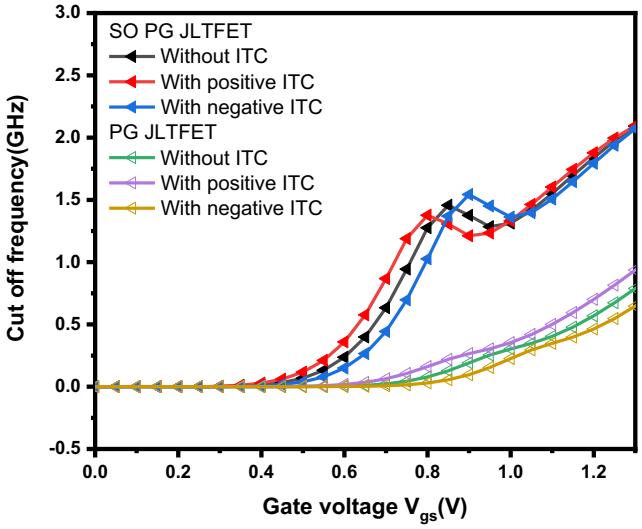


Fig. 14 f_T vs. gate voltage for PG JLTFET and SO PG JLTFET

are zero ITCs. While the reverse phenomenon takes place for the case of negative ITCs. The positive ITCs and negative ITCs, increase and decrease f_T by 23.08% and 18.63% respectively, in case of PG JLTFET. While in case of SO PG JLTFET, this data is 2.08% and 2.47%, respectively. Thereby, proving that, the stacked design is much more resistant towards the effect of interface trap charges.

Figure 15 shows the impact of different ITCs on gain bandwidth product (GBW) which is defined as the product of the device's bandwidth and the gain at which the bandwidth is measured and given by:

$$GBW = \frac{g_m}{2\pi C_{gd}} \tag{7}$$

Thus, with the increment in g_m and decrement in C_{gd}, GBW becomes directly proportional to g_m/C_{gd}.

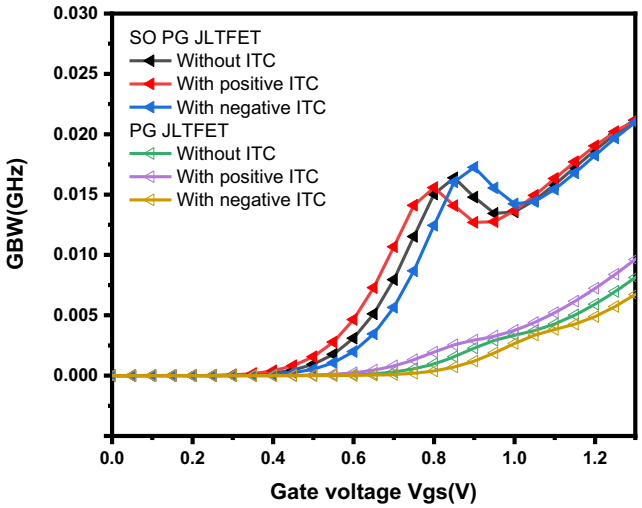


Fig. 15 GBW vs. gate voltage for PG JLTFET and SO PG JLTFET

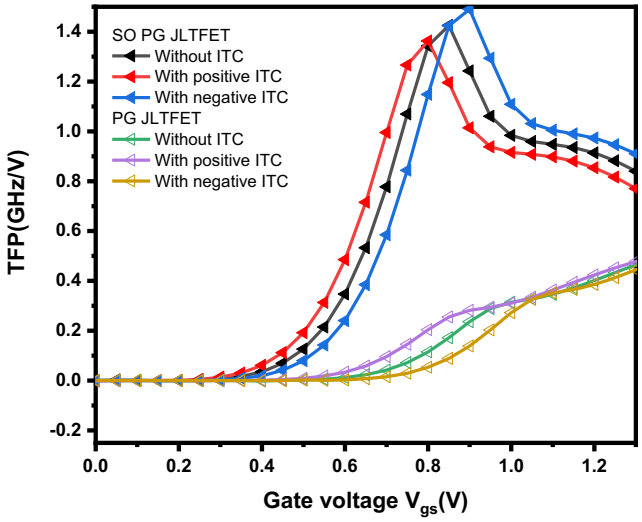


Fig. 16 TFP vs. gate voltage for PG JLTFET and SO PG JLTFET

The GBW is an important parameter for RF applications and it can be noticed that the GBW for PG JLTFET is lesser than the SO PG JLTFET, which is because of lesser value of transconductance in PG JLTFET, as compared to the stacked one. Also, the positive ITCs and negative ITCs, increase and decrease GBW by 22.10% and 17.45% respectively, in case of PG JLTFET. While in case of SO PG JLTFET, this data is 1.91% and 2.26% respectively, thus proving the reliability of stacked device.

Transconductance frequency product (TFP) is significant figure of merit for high frequency analysis, where TFP is defined as the product of ratio of transconductance to current and cut off frequency.

$$TFP = \frac{g_m}{I_{DS}} f_T \tag{8}$$

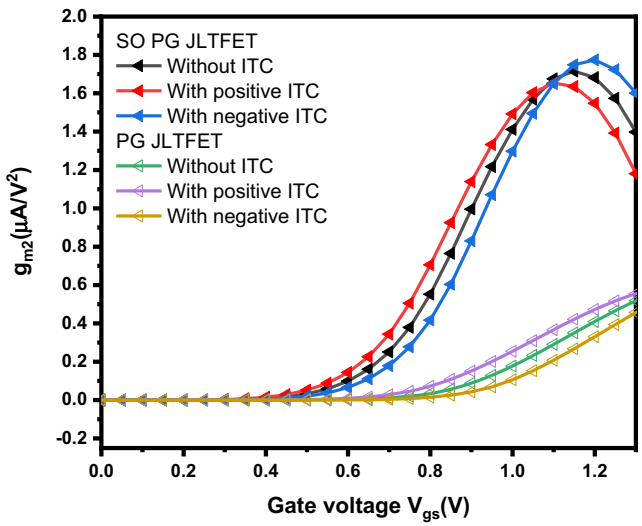


Fig. 17 g_{m2} vs. gate voltage for PG JLTFET and SO PG JLTFET

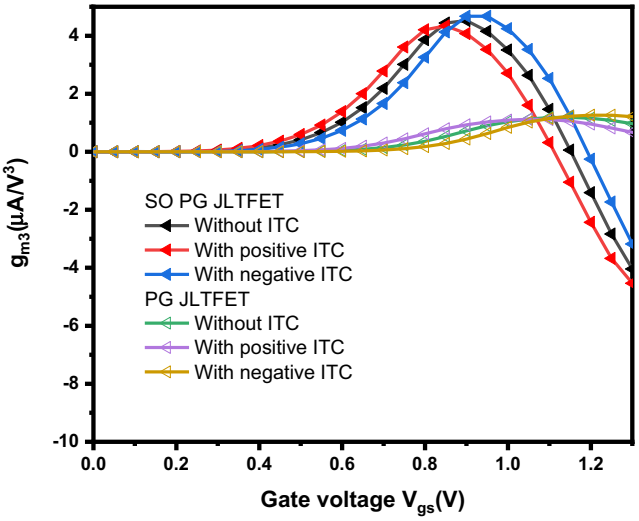


Fig. 18 g_{m3} vs. gate voltage for PG JLTFET and SO PG JLTFET

TFP depicts the tradeoff between power and bandwidth, which is required for designing of moderate to high-speed devices [38]. Figure 16 shows that TFP, first increases in linear fashion before onset of inversion region and then achieves the maximum value, and finally it reduces for the higher values of gate bias, which is because of the mobility reduction. It can be interpreted from the figures that TFP of SO PG JLTFET is about 10 decades greater, than that of PG JLTFET. Also, with introduction of positive ITCs, leads to lower value of maximum TFP as compared to negative ITCs, which lead to higher value of maximum TFP.

3.3 Effect of Interface Trap Charges on Linearity and Distortion Performance

In order for the RF devices to be compatible with present day communication systems, they must exhibit minimum signal to noise ratio, in addition to the high speed. This is also required, so that they can be used for analog/RF applications. The device must also exhibit linear characteristics, so that the desired output signal cannot be distorted by the non-linear distortion [39]. In order to exhibit the linearity characteristics, transconductance must not vary due to the change in input voltage V_{gs}. But transconductance for both MOSFET and TFET varies with the input voltage V_{gs}, thus exhibiting nonlinear characteristics for both the devices. Thus in this paper, we have analyzed the impact of both positive and negative ITCs on signal distortion and linearity for both the SO and PG JLTFET using the parameters, second order voltage intercept point (VIP_2), third order voltage intercept point (VIP_3), third order intermodulation distortion (IMD_3), third order input intercept point (IIP_3), third order transconductance coefficient (g_{m3}) and 1 dB compression point. The given parameters are defined as:

$$VIP2 = 4X\left(\frac{g_{m1}}{g_{m2}}\right), g_{mn} = \frac{1}{n!}\frac{\delta^n I_{ds}}{\delta V_{gs}^n} \tag{9}$$

$$VIP3 = \sqrt{24X\left(\frac{g_{m1}}{g_{m3}}\right)} \tag{10}$$

$$IIP3 = \frac{2}{3}X\left(\frac{g_{m1}}{g_{m3}XR_s}\right) \tag{11}$$

$$IMD3 = \left[\frac{9}{2}VIP3^2Xg_{m3}\right]^2 XR_s \tag{12}$$

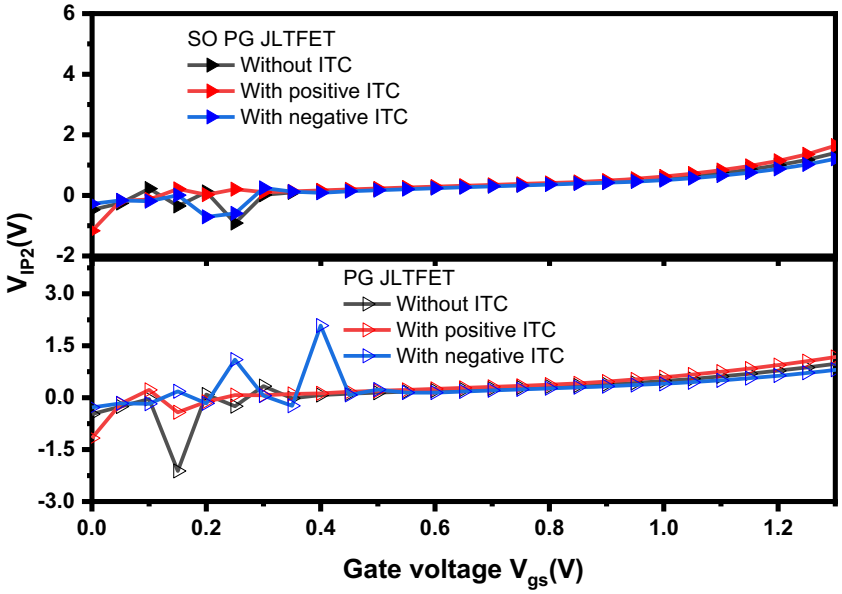


Fig. 19 V_{IP2} vs. gate voltage for PG JLTFET and SO PG JLTFET

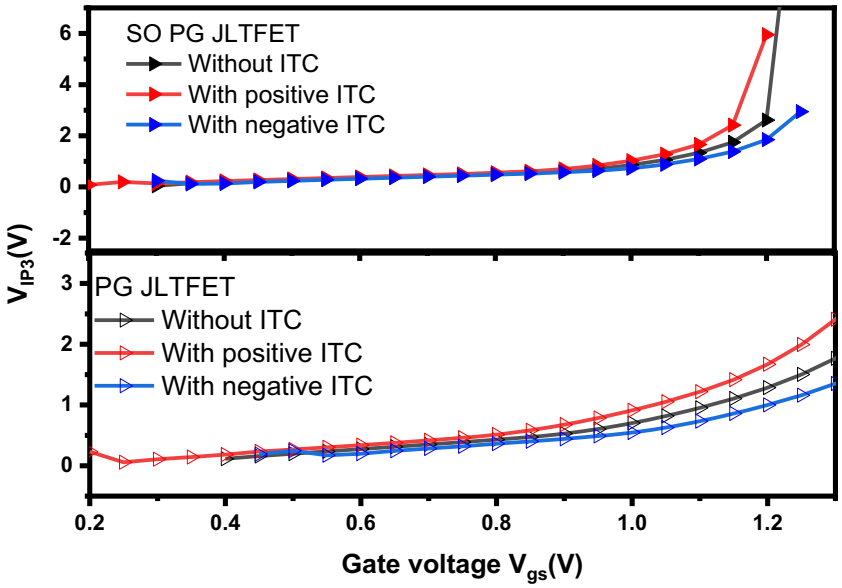


Fig. 20 V_{IP3} vs. gate voltage for PG JLTFET and SO PG JLTFET

Where, $R_s = 50\ \Omega$ for RF applications. V_{IP2} exhibits the extrapolated input voltage in case of which 1st and 2nd order harmonic voltages become equal to each other. Similarly, V_{IP3} exhibits the extrapolated input voltage in case of which 1st and 3rd order harmonic voltages becomes equal to each other, while the IIP_3 exhibits the extrapolated input power at which 1st and 3rd order harmonic powers become equal to each other. In order for the device to exhibit linear and less distortion characteristics, the above parameters must be as high as possible [40].

Figure 17 shows how the trap charges effect g_{m2} with the change in gate bias for both PG JLTFET and SO PG JLTFET. It is observed that decrease in peak amplitude of g_{m2} coefficient takes place, when the positive trap charges occur, while it increases when the negative trap charges are there. Also for the SO PG JLTFET, g_{m2} is enhanced as compared to the conventional device. Figure 18 depicts the variation in g_{m3} with V_{gs} for different trap charges. In order, for the device to exhibit better linear characteristics, g_{m3} should be lower in magnitude, since it is responsible for the fundamental amplitude distortion via signals for the intermodulation distortions. From the graphs, it can be implied that the peak value of g_{m3} in case of positive ITCs is at the lower level as well as the peak is shifted toward lower gate bias. The increase or decrease depicted in Fig. 18 is because of the lesser or bigger variation in drain current arising due to negative and positive ITCs respectively.

Figures 19 and 20 depict how the ITCs show their impact on V_{IP2} and V_{IP3} with variation in gate bias voltage at a constant V_{ds} of 1 V for PG JLTFET and the SO PG JLTFET

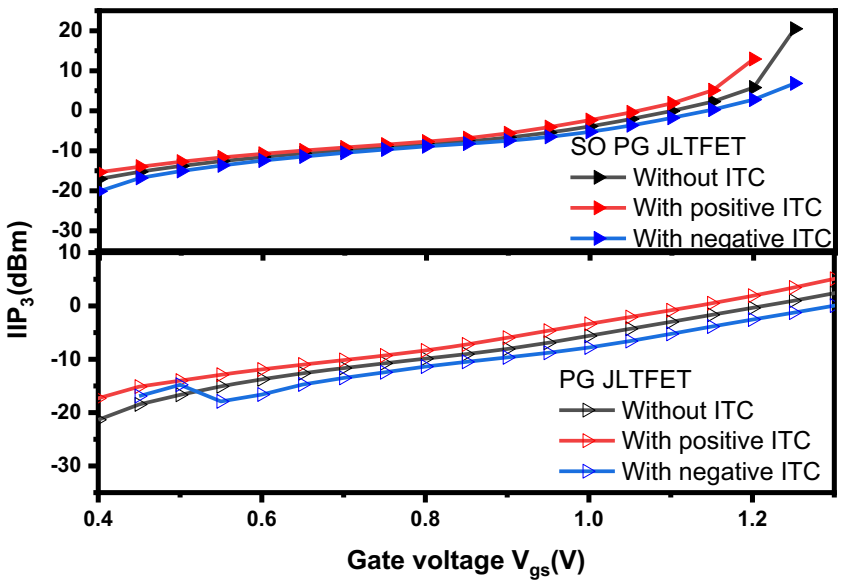


Fig. 21 IIP_3 vs. gate voltage for PG JLTFET and SO PG JLTFET

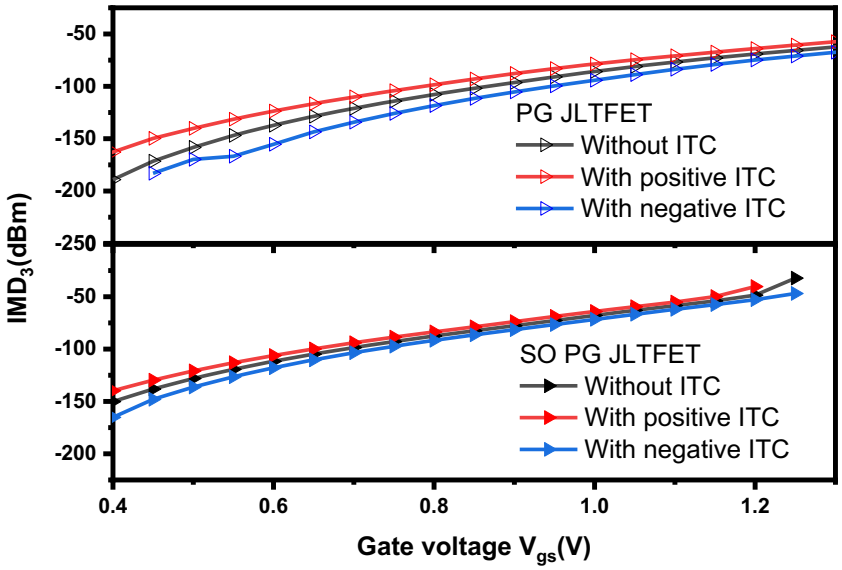


Fig. 22 IMD_3 vs. gate voltage for PG JLTFET and SO PG JLTFET

respectively. In order for the device to exhibit high linear and less distortion characteristics V_{IP2} and V_{IP3} must be greater in amplitude as possible. It can be interpreted from the graphs, that the value of V_{IP2} and V_{IP3} is enhanced for SO PG JLTFET in comparison to the PG JLTFET. Thus, this proves that with introduction of high dielectric engineering, the device exhibits enhanced linearity and reduced distortion characteristics. Also it can be deduced from the graphs that, in case of SO PG JLTFET, peak amplitude of V_{IP2} and V_{IP3} shifts towards the lower gate bias voltage, as compared to the conventional device, thus proving that higher linear characteristics can be obtained at lower values of gate bias voltage. Further, it can be seen that, for positive ITCs the peak amplitude of V_{IP2} and V_{IP3} is enhanced and vice-versa occurs in case of negative ITCs. The positive ITCs and negative ITCs, increase and decrease V_{IP2}, V_{IP3} by 20.79%, 29.67% and 18.16%, 22.08% respectively, in case of PG JLTFET. While in case of SO PG JLTFET, this data is 15.74%, 19.57% and 12.87%, 14.65 respectively, thus proving enhanced reliability of stacked device.

Figures 21 and 22 exhibits the variation of IIP_3 and IMD_3 for different ITCs with gate bias voltage V_{gs} respectively. For the device to show enhanced linear and reduced distortion characteristics, IIP_3 must be as higher in amplitude as possible and IMD_3 must be as lower in amplitude as possible. It can be seen from the graphs that SO PG JLTFET has enhanced value of IIP_3 in comparison to the conventional device, thus implying that the high dielectric leads to an enhanced linearity and reduced distortions for analog and RF applications. Also it can be

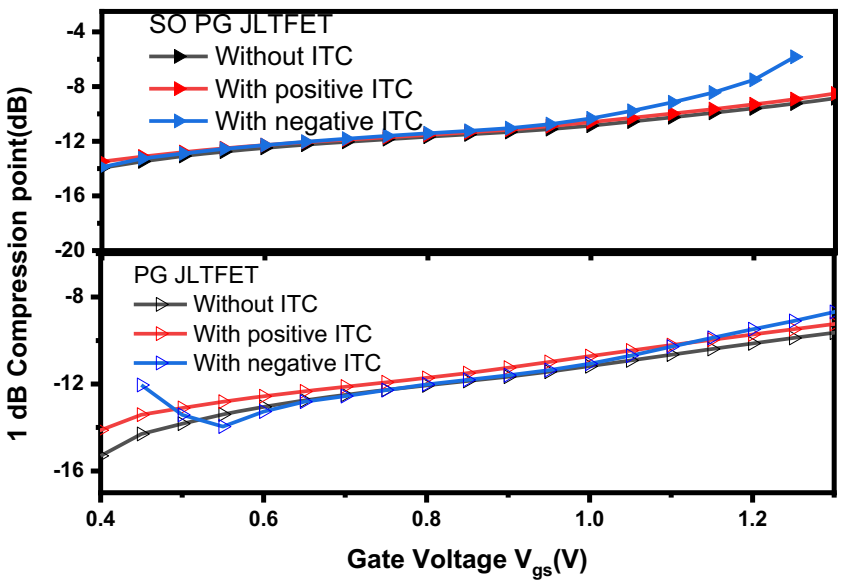


Fig. 23 1 dB compression point vs. gate voltage for PG JLTFET and SO PG JLTFET

Table 3 Comparison of characteristics of PG JLTFET with the SO PG JLTFET, with variation in negative and positive ITC

Particulars at V_{gs}=1.2 V	PG JLTFET	SO PG JLTFET
Interface Trap Charges	Positive(Negative)	Positive(Negative)
Drain Current	62.81% ↑ (43.96% ↓)	17.90% ↑ (16.68% ↓)
Transconductance	39.44% ↑ (33.96% ↓)	7.93% ↑ (9% ↓)
Outout conductance	83.15% ↑ (53.76%↓)	23.13%↑ (20.93% ↓)
Gate to source capacitance	8.89% ↓ (9.66% ↑)	5.65% ↓ (6% ↑)
Gate to drain capacitance	14.19% ↑ (20% ↓)	5.91% ↑ (6.89% ↓)
Cut off frequency	23.08% ↑ (18.63% ↓)	2.08% ↑ (2.47% ↓)
GBW	22.10% ↑ (17.45% ↓)	1.91% ↑ (2.26% ↓)
Device Efficiency	14.35% ↓ (17.83% ↑)	8.45% ↓ (9.22% ↑)
VIP2	20.79% ↑ (18.16% ↓)	15.74% ↑ (12.87% ↓)
VIP3	29.67% ↑ (22.08% ↓)	19.57% ↑ (14.65% ↓)
IIP3	40.17% ↑ (38.57% ↓)	39.87% ↑ (35.34% ↓)
IMD3	8.03% ↑(9.55% ↓)	5.54% ↑ (5.89% ↓)

deduced from graphs that enhanced immunity is there in SO PG JLTFET, with different ITCs as compared to the PG JLTFET. The positive ITCs and negative ITCs increase and decrease IIP_3, IMD_3 by 40.17%, 8.03% and 38.57%, 9.55% respectively, in case of PG JLTFET. While in case of SO PG JLTFET, this data is 39.87%, 5.54% and 35.34%, 5.89% respectively, thus proving enhanced reliability of device with stacked oxide.

1-dB compression point is the point at which the input power drops the gain by 1-dB, depicting the onset of distortion. Figure 23 exhibits the effect of positive and negative ITCs on 1-dB compression point for PG JLTFET and SO PG JLTFET. The 1-dB compression point is increased, in case of SO PG JLTFET, because of the lower signal distortion and enhanced value of transconductance in comparison to the conventional device. Also positive ITCs lead to increment in 1-dB compression point, and the reverse phenomenon takes place for negative ITCs.

Table 3 shows comparison of characteristics of PG JLTFET with the SO PG JLTFET, with variation in negative and positive ITCs. It can be implied from the table that smaller variations in device characteristics occur for the SO PG JLTFET in comparison to the PG JLTFET. Therefore, it can be deduced that SO PG JLTFET is more immune with various ITCs which are there at the silicon and oxide interface as compared to the conventional device.

4 Conclusion

In this work, we have examined the reliability of device by introducing the effect of both donor and acceptor ITCs at the interface of silicon and oxide layer. An in-depth analysis comparing the performance between the PG JL-TFET and the SO PG JL-TFET, which has the advantage of improved tunnelling current, in terms of DC, analog/RF parameters and linear distortion parameters has been done. It has been observed that the SO PG JL-TFET undergoes considerably small variation in its various parameters as compared to PG JL-TFET, with different ITCs, which is due to its high-κ gate dielectric material stacked layer structure, proving that the structure with stacked oxide is much more resistant towards effects of interface trap charges, thus making the device more reliable. Also it has been found that dielectric engineering in SO PG JLTFET, has led to improvement in all kind of performance parameters.

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Availability of Data and Material (Data Transparency) All the data taken from another resource has been given the corresponding reference. The data, for which reference is not provided, is the original data.

Code Availability (Software Application or Custom Code) The code has been implemented on 2-D silvaco ATLAS device simulator.

Author Contributions Kaushal Nigam, Sajai Vir Singh and Priyanka Kwatra in this work contributed equally to the design and implementation of the research, to the analysis of the results and to the writing of the manuscript.

Declarations

Conflict of Interest Kaushal Nigam, Sajai Vir Singh and Priyanka Kwatra state that there are no conflicts of interest. This article does not contain any studies with human or animal subjects.

Consent to Participate This is not applicable for our article, since this article does not contain any studies with human or animal subjects.

Consent for Publication This is not applicable for our article, since this article does not contain any studies with human or animal subjects.

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