mance of the interconnection. The via contact resistance of the Al/TiN/Ti/Al structure increased at annealing temperatures >450°C, since AlN is formed at both the Al/TiN and TiN/Ti/Al interfaces. For reflow sputtering processes for which a temperature higher than 450°C is required, a TiN barrier often becomes an obstacle to reducing the via contact resistance.

The electromigration performance of various via structures has been investigated. The Al/Al via has a different failure mode from that of Al/Ti/Al and Al/TiN/Ti/Al via structures, and was subject to catastrophic opening failure during electromigration stress. The Al/Ti/Al and Al/TiN/Ti/Al vias brought about an increase in chain resistance before opening failure, because the migration of Al atoms deposited at the sidewall of the via hole becomes the dominant mechanism. Al atoms can migrate more easily on a TiN surface than on a Ti surface. As a result, an Al/Ti/Al via structure is the most promising structure for improving electromigration performance.

The use of TiN as a barrier layer for the second interconnection brings about various problems, such as AlN formation and poor electromigration immunity. Therefore, a Ti buffer layer interposed at the Al/TiN and/or TiN/Al interfaces can reduce contact resistance effectively and improve electromigration immunity at process temperatures up to 450°C.

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Thin Film Transistors with Graded SiN_x Gate Dielectrics

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ABSTRACT

This paper presents results on thin film transistors with graded SiN_x gate dielectrics. All SiN_x and a-Si:H films were prepared using 250°C plasma-enhanced chemical vapor deposition processes. Device characteristics such as mobility, threshold voltage, subthreshold slope, and on/off current are discussed. The graded gate dielectric thin film transistor (TFT) may have better or worse device performance compared with the single gate dielectric TFT, depending on the interface dielectric deposition condition. The interface SiN_x deposition process influences the intensity density of states between the a-Si:H layer and the gate SiN_x layer as well as the states between the first and the second (interface) SiN_x layers. The stress mismatch between the first and the second SiN_x layers also has a profound influence on TFT characteristics.

Amorphous silicon (a-Si:H) thin film transistors (TFTs) are the most popular active matrix addressing devices for the high quality large area liquid crystal displays (LCDs). Plasma enhanced chemical vapor deposition (PECVD) is commonly used in depositing a-Si:H and dielectric layers for the TFT because it is a low-temperature process and it can be deposited over large area uniformly. In addition, the a-Si:H and gate dielectric interface can be kept clean by a sequential deposition step without breaking vacuum.

PECVD silicon nitride (SiN_x) is usually used as the gate dielectric layer in the a-Si:H TFT because it gives a high-field effect mobility μ_{eff} and a low-threshold voltage V_{th}. However, to minimize the possibility of the source/drain and gate shortage in the normal or inverted staggered TFT structure, a double-layer gate dielectric is often used. Dielectrics such as SiO_2, Ta_2O_5, and Al_2O_3 are used in combination with SiN_x.[1-3] However, SiN_x is always used as the interface layer in direct contact with a-Si:H, because it gives good interfacial qualities. Compared with a TFT with a single SiN_x gate dielectric layer, the TFT with the SiO_2 in the gate dielectric structure has inferior switching characteristics.[4]

PECVD is a thermodynamically nonequilibrium process. PECVD SiN_x films may have a wide range of compositions and properties even if they are prepared from the same feeding stream at the same temperature.[5,6] Characteristics of a-Si:H TFTs are tremendously affected by the deposition condition of the gate SiN_x film. The film deposition sequence affects the TFT characteristics. It has been shown that the inverted TFT, of which the a-Si:H layer is deposited after the gate SiN_x was deposited, has a higher μ_{eff} and a lower V_{th} than the normal staggered TFT.[7] There is an optimum gate SiN_x composition, *i.e.*, $x = 1$, that gives a minimum V_{th} and a high μ_{eff}.[8] In addition, the TFT with a nitrogen-rich SiN_x gate dielectric is more stable than that with a silicon-rich gate dielectric.[9-11] For the inverted, trilayer TFT the V_{th} decreases with the increase of the deposition power of the gate SiN_x layer.[12] Therefore, the gate SiN_x structure, which is affected by its deposition process, plays a major role on TFT characteristics.

It is generally known that the mobility of a TFT, *i.e.*, μ_{eff}, is dominated by the quality of the a-Si:H layer and the interface characteristics of a-Si:H and gate dielectric.[13] The threshold voltage V_{th} shift is due to the state creation in the a-Si:H film at or near the interface or charge trapping in the gate SiN_x layer.[10,14] It would be desirable to have a gate dielectric of which the interface and bulk properties can be controlled independently. One method of preparing this kind of structure is to deposit a dual-gate SiN_x. The first SiN_x, which is not in contact with a-Si:H, functions as the

bulk gate dielectric layer. It should be low in charge trapping so that the V_{th} is low. Its deposition rate can be high so that a thick layer can be deposited in a short period of time. The second SiN_x, which is in contact with a-Si:H, should have low interfacial density of states so that the device is stable and the mobility μ_{eff} is high. There are reports on TFTs prepared from similar concepts. For example, H_2 and NH_3 plasmas were used to modify the gate dielectric surface before the a-Si:H layer was deposited.[15-17] In these papers the second layer is limited to the surface and is very thin. Compared with the TFT without a plasma treatment, the resulting TFTs often have a higher V_{th} and a higher subthreshold slope (S) because of the plasma damage to the interface.[17] Another method of preparing the dual layer structure is to deposit a thin, *i.e.*, 100 Å, SiN_x buffer layer.[16] When the buffer layer was deposited from a low NH_3 to SiH_4 flow ratio, the TFT characteristics deteriorate. When the buffer layer was deposited from a gradually decreasing NH_3 to SiH_4 flow ratio, *i.e.*, from 10 to 5, the mobility increased and the subthreshold slope (S) decreased. The composition of the buffer layer changed toward a higher silicon to nitrogen ratio as the interface was approached. This is contradictory to other reports.[9,10] More studies are needed to explain this phenomenon. In addition, it is difficult to control the process when the film is only 100 Å thick and the feeding gas is continuously changed during the deposition. Kaneko *et al.*[11] compared the stability of TFTs with gates prepared from combinations of two kinds of SiN_x, *i.e.*, one silicon-rich and the other one nitrogen-rich. The TFT with the silicon-rich interface layer was less stable than the TFT with the stoichiometric interface layer. The threshold voltage shift was dependent on the gate electric field in the gate dielectric layer. A comparison of other TFT characteristics was not reported. However, it has been proved that there are many kinds of nitrogen-rich SiN_x films.[5,6] These films may have different characteristics. In addition, the double-layer gate dielectric structure has some advantages over the single-gate dielectric structure, *e.g.*, minimizing the source/drain and gate shortage. Therefore, a TFT with a graded gate dielectric structure, which is composed of two distinct nitrogen-rich SiN_x layers, has the potential of being highly reliable with high performance. So far, little information on this kind of TFT is available. In this paper the author studies the graded SiN_x gate dielectric TFTs. The interface SiN_x layer is about 500 Å which is thick enough for the reliable control of the deposition process and thin enough to have direct influence on the a-Si:H interface. Device characteristics of the gradient gate dielectric TFT are compared with those of a single gate dielectric TFT.

Experimental

The inverted, trilayer TFTs, as shown in Fig. 1, were prepared on Corning 7059 glass. Fours masking steps, *i.e.*, for gate, active island, source/drain vias, and top metal, were used. The gate metal was composed of 1000 Å molybdenum. The trilayer was composed of gate dielectric (about 3000 Å), a-Si:H (500 Å), and top SiN_x (2500 Å), which were deposited in a multichamber PECVD system without breaking vacuum. The source/drain layer was composed of 600 Å heavily phosphorus doped silicon, *i.e.*, n^+, and 3000 Å molybdenum. The a-Si:H active island and the n^+ source/drain area were reactive ion etched with a Plasma Therm 2480 reactor using $SiCl_4/CF_4$ 95/5 sccm at 100 mTorr, 1000 W. The detailed etching mechanism and device effects of this process have been reported previously.[18,19] Other etching steps were carried out using wet processes. After the n^+ etch step, the photoresist was stripped and transistors were annealed in air for 5 h at 250°C to remove plasma damages.[19]

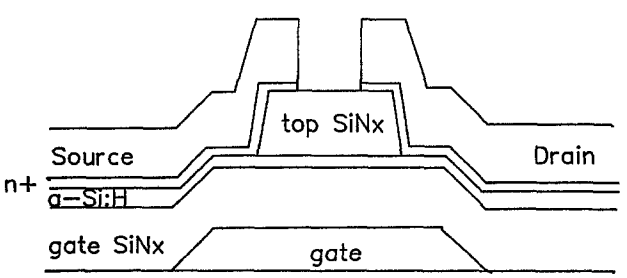

Fig. 1. Cross-sectional view of TFT.

The PECVD system used in these experiments is the Ulvac (CPD-7433) multichamber system which has a 13.56 MHz RF power supply in each chamber. The power density on the RF driven electrode was 0.048 W/cm^2 at 100 W. All films were deposited at 250°C. Gate SiN_x films were deposited from $SiH_4/NH_3/N_2$ at 500 mTorr. The flow rate of each gas and the power were varied in different experiments. Detailed relations between process parameters, such as power and gas composition, and material characteristics, such as the deposition rate, the refractive index, the stress, and the N-H/Si-H ratio, as well as the role of hydrogen in the plasma, have been published.[6] In summary, for each feeding stream there exists a critical plasma power $W_{critical}$ in the deposition curve. When the power is lower than $W_{critical}$, the process and film characteristics follow the conventional PECVD relationships, *e.g.*, the deposition rate increases and the refractive index decreases with the increase of power. When the power is greater than $W_{critical}$, the process and material characteristics cannot be explained by conventional PECVD mechanisms. The hydrogen etching phenomenon becomes important in this range.[5] For the graded TFT the first SiN_x layer was deposited from $SiH_4/NH_3/N_2$ 40/80/500 sccm at 500 mTorr and 300 W. The second (interfacial) SiN_x was deposited from same N_2 and NH_3 flow rates except the SiH_4 flow rate (between 10 and 40 sccm) and the power (between 120 and 400 W) were varied. The a-Si:H layer was deposited from SiH_4 50 sccm at 250 mTorr and 85 W. All TFTs have the same top SiN_x layer which was deposited from $SiH_4/NH_3/N_2$ 40/80/500 sccm at 500 mTorr and 300 W. The stress of the SiN_x film was estimated with one single layer of SiN_x deposited on a 3 in. silicon wafer usng a Tencor P-1 profiler (Mt. View, CA).

The field effect mobility μ_{eff} and the threshold voltage V_{th} were calculated from the saturation range of the transfer characteristics with the equation $I_d = 1/2\ \mu_{eff}\ (W/L)\ C\ (V_g - V_{th})^2$. The on current I_{on} was the drain current I_d measured at $V_g = 20$ V and $V_d = 10$ V. The off current I_{off} was the minimum drain current at $V_d = 10$ V and V_g between -5 and 0 V. The subthreshold slope S was calculated from the transfer characteristics at $V_d = 1$ V.

Results and Discussion

Figure 2 shows the transfer functions of a TFT with a graded SiN_x gate dielectric structure. The interfacial SiN_x was deposited from $SiH_4/NH_3/N_2$ 20/80/500 sccm at 500 mTorr and 200 W. This transistor has a μ_{eff} 1.02 cm^2/Vs, a V_{th} of 2.5 V, and an I_{on}/I_{off} ratio 10^8. Figures 3 to 6 show μ_{eff}, V_{th}, on/off currents, and subthreshold slope S of TFTs with graded gate dielectric layers. Characteristics of TFTs with single-gate dielectric layers are also included in the figure for comparison.

Mobility.—The following conclusions can be summarized from Fig. 3: (*i*) for TFTs with single-gate dielectrics deposited at 300 W, the μ_{eff} increases with the feeding SiH_4 concentration first and then decreases with the further increase of the SiH_4 concentration; (*ii*) for TFTs with single-gate dielectrics which were deposited from the same feeding stream ($SiH_4/NH_3/N_2$ 20/80/500 sccm) the μ_{eff} increases with the increase of the deposition power; (*iii*) for TFTs with graded gate dielectrics, the μ_{eff} increases with the increase of the deposition power of the interfacial SiN_x layer; and (*iv*) the μ_{eff} of a TFT with graded gate SiN_x is higher than that of a TFT with a single-gate SiN_x when both have the same deposition condition for the interfacial SiN_x.

The field effect mobility is related to localized state distribution in the a-Si:H layer and near the SiN_x/a-Si:H interface.[7] The stress at the SiN_x/a-Si:H interface is stronger than those in bulk adjacent films. This high stress could

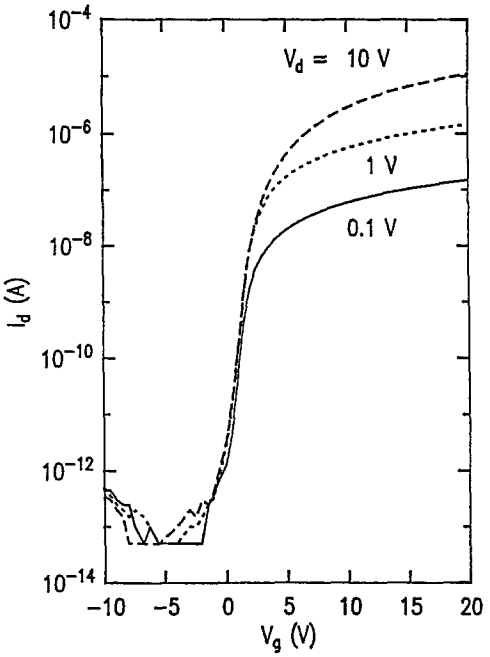

Fig. 2. Transfer characteristics of a graded gate TFT.

spread out into the bulk a-Si:H layer.[10] The higher the interfacial stress is the wider the tail state in the a-Si:H layer is. In a TFT when the width of the tail state density in the a-Si:H layer increases, its field effect mobility decreases and the subthreshold slope increases.[7,8] Since all TFTs in this paper have the same a-Si:H layer, the mobility is mainly influenced by the interface characteristics. Refractive indexes of the three 300 W deposited single dielectrics in Fig. 3 are 1.85, 1.76, and 1.90 for the SiH_4 flow rate of 10, 20, and 40 sccm, respectively.[5] In a typical PECVD SiN_x film the Si/N ratio increases with the increase of the refractive index. If the interface SiN_x structure is not affected by the a-Si:H deposition process, the order of the mobility of these three single-gate TFTs is consistent with the order of the nitrogen content in the gate SiN_x films. The same relation is true for a TFT with the single-gate dielectric deposited from $SiH_4/NH_3/N_2$ 20/80/500 sccm.

Mobilities of the graded TFTs are higher than those of single-gate TFTs although their interface SiN_x deposition conditions are the same. The reason of this improvement is not clear, currently. However, electrical defects at the interface of gate SiN_x and a-Si:H is influenced by bulk properties of the gate dielectric film. For the grade SiN_x TFT, the interface film is thin compared with the other layer, *i.e.*, about 500 *vs.* 2500 Å. For the single SiN_x TFT, the whole gate dielectric structure is uniform, *e.g.*, about 3000 Å.

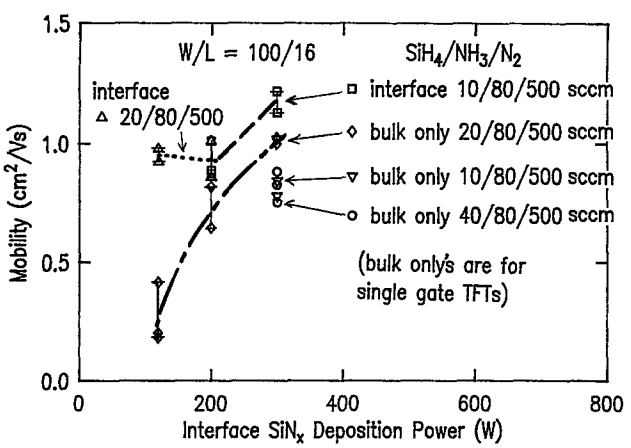

Fig. 3. Interface SiN_x power effect on TFT field effect mobility, bulk 40/80/500 sccm, 300 W, 250°C.

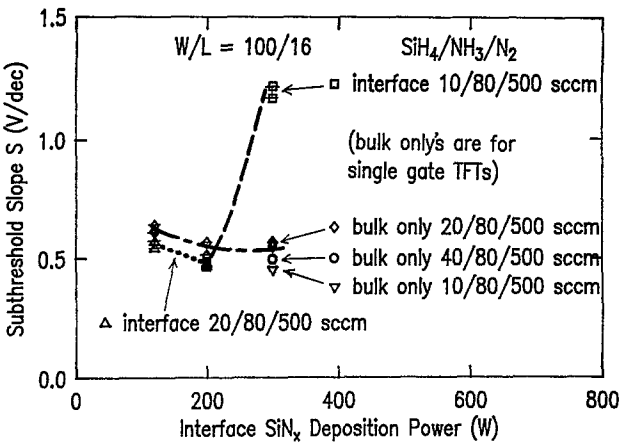

Fig. 4. SiN_x deposition power effect on TFT subthreshold slope, bulk SiN_x deposited at 500 mTorr and 250°C.

Therefore, bulk properties of the single and graded gate dielectrics are different. It is possible that electrical defects of the interface SiN_x in the graded dielectric TFT are less than those in the single SiN_x TFT. This gives the former a higher mobility than the later.

Subthreshold slope.—Figure 4 shows the subthreshold voltages of these TFTs *vs.* the interfacial SiN_x deposition power. The following conclusions can be summarized from the figure: (*i*) for TFTs with single-gate dielectrics deposited at 300 W, the subthreshold slopes are about the same; (*ii*) for TFTs with single SiN_x gate dielectrics which were deposited from the same feeding stream ($SiH_4/NH_3/N_2$ 20/80/500 sccm), the *S* decreases slightly with the increase of the deposition power; (*iii*) for TFTs with graded gate dielectrics the *S* appears to be related to the deposition condition of the second SiN_x layer. If the second SiN_x is deposited from $SiH_4/NH_3/N_2$ 20/80/500 sccm, the *S* decreases slightly with the increase of power. If it is deposited from $SiH_4/NH_3/N_2$ 10/80/500 sccm, the *S* increases drastically between 200 and 300 W; (*iv*) except for the graded gate TFT with the second gate SiN_x deposited at 300 W, TFTs with gradient gate dielectrics have *S*s lower than those having single-gate dielectrics.

The subthreshold slope is an indication of the density of states of the bulk a-Si:H layer and the interface states around the Fermi-level.[16,17,20] Since all TFTs have the same a-Si:H layer, we can assume that their bulk a-Si:H properties are the same.[10] The difference in *S* comes from the interface states which are contributed by different gate dielectric deposition processes. As discussed in the mobility section, the nitrogen content in the SiN_x film increases with the increase of the deposition power when the feeding stream is $SiH_4/NH_3/N_2$ 20/80/500 sccm. Hiranaka *et al.*[10] used cw photoluminescence spectra (He-Cd laser) to study 100 Å a-Si:H in the a-Si:H/SiN_x interface with different *x*s. They found that the photoluminescence bandedge E_{PL} shifted to lower energies as *x* increased. It was concluded that the lower-energy shift of the cw photoluminescence band was caused by an increase in the deep states near the interface a-Si:H. This effect was enhanced as the SiN_x became more nitrogen rich.[10] Therefore, the TFT subthreshold slope should decrease with the increase of the nitrogen content in the gate SiN_x layer. Figure 4 shows that for the single-gate SiN_x TFT the result is consistent with the above statement. The same relation is also true for graded gate dielectric TFTs when the second SiN_x layer is deposited at a low power, *e.g.*, less than 300 W. However, the *S* of the graded gate TFT is lower at the low power and is higher at the high power than the corresponding single-gate TFT. Since all TFTs in these experiments were prepared from the same trilayer except the gate SiN_x layers, it is reasonable to assume that the difference is related to the stress of the gate dielectric structure. It has been reported that the SiN_x film has a tensile stress when its deposition power is lower than

the critical power $W_{critical}$.[6] The stress decreases with the increase of the power. When the power is higher than the critical power, the stress becomes compressive. The $W_{critical}$ increases with the increase of the SiH_4 flow rate. Stresses of the films deposited from $SiH_4/NH_3/N_2$ 20/80/500 sccm at 120 and 200 W are higher than that deposited from $SiH_4/NH_3/N_2$ 40/80/500 sccm at 300 W, *i.e.*, 8.57×10^9, 3.59×10^9 *vs.* 1.73×10^9 dyne/cm^2. When the high stress film is deposited on top of the low stress film, its stress is relaxed slightly. Therefore, the interface defect density of states of the a-Si:H film deposited on top of it is lower than that deposited on the corresponding single dielectric layer. The subthreshold slope of the former is lower than that of the latter. However, when the stress mismatch between the second film (*e.g.*, deposited from $SiH_4/NH_3/N_2$ 10/80/500 sccm at 300 W) and the first film (*e.g.*, deposited from $SiH_4/NH_3/N_2$ 40/80/500 sccm at 300 W) is very high, *i.e.*, compressive 3.38×10^9 *vs.* tensile 2.09×10^9 dyne/cm^2, it may propagate to the interface of the second SiN_x and the a-Si:H layer. The defect density of the a-Si:H layer near the interface is higher than that at the interface with a corresponding single dielectric. This causes the extremely high subthreshold slope of graded gate TFT of which the second SiN_x was deposited from $SiH_4/NH_3/N_2$ 10/80/500 sccm at 300 W.

Threshold voltage.—The following conclusions can be summarized from Fig. 5: (*i*) for TFTs with single SiN_x gate dielectrics deposited at 300 W, the V_{th}s are about the same except for the one deposited from a SiH_4 flow rate of 40 sccm; (*ii*) for TFTs with single SiN_x gate dielectrics which were deposited from the same feeding stream ($SiH_4/NH_3/N_2$ 20/80/500 sccm), the V_{th} decreases slightly with the increase of deposition power; (*iii*) for TFTs with graded gate dielectrics the V_{th} appears to be related to the deposition condition of the second SiN_x layer. If the second SiN_x is deposited from $SiH_4/NH_3/N_2$ 20/80/500 sccm, the V_{th} decreases slightly with the increase of power from 120 to 200 W. If it is deposited from $SiH_4/NH_3/N_2$ 10/80/500 sccm, the V_{th} increases drastically from 200 to 300 W; (*iv*) except the graded gate TFT with the second gate SiN_x deposited at 300 W, TFTs with graded gate dielectrics have V_{th}s lower than those of TFTs having single-gate dielectrics.

The threshold voltage is related to the trap state distribution and the fixed charge distribution in the gate SiN_x layer which includes both in the bulk and at near the SiN_x/a-Si:H interface.[7] For the inverted, staggered TFT of which the gate SiN_x was deposited from NH_3/SiH_4 (20% in H_2), the threshold voltage has a minimum value at $x = 1$. The threshold voltage change with the SiN_x composition reflects the difference of band bending near the a-Si:H/SiN_x interface.[7] For single-gate dielectric TFTs in Fig. 5 when the gate SiN_x layers are deposited from the same gas stream ($SiH_4/NH_3/N_2$ 20/80/500 sccm), the V_{th} *vs.* power relation is similar to the refractive index *vs.* power relation.[6] In both

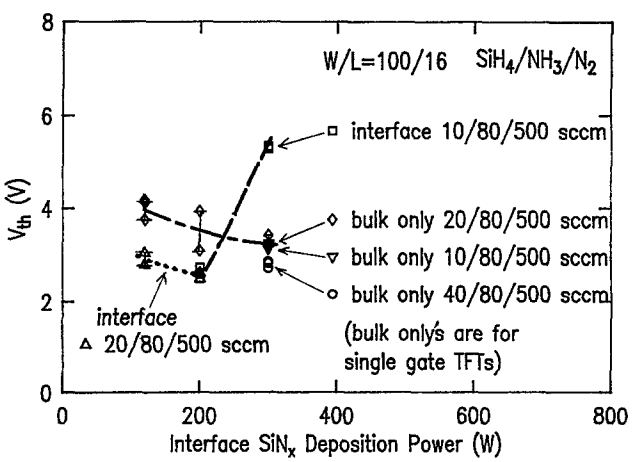

Fig. 5. Interface SiN_x power effect on TFT threshold voltage, bulk SiN_x 40/80/500 sccm, 300 W, 250°C.

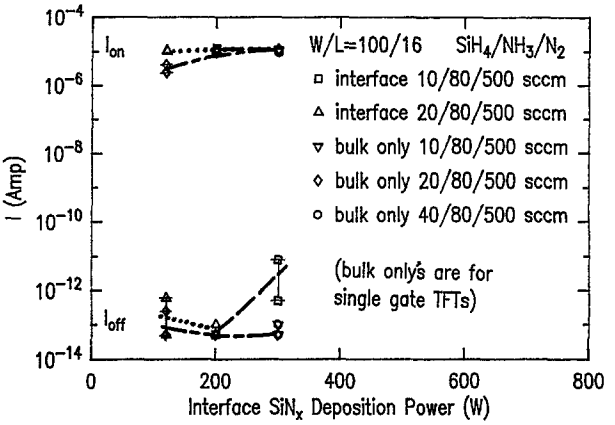

Fig. 6. Interface SiN_x power effect on TFT I_{on} and I_{off}, bulk SiN_x 40/80/500 sccm, 300 W, 250°C.

cases, the curves decrease with the increase of power when the power is less than 300 W. The N/Si ratio from the electron spectroscopy for chemical analysis (ESCA) measurement are: 1.64, 1.17, and 1.23 at the power of 100, 200, and 300 W, respectively. Therefore, for these single-gate SiN_x TFTs, the V_{th} variation is qualitatively consistent with the results in Ref. 7 although their gate SiN_x layers are deposited from different feeding gases.

For graded gate TFTs the gate dielectric defects originated from three areas: the bulk of the first SiN_x layer, the bulk of the second SiN_x layer, and the interface of the above two layers. When the last factor is negligible, *e.g.*, all conditions except $SiH_4/NH_3/N_2$ 10/80/500 sccm at 300 W, the total gate defect density is the sum of the defect densities of the two bulk layers. Since all graded gate TFTs have the same first dielectric layer, the difference in their defect densities should be the same as the difference in the second dielectric layers. Therefore, the trend of the decreasing of the V_{th} with the increase of the deposition power of the second SiN_x in the graded gate dielectric TFT is the same as that in the single-gate dielectric TFT. The findings resulted from the condition that there is no serious surface damage or stress generated at the interface of the two gate dielectric layers. When the second SiN_x is deposited from $SiH_4/NH_3/N_2$ 10/80/500 sccm at 300 W, the deposition process includes a strong hydrogen etching phenomenon.[6] This etching mechanism may change the surface structure of the first SiN_x layer. A high defect density layer is formed at the interface which drastically increases the total defect density of the gate dielectric structure. Therefore, the TFT with this kind of gate dielectric has a much higher V_{th} than other TFTs.

On and off currents.—The following conclusions can be summarized from Fig. 6: (*i*) the difference among all I_{on}s is within an order of magnitude. These I_{on}s are in the same order as the mobilities in Fig. 3; (*ii*) for TFTs with single-gate dielectrics deposited at 300 W the I_{off} of the dielectric deposited from $SiH_4/NH_3/N_2$ 10/80/500 sccm is slightly higher than others; (*iii*) when the feeding streams are the same, the I_{off} of the single gate TFT decreases slightly with the increase of the power; (*iv*) for TFTs with graded gate dielectrics the I_{off}s are slightly higher than those of corresponding single gate dielectric TFTs; (*v*) when the interfacial gate dielectric is deposited from $SiH_4/NH_3/N_2$ 10/80/500 sccm at 300 W, the I_{off} is the highest among all TFTs; (*vi*) all TFTs have an I_{on}/I_{off} ratio greater than 10^6.

Both on and off currents are related to the characteristics of the bulk and interfacial properties of the a-Si:H layer. Since all TFTs have the same a-Si:H layer, the bulk a-Si:H effect on the current flow can be assumed to be the same. The interface qualities are affected by both the chemical structure and the physical properties such as the stress of related films. It is difficult to differentiate these two factors. However, there are indications that the stress of the

gate dielectric layer may affect the off current. For example, the SiN_x films deposited from $SiH_4/NH_3/N_2$ 20/80/500 sccm, the tensile stress decreases with the increase of power, *i.e.*, 8.57×10^9, 3.76×10^9, 1.73×10^9 dyne/cm^2 at 120, 200, and 300 W, respectively. Figure 6 shows that TFTs with the above single-gate dielectrics the off current decreased slightly with the decrease the stress. The SiN_x film deposited from $SiH_4/NH_3/N_2$ 40/80/500 sccm 300 W has a tensile stress of 2.09×10^9 dyne/cm^2. Therefore, when the second SiN_x is deposited (from $SiH_4/NH_3/N_2$ 20/80/500 sccm) on top of the above SiN_x layer, the stress mismatch of the dual dielectric layer decreases with the increase of the deposition power of the second layer. This is consistent with the trend of the off current change with the interface SiN_x deposition power in Fig. 6. The SiN_x film deposited from $SiH_4/NH_3/N_2$ 10/80/500 sccm has a tensile stress of 8.16×10^8 dyne/cm^2 at 200 W and a compressive stress of 3.38×10^9 dyne/cm^2 at 300 W. When it is deposited on top of the SiN_x with a tensile stress of 2.09×10^9 dyne/cm^2, the latter causes a much higher stress mismatch than other gate dielectrics in Fig. 5. This could explain the reason for the high off current in the high power (300 W) deposited gradient TFT.

Conclusion

Graded SiN_x gate dielectric TFTs, which have two distinct nitrogen-rich SiN_x layers, have been prepared with a process temperature of 250°C. Device characteristics, such as mobility, subthreshold slope, threshold voltage, and on/off currents, were measured. They were compared with those of single-gate SiN_x TFTs. The advantage of the graded gate TFT is that the interface and the bulk SiN_x properties can be controlled independently. This redundant structure can give a higher yield for the large TFT matrix preparation. In principle, the interface SiN_x mainly influences the a-Si:H/gate dielectric interface characteristics and the bulk SiN_x mainly affects the bulk characteristics of the gate dielectric structure. However, results in this paper show that properties of these two films can influence each other. TFT performance could be improved or deteriorated with the graded SiN_x structure. Both the composition and the stress of the interface SiN_x are critical to TFT characteristics. When the interface SiN_x is deposited at a power lower than the critical power, the TFT characteristics such as the mobility, subthreshold slope, and threshold voltage are better than the single-gate SiN_x TFT. When the interface SiN_x is deposited at a power higher than the critical power, these characteristics are worse than the single gate SiN_x TFT. The off current is slightly higher in the former than in the latter. In summary, the graded gate TFT can have better device performance than the single-gate TFT if proper SiN_x deposition conditions are selected.

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