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ORIGINAL PAPER

Dual-material gate dual-stacked gate dielectrics gate-source overlap tri-gate germanium FinFET: analysis and application

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Abstract: This study proposes a novel dual-material-gate dual-stacked-gate dielectrics gate–source overlap Ge FinFET and compares its characteristics with conventional FinFET. The proposed device shows very less leakage current (I_{OFF}) ($\sim 10^{-17}$ A), significant on drain current ($\sim I_{ON}$) ($\sim 10^{-4}$ A), very high ratio of I_{ON} to I_{OFF} (I_{ON}/I_{OFF}) ($\sim 10^{13}$) and less subthreshold swing of (SS) (71 mV/dec). This study presents the effect of different dielectrics, oxide thicknesses (t_{ox}) and back-gate voltages (V_{GB}) on transfer characteristics of the proposed device. The effect of channel concentration on I_{ON}/I_{OFF}, threshold voltage (V_{th}), transconductance (g_m) and SS is also investigated. The effect of overlap length (L_{ov}) on analog parameter, gate–source capacitance (C_{gs}), is also analyzed. Moreover, the effect of fin thickness (T_{fin}) on V_{th} and SS is also studied. The height of the BOX plays an important role in reducing I_{OFF}. Moreover, with emphasis on digital application, by using the proposed device a digital inverter circuit is implemented, and this study investigates the characteristics using mixed-mode simulation.

Keywords: FinFET; Dual-stacked-gate dielectrics; Dual material gate; Gate–source overlap

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1. Introduction

The projection of Moore's law [1] causes an exponential increase in speed of chip and density of chips, an exponential decrease in power dissipation and the cost per function [2], and the easy portability of the electronic goods, which also fulfill the present semiconductor industry demands. Thus, in order to sustain these demands, the MOS device dimensions are scaled down continuously. The scaling of dimensions causes the degradation of performances in terms of short-channel effects (SCEs) [3–5]. The scaling of oxide thickness causes the band-to-band tunneling in the gate–drain overlap region which enhances gate-induced drain leakage (GIDL) current [6], high drain leakage current and the penetration of gate dopants in the channel region [7]. Due to the scaling of channel length, the charge is shared between the channel and the drain regions, which reduces the influence of gate control on the channel, which, in turn, enhances the off current (I_{OFF}). Therefore, in order to overcome these drawbacks of scaling of MOS device dimensions and to fulfill the commercial demands of the present semiconductor industry, FinFET can be used as a suitable alternative to MOSFET [8]. The fin shape–geometry with straddling nature of gate over the channel of FinFET enhances the electrostatic stability of the device. The two most important parameters of FinFET such as fin height and the fin width play a key role in improving the characteristics of the device by mitigating the SCEs. To limit the SCEs, a double-gate (DG) FinFET is proposed for scaled gate length, and the DG FinFET can be fabricated easily using the conventional MOSFET process technology [8] and has a high outstanding transconductance value at 105 nm gate length [9]. By using 2-D device and mixed-mode circuit simulation, the speed of the gate–source/gate–drain underlap FinFET is analyzed and manifests that there is no deterioration in the speed when the fin thickness is extended to the physical gate length of the device [10]. An impact of width quantization on device characteristics of trapezoidal-shaped silicon FinFET is investigated, and it is found that for a thinner bottom width the device shows more reliability [11]. A dual-material-gate heterojunction FinFET shows improved electrical

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characteristics compared with conventional FinFET, and a less drain-induced barrier lowering (DIBL) value was found [12]. To avoid the corner effects and the SCEs, omega-shaped gate FinFET and cylindrical gate-all-around FinFET are used, and it is demonstrated that the cylindrical gate-all-around FinFET shows better electrostatic behavior compared with omega-shaped gate FinFET [13]. Moreover, to improve the functionality of the device, a number of different FinFET structures have been proposed such as tapered tri-gate FinFET [14, 15], pie-shaped gate bulk FinFET [16] and scallop-shaped FinFET [17]. So, there is still a scope of new FinFET geometry, which shows very less leakage current (I_{OFF}), high ratio of on current to off current (I_{ON}/I_{OFF}) and less SCEs. A device is said to be stable, when it does not show drastic changes when temperature range is varied from low to high. In adding to it, the efficiency of the device can also be examined by using the proposed device in a low-power digital inverter circuit.

In this study, we propose a novel FinFET and its application as a digital inverter circuit. The use of high k dielectric enhances the on drain current significantly. Moreover, the overlapping of high work function gate on source reduces the leakage current (I_{OFF}). Moreover, it achieves subthreshold swing (SS) value of closer to kT/q limit (60 mV/dec), and less threshold voltage. In addition to it, for a wide range of temperatures, the proposed device does not show drastic changes in I_{OFF}, which makes the device more stable. By considering the efficiency of the proposed device, a low-power digital inverter circuit is used.

This study is organized as follows: Sect. 2 describes the geometry of the proposed device with structural specifications. The simulation setup and the different models used for simulation are discussed in Sect. 3. The extracted results and its related discussions are analyzed in Sect. 4, and finally, Sect. 5 concludes the present work.

2. Device geometry

The proposed device geometry with 3-D view and cross section of front view is shown in Fig. 1. The proposed device is a dual-material-gate dual-stacked-gate dielectric gate–source overlap Germanium (Ge) FinFET. In the proposed device, Ge material is used as a fin. The Ge material has some electronic properties. It is a diamond-type structure [18]. The energy bandgap of Ge at 0 Kbar pressure is 0.66 eV [18]. The Ge material has some properties, such as an increase in pressure increasing both direct and indirect bandgaps [18]. The gate dielectrics GeO_2 (k = 3.8) and HfO_2 (k = 22) are placed in stack. In this gate oxide, the two gate materials such as gold (ϕ_m = 5.4 eV) and aluminum (ϕ_m = 4.1 eV) are placed laterally, where the

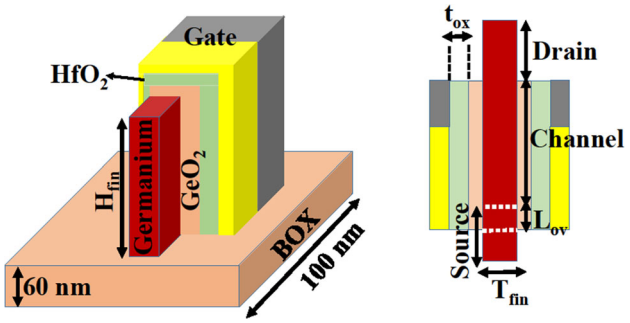


Fig. 1 Left: 3-D view and right: front view of the proposed FinFET. H_{fin} defines the height of the fin, T_{fin} defines the width/thickness of the fin, t_{ox} is the oxide thickness and L_{ov} is the overlap length of the proposed device

gold is placed in the source side and aluminum is placed in the drain side, and the gate along with oxide is overlapped on source. The n^+ source and n^+ drain have a length of 5 nm doped with a concentration of 10^{20} cm^{-3}. The device with dimensional specifications is shown in Fig. 1.

3. Simulation deck

The simulation results of the proposed device are obtained using Synopsys TCAD [19]. Fermi–Dirac statistics, which is one of the physics models used for simulation, is enabled to consider the precise distribution of carriers [19]. The doping-dependent mobility model and the bandgap narrowing model are also activated to account the effect of mobility of the carriers [19].

4. Results and discussion

4.1. Comparative analysis between the conventional FinFET and the proposed dual-material-gate dual-stacked-gate dielectrics gate–source overlap Ge FinFET

Figure 2 shows the comparative transfer characteristics between the proposed FinFET and the conventional FinFET structure. It is observed that the extracted results from the proposed device show better electrostatic characteristics in terms of significant I_{ON}, less I_{OFF}, high I_{ON}/I_{OFF} and less subthreshold swing (SS). The behavior of the characteristics can be explained from the geometry of the proposed device. In the conventional FinFET, a single dielectric having k = 3.9 is used, whereas in the proposed device, the two dielectrics having k = 3.8 and k = 22 are placed in stack. Therefore, the equivalent dielectric constant in the proposed device is $\sim$ 3.3, which is lesser than the single dielectric constant ($\sim$ 3.9). As a result, the

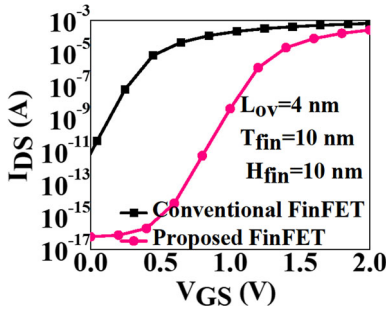


Fig. 2 Comparative transfer characteristics between the conventional FinFET and the proposed FinFET

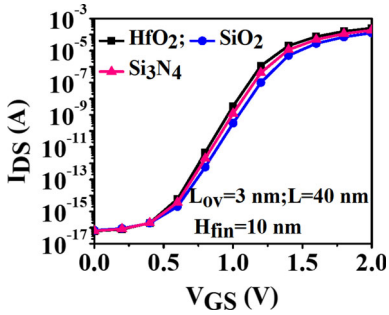


Fig. 3 Transfer characteristics for different gate stack dielectrics having T_{fin} = 10 nm and t_{ox} = 2 nm

effective capacitance is reduced and thus a significant on drain current is obtained. For the proposed device, the value of I_{OFF} is found less as the gate material of conventional FinFET replaced by two gate materials having high work function (ϕ_m = 5.5 eV) and low work function (ϕ_m = 4.1 eV), placed in parallel and also overlapping of gate on source. The overlapping of gate on source suppresses the energy barrier more on source side, and the presence of high work function gate material on source side increases the work function difference (ϕ_{ms}) between the gate material (ϕ_m) and the semiconductor (ϕ_s). The high work function gate material near the source accelerates the carrier from source to drain and enhances the electric field distribution in the channel. Thus, a very less value of I_{OFF} and a high value of I_{ON}/I_{OFF} are found in the proposed device. Since the proposed device shows high electrostatic nobility, thus further investigation is analyzed for different structural and electrical specifications of the proposed device.

4.2. Effect of different dielectrics on transfer characteristics

The change in behavior on the transfer characteristics for dielectric materials above GeO_2 is shown in Fig. 3. It is observed that the high k dielectric HfO_2 with GeO_2 shows better results compared with the other dielectrics SiO_2 and Si_3N_4. It is because the high dielectric constant (k = 22) of HfO_2 increases the effective gate capacitance and hence at same oxide thickness, the on current is increased. According to the drain current equation [20]:

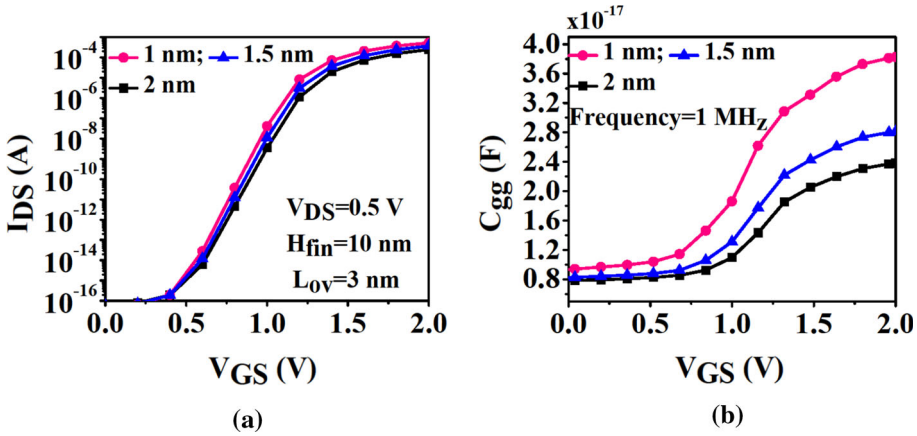
$$I_D = \mu(\varepsilon_{ox}/t_{ox})\,(W/L)\,\left((V_{GS} - V_{th})\,V_{DS} - V_{DS}^2/2\right),$$

where μ is the mobility of the carrier, W is the width of the channel, L is the length of the channel, V_{th} is the threshold voltage, and V_{DS} is drain to source voltage. So, drain current is directly proportional to the dielectric permittivity of the dielectric material. As the dielectric permittivity is increased, drain current is also increased.

4.3. Effect of different t_{ox} on transfer characteristics

Figure 4(a) shows the transfer characteristics for different t_{ox}. Figure 4(a) shows that with the increased t_{ox}, drain current decreases. The increased t_{ox} reduces the gate oxide capacitance, which in turn reduces the I_{ON}. The reason behind decreasing the drain current with respect to increased t_{ox} can also be explained from the total gate capacitance curve with respect to V_{GS}, as shown in Fig. 4(b). As in [21], with the increase in oxide thickness,

Fig. 4 (**a**) Transfer characteristics and (**b**) C_{gg} versus V_{GS} for different t_{ox} having T_{fin} = 10 nm



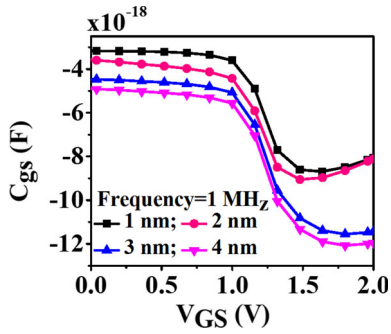


Fig. 5 C_{gs} versus V_{GS} for different L_{OV} for T_{fin} = 10 nm, H_{fin} = 10 nm and t_{ox} = 2 nm

gate capacitance decreases. That is, with the increased value of t_{ox}, gate control on the channel reduces, resulting in reduction in gate capacitance.

4.4. Effect of overlap length (L_{ov}) on gate–source capacitance (C_{gs})

The C_{gs} versus V_{GS} for different overlap lengths (L_{ov}) is shown in Fig. 5. As the overlap length increases, the energy bands get more suppressed in the source side and the barrier between the source and the channel increases. The high energy barrier for longer L_{ov} degrades the number of electrons flowing from source to drain and degrades the gate control on the overlap region. Thus, C_{gs} decreases with increasing L_{ov}.

4.5. Effect of different channel concentrations on electrical specification

The change in I_{ON}/I_{OFF} and the threshold voltage (V_{th}) with respect to different channel concentrations is shown in Fig. 6(a). Figure 6(a) shows that with the increase in channel concentration, the ratio of I_{ON} to I_{OFF} increases as well as V_{th} also increases. The increase in I_{ON}/I_{OFF} can be explained with the help of the mobility curve, as shown in Fig. 6(b). With the increase in channel concentration, mobility decreases due to scattering effect. In case of concentrations 10^{18} and 10^{19}, from the middle part of the channel, mobility increases suddenly. This is due to the presence of low work function (ϕ_m = 4.1 eV) gate material in the drain side, which influences to intensify the mobility of the carrier.

Moreover, the change in threshold voltage value with the change in concentration can be explained with the help of electrostatic potential curve, as shown in Fig. 6(c). As the channel concentration is increased, the electrostatic potential curve is decreased. That is, as concentration is increased, the same device requires more gate voltage to invert the channel. The position, where the gate material is changed from high work function to low work function, a deep at the point in the electrostatic potential curve, is noticed.

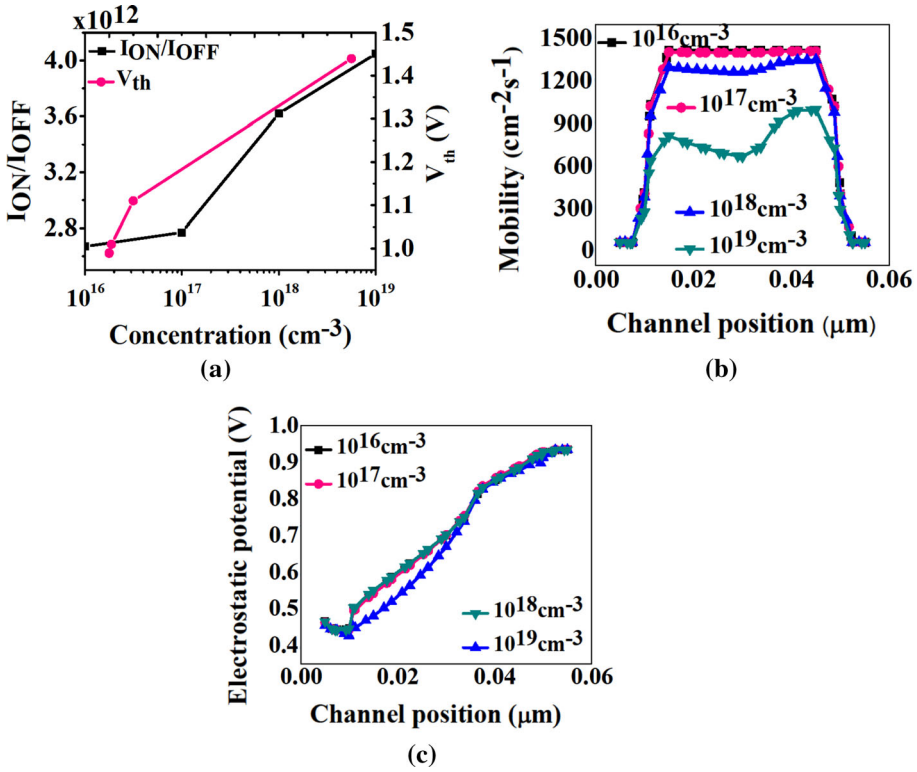


Fig. 6 (**a**) I_{ON}/I_{OFF} and V_{th} versus channel concentration, (**b**) change in mobility with respect to channel positions for different channel concentrations and (**c**) electrostatic potential at different channel concentrations for T_{fin} = 10 nm, H_{fin} = 10 nm and t_{ox} = 2 nm

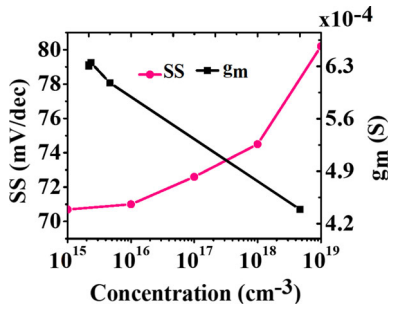


Fig. 7 g_m and SS versus channel concentration for T_{fin} = 10 nm, H_{fin} = 10 nm, L_{ov} = 4 nm and t_{ox} = 2 nm

4.6. Analysis of maximum transconductance (g_m) and subthreshold swing (SS) for different channel concentrations

The g_m and SS versus channel concentration is shown in Fig. 7. It is observed that with the increase in concentration, g_m decreases. As g_m is directly proportional to the on drain current, thus, with the increase in concentration, the maximum transconductance (g_m) decreases.

Subthreshold swing, an inverse of the subthreshold slope, increases with the increase in concentration. Subthreshold slope can be expressed as [20] = $\frac{d \log I_D}{dV_{GS}}$. That is, slope is directly proportional to the drain current. Since on drain current decreases with the increase in channel concentration, hence subthreshold slope decreases with the increase in concentration and hence the subthreshold swing increases with the increase in concentration.

4.7. Effect on leakage current (I_{OFF}) and I_{ON}/I_{OFF} for different gate materials on drain side

Leakage current (I_{OFF}) and the ratio of on current to off current (I_{ON}/I_{OFF}) are plotted with respect to the work function (ϕ_m) of different gate materials [Fig. 8(a)]. The work function is changed in drain side only by keeping the source side gate material as gold (ϕ_m = 5.5 eV) constant. As the work function is increased in the drain side, the work function difference between the gate material and the semiconductor increases, which results in a decrease in on drain current. When electron flows from source to drain, it faces two work function differences in the channel. When gate material is changed in the drain side from low work function to high work function, the work function difference (ϕ_{ms}) in drain side is less compared with the work function difference in the source side, resulting in an increase in I_{OFF} and consequently decrease in I_{ON}/I_{OFF}.

4.8. Effect on leakage current (I_{OFF}) and I_{ON}/I_{OFF} for different gate materials on source side

The plot of work functions of different gate materials placed in the source side by keeping the gate material in drain side constant with respect to the I_{OFF} and I_{ON}/I_{OFF} is shown in Fig. 8(b). With the increase in work function of the gate material placed in the source side, I_{OFF} decreases as well as I_{ON}/I_{OFF} increases. Due to the increase in work function, the work function difference between the gate material and the semiconductor increases. The larger work function difference requires more gate voltage to cause inversion in the channel. That is why, I_{OFF} decreases. Since a low work function gate material aluminum (ϕ_m = 4.1 eV) is placed in the drain side, a remarkable on drain current is found and thus high I_{ON}/I_{OFF} is found as we increase the work function.

Figure 8(a) shows more changes in the I_{ON}/I_{OFF} and I_{OFF} compared with Fig. 8(b). Moreover, it can be concluded that when high work function gate material is placed in source side and low work function gate material is placed drain side, a high ratio of I_{ON}/I_{OFF} and less I_{OFF} is found.

4.8.1. Effect of temperature on leakage current (I_{OFF}) for different fin heights

The leakage current (I_{OFF}) versus temperature for different fin heights is shown in Fig. 9(a). It is noticed that with the increase in temperature I_{OFF} increases. Moreover, for higher value of fin height, the I_{OFF} is more.

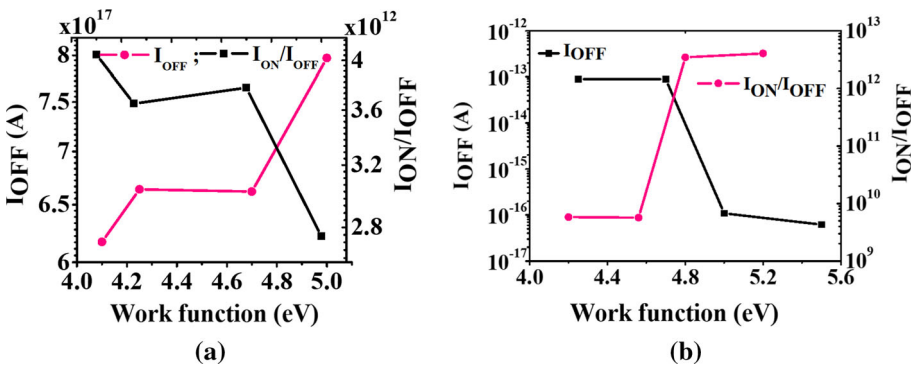


Fig. 8 Effect of (**a**) different gate side gate materials and (**b**) different source side gate materials on I_{OFF} and I_{ON}/I_{OFF} for T_{fin} = 10 nm, H_{fin} = 10 nm, L_{ov} = 4 nm and t_{ox} = 2 nm

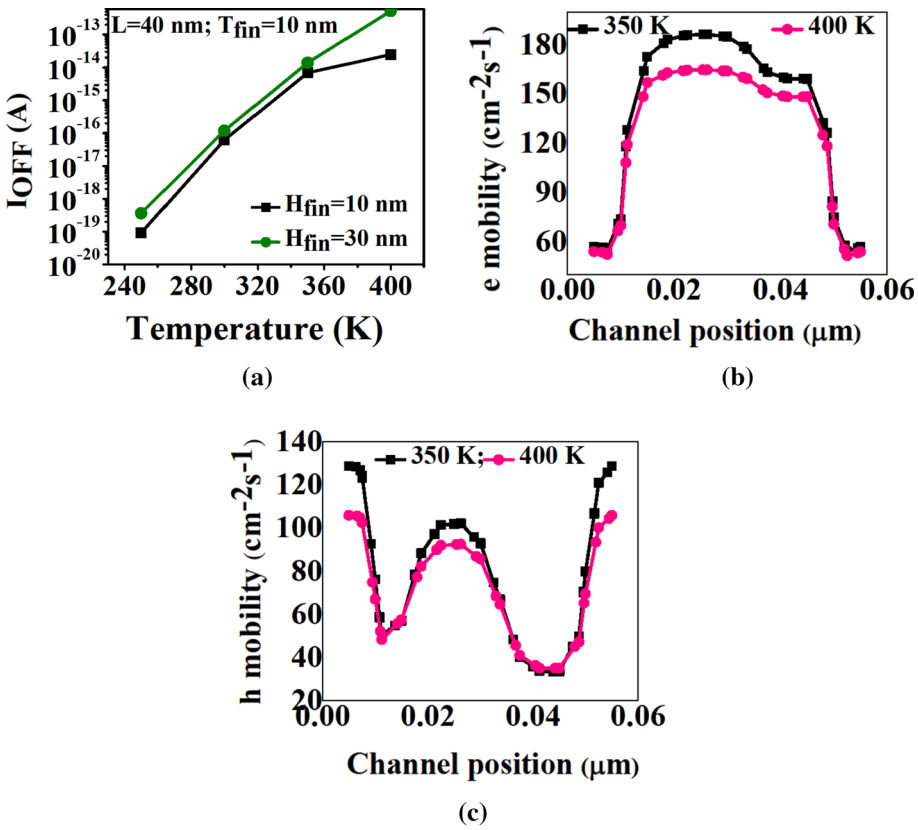


Fig. 9 (**a**) Leakage current (I_{OFF}) versus temperature at different fin heights, (**b**) electron mobility and (**c**) hole mobility with respect to channel position for different temperatures at V_{GS} = 0 V and H_{fin} = 10 nm

Mathematically, relation between temperature and the mobility can be expressed as [22]: $\mu_{eff} = \mu_0(T/T_0)^{-2}$, where μ_{eff} is the effective mobility, μ_0 is the mobility at ambient temperature T_0, and T is the lattice temperature.

The increase in temperature causes degradation of the mobility of the carriers, which results in an increase in I_{OFF}. The effects of temperature on electron and hole mobility at V_{GS} = 0 V are shown in Fig. 9(b) and (c). As shown in Fig. 9(a), I_{OFF} increases for a wide range of temperatures. But the increase in I_{OFF} for a wide range of temperature is not severe. Thus, the proposed device can be used for a wide range of temperatures and feasible for circuit applications.

4.9. Effect of back-gate voltage (V_{GB}) on transfer characteristics for different BOX heights

The effect of back-gate voltage (V_{GB}) on transfer characteristics for different BOX heights is shown in Fig. 10(a) and (b). Figure 10(a) shows that with the decrease in V_{GB}, subthreshold drain current decreases. This can be explained as due to V_{GB}, the total potential drop on the gate decreases with the decrease in V_{GB} at same V_{GS}. That is why, the subthreshold drain current decreases with the decrease in V_{GB} at same V_{GS}. The better transfer characteristics are found when the BOX height is changed to higher value which is shown in Fig. 10(b). It is observed that the leakage current is reduced by four orders of magnitude for a positive V_{GB}. As the height of the BOX is increased, the influence of control of back gate increases at positive V_{GB} and thus the less leakage current (I_{OFF}) is found for a BOX having height of 20 nm compared with 5 nm at V_{GB} = 2 V.

4.10. Effect of fin thickness on threshold voltage

The effect of fin thickness on threshold voltage is shown in Fig. 11(a). With the increase in fin thickness, the influence of control of side two gates on the midpoint of the channel decreases [12]. As a result, the subthreshold drain current decreases as we increase the fin thickness. That is, the wider fin requires more gate voltage to cause inversion in the channel. That is why, threshold voltage increases with the increase in fin thickness. The relation of threshold voltage value with fin thickness can also be explained with the help of the electrostatic potential curve by keeping the V_{GS} = 0.7 V called mid-gate voltage, at different fin thicknesses [Fig. 11(b)]. As the gate losses the control over the channel for wider fin thickness, the potential curve decreases with the increase in fin thickness.

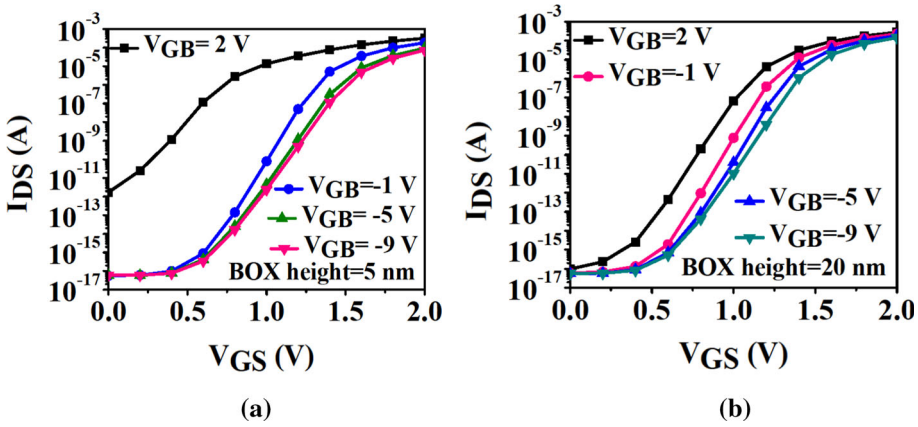


Fig. 10 Effect of V_{GB} on transfer characteristics for BOX height (**a**) 5 nm and (**b**) 20 nm

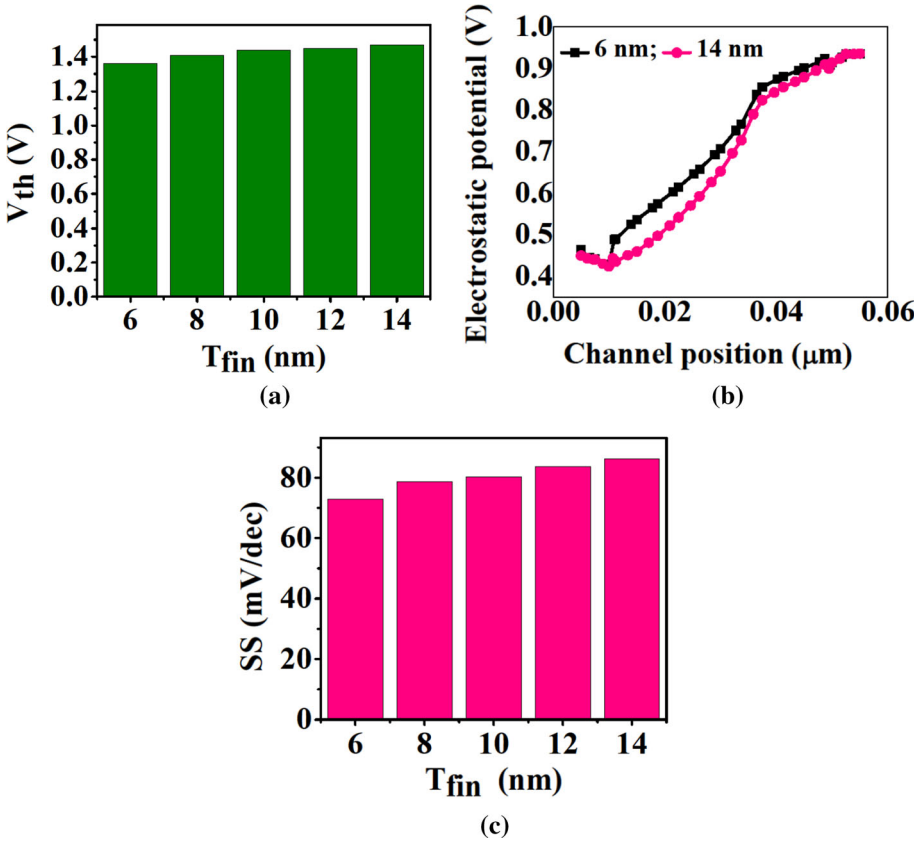


Fig. 11 (**a**) Effect of fin thickness on threshold voltage, (**b**) electrostatic potential curve versus channel position for different fin thickness at V_{GS} = 0.7 V and (**c**) effect of fin thickness on subthreshold swing. H_{fin} = 10 nm, t_{ox} = 2 nm and V_{DS} = 0.5 V

4.11. Effect of fin thickness on subthreshold swing

The subthreshold swing (SS) versus fin thickness is plotted in Fig. 11(c). It is observed that with the increase in fin thickness, SS increases. It can be explained that as we increase the fin thickness, the subthreshold drain current decreases as the gate control over the channel reduces and SS is inversely proportional to the drain current. Therefore, it can be concluded that the SS increases with the increase in fin thickness.

4.12. Implementation of the low-power digital inverter circuit using the proposed FinFET

A complementary FinFET inverter circuit is implemented using both proposed pFinFET and nFinFET, as shown in Fig. 12(a). The transient characteristics of the inverter circuit at V_{DD} = 2 V and load capacitance (C_L) 7 × 10^{-16} F are shown in Fig. 12(b). Figure 12(b) shows that there is no overshoot and undershoot is present in the characteristics. To understand the effect of C_L on transient characteristics, C_L is varied from higher value to lower value, as shown in Fig. 12(c). It is distinguished from

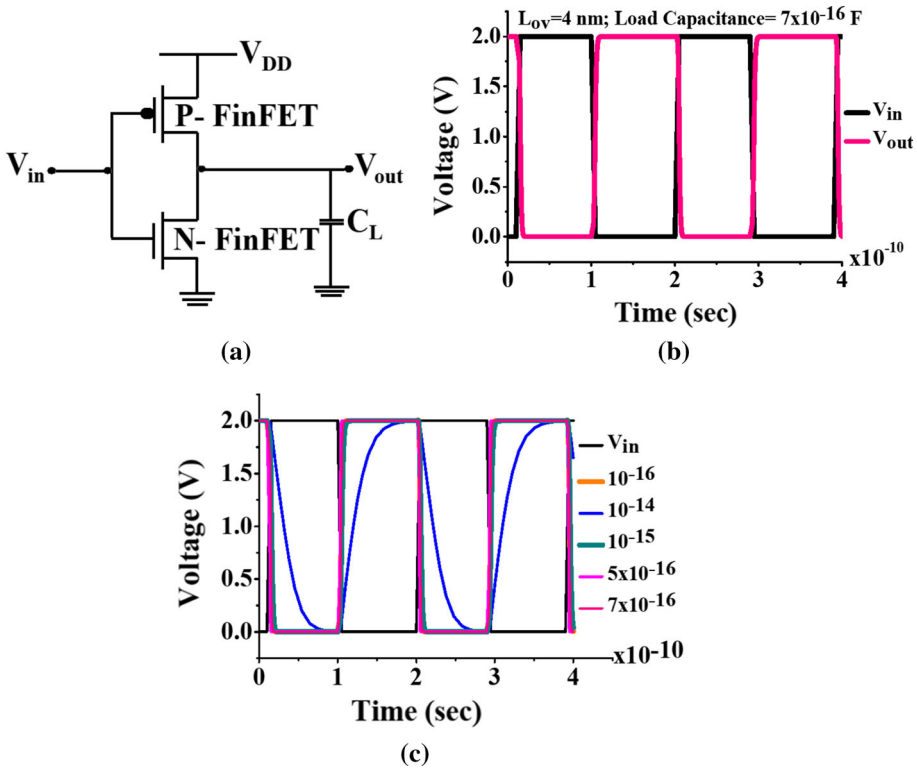


Fig. 12 (**a**) Inverter circuit of the proposed device, C_L defines the load capacitance, (**b**) transient characteristics of the inverter circuit for V_{DD} = 2 V and (**c**) effect of load capacitance on transient characteristics of the proposed device-based inverter circuit

Fig. 12(c) that in case of high C_L, 10^{-14} F, circuit takes more time for charging and discharging. Also, it is observed that as we increase the load capacitance, the propagation delay also increases.

5. Conclusion

The investigations carried out in this study demonstrate that the proposed dual-material-gate dual-stacked-gate dielectrics gate–source overlap Ge FinFET reduces the leakage current (I_{OFF}) by six orders of magnitude and the ratio of on current to off current (I_{ON}/I_{OFF}) increases by six orders of magnitude compared with conventional FinFET. By further analyzing the device, it reveals that the thinner fin exhibits better characteristics than the wider fin. Moreover, the use of high k dielectric with low k dielectric in stack shows magnificent results compared with other gate dielectrics in stack. However, the proposed device in this work is used as a potential device in low-power digital application, inverter. The absence of overshoot and undershoot in the transient characteristics makes the proposed device useful for other digital circuit applications such as logic gates.

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