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Radio System Design And RF/Microwave Measurement Techniques

TTT4201

Semester Project - Power Amplifier

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Summary

A class AB power amplifier is designed and simulated in ADS. It is designed to be unconditionally stable, have a small signal gain of 18.6 dB, and a power added efficiency of 55% (Output power 40 dBm) at 2.4 GHz. at 2.4 GHz, the small signal gain is measured to be 13.4 dB, and the power added efficiency is equal to 44.1% . Measured at 2.3 GHz the small signal gain is measured to 17.1 dB while the power added efficiency is equal to 55%. Inconsistencies in the microstrip substrate may be the reason for the amplifiers poor performance at 2.4GHz.

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1 Introduction

1.1 Power Amplifiers - A Brief Introduction

Power amplifiers (PA) are amplifiers designed to increase the power of a signal, typically found in the later stages of a radio system. In cellphones, their output may be in the order of 500mW. For larger systems, the output can reach as high as 100W. PA's can be designed to have different characteristics, depending on the users specifications. A high gain is often desired, but a trade-off may be made in order to make the amplifier more efficient. In a handheld device like a cellphone, most of the DC-power is dissipated in the PA. In this scenario, an efficient amplifier is desired in order to conserve energy. Several measures are used in order to characterize an amplifier. Metrics such as power-added efficiency (η_{PAE}) tells how efficient a transistor is. The amplifiers 1dB compression point (P1dB) gives us a range of input powers in which the amplifier operates as a linear device. Finally, a small signal analysis may be performed to deduce the amplifiers gain.

1.2 Design Specifications

For this amplifier design, several specifications should be satisfied:

1.2.1 Small signal Specifications

- The device must be unconditionally stable.
- The small-signal bandwidth should be at least 100MHz within 1 dB.
- A gain of at least 14dB should be attained through the bandwidth (2.35GHz to 2.45GHz).

1.2.2 Large signal Specifications

- An output power P_{out} of at least 40dBm should be produced with a single-tone input power P_{in} of 28dBm.
- The power added efficiency η_{PAE} should be as high as possible with a single tone input of 27dBm.
- For a two-tone peak output power of 38dBm, the intermodulation distortion should be as little as possible.

1.2.3 Design Restrictions

- The frequency of operation (f_c) is 2.4GHz,
- The device must be biased with a drain voltage V_D of 28V.
- The drain current should be no less than 50 mA.

2 Theory

2.1 Transistor technology

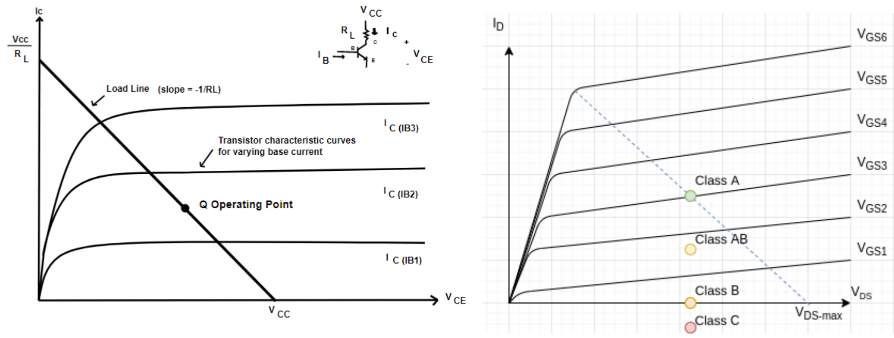
Several different transistor technologies exist. Two of the most known are Metal-Oxide-semiconductor Field Effect Transistors (MOSFET) and Bipolar junction transistors (BJT). *High electron mobility transistor* (HEMT) is another type of transistor technology, and can also be known as heterostructure field effect transistor (HFET). A *heterostructure* FET have a junction between two materials with different band gaps as the channel, instead of a single doped channel like a MOSFET[1]. Different semiconductor types used in a HEMT yield different desired effects. Indium gives a better high-frequency performance while *gallium nitride* (GaN) gives a *high-power* performance.

The transistor that is used in this power-amplifier design is the Wolfspeed CG2H40010 [2]. The Wolfspeed CG2H40010 is a powerful and unmatched GaN HEMT transistor which can deliver more than 10 W. Since it is a GaN transistor, it is a good choice of transistor technology for power amplifiers.

2.2 Bias point and amplifier class

Biasing a transistor is important as it decides the characteristics of the amplifier, as well as its *class*. To bias a transistor means to select an *operating point*; a specific voltage applied to the gate of the transistor (or in the case of a BJT, a current applied to the base), corresponding to a certain drain current through the transistor. This point may be plotted as a discrete point in a transistors *I-V curve*, illustrated in figure 1(a).

This point may be moved around such that certain characteristics are attained: in a low noise amplifier, the operating point is set such that the least amount of noise is introduced to the amplified signal. The operating point may be chosen such that a small input signal yields the largest output signal, producing more gain. In the case of a PA, the operating point is usually chosen based on whether efficiency or linearity is desired, giving rise to the different *amplifier classes*. These are illustrated in figure 1(b).



(a) I-V characteristic of a BJT. collected from [3]

(b) Different PA classes.

Figure 1

In figure 1(b), the load line is drawn as a dashed blue line from the ’knee’ of the I-V curve, down to the x-axis corresponding to the voltage across the transistor.

- The operating point of the class A amplifier is placed in the middle of the load line, such that $I_D = \frac{I_{max}}{2}$. This corresponds to a conduction angle of 360 degrees, or 2π. Class A amplifiers have the most *linearity* of the amplifier classes. However, Class A amplifiers are not very efficient, with a maximum theoretical efficiency of 50%. Since they also conduct current with no signal applied, they dissipate a lot of power and produce heat.
- The class B amplifier is biased such that only half of the signal is amplified, corresponding to a conduction angle of π. The theoretical efficiency of the class B amplifier is 78.5%. Class B amplifiers are less linear than class A amplifiers. A class AB-amplifier is the middle ground between a class A and class B amplifier. It is more linear than a class B amplifier, and more efficient than a class A amplifier. They have a conduction angle between 2π and π. The operating point for a class AB amplifier is chosen such that $0 < I_D < \frac{I_{max}}{2}$.
- A class C amplifier is biased such that the operating point lies in the cut-off region. This means that the amplifier conducts current for less than half of the signal period, corresponding to a conduction angle smaller than π. This leads to a lot of distortion, and this class of amplifier is not very linear. It is however very efficient.

2.3 Power, efficiency and linearity

A great measure of efficiency in an amplifier is the Power-added efficiency (PAE) metric, as this also accounts for the RF-power at the input. This is defined as (1)

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \tag{1}$$

This formula yields the efficiency of the amplifier.

To evaluate the linearity of a device, a two-tone test is carried out. In a two-tone test, two sine signals are applied to the input of the device. The power is then gradually increased, until intermodulation distortion occurs. The output of the DUT[1] is then monitored with a spectrum analyzer. As the power is increased, the magnitude of the intermodulated products also increase. The third order intermodulation products (IMD3) grow at a rate of 3dB for each dB increase of input power, and will eventually significantly distort the output. As a measure of linearity, the magnitude of the IMD3-products may be measured for a given power. Another metric is the 1dB compression point of the amplifier. This occurs when the output deviates by 1dB from the ideal response of the amplifier. This is shown in figure 2.

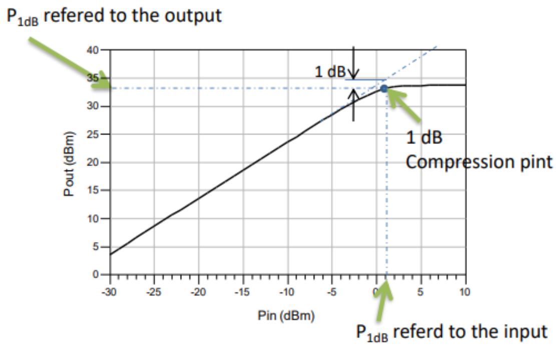


Figure 2: 1dB compression point. Taken from [7]

2.4 Microstrip

As for transistor technology, there are different variants of transmission lines; coax, striplines and microstrips. A key parameter of transmission lines is its *electrical size/length*, where the phase and magnitude will change by the length of the line. Microstrip is a type of transmission line where the conductor is separated from a ground plane by a substrate of dielectric material. There are both positive and negative sides to microstrip lines compared to traditional waveguide technology. They are less expensive to manufacture, lighter and use a smaller area. The disadvantages are the poor power handling, high losses and more susceptible to cross-talk and unintentional radiation due to microstrip lines not being enclosed. Microstrips can be utilized in different ways to implement desired effects in matching and can be used to replace passive components like capacitors and inductors.

2.5 Impedance Matching

Impedance matching a load is important, as a properly matched load will ensure that the largest amount of power is delivered to it, while reducing reflections in the system. To impedance match means to design a *matching network* for a load Z_L such that when looking into the matching network (and load), the generator sees the characteristic impedance Z_0(Typically the impedance of the transmission lines used). As long as the load has a positive

[1]Device Under Test

real component, then any impedance can be matched. This impedance may be plotted as a point in a Smith chart, as illustrated in figure 3.

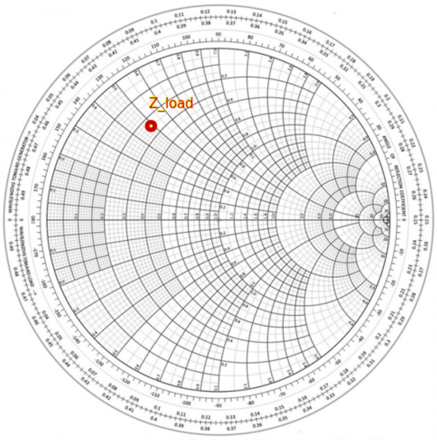
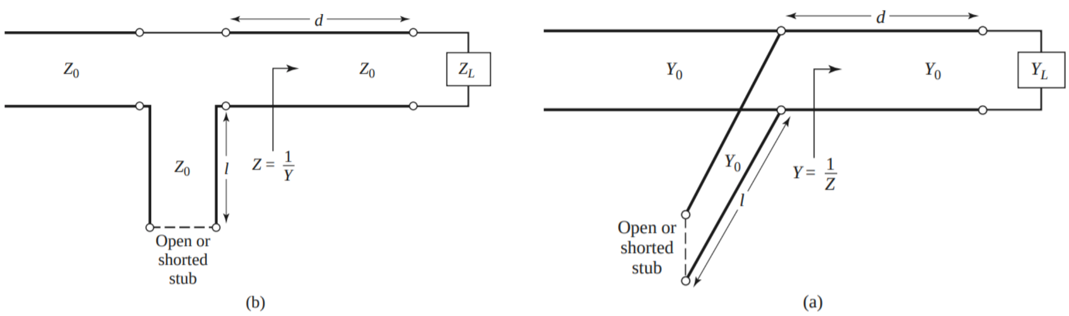


Figure 3: A load impedance plotted in a smith chart.

It is usually desired to match the load to the characteristic impedance, i.e. the center of the smith chart. However, one may want to match for other points in this chart, in order to ensure stability, maximum gain, or the least amount of noise. Matching can be done in several ways. Lumped components may be used, or one may use transmission lines. In this design, microstrip lines are used in a method called single stub tuning. Any desired reactance may be realised by using an open or shorted length of transmission line ([5], chapter 5.2, page 234). This is desirable when designing a matching network with microstrip lines, as an open-circuit length of line may easily be printed onto the PCB. In single stub tuning, a length of transmission line will move the load in a circle of constant radius in the smith chart. The length of this line will be such that the $R = 1$ or the $G = 1$ circle is intersected, and the appropriate reactance is added either in series or in parallel such that the load is matched. This is shown in figure 4.



(a) A series-stub. (b) A parallel stub.

Figure 4: Single stub tuning. Figures are collected from [5], chapter 5.2, page 235.

2.6 Stability

Stability is an important term when it comes to amplifier design. An unstable amplifier may *oscillate* due to feedback from the output, which may combine with existing reflections on the input. This corresponds to $|\Gamma_{in}| > 1$ and $|\Gamma_{out}| > 1$. A device may be *unconditionally stable*, which means it will not oscillate for any source or load impedance. A *conditionally stable* device will only be stable for certain source and/or load impedances. These regions of stability may be plotted in a smith-chart as stability circles, shown in figure 5.

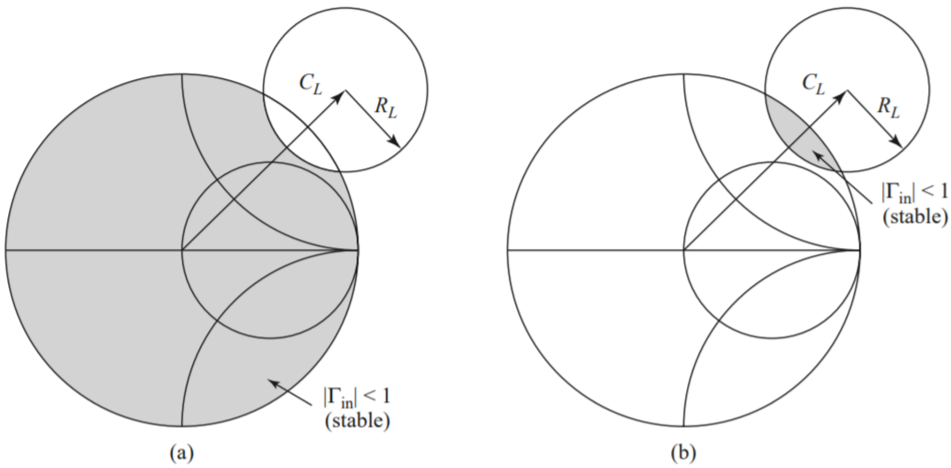


FIGURE 12.5 Output stability circles for a conditionally stable device. (a) $|S_{11}| < 1$. (b) $|S_{11}| > 1$.

Figure 5: Stability circles. From [5], chapter 12, page 566.

A metric of stability is the μ-factor, defined in (2)

$$\mu = \frac{1 - |S_{11}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} \tag{2}$$

μ tells the distance from the center of the Smith chart to the nearest output load stability circle. if $\mu > 1$, then the device is unconditionally stable. A larger μ will also imply more stability ([5], chapter 12, page 567). Another metric is μ_{prime}. It is defined in equation (3).

$$\mu_{prime} = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} \tag{3}$$

It is quite similar to μ, but yields the distance to the input stability circle instead. There are several ways to stabilize a device, and they usually involve introducing some sort of loss at the input or output. Resistive loading introduces loss for all frequencies, but is not desirable to have at the output of a power amplifier. Instead, one may use a combination of lumped components to achieve a more frequency selective introduction of loss. These circuits are shown in figure 6.

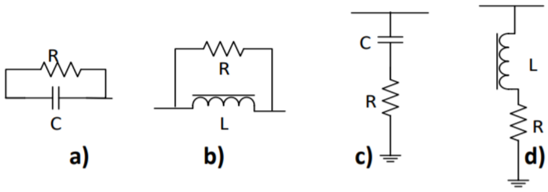
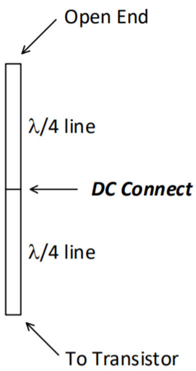


Figure 6: Stabilization circuits. Collected from [4].

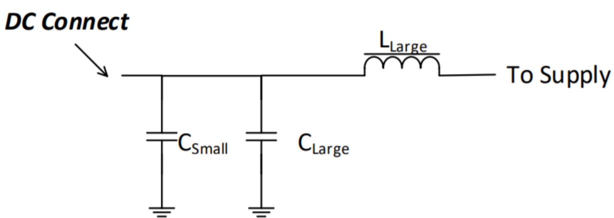
in figure 6, circuit a) will introduce loss for frequencies $f < \frac{1}{RC}$. b) introduces loss for $f > \frac{1}{R}$. c) has loss for $f > \frac{1}{RC}$, and d) has loss for $f < \frac{1}{RC}$.

2.7 DC-feed & DC-block

An ideal DC-feed will provide a clean source of DC current, while stopping all RF from entering it. It must present a low DC-resistance, and a high RF-impedance at the desired frequency. In order to ensure that no RF leaks into the DC-feed, two quarter-wave transmission lines may be used, shown in figure 12 (a). A quarter wavelength line will convert an open circuit to a short circuit, and vice versa; the open circuit end is transformed to a short circuit, in which the DC-supply is connected. Another quarter wavelength line will transform it to an open circuit, presenting an (almost) infinite impedance to the transistor. This won't be the case for all frequencies, but it should be designed around the center frequency as this will be the most prominent RF-frequency in the system. figure 12 (b) illustrates a DC-bias network. The shunt capacitors are decoupling capacitors, which lead RF away from the rest of the network.



(a) Two quarter wavelength lines.



(b) A DC-bias network.

Figure 7: Figures are collected from [4].

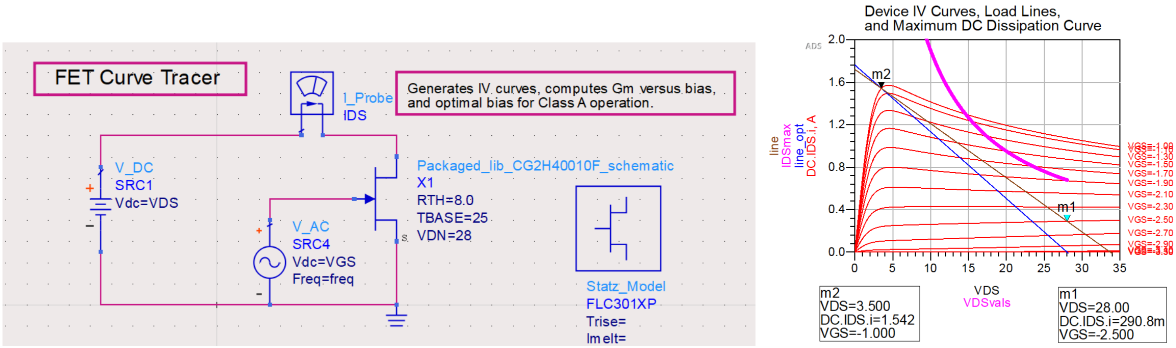
To prevent DC from passing through the amplifier, capacitors are used in order to block undesired flow of DC current while adding minimum interference to signals of radio frequency. This is the working principle of a DC-block.

3 Design and Optimizations

Advanced Design Systems (ADS) is an electronic design automation software system made by Pathwave. The software is a powerful way to design and simulate circuits.

3.1 Choosing an operation point

For this design, the class is decided to be that of an AB-amplifier. A simulation of the transistor is done in ADS, by including the 'designkit' of the transistor into a predefined designguide. This is shown in figure 8(a). Upon simulation, the designguide generates IV curves for the transistor, which is used to select the appropriate operation point.



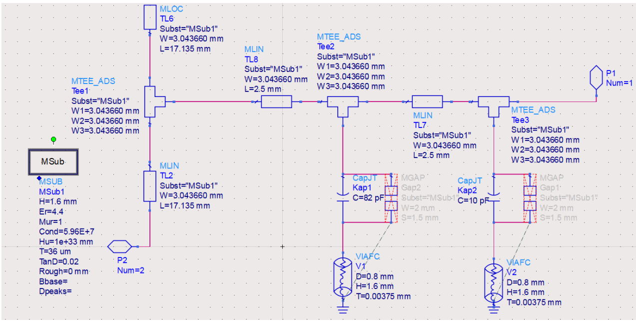
(a) (b)

Figure 8: Figures are collected from [4]

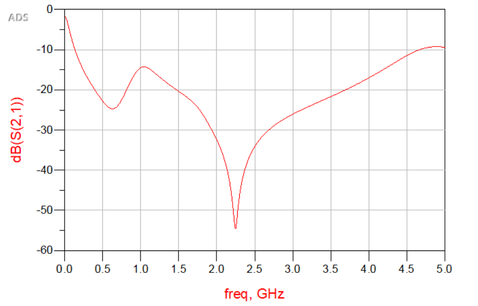
The datasheet of the transistor[2] states that the maximum current it can handle is 1.5A, and the marker m2 is placed on the corresponding 'knee' in the IV-curves, shown in figure 8(b). To bias this amplifier as an AB-amplifier, the operation point is decided such that $V_{GS} = -2.5V$. This corresponds to a drain current of $I_{DS} = 290.8mA$. This point is shown as 'm1' in figure 8(b).

3.2 Designing a DC-feed

To implement the quarter-wave lines in the DC-feed, a tool in ADS called LineCalc is used. This tool will output microstrip lengths and widths, when inputting the desired electrical length and characteristic impedance. The tool also works the other way around. At 2.4GHz, the lines are calculated to be about 3.046mm wide, and 17.135mm long. The design and substrate parameters are shown in figure 9(a). A S-parameter simulation of this circuit shows that the transmission coefficient, S_{21} is greatly suppressed around 2.4GHz, while DC is not attenuated much. This is shown in figure 9(b). A 10pF and a 82pF capacitor is used as decoupling capacitors, and via-holes ensure connection to the ground plane. In the DC feed for the transistor bias, a resistor is also included for improved stability. The added impedance will have almost no contribution to a reduction in small signal gain since the transistor sees the DC feed as an infinite impedance.



(a) DC-feed design.



(b) S-parameter simulation of the DC feed.

Figure 9

3.3 Matching network

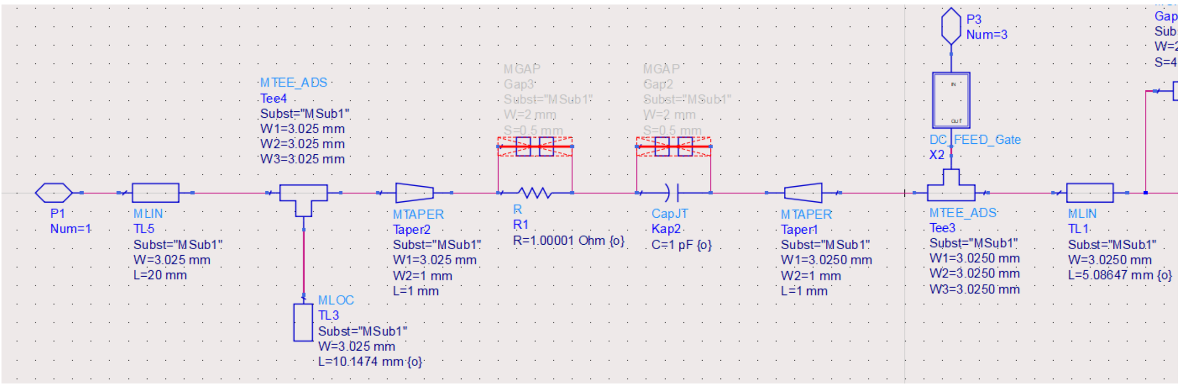


Figure 10: The input network.

The input matching network shown in figure 10 has 4 important components: the microstrip lines TL1 and TL3, the capacitor Kap2 and the resistor R1. The lines are set up as a shunt stub, producing an ideal matching reactance. The resistor aid in stabilizing the amplifier. The capacitor is used as a DC-block. The value of these components are simultaneously optimized for gain and stability, in such a way that the transmission coefficient S_{21} is forced as high as possible, while μ and μ_{prime} are kept above 1. This is shown in figure 12(a).

The output matching network is shown in figure 11. The transmission lines TL2 and TL4 are here optimized such that an output power of at least 40dBm is attained, while simultaneously trying to increase the PAE. This is shown in figure 12(b).

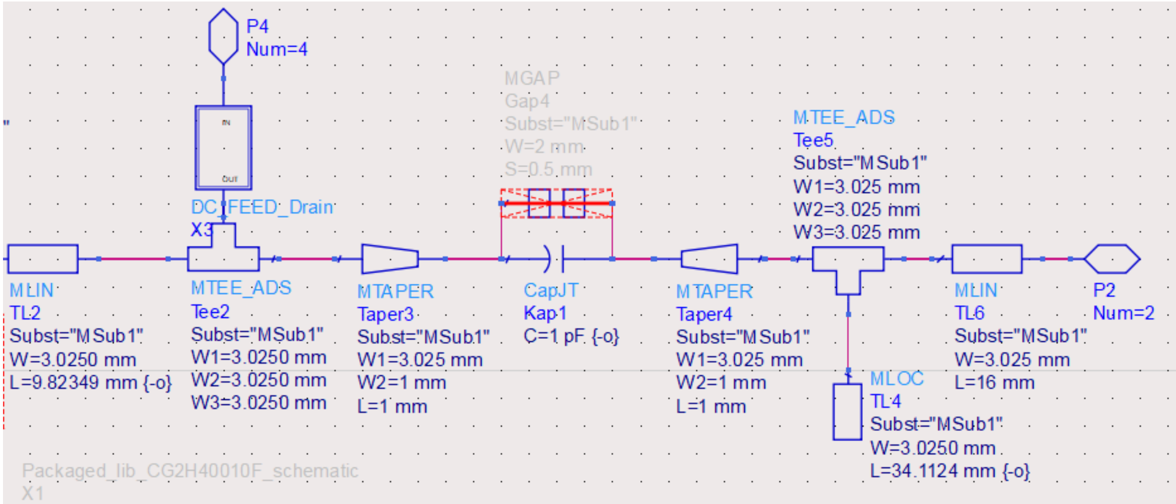


Figure 11: The output network.

(a) Optimizing input for gain and stability. (b) Optimizing output for gain and efficiency.

Figure 12: Optimizations done in ADS.

3.4 Designing a layout

When the optimization is deemed satisfactory, the layout for the PCB can be finalized, adding soldering masks for the RF-connectors and connection points for the bias, supply, and ground. This is shown in figure 13. Microstrip tapers are used where components are soldered to the PCB.

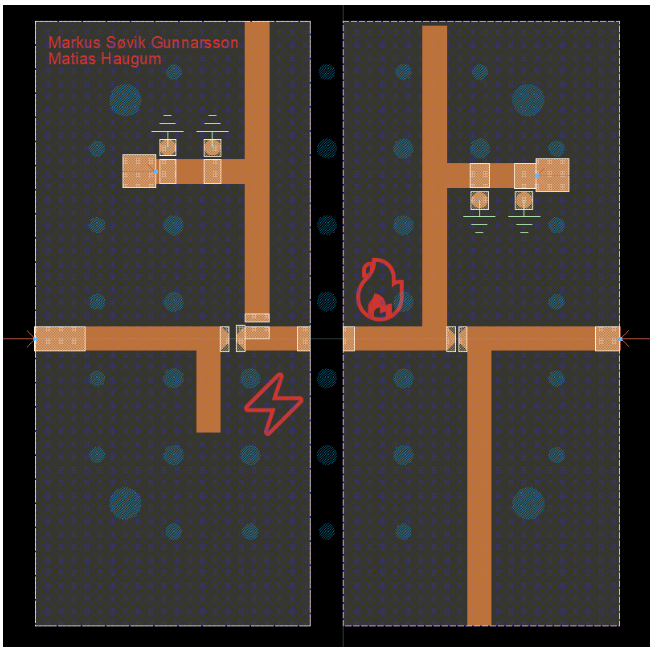


Figure 13: PCB-layout.

Figure 13 shows that the amplifier circuit is divided into two PCBs. The transistor is mechanically mounted between the two PCBs and into the heat sink underneath. This makes it easier to add and remove the transistor without damaging it. Holes for screws are also drilled in the PCB. These screws ensure a good structural, thermal and electrical connection with the heat sink and the PCB.

The values used in the input design are listed in table 1. The output network values are listed in table 2. All microstrip lines have a width of 3.025mm. At 2.4GHz, this is equivalent to a characteristic impedance of 50Ω.

Table 1: Component values used in the input network

Component	Value1
TL1	L = 5.08647mm
TL3	L = 10.1474mm
R1	1Ω
Kap2	1pF
DC-resistor	22.6Ω

Table 2: Component values used in the output network

Component	Value1
TL2	L = 9.82349mm
TL4	L = 34.1124mm
Kap1	1pF

4 Testing

4.1 Small Signal Analysis

The desired values from a small signal measurement is the *scattering-parameters*. They yield many of the electrical properties such as return loss, voltage standing wave ratio, reflection coefficient, and the gain of the amplifier. The s-parameters are also used in calculating the stability. Figure 14 is a diagram of the small signal test setup used at the lab.

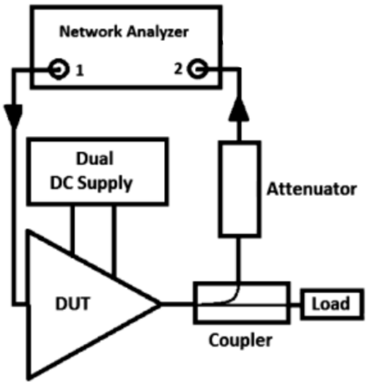


Figure 14: Test equipment for small signal measurement. Figure is taken from [6]

The main component from figure 14 is the *vector network analyzer* (VNA). The network analyzer is able to measure the S-parameters of a device, by sending signals through it from both sides and measuring the reflections and transmitted signals. To protect the VNA from the signals amplified by the DUT in figure 14, a 20dB attenuator is used. Note that this attenuator may influence the signals from the network analyzer. Figure 15 is a picture of the complete test system. In order to protect the amplifier from large currents, it is required to apply the gate voltage before applying the drain voltage.

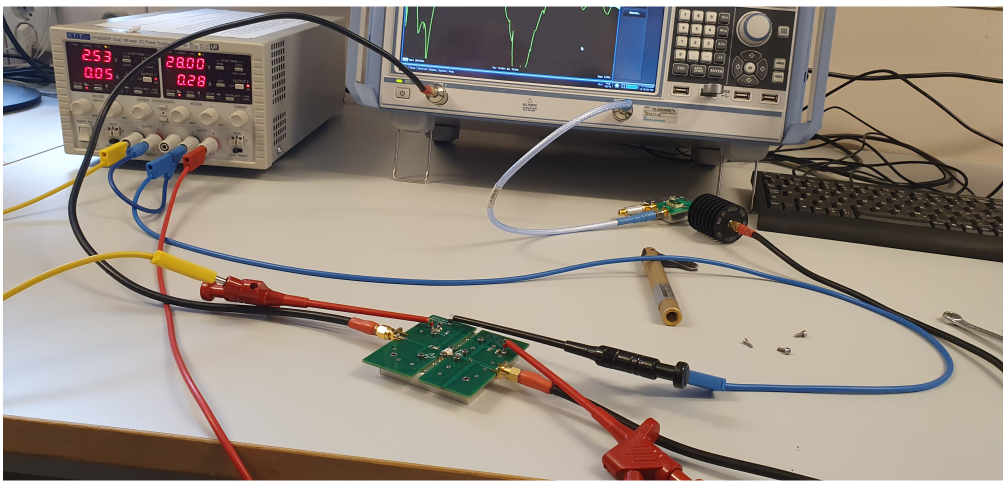


Figure 15: A picture of the complete test setup

4.2 Large Signal Analysis

The goal of the large signal analysis is to measure the power and efficiency of the DUT. Figure 16 is a diagram of the large signal test setup.

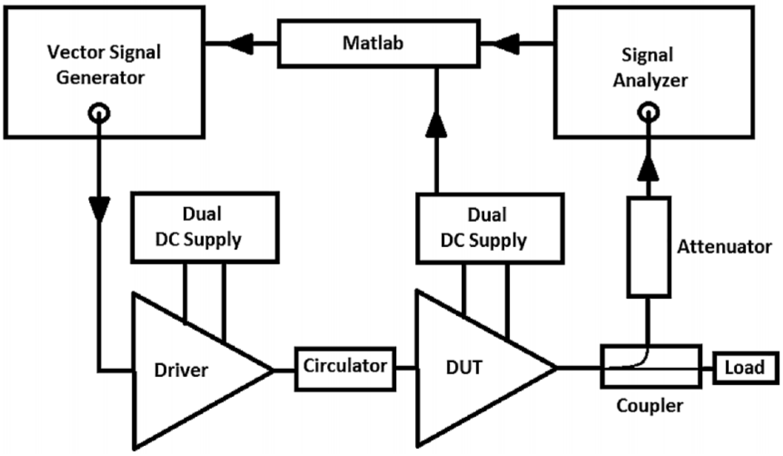


Figure 16: Test equipment for large signal measurement. Figure is taken from [6].

Both test systems, figure 14 and figure 16, use some of the same components (attenuator, coupler, load and DC supplies). In order to test the device with enough power, a driver is placed in the test system. Figure 17 shows two images of a signal generator and a signal analyzer.

(a) Rhode & Schwarz signal generator

(b) Rhode & Schwarz signal analyzer

Figure 17

A Matlab script is used to generate custom waveforms representing either a single tone or a 2-toned signal depending on the test to be performed. This custom waveform is sent into the signal generator in figure 17(a) to synthesize tones for the test. The signal is then transmitted through the driver and the PA before it is displayed in the signal analyzer in figure 17(b). This is where the results from the measurements are gathered. A picture of the whole system is depicted in figure 18.

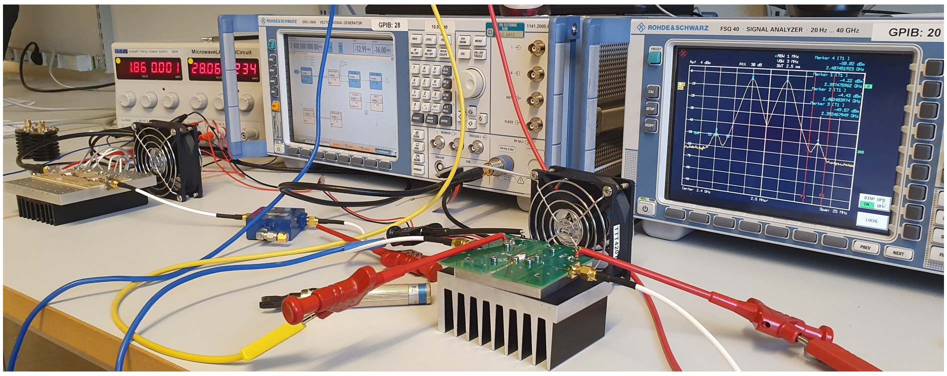
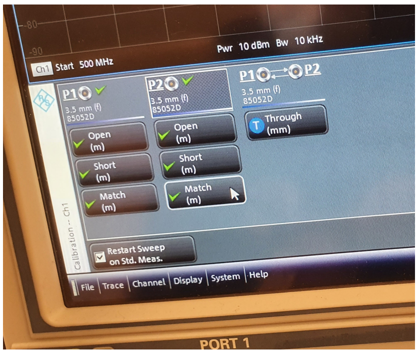


Figure 18: A picture of the complete large signal analysis setup.

4.3 Calibration

Calibrating the VNA is necessary in order to ensure accurate measurements and removing systematic errors. To calibrate, a set of known *calibration values* are used alongside the software of the VNA. For a two-port device it is required to use 4 known calibration values. Figure 19(a) shows a selection of calibration values along with the included torque wrench. Tightening the connectors with appropriate force is necessary for an accurate calibration process. Figure 19(b) depicts the screen of the VNA while these calibration values are connected and the VNA is being calibrated. Calibration is done by pressing the button corresponding to the calibration component which is affixed to the ports of the VNA.

(a) Box with different calibration values and a torque wrench.



(b) The screen of the VNA while calibrated.

Figure 19

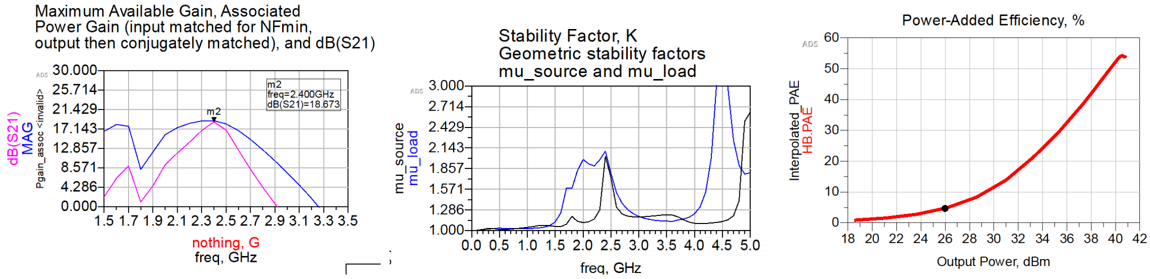
The 4 calibration values from figure 19(a) are called short, open, load and through. These make up the calibration standard called *SOLT*. An observation is that the value for load is called match. The calibration component names often differ between manufacturers of VNAs, yet the essence of the calibration method remains the same.

The large signal test setup was pre-calibrated.

5 Results

5.1 Simulated results

Using design-guides in ADS, the design is simulated for its gain, shown in figure 20(a). Figure 20(b) shows the simulated stability of the amplifier. μ and μ_{prime} are both above 1 for all frequencies, indicating a unconditionally stable device. The power-added efficiency is simulated in figure 20(c). At an output-power of around 40 dBm, an efficiency of around 55% should be expected.



(a) Transmission coefficient and maximum available gain.

(b) μ and μ_{prime}.

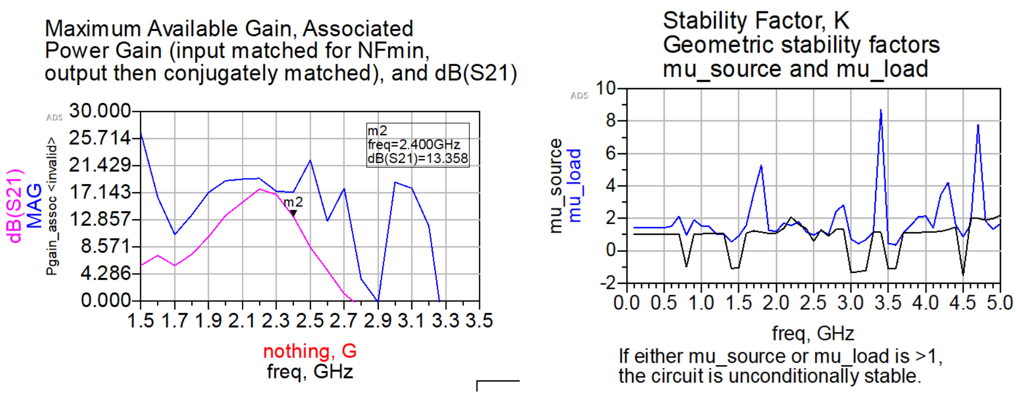
(c) PAE.

Figure 20: Simulated results from ADS.

5.2 Measured results

5.2.1 Small signal analysis

A S-parameter file is generated upon analyzing the device in an VNA. This file may be used in ADS to generate gain and stability plots, shown in figure 21.



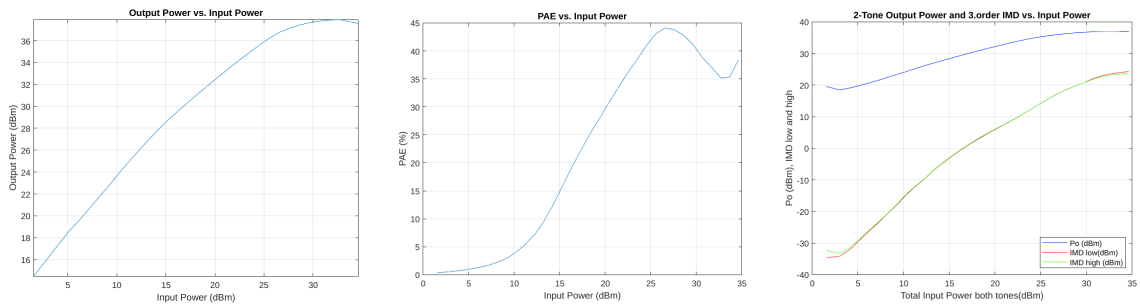
(a) Transmission coefficient

(b) μ and μ_{prime}.

Figure 21: Measured results.

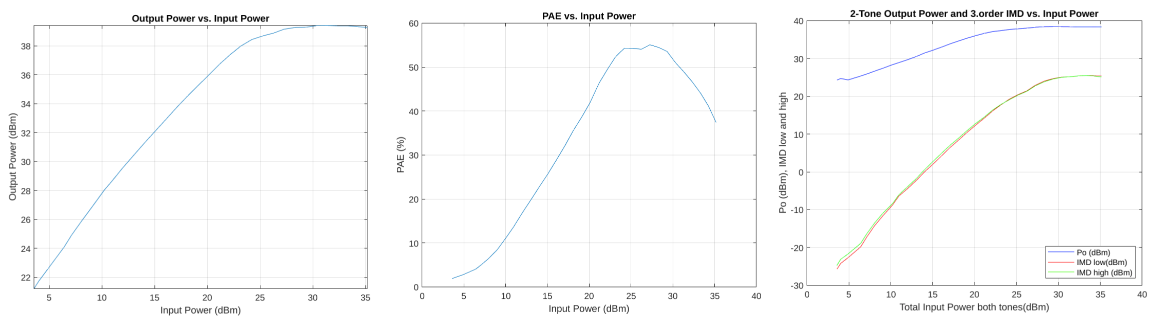
5.2.2 Large signal analysis

The device is tested at two frequencies: 2.4GHz (figure 22) and 2.3GHz (figure 23).



(a) Single tone test. (b) Single tone, PAE. (c) Two tone, third order intermodulation.

Figure 22: Measured results at 2.4GHz.



(a) Single tone test. (b) Single tone, PAE. (c) Two tone, third order intermodulation.

Figure 23: Measured results at 2.3GHz.

The results from figure 22 and 23 are presented in table 3.

Table 3: Results from large signal analysis

Frequency	P_{out} at P_{in} =28dBm	max P_{AE} vs P_{in}(27dBm)	IMD3, dBc
2.4GHz	37.2dBm	44.1%	NA
2.3GHz	39.25dBm	55%	-16.7dBc

6 Discussion and Conclusion

6.1 Discussion

There is a significant left shift of the peak of the transmission coefficient in figure 21(a), compared to the simulation in figure 20(a). Upon testing, the highest gain was found to be around 2.25GHz, instead of the desired 2.4GHz. This left shifting may be attributed to inconsistencies in the substrate, as this left shifting was also prominent in other amplifier designs using the same substrate. At the operation frequency f_c, a small-signal gain of 13.35dB is attained. The bandwidth requirement is not met, as the gain in the 100MHz-range varies from 15.28dB at 2.35GHz to 10.59dB at 2.45GHz. With the shifting in mind, a gain of 18.12dB is realised at 2.25GHz, falling down to 16.8dB at 2.3GHz, which is 0.32dB shy of the bandwidth requirement.

Based on the simulations, the amplifier was assumed stable. However, the presence of low frequency (<1GHz) oscillations was confirmed in the circuit using a spectrum analyzer. Interestingly, the capacitance introduced from the probes of a voltmeter applied to the gate and drain of the transistor was sufficient to stabilize the circuit. To fix the issue, a capacitor in the μF order was added to each DC-feed of the amplifier circuit. Stability measurements from figure 21(b) shows that the amplifier is not unconditionally stable, and oscillations may occur for certain frequencies. At the operation frequency f_c and at $f = 2.3$GHz however, the amplifier is stable.

The large-signal analysis was performed at f_c, but also at 2.3GHz in order to get an idea of how efficient the transistor is at this frequency. Ideally, it would be simulated at 2.25GHz, but 2.3GHz was the lowest available testing frequency. At f_c, an output power of 37.2dBm is measured with an input power of 28dBm, 2.8dB shy of the 40dBm requirement. This rises to 39.25 at 2.3GHz. The power added efficiency is measured to be 44.1% at f_c, and 55% at 2.3GHz. A large signal analysis at 2.25GHz would have been desirable, to see if the power requirements would be met at this frequency.

The peak output power of the IMD3-products is measured to be -16.7dBc at 2.3GHz. It cannot be measured at f_c, due to the insufficient output power at this frequency. Ideally, this number would be smaller. Biasing the amplifier higher in the AB class could improve the linearity, however the potential loss in efficiency must also be considered.

6.2 Conclusion

A class AB power amplifier is designed in ADS. A matching and bias network is presented to the reader, and the amplifier is optimized for stability, gain and efficiency at an operating frequency of 2.4GHz. Upon testing, the performance is worse than simulated, with the amplifier performing best at around 2.25GHz. Inconsistent substrate parameters are assumed to be the source of the deviation. Stability issues are corrected by soldering additional capacitors at the DC-feeds. Poor linearity results points to that the amplifier would benefit from being biased higher in the AB-class.

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