

AND

The screenshot shows the Quartus II IDE with three main windows open:

- HDL Editor:** Contains Verilog code for a 16-bit AND gate. The code defines inputs `a[16]` and `b[16]`, and output `out[16]`. It includes comments for bit numbering and logic assignments.
- Pin Manager:** Shows the configuration for the device `AND1250918`. Inputs `a[16]` and `b[16]` are assigned to pins `-19737` and `-5291` respectively. Output `out[16]` is assigned to pin `-23995`.
- Simulation Waveform:** Displays the timing diagram for the simulation. It shows signals `a`, `b`, and `out` over time. The output `out` is shown as a series of 1s, indicating the result of the AND operation.

XNOR

Hardware Simulator (2.5) - D:\NAND2TETRIS\Ejercicios Arqu\HT2\XNOR1250918.hdl

File View Run Help

Slow Fast

Animate: Program flow Format: Decimal View: Output

Chip Name: XNOR1250918 Time: 0

Input pins		Output pins	
Name	Value	Name	Value
a[16]	-19737	out[16]	-22963
b[16]	-5291		

HDL		Internal pins	
		Name	Value
CHIP XNOR1250918 {	^	SoloA0	0
IN a[16], b[16];		SoloB0	0
OUT out[16];		AB0	0
PARTS:		AABB0	1
		SoloA1	0
//Bit Num. 0		SoloB1	1
Nand(a = a[0], b = a[0], out		AB1	1
Nand(a = b[0], b = b[0], out		AABB1	1
Nand(a = a[0], b = b[0], out		SoloA2	0
Nand(a = SoloA0, b = SoloB0		SoloB2	0
Nand(a = AB0, b = AABB0, out		AB2	0
//Bit Num. 1		AABB2	1
Nand(a = a[1], b = a[1], out	^	SoloA3	1
		SoloB3	1

End of script

XCHANGE

Hardware Simulator (2.5) - D:\NAND2TETRIS\Ejercicios Arqu\HT2\XCHANGE1250918.hdl

File View Run Help

Animate: Program flow Format: Decimal View: Output

Chip Name: XCHANGE1250918 Time: 0

Input pins		Output pins	
Name	Value	Name	Value
a[16]	-19737	out[16]	-17827
b[16]	-5291		

Internal pins	
Name	Value

HDL

```
CHIP XCHANGE1250918 {  
  IN a[16], b[16];  
  OUT out[16];  
  PARTS:  
    // Code here  
    Nand(a = a[8], b = b[8])  
    Nand(a = a[9], b = b[9])  
    Nand(a = a[10], b = b[1])  
    Nand(a = a[11], b = b[1])  
    Nand(a = a[12], b = b[1])  
    Nand(a = a[13], b = b[1])  
    Nand(a = a[14], b = b[1])  
    Nand(a = a[15], b = b[1])  
}
```

a	b	out
1	0	1
1	0	1
1	0	1
0	0	1
0	1	0
1	1	1
1	1	1

End of script