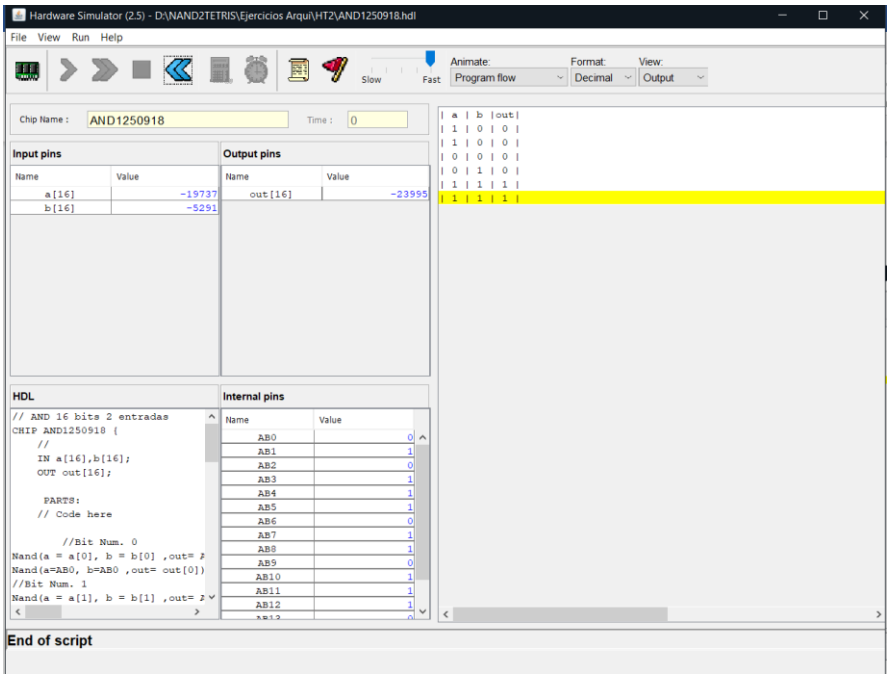
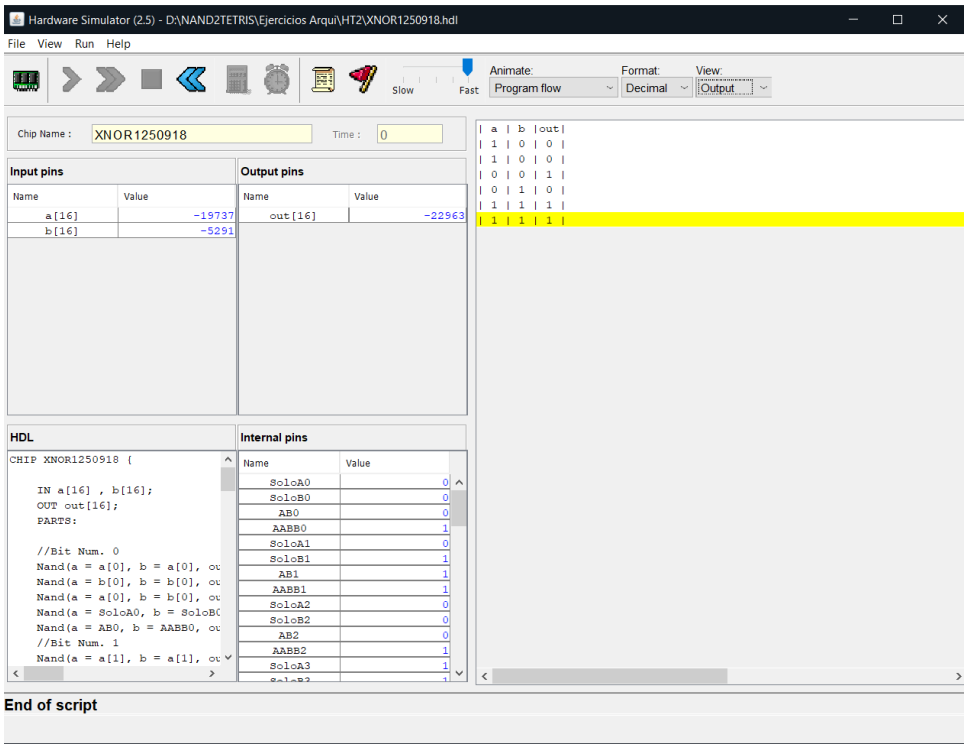
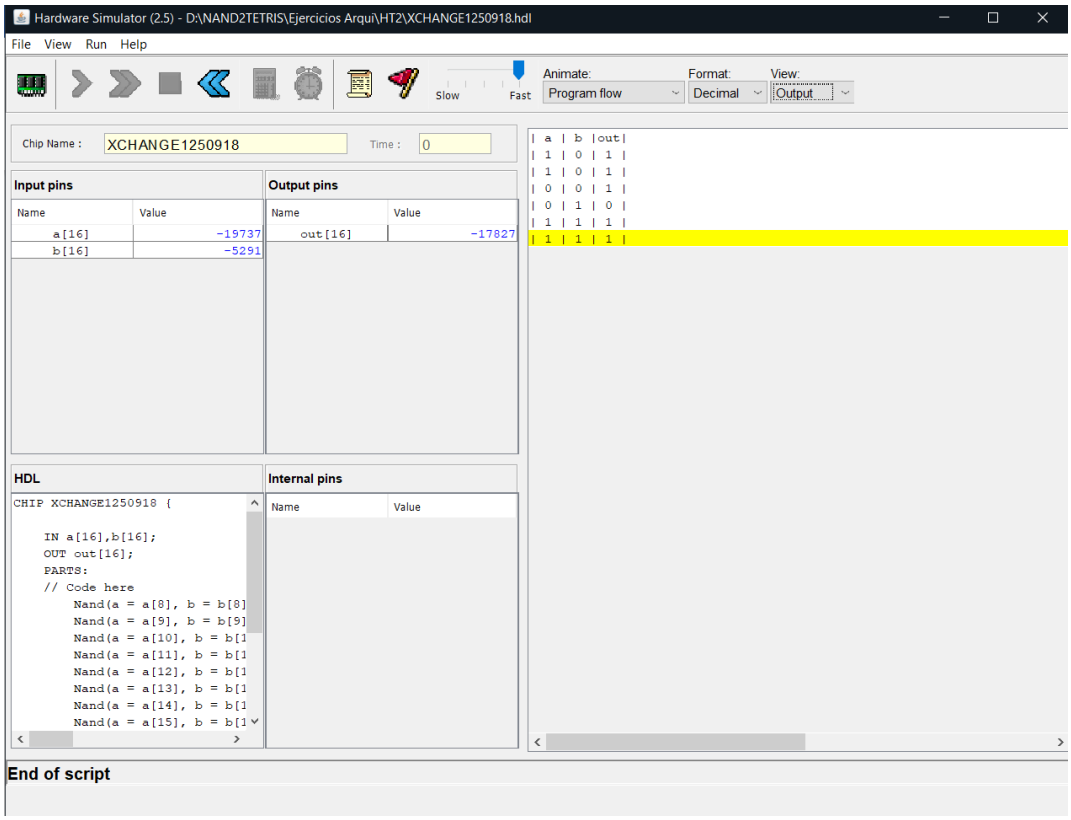
AND


Hardware Simulator (2.5) - D:\NAND2TETRIS\Ejercicios Arqui\HT2\AND1250918.hdl
File View Run Help
Animate: Program flow
Format: Decimal
View: Output
Chip Name : AND1250918
Time : 0
Input pins
Name Value
a[16] -19737
b[16] -5291
Output pins
Name Value
out[16] -23995
a	b	out
1	0	0
1	0	0
0	0	0
0	1	0
1	1	1
1	1	1
HDL
// AND 16 bits 2 entradas
CHIP AND1250918 {
IN a[16],b[16];
OUT out[16];
PARTS:
// Code here
//Bit Num. 0
Internal pins
Name Value
AB0 0
AB1 1
AB2 0
AB3 1
AB4 1
AB5 1
AB6 0
AB7 1
AB8 1
AB9 0
AB10 1
AB11 1
AB12 1
End of script

XNOR


Hardware Simulator (2.5) - D:\NAND2TETRIS\Ejercicios Arqui\HT2\XNOR1250918.hdl
File View Run Help
Animate: Program flow
Format: Decimal
View: Output
Chip Name : XNOR1250918
Time : 0
Input pins
Name Value
a[16] -19737
b[16] -5291
Output pins
Name Value
out[16] -22963
a	b	out
1	0	0
1	0	0
0	0	1
0	1	0
1	1	1
1	1	1
HDL
CHIP XNOR1250918 {
IN a[16] , b[16];
OUT out[16];
PARTS:
//Bit Num. 0
Nand(a = a[0], b = a[0],
Nand(a = b[0], b = b[0],
Nand(a = a[0], b = b[0],
Nand(a = SoloA0, b = SoloB0
Nand(a = AB0, b = AABB0,
//Bit Num. 1
Nand(a = a[1], b = a[1],
Internal pins
Name Value
SoloA0 0
SoloB0 0
AB0 0
AABB0 1
SoloA1 0
SoloB1 1
AB1 1
AABB1 1
SoloA2 0
SoloB2 0
AB2 0
AABB2 1
SoloA3 1
End of script

XCHANGE


Hardware Simulator (2.5) - D:\NAND2TETRIS\Ejercicios Arqui\HT2\XCHANGE1250918.hdl
File View Run Help
Slow
Fast
Animate:
Program flow
Format:
Decimal
View:
Output
Chip Name :
XCHANGE1250918
Time :
0
Input pins
Name
Value
a[16]
-19737
b[16]
-5291
Output pins
Name
Value
out[16]
-17827
a	b	out
1	0	1
1	0	1
0	0	1
0	1	0
1	1	1
1	1	1
HDL
CHIP XCHANGE1250918 {
IN a[16],b[16];
OUT out[16];
PARTS:
// Code here
Nand(a = a[8], b = b[8]
Nand(a = a[9], b = b[9]
Nand(a = a[10], b = b[1
Nand(a = a[11], b = b[1
Nand(a = a[12], b = b[1
Nand(a = a[13], b = b[1
Nand(a = a[14], b = b[1
Nand(a = a[15], b = b[1
Internal pins
Name
Value
End of script