Lab assigment 03 - Vivado

Prep. task - Table with connection of slide switches for LEDs on Nexys A7 board

LED	Connection	Switch	Connection
LED0	H17	SW0	J15
LED1	K15	SW1	L16
LED2	J13	SW2	M13
LED3	N14	SW3	R15
LED4	R18	SW4	R17
LED5	V17	SW5	T18
LED6	U17	SW6	U18
LED7	U16	SW7	R13
LED8	V16	SW8	T8
LED9	T15	SW9	U8
LED10	U14	SW10	R16
LED11	T16	SW11	T13
LED12	V15	SW12	H6
LED13	V14	SW13	U12
LED14	V12	SW14	U11
LED15	V11	SW15	V10

Multiplexer - 2-bit wide 4-to-1 mux

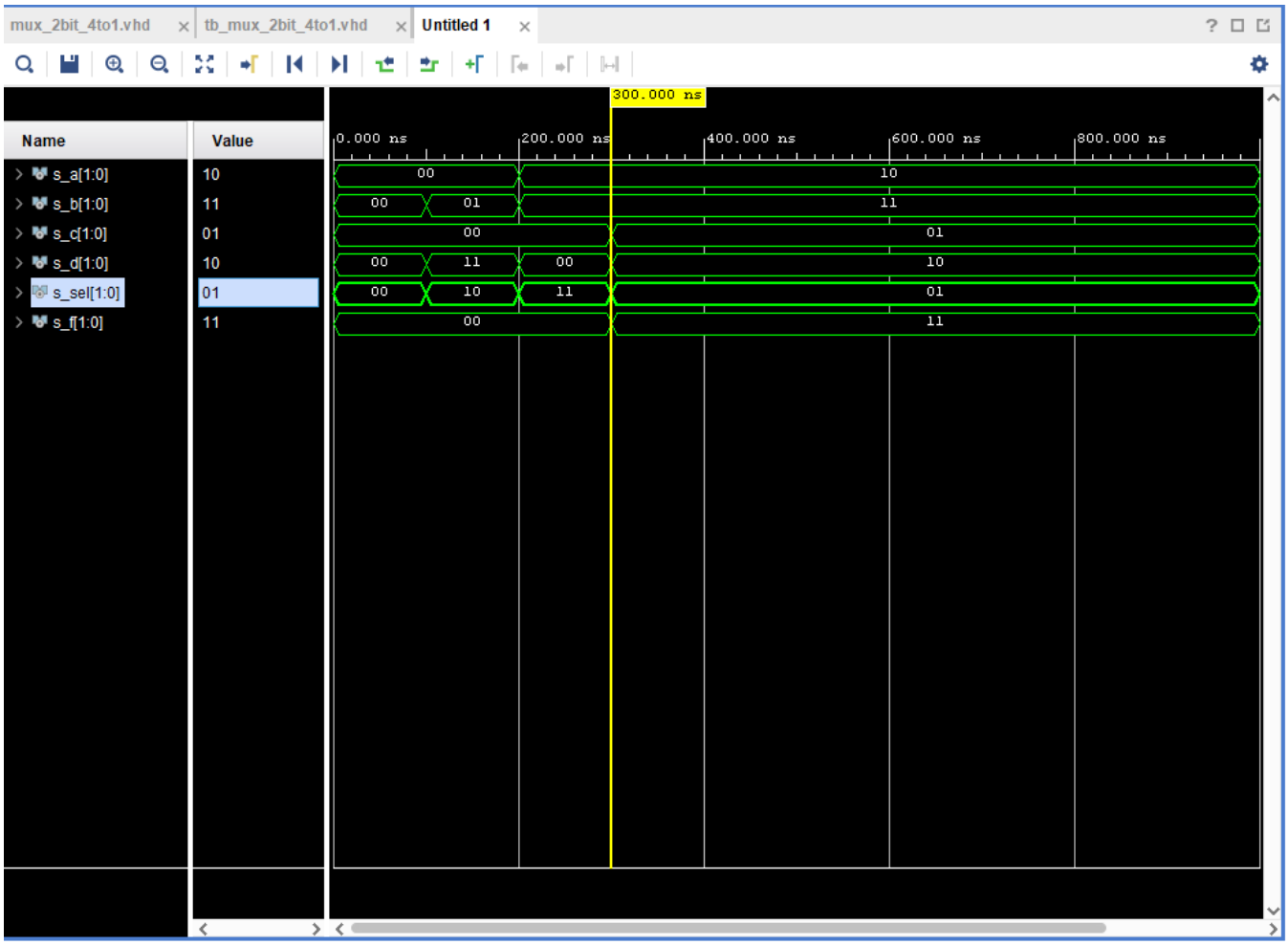
Listing of VHDL architecture from source file `mux_2bit_4to1.vhd` with syntax highlighting

```
architecture Behavioral of mux_2bit_4to1 is

begin

    f_O <= a_i when (sel_i ="00") else
           b_i when (sel_i ="01") else
           c_i when (sel_i ="10") else
           d_i when (sel_i ="11");

end Behavioral;
```

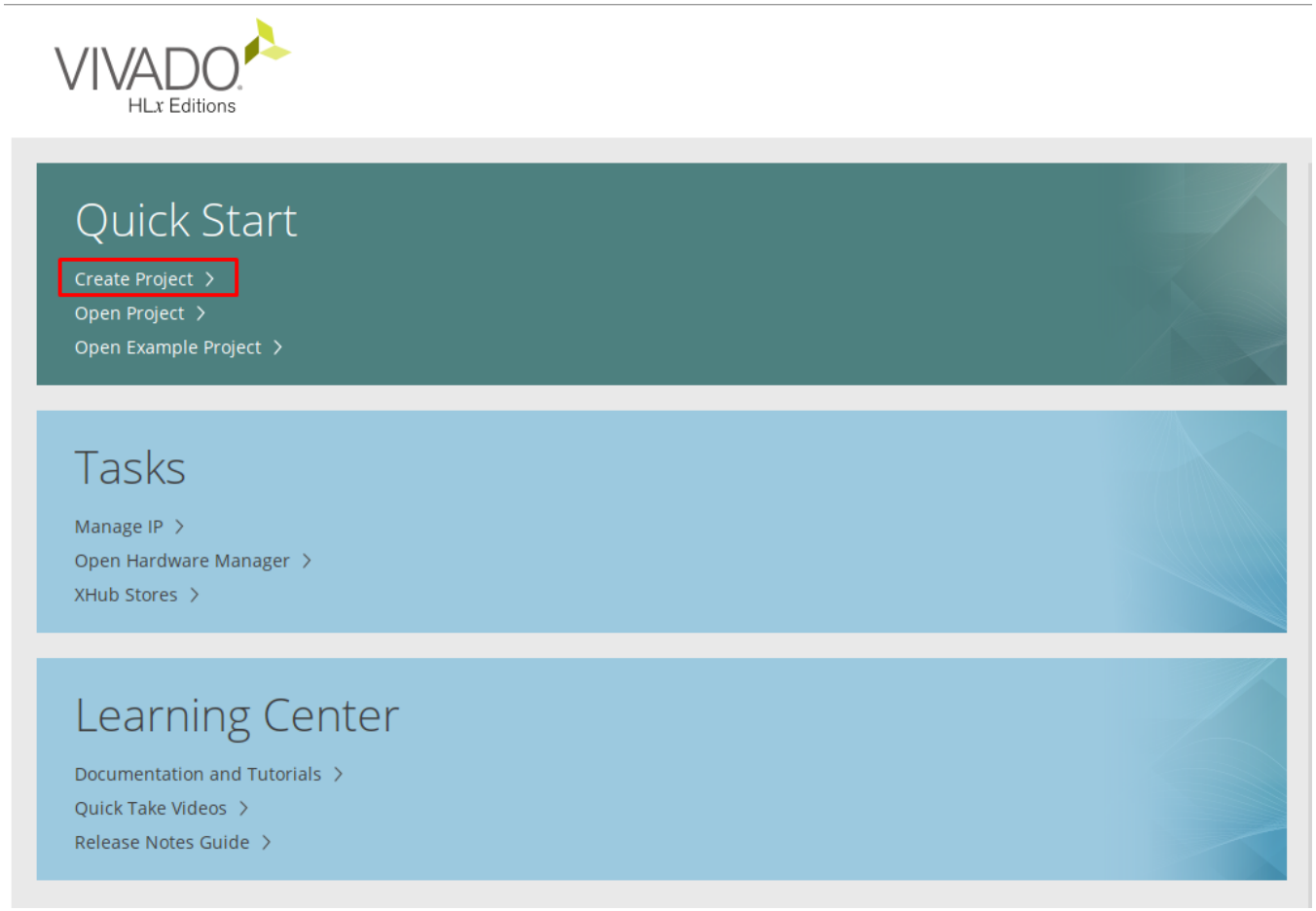
Listing of VHDL stimulus process from testbench file `tb_mux_2bit_4to1.vhd` with syntax highlighting

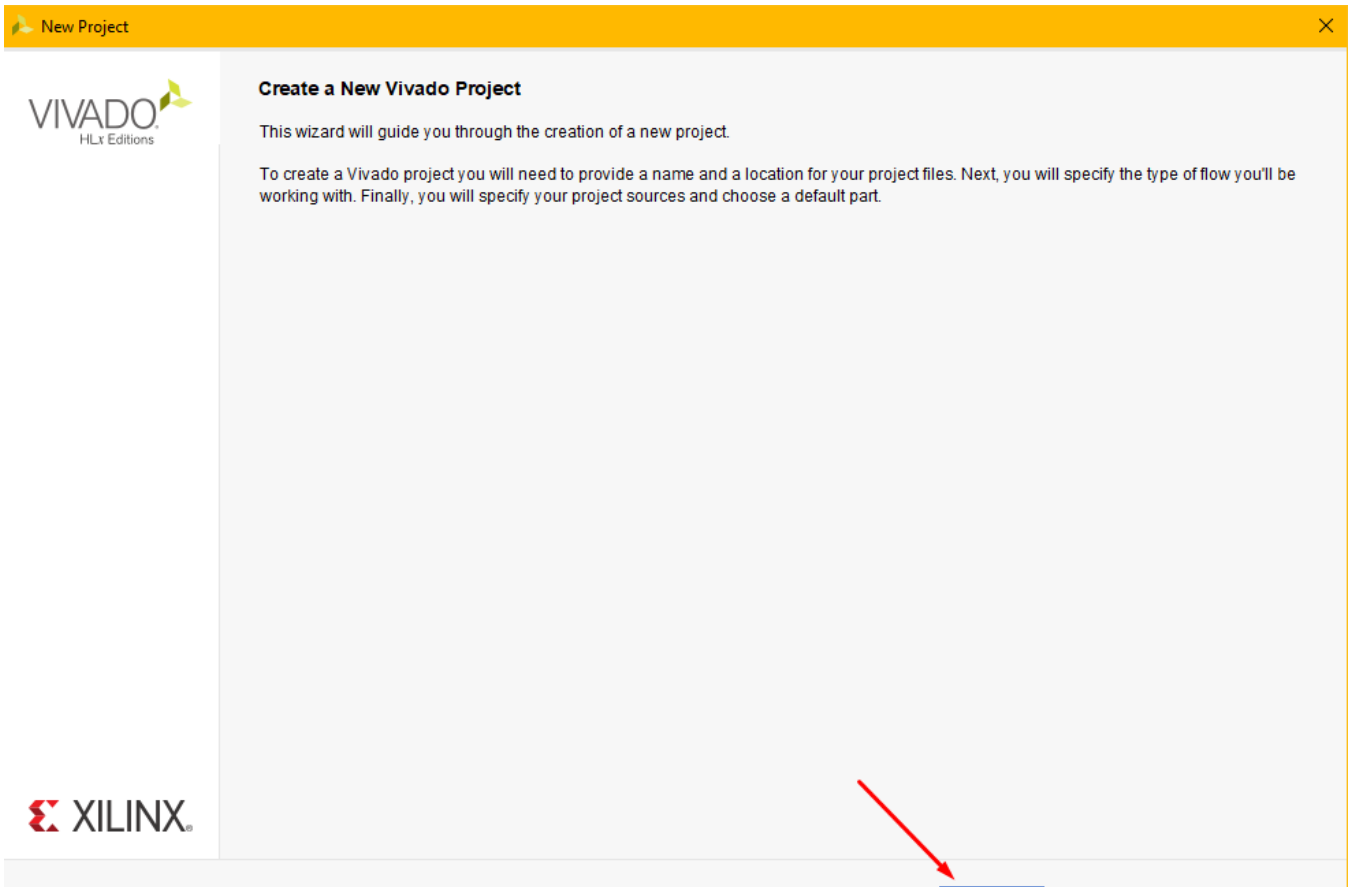
```
p_stimulus : process
    begin

        report "Stimulus process started" severity note;

        s_d <= "00" ;s_c <="00"; s_b <= "00"; s_a <= "00";
        s_sel <= "00"; wait for 100 ns;

        s_d <= "11" ;s_c <="00"; s_b <= "01"; s_a <= "00";
        s_sel <= "10"; wait for 100 ns;

        s_d <= "00" ;s_c <="00"; s_b <= "11"; s_a <= "10";
        s_sel <= "11"; wait for 100 ns;

        s_d <= "10" ;s_c <="01"; s_b <= "11"; s_a <= "10";
        s_sel <= "01"; wait for 100 ns;

        report "Stimulus process finished" severity note;
        wait;

    end process p_stimulus;

end testbench;
```

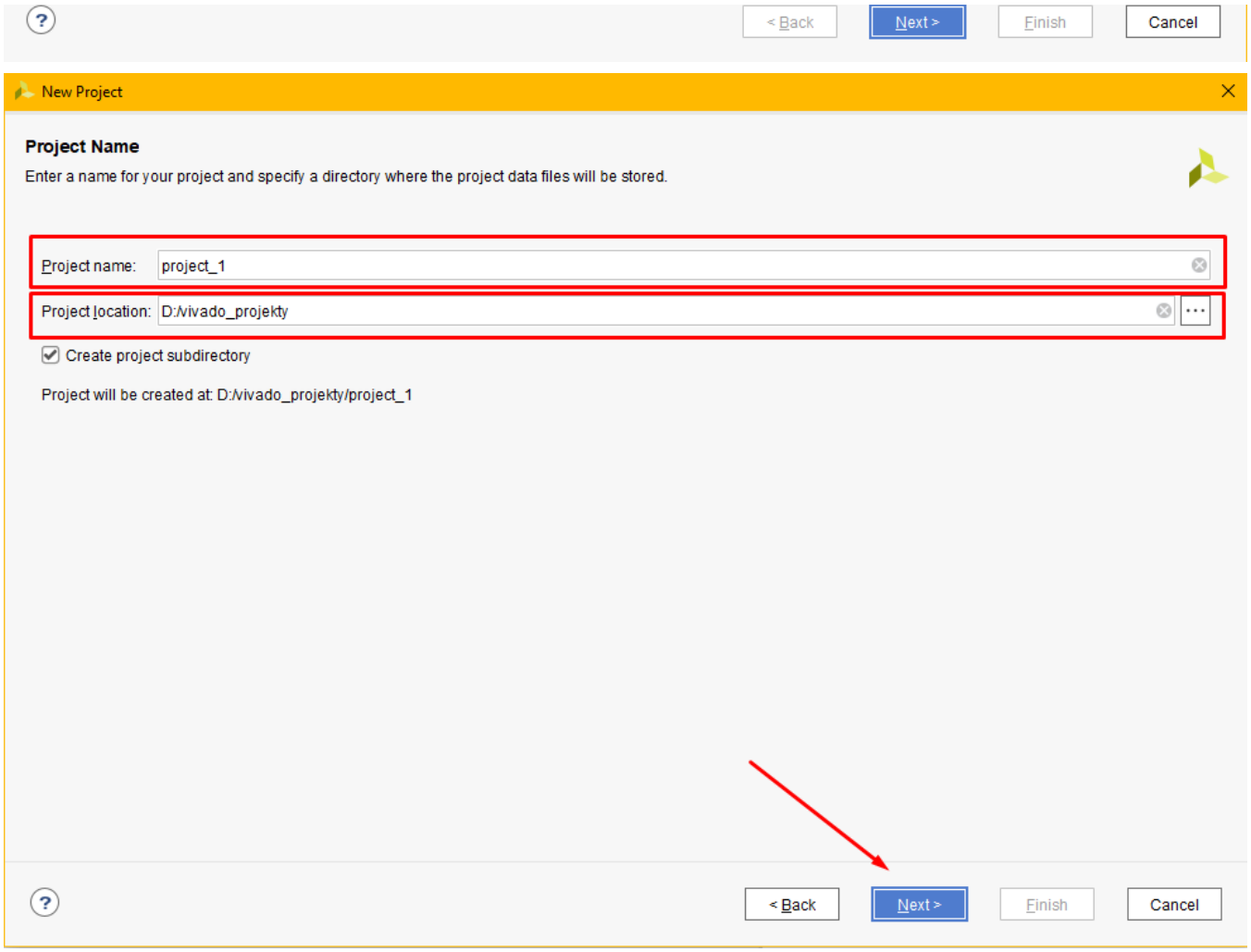
Screenshot with simulated time waveforms

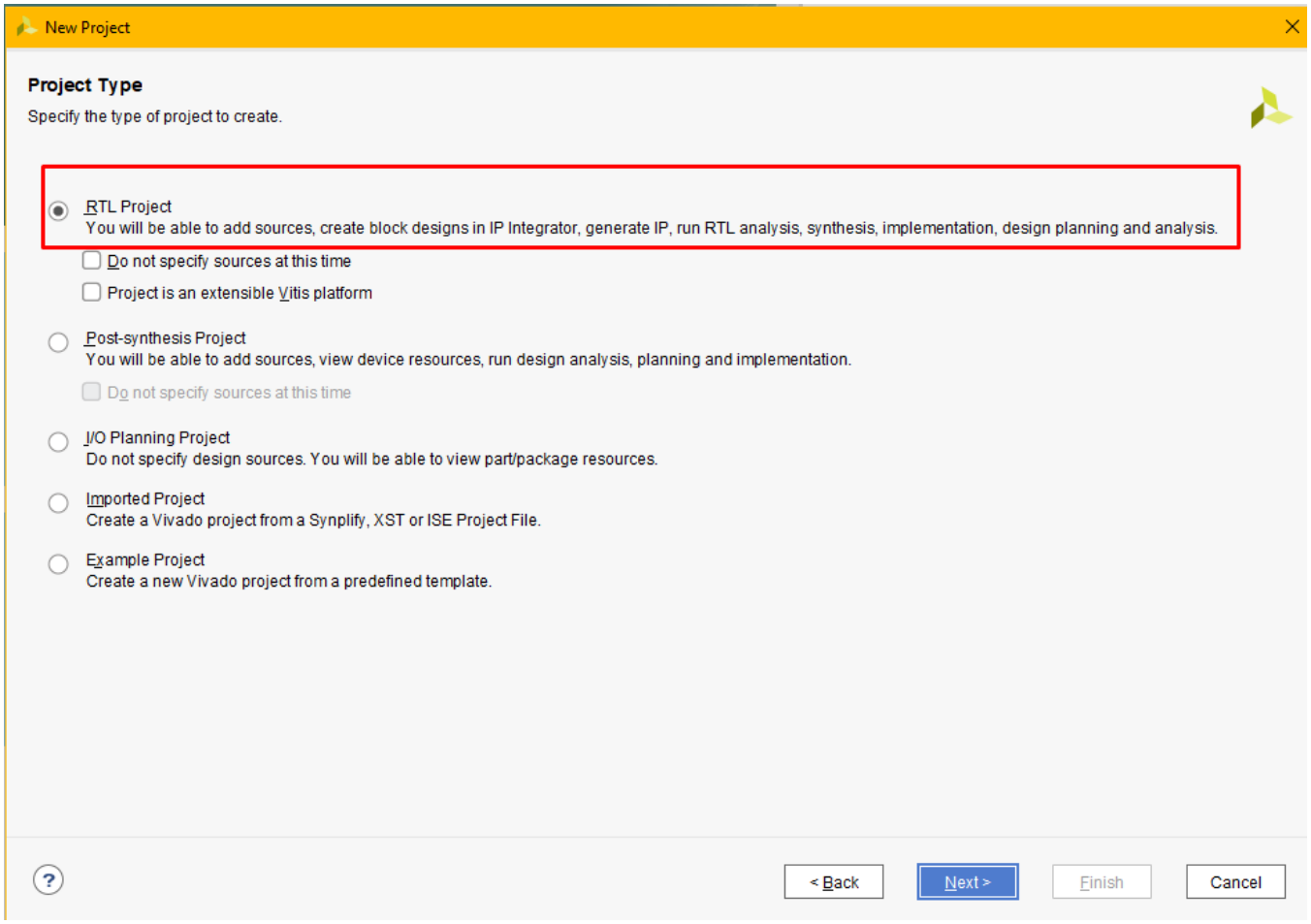


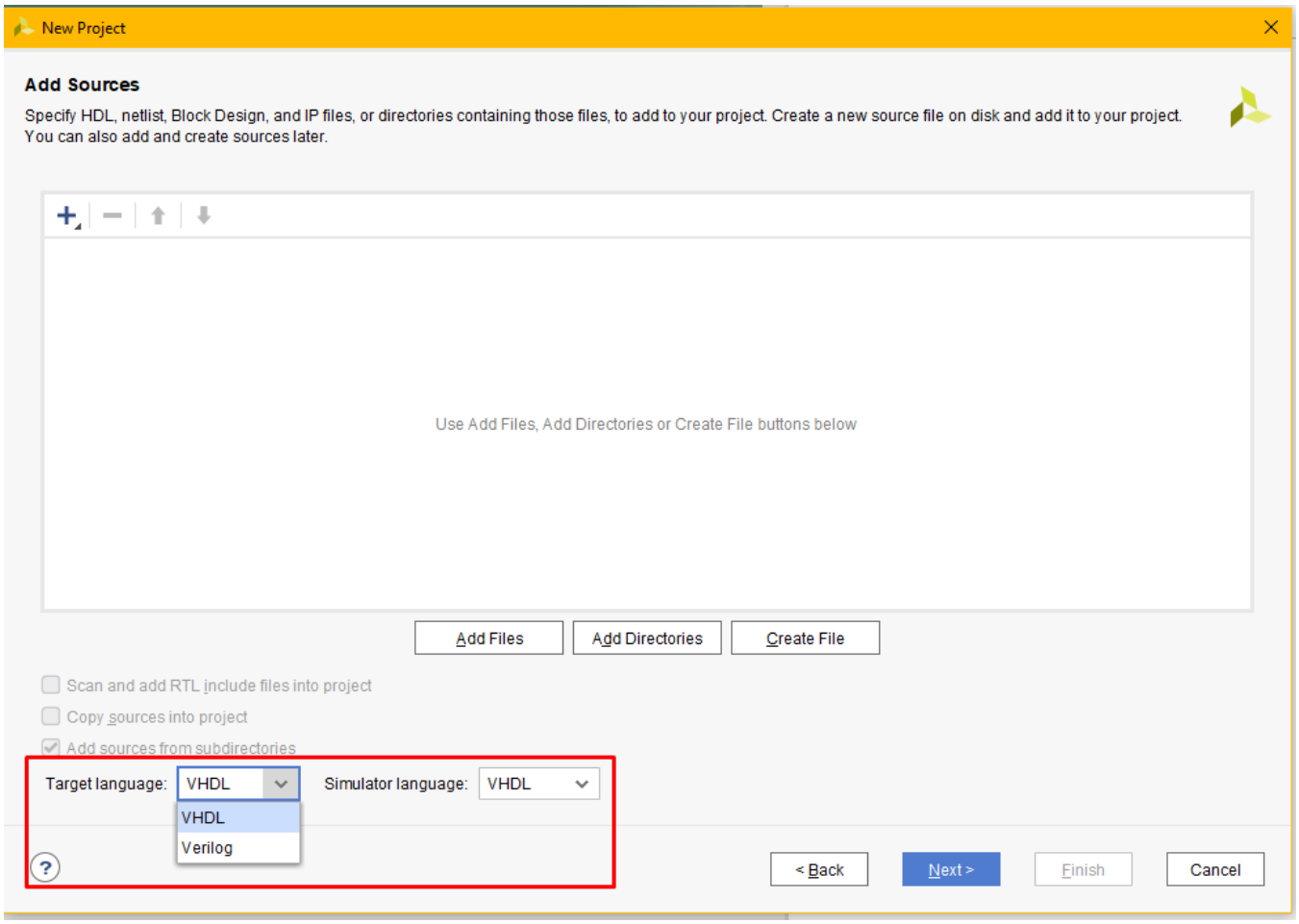
A Vivado tutorial

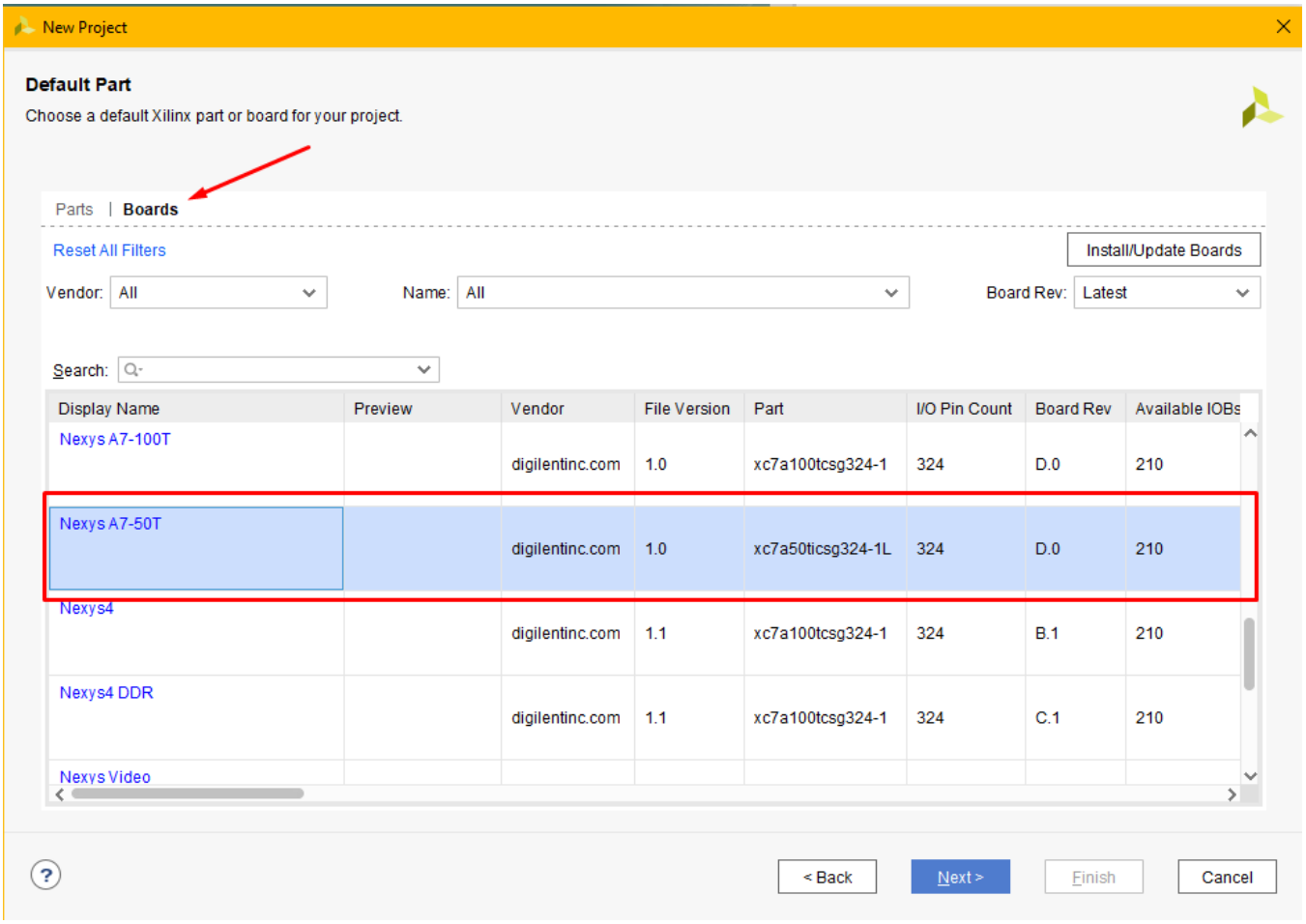

VIVADO
HLx Editions
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
XHub Stores
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide

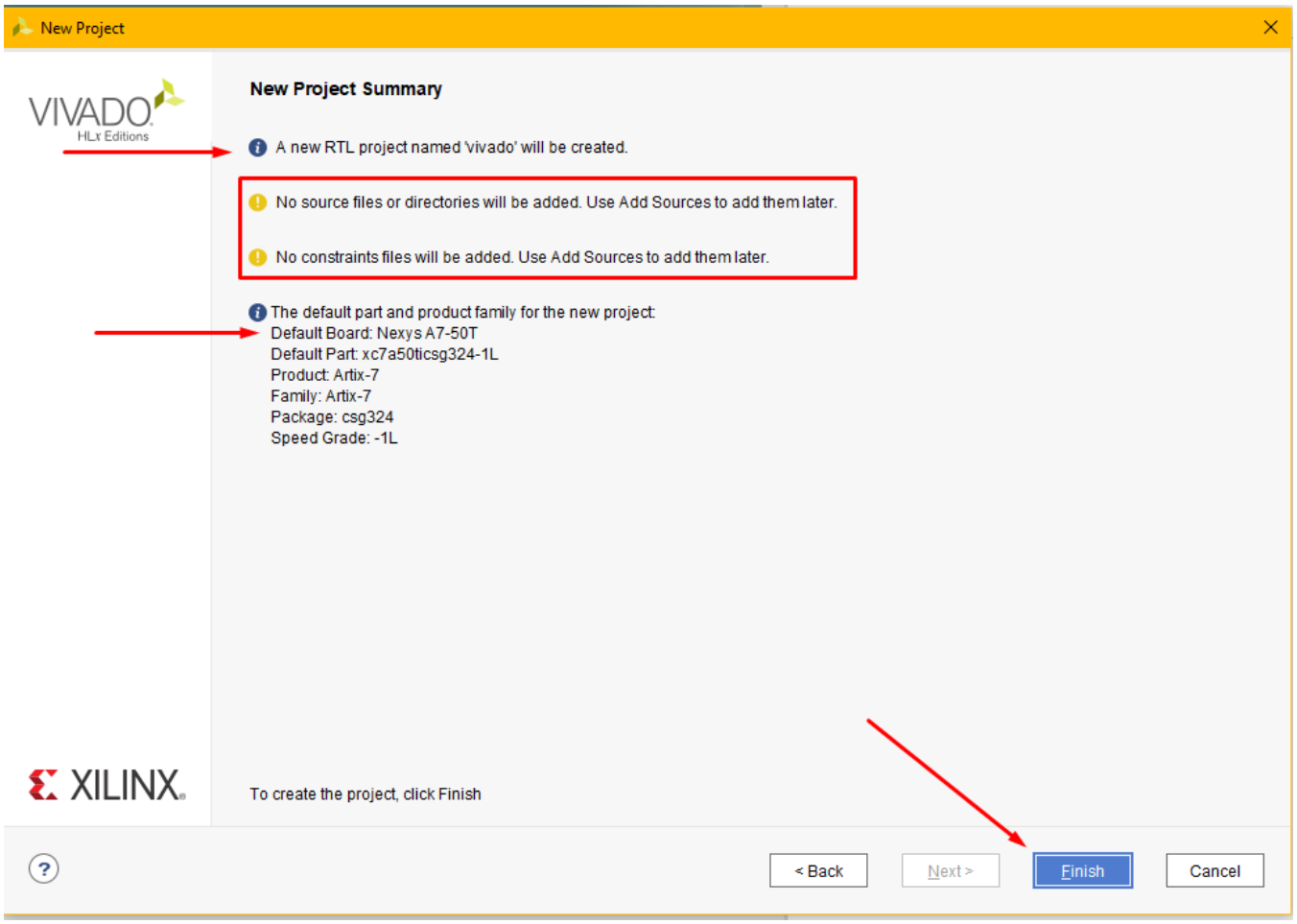

New Project
VIVADO
HLx Editions
Create a New Vivado Project
This wizard will guide you through the creation of a new project.
To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.
XILINX


< Back
Next >
Finish
Cancel
New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name: project_1
Project location: D:/vivado_projekty
Create project subdirectory
Project will be created at: D:/vivado_projekty/project_1
< Back
Next >
Finish
Cancel

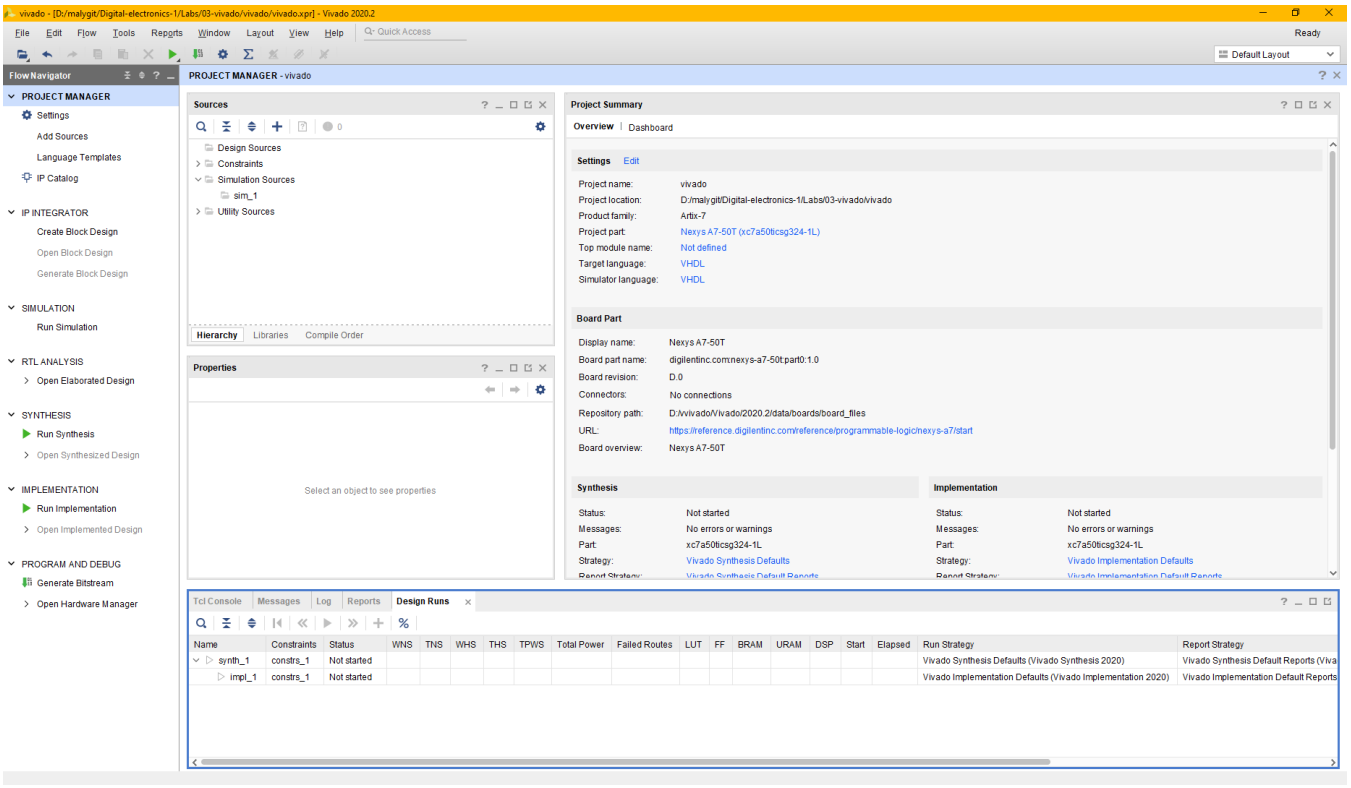

New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel


New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project.
You can also add and create sources later.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language:
VHDL
Verilog
Simulator language:
VHDL
< Back
Next >
Finish
Cancel


New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Install/Update Boards
Vendor: All
Name: All
Board Rev: Latest
Search:
Display Name
Preview
Vendor
File Version
Part
I/O Pin Count
Board Rev
Available IOBs
Nexys A7-100T
digilentinc.com
1.0
xc7a100tcsg324-1
324
D.0
210
Nexys A7-50T
digilentinc.com
1.0
xc7a50ticsg324-1L
324
D.0
210
Nexys4
digilentinc.com
1.1
xc7a100tcsg324-1
324
B.1
210
Nexys4 DDR
digilentinc.com
1.1
xc7a100tcsg324-1
324
C.1
210
Nexys Video
< Back
Next >
Finish
Cancel

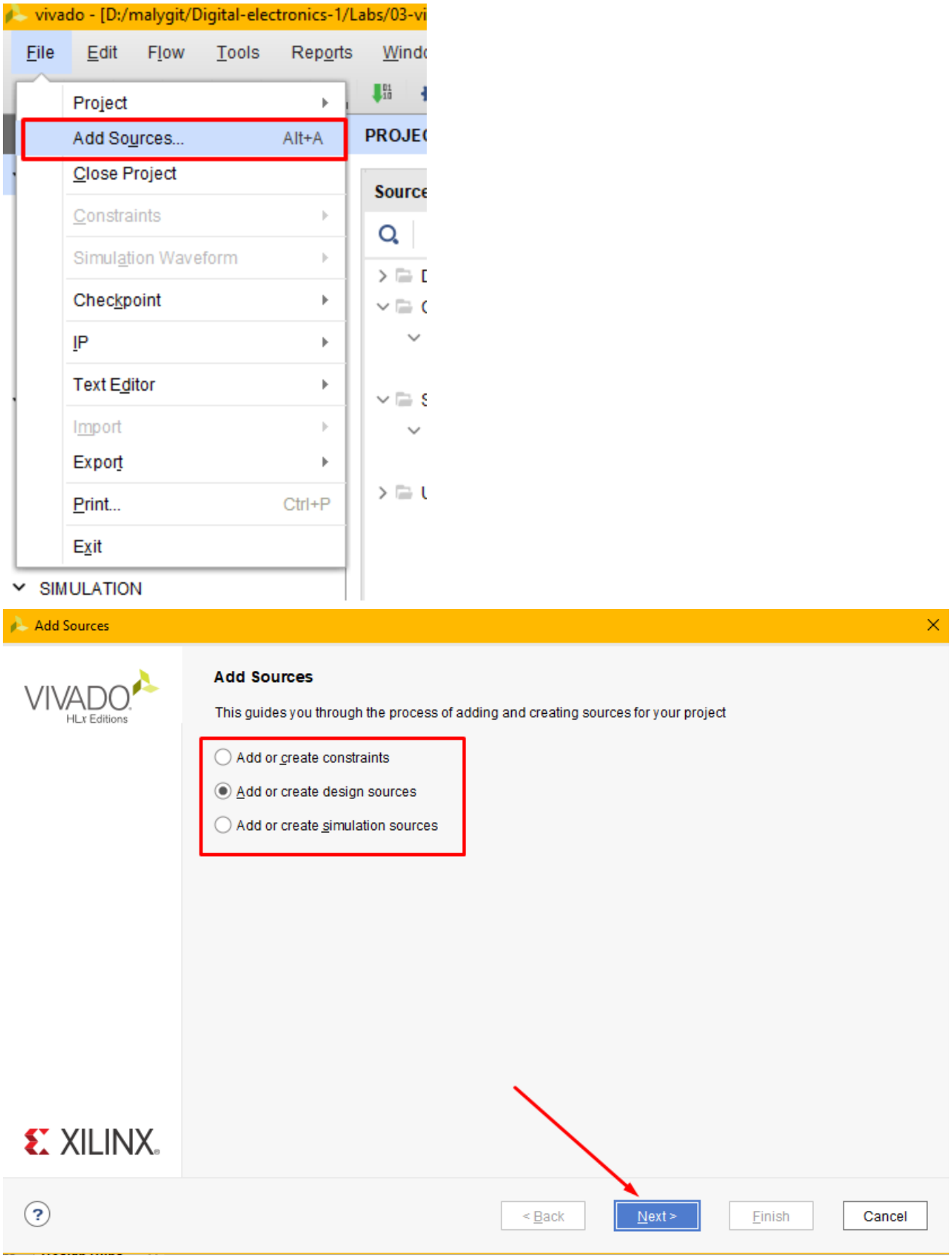


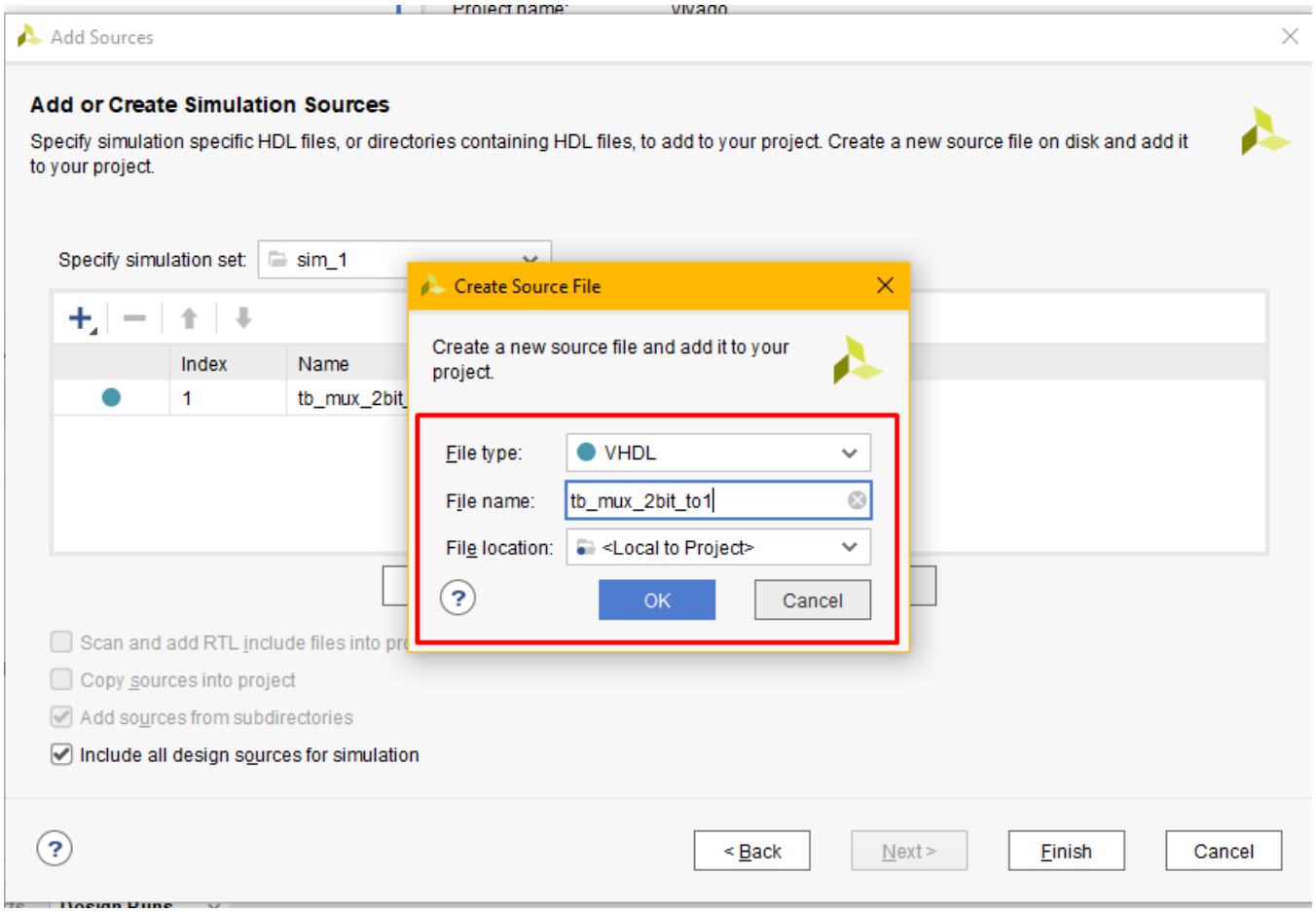
After sucessful creation of your project you will get into this window

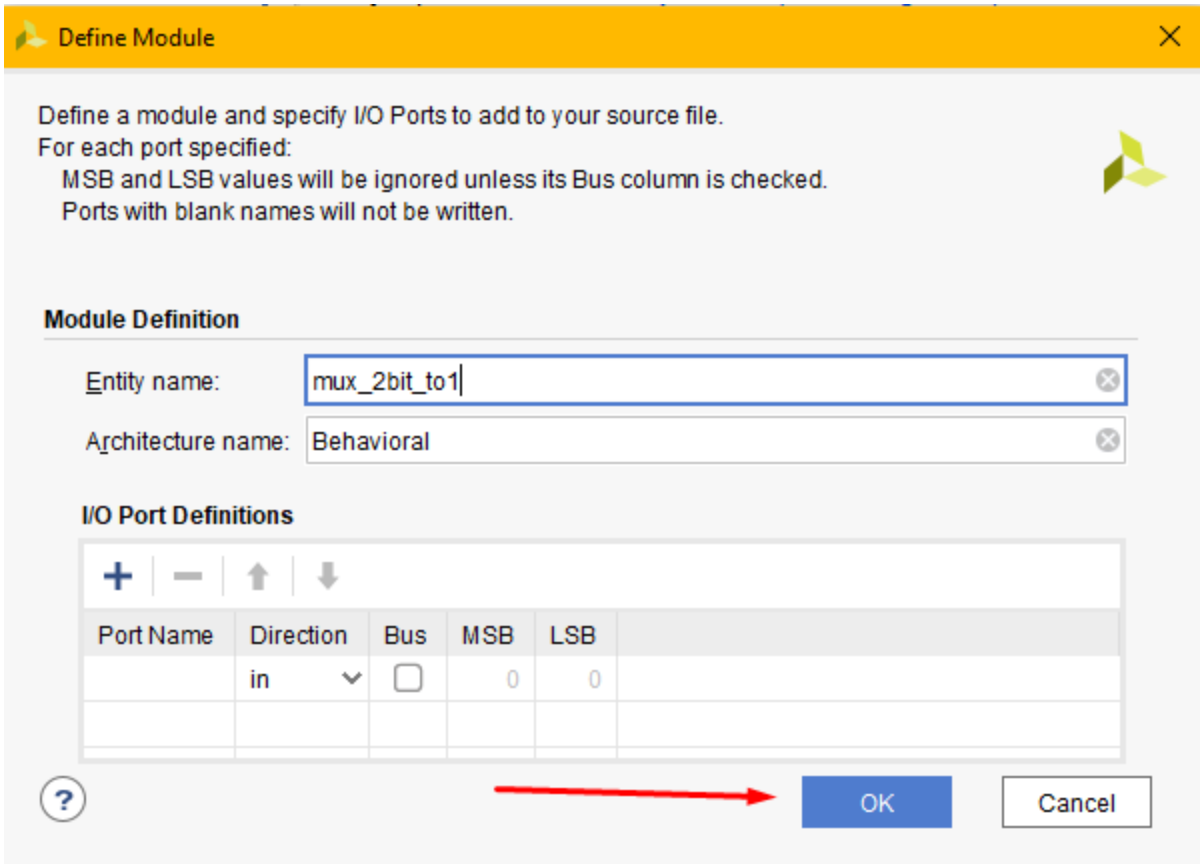


Now you must add/create testbench and design to your project, also constraints if needed

Steps for creating any of them are similar


vivado - [D:/malygit/Digital-electronics-1/Labs/03-vi
File
Edit
Flow
Tools
Reports
Project
Add Sources... Alt+A
Close Project
Constraints
Simulation Waveform
Checkpoint
IP
Text Editor
Import
Export
Print... Ctrl+P
Exit
SIMULATION
Add Sources
VIVADO
HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Index
Name
1
tb_mux_2bit_
Create Source File
Create a new source file and add it to your project.
File type:
VHDL
File name:
tb_mux_2bit_to1
File location:
<Local to Project>
OK
Cancel
Scan and add RTL include files into pr
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel


Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Entity name:
mux_2bit_to1
Architecture name:
Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
in
0
0
OK
Cancel

How to run simulation

After clicking `Run Behavioral Simulation`, program will start to process simulation (may take a moment), then new window with simulated waveforms, inputs and outputs will appear