

02 - Logic

[EDA Playground link for 2-bit comparator](#)

Dec. equivalent	B[1:0]	A[1:0]	B is greater than A	B equals A	B is less than A
0	0 0	0 0	0	1	0
1	0 0	0 1	0	0	1
2	0 0	1 0	0	0	1
3	0 0	1 1	0	0	1
4	0 1	0 0	1	0	0
5	0 1	0 1	0	1	0
6	0 1	1 0	0	0	1
7	0 1	1 1	0	0	1
8	1 0	0 0	1	0	0
9	1 0	0 1	1	0	0
10	1 0	1 0	0	1	0
11	1 0	1 1	0	0	1
12	1 1	0 0	1	0	0
13	1 1	0 1	1	0	0
14	1 1	1 0	1	0	0
15	1 1	1 1	0	1	0

$\text{equals_SoP} = m_0 + m_5 + m_{10} + m_{15} = (!b_1.!b_0.!a_1.!a_0) + (!b_1.b_0.!a_1.a_0) + (b_1.!b_0.a_1.!a_0) + (b_1.b_0.a_1.a_0)$

$\text{less_PoS} = M_0 \cdot M_4 \cdot M_5 \cdot M_8 \cdot M_9 \cdot M_{10} \cdot M_{12} \cdot M_{13} \cdot M_{14} \cdot M_{15} =$
 $= (b_1+b_0+a_1+a_0).(b_1+!b_0+a_1+a_0).(b_1+!b_0+a_1+!a_0).(b_1+b_0+a_1+a_0).(b_1+b_0+a_1+!a_0).$
 $(b_1+b_0+!a_1+a_0).(b_1+!b_0+a_1+a_0).(b_1+!b_0+a_1+!a_0).(b_1+!b_0+!a_1+a_0).(b_1+!b_0+!a_1+!a_0)$

Karnaugh maps for 2-bit

greater
SOP

SOP

$b_1 b_0$

		$a_1 \ a_0$			
		00	01	11	10
00					
01	1				
11	1	1			1
10	1	1			

less

POS

less $a_1 a_0$

POS

	00	01	11	10
00	0			
01	0	0		
11	0	0	0	0
10	0	0		0

$$\text{greater_SOP} = b_1 \bar{a}_1 + b_0 \bar{a}_1 \bar{a}_0 + b_1 b_0 \bar{a}_0$$

$$\text{less_POS} = (a_1 + a_0) \cdot (\bar{b}_1 + \bar{b}_0) \cdot (\bar{b}_1 + a_1) \cdot (\bar{b}_0 + a_1) \cdot (\bar{b}_1 + a_0)$$

		$A1 \ A0$			
		00	01	11	10
$B1 \ B0$	00	1	0	0	0
	01	0	1	0	0
	11	0	0	1	0
	10	0	0	0	1

4-bit comparator

EDA Playground link for 4-bit comparator

```

95     assert ((s_b_greater_A = '0') and (s_b_equals_A = '1') and (s_b_less_A = '0'))
96     report "Test failed for input combination: 1000, 1000" severity error;
97
98     s_b <= "1011"; s_a <= "1101"; wait for 100 ns;
99     assert ((s_b_greater_A = '0') and (s_b_equals_A = '1') and (s_b_less_A = '0'))
100    report "Test failed for input combination: 1011, 1101" severity error;
101
102
103    -- WRITE OTHER TESTS HERE
104
105
106    -- Report a note at the end of stimulus process
107    report "Stimulus process finished" severity note;
108    wait;
109 end process p_stimulus;
110
111 end architecture testbench;
112

```

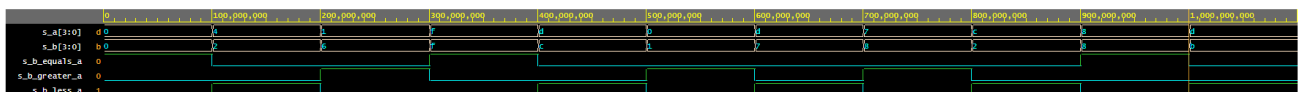
Log

Share

```

[2021-02-17 06:54:04 EST] ghdl -i design.vhd testbench.vhd && ghdl -m tb_comparator_2bit && ghdl -r tb_
analyze design.vhd
analyze testbench.vhd
elaborate tb_comparator_2bit
testbench.vhd:51:9:@0ns:(report note): Stimulus process started
testbench.vhd:99:16:@1100ns:(assertion error): Test failed for input combination: 1011, 1101
testbench.vhd:107:9:@1100ns:(report note): Stimulus process finished
Finding VCD file...
./dump.vcd
[2021-02-17 06:54:05 EST] Opening EPWave...
Done

```



VHDL testbench

```

p_stimulus : process
begin

    report "Stimulus process started" severity note;

    s_b <= "0000"; s_a <= "0000"; wait for 100 ns;
    assert ((s_b_greater_A = '0') and (s_b_equals_A = '1') and (s_b_less_A
= '0'))
    report "Test failed for input combination: 0000, 0000" severity error;

    s_b <= "0010"; s_a <= "0100"; wait for 100 ns;
    assert ((s_b_greater_A = '0') and (s_b_equals_A = '0') and (s_b_less_A
= '1'))
    report "Test failed for input combination: 0010, 0100" severity error;

    s_b <= "0110"; s_a <= "0001"; wait for 100 ns;
    assert ((s_b_greater_A = '1') and (s_b_equals_A = '0') and (s_b_less_A
= '0'))
    report "Test failed for input combination: 0110, 0001" severity error;

```

```

        s_b <= "1111"; s_a <= "1111"; wait for 100 ns;
        assert ((s_B_greater_A = '0') and (s_B_equals_A = '1') and (s_B_less_A
= '0'))
        report "Test failed for input combination: 1111, 1111" severity error;

        s_b <= "1100"; s_a <= "1101"; wait for 100 ns;
        assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less_A
= '1'))
        report "Test failed for input combination: 1100, 1101" severity error;

        s_b <= "0001"; s_a <= "0000"; wait for 100 ns;
        assert ((s_B_greater_A = '1') and (s_B_equals_A = '0') and (s_B_less_A
= '0'))
        report "Test failed for input combination: 0001, 0000" severity error;

        s_b <= "0111"; s_a <= "1101"; wait for 100 ns;
        assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less_A
= '1'))
        report "Test failed for input combination: 0111, 1101" severity error;

        s_b <= "1000"; s_a <= "0111"; wait for 100 ns;
        assert ((s_B_greater_A = '1') and (s_B_equals_A = '0') and (s_B_less_A
= '0'))
        report "Test failed for input combination: 1000, 0111" severity error;

        s_b <= "0010"; s_a <= "1100"; wait for 100 ns;
        assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less_A
= '1'))
        report "Test failed for input combination: 0010, 1100" severity error;

        s_b <= "1000"; s_a <= "1000"; wait for 100 ns;
        assert ((s_B_greater_A = '0') and (s_B_equals_A = '1') and (s_B_less_A
= '0'))
        report "Test failed for input combination: 1000, 1000" severity error;

        s_b <= "1011"; s_a <= "1101"; wait for 100 ns;
        assert ((s_B_greater_A = '0') and (s_B_equals_A = '1') and (s_B_less_A
= '0'))
        report "Test failed for input combination: 1011, 1101" severity error;

        report "Stimulus process finished" severity note;
        wait;
    end process p_stimulus;

```

VHDL design

```

architecture Behavioral of comparator_2bit is
begin

```

```
B_greater_A_o <= '1' when (b_i > a_i) else '0';  
  B_equals_A_o <= '1' when (b_i = a_i) else '0';  
  B_less_A_o   <= '1' when (b_i < a_i) else '0';  
  
end architecture Behavioral;
```